NASA CR-

147590

(NASA-CR-147590) HARDWARE SIMULATION OF Ku-BAND SPACECRAFT RECEIVER AND BIT SYNCHRONIZER, VOLUME 1 (LinCom Corp., Pasadena, Calif.) 105 p HC $5.50 CSCL 17B

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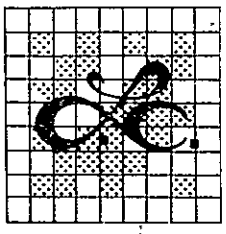

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HARDWARE SIMULATION OF KU-BAND SPACECRAFT RECEIVER AND BIT SYNCHRONIZER

VOLUME I

Prepared for

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MARCH 1976

TR-03-7506-7

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ACKNOWLEDGEMENT

The authors wish to thank Mr. Jack Seyl and Dr. Jack Sheppard of the Johnson Spacecraft Center and Dr. Phillip M. Hopkins of Lockheed for their support and participating in various stimulating discussions throughout the contract period.

HARDWARE SIMULATION OF KU-BAND SPACECRAFT RECEIVER AND BIT SYNCHRONIZER

VOLUME I: SYSTEM ENGINEERING AND TRADE-OFF ANALYSIS

VOLUME II: HARDWARE SIMULATION

VOLUME III: COMPUTER PROGRAM DOCUMENTATION

This three volume report documents the work accomplished during Phase I of the Contract Number NAS 9-14636. The system architecture and trade-off analysis that led to the selection of the system to be simulated is presented in Volume I. The construction of results obtained from the hardware simulation are described in Volume II. A high level software description is also presented in this volume. A detailed software documentation of the computer programs are to be found in the appendices of Volume III.

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MARCH 1976

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GLOSSARY OF SYMBOLS AND ABBREVIATIONS

The following symbols and abbreviations are used throughout this report. They are defined here for convenience and clarity.

PNSS	Pseudo Noise Synchronization Subsystem
CSS	Carrier Synchronization Subsystem
SSS	Symbol Synchronization Subsystem
DLL	Delay-Locked Loop
VCO	Voltage Controlled Oscillator
R_s	Energy-Per-Symbol to Noise Ratio
$\mathcal{R}_s$	Symbol Data Rate
R_r	VCO Effective Sweep Rate
α	Probability of False Alarm
β	Probability of Missed Sync Detection
Th	Threshold
T_1	PN Dwell Time or Integration Time
B_i	Bandwidth of Costas Arm Filters
B_L	Costas Loop Bandwidth
$R_{PN}(\tau)$	Correlation Function of PN Code
$R_{xy}(\tau)$	Cross-Correlation Function of PN Code and RF/IF Filter Output
N_0	Single-Sided Noise Spectral Density
C	Average Carrier Power
C/N_0	Carrier-to-Noise Density Ratio
$\mathcal{L}_L$	Squaring Loss
D	Filter Distortion
τ_s	Lock Detector Filter Integrate Time
ϕ	Loop Phase Error
Δ	Duration of a Code Chip
PN	Pseudo-Noise

GLOSSARY OF SYMBOLS AND ABBREVIATIONS (Cont'd)

BPSK	Binary Phase Shift Keying
IF	Intermediate Frequency
RF	Radio Frequency
TDRS	Tracking and Data Relay Satellite
P_E	Symbol Error Probability
δ	Ratio of Symbol Data Rate to Loop Bandwidth
σ_t	τ-dither loop jitter
Bi-ϕ	Bi-Phase or Manchester Baseband Modulation
T	Symbol Duration
AGC	Automatic Gain Control
PLL	Phase Locked Loop
LO	Local Oscillator
"I"	Signal Appearing in Phase Arm of Costas Loop
"Q"	Signal Appearing in the Quadrature Arm of Costas
d(t)	Channel Doppler Profile
e	Sweep Voltage Waveform
$N_{eq}(t)$	Equivalent Phase Noise in Costas Loop
K_V	VCO Gain Constant
K_m	Phase Detector Gain Constant
$A^2=S$	Received Signal Power
F(p)	Loop Filter Transfer Function
G(p)	Costas Arm Filter Transfer Function
τ	PN Jitter Variable
g	AGC Gain Fluctuation
NRZ	Nonreturn to Zero Waveform
m(t)	Data or Message Waveform
$\Omega_0=2\pi\Delta f$	Doppler Uncertainty
Ω_1	Doppler Rate
$s_{PN}(t)$	PN Modulation
$n_i(t)$	Receiver Input Noise

GLOSSARY OF SYMBOLS AND ABBREVIATIONS (Cont'd)

ρ	Costas Loop Signal-to-Noise Ratio
$S_m(f)$	Power Spectral Density of Manchester
$\sigma_{2\phi}$	Costas Loop Phase Jitter
$\bar{S}$	Cycles Slipping Rate
T_a	Time to Sweep Uncertainty Band
FP	Frazier-Page
$\overline{T}_{acq}$	Average Acquisition Time
T_{90}	Time to Acquire Carrier with 90% Probability
$\sigma_{T_{acq}}$	Standard Deviation of Acquisition Time
V_{Th}	Threshold Voltage
φ_{ss}	Steady State Phase Error

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VOLUME III

OBJECTIVES

LINCOM's overall objective under this contract was to develop a hardware simulation which emulates an automatically acquiring transmit receive spread spectrum communication and tracking system that appears to be candidate for use in future NASA programs involving digital communications.

Since the frequencies, bit rates, modulation formats, and overall system concepts and operations on evolving NASA programs may be new to space hardware, and since the link margins are low, a number of potential pitfalls and mutual interacting problem areas will be sure to occur. Low margins in any telecommunication system are always dangerous owing to the impact they may have on redesign of payloads, platform antenna configuration, etc. In order to minimize expensive redesign and avoid changes in system test and verification procedures with actual equipment, it is highly desirable that these be resolved and uncovered prior to final hardware fabrication.

It is felt that the hardware simulation developed under this contract will identify and validate these intolerable losses in link margins, where they occur, and how they can be avoided. The simulation will allow for concept and/or parameter variations to optimize overall system performance and resolve such things as the acquisition and tracking problems encountered on Skylab prior to the actual construction of hardware. In addition, the simulation will be useful in validating actual hardware performance and demonstrate results when analysis cannot be made or verified.

The simulation was developed under the constraints of assuming a fixed network operation, the system must be real world implementable, it must be cost effective, the program execution time must not be excessive, the modulation technique is PN/Bi-ϕ/BPSK, and optimum performance is desirable.

SCOPE

Due to funding limitations, the overall goals and objectives described above are to be attained through a multiphase effort. This three volume report presents the results obtained during the first phase. The second phase of the program is designed to efficiently blend and extend the results obtained in this first phase effort in the most timely and cost effective manner.

SUMMARY

Performance

Symbol error rate performance will be degraded from theoretical by .94 dB at the system design point C/N_0 of 51.3 dB-Hz. A 4 pole Chebyshev filter accounts for .33 dB of this loss with another .3 dB attributed to both loops and the remaining .31 dB associated with the 2nd IF filter. Loss due to an IF filter is included because it is felt that one will be required from an actual hardware implementation point of view.

The composite receiver acquisition performance study is not completed at this time. Information at hand indicates that the system will have no trouble acquiring sync at our design point C/N_0 of 51.3 dB-Hz with average acquisition times being slightly better than that predicted analytically. At lower C/N_0 values the time-shared delay locked loop limits performance, but even so, acquisition times under worst case doppler conditions will be better than expected.

Quoted performance is based on algorithms selected for implementation that have assumed an absence of hardware imperfections. Caution is advised since performance, particularly during acquisition, is extremely sensitive to degradations. When the extent and types of hardware imperfections are known, it is suggested that they be included in the simulation and that the algorithms be accordingly reoptimized.

Recommendations for Further Study

The software breadboard was carefully constructed with simulated and theoretical results being cross checked at both the subsystem and system level. Results at the subsystem level, and in most cases those on a system level, are in excellent agreement. There were three areas, however, where the analytical and simulated data differed. Over a range of C/N_0 values measured Costas loop phase jitter was slightly better than predicted. This is not surprising since loop jitter performance at low signal-to-noise ratios requires the use of the nonlinear loop model for predicting performance. Since no exact theory is known for predicting jitter in second-order loops, mathematical approximations were required in order to predict results. Code loop phase jitter was worse than predicted by the theory at low toggling rates; however, at higher toggling rates, i.e., low BT products. Theory and simulation results were in good agreement. Again,

the theory developed is approximate at high BT products and it is expected not to give accurate predictions of the true jitter. In addition, the analytical evaluation of carrier acquisition times were not in as close agreement as one would desire; this no doubt is due to the fact that one cannot manipulate with exactness the nonlinear transients generated by the loop in noise.

Mathematical formulations required to evaluate performance in these three areas were of necessity made at a system level. The nonlinear, statistical nature of the closed form expressions, accounting for a multiplicity of mixers, filters, samplers, and etc., made exact calculations of the real world system difficult. Modeling and other approximations necessary to obtain expressions capable of being solved analytically resulted in reduced accuracy. It is felt that additional analysis to improve accuracy is both feasible and warranted. The simulation would serve as a useful adjunct in supporting this type of state-of-the-art effort.

Information currently available indicates that code acquisition times, limited by time-shared delay-locked loop performance, will establish the range of C/N_0 values required for acceptable system operation. Additional studies to improve code loop performance, particularly in the area of bandwidth reduction techniques, could prove fruitful. Improved operation through a reoptimization of the PN acquisition algorithms to account for the code loop/PN correlation process interactions may also be possible and should be studied in more detail.

The issue of selecting an optimum RF filter design has not been resolved. A truly optimum design was beyond the scope of this report as it is a study unto itself involving detailed evaluation and trade-offs between RF front end rejection requirements and PN acquisition/tracking behavior. This needed information is not available in the current open literature.

It is recommended that the degradations and distortions introduced in the TDRS be investigated. These include AM to PM conversion effects, potential effects due to intersymbol interference generated in the code chips and the effects of nonlinearities in the TWT.

A final area where further study is recommended will be touched on but briefly. It is, however, one which has the greatest potential when it comes to using the software breadboard in support of a hardware test facility and in the design and specification of future systems. This broad area involves studying the effects that various hardware degradations, algorithms, and

nonlinearities such as bandpass limiters have on performance. These documents were written, it is hoped, in a manner which demonstrates to our readers that simulation techniques can be successfully used in supporting such studies.

Issues of Concern

Five technical problems have not been resolved in Phase I. They are:

1. Effects of carrier sweep on PN tracking performance; particularly its impact on establishing the noise estimate.
2. Degradations associated with a realistic bit synchronizer implementation capable of tracking the signal in deep noise.
3. Transient behavior of the system under signal fades and antenna switching conditions.
4. Correlation associated with realizable loops reducing the coding gain of the maximum likelihood type Viterbi decoder.
5. Reoptimization of algorithms to account for hardware degradations.

The first three issues will be resolved by LINCOM during the Phase II effort. Item No. 4 is a LINCOM design goal but could easily be studied by JSC personnel using their existing coder/decoder programs as only a minimal understanding of the delivered software is required. It is expected that Item No. 5 will be resolved by NASA personnel with LINCOM support.

1.0 Background

The telecommunication services required to support the Skylab program generically involved communications and tracking between a multiplicity of ground stations and a Spacecraft. The Skylab communication design utilized a manual acquisition procedure. Frequent hand-overs between ground stations and the moving platform and the resultant loss of lock and manual reacquisition required, proved to be an extremely serious problem.

A manual acquisition procedure will be an even greater problem for future NASA programs which are sure to involve a larger network of ground stations, repeater satellites and orbiting platforms. The problem will be further compounded by the fact that new modulation and coding techniques as well as new areas in the radio frequency spectrum will be exploited in the future.

Manchester encoding of NRZ baseband signals and QPSK modulation in the Ku frequency band are sure to be of interest in the future. In some cases involving satellite links, the transmitter will be required to use an additional layer of modulation called spread spectrum modulation in order to meet CCIR flux density requirements. Two-way channels, in which the carrier is suppressed, will need to be established and these are new with respect to operation of Earth/Platform/Earth type links. To meet the increasing data transfer rate requirements expected on future programs with minimum cost and system stress, and to provide adequate system margin, some form of error control is required and therefore the links will be coded.

Coded links operate with very low signal-to-noise ratios and will make a Skylab type manual acquisition procedure nearly, if not completely, impossible. Thus, it is apparent that evolving NASA programs, having significantly increased communication

sophistication relative to the Skylab requirements, will need to be provided with an automatically acquiring receive system that will make operator intervention unnecessary in the event of loss of lock.

1.1 Hardware Simulation Purpose

The purpose of the hardware simulation is several fold. It allows for: (1) the evaluation of overall system performance due to dynamical subsystem interactions not analytically tractable, (2) the evaluation of overall system performance during antenna switching and other types of signal dropouts, (3) the optimization of overall system performance through the use of an initial concept stage followed by a development and system integration stage (which can lead to the suggestion of alternatives). In addition, a hardware simulation can be used to identify hardware implementation problems early so as to cost effectively circumvent these in a final design; it can also provide a mechanism to support hardware testing.

1.2 Hardware Simulation Potential

This report is written with the hope of demonstrating to the reader the potential of a hardware simulation developed by experienced communication engineers. Over the duration of the Phase I effort the program has been used:

(1) To characterize and verify overall system performance degradations in a dynamical physical model;

(2) To study and evaluate mutual interactions and degradations among subsystem interfaces;

(3) To evaluate analytically nontractable design and system problems, e.g., sync acquisition and detection algorithms, degradations;

(4) To verify and guide hardware design so as to avoid expensive redesign;

(5) To emulate and evaluate varying channel conditions and effects;

(6) To serve as an aid in advanced system planning and/or evaluation;

(7) To support the evaluation, modification, and testing of actual space hardware.

2.0 Functional Diagram of the System

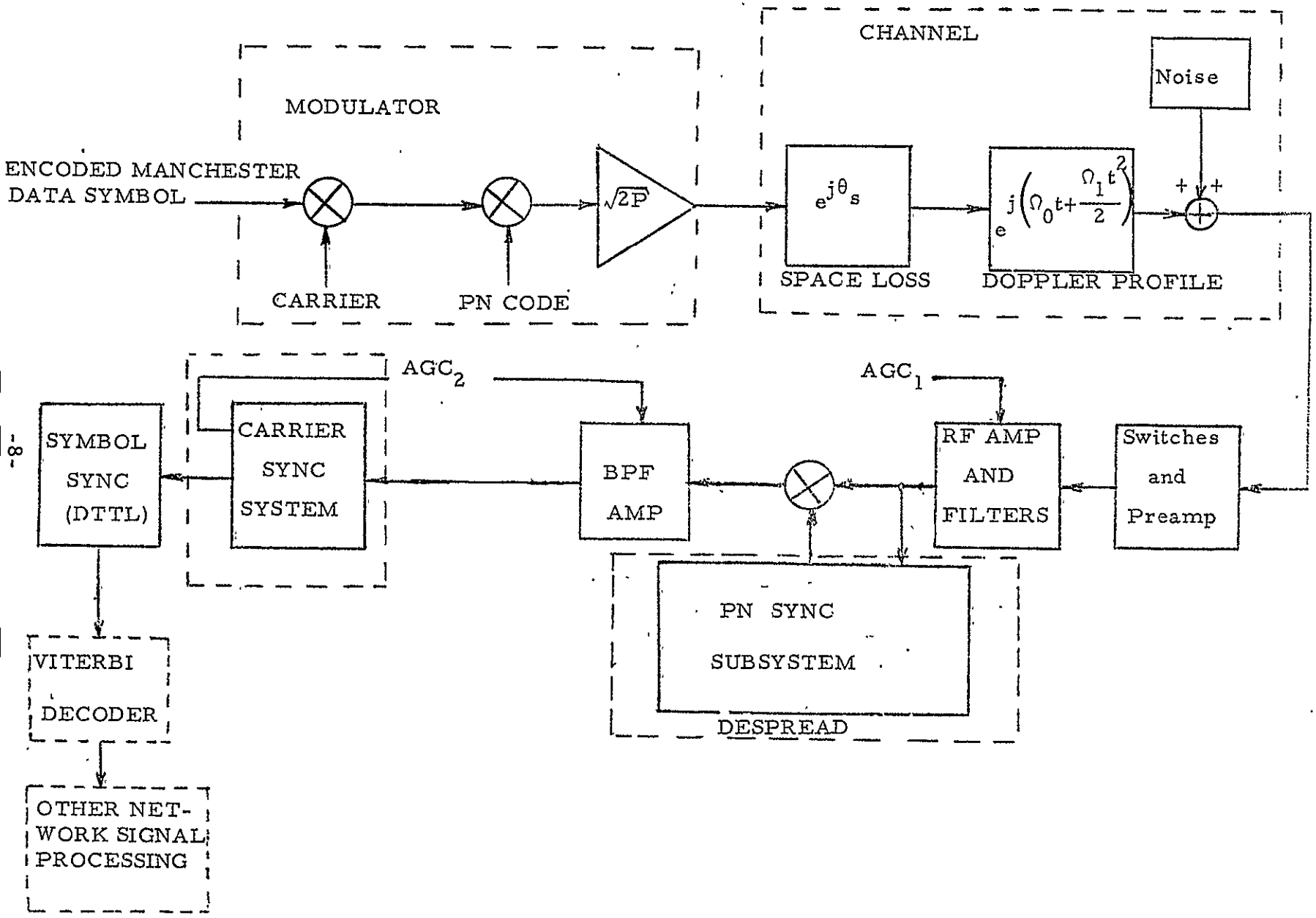
Fig. 2-1 serves to illustrate a high level functional diagram of the system to be simulated. It consists of several major subsystems. These include, see Fig. 2-1, the modulator, the channel, the RF front end, the PN sync subsystem, the carrier sync subsystem, the symbol sync subsystem, the AGC subsystem, the Viterbi decoder and other network signal processing. During this, the first phase of the program, software has been developed which serves to emulate the modulator, the channel, the AGC's, the RF/IF front end, the PN Sync Subsystem, (PNSS), and the Carrier Sync Subsystem (CSS). These programs have been developed for the most commonly used modulation technique in digital communications, viz., binary phase shift keying (BPSK) which has been spread by a PN sequence. LINCOM has performed a combination of analytical and computer simulation experiments to obtain what it considers to be the optimum realizable algorithms for each of the following:

(1) PN Code Acquisition and Tracking Subsystem.

(2) Carrier Acquisition and Tracking Subsystem.

In addition, LINCOM has: (1) performed the appropriate analysis to support and verify the result simulation programs, (2) evaluated the resulting acquisition performance for each of the subsystems, (3) integrated the PN Sync and Carrier Sync Subsystem package into a composite computer simulation suitable for evaluating and verifying end-to-end symbol error rate performance.

Figure 2.1. FUNCTIONAL BLOCK DIAGRAM OF SPREAD SPECTRUM MODULATOR/CHANNEL/RECEIVER FOR ORBITER



3.0 Block Diagram Description of the Spread Spectrum BPSK Receiver Simulated

The receiver configuration of Figure 3-1 was selected for simulation based on the series of system architecture and trade-off studies that will be discussed in Sections 4, 5 and 6 of this volume. Major subsystems include the: (1) Channel and Modulator (not shown), (2) RF and AGC Front End, (3) PN Sync Sybsystem (PNSS), (4) Carrier Sync Subsystem (CSS), (5) Carrier Lock Detection Subsystem, (6) Carrier Sync Acquisition Circuit, (7) Symbol Synchronization Subsystem, and (8) the Viterbi Decoder. The design philosophy used in partitioning the system is summarized below:

- Rapid Acquisition Carrier Sync System
- Despreading Process Independent of Carrier Acquisition and Tracking and Modulation
- Data Detection Independent of Despreading Process

The RF input, viz., a Manchester Encoded/BPSK/Spread Carrier with nominal frequency of 2 GHz, is first processed via an RF filter. The bandwidth of this filter must be sufficiently wide to pass the PN chips and the roll off must be sufficient to meet the desired rejection requirements. The details of the design and performance can be found in the RF filter design section contained in Section 7 of this volume and in Volume II.

The signal level into the first IF mixer is held constant by the noncoherent AGC_1. The first LO is selected to run at 1.6 GHz; therefore, the first IF frequency, at zero Doppler, is 400 MHz. The output of the first IF mixer is further filtered by the first IF filter whose bandwidth is sufficiently wide to pass the PN chips. The cascaded frequency response of the RF filter and the first IF filter are collectively designed to meet the desired front end rejection requirements.

The first IF frequency is translated to the second IF frequency

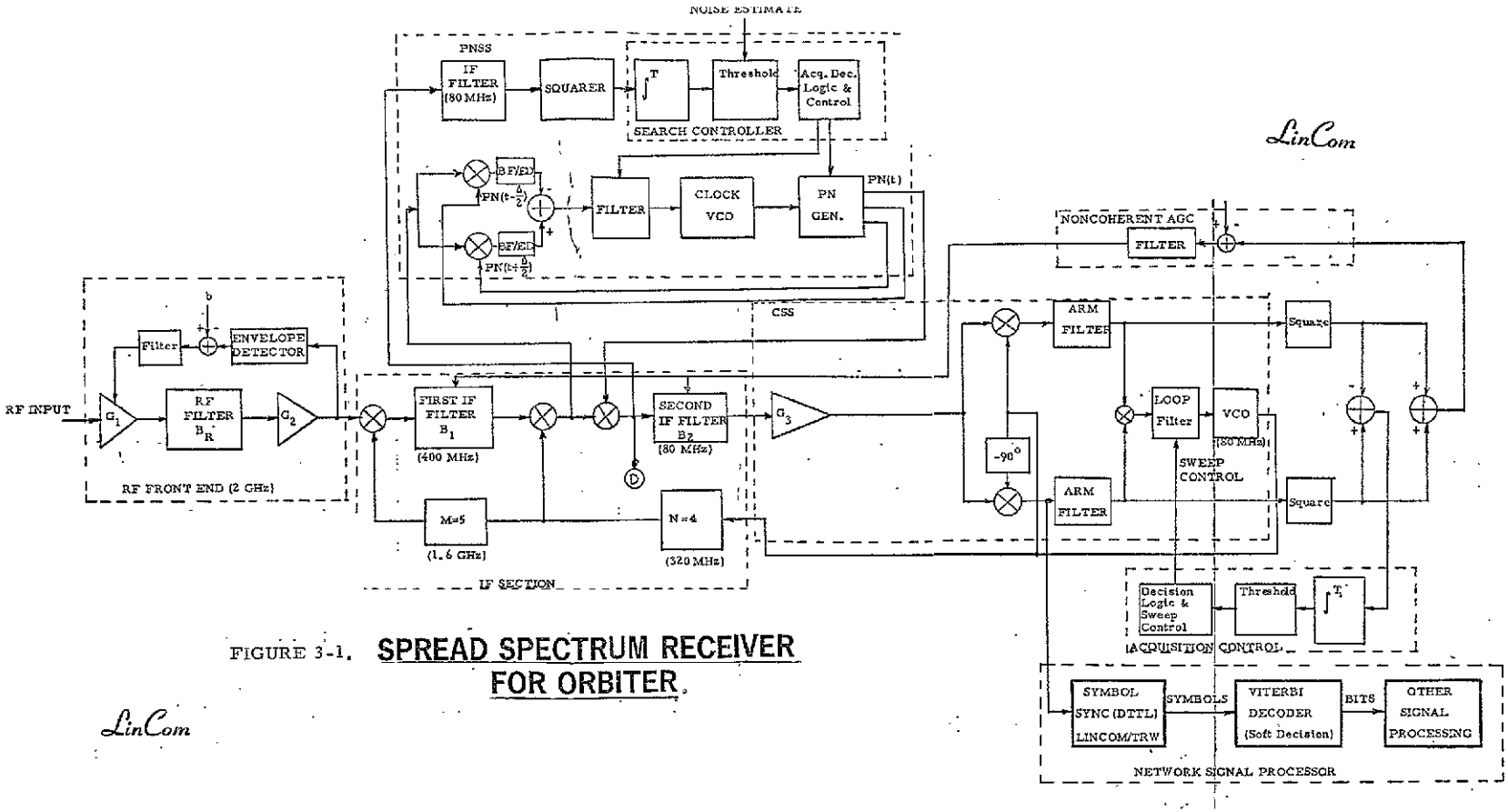


FIGURE 3-1. **SPREAD SPECTRUM RECEIVER FOR ORBITER.**

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FOLDOUT FRAME

FOLDOUT FRAME

of 80 MHz via a LO running at 320 MHz. The second IF output serves as the input to the PN synchronization system. The PN synchronization system (PNSS) of Fig. 3-1 incorporates a noncoherent PN acquisition and tracking design. The details associated with the particular algorithms selected will be presented in the PN Sync Subsystem Design and Analysis section of this Volume and Volume II.

The PNSS is configured to give rapid acquisition of the chosen PN code in deep noise and in the presence of worst-case Doppler frequency shifts. The PNSS also provides highly reliable code loop tracking performance under a chosen minimum input signal-to-noise level without severely degrading the symbol synchronizer, carrier tracking loop and data detection processes.

As shown in Fig. 3-1, the output of the second IF mixer is processed via two paths. One path is selected for signal demodulation and carrier recovery while the other for PN code acquisition and tracking. Based upon hardware considerations a τ-dither early/late gate code tracking loop has been implemented. This loop generates a code error signal proportional to the phase difference between the locally generated PN code and the received signal code. The code error signal generated at IF is filtered in the bandpass filter/envelope detector arrangement shown. A loop filter integrates the code phase error signal and drives a VCO to null the error signal. This assures precise code alignment at the on-time correlator or PN despreading mixer. The PN despreading mixer output contains the data signal without the code and is then processed as a normal BPSK suppressed carrier signal by means of a Costas loop.

The PNSS must acquire and track the PN code at a relatively low carrier-to-noise ratio, C/N_0, and a large carrier frequency uncertainty determined by the channel doppler and oscillator long term instabilities. The PNSS noncoherent code acquisition

circuitry was designed to provide optimum performance at a subsystem design point signal-to-noise condition of 48.3 dB-Hz. A code phase synchronization search is performed over the entire doppler-expanded code length by stepping the local PN code generator at half-chip intervals, integrating the envelope detector's output for a dwell time of T_d seconds, and then making a sync decision based upon a threshold comparison of is integrated output. The threshold is established by means of a noise estimate produced via an algorithm discussed in detail in Volume II. If the decision is not in favor of the particular code phase being searched, the code-tracking loop filter is quenched and the search proceeds to the next code phase position. The PN code acquisition stage of synchronization ends with the two codes (transmitted and local) most probably aligned to within an average of one-quarter of a chip. The second-order early-late gate τ-dither code tracking loop will then pull the system into final alignment.

As already noted, the code error signal is recovered at the output of the bandpass filter/envelope detector. The error signal polarity is toggled in synchronism with the early/late switching of the local PN code thereby creating a voltage proportional to the phase difference between the locally generated and received PN waveforms. This voltage is filtered by the loop filter and used to drive the VCO so as to null the error signal. Once the code loop locks, the loop filter positions the code loop VCO frequency so that the phase error between the local and received codes approach zero. The code loop bandwidth, B_L, is optimized to be 200 Hz for acquisition at C/N_0 = 48.3 dB-Hz and at C/N_0 = 51.3 dB-Hz the bandwidth opens to 350 Hz. This bandwidth is reduced to 12.5 Hz (C/N_0 = 48.3 dB-Hz) for tracking in order to minimize data and carrier loop performance degradations.

The arriving PN/BPSK signal is despread prior to filtering by the second IF filter. This gives rise to an ordinary BPSK

signal when the τ-dither loop is locked. The output from the second IF filter goes to the input of the carrier recovery circuit. The bandwidth of the second IF filter is chosen to be wide with respect to the data rate. This avoids creating intersymbol interference in the data stream; however, it may be found in practice that in order to avoid saturation of the carrier recovery circuit phase detectors due to low signal-to-noise ratios, the second IF may be required to be somewhat narrow.

A Costas (I/Q) loop configuration is chosen for carrier acquisition, tracking and data demodulation. This configuration was chosen because it was determined to be optimum when all considerations, including the ability to square perfectly over temperature and signal level, are traded against lock detection and synchronization monitoring. More concerning this topic will be discussed later.

Noncoherent AGC is derived from the sum "I" plus "Q" channels appearing in the arms of the Costas Loop. In addition, lock detection for the carrier circuit is accomplished by using the difference between the "I" and "Q" channels of the Costas arms. The non-coherent AGC_2 controls the receiver gain (prior to phase detection) with the signal plus noise level appearing in the outputs of the Costas loop arm. This feature is used to control the loop bandwidth and damping factor during acquisition and tracking. The bandwidth of the arm filters are chosen to minimize the so-called squaring loss and their roll-off chararacteristics selected to avoid the false lock problem.

The loop filter receives the signals from the phase detector (third multiplier) and supplies an error signal to the VCO which controls the local frequency. The loop filter sets the tracking loop bandwidth and damping factor. An AGC voltage, proportional to the incoming signal plus noise power, is low pass filtered and amplified to drive variable gain elements in the first and second IF

amplifiers. (These amplifiers are included here in the first and second IF filters for simplicity.) Additional integrate and dump circuits and threshold detector circuits control the sweep and the lock indicator needed for loop supervisory control. It is to be noted that the carrier sweep is not activated until PNSS is synchronized.

The carrier sync detector circuit monitors the integrate and dump voltage formed at discrete points in time by differencing the squares of the In-Phase and Quadrature arm outputs. The output of the integrate and dump circuit is compared to a fixed threshold level. If the I and D output exceeds the fixed threshold level a preliminary indication of lock is given and the search sweep is disabled. When lock is verified the loop bandwidth could be reduced, if necessary, to further reduce loop jitter. In such a case the loop bandwidth would be optimized for both acquisition and tracking.

Data extraction can be derived in two different ways. The most convenient way is to extract the data from the output of the Q channel and apply the symbol stream to the symbol sync system as shown in Fig. 3-1. The symbol synchronizer extracts the Manchester clock, resolves the two-fold ambiguity and applies the symbol (soft decision) voltages to the Viterbi decoder for further processing. The 180 degree phase ambiguity in the Costas loop is of no consequence since the K = 7 rate 1/3 convolutional code is not sensitive to code polarity.

An alternate approach to data extraction is to use a wideband phase detector and reflect the data to baseband by using the de-spread signal which appears at the input to the second IF filter. In practice this could be the preferable approach owing to the fact that the bandwidth of the second IF filter must be small enough to give a sufficient signal-to-noise ratio into the in-phase

and quadrature detectors of the Costas loop. When the signal-to-noise ratio into these phase detectors is too small, the problems associated with imperfect multiplication arise, viz., dc offsets in the loop and limiting of the noise. However, the differential phase shift accumulated between the second IF filter input and the input to the wideband phase detector created by the loop must be carefully controlled if this approach is used. The hardware simulation extracts the data from the Q-channel of the Costas loop, via a symbol synchronizer, see Fig. 3-1. The simulation does not include the Viterbi decoder.

3.1 Subsystem Interactions and System Degradations

Overall receiver performance is affected by various system interactions. These include the AGCs, PNSS, CSS, SSS and the Viterbi decoder. In what follows we point out these subsystem interactions by disecting either the equations of operation of the individual subsystems, or the signal model which serves at the input to the subsystem. These effects are summarized via equations which are developed in section four of this volume. They include the transponder equation of operation, the symbol sync and Viterbi decoder input, the lock or sync detection and carrier tracking loop monitor, the noncoherent AGC drives for the carrier tracking loop, and the effects of RF filtering.

3.1.1 Degradations in the Costas Loop SNR Due to the AGC and Despreading Subsystem Interaction

The equation of operation of the transponder simulated is given by

$$2\dot{\varphi} = 2\dot{d} - K_V K_m^2 g A^2 G(p)F(p)R_{xy}^2(\tau) \sin 2\varphi + \frac{N_{eq}}{A^2} - 40\, K_V e$$

where φ is the loop phase error, $d(t)$ is the channel Doppler profile, K_V is the VCO effect, e represents the transponder sweep voltage, N_{eq} is the equivalent loop noise, K_m is associated with the gain of

the in-phase and quadrature detectors, g is due to the noncoherent AGC variations, A^2 is the received signal power, G(p) represents the transfer function of the Costas arm filters, F(p) is the transfer function of the Costas loop filter, $R_{xy}(\tau)$ represents the PN-cross correlation between the filtered incoming code and the locally generated code. Here τ denotes the PN synchronization error. Several points are worth pointing out: (1) notice the 2φ and 2d effect which says that the Costas loop doubles the channel frequency uncertainty; (2) notice that the transponder loop signal-to-noise ratio is degraded by the RF/IF filter through $R^2_{xy}(\tau)$ (the despreading process); (3) the transponder loop signal-to-noise ratio is degraded by the jitter in the τ-dither loop; (4) the AGC degrades loop performance as well as other hardware imperfections not accounted for in the above equation. In the derivation of the above equation, the gain/phase imbalance in the Costas arm filters are neglected; however, in a well designed transponder these should be small.

3.1.2 Degradations in the Symbol Synchronizer/Viterbi Decoder Due to the PN Despreader/Demodulation/AGC Subsystem Interactions

The input to the symbol synchronizer and Viterbi decoder is given by

$$s(t) = (g \; R_{xy}(\tau) \cos \varphi(t)) \, A \, d(t) + g \, N(t)$$

AGC; PN-Cross-Correlation; PN Jitter; CSS; Data; AGC; Noise

Notice here that the AGC degrades the soft decisions fed to the Viterbi decoder, the cross-correlation due to the despreading process degrades the soft decisions, the transponder phase jitter degrades the soft decisions as well as the additive channel noise. All hardware degradations are neither indicated nor included.

3.1.3 Degradations in the Lock Detection and Carrier Tracking Monitor Due to the AGC, PN Despreader and Carrier Sync Subsystem Interactions

The lock or sync detection and Costas monitor subsystem sees as its input the signal

$$Z(t) = (g^2 \; R_{xy}^2(\tau) \cos 2\varphi) A^2 + N_{sq}(t)$$

(AGC; PNSS; CSS; Noise Squared)

With no degradations the output would be $A^2 \cos 2\varphi$ when the transponder is unlocked and A^2 when it is locked. Notice that the AGC degrades the sync detection and monitor process, the despreading in the receiver produces the cross-correlation $R_{xy}(\tau)$ which degrades performance and the squared noise further degrades performance.

3.1.4 Degradation in the Costas Noncoherent AGC Process Due to the PN Despreader and AGC Interactions

The noncoherent AGC drive is easily shown to be given by

$$Z_0(t) = (g^2 R_{xy}^2(\tau) A^2) + N_{sq}(t)$$

With no degradations the output would be the signal power A^2; notice that the AGC drive is degraded by the AGC fluctuations, the despreading process and the noise N_{sq}.

In all cases the Costas arm filter gain/ phase imbalance has been omitted; however, in a well designed system these effects can be made small such that our assumptions leading to the above equations remain valid.

3.1.5 RF/IF Filter Degradations

Proper choice of the RF filters gain/phase characteristic is important because any deleterious effects which is produces propagate throughout the process of despreading, demodulation, data detection, lock detection and Costas AGC. In particular,

through the cross-correlation function $R_{xy}(\tau)$ of the locally generated code and the filtered incoming code, the PN code tracking phase detector's slope and peak-to-peak values are degraded, the phase detectors in the I and Q channels are degraded, the phase detector in the symbol synchronizer, the lock detection system in the PNSS, CSS and the SSS, and the bit error probability are all degraded. Fig. 3.1.5-1 serves to illustrate the effects on the PN chips for the case where the RF filter bandwidth times the code chip product is two. The Butterworth, Chebycheff and Bessel filters are all two-pole at the baseband which implies four pole at bandpass. Notice the effects of intersymbol interference in the chips. Further illustrations of the effects of the RF filter on the τ-dither loop, S-curve and the cross-correlation function $R_{xy}(\tau)$ are given in Section 7 and Volume II for both Butterworth and Chebycheff filters.

3.1.6 Design Parameters

The system parameters and conditions of Table 3.1.6-1 are typical of the forward link associated with the TDRS to Shuttle Orbiter. The main feature associated with this link is the low signal-to-noise ratio which implies low system performance margins. These parameters were used, where appropriate, in developing the simulation.

4.0 Design of the Coherent Transponder and Theoretical Performance for the Carrier Sync System

The functional diagram of the transponder is shown in Fig. 4-1. The main interest in this section is to discuss the various approaches which allow one to reconstruct a carrier from a suppressed carrier signal. A number of methods have been proposed for generating a carrier reference from the received waveform. These are summarized in Table 4-1. Of these, the three most popular are the squaring loop method (Refs. 1-5), the Costas loop method

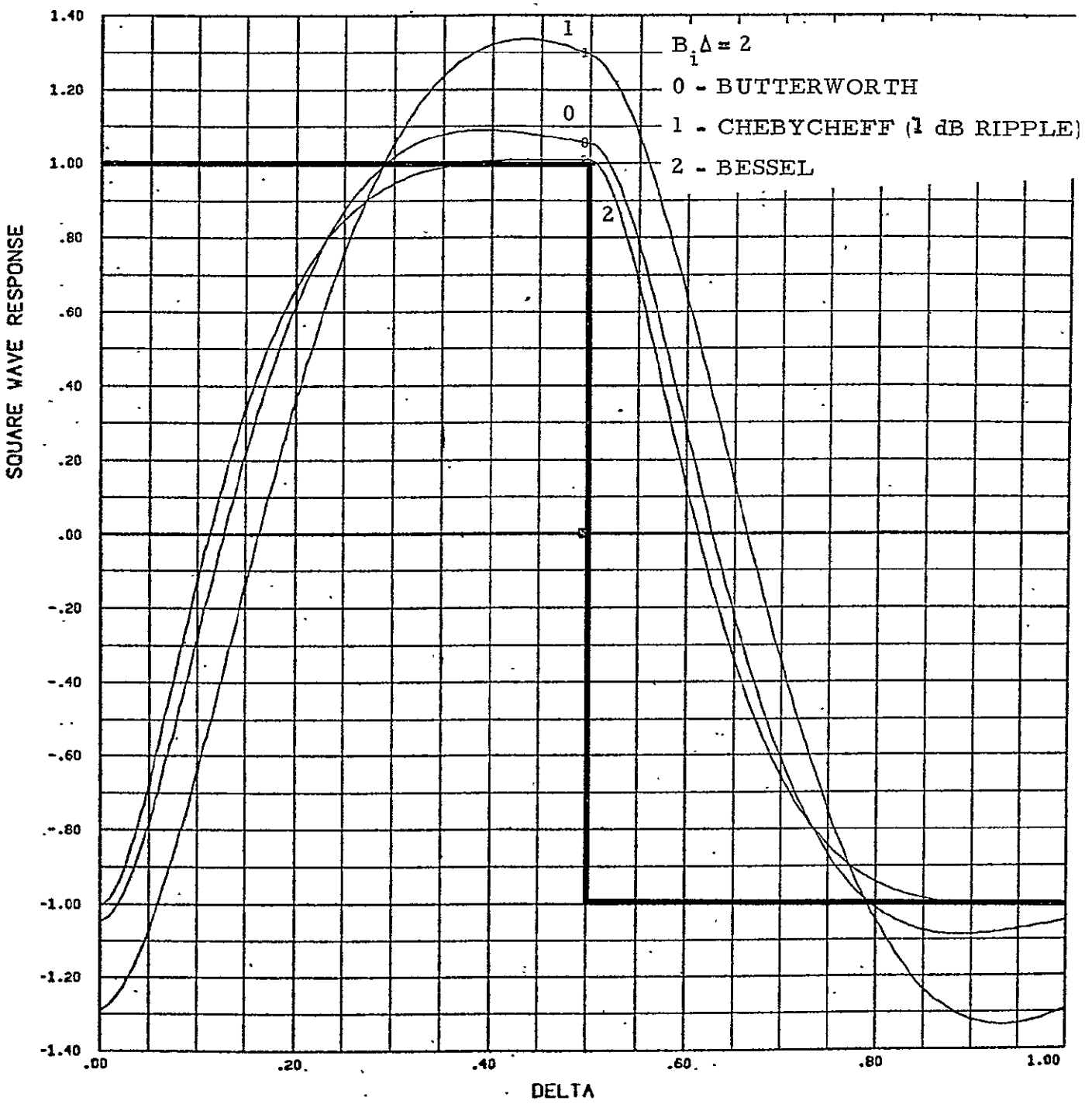

FIGURE 3.1.5-1. PULSE RESPONSE FOR VARIOUS FILTERS.

TABLE 3.1.6-1. TDRS/ORBITER FORWARD LINK CARRIER/ NOISE CONDITIONS.

	Specification	Value
1.	NRZ/Convolutionally Coded/Manchester	
2.	Total Received Power/Noise Spectral Density (Nominal)	54.7
3.	Encoded Data Rate, 10 log (216 Ksps) dB	53.3
4.	Signal/Noise in Symbol Rate Bandwidth, dB (Nominal)	1.4
5.	Signal/Noise in Symbol Rate Bandwidth, dB (Worst Case)	-5
6.	PN Chip Rate (MHz)	11.232
7.	PN Code Length (Chips)	2047
8.	PN Code Period (msec)	0.182
9.	Maximum Code Doppler Error (Chips/sec)	±300
10.	Channel Doppler (kHz)	±55
11.	Maximum Rate of Change of Doppler (Hz/sec)	±0.4

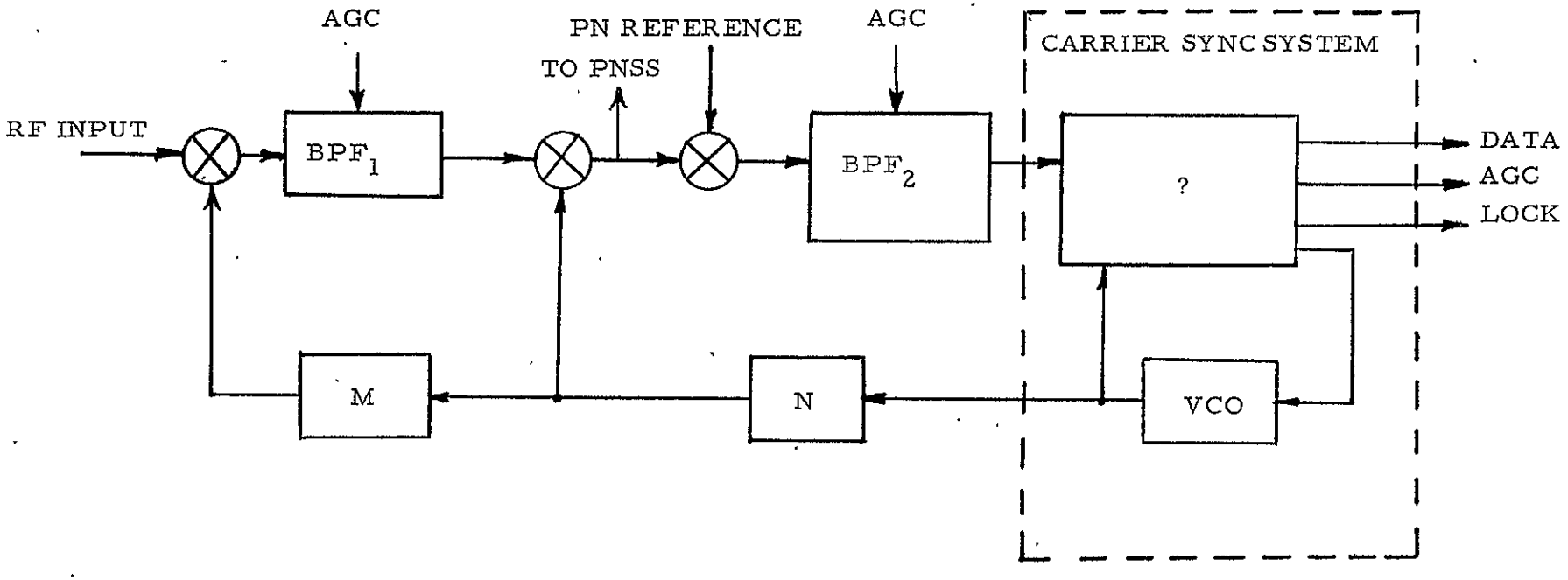

FIGURE 4-1. TRANSPONDER FUNCTIONAL DIAGRAM.

TABLE 4-1. SUPPRESSED CARRIER SYNC TECHNIQUES.

- OPTIMUM
  - MAP ESTIMATION THEORY
  - NONLINEAR FILTERING THEORY
- INTEGRATE AND DUMP
- DECISION-DIRECTED LOOP
- POLARITY TYPE
- COSTAS TYPE
- SQUARING LOOP

(Refs. 1, 2, 4-6), which is theoretically equivalent to the squaring loop, and the decision-directed feedback loop (Refs, 1, 2, 7-9) which first estimates the modulation, and then uses this estimate to eliminate the modulation from the carrier, leaving as nearly as possible, an unmodulated sinusoid which can be tracked with a phase-locked loop. Each of these methods has advantages and disadvantages (practical or otherwise) but what ultimately determines which method is used in a particular application is a tradeoff between the requirements on performance capability, the lock detection system and cost of implementation.

A comparison of these various techniques is given in Table 4-2. From this comparison the Costas loop and squaring loop form the basis upon which the carrier sync system is to be selected. This is due to the fact that the interface between the bit synchronizer and carrier loop must remain uncoupled. The Costas vs Squaring loop must be determined from the hardware implementation viewpoint. Table 4-3 summarizes the key considerations; major factors which enter into the final choice include the gain-phase imbalance in the Costas arm filters which effect sync acquisition at low signal-to-noise ratios versus the ability to square perfectly over temperature and a large variation in signal level. For the hardware simulation, the Costas loop has been selected because of its superior performance (0.5 to 1.0 dB) obtained over a real world squaring circuit at low signal-to-noise ratios.

4.1 Costas Loop Design

As is well-known from previously published documents (Refs. 10-12) suppressed carrier modulation is employed on both the TDRSS-to-Orbiter (Forward) and Orbiter-to-TDRSS (Return) S-band links. In the case of the forward link, the convolutionally encoded, time-division multiplexed (TDM) data sequence is converted from NRZ-L to Bi-phase-L format, modulo-2 added

TABLE 4-2. COMPARISON OF BPSK SUPPRESSED CARRIER RECONSTRUCTION LOOPS.

TECHNIQUE	COMMENTS	
	Acquisition	Tracking
Decision Directed	(1) Poor Acquisition Performance due to False Lock (2) Requires Symbol Sync	(1) Good Tracking Performance (2) Requires Symbol Sync
Hard Decision Demod/Remod	(1) Suboptimum Performance at Low SNR	(1) Suboptimum Performance at Low SNR
Costas Loop (I and D Type)	(1) Optimum Performance (2) Requires Symbol Sync (3) False Lock	(1) Optimum Performance (2) Requires Symbol Sync
Costas Loop (Polarity Type)	(1) Poor Performance at Low SNR (2) Symbol Sync Not Required (3) 3rd Multiplier Relief (4) False Lock	(1) Poor Performance at Low SNR (2) Symbol Sync Not Required (3) 3rd Multiplier Relief
Costas Loop (3rd Multiplier)	(1) Good Performance at Low SNR (2) Symbol Sync Not Required (3) False Lock (4) Gain Imbalance/Phase Shift in Arm Filters	(1) Good Performance at Low SNR (2) Symbol Sync Not Required (3) Gain Imbalance/Phase Shift in Arm Filters
Squaring Loop	(1) Good Performance at Low SNR (2) Symbol Sync Not Required (3) False Lock (4) Squaring Circuit Sensitive to SNR and Temperature (5) No Gain Imbalance	(1) Good Performance at Low SNR (2) Symbol Sync Not Required (3) No Gain Imbalance (4) Squaring Circuit Sensitive to SNR and Temperature

TABLE 4-3. COSTAS VS SQUARING LOOP.

- MUST BE DETERMINED FROM HARDWARE IMPLEMENTATION VIEWPOINT AS THEY HAVE SAME COMMUNICATION PERFORMANCE

- SELECTION MUST CONSIDER
  - AGC
  - SYNC DETECTION
  - HARDWARE COMPLEXITY
  - HARDWARE DEGRADATIONS

to a PN NRZ-L code sequence, and the resulting spread-spectrum sequence used to biphase modulate the transmitted carrier. After transmission through the TDRSS, the Orbiter receiver first despreads the signal by acquiring and tracking the PN code. Following this procedure, the baseband data symbol sequence is restored by demodulating the suppressed carrier signal with a Costas loop. In the return link, similar carrier modulation and demodulation processes take place with the exception that the signal is neither PN spread nor despread.

It is clear from the above that in order to assess the degrading effects of the carrier regeneration process on the overall system performance (including the average error probability performance of the data decoder), a thorough understanding of the acquisition and tracking performance of Costas loops and their optimum design in the Shuttle relay link environment is required.

The tracking performance of a Costas loop in response to a biphase modulated suppressed carrier input is well-documented in the literature (Refs. 1, 2, 4-6). All of these analysis have assumed that the in-phase and quadrature arm filters have sufficiently wide bandwidths to as to pass the data modulation undistorted. In practice, the bandwidths of these filters are more commonly chosen on the order of the data rate and thus the above assumption is strictly speaking invalid. In Refs. 13 and 14, the effect of arm filter distortion has been studied in detail, graphically demonstrated, and compared with the results given in the literature which have neglected this important effect. In fact, careful control of the distortion term in any design gives rise to the highest noise immunity achievable with passive arm filters. Even these analyses, however, have not included the degrading effect of a spread spectrum modulation on the signal being tracked.

It is the purpose of this section to augment the previous work

on Costas loops by including the effect of a PN spread spectrum modulation on tracking performance. The approach will parallel the development taken in Ref. 13 and thus much of the detail given there will be omitted in the presentation here. Finally, the results obtained will be adapted to cover the case where the Manchester coded data is also convolutionally encoded. The Costas loop characteristics and performance measures of interest in the design are summarized in Table 4-4.

4.1.1 Costas Loop Model

Consider the transponder illustrated in Fig. 4.1.1-1 where the Costas loop portion is enclosed within the dashed outline. Since our main interest here is in the performance of the Costas loop itself, it is sufficient for us to model the signal at its input and concentrate on how the loop processes this signal. Referring to Fig. 4.1.1-1, if the received signal $x_1(t)$ at point 1 is modeled as

$$x_1(t) = \sqrt{2S}\, s_{PN}(t)m(t) \sin \Phi(t) + n_i(t) \tag{1}$$

then, using straightforward trigonometric manipulations, one finds that the signal at the input to the Costas loop (point 4) is given by

$$x_4(t) = K_e s_{PN}(t+\tau_e)\left[\sqrt{2S}\, s_{PN}(t)m(t) \sin\left[\Phi(t) - \frac{M+1}{M}\Phi(t)\right] + n_4(t)\right] \tag{2}$$

In Eq. (1), $\Phi(t) \triangleq \omega_0 t + \theta(t)$ with ω_0 the radian carrier frequency and $\theta(t) \triangleq \Omega_0 t + \theta_0$ the input phase to be estimated, $m(t)$ is the data modulation (a ± 1 digital waveform), $s_{PN}(t)$ is the received PN modulation, and $n_i(t)$ is the additive channel noise which can be expressed in the form of a narrowband process about the actual frequency of the input observed data, i.e.,

$$n_i(t) = \sqrt{2}\left[N_c(t) \cos \Phi(t) - N_s(t) \sin \Phi(t)\right] \tag{3}$$

where $N_c(t)$ and $N_s(t)$ are approximately statistically independent,

TABLE 4-4. CARRIER TRACKING LOOP CHARACTERISTICS AND PERFORMANCE MEASURES

- ARM FILTER CHARACTERISTICS
- DISTORTION AND INTERSYMBOL INTERFERENCE
- OPTIMUM ARM FILTER BANDWIDTHS
- SQUARING LOSS
- PHASE JITTER
- LOOP BANDWIDTH AND DAMPING
- SLIP RATE
- SLIP PROBABILITIES

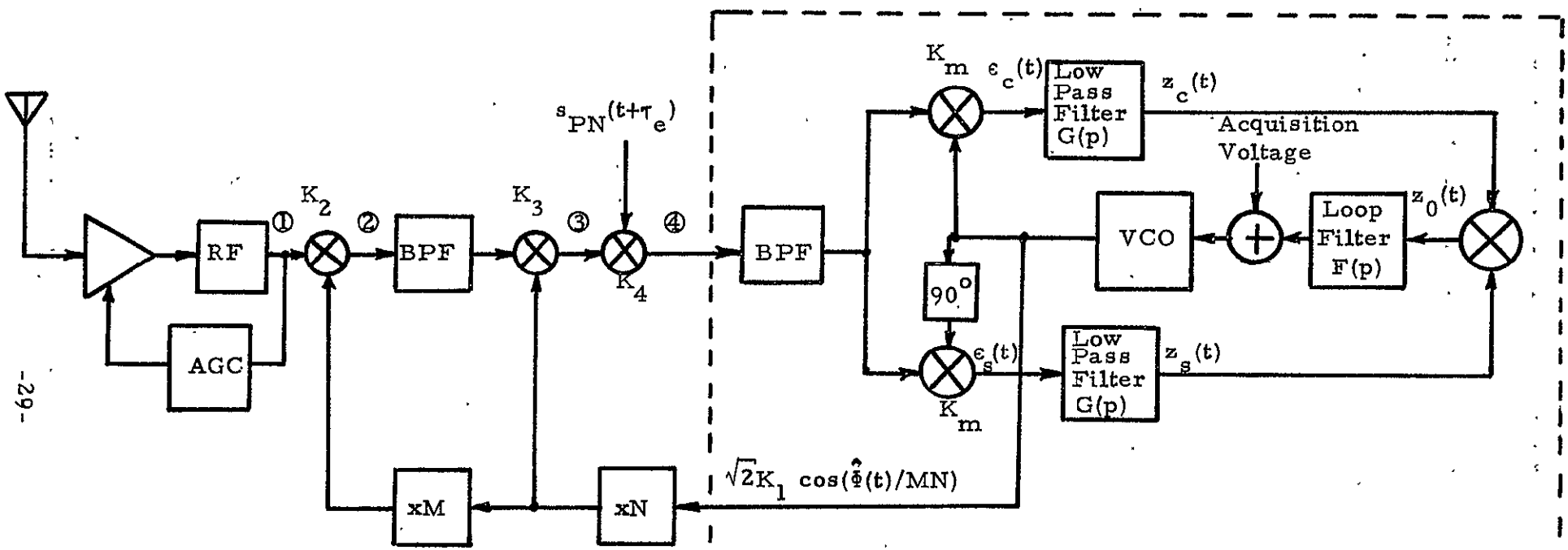

FIGURE 4.1.1-1. TRANSPONDER/COSTAS LOOP BLOCK DIAGRAM.

stationary, white Gaussian noise processes with single-sided noise spectral density N_0 w/Hz (see Ref. 2) and two-sided bandwidth $B_i < \omega_0/2\pi$. In Eq. (2), $s_{PN}(t+\tau_e)$ is the PN reference signal derived from the PN tracking loop, $K_e = K_1^2 K_2 K_3 K_4/2$ is an equivalent loop gain, and

$$n_4(t) = \sqrt{2}\left\{N_c(t)\cos\left[\Phi(t) - \frac{M+1}{M}\hat{\Phi}(t)\right] - N_s(t)\sin\left[\Phi(t) - \frac{M+1}{M}\hat{\Phi}(t)\right]\right\} \quad (4)$$

Also assumed in Eq. (2) is that the bandpass filter which precedes the Costas loop is sufficiently wide as to pass the data modulation m(t) undistorted. Denoting the in-phase and quadrature detector (multiplier) gains by K_m, then the output $\epsilon_c(t)$ of the quadrature phase detector is (ignoring second harmonic terms)

$$\epsilon_c(t) = K_m x_4(t)\sqrt{2}K_1 \cos\frac{\hat{\Phi}(t)}{MN} = K_e K_1 K_m\left[\sqrt{S}R_{PN}(\tau_e)m(t) - N_s'(t)\right]\sin\varphi(t) + K_2 K_1 K_m N_c'(t)\cos\varphi(t) \quad (5)$$

while the in-phase arm phase detector output is

$$\epsilon_s(t) = K_m x_4(t)\sqrt{2}K_1 \sin\frac{\hat{\Phi}(t)}{MN} = K_e K_1 K_m\left[\sqrt{S}R_{PN}(\tau_e)m(t) - N_s'(t)\right]\cos\varphi(t) - K_e K_1 K_m N_c'(t)\sin\varphi(t) \quad (6)$$

where $\varphi(t) \triangleq \Phi(t) - \frac{(M+1)N+1}{MN}\hat{\Phi}(t)$ is the loop phase error, $R_{xy}(\tau_e) \triangleq \overline{s_{PN_f}(t)s_{PN}(t+\tau_e)}$ is the cross-correlation function between the locally generated code and the RF/IF filtered PN code, and $N_c'(t)$ and $N_s'(t)$ are equivalent noise processes defined by

$$\begin{aligned} N_c'(t) &= s_{PN}(t+\tau_e)N_c(t) \\ N_s'(t) &= s_{PN}(t+\tau_e)N_s(t) \end{aligned} \quad (7)$$

In writing Eqs. (5) and (6), we have again assumed that the data modulation is passed undistorted by the bandpass filter following point 4. Multiplying the two low-pass filter outputs (assuming

multiplier has unit gain) gives the dynamic error signal

$$z_0(t) = z_c(t)z_s(t) = \frac{K_e^2K_1^2K_m^2}{2}\left\{\left[\sqrt{S}R_{PN}(\tau_e)\hat{m}(t)-N_s''(t)\right]^2 - N_c''^2(t)\right\}\sin 2\varphi(t)$$

$$+ K_e^2K_1^2K_m^2N_c''(t)\left[\sqrt{S}R_{PN}(\tau_e)\hat{m}(t)-N_s''(t)\right]\cos 2\varphi(t) \qquad (8)$$

The instantaneous frequency of the VCO output is related to $z_0(t)$ by

$$\frac{d\hat{\phi}(t)}{dt} = K_V\left[F(p)z_0(t)\right] + \omega_0 \qquad (9)$$

and hence the stochastic integro-differential equation of operation of the Costas loop becomes

$$2\frac{d\varphi(t)}{dt} = 2\Omega_0 - KF(p)\{SR_{PN}^2(\tau_e)\hat{m}^2(t)\sin 2\varphi + v_2[t, 2\varphi(t)]\} \qquad (10)$$

where $K \triangleq K_e^2K_1^2K_m^2K_V$, and

$$v_2[t, 2\varphi(t)] \triangleq \left[-N_c''^2(t) + N_s''^2(t) - 2\sqrt{S}R_{PN}(\tau_e)\hat{m}(t)N_s''(t)\right]\sin 2\varphi(t)$$
$$+ \left[2\sqrt{S}R_{PN}(\tau_e)\hat{m}(t)N_c''(t) - 2N_c''(t)N_s''(t)\right]\cos 2\varphi(t) \qquad (11)$$

In arriving at (11), we have made the practical assumption that the data rate $\mathcal{R}_s \triangleq 1/T_s$ is large relative to the equivalent loop bandwidth W_L, and thus $\hat{m}^2(t)$ can be replaced by its mean-squared value, i.e.,

$$\overline{\hat{m}^2(t)} \triangleq \int_{-\infty}^{\infty} S_m(f)\left|G(j2\pi f)\right|^2 df \qquad (12)$$

with $S_m(f)$ denoting the power spectral density of the data modulation $m(t)$.

4.1.2 Steady-State Tracking Performance

Using Fokker-Planck techniques, the steady-state probability density function (p.d.f.) $p(2\phi)$ of the modulo 2π reduced phase error 2ϕ can be determined from (10). Assuming a loop filter of the form

$$F(s) = \frac{1+s\tau_2}{1+s\tau_1}; \quad F_1 = \frac{\tau_2}{\tau_1} \tag{13}$$

then, (Ref. 1, Chap. 2 and Ref. 2, Chaps. 9, 10)

$$p(2\phi) = C_0 \exp(\beta 2\phi + \alpha \cos 2\phi) \int_{2\phi}^{2\phi+2\pi} \exp(-\beta 2x - \alpha \cos 2x)dx \tag{14}$$

where C_0 is a normalization constant and

$$\alpha = \left(\frac{r+1}{r}\right) \rho' - \frac{1-F_1}{r\sigma_G^2} \tag{15}$$

$$\beta = \left(\frac{r+1}{r}\right)^2 \frac{\rho'}{2W_L} \left[2\Omega_0 - SR_{PN}^2(\tau_e)\overline{\hat{m}^2(t)}K(1-F_1)\overline{\sin 2\phi}\right] + \alpha \overline{\sin 2\phi}$$

with

r = second order loop damping parameter = $SR_{PN}^2(\tau_e)\overline{\hat{m}^2(t)}KF_1\tau_2 = 4\zeta^2$

ζ = loop damping

ρ' = effective signal-to-noise ratio in the loop bandwidth = $(\rho/4)\mathscr{S}_L$

ρ = equivalent signal-to-noise ratio in the loop bandwidth of second-order PLL = $2SR_{PN}^2(\tau_e)/N_0W_L$

$\sigma_G^2 = \overline{\sin^2 2\phi} - \overline{(\sin 2\phi)}^2$

= loop squaring loss $\triangleq \dfrac{4SN_0\overline{(\hat{m}^2(t))}^2 R_{PN}^2(\tau_e)}{}$

$$N_{sq} \triangleq 2\int_{-\infty}^{\infty} R_{v_2}(\tau)d\tau \tag{16}$$

and

$$R_{v_2}(\tau) \triangleq \overline{v_2(t,2\phi)v_2(t+\tau,2\phi)} = 4\left[SR_{PN}^2(\tau_e)R_{\hat{m}}(\tau)R_{N_c''}(\tau) + R_{N_c''}^2(\tau)\right] \tag{17}$$

In arriving at (17) we have made use of the previous assumption that the arm filters are narrowband relative to the input bandpass (IF) filter. The probability density function in (14) will be useful in what follows.

The squaring loss $\mathscr{L}_L$ can be derived in terms of basic system parameters. Using (16) and (17) and the definition of $\mathscr{L}_L$ it is easy to derive the square loss formula

$$\mathscr{L}_L = \frac{D}{K_D + K_L \frac{B_i/R_s}{2R_s' D}} \tag{18}$$

where we have used $D \triangleq \hat{m}^2(t)$ to denote the modulation distortion factor, $R_s' = SR^2_{PN}(\tau_e)\, T_s/N_0$ is the effective data (symbol) signal-to-noise ratio, B_i, denotes the two-sided noise bandwidth of the arm filter $G(j2\pi f)$, i.e.,

$$B_i \triangleq \int_{-\infty}^{\infty} |G(j2\pi f)|^2 df \tag{19}$$

K_L is a constant dependent only on the filter type and K_D is a constant dependent on both the baseband data power spectrum and the filter type. Typical values of K_L for well-known filter types may be found in Table 2-1 of Ref. 1, Chap. 2. For example, $K_L = 1$ for an ideal low-pass filter while $K_L = (2n-1)/2n$ for an n-pole Butterworth filter. Since the modulation distortion factor D_m and the constant K_D respectively depend on the baseband data power spectrum $S_m(f)$, the format of the baseband data encoding must be specified before these quantities can be computed. The case of interest here is when the modulation m(t) is a Manchester coding of equiprobable, independent transmitted symbols. The power spectral density $S_m(f)$ for such a data modulation is, Ref. 1, Chap. 2,

$$\frac{S_m(f)}{T_s} = \frac{\sin^4(\pi f T_s/2)}{(\pi f T_s/2)^2} \tag{20}$$

Recalling that an n-pole Butterworth filter is characterized by the transfer function

$$|G(j2\pi f)|^2 = \frac{1}{1 + (f/f_c)^{2n}} \tag{21}$$

where f_c, the 3 dB bandwidth, is related to the two-sided noise bandwidth B_i of the filter by

$$f_c = \frac{nB_i}{\pi} \sin\left(\frac{\pi}{2n}\right) \tag{22}$$

then, the modulation distortion factor D and constants K_L and K_D can be computed by numerical integration as functions of the ratio $B_i/\mathcal{R}_s$. Using these results, Fig. 4.1.2-1 illustrates the square loss $\mathcal{L}_L$ vs $B_i/\mathcal{R}_s$ with R_d as a parameter for a one and two-pole Butterworth filter. We observe that for a fixed R_d there exists an optimum noise bandwidth B_i for the arm filters in the sense of minimizing the squaring loss. These values of optimum arm filter bandwidth occur in the vicinity of the Nyquist bandwidth; in particular, for n = 2 the optimum arm filter bandwidth is approximately one and one-half times the data rate. The modulation distortion factor for this bandwidth is approximately 1.3 dB.

The minimum square loss achievable with two-pole Butterworth arm filters is illustrated in Fig. 4.1.2-2. At C/N_0 = 48.3 dB-Hz and 53.3 dB-Hz the direct attack on C/N_0 is 8.5 dB and 4.8 dB respectively. Figure 4.1.2-3 illustrates the rms 2φ jitter in a Costas loop versus C/N_0. Notice that C/N_0 = 48.7 dB-Hz the rms jitter is approximately 28 degrees when B_L = 500 Hz. In the hardware simulation a bandwidth of 500 Hz is used at the chosen system design point of C/N_0 = 51.3 dB-Hz. Please note that the PNSS design point is 48.3 dB-Hz. Figure 4.1.2-4 illustrates a plot of the Costas loop cycle slipping rate vs C/N_0. At C/N_0 = 48.7 dB-Hz the number of cycle slips per minute is approximately six. Other values can be taken directly from this figure.

Figure 4.1.2-5 illustrates the bit error probability noisy

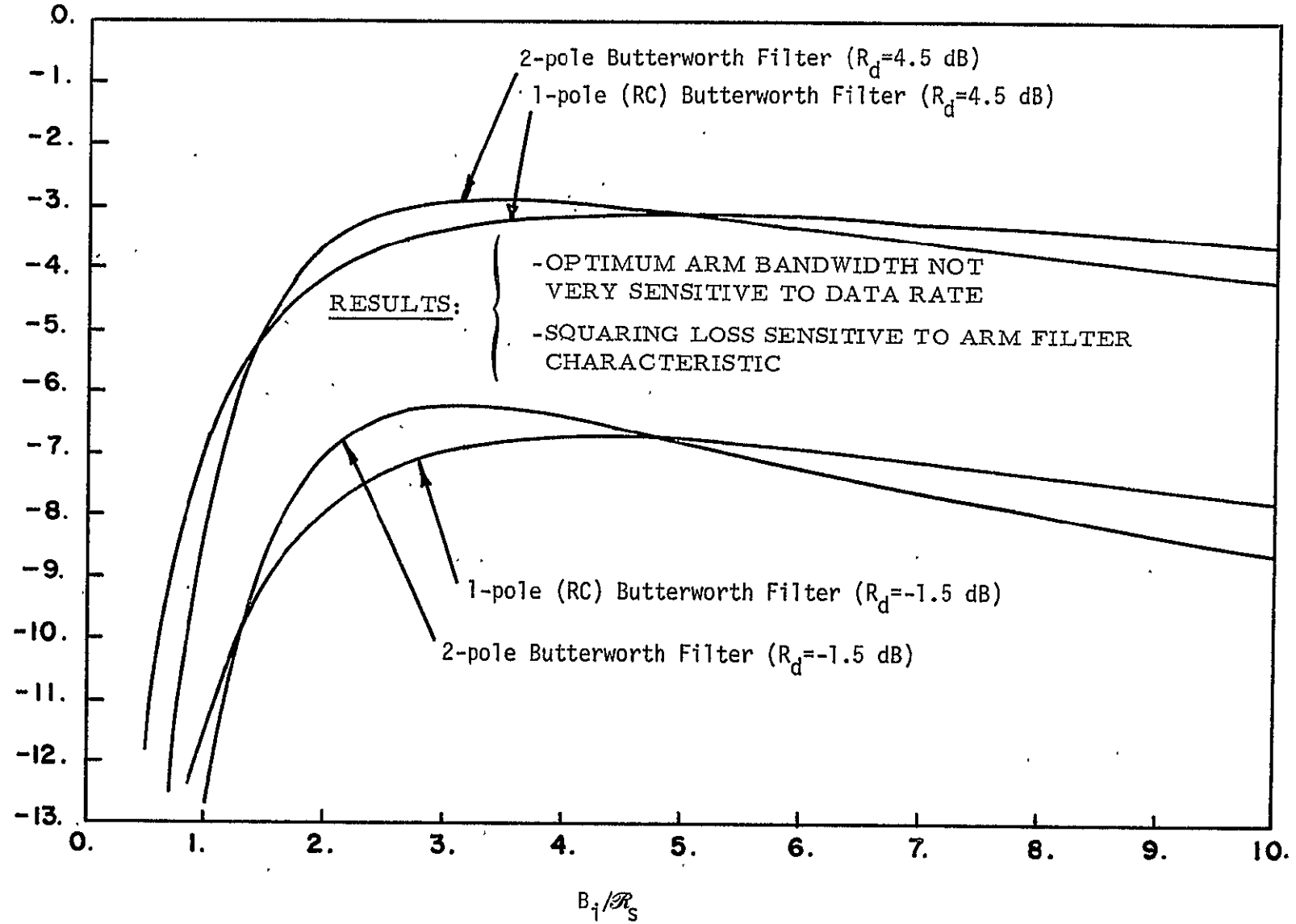

FIGURE 4.1.2-1. SQUARING LOSS IN A COSTAS LOOP VS $B_i/\mathscr{R}_s$.

FIGURE 4.1.2-2. SQUARING LOSS $\mathscr{L}_L$ vs C/N_0.

LinCom

Manchester Data With 50% Transition Density in NRZ

Arm Filter Bandwidth Optimized

RESULT

$\mathscr{L}_L$ @ 48.7 dB-Hz = 8.5 dB

$\mathscr{L}_L$ @ 53.7 dB-Hz = 4.8 dB

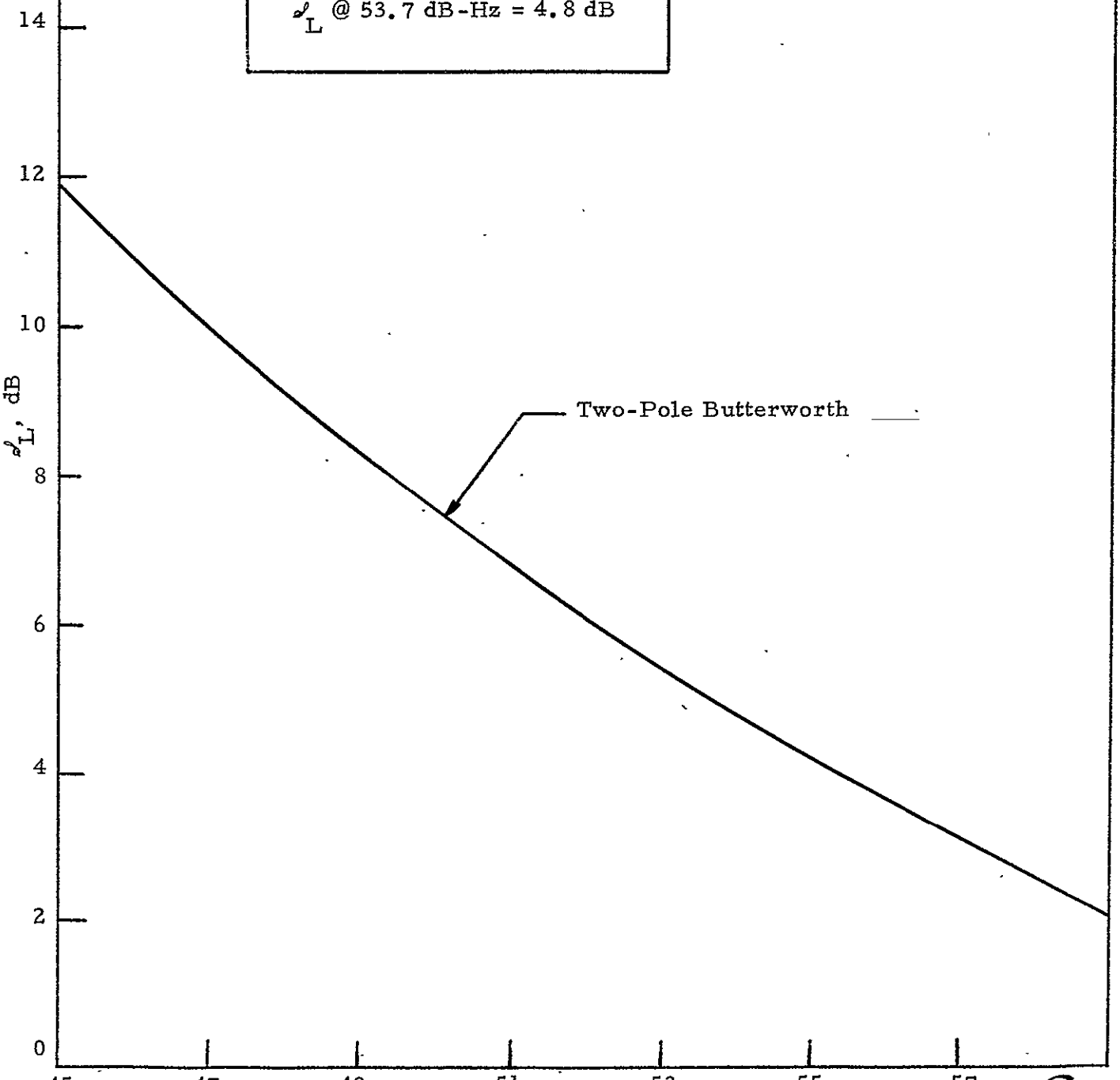

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FIGURE 4.1.2-3.
LOOP PHASE JITTER $\sigma^{o}_{2\phi}$ vs. C/N_0.

LinCom

- Two-Pole Butterworth in Arm Filters (Bandwidth Optimized: B_i = 324 kHz)
- Manchester Data @ 50% Transition Density in NRZ
- Data Rate = 216 ks/s

RESULT

$\sigma^{o}_{2\phi}$ = 28° @ 48.7 dB-Hz

$\sigma^{o}_{2\phi}$ = 8° @ 54.7 dB-Hz

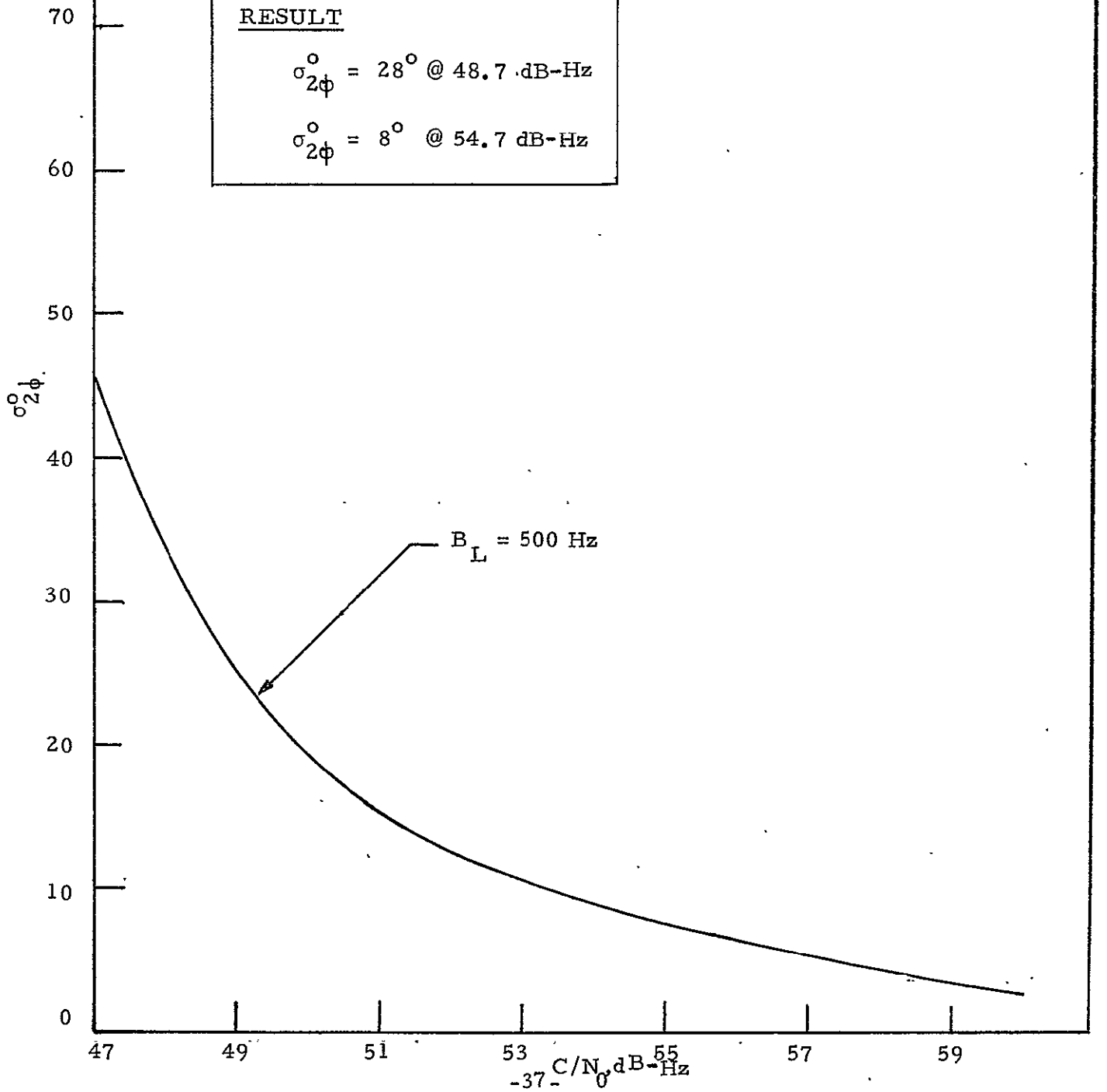


FIGURE 4.1.2-4. CYCLE SLIP RATE VS C/N_0.

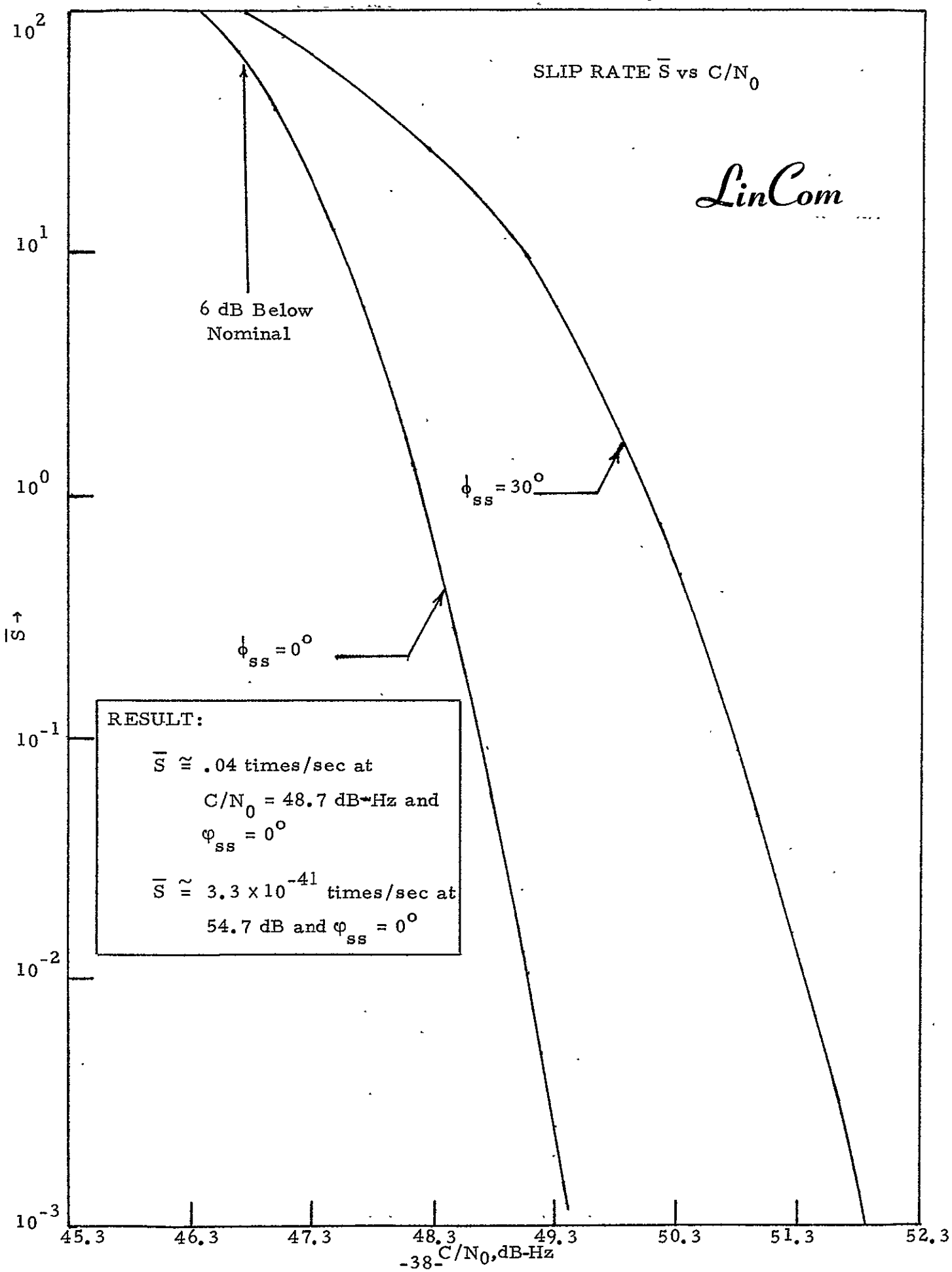
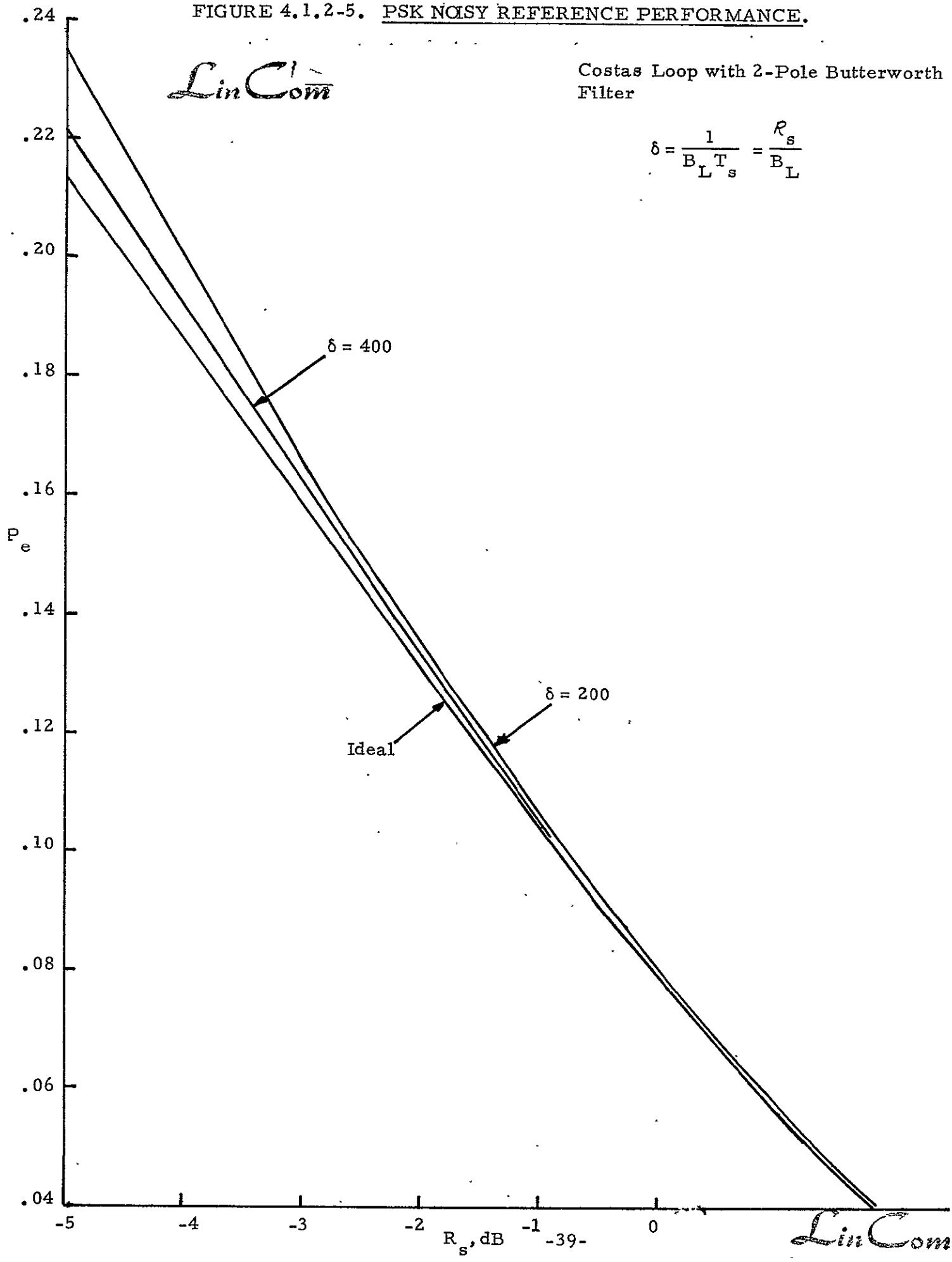


FIGURE 4.1.2-5. PSK NOISY REFERENCE PERFORMANCE.



reference loss degradations as a function of the energy per symbol to noise ratio R_s with the ratio of the data rate $\mathcal{R}_s$ to loop bandwidth B_L as a design parameter. For the hardware simulation $\delta = \mathcal{R}_s/B_L$ is 432 so that the noisy reference loss is a few tenths of a dB at R_s = -3 dB.

4.2 Carrier Acquisition and Sweep Circuit Design

After the PN τ-dither loop locks it is then possible for the Costas loop to lock. Owing to the fact that the maximum Doppler is many times the Costas loop acquisition bandwidth it is necessary to provide the Costas loop with some form of an acquisition aid. There are several practical methods for deriving a control voltage proportional to the frequency error so as to improve the frequency acquisition capability of the loop. These include: (1) an automatic frequency control (AFC) augmentation and an acquisition monitor circuit, (2) step the local VCO in predetermined step sizes across the frequency uncertainty band and monitor acquisition via the lock detection system at discrete points in time, (3) sweep the local VCO, at a predetermined rate, across the uncertainty band and continuously monitor acquisition via a lock detection system, (4) open loop search and monitor acquisition. These techniques are compared in Table 4-2.1

For the hardware simulation LINCOM has chosen technique three which incorporates sweeping the VCO and verifying lock by processing the I and Q channel outputs in and integrate and dump circuits; see the system block diagram illustrated in Figure 3-1. Furthermore, for the data rate of interest and the VCO offset required, the Costas will not false lock to a signal sideband when no data modulation is present. For the filters implemented group delay did not degrade acquisition performance.

In the design of a sweep circuit for acquisition and a lock detection system, various search and loop performance parameters come into play. These are summarized in Table 4-2.2.

TABLE 4.2-1. CARRIER SYNC ACQUISITION ALGORITHMS.

TECHNIQUE	COMMENTS
1. OPTIMUM BASED UPON NONLINEAR FILTERING THEORY	ESTIMATOR/CORRELATOR IS DIFFICULT TO IMPLEMENT
2. SERIAL MAXIMUM LIKELIHOOD (FIXED-SAMPLE SIZE) WITH STEPPED OR SWEPT LOCAL VCO	EASY TO IMPLEMENT. MAY HAVE TENDENCY TO FALSE LOCK WHICH DEPENDS UPON DOPPLER AND DATA TRANSITION DENSITY
3. SPR TEST COMBINED WITH STEPPED LOCAL VCO	DIFFICULT TO IMPLEMENT. RARELY USED IN CARRIER SYNC SYSTEMS.
4. SWEPT LOCAL VCO	EASY TO IMPLEMENT; PERFORMANCE INFERIOR TO 2. FREQUENTLY USED IN PRACTICE. SAME FALSE LOCK COMMENT AS IN 2.
5. OPEN LOOP SEARCH	EASY TO IMPLEMENT; HOWEVER, 2 dB PERFORMANCE PENALTY COMPARED TO CASE 2.
6. USE IN AFC AUGMENTATION	AVOIDS FALSE LOCK MECHANISM; HOWEVER REDUCES TRACKING THRESHOLD AT LOW SNR.

TABLE 4-2.2 SEARCH AND LOOP PERFORMANCE PARAMETERS.

$\Omega_0 = 2\pi\Delta f$ - DOPPLER UNCERTAINTY

Ω_1 - DOPPLER RATE

T_a - TIME TO SEARCH FREQUENCY UNCERTAINTY BAND ONCE

B_L - LOOP BANDWIDTH

$S_r = \frac{\Delta f}{T_a}$ - SEARCH RATE

τ_s - SYNC PULSE DURATION

A_s - SYNC PULSE AMPLITUDE

α – SYNC FALSE ALARM PROBABILITY

β — PROBABILITY OF FALSE SYNC DISMISSAL

Th - THRESHOLD VALUES

ρ – LOOP SNR

Major considerations which must be taken into account in the design include: (1) a statistical characterization of the sync pulse generated in the in-phase arm of the Costas loop when it locks, (2) gain and phase imbalances in the Costas arm filters, (3) the "beat note" prematurely stopping the sweep because the threshold is too low, (4) signal distortion generated in the Costas arm filters, (5) AGC fluctuations which modulate the loop bandwidth, (6) threshold strategy before and after lock,(7) dc offsets in the phase detectors, (8) imbalances and nonlinearities in the in-phase and quadrature phase detectors. Figure 4-2.1 serves to illustrate the sweep waveform parameters which must be specified for any design.

4.3 Acquisition Time, Sweep Rate and the Cumulative Probability of Acquisition

The optimum sweep rate, R_r, which gives a ninety percent probability of acquisition is illustrated in Fig. 4.3-1. For comparison purposes, the stepping rates as found from Frazier and Page are also plotted. Notice at low values of C/N_0, the theory indicated that a slightly slower sweep rate is desired when compared with Frazier and Page. At higher values of C/N_0, the theory indicates that one should sweep faster than the Frazier-Page (FP) result indicates. This is understandable when one considers the fact that the FP results were based upon the fact that the loop is required to track its own sweep. The theoretical results are derived for the condition that the loop sweep is stopped once an indication of lock is established. Table 4.3-1 summarizes the sweep rates, both theoretical and as determined by the Frazier-Page empirical results. In the table T_{90} is the time required to achieve a 90% probability of acquisition, T_{acq} is the average acquisition time, and the time constant of the integrate and dump circuit which drives the lock detector threshold is T_s. Figure 4-3.2 illustrates the cumulative probability of acquisition versus time for three different design point C/N_0 values. In addition,

FIGURE 4.2-1. SWEEP WAVEFORM.

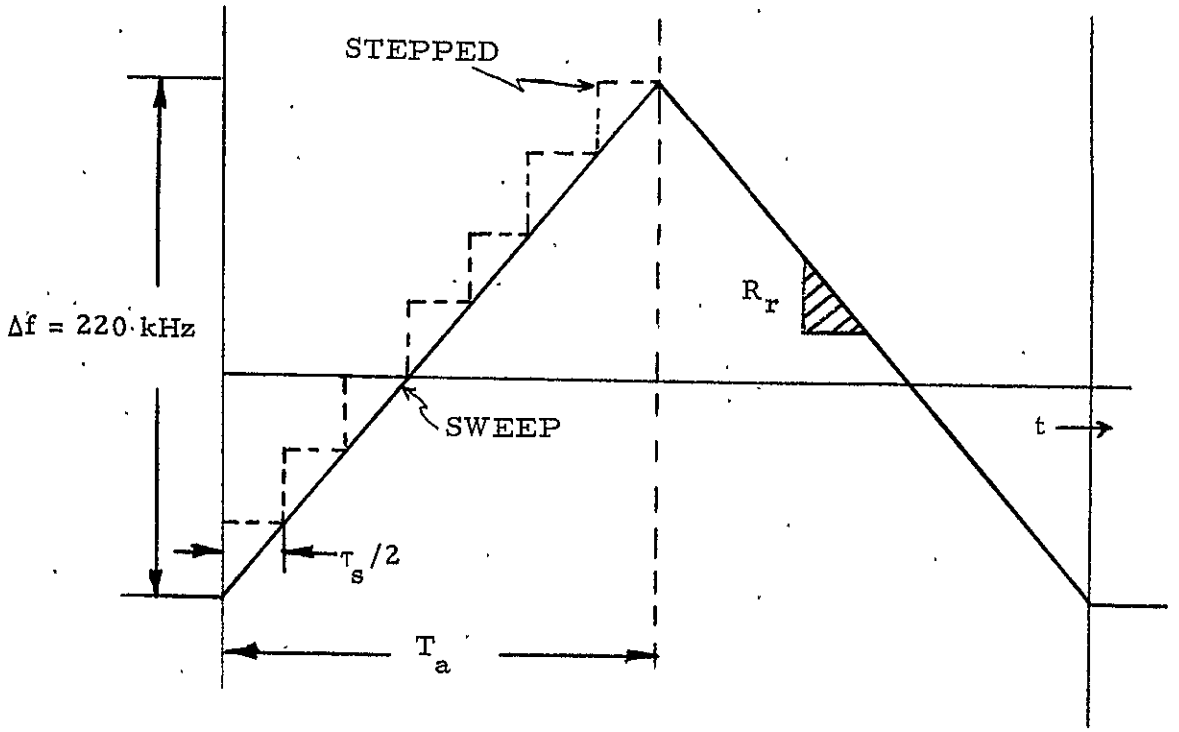


FIGURE 4.3-1. BI-ϕ CARRIER SWEEP RATE R_r VS C/N_0.

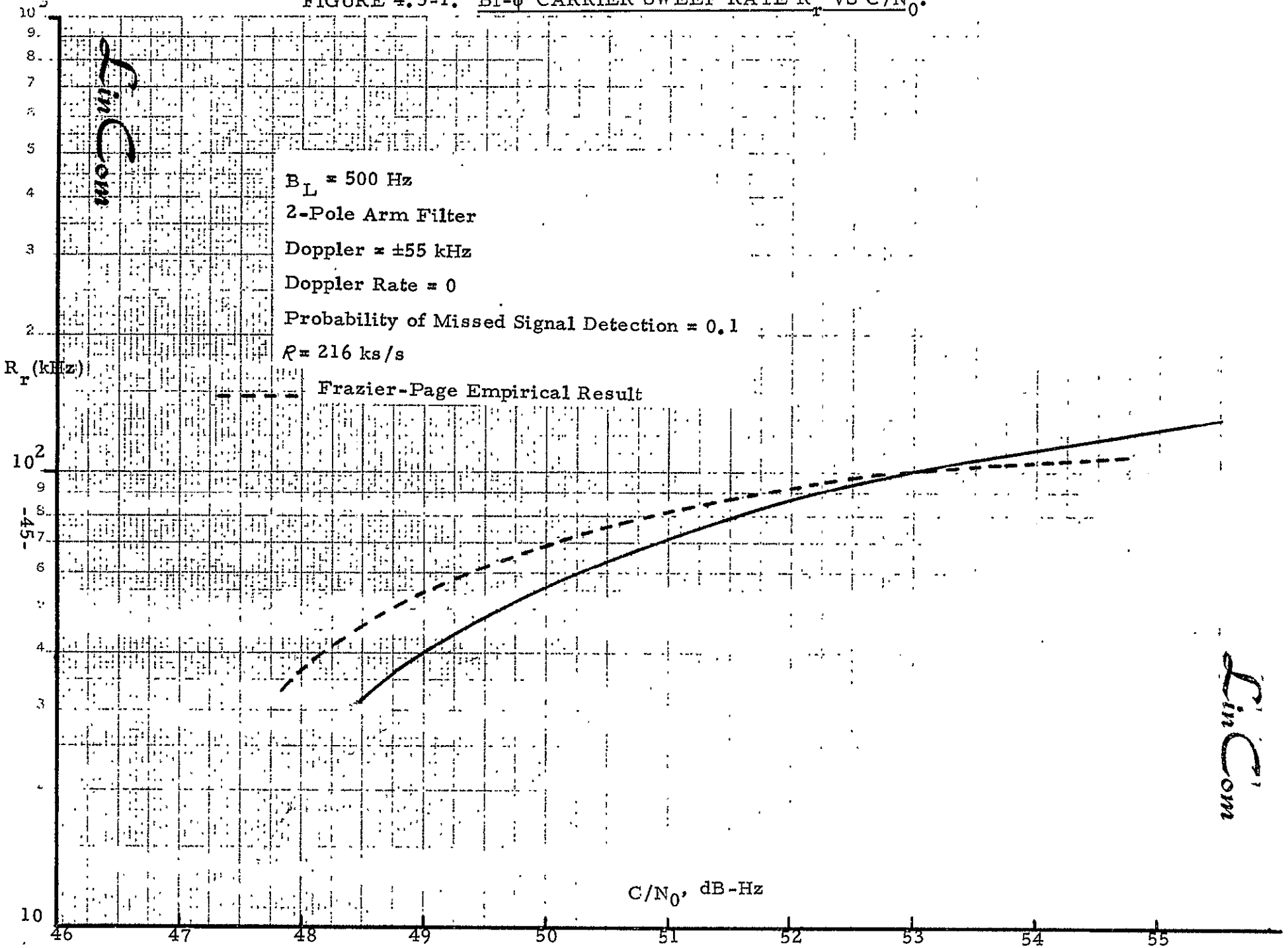
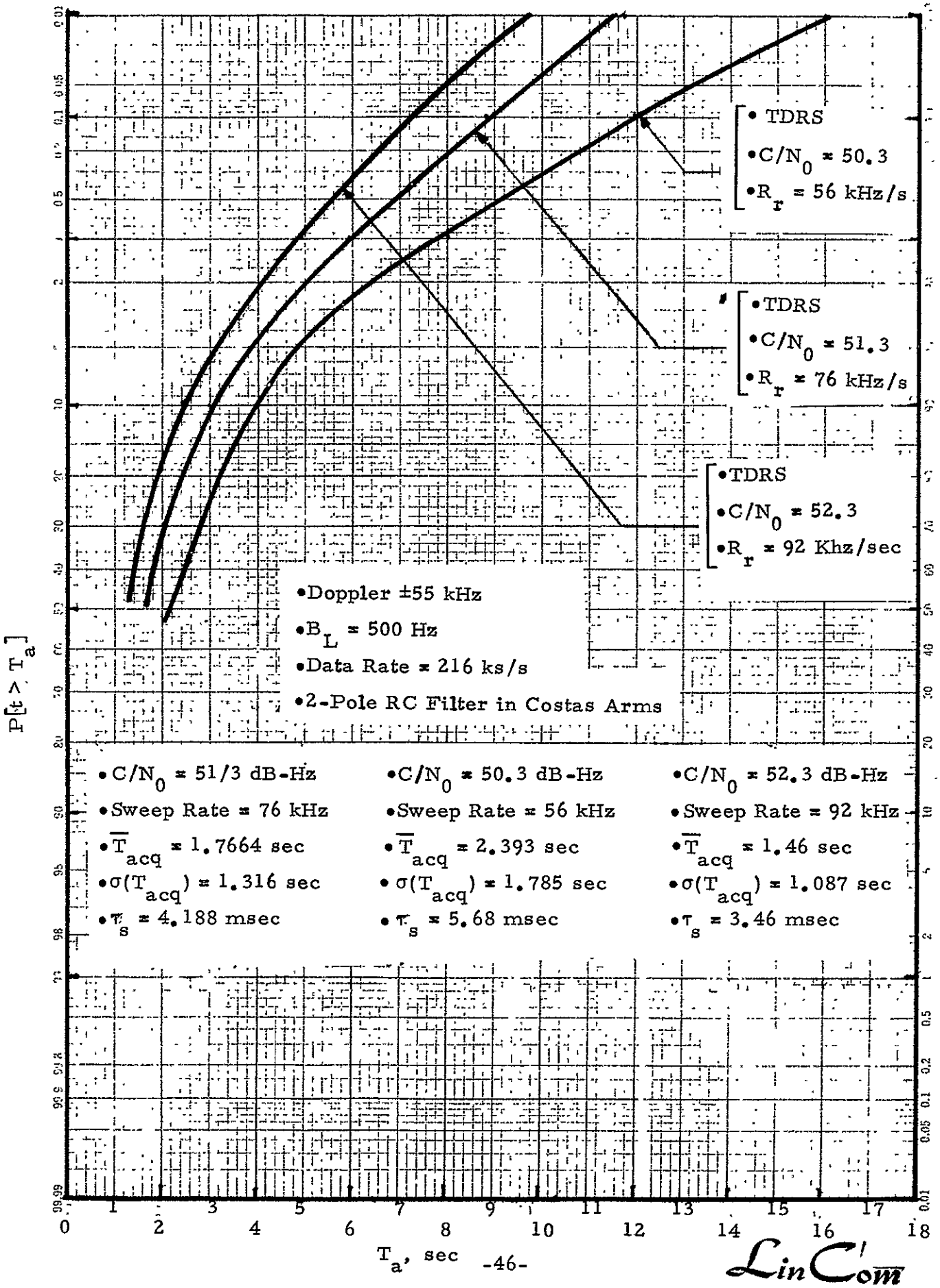


FIGURE 4.3-2. PROBABILITY OF CARRIER ACQUISITION AT $t \leq T_a$ SECONDS.



the mean and standard deviation of the acquisition time is also given in Fig. 4.3-2. The figure summarizes the sweep rate, average acquisition time, variance of the acquisition and integrator time constant τ_s for a given doppler of ±55 kHz and a loop bandwidth of 500 Hz. Notice that for C/N_0 = 52.3 dB-Hz the probability that the carrier loop will acquire in less than 4 seconds is 0.9. Table 4.3-2 summarizes the variations in the probability of missed sync detection β and false alarm α about the carrier recovery subsystem design point C/N_0 of 51.3 dB-Hz with a sweep rate of 80 kHz/sec. As observed from this table both probabilities are rather sensitivity to variations in C/N_0 about the design point value.

4.4 Lock Detection Subsystem Design

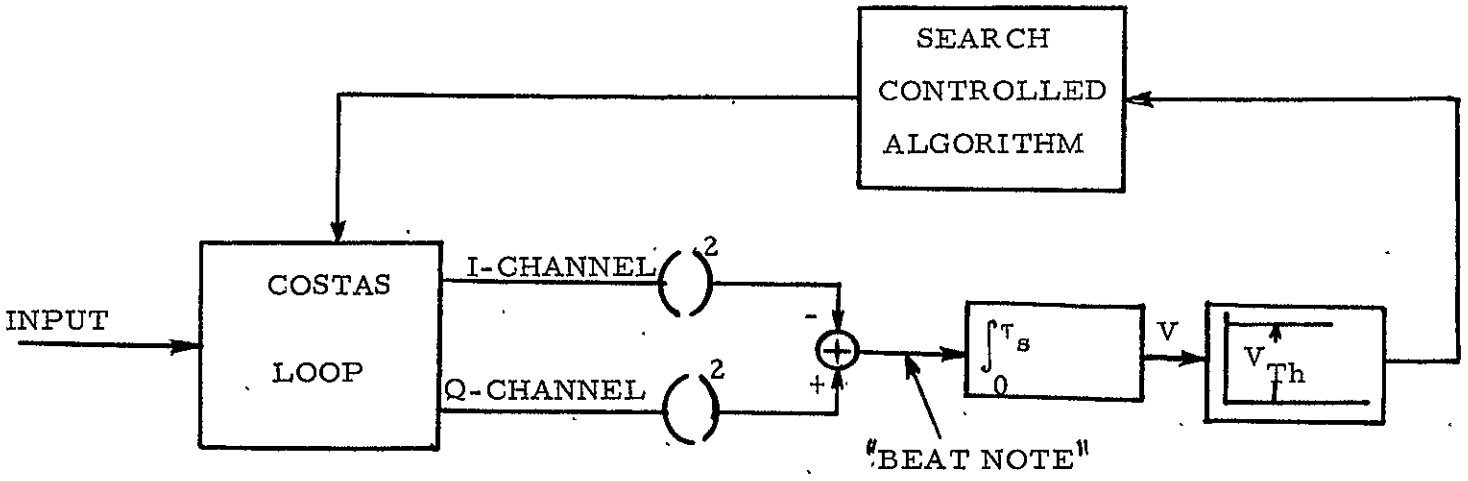
The problem of lock detection is of key concern because of the important role it plays in carrier acquisition and tracking system performance. Even though the Costas loop is capable of locking one must be able to identify this state in order to kill the sweep and reduce the offending loop stress. As is the case in any detection problem, there are various ways in which a lock detection system can be designed; however, of primary concern is the fact that the system should not greatly effect the overall acquisition time. Lock detection in a Costas loop can be accomplished by processing the difference of the squares, see Fig. 4.4-1, of the in-phase and quadrature arms to generate a signal proportional to cos 2φ where φ is the loop phase error. Alternatively, lock detection can be accomplished by processing the difference of the absolute values obtained from the in-phase and quadrature channels. The squaring circuit approach is preferable when the phase detector dc offsets are small, when the AGC gain variations are negligible, the Costas arm gain imbalance is negligible, and the arm squaring circuit imbalance is small. However, when these effects are considered large the absolute value approach

TABLE 4.3-1. SWEEP RATES, ACQUISITION TIME AND INTEGRATOR TIME CONSTANT SUMMARY

C/N_0, dB-Hz	R_r (kHz) Theoretical	R_r (kHz) Frazier-Page	T_{90}(sec)	$\overline{T}_{acq}$(sec)	τ_s (ms)
48.3	25	44	8.8	5.4	13
49.3	42	58	5.2	3.2	7.6
50.3	56	75	3.9	2.4	5.7
51.3	76	86	2.9	1.8	4.2
52.3	92	95	2.4	1.5	3.5
53.3	110	102	1	1.2	2.9

TABLE 4.3-2. VARIATIONS IN SYNCHRONIZATION PROBABILITIES ABOUT THE DESIGN POINT C/N_0 = 51.3 dB-Hz.

C/N_0 dB-Hz	α	β
47.3	0.189	0.436
48.3	0.165	0.363
49.3	0.142	0.242
51.3	0.100	0.119
53.3	0.066	0.065
55.3	0.043	0.037



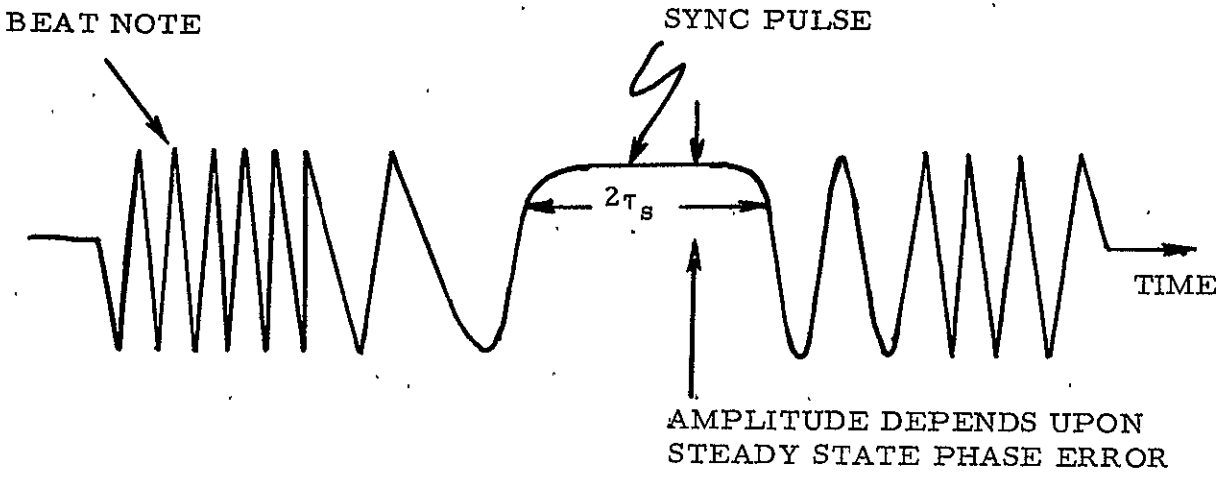
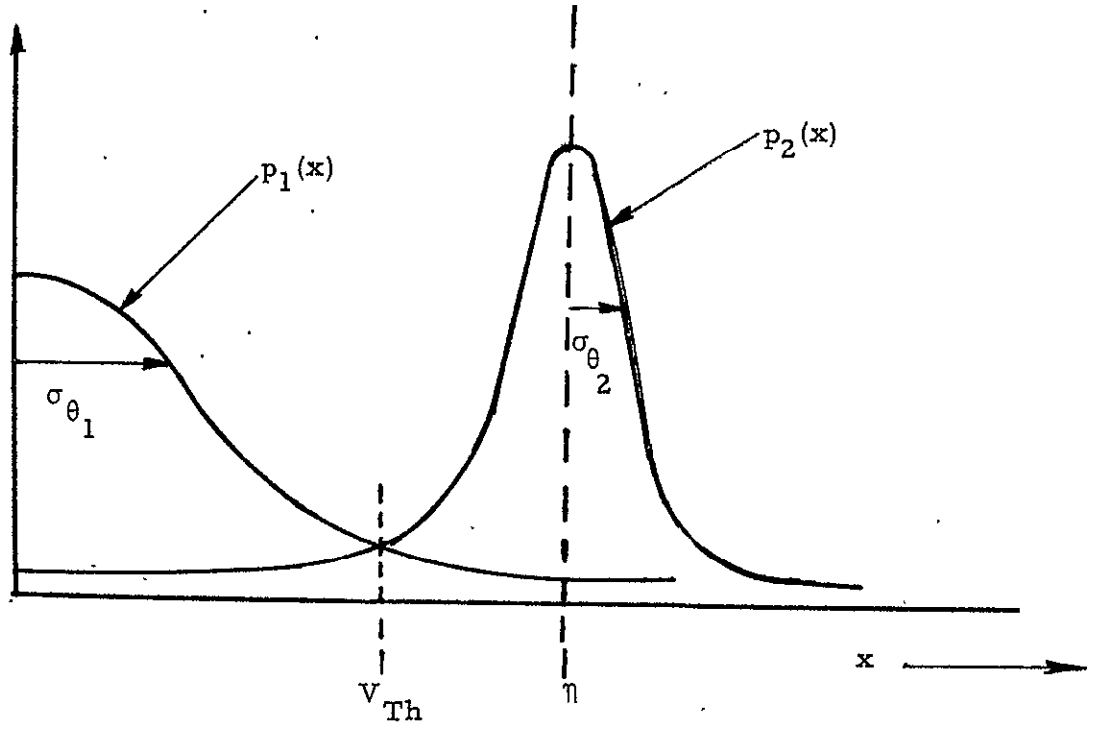


FIGURE 4.4-1. COSTAS LOCK DETECTION SYSTEM.

is preferable. For low SNRs, it appears that an optimum design would incorporate balanced squaring circuits and minimize other effects by careful hardware design. This approach which also allows for the sharing of common hardware with the AGC subsystem has been chosen for hardware simulation, see Fig. 4.4-1. In addition, in order to minimize acquisition time, the Costas loop cannot track its own sweep. Thus, prior to the loop locking, a 2φ beat note appears at the output of the difference channel, see Fig. 4.4-1. At some point in the sweep this beat note goes away and a sync pulse of duration τ_s is generated at the output of the difference channel. The duration of the pulse is controlled by the sweep rate and if the sweep is not killed the loop may, depending upon the sweep rate, break lock and start beating the sweep continues. In addition, the amplitude of the sync pulse is affected by the additive noise and loop jitter. An important point to note; however, is that the signal-to-noise ratio in the sync pulse can be increased by slowing the sweep with a subsequent increase in τ_s. Thus the sweep rate R_r is set by the probability of false alarm and probability of sync detection. Moreover, the optimum detection of a pulse in white Gaussian noise requires a matched filter or correlation operation. Therefore, the hardware simulation utilizes an integrate and dump circuit to process the sync pulse generated when the loop locks. The output of the integrate and dump circuit is compared to a threshold. This decision is used in the search controller to supervise the sweep circuit during acquisition and tracking.

Fig. 4.4-2 serves to illustrate statistics which form the basis of the decision to stop or continue the sweep. The probability density $p_1(x)$ represents the distribution of the voltages seen at the output of the integrate and dump circuit as the beat note

FIGURE 4.4-2. LOCK DETECTION STATISTICS.



EXAMPLE:

$\alpha = \beta = 0.1$

$C/N_0 = 51.3$ dB-Hz

$\eta = 1.0$; $V_{Th} = 0.41$

$\frac{\sigma_{\theta_1}}{\sigma_{\theta_2}} = 2$, $\tau_s = 2$ msec

$B_f = 250$ Hz

begins to disappear (low SNR assumed). In the parlance of detection theory it is useful in setting the threshold V_{th} for a preset false alarm probability. The variance σ_{θ_1} of the random variable x associated with $p_1(x)$ is larger than that of x when the loop is locked. This is due to the fact that the beat note adds noise into the integrate and dump output when the loop is near the lock state (low SNR assumed). The probability of missed sync detection β is then set by mean, η, and the variance σ_{θ_2} associated with the integrate and dump voltages after the loop locks. The state of affairs between the various detection system parameters is illustrated in Fig. 4.4-2 for $C/N_0 = 51.3$ dB-Hz. For a sync pulse of duration 2 msec the noise bandwidth of the integrate and dump circuit is $B_f = 250$ Hz. Table 4.4-1 summarizes the optimum values for the integrate and dump time τ_s, or equivalently, B_f for various C/N_0.

The detailed algorithms used to verify sync and monitor tracking are discussed in Volume II.

Fig. 4.4-3 illustrates a plot of the SNR present at the input to the AGC loop filter versus signal energy per bit to noise ratio E_b/N_0. Note the sensitivity of the SNR as a function of Costas arm filter gain imbalance.

4.5 Costas AGC Subsystem Design

Various approaches can be used to provide gain control for setting the Costas loop design point operating conditions. These include:

1. Coherent AGC
2. Coherent AGC Incorporating a Bandpass Limiter (BPL)
3. Noncoherent During Acquisition, AGC Switched to Coherent After Acquisition
4. Noncoherent AGC

Coherent AGC cannot be provided until the loop is locked. This is too late, therefore this approach is only useful after the loop

TABLE 4.4-1. LOCK DETECTION INTEGRATE AND DUMP TIMES FOR VARIOUS VALUES OF C/N_0

C/N_0, dB-Hz	τ_s, msec	B_f, Hz
48.3	5	50
50.3	3	167
51.3	2	250
54.3	1.5	350

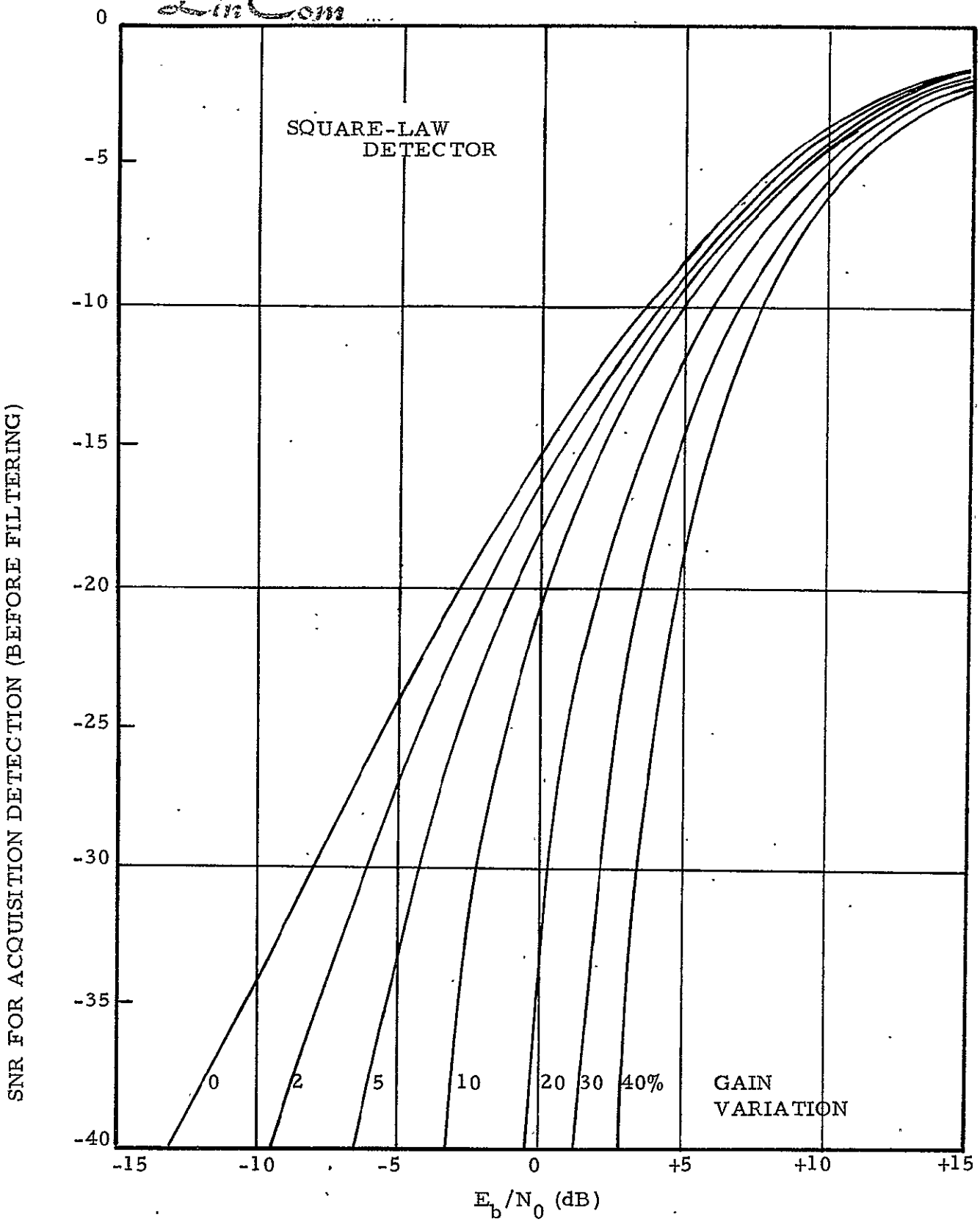


FIGURE 4.4-3. SNR VERSUS E_b/N_0 FOR VARIOUS ARM FILTER GAIN VARIATIONS.

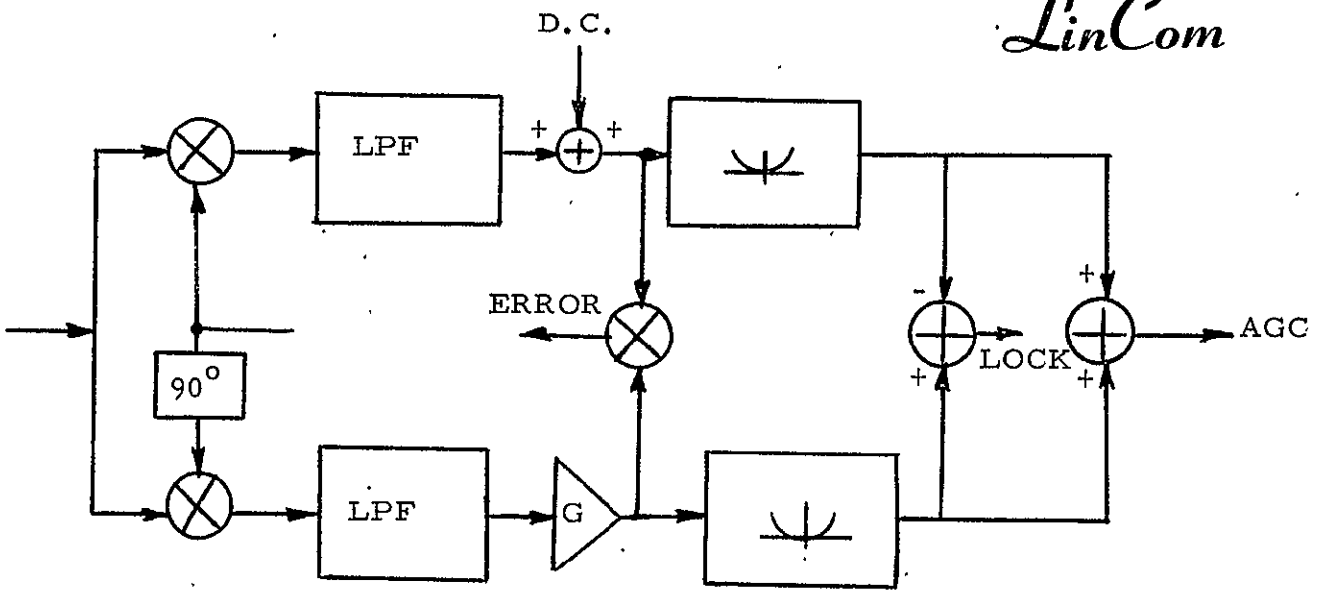
locks. Approach two, which uses a bandpass limiter is suitable; however, the presence of a BPL prior to phase detection degrades system performance by 2 dB when the signal-to-noise ratio is low and BPSK modulation is present. Approach three, is also suitable; however, this is more complicated to implement than any of the other three approaches and one must contend with a switching transient when the AGC is switched. Approach three is attractive from the viewpoint that a coherent AGC can establish a "tighter" control on the loop damping and loop bandwidth during tracking. When hardware degradations are accounted for this technique may be preferable. For the hardware simulation, the noncoherent AGC technique has been chosen for carrier acquisition as well as tracking. This is because it provides adequate performance when implementation imperfections (dc offsets, arm gain imbalance) are not considered.

Noncoherent AGC can be provided by filtering the sum of the squares of the in-phase and quadrature signals appearing at the output of the Costas arm filters, see Fig. 3-1. The time constant chosen for C/N_0 = 51.3 dB-Hz is approximately 20 msec; however, anything larger is probably adequate and must be determined at the systems level after the system operating scenario is established.

Fig. 4.5-1 functionally illustrates the AGC techniques and summarizes implementation imperfections which must be considered in a hardware design.

5.0 PN Sync Subsystem (PNSS) Design and Analysis

This section of the report discusses various candidate techniques for acquisition and tracking of a pseudonoise code (PN) in a spread spectrum receiver at low signal-to-noise ratios and large code doppler. The technique chosen for the hardware simulation incorporates a wideband noncoherent square law integrate and dump detector for code acquisition and an algorithm



- COSTAS IMPLEMENTATION IMPERFECTIONS
  - NONLINEARITIES IN PD
  - GAIN IMBALANCE
  - DC OFFSETS
- DELETERIOUS EFFECTS
  - LOOP ACQUISITION
  - LOCK INDICATION
  - MONITOR AND VERIFY
  - AGC
  - DATA CHANNEL

FIGURE 4.5-1. COSTAS NONCOHERENT AGC TECHNIQUE.

for controlling and supervising the PNSS during all phases of operation. In the tracking mode a τ-dither loop is selected with two bandwidths; one for code sync acquisition and another for tracking. The design point C/N_0 = 51.3 dB-Hz and a code doppler of 300 chips/sec is assumed present on a PN code clocked at 11.232 MHz/sec.

5.1 PNSS Functional Requirements

Figure 5.1-1 illustrates a functional diagram of the PNSS. Major functions which this system must perform include:

(1) Despreading the Received Signal

(2) Maintain Code Alignment Between the Received and Local Code

(3) Perform Acquisition, In Lock Detection and the Sync Monitoring Process

In the design of the despreader various considerations play key roles. These include (1) the effects of the RF filter, e.g., the generation of code intersymbol interference and the group delay through the filter, (2) selection of an optimum code sync acquisition algorithm and a sync monitoring algorithm, (3) design of the code tracking loop and (4) the interactions with the carrier sync system (CSS) and the symbol sync system (SSS).

5.2 PN Code Acquisition

Despreading the received Manchester encoded BPSK signal is a problem because of the low signal-to-noise ratios and high code doppler. The situation is illustrated in Fig. 5.2-1 where it is shown that the presence of the signal plus noise gives rise to a signal level that is hard to distinguish from the case where noise along is present.

The acquisition process includes estimation of the noise level, subtracting the noise estimate from a filtered and integrate sample of the observed signal, and from this make a determination of the presence or absence of a signal for the particular code phase chosen. More specifically Fig. 5.2-2 illustrates and summarizes

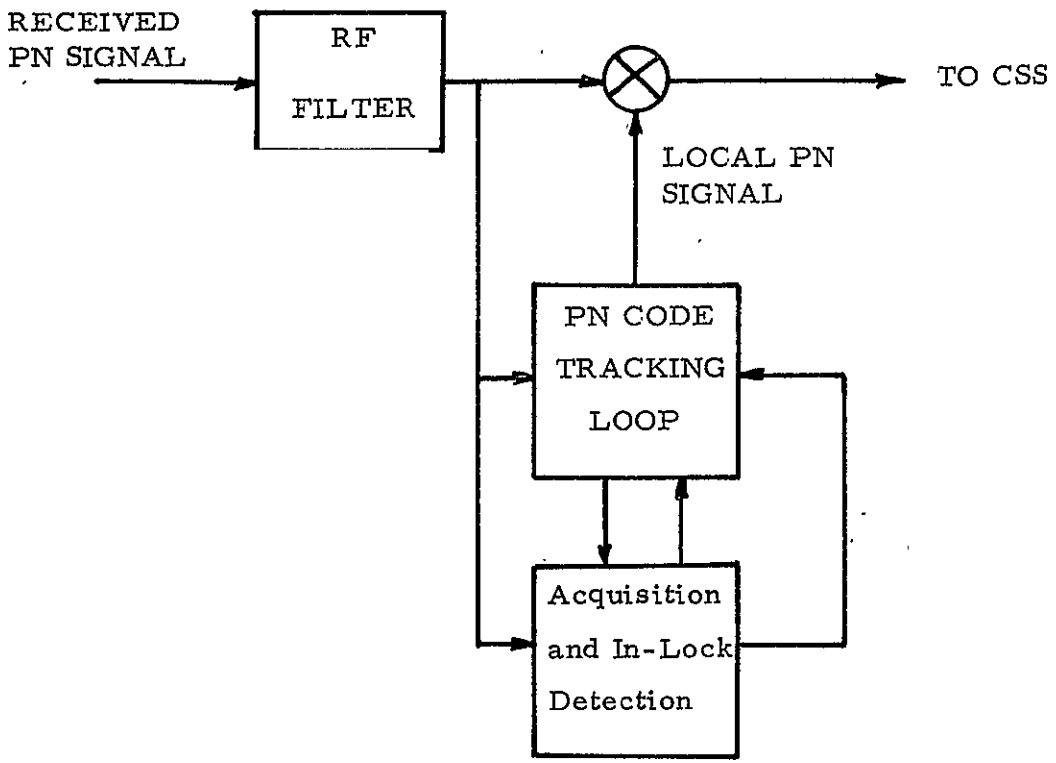
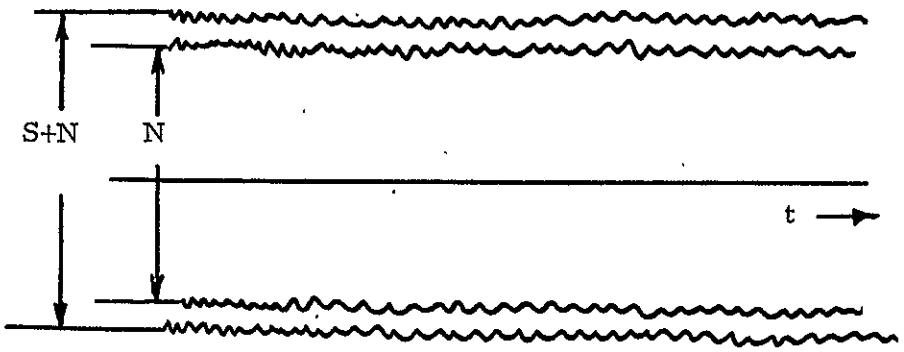
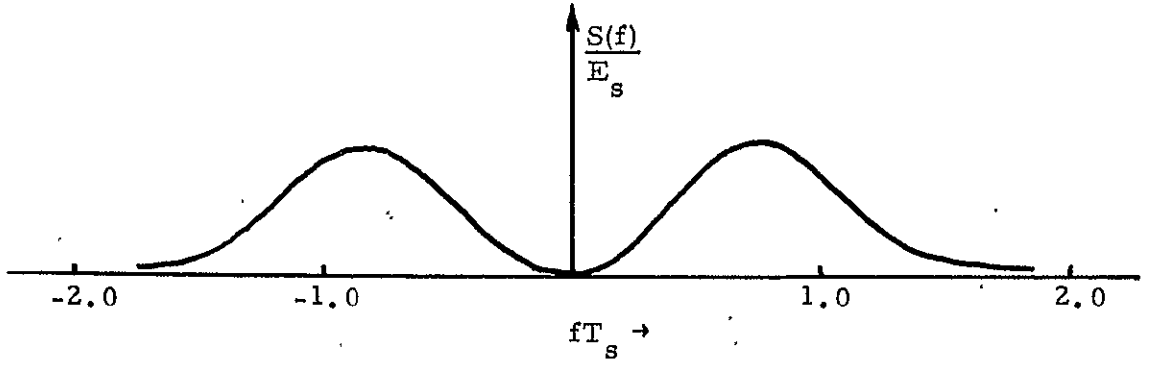


FIGURE 5.1-1. PN DESPREADER FUNCTIONAL DIAGRAM.

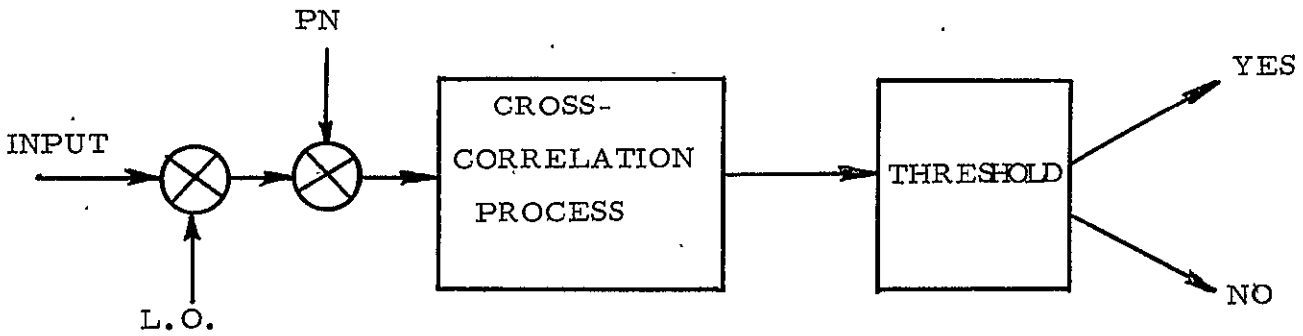
FIGURE 5.2-1. CODE ACQUISITION PROBLEM.



SIGNAL-PLUS NOISE S/N ≃ -20 dB



MANCHESTER SPECTRUM



- COHERENT PROCESS
  - BPF/INTEGRATE
  - MATCHED FILTER
  - I AND D
- NONCOHERENT PROCESS
  - BPF/ENVELOPE/INTEGRATE
  - MATCHED FILTER/ENVELOPE
  - I AND D/ENVELOPE

FIGURE 5.2-2. TECHNIQUES FOR GENERATING DECISIONS TO DRIVE CODE SYNC ALGORITHM.

alternate approaches (coherent vs noncoherent) which can be considered as candidate techniques for generating decisions that can be used to govern the acquisition process. Since the code must be acquired in the presence of data with an unknown clock epoch, a noncoherent crosscorrelation process followed by envelope detection (ED) is optimum. Figure 5.2-3 summarizes the design considerations and design parameters of concern in the implementation of the noncoherent correlation process. The selected design parameters will set the performance of the PN sync system once a particular code acquisition algorithm is chosen.

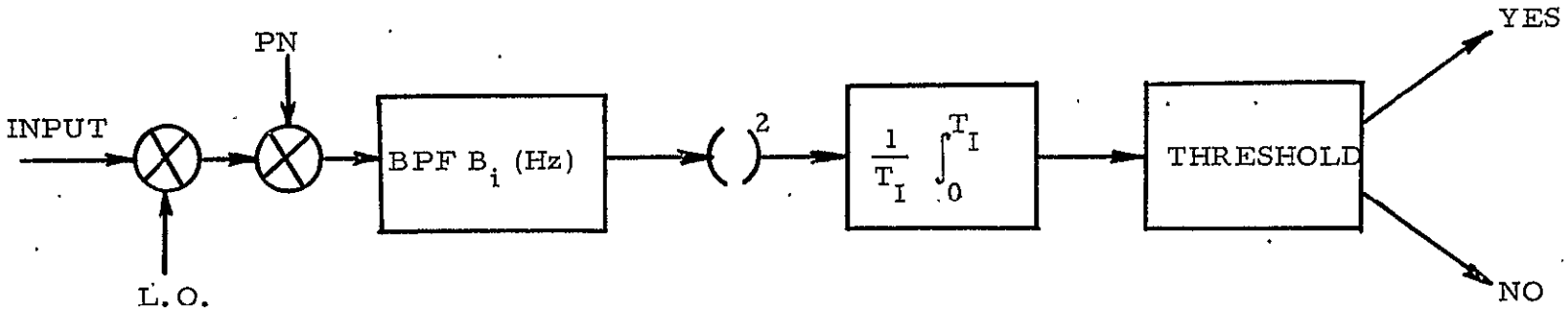
5.3 Code Acquisition Algorithms

Various search algorithms were investigated during the contract period. These included: (1) maximum likelihood (parallel search), (2) serial maximum likelihood (serial search), (3) sequential probability ratio tests, (4) parallel acquisition due to Hopkins (Ref. 15). A maximum likelihood parallel search requires too much hardware and a true sequential probability ratio test is difficult to implement; however, the algorithm suggested by Hopkins (Ref. 15) appears to be implementable and performs much like a serial maximum likelihood test. In addition, Hopkins correctly suggests that the code tracking loop be operating in parallel during each particular code phase test. When the code phase is rejected Hopkins (Ref. 15) suggests discharging the loop filter. For the hardware simulation, the Hopkins approach has been selected because it gives near optimum performance. In the next section, the acquisition time hold-in time tradeoffs are made.

5.3.1 PN Acquisition Algorithm Comparisons

During the contract period the performance of various algorithms which incorporate the Hopkins approach (Ref. 15) were investigated. The study included algorithms which employ the reset counter concept, and those which employ an up-down counter concept.

FIGURE 5.2-3. NONCOHERENT CORRELATION PROCESS.



- DESIGN CONSIDERATIONS
  - SELF NOISE
  - FILTER BANDWIDTH
  - DOPPLER
  - DATA TRANSITION DENSITY
  - FILTER AMPLITUDE AND PHASE CHARACTERISTIC
  - PARTIAL CORRELATIONS
- DESIGN PARAMETERS
  - B_i - NOISE BANDWIDTH
  - T_I - INTEGRATION TIME
  - V_{Th} - THRESHOLD
  - (α, β) - POWER OF TEST

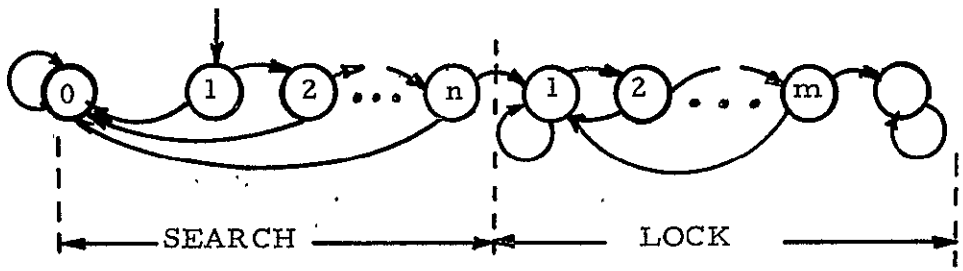
Figure 5.3.1-1 serves to illustrate the two counter schemes just mentioned. Notice the two modes, search and lock, and that each mode has n and m states respectively. The choice of n and m are determined by such considerations as average acquisition time, mean hold-in time, and the duration of signal drop-outs.

In order to make the necessary tradeoffs for final selection of an algorithm and its associated parameters, various reset and up-down counter/threshold arrangements and code integration times were studied using a digital computer. Certain results from this tradeoff study are summarized in Figs. 5.3.1-2, 5.3.1-3 and 5.3.1-4. Here T_1 represents the post correlation integration time. In addition, Δf represents the code doppler rate in chips (bits)/sec and serves to set the probability of false alarm which determines the threshold for each state. As noted best performance is achieved by setting the threshold high and then lowering it as the degree of confidence of the lock state increases. Figures 5.3.1-5 and 5.3.1-6 illustrate comparisons of the mean hold-in time for various up-down and reset counter arrangements. In all cases, the mean hold in time exceeded one hour for C/N_0 greater than approximately 48 dB-Hz. Figure 5.3.1-7 represents the probability density function of code acquisition time for C/N_0 = 48.3 dB-Hz. This curve was produced by Dr. Phillip Hopkins and Jim Benelli of Lockheed.

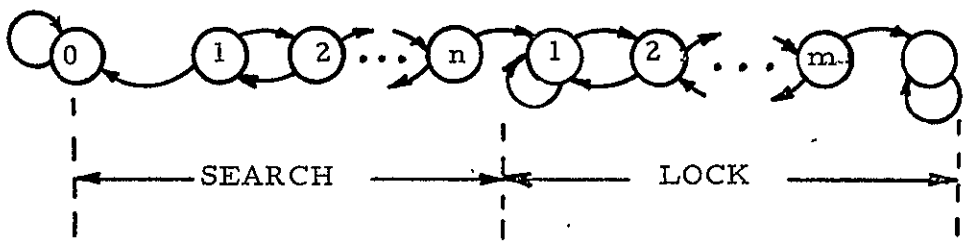
A summary comparison of the various algorithms is given in Table 5.3.1-1 for two different SNRs. The algorithm chosen for the hardware simulation is a reset counter arrangement which possesses three search states and twenty lock states. The detailed performance of the chosen algorithm for the hardware simulation is illustrated in Fig. 5.3.1-8. Twenty lock states is required in order to give the desired "fly-wheel"

FIGURE 5.3.1-1. PN ACQUISITION ALGORITHMS.

•RESET COUNTER



• UP-DOWN COUNTER



•HYBRID

FIGURE 5.3.1-2. PN ACQUISITION TIME VS SNR.

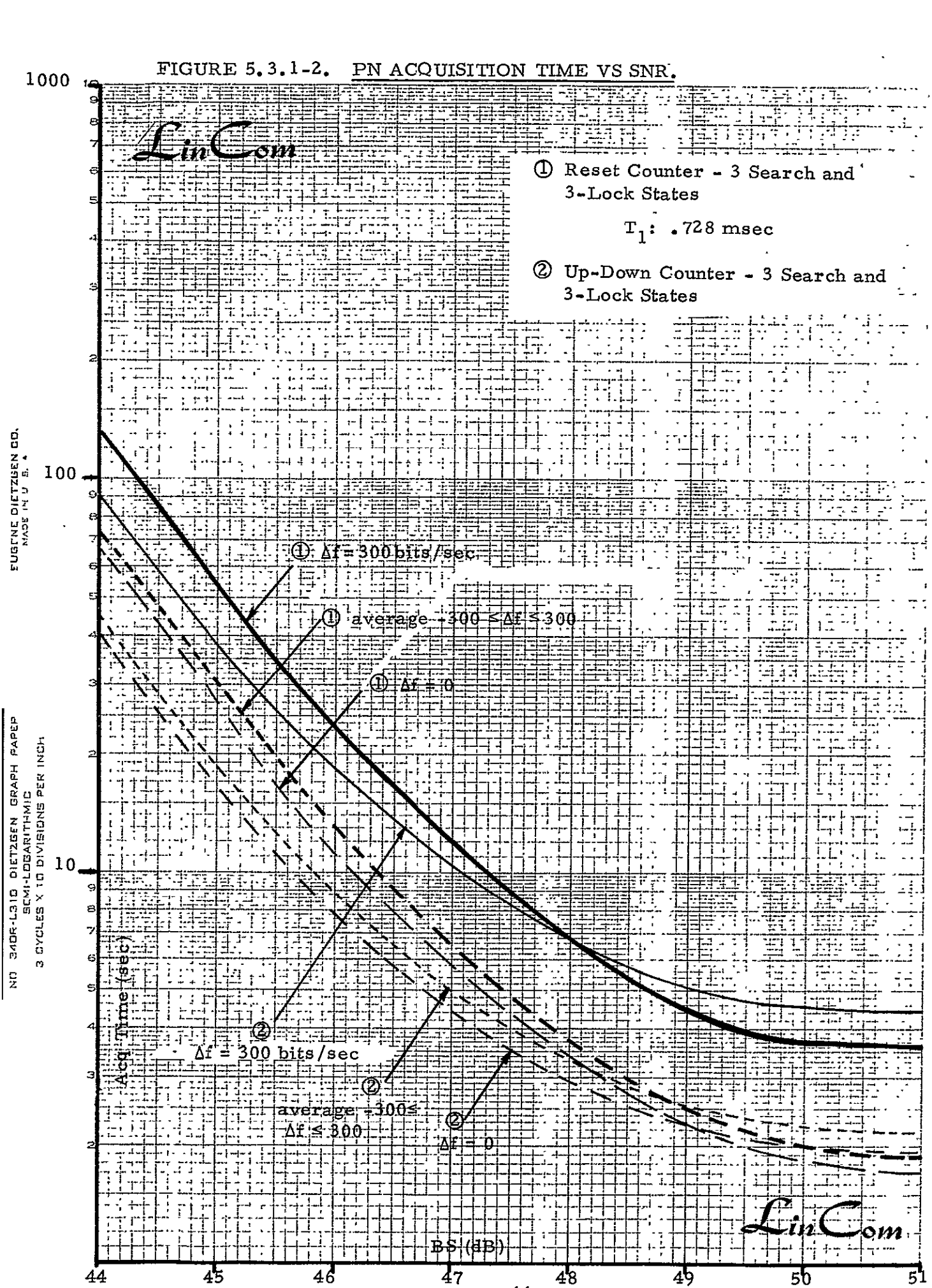


FIGURE 5.3.1-3. PN ACQUISITION TIME VS SNR.

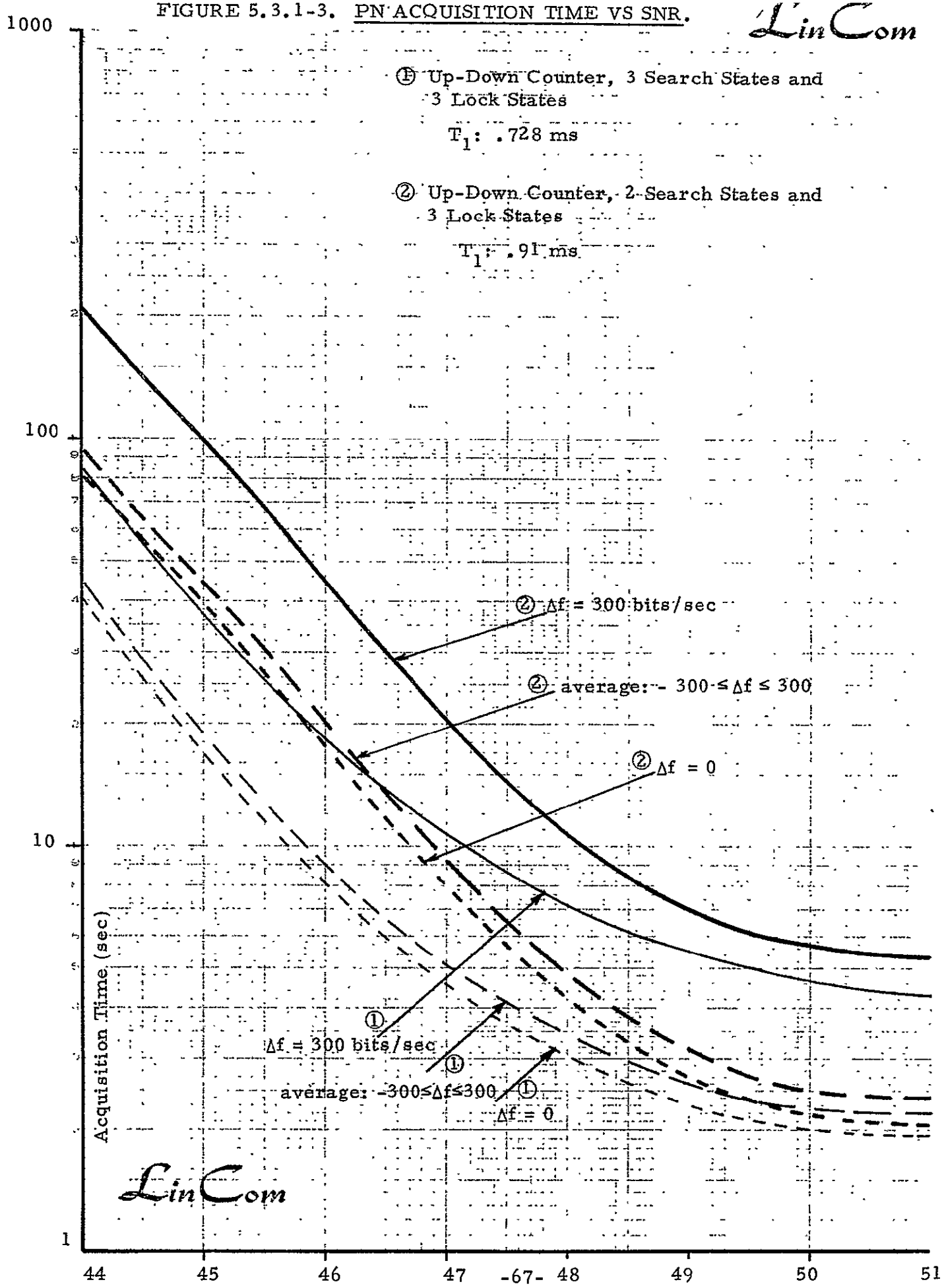


FIGURE 5.3.1-4. PN ACQUISITION TIME VS SNR.

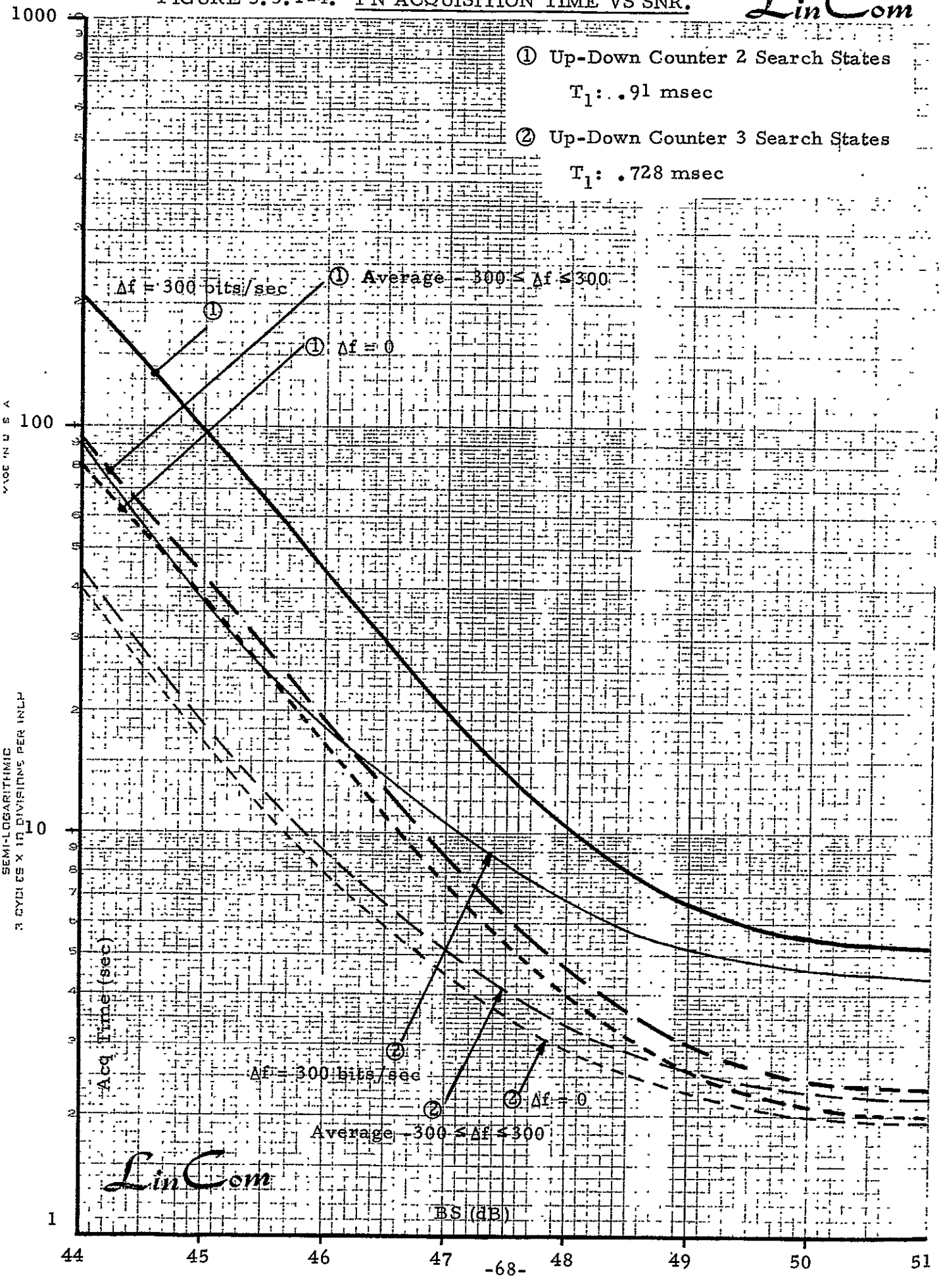


FIGURE 5.3.1-5. PN HOLD-IN TIME VS C/N_0.

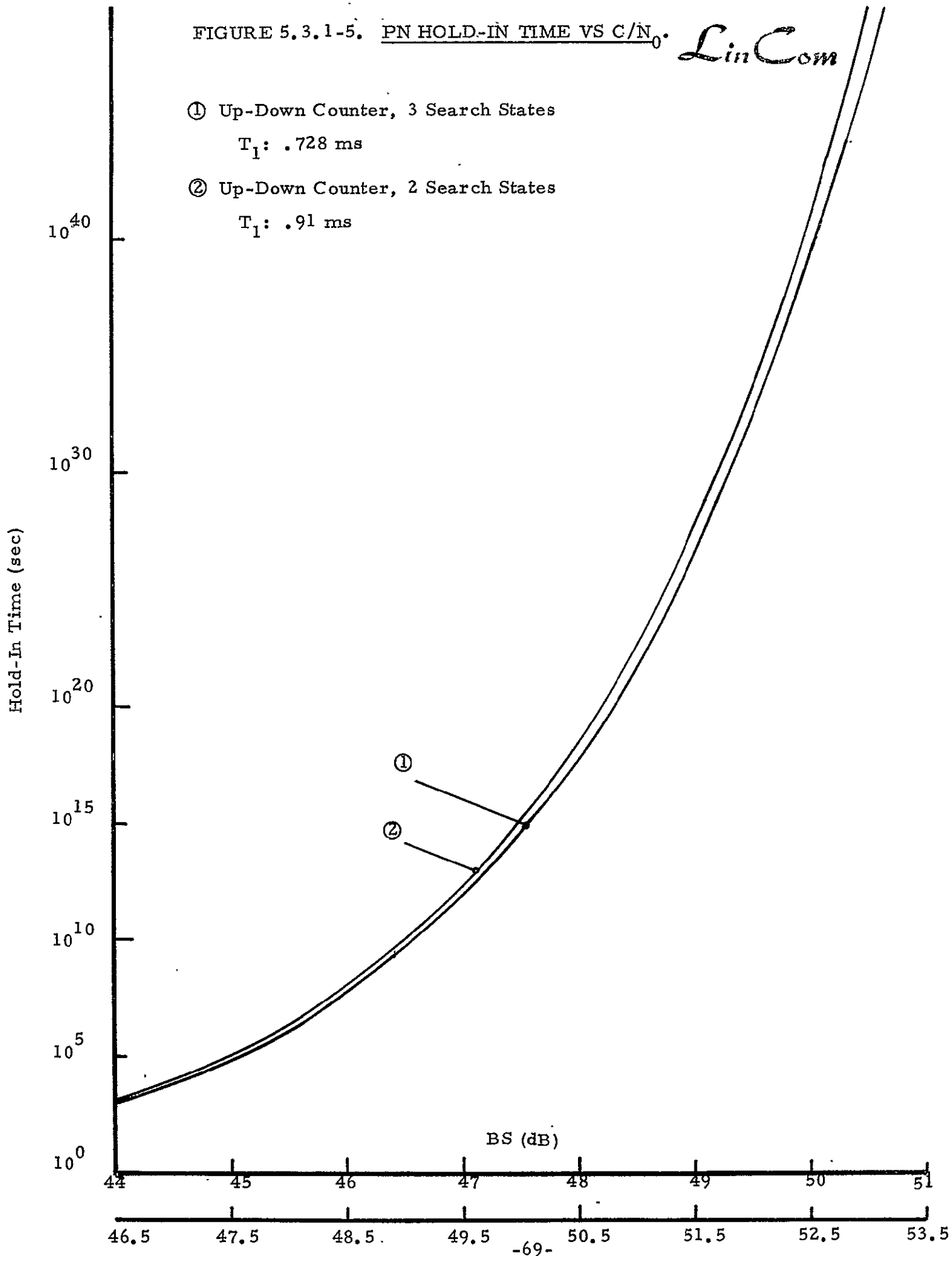


FIGURE 5.3.1-6. PN HOLD-IN TIME VS C/N_0.

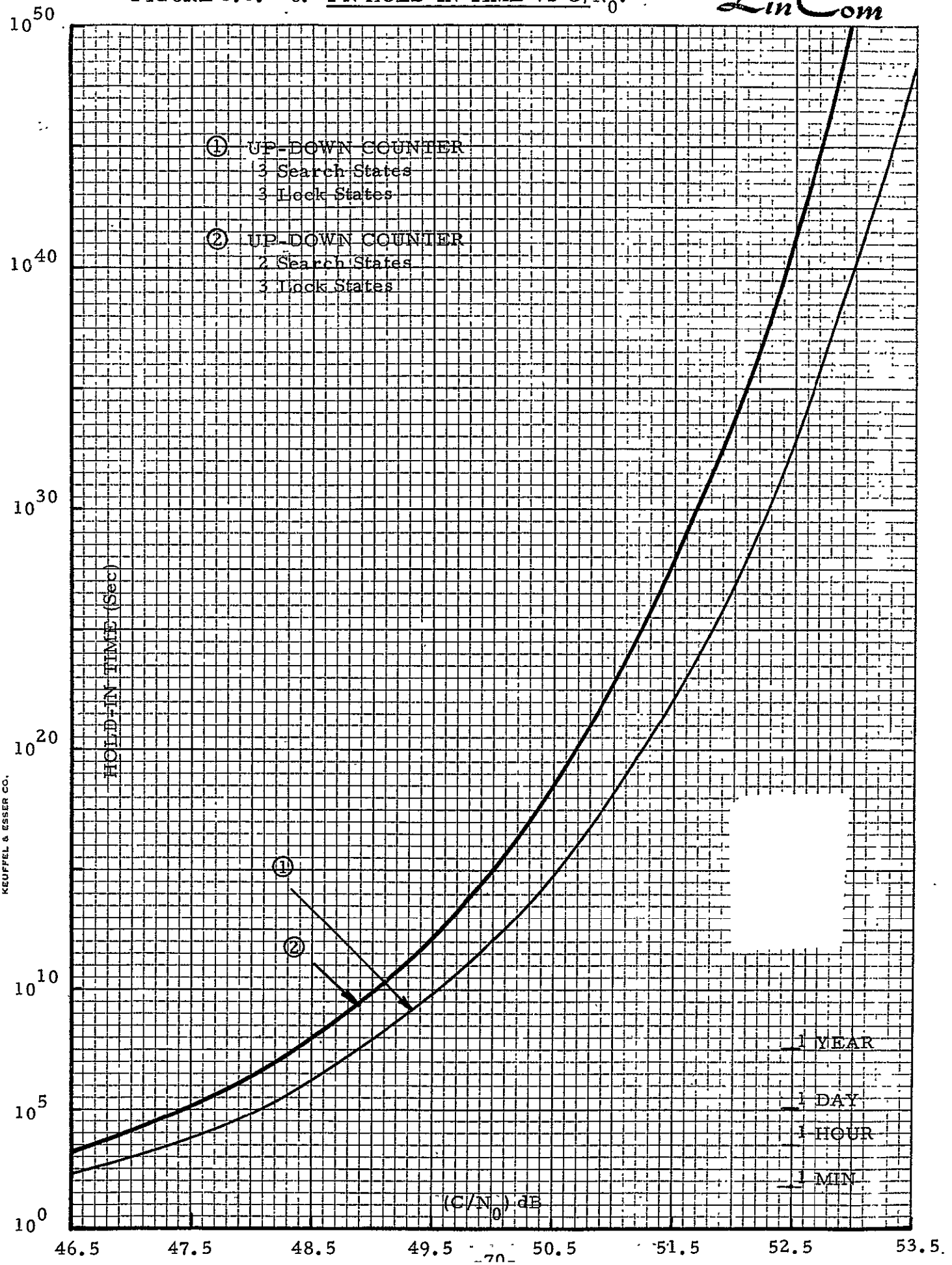


FIGURE 5.3.1-7. PROBABILITY DENSITY FUNCTION OF THE PN ACQUISITION TIME.

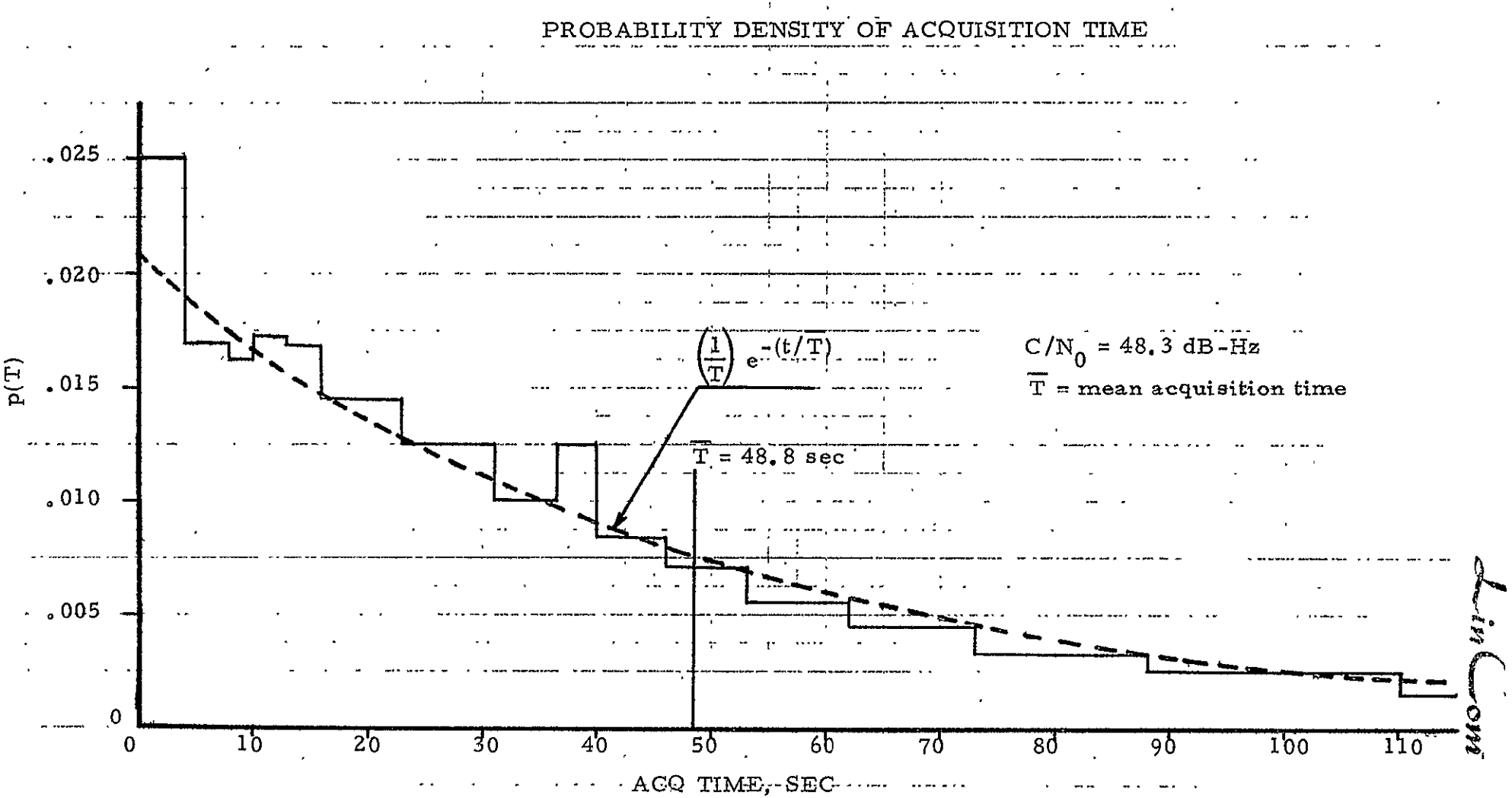
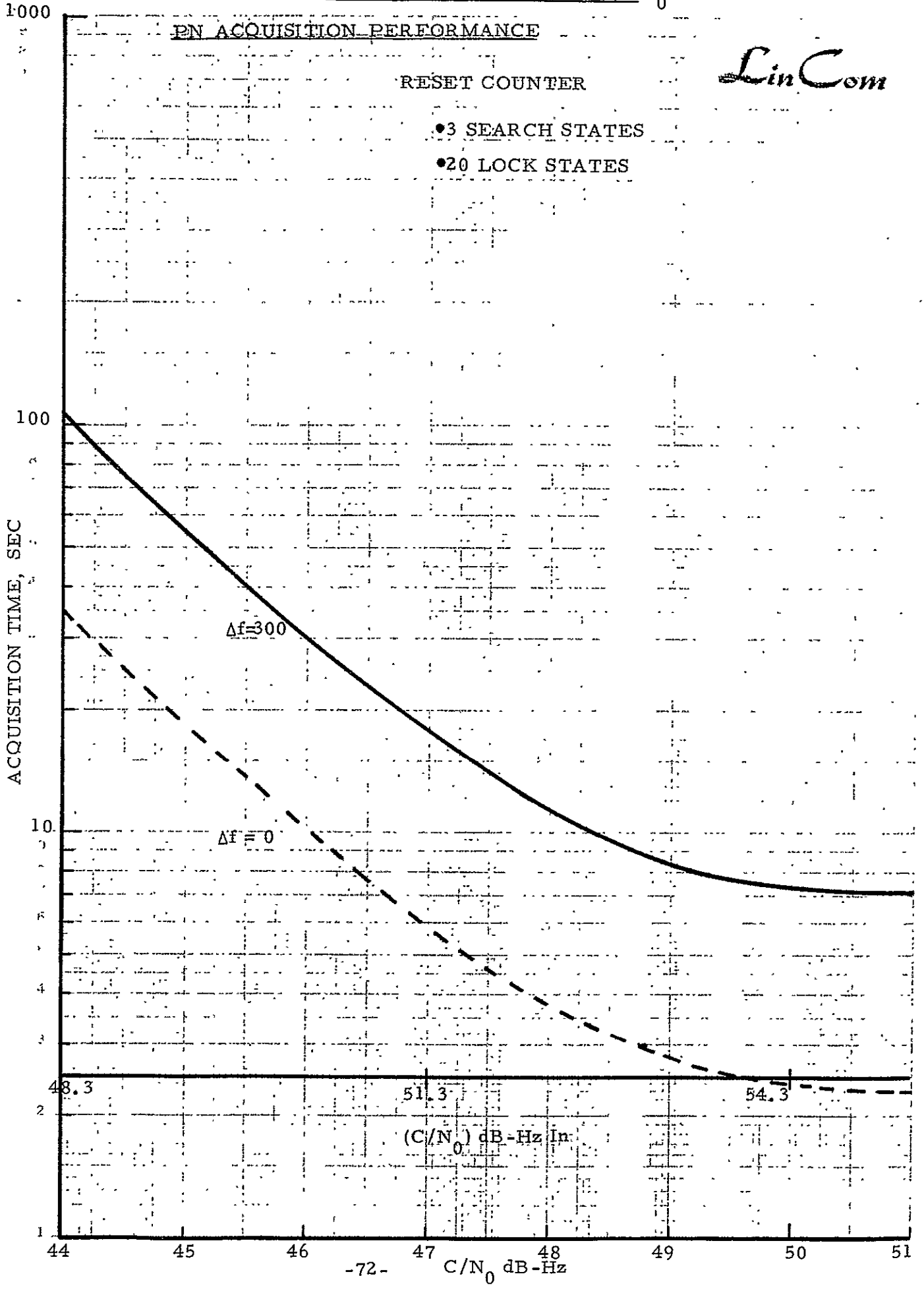


FIGURE 5.3.1-8. PN ACQUISITION TIME VS C/N_0.



LinCom

TABLE 5.3.1-1 ALGORITHM COMPARISONS

Type	Search States	Lock States	Integration Time		Worst Case Acq. Time*		Acq. Time - Zero Doppler*	
			Search	Lock	C/N_0=48.3dBHz	C/N_0=51.3dBHz	C/N_0=48.3dBHz	C/N_0=51.3dBHz
U/D	3	3	.91 ms	4(.91)ms	205 sec	20.5 sec	80 sec	7.6 sec
U/D	3	3	.73; 4(.73)	5(.73)	90 sec	10.5 sec	39 sec	4.5 sec
U/D	3	3	.73;6(.73)	6(.73)	83 sec	10.5 sec	40 sec	4.5 sec
R.S.	3	3	.73;5(.73)	5(.73)	132 sec	12 sec	66 sec	5.9 sec
R.S.	3	20	.91;4(.91)	4(.91)	105 sec	17 sec	35 sec	5.7 sec

DOPPLER = 300 Chips/Sec

*LOSSES - 2.5 dB (↑ $\frac{1}{4}$ CHIP OFF) + 0.4 dB (↑ RF FILTER) + 1.4 dB (↑ CORRELATION) = 4.3 dB

HOLD IN TIME GREATER THAN ONE HOUR

CHOICE - SELECT RESET COUNTER WITH 3 SEARCH AND 20 LOCK STATES FOR HARDWARE SIMULATION

action during signal dropouts. Finally, Figure 5.3.1-9 illustrates the sensitivity of system performance due to threshold variations of 0.1, 0.5, 1 and 1.5% respectively. Figure 5.3.1-10 illustrates the sensitivity of an alternate PN sync acquisition algorithm which was studied during the contract period.

5.4 PN Code Tracking Loop Design and Tradeoffs

PN code tracking can be accomplished by one of two well known techniques. These two techniques, which were investigated during the contract period, include the delay-locked loop (DLL) and a time-shared or τ-dither loop. Since it is presumed that the data is present during initial lock up an envelope correlating type DLL is required. On the other hand, a linear correlator requires feedback from the data detector, which implies bit synchronization, and neither of these requirements appear to be feasible from an implementation point of view. Therefore, the envelope correlating DLL will be compared with the time-shared delay locked loop.

It is well known (Ref. 16) that the delay-locked loop gives a superior jitter performance (3 dB) when compared to the time-shared DLL; however, the delay-locked loop requires two-parallel RF channels of signal processing. Mismatches in these channels rapidly degrades performance at low signal-to-noise ratios and most practical implementations prefer an approach which time shares a common channel. For the hardware simulation the time-shared DLL has been chosen.

A functional diagram of the time-shared DLL is illustrated in Fig. 5.4-1. The bandwidth of the BPF has been chosen so as to maximize the probability of detection, see Fig. 5.4-1. In Fig. 5.4-2 the pull in transients of the loop are shown. The acquisition bandwidth is chosen on the basis of loop jitter performance combined with the fact that the loop will not acquire the code doppler when the codes are misaligned by ± 1.5 chips.
For $C/N_0 = 48.3$ dB-Hz, and acquisition bandwidth

FIGURE 5.3.1.9. PN ACQUISITION TIME VS SNR.

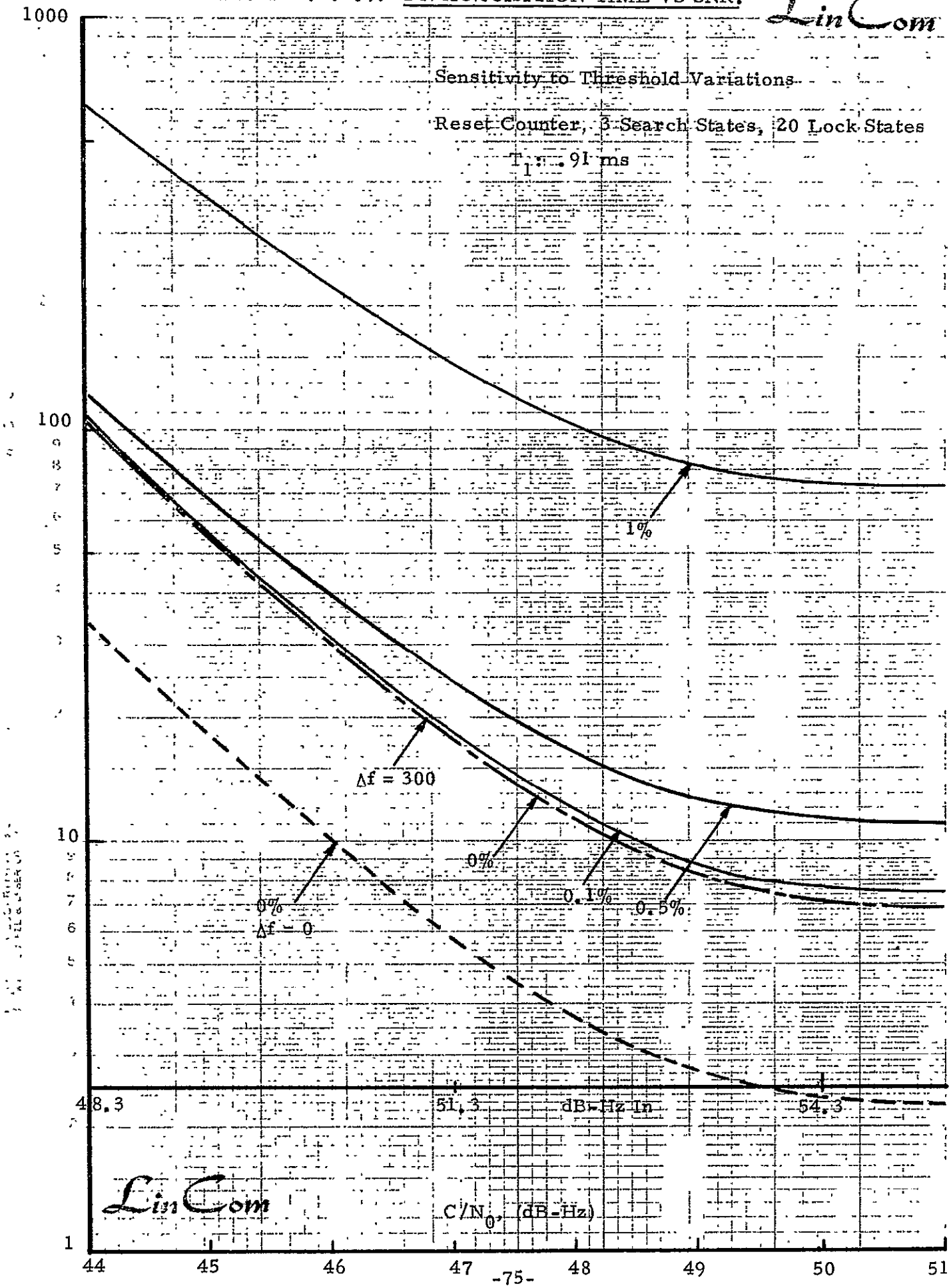


FIGURE 5.3.1-10. PNSS ACQUISITION TIME VS C/N_0.

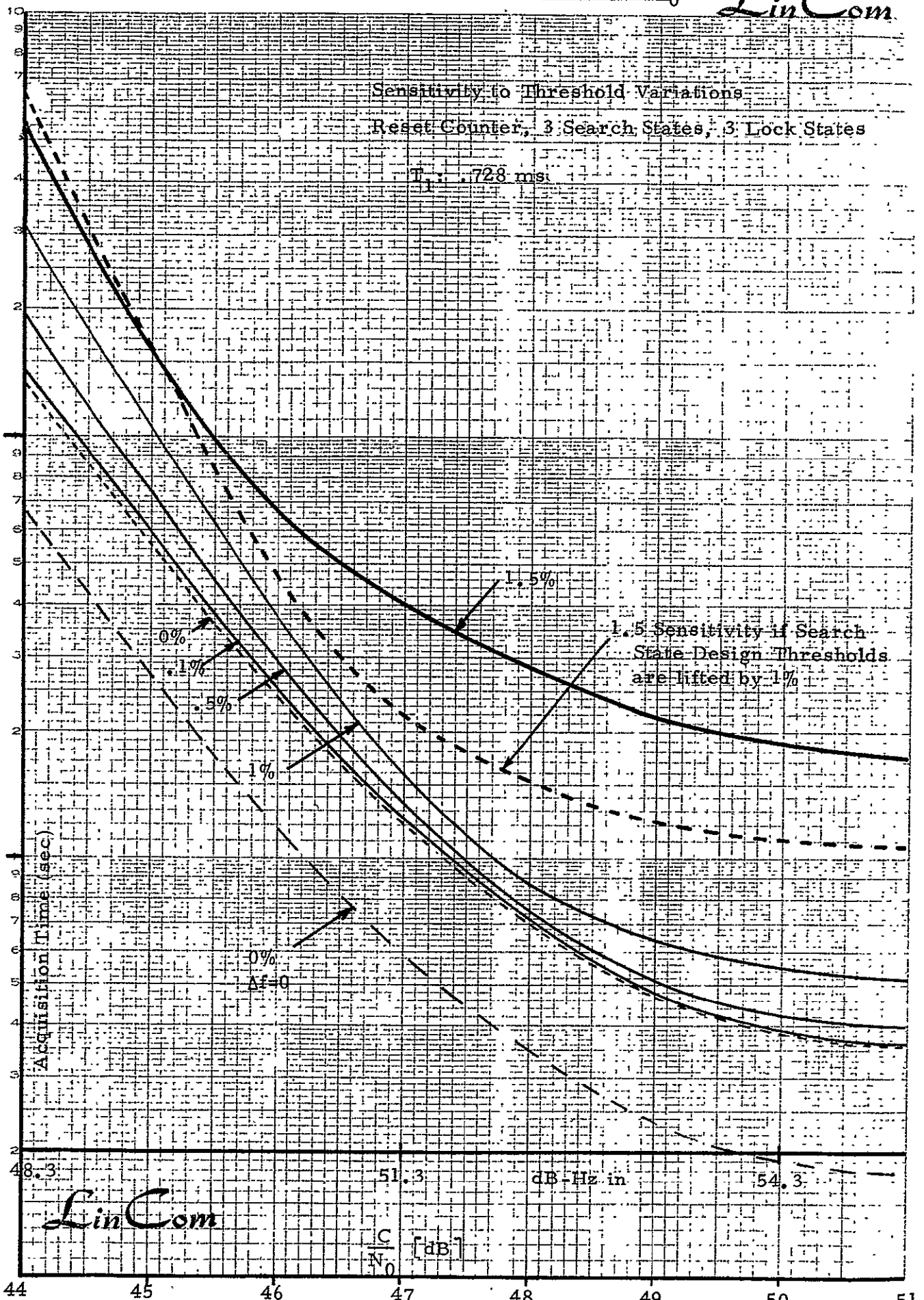
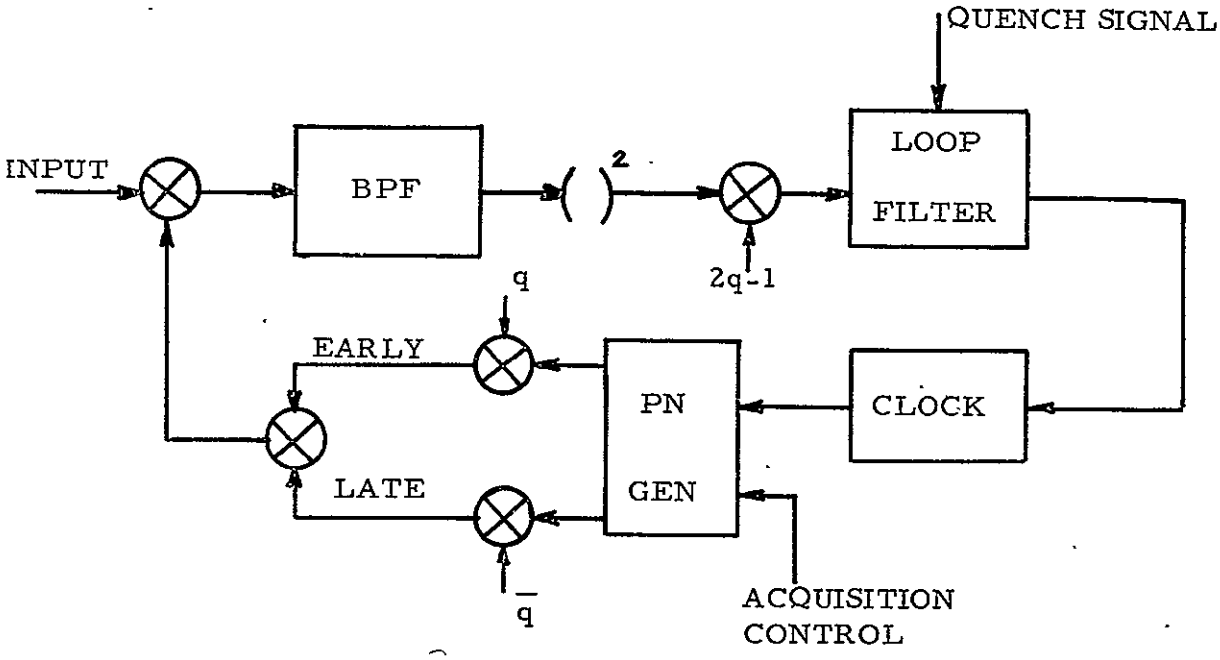
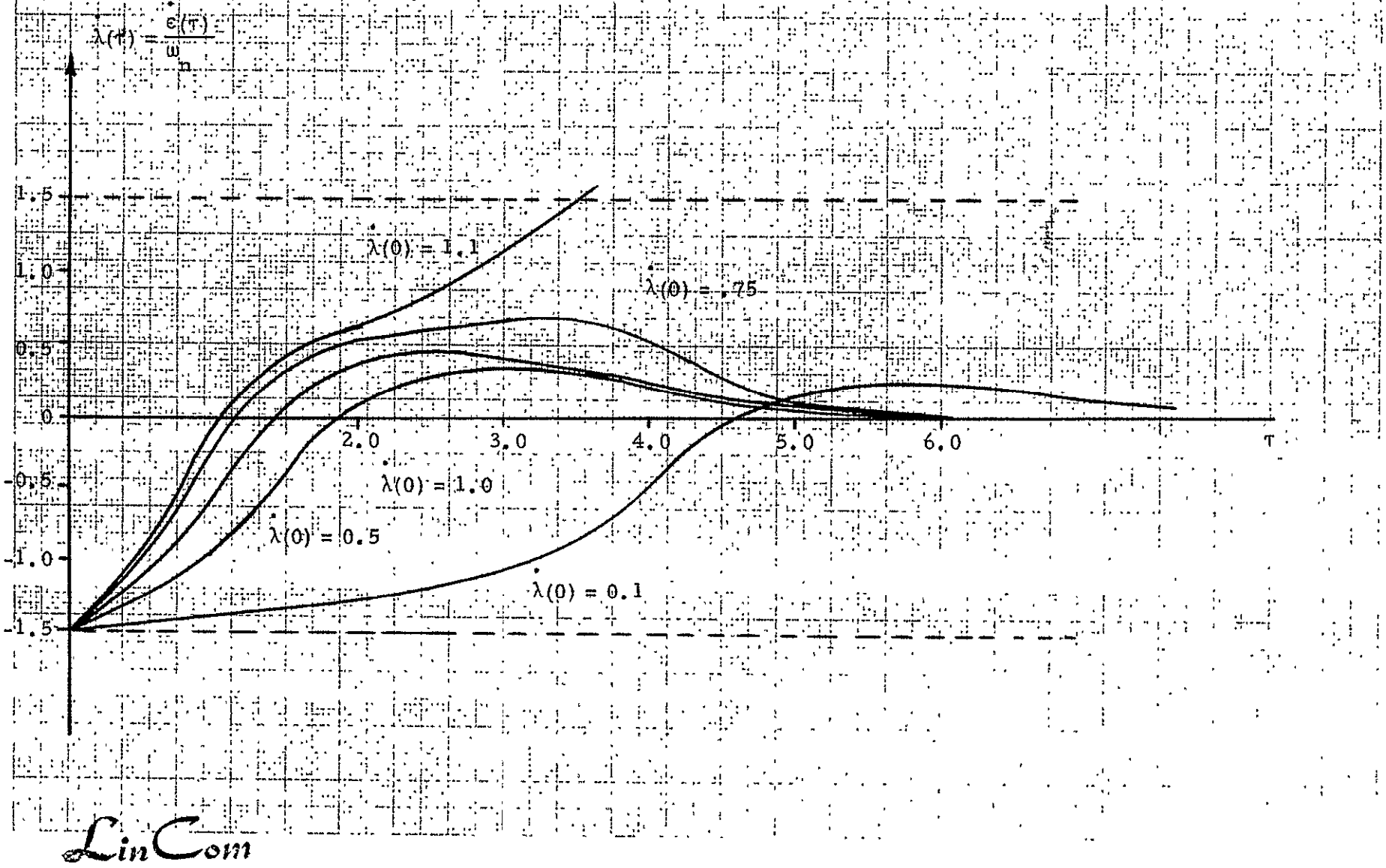


FIGURE 5.4-1. TIME-SHARED DELAY LOCKED LOOP.



- BPF - 4 POLE BUTTERWORTH
  BANDWIDTH = 550 KHz
- B_L - { 200 Hz @ 48.3 dB-Hz for Acquisition
  10 Hz @ 48.3 dB-Hz for Tracking
- EARLY-LATE INTERVAL IS ONE CHIP (One-Δ Loop)
- q(t) - RZ SQUARE WAVE @ 100 kHz/sec
- LOOP BANDWIDTH CONTROL IS STEPPED FROM ACQUISITION TO TRACKING

FIGURE 5.4-2. TRANSIENT RESPONSE OF ONE Δ TIME SHARED DLL LOOP ERROR.



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of 200 Hz represents an optimum compromise between loop jitter and its ability to acquire the 300 chips/sec of code doppler. Since the PNSS gives limiting performance due to noncoherent detection, the design point was chosen to be 3 dB lower than in the carrier recovery loop.

The normalized loop jitter σ/Δ versus C/N_0 is plotted in Fig. 5.4-3 for various loop bandwidths. From these curves acquisition and tracking loop bandwidths of 200 and 10 Hz have been selected. The performance of a one-delta time shared loop is given in Fig. 5.4-4 for these two bandwidths. In addition, for comparison purposes the performance of a 200 Hz enveloping correlating DLL is illustrated. Finally, Table 5.4-1 summarizes the acquisition and tracking mode jitter performance along with the acquisition time for two signal-to-noise conditions.

6.0 Effect of the RF/IF Filtering on the Correlation and Error Signals in the PNSS

The effectiveness of the frequency spreading will be limited by the frequency response of the end-to-end channel through which the wide-band signal must pass. The frequency response of the channel will be imperfect for several reasons. First of all, the TDRS will produce filtering and reprocessing of the signal. The RF and IF filters will also limit the bandwidth of the signal as their filter skirts must fall sufficiently fast to suppress out of band interference and meet the desired specification.

Figure 6-1 serves to model the problem under consideration. The PN signal is first filtered and then cross correlated with the local reference created in the receiver. The filtered cross-correlation function $R_{xy}(\tau)$ can be studied as a function of the RF filter characteristics; it is this function that is used to create the error signal for the τ-dither loop. As shown earlier, (Section 4.0) this function also degrades the carrier recovery loop, the data channel and the AGC. Computer programs were

FIGURE 5.4-3. τ-DITHER LOOP VS C/N_0.

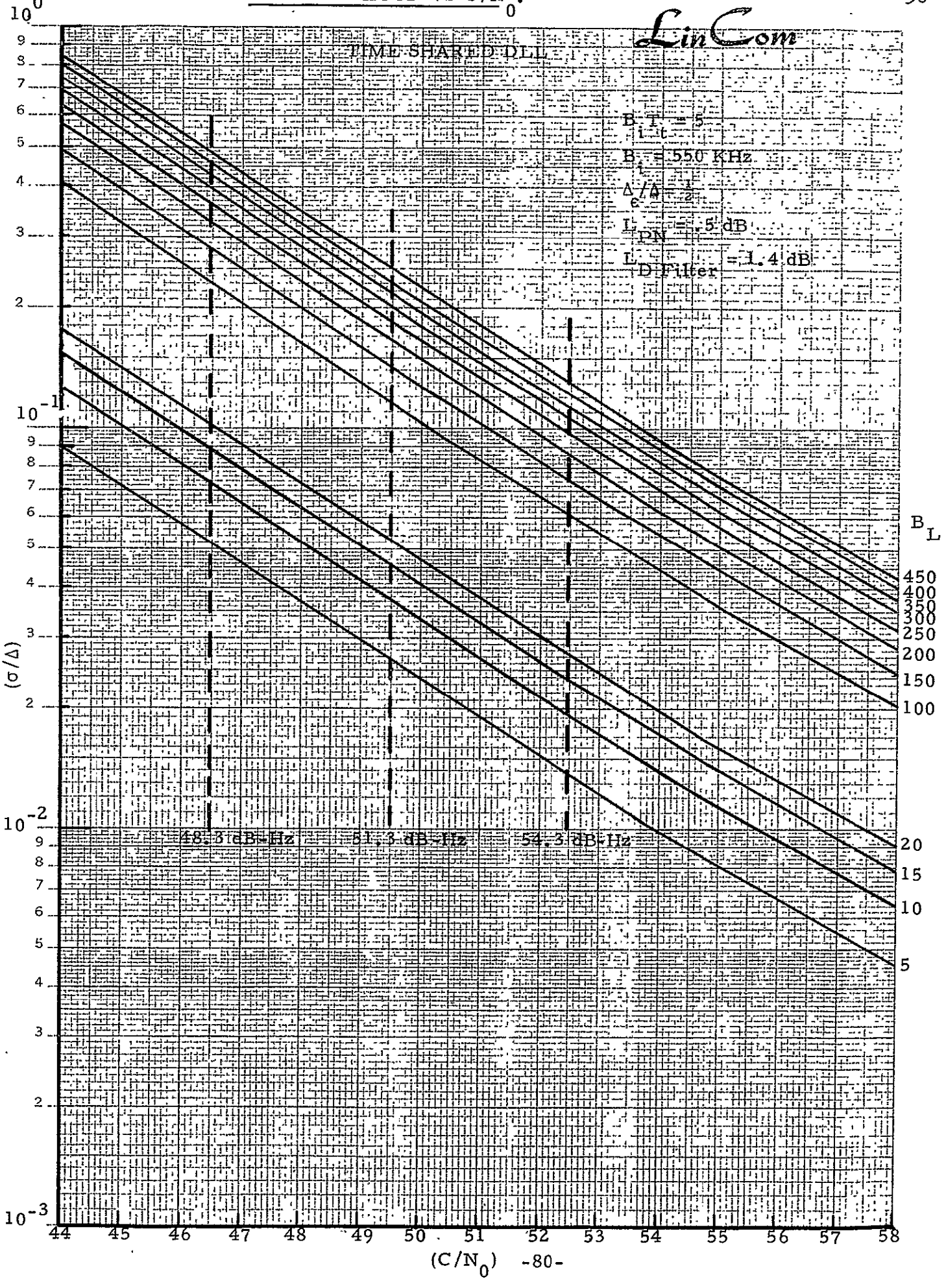

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FIGURE 5.4-4. τ-DITHER LOOP JITTER vs C/N_0.

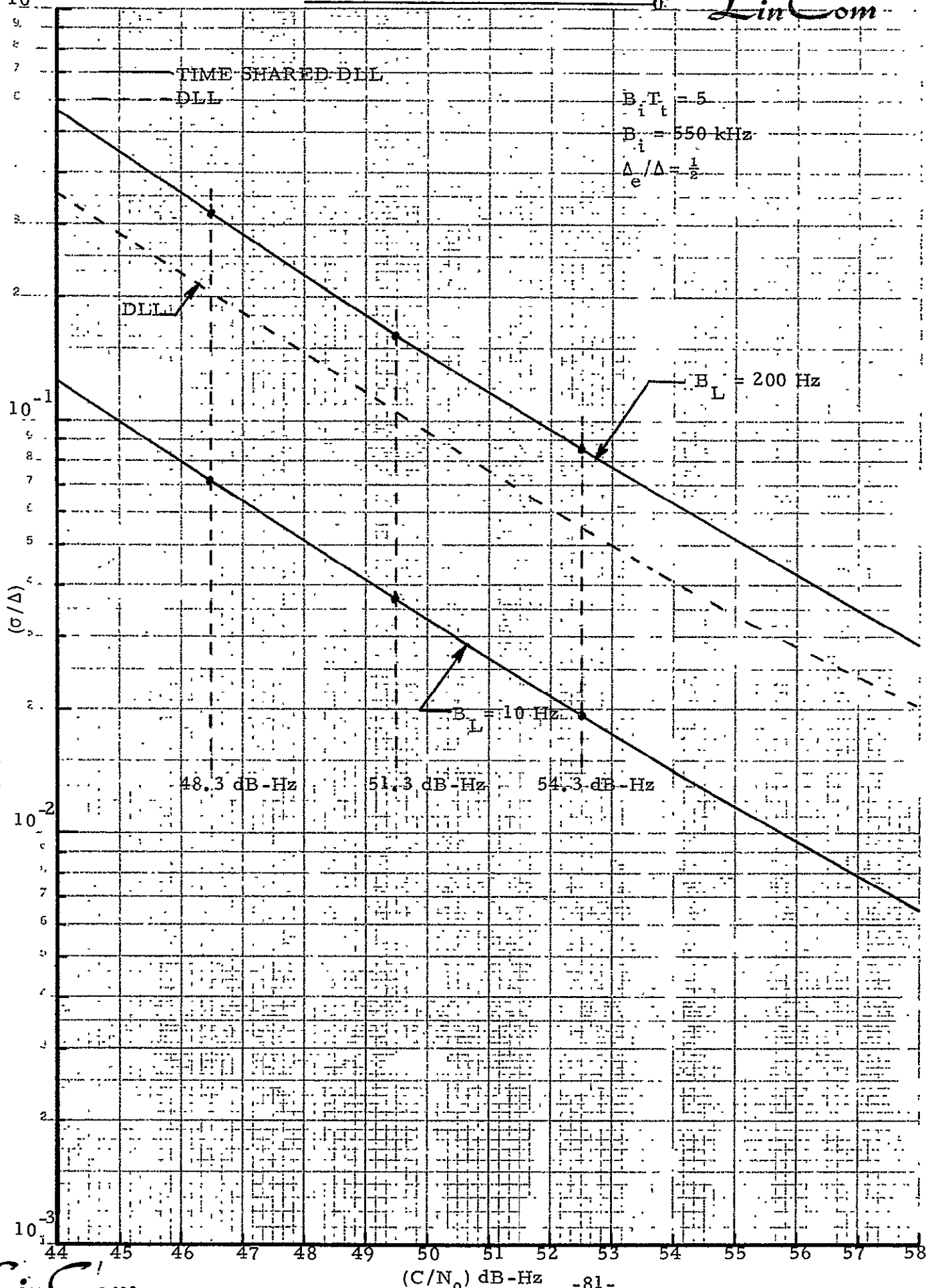


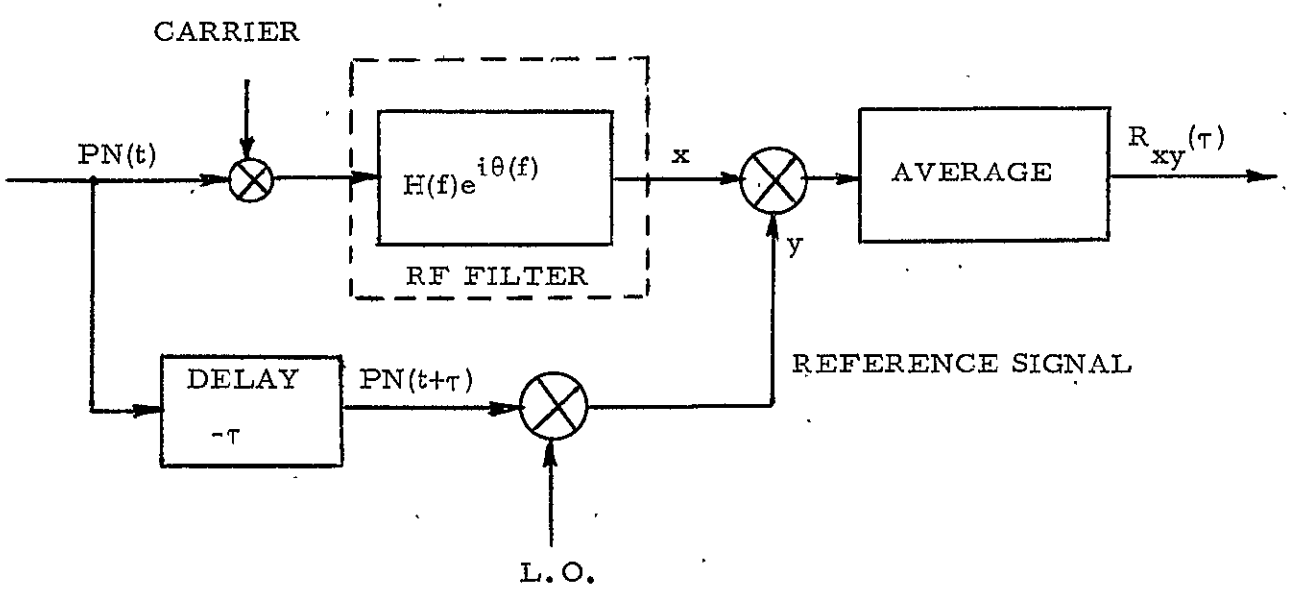
TABLE 5.4-1. TIME-SHARED DLL PERFORMANCE.

Mode	B_L-Hz	C/N_0, dB-Hz	Jitter-Chips	Peak Doppler (Chips)	Loop Pull in Time
Acq.	200	48.3	.33	.40 (.26)	15 msec
	335	51.3	.21	.30 (.22)	12 msec
Track	10	48.3	.07	NA	NA
	10	51.3	.045	NA	

DOPPLER = 300 Chips/Sec

LOSSES $\simeq$ .4 dB (RF FILTER) + 1.4 dB (CORRELATION FILTER) $\simeq$ 1.8 dB

FIGURE 6-1. RF FILTER CORRELATION EFFECTS IN DATA CHANNEL.



written so as to provide a means of evaluating the effects of the RF/IF filtering on the correlation error signals. Volume II provides information and plots of the correlation function $R_{xy}(\tau)$. Figure 6-2 serves to illustrate the effect of cubic phase distortion on the phase-detector characteristic of a delay-locked loop. There are four attributes caused by the filtering of PN chips. First there is a reduction in peak correlation or equivalently a reduction in the energy available for lockup of the time-shared delay-locked loop. Second, there is partial correlation outside the desired region, which, at high signal-to-noise ratios will degrade loop lock up, i.e., the Tchebycheff filter causes cross-overs of the zero axis in such a manner to give undesirable stable lock point. Fourth, the desired stable lock point has been shifted. This causes a delay which must be accounted for in the system used for ranging.

7.0 Transponder Parameter Summary

Receiver Front-End

Center Frequency	2.0 GHz
RF Filter; Selectable Butterworth or Tchebycheff	4 poles
RF Filter Bandwidth	22 MHz, 1 dB ripple factor
First LO Frequency	1.6 GHz
First IF Frequency	400 MHz
Second LO Frequency	320 MHz
Second IF	80 MHz
RF AGC Loop Filter	RC Single Pole
RF AGC Time Constant	20 msec
First IF Filter	Combined with RF Filter
Second IF Filter	2 Pole
Second IF Filter Bandwidth	864 kHz

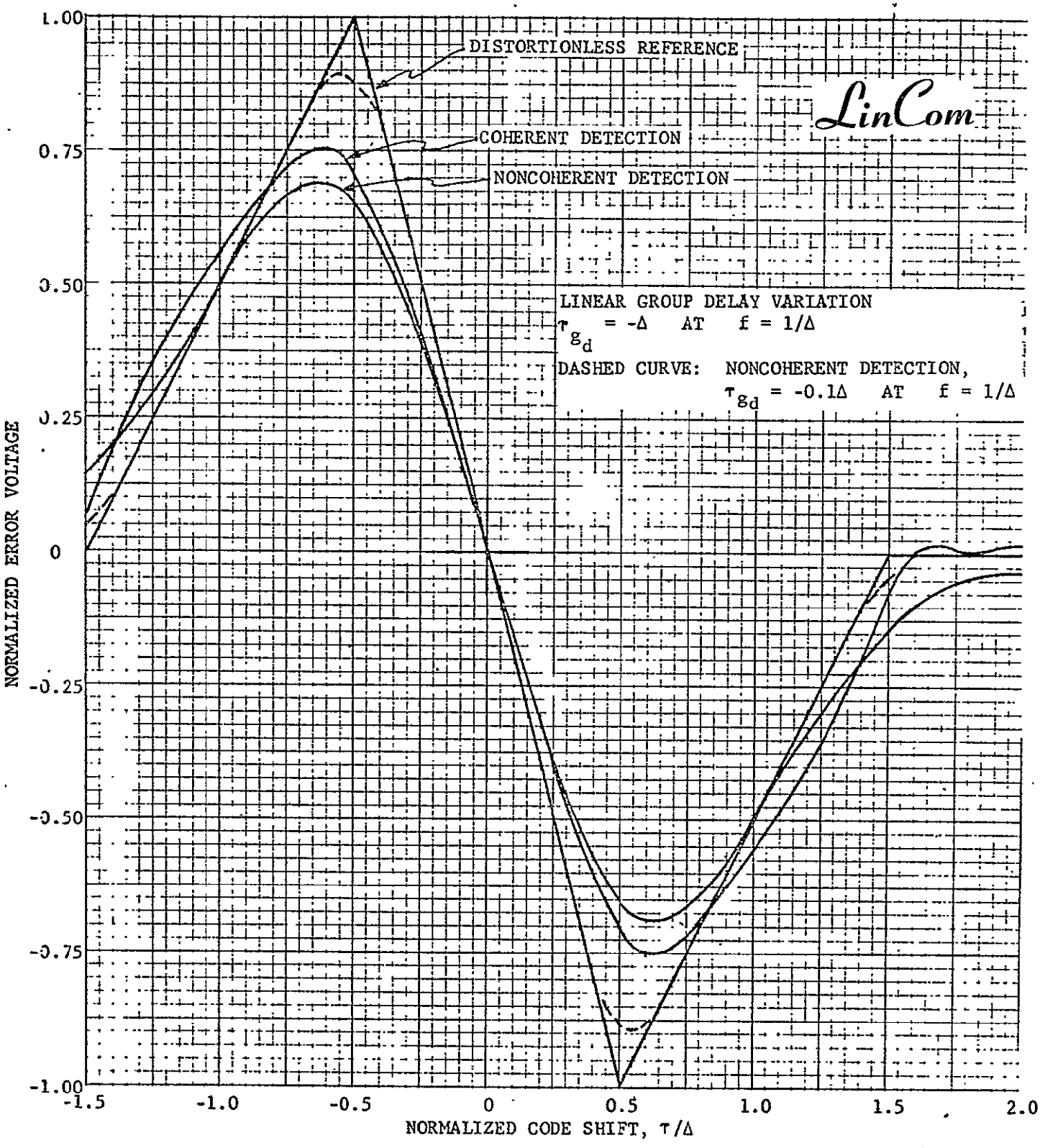


FIGURE 6-2. EFFECT OF CUBIC PHASE DISTORTION ON DLL PD CHARACTERISTIC.

Local PN Reference

Chip Rate (chips/sec)	11.232 MHz
Code Length	2047 Chips
Modulation	BPSK
RF Filter Correlation Loss	0.4 dB

PN Code Acquisition

Dwell Time	.91 msec
Search States	4
Lock States	20
PN Acquisition Time (48.3 dB-Hz)	100 sec
Code Doppler	±300 chips/sec
Code Doppler Rate	$\pm .4$ chip/sec^2
PN Loop Acquisition Bandwidth (48.3 dB-Hz)	200 Hz
Time Error (48.3 dB-Hz)	≤.33 chip
PN Post Correlation Filter Bandwidth	550 kHz

PN Code Tracking

PN Post-Correlation Bandwidth	550 kHz
Loop Bandwidth (48.3 dB-Hz)	12.5 Hz
Tracking Loop Jitter (48.3 dB-Hz)	0.1 chips
Dwell Time	3.64 msec

Costas Loop

Arm Filter Bandwidth	324 kHz
Acquisition Loop Bandwidth (51.3 dB-Hz)	500 kHz
Sweep Rate	40 kHz
Max Doppler	±55 kHz
Acquisition Time at 90% Probability (51.3 dB-Hz)	3 sec
Average Acquisition Time (51.3 dB-Hz)	1.8 sec
Standard Deviation Acquisition Time (51.3 dB-Hz)	1.3 sec

Lock Indicator

Integrate and Dump Time Acquisition	2 msec
I and D Time Tracking	8 msec

Costas Noncoherent AGC

Loop Filter	RC Single Pole
Time Constant	2.0 msec

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