Investigation of Television Transmission Using Adaptive Delta Modulation Principles

Final Report

April 15, 1975 – April 14, 1976

NASA Johnson Space Center

Houston, Texas 77058

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DEPARTMENT OF ELECTRICAL ENGINEERING

THE CITY COLLEGE OF
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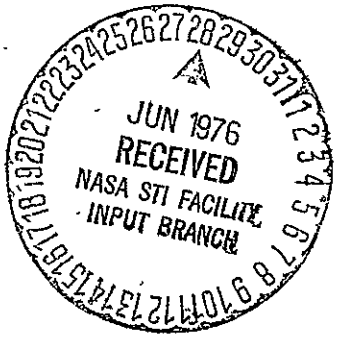

Abstract

This paper presents the results of a study on the use of the delta modulator as a digital encoder of television signals. The study began with the computer simulation of different delta modulators in order to find a satisfactory delta modulator. After finding a suitable delta modulator algorithm via computer simulation, we analyzed the results, and then implemented it in hardware to study its ability to encode real time motion pictures from an NTSC format television camera.

We then investigated the effects of channel errors on the delta modulated video signal and tested several error correction algorithms via computer simulation. A very high speed delta modulator was built (out of ECL logic), incorporating the most promising of the correction schemes, so that it could be tested on real time motion pictures.

The final area of investigation concerned itself with finding delta modulators which could achieve significant bandwidth reduction without regard to complexity or speed. The first such scheme to be investigated was a real time "frame to frame" encoding scheme which required the assembly of fourteen, 131,000 bit long shift registers as well as a high speed delta modulator. The other schemes involved the computer simulation of two dimensional delta modulator algorithms.

Introduction

Developments that have taken place over the past ten years clearly show a trend toward digital processing of communication signals. Already voice signals and computer data are being processed digitally in many systems, but digitization of television signals has achieved only limited acceptance. There are two reasons for the lack of applications for the digital transmission of television signals. First, a cheap, high speed, binary, digital encoder that can accommodate the large bandwidths required for television signals is not available, and secondly, those systems that are relatively cheap, such as DPCM and PCM increase the already large bandwidth of television signals by a factor of between three and eight. A binary, digital encoding technique which may overcome some of these difficulties is the delta modulator.

This paper presents the results of a study on the use of the delta modulator as a digital encoder of television signals. The study began with the computer simulation of different delta modulators in order to find a satisfactory delta modulator. A satisfactory delta modulator was one that could operate at the very high sampling rates required for real time processing of television signals, and could also provide a bit rate reduction over PCM digital encoding techniques. After finding a suitable delta modulator algorithm via computer simulation, we analyzed the results, and then implemented it in hardware to study its ability to encode real time motion pictures from an NTSC format television camera.

We then investigated the effects of channel errors on the delta modulated video signal and tested several error correction algorithms via computer simulation. A very high speed delta modulator was built (out of ECL logic), incorporating the most promising of the correction schemes, so that it could be tested on real time motion pictures.

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encoding scheme which required the assembly of fourteen, 131, 000 bit long shift registers as well as a high speed delta modulator. The other schemes involved the computer simulation of two dimensional delta modulator algorithms.

The Delta Modulator

The delta modulator chosen to encode the pictures in this paper is shown in Fig 1. The equations describing the operations of the delta modulator are given below:

$$E_k = \text{Sgn}\,(S_k - X_k) \tag{1}$$

$$X_{k+1} = X_k + Y_{k+1} \tag{2}$$

$$Y_{k+1} = \begin{cases} |Y_k|\,(\alpha E_k + \beta E_{k-1}) & ;\ 2Y_{min} \le |Y_k| \le Y_{max} \\ 2Y_{min}\,E_k & ;\ |Y_k| < 2Y_{min} \\ Y_{max} & ;\ |Y_k| > Y_{max} \end{cases} \tag{3}$$

$E_k \equiv$ Output of the encoder

$S_k \equiv$ Input to the encoder

$Y_k \equiv$ The encoder's estimate of the input signal at the k^{th} instant of time; also, the decoder's output at the k^{th} instant of time

$Y_k \equiv$ The step size of the delta modulator

Y_{min}, $Y_{max} \equiv$ Constants that determine the minimum and maximum allowable value for Y_k

α, $\beta \equiv$ Other constants

There are other delta modulator algorithms besides the one described by Eq 1, 2 and 3. In general the differences lie in Eq 3, the way the step size is formed. In some delta modulators $|\ Y_k\ |$ is a constant. In others it increases or decreases linearly. In our delta modulator the step size, Y_k, changes exponentially. It has been experimentally determined that an exponentially changing step size type of delta modulator is more appropriate then the other types of delta modulators at encoding a signal with large step type changes in amplitude as found in video signals.

In order to test our delta modulator on video signals from actual pictures, and to find good values for α, β, Y_{min} and Y_{max} (see Eq 3) we set up a computer processor for pictures as shown in Fig 2. With the experimental aparatus of Fig 2 we were able to program the PDP 8 computer to simulate a delta modulator. By varying the values of α, β, Y_{min} and Y_{max} in the computer program, and then comparing the resulting pictures, we obtained values for α, β, Y_{min} and Y_{max} which would produce satisfactory pictures.

In choosing the best set of values for α, β we also considered the effects of different sets of values on a real time hardware implementation of the delta modulator. Since very high sampling rates would be required for the real time processing of video signals, we restricted our choice of values of α and β to those values that would minimize the time required to perform the multiplications of $|\ Y_k\ |$ by α and β. From the computer simulations we found that $\alpha = 1$ and $\beta = .5$ produce about the best pictures. Since these values are also powers of 2 the multiplication by 1 and .5 are wired shift operations and require no hardware to implement nor any time to perform. Clearly, $\alpha = 1$ and $\beta = .5$ was an ideal choice for α and β and thus these values were used in all our delta modulators.

To determine the effects of Y_{min} and Y_{max} on a delta modulated encoded picture we examined the response of the delta modulator to a step like input. We chose a step like input because the edges of objects in pictures produce step like changes in the video signal. From Fig 3 we see that at first the delta modulator's output does not rise as fast as the input signal. This effect gives rise to a type of degradation

called slope overload noise. After the delta modulator catches up with the input signal it may overshoot the input, and then after a period of time known as the settling time, the delta modulator settles down to a repetitive four bit pattern that bounces around the input signal. This last effect is a type of degradation often called granular noise. The amplitude of the granular noise determines the minimum voltage change of the input signal that can be resolved by the delta modulator. Note also that when the step size, Y_k, increases, it increases by a factor of 1.5 until Y_{max} is reached. When the step size decreases, it decreases by a factor of .5 until Y_{min} is reached. This, of course, follows from Eq 3 and $\alpha = 1$, $\beta = .5$.

Table 1 sumarizes the relationship between slope overload noise, granular noise, overshoot, settling time and increasing or decreasing the value of Y_{min} and Y_{max}. From table 1 it is clear that a tradeoff exists between slope overload noise and granular noise when choosing a value for Y_{min}. For Y_{max} the tradeoff is between slope overload noise against settling time and overshoot amplitude. From our computer simulations on real pictures we found that a value for Y_{min} equal to 1/64 the peak to peak video input signal produced the best pictures. This result is not surprising since this value of Y_{min} will allow the delta modulator to resolve 64 gray levels and it is well known that at least 64 gray levels are required to produce satisfactory pictures. It was also found that the quality of our pictures was not very sensitive to the value of Y_{max}. It was observed that the value of Y_k rarely grew larger than 1/4 the peak to peak input signal and that large overshoots and ringing usually produced out of band frequency components that were eliminated by low pass filtering. After considering all factors we chose a value of 1/4 the peak to peak input signal for Y_{max}.

In conclusion we found that the delta modulator worked best with $\alpha = 1$, $\beta = .5$, $Y_{min} = 1/64$ p- p input signal and $Y_{max} = 1/4$ p - p input signal. These values were used in all subsequent delta modulators.

	Slope Overload Noise	Granular Noise	Settling Time	Overshoot Amplitude
Increasing Y_{min}	Decreases	Increases	No Change	No Change
Decreasing Y_{min}	Increases	Decreases	No Change	No Change
Increasing Y_{max}	Decreases	No Change	Increases	Increases
Decreasing Y_{max}	Increases	No Change	Decreases	Decreases

Table I

PCM vs. Delta Modulated Pictures

In Fig 4 a comparison can be made between delta modulated pictures and 64 quantization level PCM encoded pictures. The pictures were taken using the experimental setup shown in Fig 2. Note that at high bit rates (682 bits/line) both PCM and delta modulation produce satisfactory pictures. At low bit rates (410 bit per line) edge business can be seen in the delta modulated pictures and a loss of resolution can be seen in the PCM encoded pictures. The edge business shows up as a wiggliness along the right edge of my face, and the loss of resolution in the PCM encoded pictures is apparent by the loss of the stripes on my shirt. A subjective evaluation of Fig 3 leads us to the conclusion that at high bit rates PCM encoding is desirable and at low bit rates delta modulation preserves more detail in the picture then PCM.

The degrading of PCM encoded pictures at low bit rates by a loss of resolution is completely explained by the Nyquist sampling theorem; however, the degrading of delta modulated pictures at low bit rates by edge business requires further explanation. The solid line in Fig 5 shows the response of the delta modulator to step input S_k. The dotted line shows the response of the same delta modulator to the same step input but the delta modulator had different initial conditions at the start of the step. In the first case the slope overload is large and in the second case it is small. In a picture this would have the effect of delaying an edge sometimes, but not at other times. The resulting effect would be to cause all sharp edges at right angles to the direction of scan to wiggle. This effect we call edge business.

A High Speed Real Time Delta Modulator

From the computer simulations we were able to find a satisfactory delta modulator and investigate its behavior when encoding a single frame of a still picture. In order to investigate the behavior of the delta modulator on motion pictures it became necessary to build a high speed delta modulator which could encode pictures from an NTSC standard TV camera in real time.

The block diagram for the high speed video delta modulator is shown in Fig 6. The two flip-flops on the top of the diagram store E_k and E_{k-1}. The upper adder/substractor, register, multiplexor and "OR" gate implement Eq 3. The lower adder/substractor and register carry out Eq 2, and the D/A converter and comparator implement Eq 1.

The complete circuit schematic for the high speed delta modulator is shown in Fig 7, and in Fig25 (top left picture) the component side of the circuit board is shown. The delta modulator contains 16 Schotky TLL integrated circuits, two high speed D/A converters, and a high speed comparator.

When constructing a very high speed digital and analog system such as shown in Fig 7 it is necessary to adhere to certain construction practices or else "switching gliches", ringing, and oscillations may degrade the performance of the system. Some of the construction practices we used are listed below:

1) Bread board the unit on a double sided copper clad board. Use the lower copper side as a ground plane along which all wires are run. The upper copper side may be used as a power buss.
2) Put bypass capacitors between the power buss and the ground plane. It may be necessary to put bypass capacitors at every IC.
3) Isolate the analog portion of the system (D/A converter and comparator) from the switching noise of the digital section by providing separate bypass capacitors for all analog devices' power input pins.
4) High speed comparators love to oscillate as they pass thru their linear region of operation. To prevent this, keep the input and output wires short, far apart, and if possible shielded.

5) Keep all wires as short as possible to prevent stray inductance and capacitance from causing ringing on the logic signals which might cause retriggering of the logic gates.

The high speed delta modulator was tested using the experimental setup shown in Fig 8. The setup funtioned in the following manner: A scene from a slide was converted to a video signal by the TV camera. The video signal was band limited by an adjustable cutoff low pass filter whose output provided the input to the delta modulator. The delta modulator was then clocked at its maximum rate of 10 MHz. The output of the delta modulator feeds another adjustable low pass filter whose cutoff is set to the same frequency as the previous filter. The processed picture is then displayed on a monitor and photographed. Sync for the camera and monitor is supplied by a separate sync generator. A switch is also provided so that a quick comparison can be made between the delta modulated encoded video signal and the unencoded video signal.

The output from the delta modulator used in Fig 8 was the test output marked on the diagrams of Fig 6 and 7. This output, in the absence of channel errors is the same as the output of the delta modulator receiver shown in Fig 1. This property made it unnecessary to build a receiver in order to test the delta modulator's ability to encode a video signal in the absence of channel errors.

The pictures in Fig 9 are representative of the quality of the pictures that we obtained from the test setup of Fig 8. The pictures on the left half of the page have been delta modulated while those on the right are the originals. The fact that the pictures on the right appear to be blurred is not due to bad photography, but is a consequence of low pass filtering the video signal. The bandwidth of the pictures, as determined by the settings on the filters of Fig 8, are given as follows: upper row, 2 MHz; middle row, 1.5 MHz; and lower row 1 MHz.

Since the pictures in Fig 9 have frozen a single frame from the 30 frames per second TV camera and monitor, some effects of real time processing are not shown in the "frozen scenes" of Fig 9. I will therefore try to describe these

effects. In Fig 9, upper left hand corner, edge business can can clearly be seen on the edges of vertical objects. The edge businesss appears as a slight horizontal displacement of each scanning line about the edge. Because some lines appear to be displaced more than others, straight vertical edges become wiggled as shown in Fig 7a. Now, imagine that sucessive frames of the same scene are flashed at the eye and each frame has its own wiggle pattern, as is the case with the real time processor, then the eye will see the edges flutter in time. This fluttering appears as a shimmering on the edges of objects. Although the shimmering is noticable it does not seem to cause a lose of resolution in the pictures and it is no more annoying then the edge business seen in Fig 7.

Just as the effect of viewing successive frames of a still picture cannot be seen in Fig 9, nor can the effect of the TV camera viewing a changing scene be determined from Fig 9. To determine the effect of the delta modulator on the video signal from a moving scene, we removed the slide projector from Fig 8 and aimed the camera at a room full of people at a party. The delta modulator showed no new kind of degradation for the moving scene. In fact, moving objects suffered slightly less edge business then still objects because the eye does not see moving objects very clearly.

If we assume that the pictures on the right in Fig 9 were encoded using 64 level PCM (sampling at the Nyquist rate) then we can calculate and compare the bit rate, and the number of bits per pixel for the pictures on the right with those on the left of Fig 9 from the following equations

$$\frac{\text{Bits}}{\text{Pixel}} = \frac{(\text{Sampling Rate})\ (\text{Bits Per Sample})}{2 \times \text{Picture Bandwidth}} \qquad \text{(Eq 4)}$$

$$\text{Bit Rate} = (\text{Sampling Rate})\ (\text{Bits Per Sample}) \qquad \text{(Eq 5)}$$

This yields:

Table II

Picture	Delta Modulator		PCM	
	bit rate	bits per pixel	bit rate	bits per pixel
TOP	10 MHz	2.5	24 MHz	6
MIDDLE	10 MHz	3.3	18 MHz	6
BOTTOM	10 MHz	5.0	12 MHz	6

From the values in Table II, the pictures in Fig 9, as well as motion picture observations, we have concluded that our real time delta modulator can compress the bit rate over PCM by a factor of between 2 to 3 without any loss of detail. Although no loss of detail is observed it is clear that the pictures in the left column are degraded over those in the right column of Fig 9. The degradation is most severe for the top row where the bit rate compression is 2.5 and almost unnoticable in the bottom row where the bit rate compression is 1.2.

The Effects of Channel Errors on the Delta Modulated Signals

When transmitting signals over real channels it is necessary to consider the effects of channel errors. The next section of this report explains the effects of channel errors on the delta modulated video signal and explores several error correction algorithms.

The response of the delta modulator decoder to a step input at the encoder in the presence of a single channel error is shown in Fig 10. The solid lines represent the output signal, X_k, of the decoder in the absence of channel errors, while the dashed lines represent the output signal of the decoder in the presence of a single channel error.

Channel errors have two effects on the delta modulator. The first and most obvious effect that can be seen in Fig 10 is that channel errors always cause a permanent, and usually large DC shift in the received signal. Less obvious is the fact that a single channel error may cause an increase, decrease or have no effect at all on the step size of the delta modulator decoder, and less obvious still, is the fact that step size errors, when they occur, become self correcting within a few samples. Because step size errors last for only a few samples, and delta modulators typically sample at several times the nyquist rate of the input signal, the disturbance caused by step size errors is usually one to two pixels long and can bearly be perceived in the picture.

We have both quantitative results and experimental evidence to support the statements made in the preceeding paragraph. The quantitative results were arrived at through the following process. Observe from Fig 10 and Eqs 1, 2 and 3 that the step size, Y_k, will decrease while the delta modulator is tracking a constant DC level. If the constant signal level persists long enough the delta modulator reaches the minimum step size, Y_{min}, whether or not a channel error has occured. When the delta modulator reaches the minimum step-size, the step size error has corrected itself, since both the corrupted signal and the ideal error free signal would have the same step size namely Y_{min}, the minimum step size.

The number of transmitted bits, N, that will reach the receiver after the occurrence of a channel error, but before the step size corrects itself, has an upper bound for the delta modulator tracking a constant DC level, This upper bound can be shown to be

$$.75\ N/2 = Y_{min}/Y_{k+1}$$

or

$$N = \frac{2 \ln Y_{min}/Y_{k+1}}{\ln .75} \tag{6}$$

where N ≡ the number of transmitted bits until step size correction occurs

Y_{k+1} ≡ the step size one sample time after the occurrence of the error

Y_{min} ≡ the minimum allowable value for Y_k.

For the pictures in this paper the worst case parameters for Eq 6 are $Y_{min} \equiv 1$ and $Y_{k+1} = 16$ which yield a worst case N = 19. If the delta modulator samples at six times the nyquest rate of the video signal then the step size error should last for less that 3 pixels if the conditions imposed in deriving Eq 4 hold for a real picture.

The series of pictures in Fig 11 were taken to confirm the results of Eq 6, i.e., step size errors quickly correct themselves, and to confirm that channel errors cause a large permanent shift in the DC level of the output of the delta modulator. Figure 11a shows the original picture without any errors. In Fig 11b channel errors were introduced at a rate of one error for every 2,500 transmitted bits. From Fig 11b we see that each channel error caused a shift in the level of the decoders output signal. This shift, seen as a streak, lasts until the end of the scanning line where the effect of the error is ended by resetting all the registers in the encoder and decoder to a fixed predetermined value. In Fig 11c we have displayed the absolute value of the step size without any channel errors and in Fig 11d we introduced channel errors. Figure 11e is the difference between Fig 11c and Fig 11d.

The uniform gray background in Fig 11e represents zero difference between Fig 11c and Fig 11d or equivently, no step size error. The white and black dots are the regions where the difference between Fig 11c and Fig 11d was not zero or equivently, where a step size error exists. Figure 11e confirms the fact that step size errors become self correcting after a few samples. The conclusions that we have drawn from our studies of the effects of channel errors on delta modulated video signals is that channel errors have a significent effect only on the DC level of the estimate, X_k, of the delta modulator decoder and that error correcting schemes need only correct for errors in the decoder's estimate, X_k.

Error Correcting Algorithms

The preceeding analysis has revealed that channel errors effect delta modulated encoded video signals by changing the DC level of the decoded signal. In the rest of this paper we will describe three techniques to minimize this effect.

Direct Approach

It is possible to correct the DC level of the decoders estimate by periodically sending the transmitters current estimate, X_k, to the receiver. The effect of this correction technique, (shown in Fig 12) is to shorten the length of the error streaks. The more often the transmitters estimate is sent to the receiver the shorter the streaks become. Unfortunately the more often we send the transmitters estimate, the more we must increase the transmission rate to accommodate this extra information.

The equation that relates the several parameters that determine the increase in transmission rate is given by Eq 7.

$$f_s' = f\left(1 + \frac{cb}{s}\right) \qquad (7)$$

where

f_s' ≡ The bit rate with correction

f ≡ The bit rate without correction

c ≡ The number of times X_k is sent to the receiver per frame

b ≡ The number of bits in each X_k sent to the receiver

s ≡ The total number of E_k's transmitted per frame

From Eq 7 it is apparent that "c" and "b" should be as small as possible. "c" is lower bounded by the desired degree of correction required in the picture since the length of the remaining error steaks in the received picture are inversely proportional to c, and b is lower bounded by the accuracy of the correction.

To understand the effect of "b" on the correction algorithm refer to Fig 13. Figure 13 shows how the correction algorithm is implimented. First the "b" most significent bits of the transmitters estimate are sent to the receiver via a PCM format. Upon receiving the PCM word the receiver sets the "b" most significent bits in its estimate equal to the transmitters estimate. Then both the transmitter and receiver set their b +.1 most significent bit to 1 and all less significent bits to zero. The total effect is to make the transmitter's and receiver's estimate equal, and to introduce an inaccuracy in the estimates equal to 2^{-b-1} percent.

The effect of the inaccuracy in the estimates introduced by the correction algorithm is shown in Fig 14. Note that the effect is transient and is completely undetectable for b = 4. The value b = 4 was used in the pictures of Fig 12.

Leaky Integrator

The effects of channel errors on delta modulated encoded pictures can be minimized by introducing leaky integrators in the feed back loop of the encoder and in the decoder. Leaky integration is achieved by introducing the factor L, ($L \leq 1$), into Eq 2 as shown in Eq 8.

$$X_{K=1} = LX_K + Y_{K+1} \tag{8}$$

If a channel error causes the estimate, X_K, to become shifted by an amount "e" at time "k", then at time K + N Eq 8 will become

$$X_{K+N} = L^N X_K + \sum_{i=1}^{N} L^{N-i} Y_{K+i} + L^N e \tag{9}$$

From Eq 9 we see that the error "e" will leak away by the factor L, and after N samples the amplitude of the error will be $L^N e$. Clearly, the smaller the value of L the sooner the error will disappear. The smallest value of L that may be used without degrading a picture with 64 quantization levels ranging from -32 to +31 is L = .967.

Figure 15 shows the effect of using a leaky integrator with L = .967 on delta modulated encoded pictures that were transmitted over a noisy channel. From Fig 15 we see that the inclusion of leaky integration in our delta modulator will substantially reduce the effects of channel errors on the received pictures.

Line to Line Correlation

In this section we will explain a technique, shown in Fig 16, which locates error streaks in pictures and which then eliminates the streaks by readjusting the DC level of the streak to its proper value.

To detect an error streak in a picture a comparison is made between the DC level of the portion of a scan line under test and the corresponding portion of the scan line above and below the line under test. If the DC level of the portion of the line under test differs from both the line above and below by more than a certain "threshold" then an error has been detected. When an error is detected the DC level of the portion of the line under test is replaced by the average DC value of the corresponding portion of the line above and below. The part of the picture referred to as "the portion under test" is formed from "N" consective samples on a scanning line.

There are two parameters in the above algorithm that must be adjusted, "N" and the "threshold", to eliminate the error streaks. In Fig 17 we can see the effects of "N" and the "threshold" on both the error streaks and the quality of the picture. Small values of "N" and low thresholds eliminate the error streaks but they tend to degrade the picture by eliminating thin objects such as the bottom of my glasses as shown in Fig 17e. Large values of "N" and high thresholds leave some error streaks undetected and parts of others uncorrected but they do not degrade the picture. It is our opinion that Fig 17c represents the best compromise between the degree of error correction necessary and the amount of degradation that can be tolerated in the picture.

High Speed Delta Modulator With Error Correction

It was necessary to implement one of the error correction schemes on a real time delta modulator to enable us to see the effects of the 30 frame/sec real time frame rate on the visibility of channel errors after error correction.

The leaky integrator method of error correction was chosen for our delta modulator. The following four reasons are given for our decision to use the leaky integrator error correction technique.

1) The leaky integrator did not increase the signal bandwidth.
2) The leaky integrator did not degrade the picture as line to line interpolation could.
3) The leaky integrator was the simplest to implement at high speeds.
4) The leaky integrator corrected channel errors in the computer simulations as well as the other two methods tested.

The circuit schematic for the delta modulator is shown in Fig 18. The delta modulator is built out of MECL 10,000 series logic and will operate at a 15 MHz clock rate. Figure 18 shows only the delta modulator transmitter; however, the receiver is just the feedback loop of the transmitter as is shown in Fig 1. From Eq 8, shown again below, it is clear that the leaky integrator correction scheme is implemented by multiplying the leak factor L by X_K.

$$X_{K+1} = L X_K + Y_{K+1} \tag{10}$$

If the leak factor is chosen such that it can be written in the form below with n an integer

$$L = 1 - 2^{-n} \tag{11}$$

then we have

$$X_{K+1} = X_K - 2^{-n} X_K + Y_{K+1} \tag{12}$$

and the multiplication by L becomes a substraction of X_K by X_K shifted n places to the right. The circuit schematic of Fig 18 is drawn for n = 6; however, we also plan to test the delta modulator with n = 5. From the computer simulations we already know that n = 5 or 6 will give the best results.

A problem arises in the implementation of the leaky integrator multiplication algorithm because X_K is a 6 bit wide binary number and the multiplication algorithm yields a number for L X_K equal to 6 + n bits wide. Rather than save all 6 + n bits and significantly increase the amount of hardware in the delta modulator we truncated L X_K at 8 bits wide. This truncation results in the inability of errors to completely leak away. The error will leak until the difference between the estimate in the transmitter and receiver is 1/4 the peak to peak signal for n = 6 and 1/8 the peak to peak signal for n = 5.

To prevent the residual error that does not leak away from being propagated indefinately, circuitry is included in Fig 18 to reset the delta modulator's estimate and step size registers, in both the transmitter and receiver to a zero value at the end of every scan line. The end of the scan line is detected from the composite video signal by setting a comparator to flip on the negative sync pulse. The resetting of the estimate and step size registers occurs on the first positive bit (e_k) generated by the transmitter after the sync pulse is detected. This guarantees that the transmitter and receiver reset their registers at the same time which is necessary to prevent the resetting algorithm from introducing its own errors.

Figure 19 shows the test setup used to test the delta modulator. Note that channel errors are introduced between the transmitter and receiver. Note also that the sync signals are generated internally by the TV camera and reach the monitor via the composite video signal.

[The delta modulator in Fig 18 is currently being built. We expect to have some results by September 1976.]

High Speed Frame to Frame Delta Modulation

From the previous work presented in this report it is apparent that the key to producing high quality picture, at low bit rates, with delta modulation, lies in reducing edge business. In this section of the report we explain a frame to frame encoding technique employing a delta modulator which will reduce edge business in real time motion pictures.

Successive frames of a motion picture contain redundant information. The amount of redundancy depends upon the degree of change in the scene from frame to frame. It has been found that for picturephone application on the average, only 9 percent of the picture changes from frame to frame For broadcast television service about 10% of the picture changes from frame to frame . It is also known from the psychophysics of vision that the more rapid the motion from frame to frame of the image, the more difficult is the resolving of image detail for the observer. It is possible to design a delta modulator which will produce good pictures at low bit rates by taking advantage of the interframe redundancy of pictures and the psychophysical property of vision mentioned above.

Figure 20 shows the encoding scheme that the frame to frame delta modulator will use. Each large square represents a successive frame of a motion picture. Each dot on a frame represents a pel (picture element). Note that each pel has associated with it a delta modulator (ΔMOD) that follows the same pel through successive frames. Thus the ΔMOD in the upper most left hand corner always encodes the pel in the upper most left hand corner for every frame.

The encoding of high quality pictures at a low bit rate is achieved in the following manner. From previous studies of delta modulators it has been observed that high sampling rates are required for a delta modulator to accurately encode rapidly changing signals and low sampling rates may be used on slowly varying signals. The usual method of encoding a picture by sampling successive pels within the same frame results in rapidly changing signals which require a high delta modulator bit rate. With the frame to frame encoding technique of Fig 20 each delta modulator is associated with its own pel. On the average, 90%

of the pels will not change value from frame to frame, allowing the delta modulator to accurately encode the value of the pel at a low bit rate. Of course, those pels that do change value will not be encoded accurately, but the eye will not see the inaccuracy if the pel was associated with rapid motion. Using this scheme motion pictures will be encoded at 1 bit per pel.

At first thought, hardware implementation of Fig 20 may seem impossible since, at one delta modulator per pel, a typical 200,000 pel/frame 3 MHz bandwidth TV system would have to contain 200,000 delta modulators each operating at a 6 MHz sampling rate. Fortunately only one 6 MHz delta modulator need be used to implement Fig 20; however, this single delta modulator will have to contain enough shift register type memory to store an entire picture frame.

The reason that one delta modulator can replace all the delta modulators of Fig 20 with no increase in operating speed is simple. If Fig 20 was implemented as shown all 200,000 pels could be encoded, decoded and displayed in parallel, but a real time television system requires only one pel at a time in serial. The retention time of the eye and screen give the appearance of a full picture. We may take advantage of this by starting a single delta modulator at the upper most left hand corner of a frame, let it encode that pel based upon its previous estimate of the pel from the previous frame, transmit a bit (E_K), store its new estimate (X_K) for that pel, and then repeat the process for the next adjacent pel in the same frame. The delta modulator will continue to encode, and transmit for each adjacent pel in turn, until the delta modulator has been multiplexed through the entire frame (typically 1/30 sec). Then the delta modulator will return to the first pel and repeat the process for the next frame.

Figure 21 shows the block diagram of the frame to frame delta modulator. This delta modulator is the same as the one shown in Fig 6 except for the addition of fourteen 131,000 bit long shift registers. The shift registers were assembled out of Intel's 2107 4K dynamic random access memories.

The following paragraph gives a brief explanation of how the random access memories were assembled into shift registers. The memory chips were paired as

shown in Fig 22 to produce two hundred and twenty four, 8,195 bit long shift registers. A memory can be turned into a shift register by sequenially addressing the memory, one memory location for each read-modify-write cycle of the memory. In this way the memory appears to shift all the data bits one place to the right (just like a shift register does) for each memory cycle. Since the read-modify-write cycle of these memories takes 1 μs, the maximum shift rate of the 8,195 bit long shift register was only 1 MHz. To achieve a minimum 6 MHz shift rate required for real time processing, sixteen of the 8,195 bit long shift registers were cascaded by two and multiplexed by eight as shown in Fig 23 to produce one 131,120 bit long 8 MHz shift rate shift register. Timing signals and syncronization were provided by the circuits shown in Fig 24 and 25. Pictures of the circuit boards can be seen in Fig 26.

[The hardware for the frame to frame delta modulator is not yet complete. We hope to complete the unit and obtain results by September 1976.]

Two Dimensional Delta Modulators

We are developing two dimensional delta modulator algorithms to encode video signals. Preliminary results suggest that pictures encoded by these two dimensional delta modulators will not suffer as severely from edge business as do pictures encoded by one dimensional delta modulators.

At the present time we are investigating several types of two dimensional delta modulators. One type under investigation consists of two, one dimensional delta modulators such that one delta modulator scans the picture horizontally, while the other scans the picture vertically. The two delta modulators interacted at every picture element to produce a combined estimate of the picture and a single one bit output for each picture element in the picture. The defining equations for the delta modulator are:

Output Equations

$$E_k = \text{Sign} \quad S_k - X_k^P$$

$$X_k^P = (X_k^H + X_k^V) / 2$$

Estimate Equations

$$X_k^H = LX_{k-1}^H + Y_k^H$$

$$X_k^V = LX_{k-n}^V + Y_k^V$$

Step Size Equations

$$Y_k^H = | Y_{k-1}^H | \quad a E_{k-1} + b E_{k-2}$$

$$Y_k^V = | Y_{k-n}^V | \quad a E_{k-n} + b E_{k-2n}$$

E_K = One bit wide output of the two dimensional delta modulator

S_K = k^{th} sample of the input picture

X_K^P = The two dimensional delta modulator's estimate of the picture

X_K^H = The horizontally scanned delta modulator's estimate of the picture

X_K^V = The vertically scanned delta modulator's estimate of the picture

Y_K^H = The horizontally scanned delta modulator's step size

Y_K^V = The vertically scanned delta modulator's step size

n = The number of samples in a scanning line of the picture

a, b, L = Constants which are experimentally adjusted to optimize the delta modulated encoded picture

In Fig 27 a one dimensional delta modulator is compared with a two dimensional delta modulator. Although the picture encoded with the two dimensional delta modulator is unsatisfactory due to "corner effects" the almost complete lack of edge business on horizontal and vertical edges, suggests that this approach to two dimensional delta modulation if investigated further might be modified to yield satisfactory pictures. It has been suggested that a third delta modulator scanning diagonally (the other two scan horizontally and vertically) may eliminate the corner effect, or even a modification of the step size equation may help.

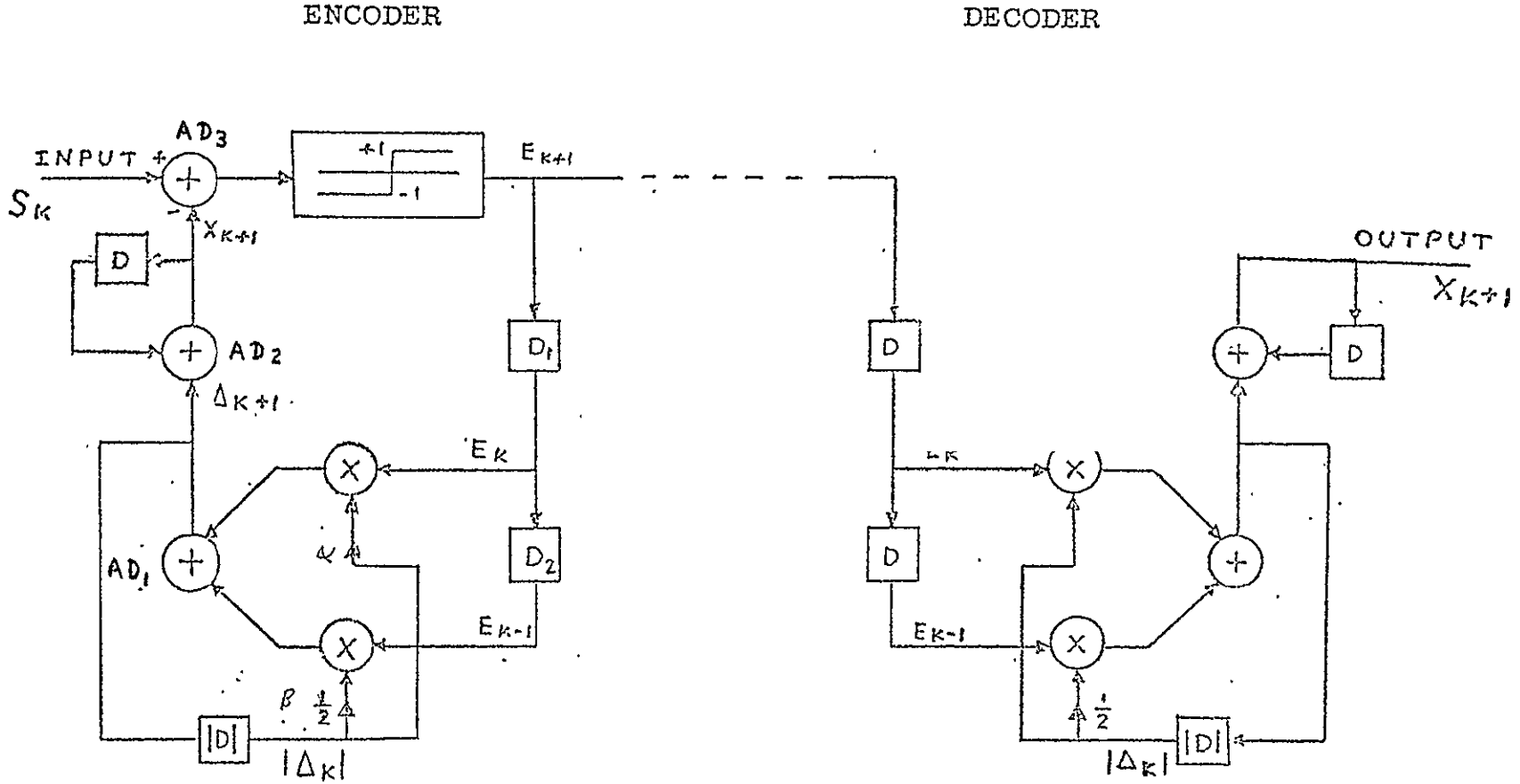


FIG. 1 DIGITAL ADAPTIVE DELTA MODULATOR

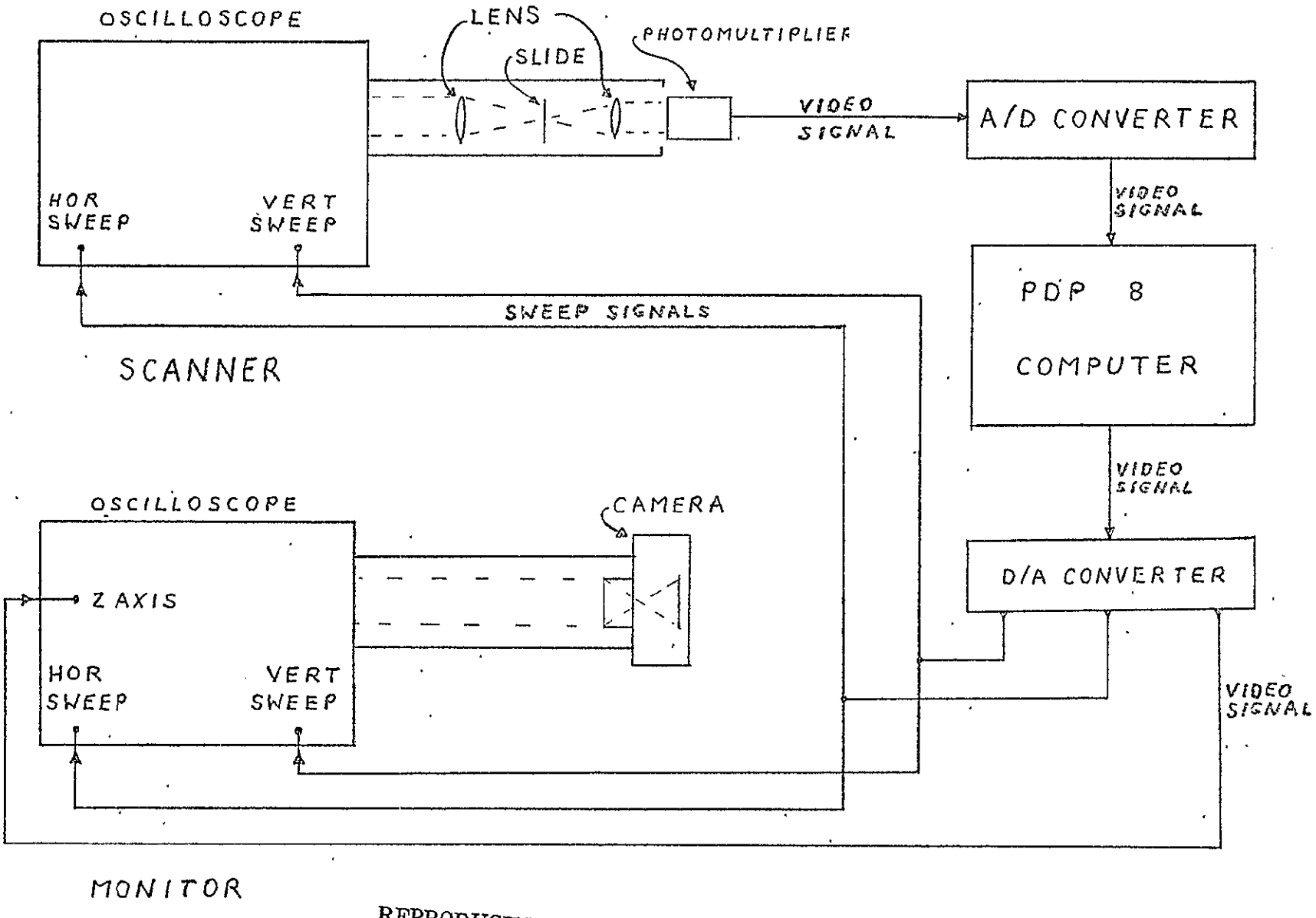


FIG. 2 COMPUTER PROCESSOR FOR PICTURES

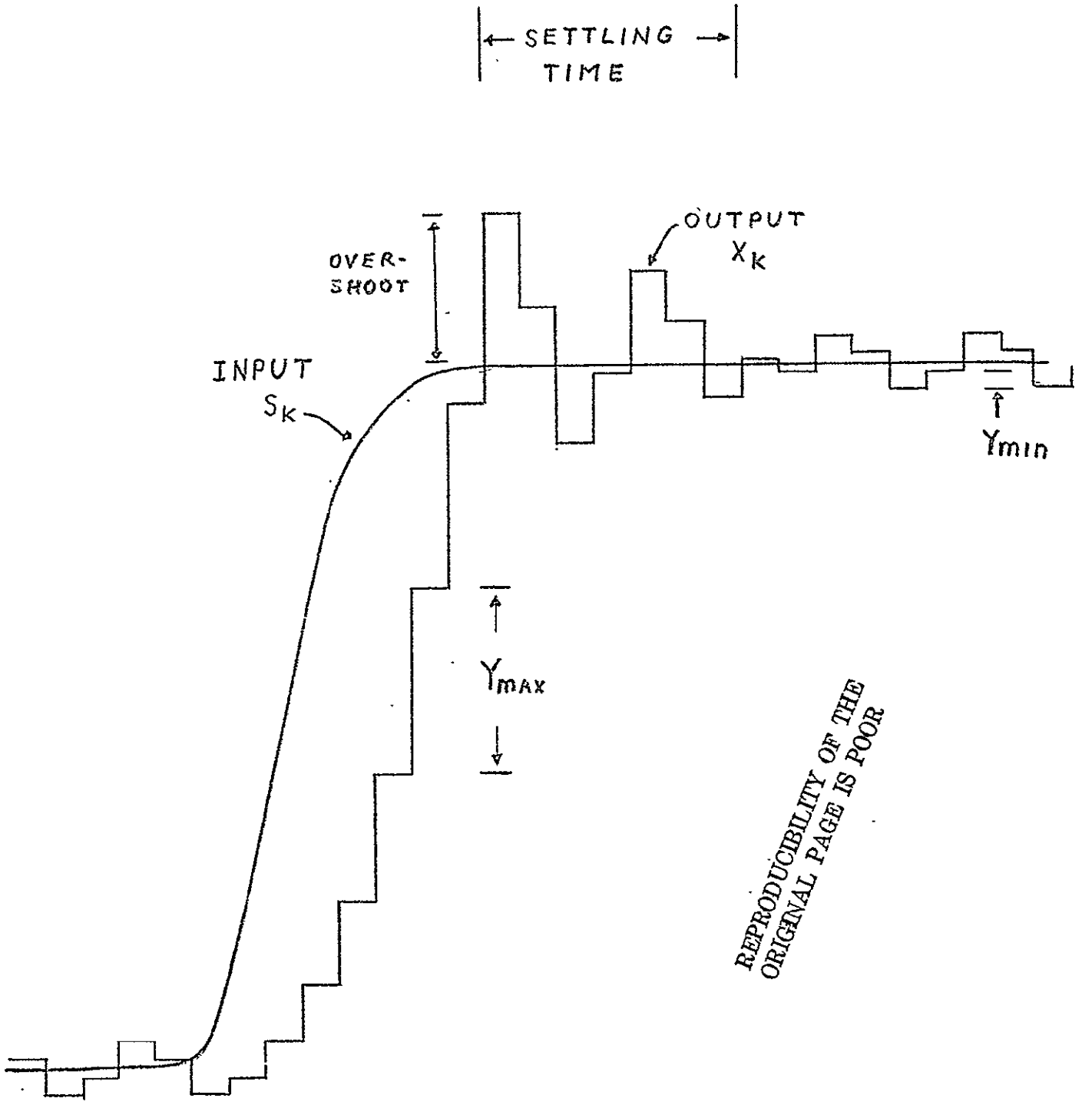
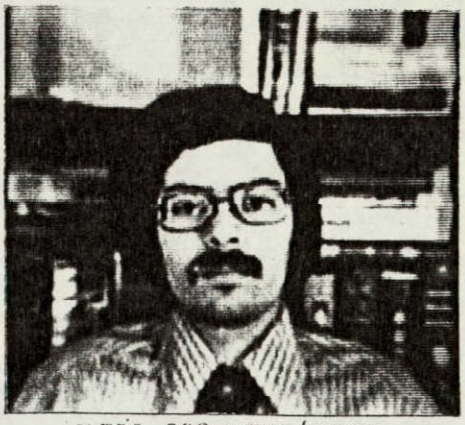
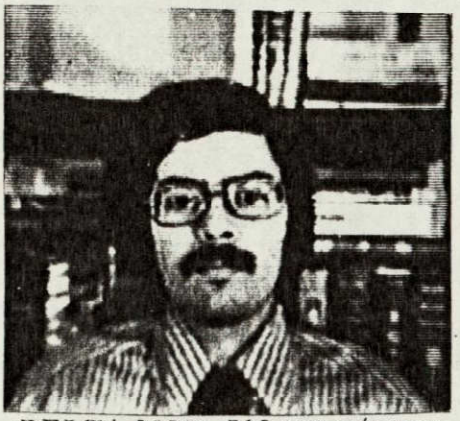


Fig. 3 The response of the delta modulator to a step like input

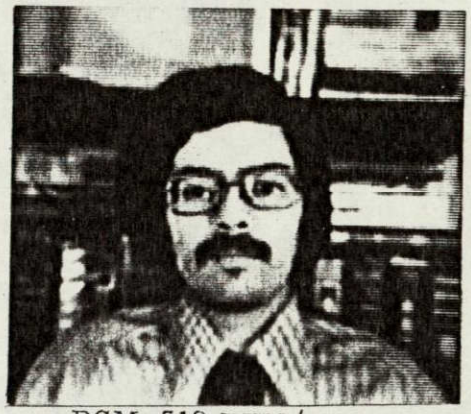
DELTA MOD 682 BITS/LINE



PCM 682 BITS/LINE



DELTA MOD 512 BITS/LINE



PCM 512 BITS/LINE

DELTA MOD 410 BITS/LINE

PCM 410 BITS/LINE

Fig. 4 A comparison of an adaptive delta modulator and a PCM encoder of video signals; 170 scaning lines per picture; PCM pictures have 64 quantization levels.

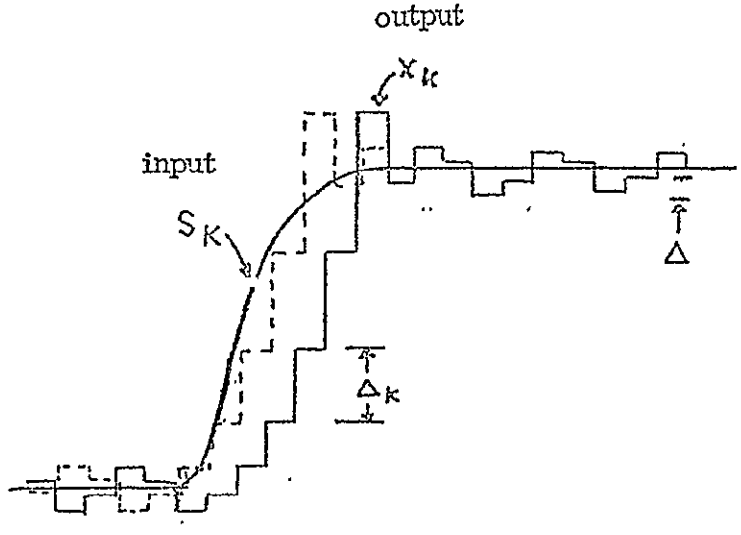


Fig. 5 Response of the Delta Modulator to a Step Input with Different initial Conditions

FIG. 6 HIGH SPEED VIDEO ΔMOD

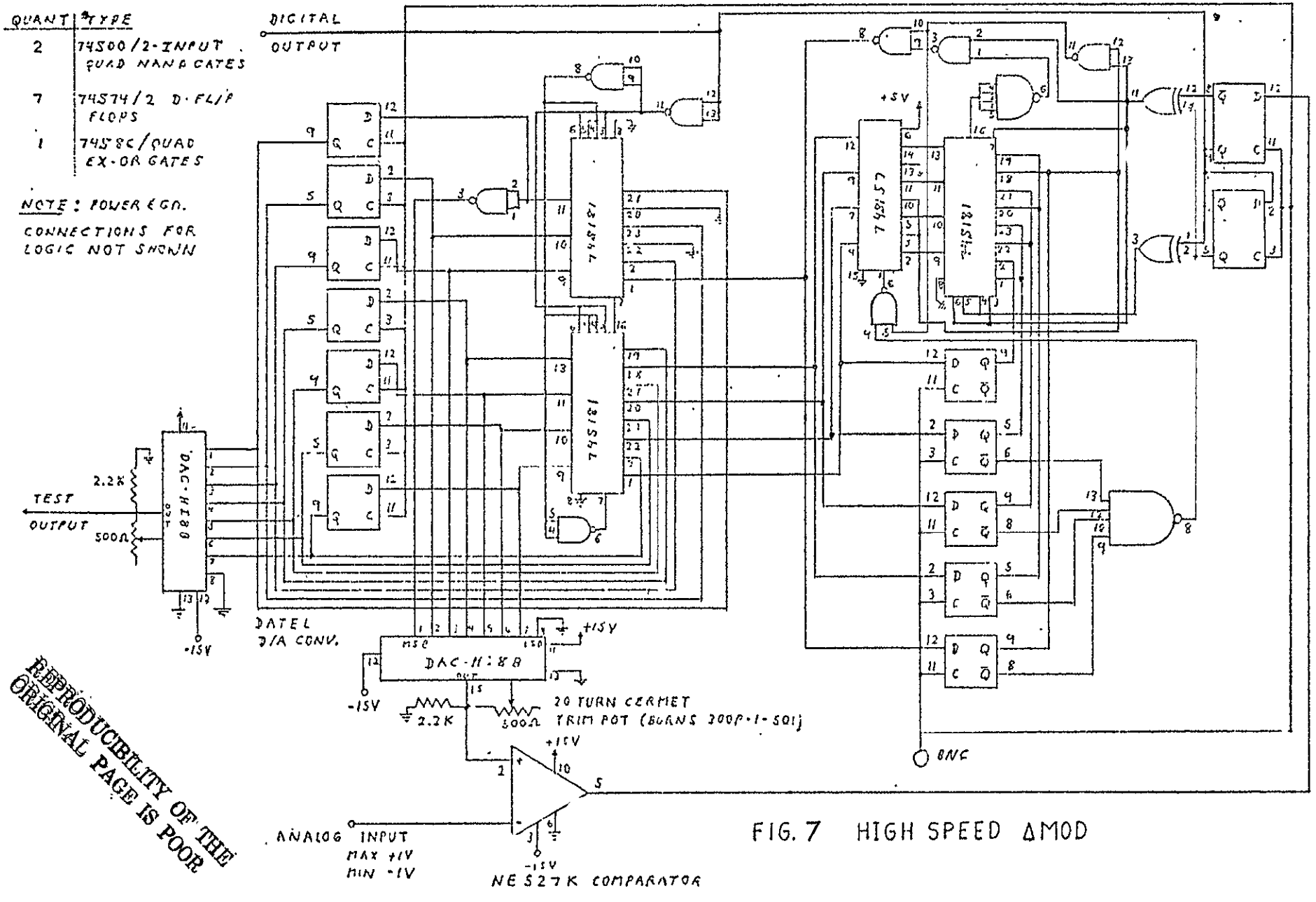


FIG. 7 HIGH SPEED ΔMOD

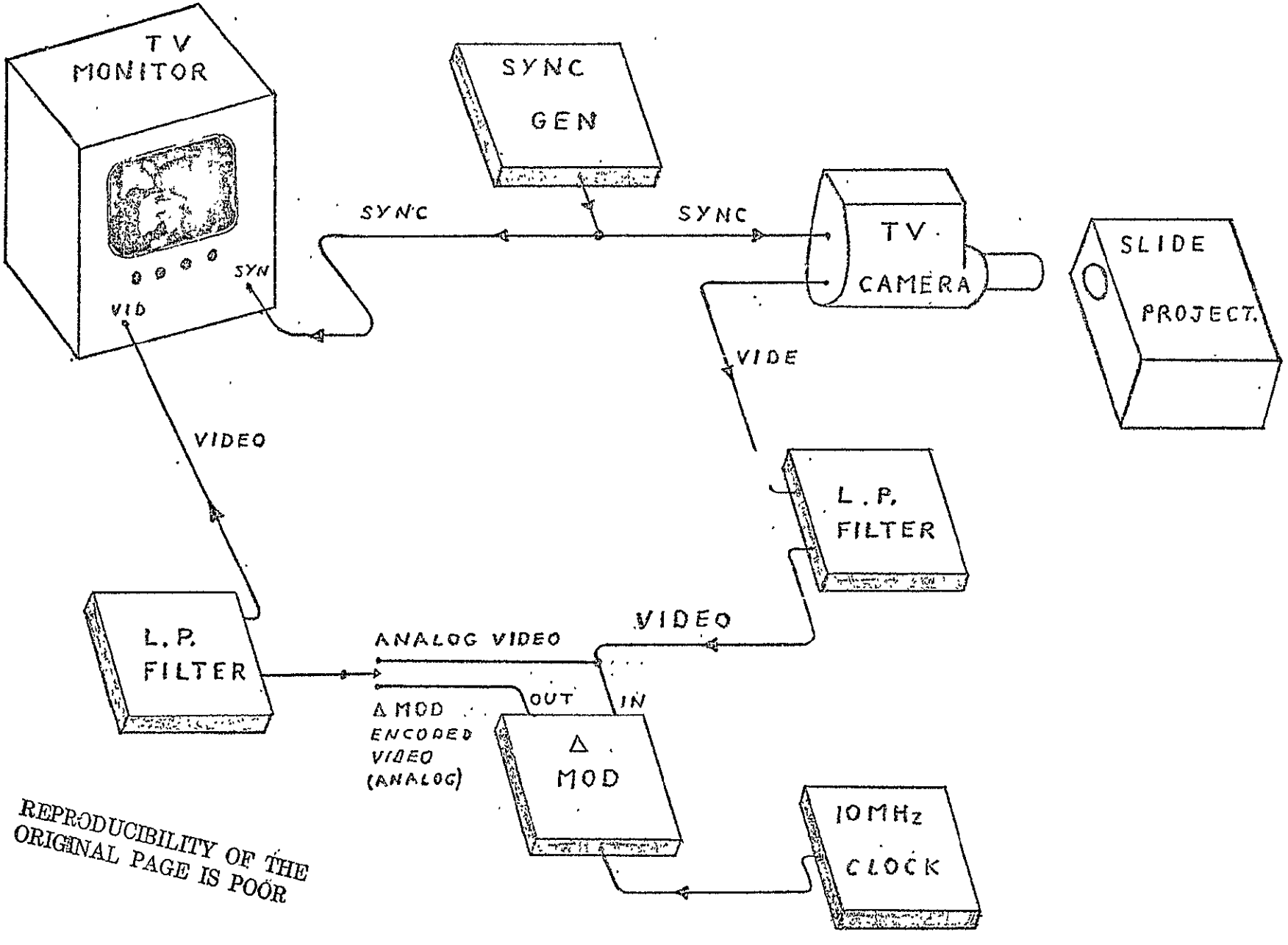


Fig. 8 Real-Time Video Processor For Delta Modulated Television Pictures

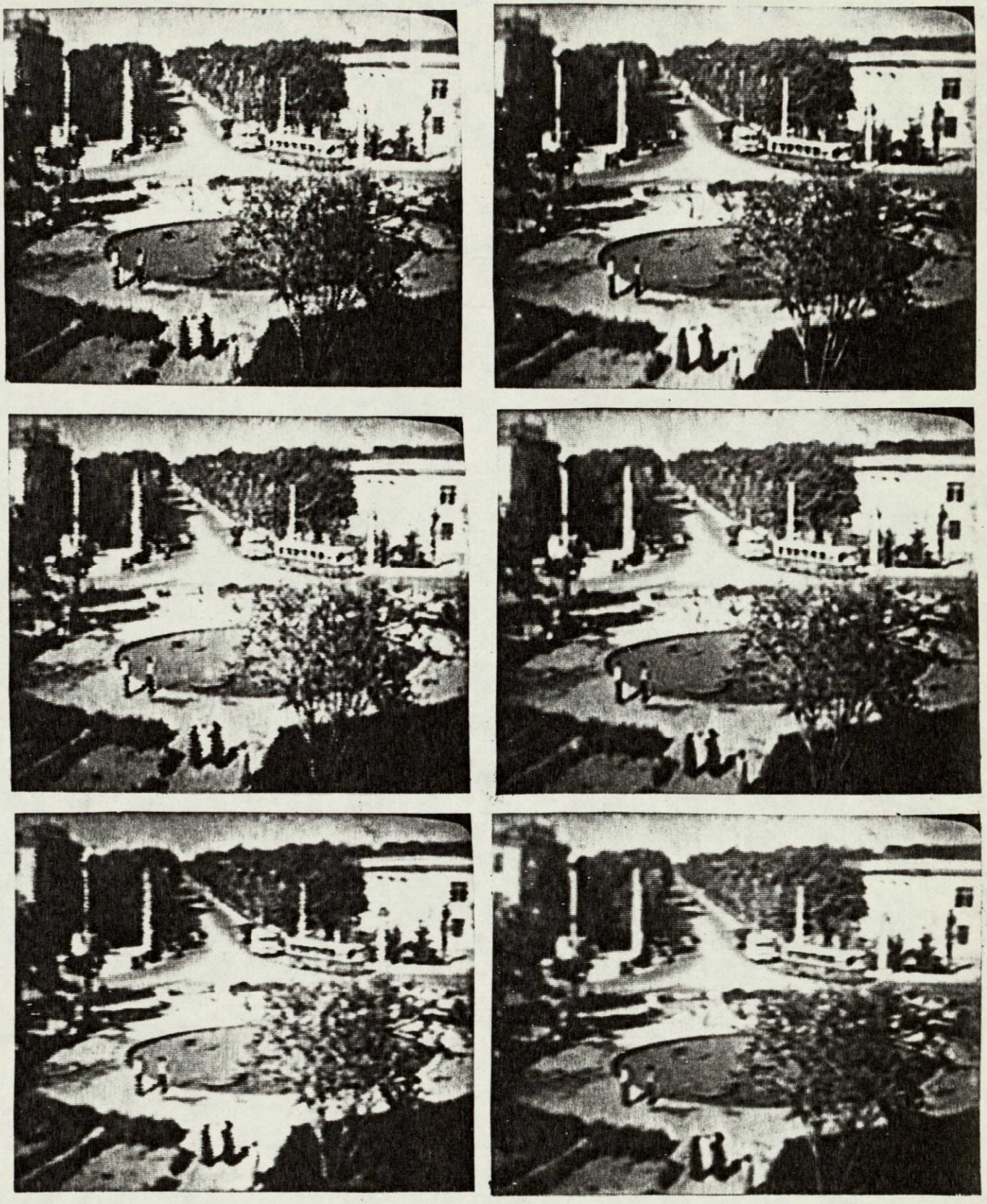
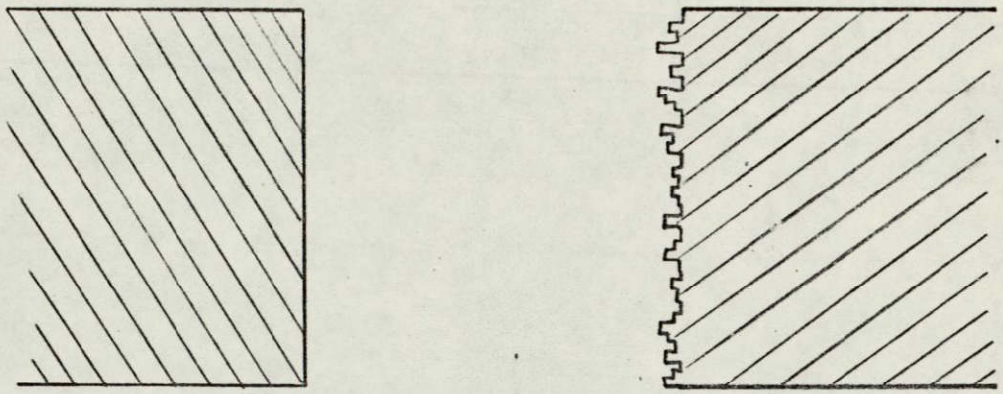


Fig. 9 A comparision of delta modulated pictures (left column) and unencoded pictures (right column) from a real time NTSC TV camera; Top row, $2MH_Z$ bandwidth; Middle row, $1.5MH_Z$ Bottom row, $1MH_Z$



(a) (b)

Fig. 9a The effects of edge business on an edge
(a) Edge before delta mod encoding
(b) Edge after delta mod encoding

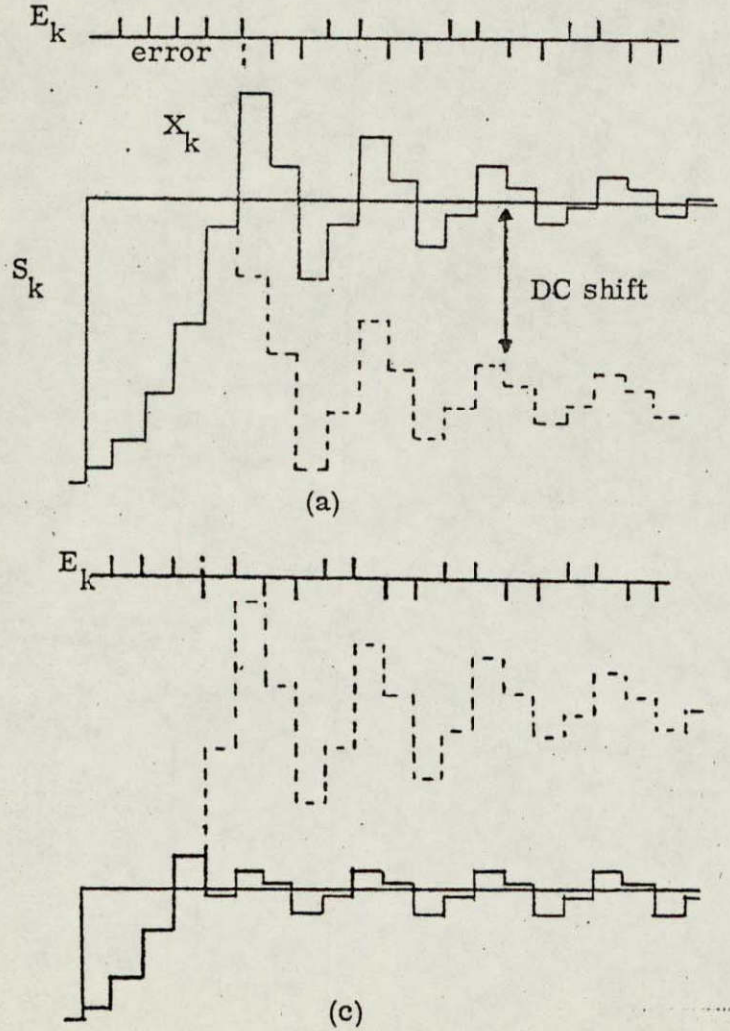
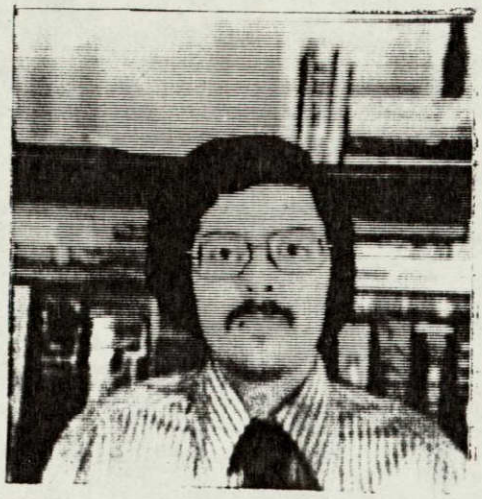
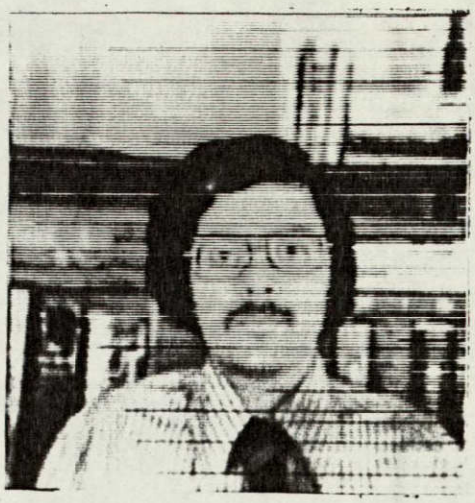


Fig.10 The effects of a single channel error on the output of the delta modulator
(a) No change in step size
(b) Decrease in step size
(c) Increase in step size

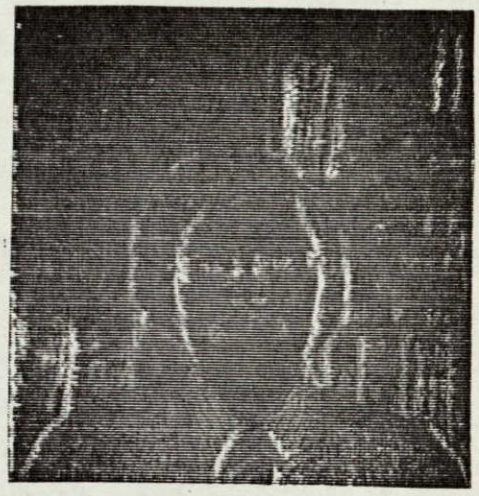


(a)

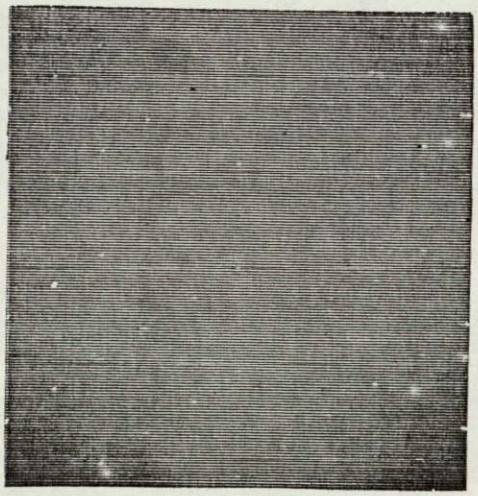


(b)

(c)



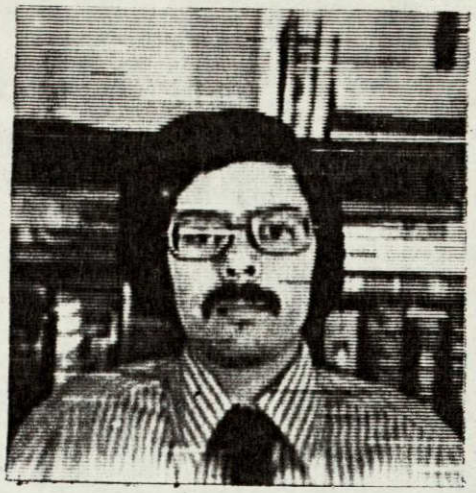
(d)



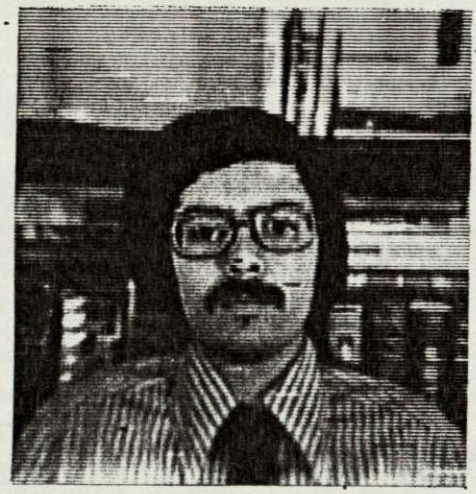
(e)

Fig. 11 The effects of channel errors on delta modulated encoded pictures. (a) Delta modulated picture without channel errors; 682 bits/line, 170 lines. (b) Error rate of 4×10^{-4}. (c) Aboslute value of Δ_k (d) Absolute value of Δ_k with channel errors (e) Difference between (c) and (d), i.e. step size errors.

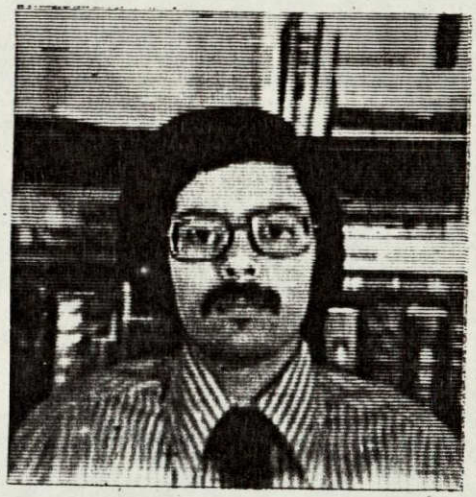
(a) Nosiy picture; 3×10^{-4} error rate; 1024 bits/line; 170 lines.



(b) 4 corrections per line; 1.5% increase in bit rate.



(c) 8 corrections per line; 3% increase in bit rate.



(d) 16 corrections per line; 6% increase in bit rate.

Fig.12 The effect of sending the encoders estimate to the decoder to acheive error correction.

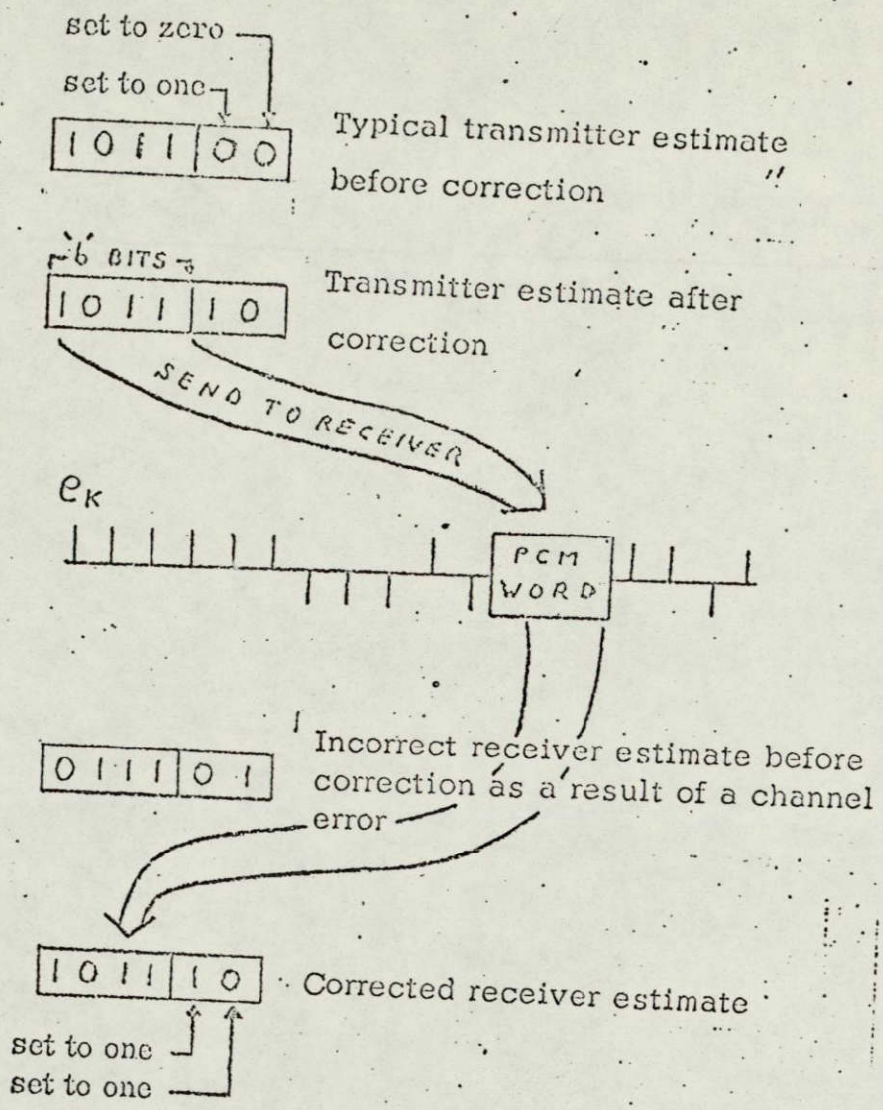
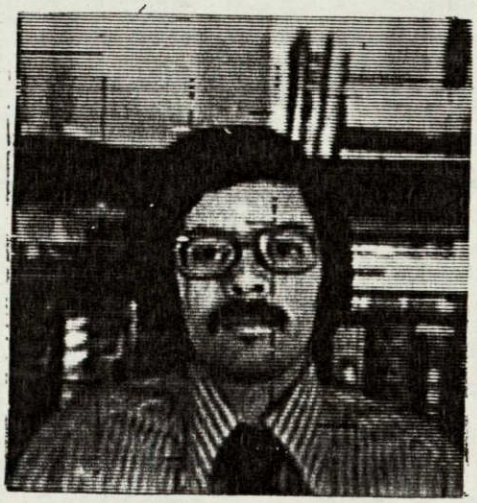
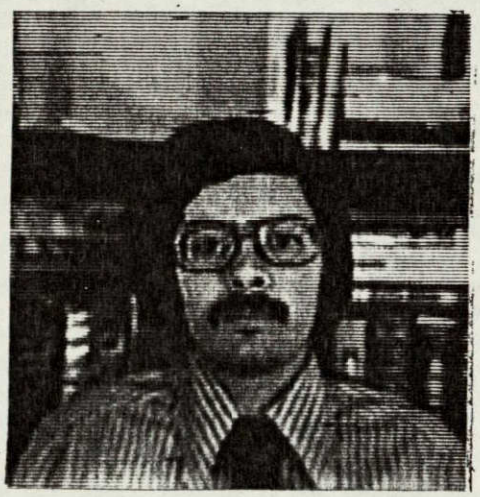


Fig.13 Error correction is achieved by sending the "b" most significent bits of the transmitter's estimate to the receiver.

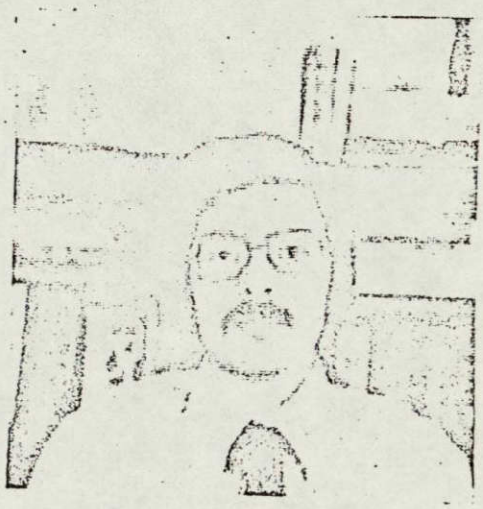
(a) b = 1



(b) b = 2

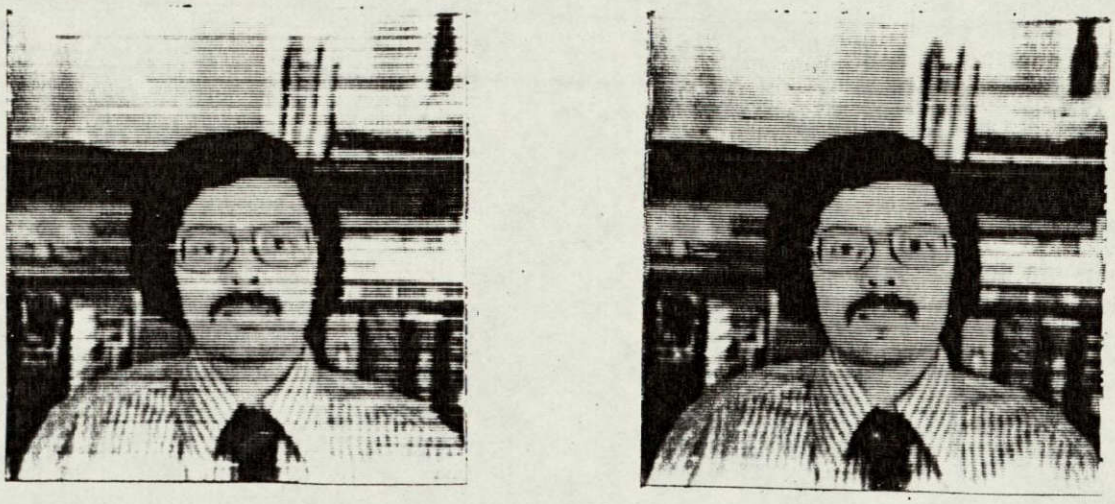


(c) b = 3



(d) b = 4

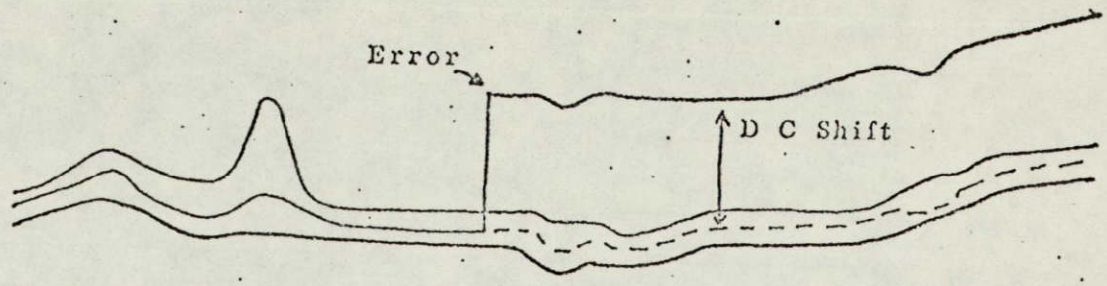
Fig. 14 The effect of sending only the "b" most significent bits of the encoders estimate to the decoder for error correction.



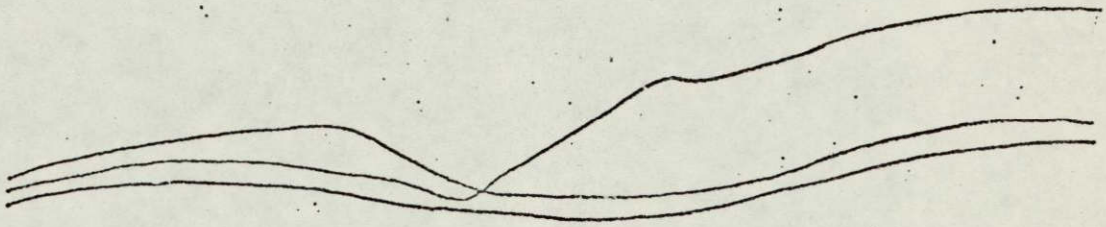
(a)

(b)

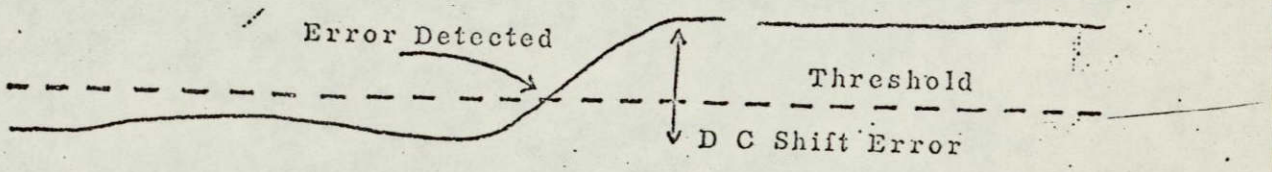
Fig. 15 Error correction is achieved by the use of a leaky integrator.
(a) Error rate 4×10^{-3}; 682 bits / line; 170 lines per picture
(b) Leaky integrator with a leak factor of 1 = .937



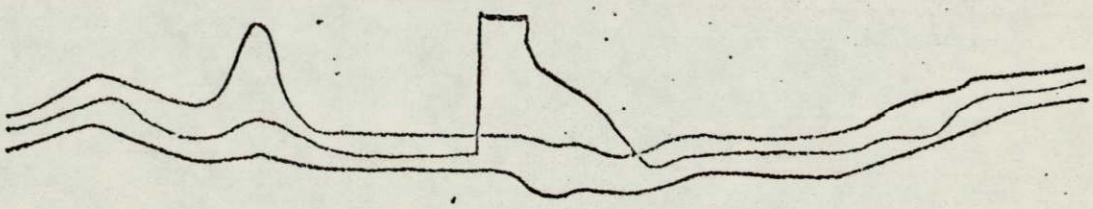
Part A. The Video Signal From 3 Consecutive Scanning Lines



Part B. The Video Signal After Averaging 'N' Consecutive Pixels



Part C. The Absolute Value of the Difference Between the Middle Wave form and the Average of the Top and Bottom of Part B. is Shown in Part C.



Part D. The D C Shift of Part C. is Subtracted from the Video Signal to Produce the Corrected Signal of Part D.

Fig. 16 A line to line correlation algorithm for error correction

Original Picture
(a)

Noisy Picture
(b)

Threshold 1/16 P-P Signal
Averaged Over 1/16 Of A Line
(c)

Threshold 1/32 P-P Signal
Averaged Over 1/16 Of A Line
(d)

Threshold 1/16 P-P Signal
Averaged Over 1/128 Of A Line
(e)

Threshold 1/32 P-P Signal
Averaged Over 1/128 Of A Line
(f)

Fig 17 The results of using the line to line correlation algorithm on noisy pictures. 1000 bits/line; 170 lines per picture; error rate of 3×10^{-3}

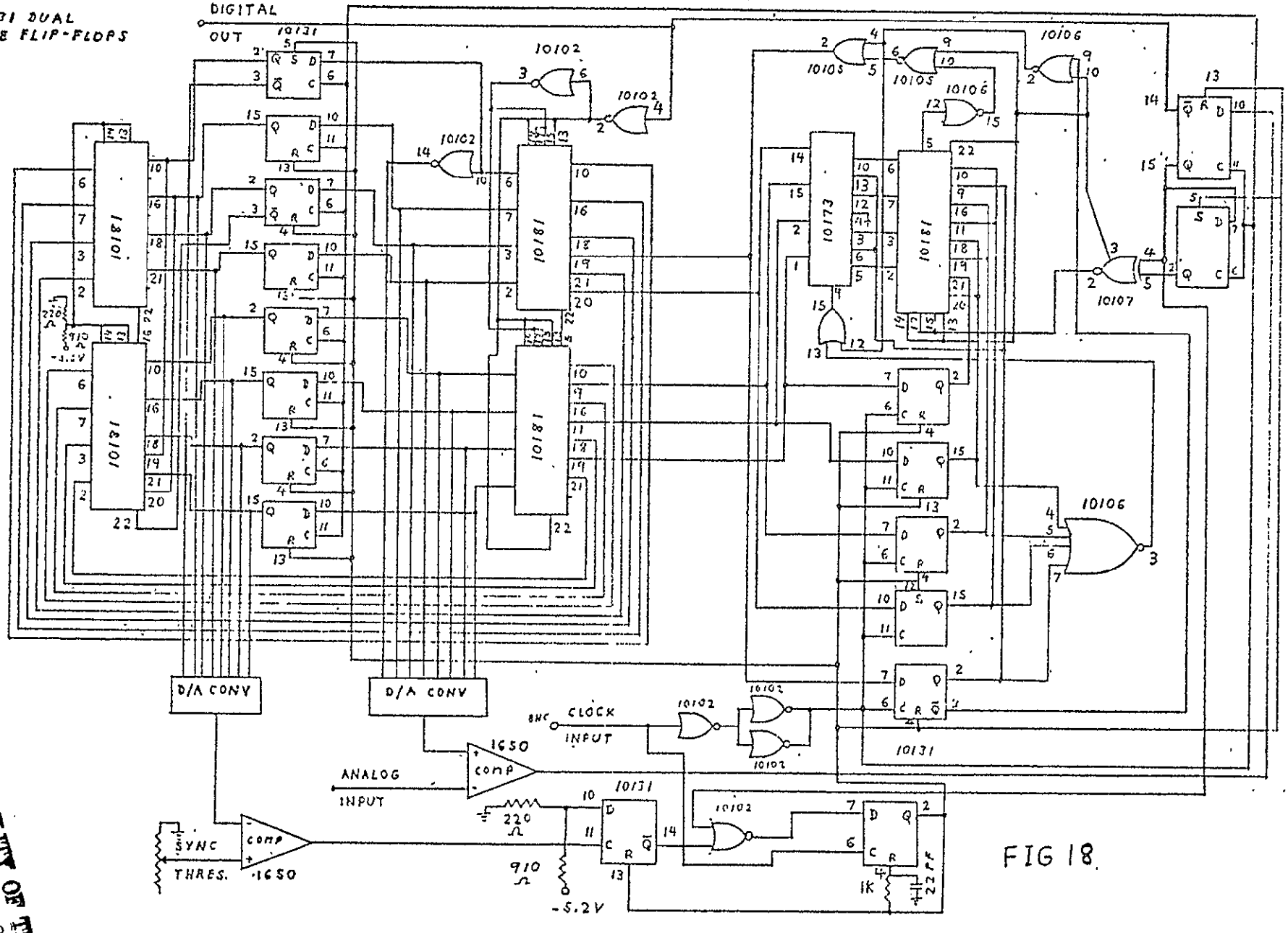


FIG 18.

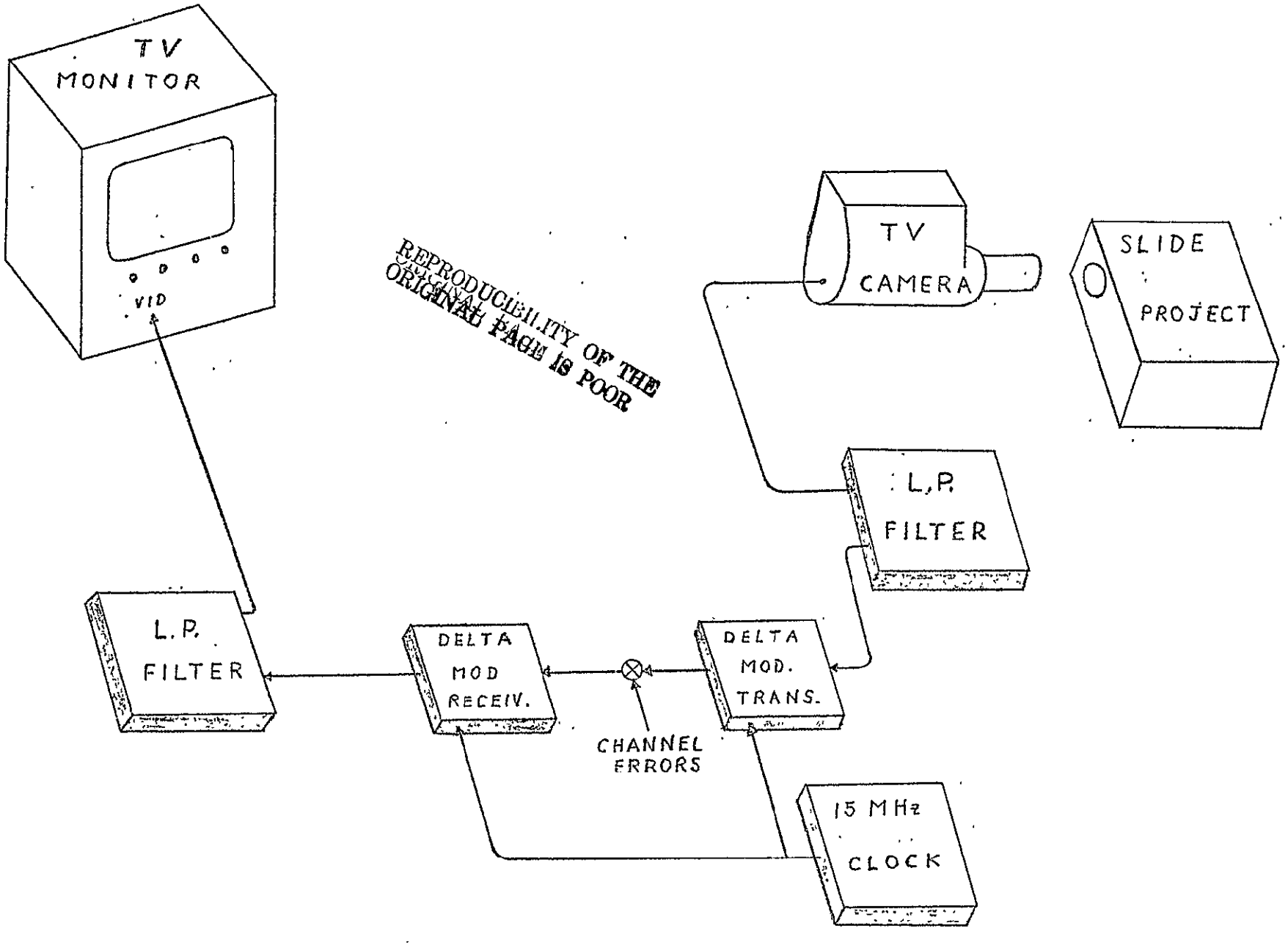


Fig. 19 Real time video processor for delta modulator with error correction

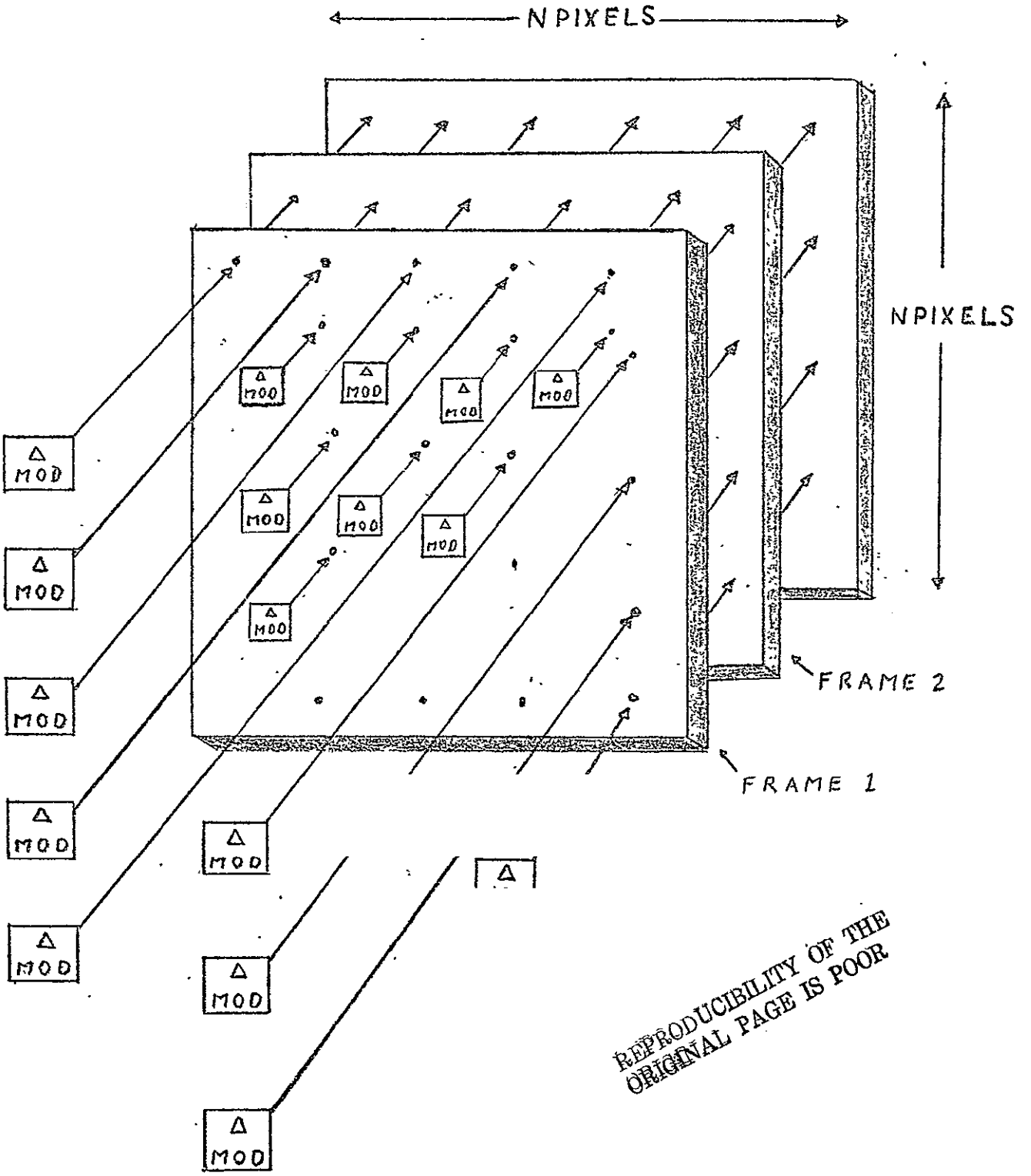


FIG.20 FRAME TO FRAME ENCODING OF PICTURES USING DELTA MODULATION

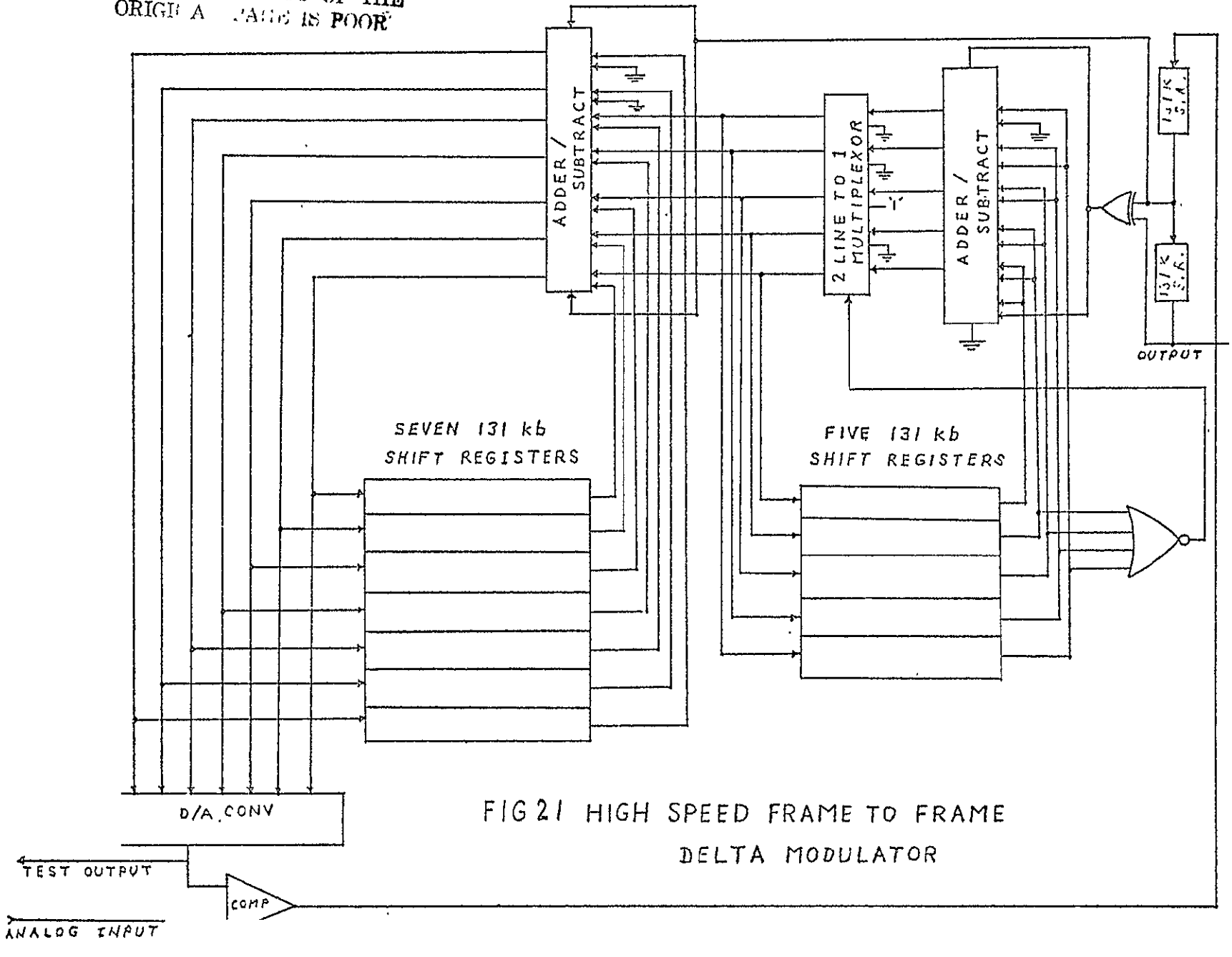
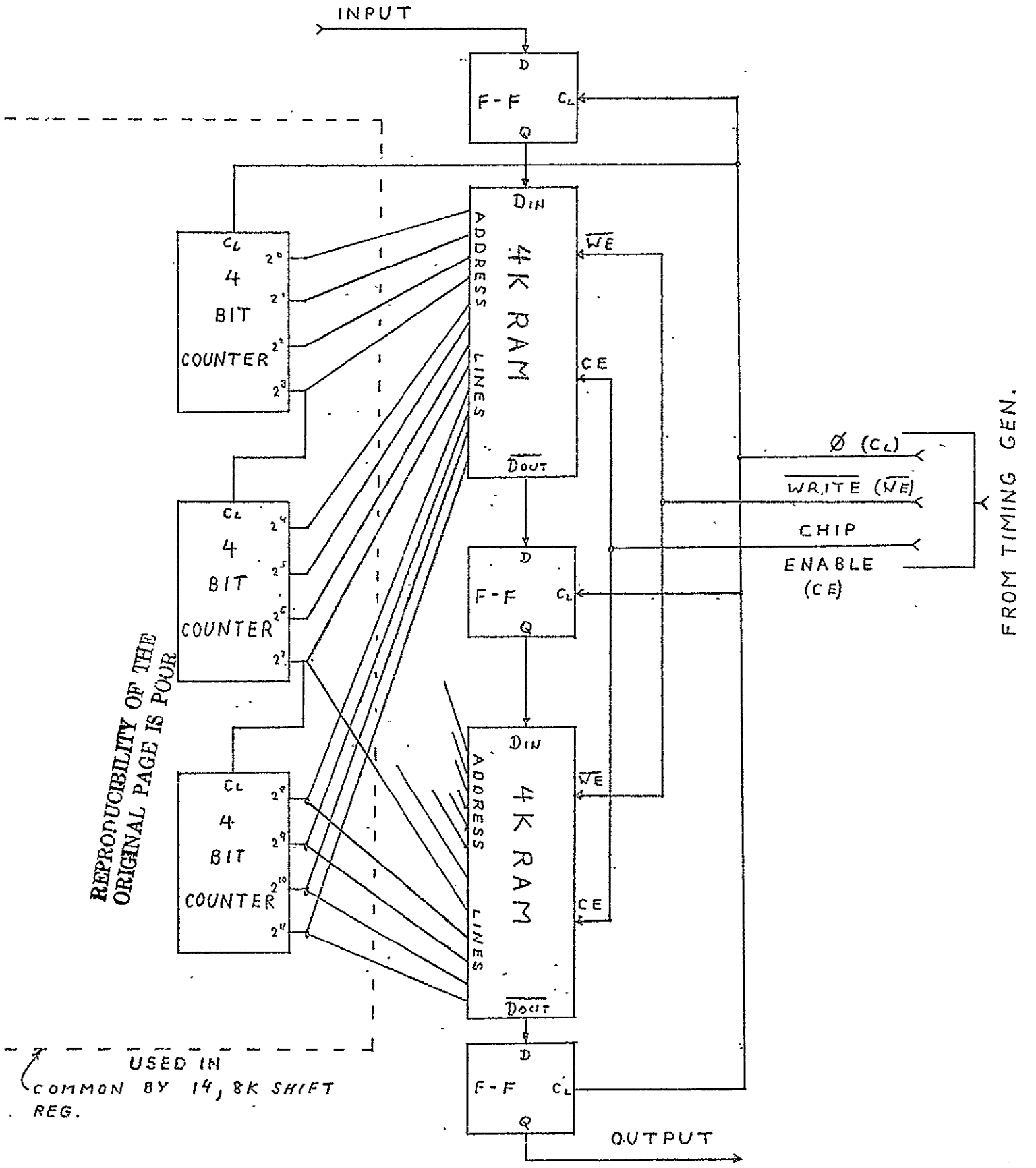


FIG 21 HIGH SPEED FRAME TO FRAME DELTA MODULATOR

Fig.22 One 8K Shift Register Made From 8K of Random Access Memory



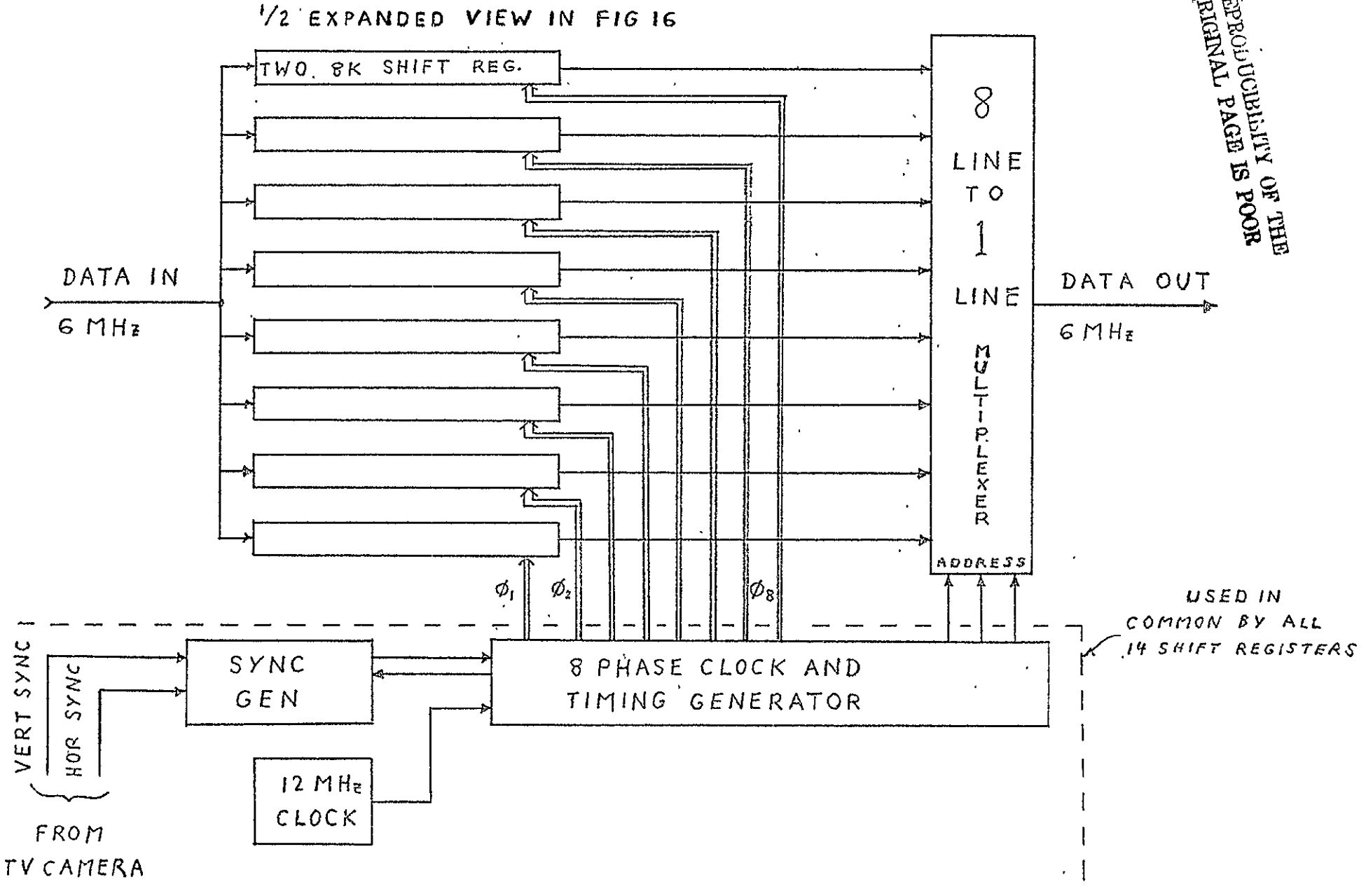


Fig.23 One of Fourteen, 131,000 Bit Long Shift Registers

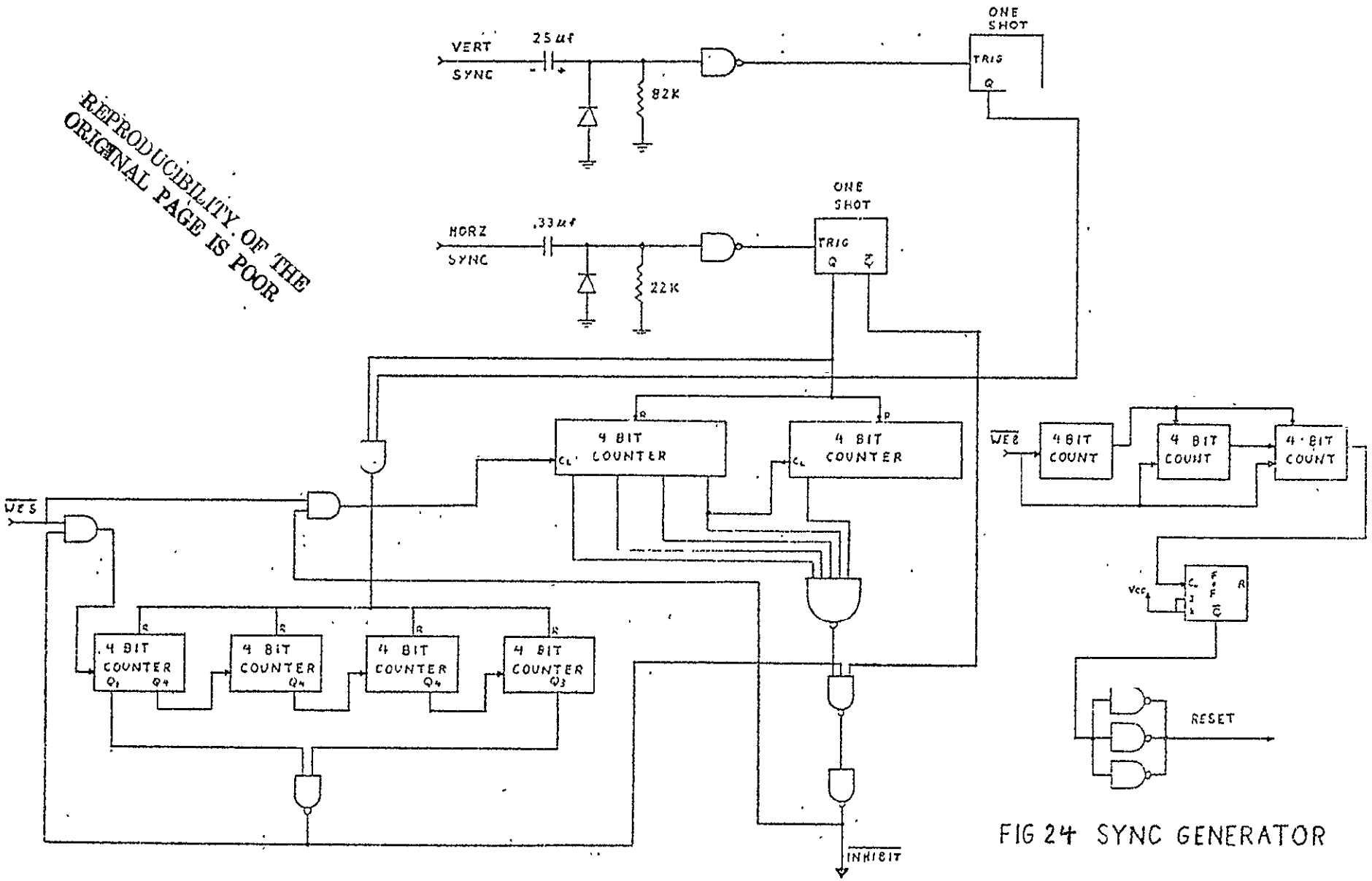


FIG 24 SYNC GENERATOR

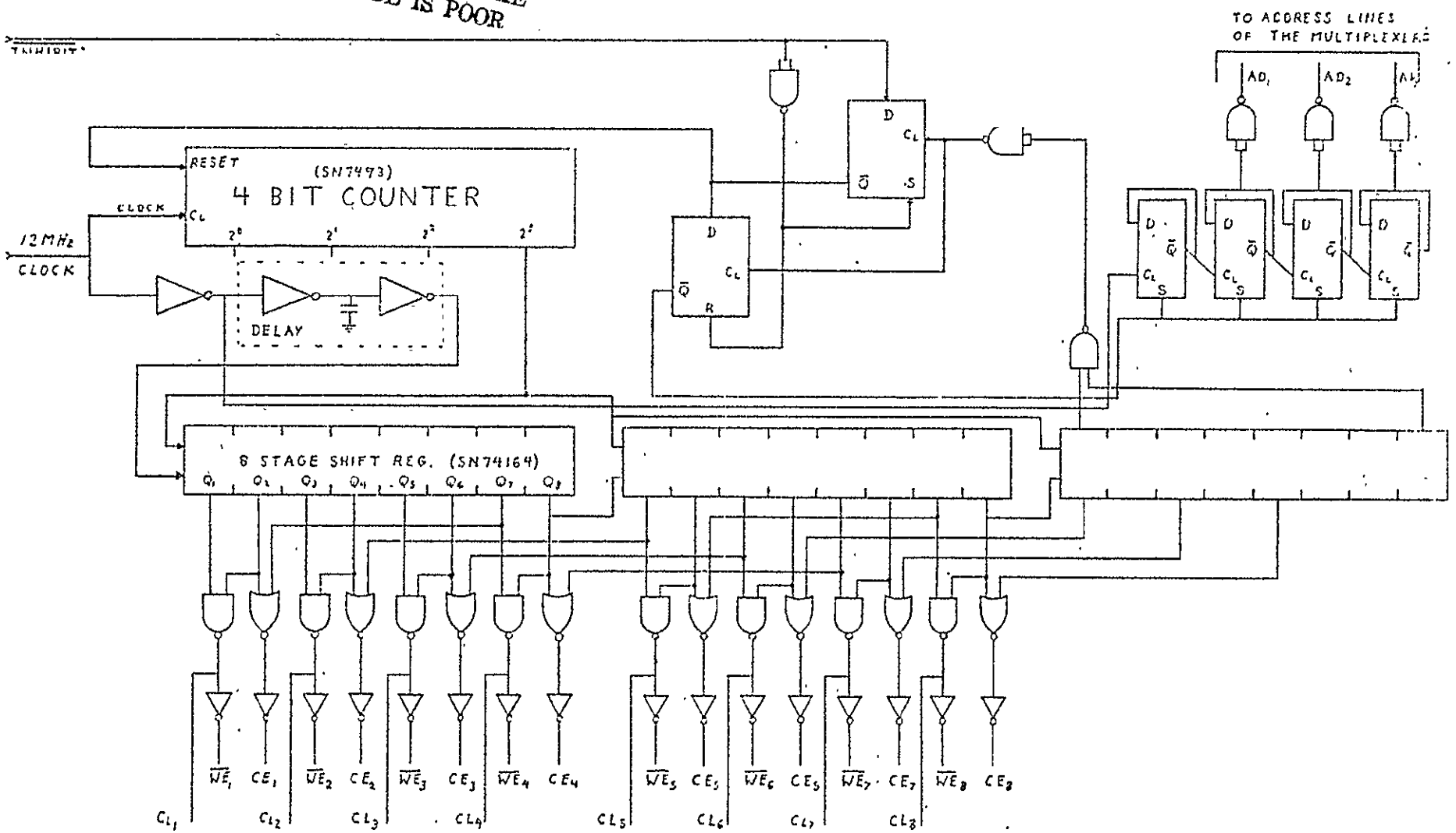
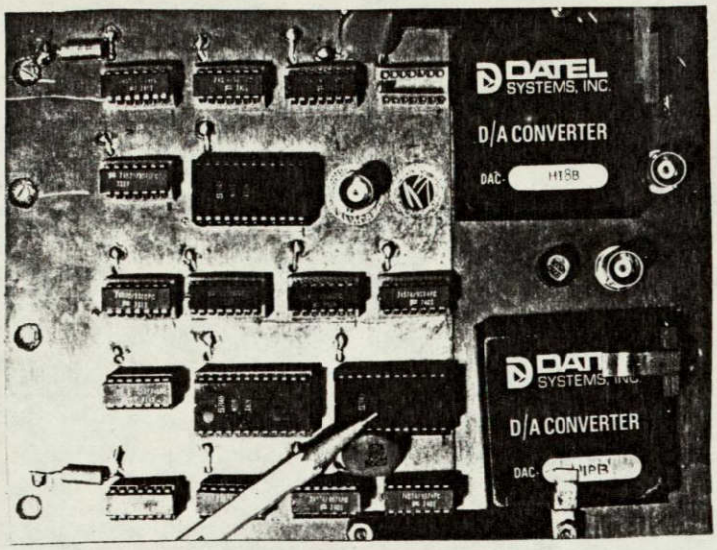
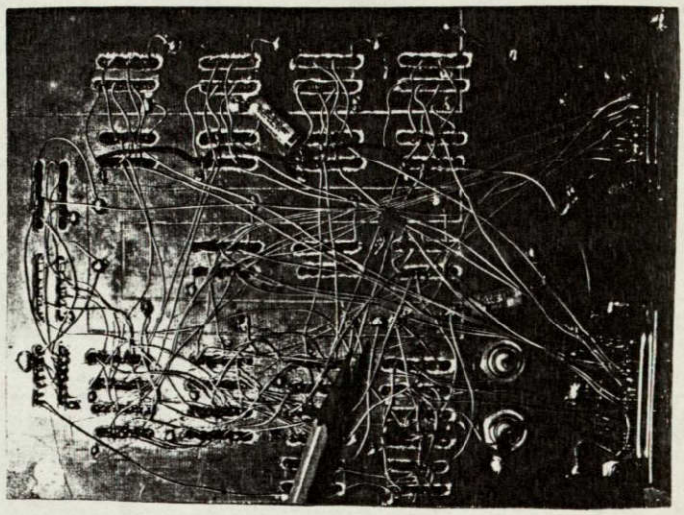
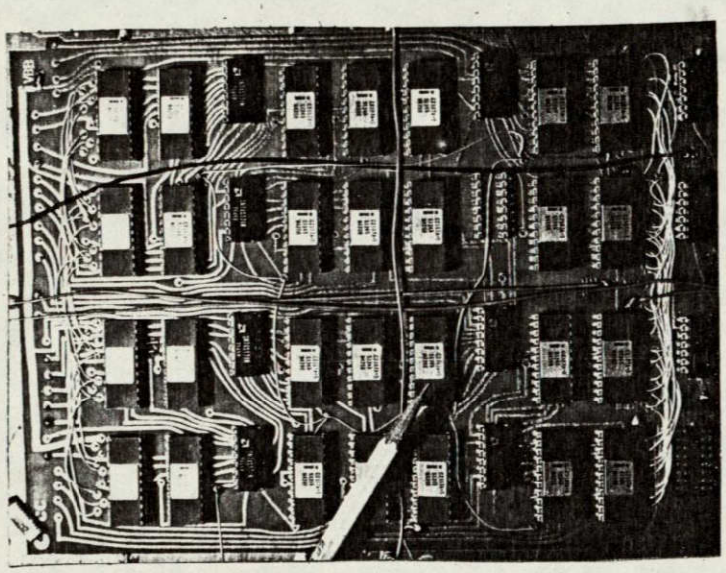


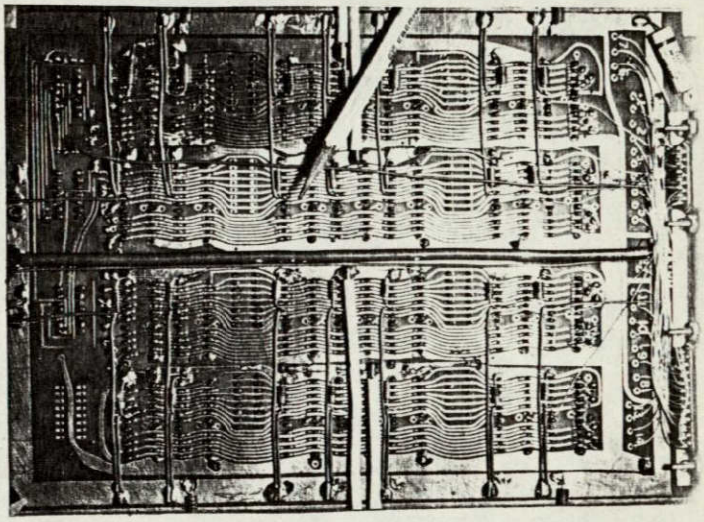
FIG 25 8 STAGE CLOCK AND TIMING GENERATOR

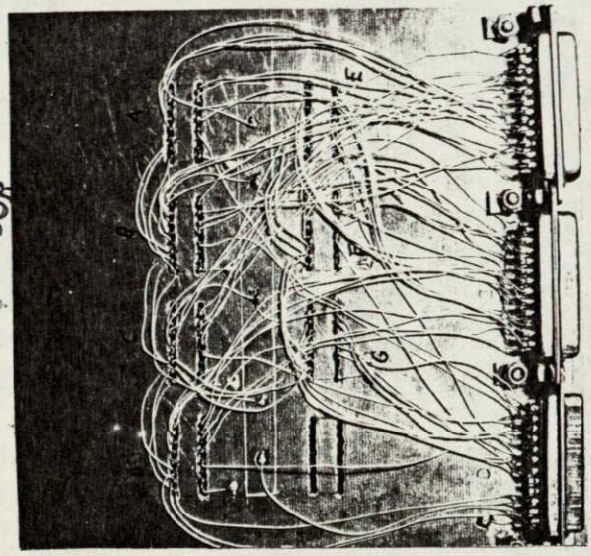
Fig. 26 Circuit boards for the frame to frame delta modulator
Clockwise from top left: Delta modulator;Timing generator;
One of 16 shift register boards - bottom view;Sync generator;
Multiplexer;Shift register board-top view.











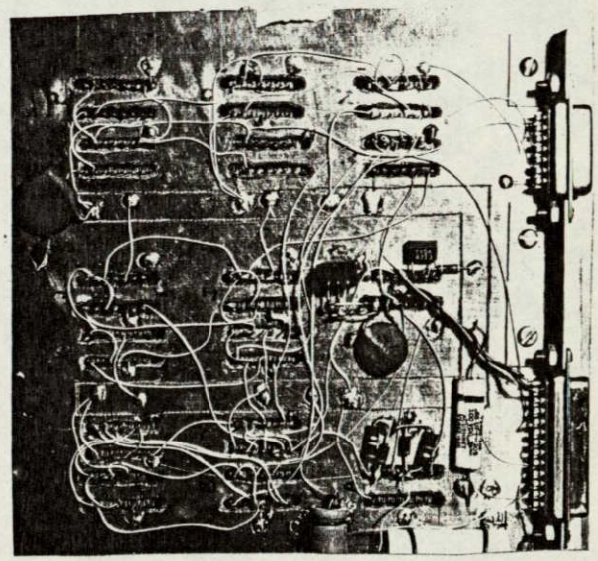
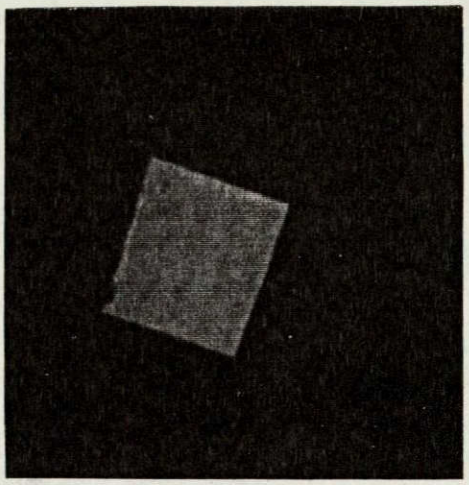
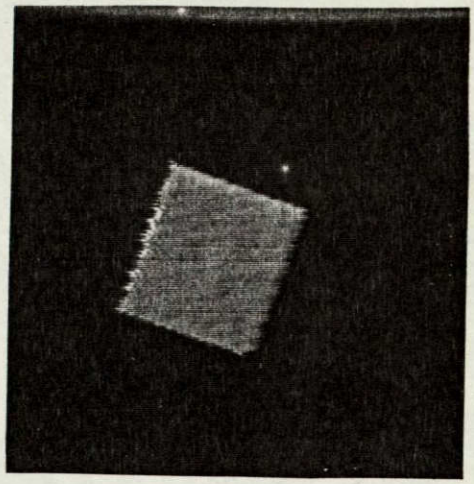


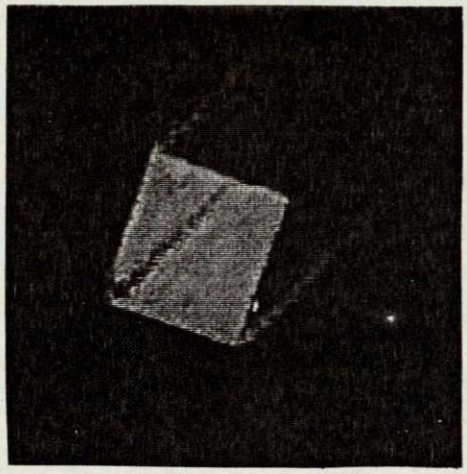
FIG. 26



(a)



(b)



(c)

Fig. 27 A comparision of one and two dimensional delta modulator picture encoders; (a) Original picture; (b) One dimensional delta modulator; (c) Two dimensional delta modulator