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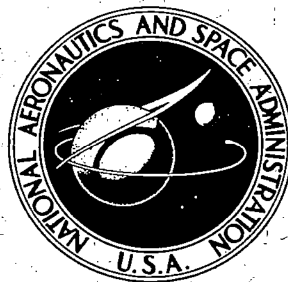

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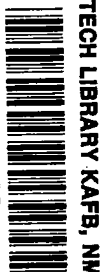
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HIGH AND LOW THRESHOLD P-CHANNEL METAL OXIDE SEMICONDUCTOR PROCESS AND DESCRIPTION OF MICROELECTRONICS FACILITY

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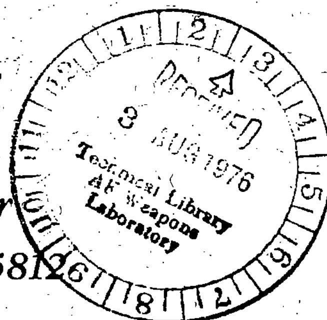
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16. ABSTRACT

The fabrication techniques and detail procedures for creating P-channel Metal-Oxide-Semiconductor (P-MOS) integrated circuits at George C. Marshall Space Flight Center (MSFC) are described. Examples of P-MOS integrated circuits fabricated at MSFC together with functional descriptions of each are given. Typical electrical characteristics of high and low threshold P-MOS discrete devices under given conditions are provided. A general description of MSFC design, mask making, packaging, and testing procedures is included.

The capabilities described in this report are being utilized in: (1) research and development of new technology, (2) education of individuals in the various disciplines and technologies of the field of microelectronics, and (3) fabrication of many types of specially designed integrated circuits which are not commercially feasible in small quantities for in-house research and development programs.

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LIST OF SYMBOLS

Symbol	Definition
V_T	Threshold Voltage, V
V_{GS}	Gate to Source Voltage, V
V_{DS}	Drain to Source Voltage, V
V_{FB}	Flatband Voltage, V
ΔV_{FB}	Shift of Flatband Voltage, V
BV_{DSS}	Drain to Source (Gate Shorted) Breakdown Voltage, V
I_{DSS}	Drain to Source (Gate Shorted) Leakage Current, A
I_{DS}	Drain to Source Current, A
g_m	Transconductance
ϕ	Phase
P^+	Heavy Concentration of P-type ions
H_2O	Water
N_2	Nitrogen Gas
O_2	Oxygen Gas
SiO_2	Silicon Dioxide
HCl	Hydrochloric Acid
HF	Hydroflouric Acid
HNO_3	Nitric Acid
H_3PO_4	Phosphoric Acid
H_2SO_4	Sulfuric Acid

LIST OF SYMBOLS (Concluded)

Symbol	Definition
CH_3COOH	Acetic Acid – Glacial
CrO_3	Chromic Acid Anhydride – Crystal
NH_4F	Ammonium Flouride – Crystal
SiH_4	Silane
BN	Boron Nitride

STANDARD ABBREVIATIONS

Symbol	Definition
s	second
m	meter
l	liter
g	gram
V	volt
A	ampere
K	kelvin
Hz	hertz
cm^3	cubic centimeter
min	minute
in.	inch
mil	10^{-3} inch
C	celsius

STANDARD ABBREVIATIONS (Concluded)

Symbol	Definition
k	kilo, 10^{3}
M	mega, 10^{6}
c	centi, 10^{-2}
m	milli, 10^{-3}
μ	micro, 10^{-6}
n	nano, 10^{-9}

NONSTANDARD ABBREVIATIONS

Symbol	Definition
P-MOS	P-channel Metal Oxide Semiconductor
IC	Integrated Circuit
MSFC	George C. Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
LSI	Large Scale Integration
LSIC	Large Scale Integrated Circuit
MSI	Medium Scale Integration
MSIC	Medium Scale Integrated Circuit
SSI	Small Scale Integration
SSIC	Small Scale Integrated Circuit
CAD	Computer Aided Design

NONSTANDARD ABBREVIATIONS (Concluded)

Symbol	Definition
HODAD	Hybrid Operational Digital Attenuator Device
Deltic	Delay Line Time Compressor
TG	Transmission Gate
PR	Photoresist
SN	Sulfuric-Nitric Acids
ACE	Acetone
TCE	Trichloroethylene
P	Positive
N	Negative
MIN	Minimum
MAX	Maximum
TYP	Typical
ppm	parts per million
tds	total dissolved solids
rps	revolutions per second
UV	Ultraviolet

HIGH AND LOW THRESHOLD P-CHANNEL METAL OXIDE SEMICONDUCTOR PROCESS AND DESCRIPTION OF MICROELECTRONICS FACILITY

SUMMARY

This report presents a description of the fabrication techniques, basic materials used, and other necessary details to create a P-channel Metal Oxide Semiconductor (P-MOS) integrated circuit. Examples of P-MOS integrated circuits fabricated at George C. Marshall Space Flight Center (MSFC) are shown with their functions and applications described. The detailed process is given with single discrete transistor configurations. Typical electrical characteristics of high and low threshold P-MOS discrete devices under given conditions are provided. Curves of silicon oxidations in two ambients, of boron diffusions, and of etch rates are included. A general description of MSFC design, mask making, packaging, and testing procedures is included.

This report demonstrates the capability of the Electronics Development Division at MSFC in the field of P-MOS microelectronics from conceptual design through final testing including mask making, fabrication, and packaging. The capabilities described in this report are being utilized in: (1) research and development of new technology, (2) education of individuals in the various disciplines and technologies of the field of microelectronics, and (3) fabrication of many types of specially designed integrated circuits which are not commercially feasible in small quantities for many in-house research and development programs.

I. INTRODUCTION

The P-MOS process for the fabrication of microelectronic integrated circuits (IC) is the initial monolithic MOS technology. The P-MOS process is a well established process in the Design Techniques Branch of the Electronics Development Division of the Electronics and Control Laboratory at MSFC of the National Aeronautics and Space Administration (NASA). This report contains the P-MOS process used at the present time together with a general explanation of the process. Other information helpful in processing is included. A general description of MSFC design, mask making, packaging, and testing procedures is also provided. Although this report provides a general explanation of the procedures from conceptual design to final testing necessary for the fabrication of IC, the process itself is provided in greater detail.

The general description of the process together with the illustrations included will aid those persons who are unfamiliar with processing to obtain a general concept of the work and facilities required to process one of the simplest types of IC. The general

descriptions of the other various aspects will help complete the overall picture of a complete MOS microelectronics facility.

The process itself is presented in greater detail to serve as a guide and aid to those who are attempting to establish a P-MOS process. This report may also be used to compare an existing process to one which has proven successful in the past. Included in this report are examples of useful research and development IC fabricated at MSFC which show finished P-MOS IC before packaging. These examples demonstrate a few of the numerous applications that P-MOS IC can perform. This report also contains brief descriptions of three of the major functions of the Electronics Development Division for NASA. These functions include: (1) research and development of new technology, (2) education of individuals in the various disciplines and technologies of the field of microelectronics, and (3) fabrication of many types of specially designed IC which are not commercially feasible in small quantities for many in-house research and development programs.

II. MICROELECTRONICS CAPABILITY

The Microelectronics facility of the Electronics Development Division possesses the total capability required to create an IC from conceptual design through final testing of the packaged device prior to application. The various steps involved in each of the necessary phases of creating an IC are described in general with the exception of processing. Processing is described in greater detail in later sections of this report.

A. Computer Aided Design

The design and artwork generation phase of the Large Scale Integration (LSI) Computer Aided Design (CAD) System [1] is the first phase in the creation of an IC. To design a Large Scale Integrated Circuit (LSIC), the logic necessary to perform the intended functions must be ascertained. Employing Boolean algebra, the logic requirements are organized into a logic diagram. Each of the Boolean functions can be performed electrically using a standard cell which performs a given function such as the NAND or the NOR operation. If these standard logic cells are electrically connected in a proper manner, the original logic requirements will be satisfied. From the logic diagram and the Standard Cell Notebook [2], a network interconnection list is developed and punched onto computer cards. A large batch computer program called Automatic Layout is executed using these cards as input data. A data base consisting of the layout of the microcircuit with input and output pads, power supply pad, and test devices is formed. This data base is transferred into an interactive graphics computer system [3] and the chip layout is displayed on the face of a cathode ray tube. The designer studies the design in great detail and can make modifications to the design with the graphics system. This data base can also be run as input data into logic simulator computer programs to verify that the logic meets the designer's requirements. If the logic does not, the design phase is repeated until correct.

After the design phase has been completed, the mask artwork must be generated. The automatic layout data are used as an input into an Artwork Computer Program. This program searches a library which contains all of the mask data for the cells and, with another program, organizes connection patterns and cell shapes into a data format compatible with the mask pattern generation hardware. Before these data, in the form of a magnetic computer tape, are provided to the mask generation facility, the final circuit design is carefully studied using the interactive graphics system to find any design errors. The design phase from conception to artwork generation is generally accomplished in one to three weeks.

B. Mask Making

The making of photographic masks in the mask generation facility is the second phase in the creation of an IC. In a temperature controlled clean room environment [4], the CAD magnetic tape is loaded onto a computer which transfers the circuit geometry information from the tape into exposures on a high resolution photographic glass plate by means of a pattern generator. This 5.1 by 5.1 cm (2 by 2 in.) glass plate containing a magnified (10X) copy of the circuit is then chemically developed. The quality of the circuit image is carefully inspected under a microscope since this glass plate is used as the master from which all circuit patterns on the final mask are reproduced. After inspection, the master is aligned to a metal frame and cleaned. The master is placed in a step and repeat camera system. In this system, the circuit pattern is reduced by a factor of ten before it is stepped and repeated in a precise X and Y array. The pattern is reproduced onto another 5.1 by 5.1 cm (2 by 2 in.) high resolution photographic glass plate that is chemically developed. This final copy is then carefully inspected under a microscope because this plate may be used to contact print additional masks that will be used in the processing phase. In some cases where low volume research and development circuits are to be created, the final step and repeat copies are used directly as they are produced without additional contact printing [5]. In the P-MOS process, five different masks are used to define the necessary patterns. Each of these must be made individually using the previously described process. Each mask of the set is carefully inspected under a microscope for quality before it is provided to the wafer processing facility. The mask generation phase from magnetic tape to completed set of masks is generally accomplished in 1 week.

C. Wafer Processing

The processing of the silicon wafers into integrated circuits is the third phase in the creation of an IC. The P-MOS process is provided in the next section with a general explanation of the procedures following it. Before the wafers are ready to be tested, the wafers are carefully inspected for processing defects. The wafer processing phase from blank silicon wafer to finished circuit is generally accomplished in 1 week for one processing run. Multiple runs are sometimes required to create a specific number of properly functioning circuits.

D. Testing

The testing of the finished wafers for electrical and visual quality is the fourth phase in the creation of an IC. Discrete testing is the first test performed. The wafer is held in place on a chuck by a vacuum while small moveable probes are placed on the bonding pads to make electrical connection. The discrete test circuit is used to determine threshold (turn-on) voltage (V_T), drain leakage current (I_{DSS}), drain-source breakdown voltage (BV_{DSS}), and transconductance (g_m). These tests are performed at five positions on the wafer to give an indication of the variation of the parameters across the wafer. The shift of the flatband voltage (V_{FB}) is measured using a capacitance-voltage system which traces curves before and after the wafers are subjected to elevated temperature and voltage bias. This test indicates the worst-case, long-term V_T shift that should occur. Electrical test parameters are given in the following Table.

TABLE. ELECTRICAL TEST PARAMETERS

Symbol	MIN	TYP	MAX	Units	Conditions
High V_T	-3.0	-4.0	-4.5	V	$V_{GS} = V_{DS}$
Low V_T	-1.5	-2.0	-2.5	V	$I_D = -10\ \mu A$
I_{DSS}	(a)	-2.0	-10.0	nA	$V_{DS} = -10$ V $V_{GS} = 0$
BV_{DSS}	-30	-35	(b)	V	$I_D = -10\ \mu A$ $V_{GS} = 0$
g_m(c)	3000	3500	(b)	μmhos	$V_{GS} = V_{DS} = -10$ V
ΔV_{FB}	(a)	-0.2	-0.5	V	Bias = +10 V 573°K (300°C) 300 s (5 min)

a. Value approaches zero.
b. No upper limit on specification.
c. Width/length ratio assumed to be five.

If the discrete devices meet the required specifications, dynamic testing is performed. An algorithm generator and an automated wafer prober are used to measure circuit behavior under simulated operating conditions. This test involves simulating input signals and observing output waveforms on each circuit. All input combinations are simulated, if possible. The properly functioning circuits are isolated from the defective circuits by the automated wafer prober using an inking technique which marks the defective circuits. The wafer is then scribed with a diamond tipped scribe and rolled to separate the circuits into individual chips. The properly functioning chips are then individually cleaned and visually inspected to remove those chips which would have the highest possibility of failure. The testing phase from discrete testing to visual inspection is generally accomplished in 1 week for one processing run.

E. Packaging

The packaging [6] of the functional chips into individual packages is the fifth phase in the creation of an IC. Together with electrical contacts, packaging provides physical and environmental protection to the circuit. A suitable package for the device's application, such as flatpacks, "TO" cans, or dual-in-lines, is chosen for mounting the chip. The chip is attached inside the package by a eutectic or epoxy bonding material. Electrical connections are then made from aluminum bonding pads on the chip to the package's interior leads with small diameter (0.018 to 0.025 mm) gold or aluminum wire. These interconnects are made by either a thermocompression or an ultrasonic wire bonding process. A cover is placed on the package and hermetically sealed. An inert gas, such as nitrogen, is placed inside the package prior to sealing. The time required for the packaging operation varies according to the complexity of the chip, number of wires, and other factors. However, an estimate of 0.25 to 1.0 hour per packaged device is typical for low volume, specially designed LSIC.

F. Final Testing

The final testing of the IC is the sixth and final phase in the creation of the IC prior to application. The IC are dynamically tested again using a different electrical connection applicable to the package to eliminate failures due to packaging. The final testing phase is generally accomplished in 1 day for one processing run. The IC are now ready for application.

III. EXAMPLES OF APPLICATIONS

Many types of P-MOS IC have been produced at MSFC which range in size and complexity. Three categories established to indicate these two factors are small, medium, and large scale integration (designated respectively SSI, MSI, LSI). SSI is defined to be an IC containing less than 250 devices per chip with MSI containing from 250 to 500 and LSI containing more than 500.

A. Hybrid Operational Digital Attenuator Device

An example of an SSIC is the Hybrid Operational Digital Attenuator Device (HODAD). HODAD is a four channel, common-source transmission gate (TG) circuit with data latch and enable as shown in Figure 1 of one of the four channels. Since the circuit contains 44 devices plus test devices and a capacitor, it was digitized from a layout sketch with the assistance of the Mask and Pattern Program using generous dimensions for layout and interconnection. In a computer, this circuit, shown in Figure 2, functions as a switching mechanism for a digital-to-analog converter.

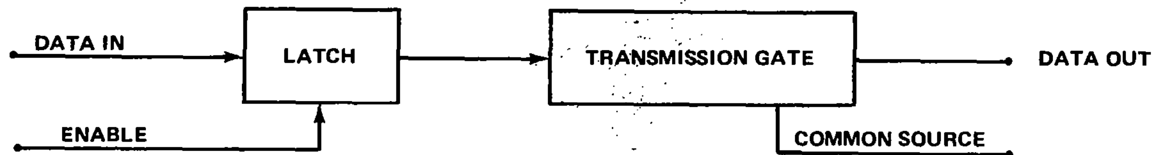

Figure 1. Hybrid operational digital attenuator device functional block diagram.

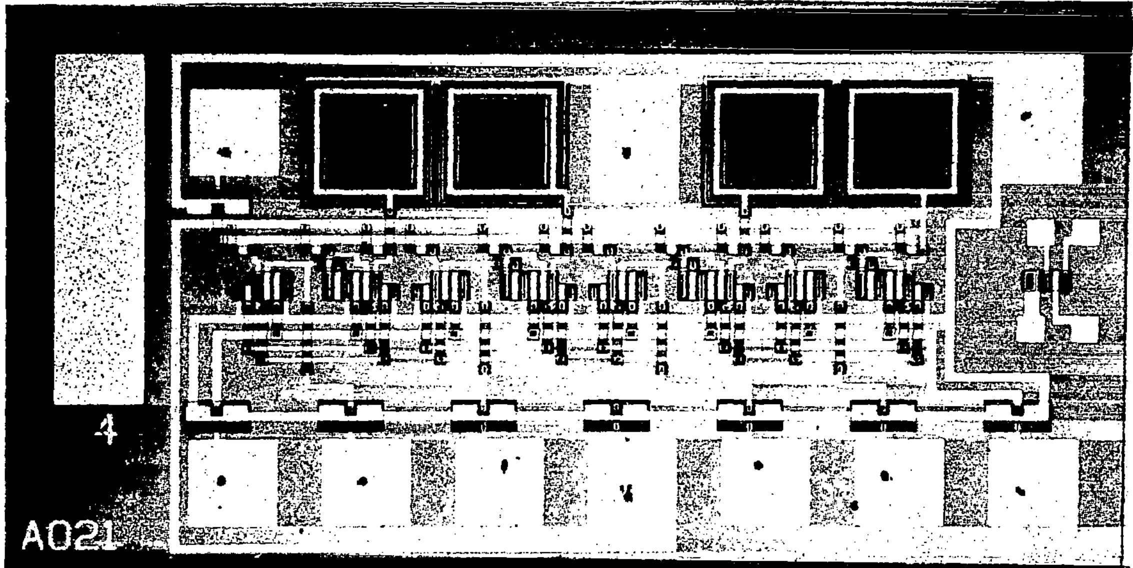

Figure 2. Hybrid operational digital attenuator device chip (40X).

B. Stepped Sine Wave Generator

An example of an MSIC is the stepped sine wave generator which contains approximately 500 devices plus discrete test devices. This device is a digital, stepped, 400 Hz, sine wave generator when supplied with the proper clock frequency. It sequentially turns on one of 24 TG (Fig. 3) to which discrete voltages have been applied to form the steps of a sine wave (or any other desired wave form). This device which contains the logic to divide the clock frequency also has provisions to synchronize one of two other stepped sine wave generator chips or to be synchronized by one of them to form 3 phase

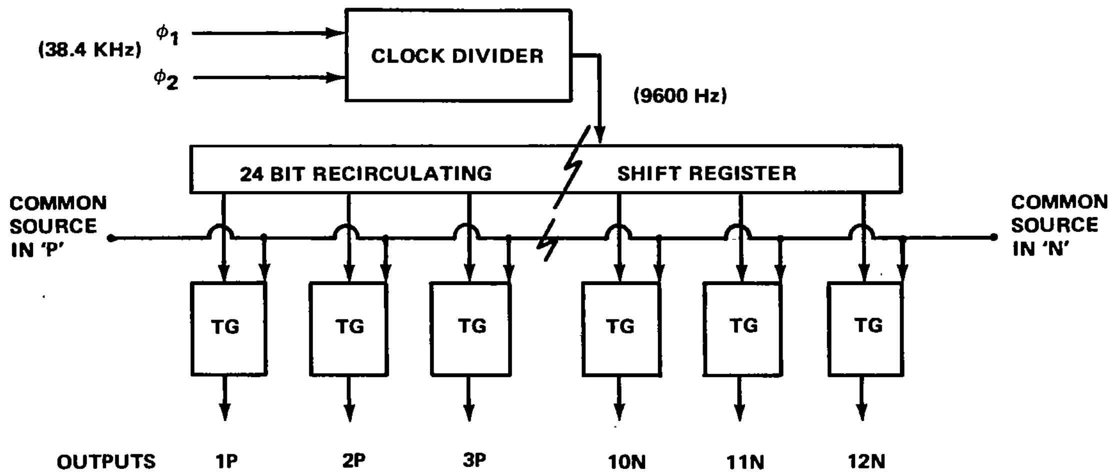

Figure 3. Stepped sine wave generator functional block diagram.

(ϕ) signals 120° apart, using only three chips. This circuit, shown in Figure 4, was produced by the MSFC CAD system using "MSFC standard cell" logic elements and automated layout.

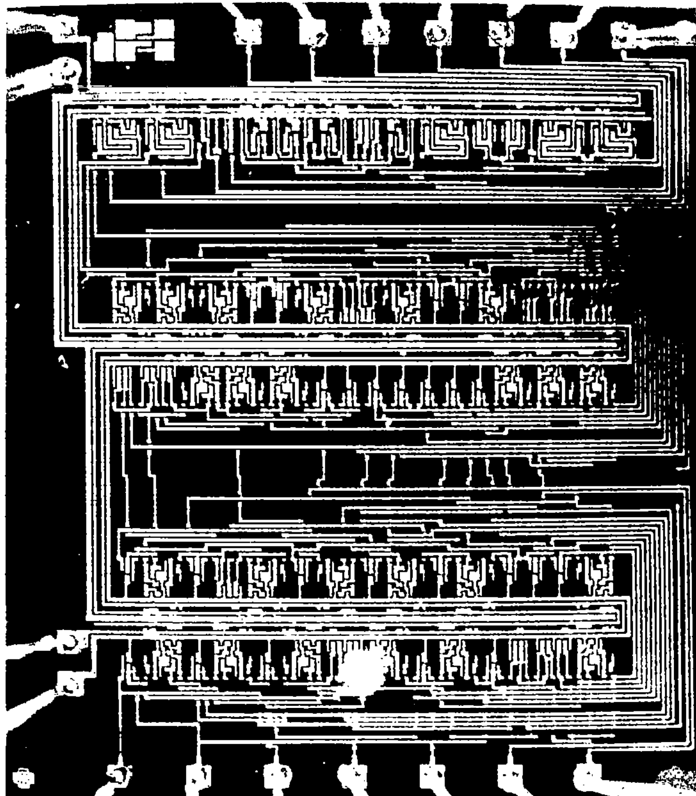

Figure 4. Stepped sine wave generator chip (25X).

C. Delay Line Time Compressor

An example of an LSIC is the Delay Line Time Compressor (Deltic) containing approximately 1250 devices plus discrete test devices. Deltic is a 200 bit shift register with a recirculating output (for correlation) at bit 199. Data may be held by recirculating 200 bits or correlated by recirculating 199 bits as shown in Figure 5. Additional logic enables chips to be serialized to increase effective shift register length. Shown in Figure 6, Deltic, also a product of CAD, is the major component in a system which is used to detect data within a noisy signal by means of correlation.

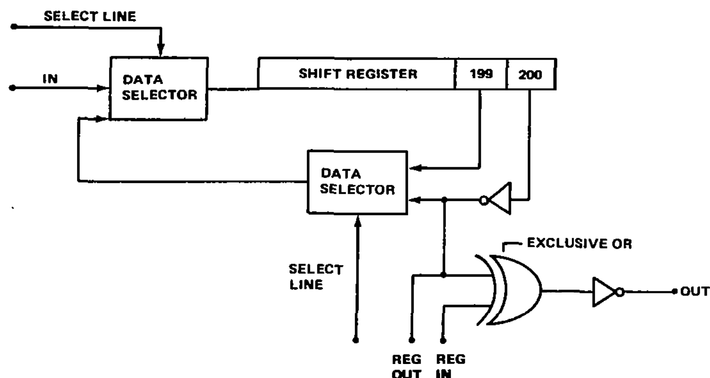

Figure 5. Delay line time compressor functional block diagram.

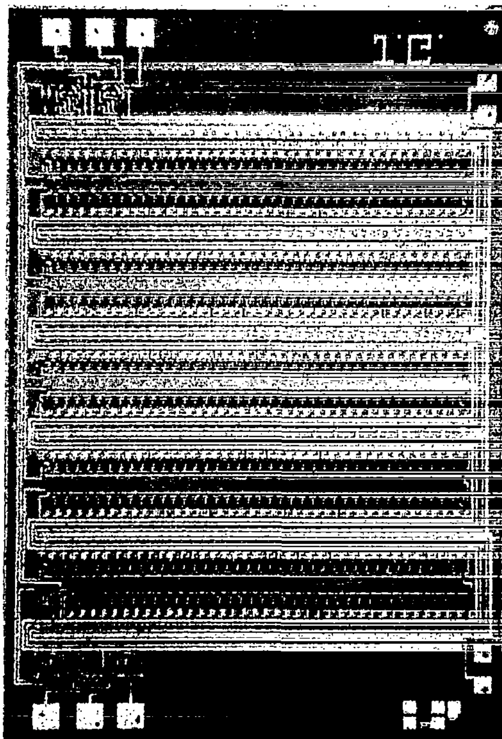

Figure 6. Delay line time compressor chip (25X).

Many other P-MOS IC have been fabricated at MSFC [7] using the facilities and capabilities described within this report. Other MOS processes have been established and are used in maintaining the state-of-the-art capabilities required by NASA.

IV. P-MOS PROCESS

The P-MOS process as it is currently applied at MSFC is described in sufficient detail to produce P-MOS IC in an adequately furnished IC laboratory. Explanations of the processing steps are covered in the next section of this report. Two variations of the process which result in a broader functional range of the V_T parameter are provided. The process is given for the higher V_T variation with the required changes indicated in brackets for the lower V_T variation. For the higher V_T variation, silicon wafers of (111) orientation are used while silicon wafers of (100) orientation are used for the low V_T variation. Both types of wafers required are phosphorus doped N-type to a resistivity of 3 to 5 ohm-cm.

All specific data given in this process are typical averages obtained in the processing facility at MSFC and, therefore, are not intended to be taken as exact values. Alternate methods for almost every phase of the process are available at MSFC providing countless variations in the P-MOS process. These variations serve as back-ups in the event a problem arises in an area. The variation given in this report has proven to be very successful.

The formulas for chemical solutions used in the process are provided in Appendix A if not provided in the text. Curves for silicon dioxide (SiO_2) growth rates are provided in Appendix B with a curve for Boron Nitride (BN) diffusions provided in Appendix C. Appendix D provides information on oxide etch rates using solutions described in Appendix A. Discrete P-MOS transistor device configurations are included to demonstrate main processing steps. The drawings in the photolithographic steps indicate that negative PR is being used. The same drawings are applicable for positive PR if the masks are reversed (the areas where light is allowed to pass are switched with the areas where it is not). The times which are primarily dependent upon the operator or the number of wafers being processed are omitted.

A. Field Oxide

1. Initial Clean

   a. Rinse in water (H_2O) — 300 s (5 min)

   b. Ultrasonic clean in acetone (ACE) — 10 s

c.	Ultrasonic clean in trichloroethylene (TCE)	300 s (5 min)
d.	Ultrasonic clean in ACE	300 s (5 min)
e.	Rinse in H_2O	600 s (10 min)
f.	Sulfuric acid-nitric acid (SN) solution 388 ± 5°K (115 ± 5°C)	600 s (10 min)
g.	Rinse in H_2O	600 s (10 min)
h.	Blow dry with nitrogen gas (N_2)	

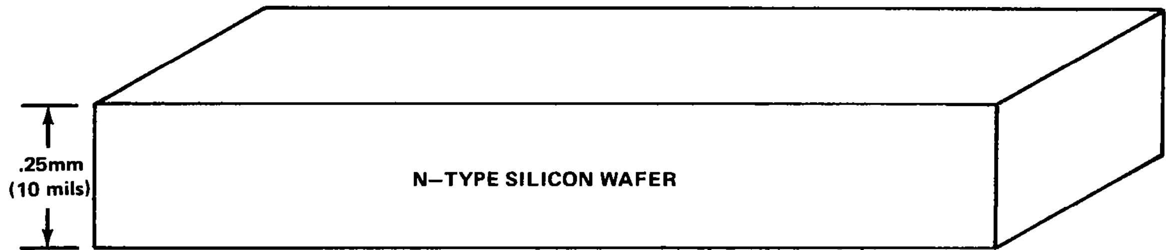

Figure 7. Silicon wafer after initial clean.

2. Field Oxidation 1500 nm [800 nm] 1423°K (1150°C)

a.	Oxygen gas (O_2)	28 cm^3/s	900 s (15 min)
b.	O_2 + steam (370 ± 2°K)(97 ± 2°C)	5 cm^3/s	12000 s (200 min) [3600 s (60 min)]
c.	O_2	28 cm^3/s	900 s (15 min)
d.	N_2	31 cm^3/s	900 s (15 min)

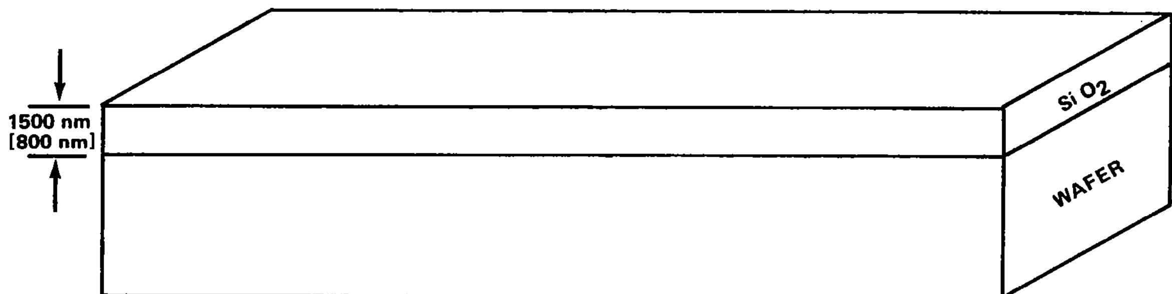

Figure 8. Field oxidation.

B. Boron P^+ Diffusion

1. PR with Mask 1

   a. Apply PR

   b. Spin at 100 rps — 15 s

   c. Prebake in N_2 at 343°K (70°C) — 1200 s (20 min)

   d. Align Mask 1

   e. Expose with ultraviolet (UV) light — 3 s

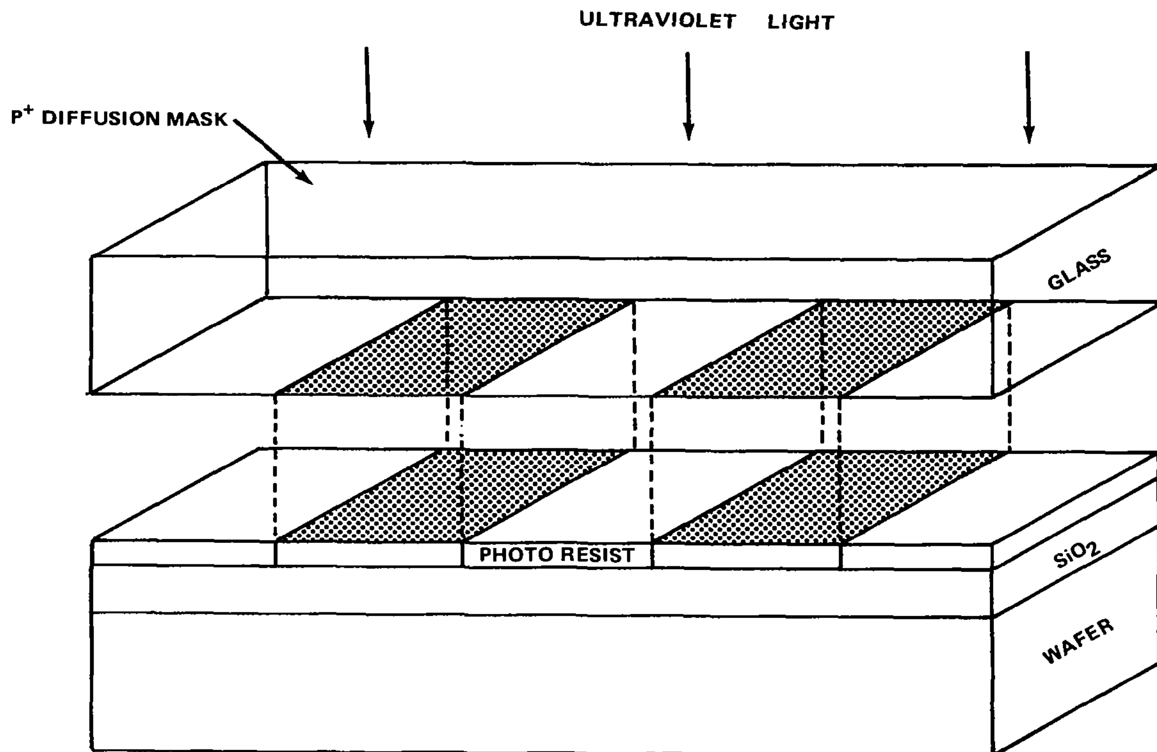

Figure 9. P^+ diffusion mask alignment and exposure.

   f. Develop with PR developing solution — 30 s

   g. Rinse with PR rinsing solution — 30 s

   h. Blow dry with N_2

   i. Postbake in N_2 at 413°K (140°C) — 1800 s (30 min)

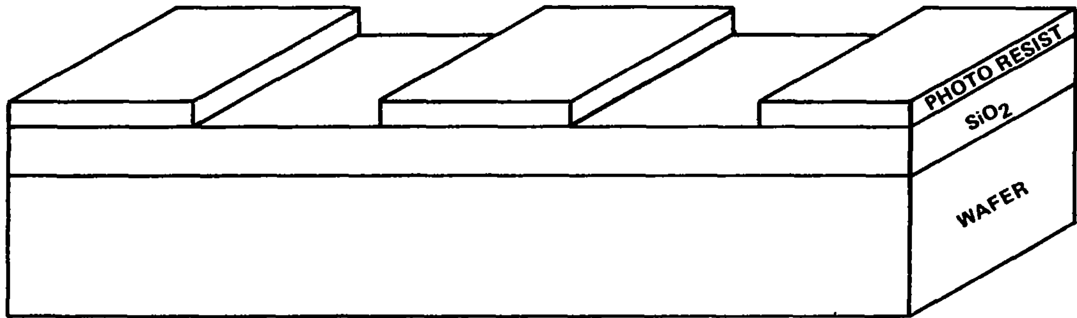

Figure 10. Patterned photoresist.

2. Boron P^+ Diffusion Etch

   a. Etch in buffered oxide etchant at 323°K (50°C) 185 s (100 s)

   b. Rinse in H_2O 600 s (10 min)

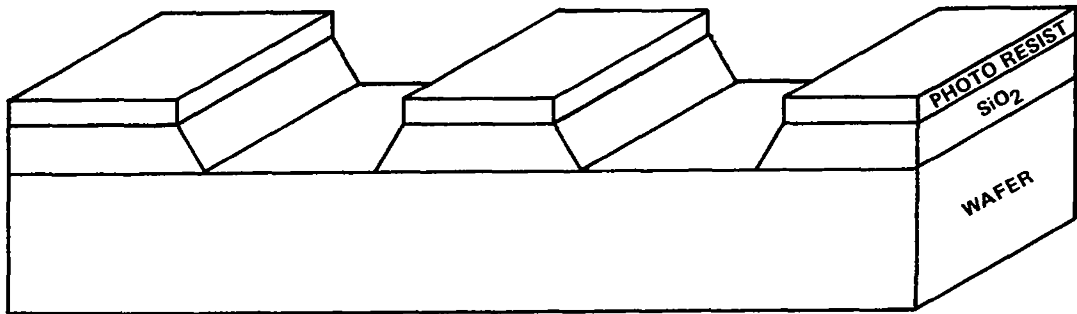

Figure 11. P^+ diffusion etch.

3. PR Removal

   a. SN solution at 388 ± 5°K (115 ± 5°C) 600 s (10 min)

   b. Rinse in H_2O 600 s (10 min)

   c. Etch in hydroflouric acid (HF) solution at 298 ± 5°K (25 ± 5°C) 5 s

   d. Rinse in H_2O 600 s (10 min)

   e. Blow dry with N_2

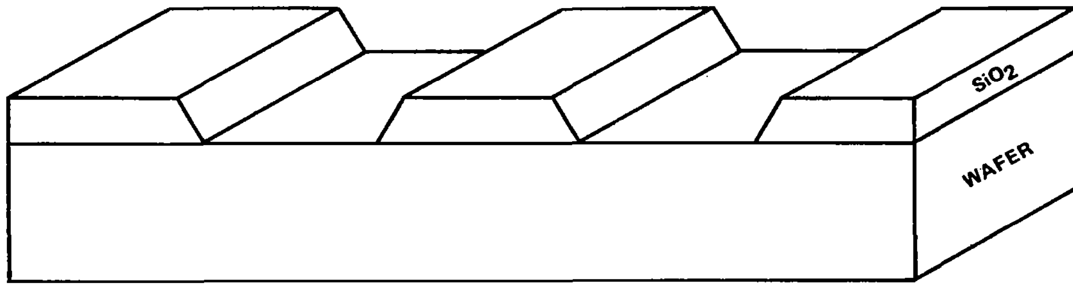

Figure 12. Photoresist removal.

4. Boron P^+ Diffusion 1053°K (980°C)

   a. N_2 (wafers adjacent to boron nitride (BN) wafers) 31 cm^3/s 2400 s (40 min)

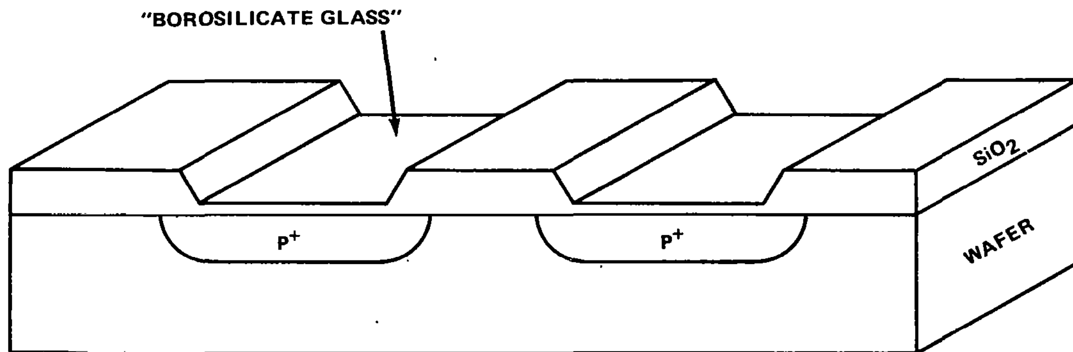

Figure 13. Boron P^+ diffusion.

5. Borosilicate Glass Removal

   a. Etch in buffered oxide etchant at 298 ± 5°K (25 ± 5°C) 60 s (1 min)

   b. Rinse in H_2O 300 s (5 min)

   c. Etch in Jacobson's etchant at 368 ± 1°K (95 ± 1°C) 3600 s (60 min)

   d. Rinse in H_2O 600 s (10 min)

   e. Etch in buffered oxide etchant at 298 ± 5°K (25 ± 5°C) 30 s

f. Rinse in H_2O 600 s (10 min)

g. Blow dry with N_2

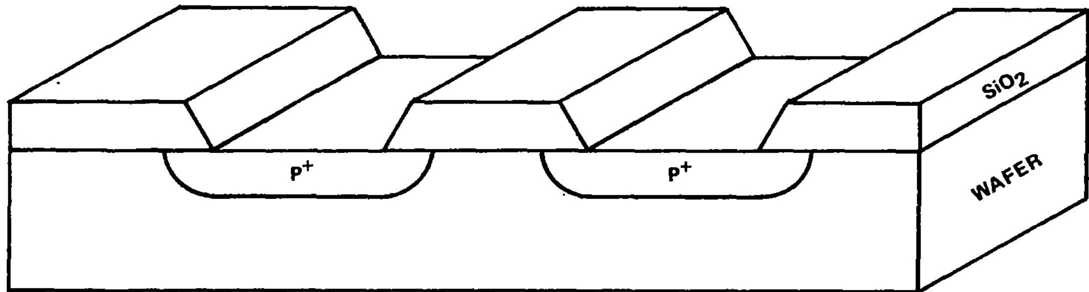

Figure 14. Borosilicate glass removal.

6. Second Oxide 33 nm 1423°K (1150°C)

a. O_2	28 cm³/s	600 s (10 min) [900 s (15 min)]
b. N_2	31 cm³/s	300 s (5 min)

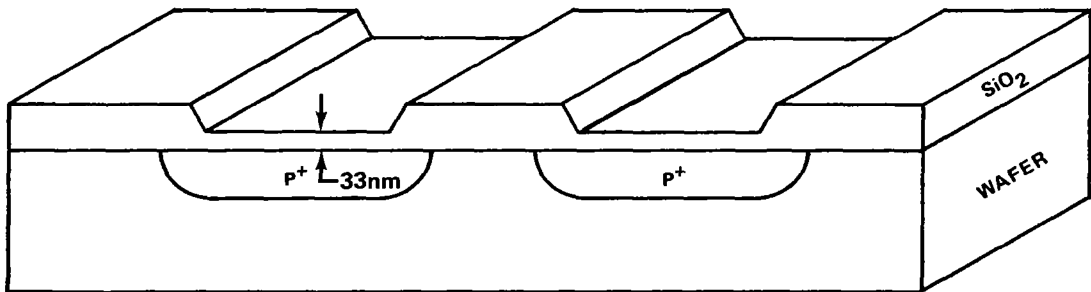

Figure 15. Second oxidation.

C. Gate Oxide

1. PR with Mask 2

a. Apply PR

b. Spin at 100 rps 15 s

c. Prebake in N_2 at 343°K (70°C) 1200 s (20 min)

d. Align Mask 2

e. Expose with UV light 3 s

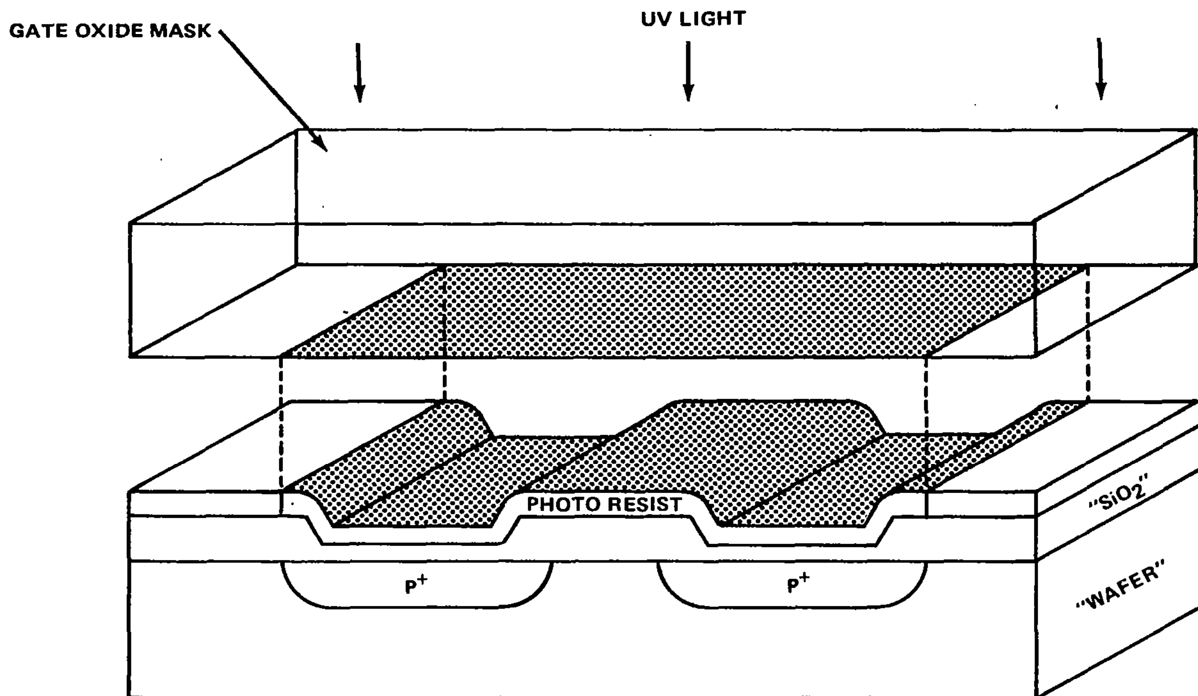

Figure 16. Gate oxidation photoresist.

f. Develop with PR developing solution 30 s

g. Rinse with PR rinsing solution 30 s

h. Blow dry with N_2

i. Postbake in N_2 at 413°K (140°C) 1800 s (30 min)

2. Gate Etch

a. Etch in buffered oxide etchant at 323°K (50°C) 185 s [100 s]

b. Rinse in H_2O 600 s(10 min)

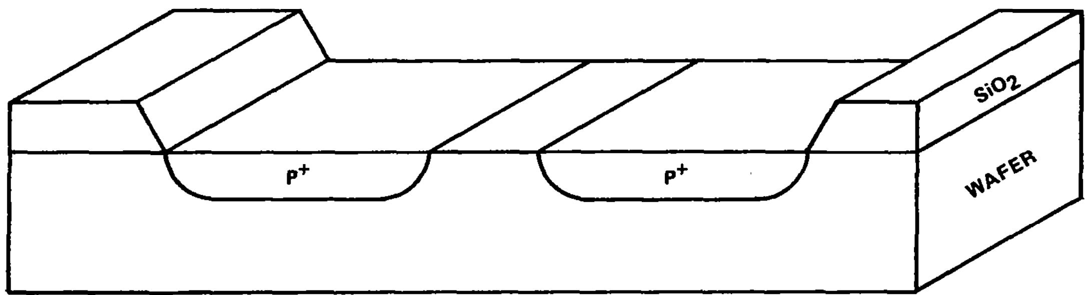

Figure 17. Gate etch.

3. PR Removal

a. SN solution at 388 ± 5°K (115 ± 5°C)	600 s (10 min)
b. Rinse in H_2O	600 s (10 min)
c. Etch in HF solution at 298 ± 5°K (25 ± 5°C)	5 s
d. Rinse in H_2O	600 s (10 min)
e. Blow dry with N_2	

4. Pre-Gate Clean

a. Nitric acid (HNO_3) at 358 ± 2°K (85 ± 2°C)	600 s (10 min)
b. Rinse in H_2O	600 s (10 min)
c. Blow dry with N_2	

5. Gate Oxidation 115 nm	1423°K (1150°C)	
a. O_2	28 cm^3/s	2100 s (35 min) [3000 s (50 min)]
b. N_2	31 cm^3/s	900 s (15 min)

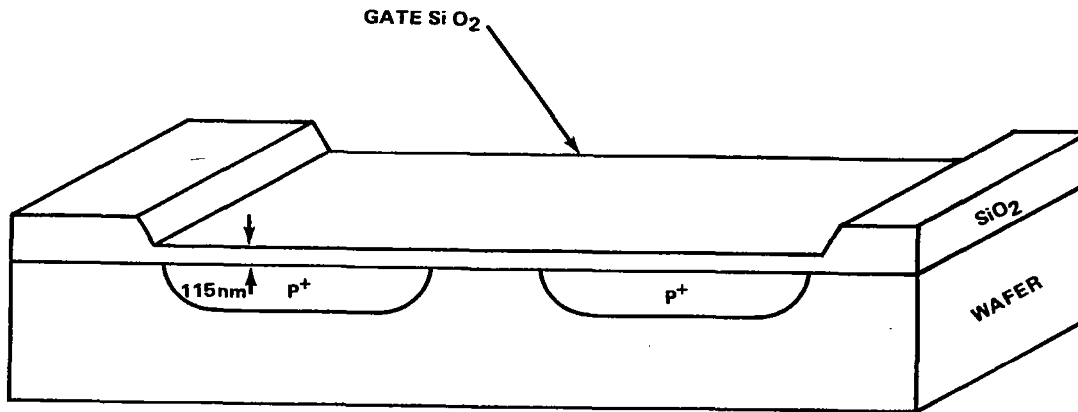

Figure 18. Gate oxidation.

D. Metal Contacts

1. PR with Mask 3

a. Apply PR	
b. Spin at 100 rps	15 s
c. Prebake in N_2 at 343°K (70°C)	1200 s (20 min)
d. Align Mask 3	
e. Expose with UV light	3 s

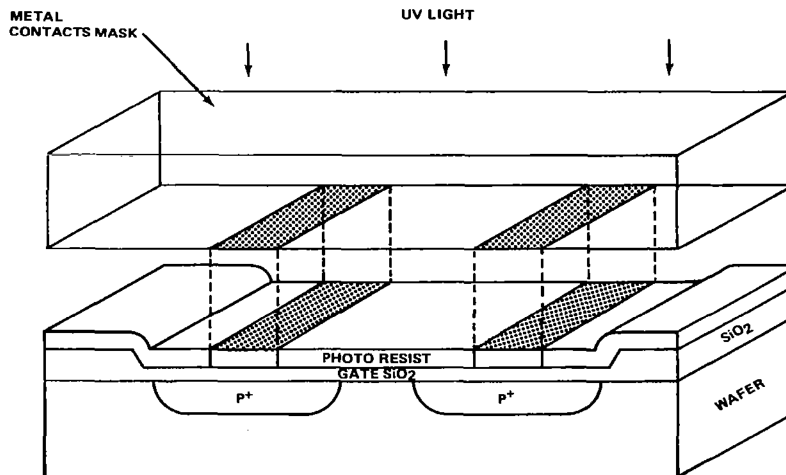

Figure 19. Metal contacts photoresist.

f. Develop with PR developing solution — 30 s

g. Rinse with PR rinsing solution — 30 s

h. Blow dry with N_2

i. Postbake in N_2 at 413°K (140°C) — 1800 s (30 min)

2. Metal Contacts Etch

a. Etch in buffered oxide etchant at 298 ± 5°K (25 ± 5°C) — 60 s (1 min)

b. Rinse in H_2O — 600 s (10 min)

3. PR Removal

a. SN solution at 388 ± 5°K (115 ± 5°C) — 600 s (10 min)

b. Rinse in H_2O — 600 s (10 min)

c. Etch in HF solution at 298 ± 5°K (25 ± 5°C) — 5 s

d. Rinse in H_2O — 600 s (10 min)

e. Blow dry with N_2

4. Gate Thickness Definition Etch

a. Etch in HF solution at 298 ± 5°K (25 ± 5°C) — 25 s

b. Rinse in H_2O — 600 s (10 min)

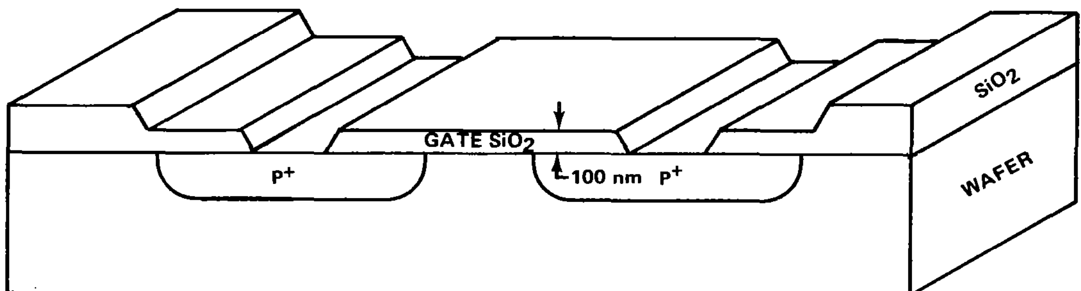

Figure 20. Metal contacts etch and gate thickness definition.

E. Metallization

1. Pre-Aluminum Clean

   a. Ultrasonic clean in ACE — 300 s (5 min)

   b. Rinse in H_2O — 600 s (10 min)

   c. Blow dry with N_2

2. Aluminum Deposition 1000 nm Ar at 5 μm of Mercury

   a. Sputter aluminum — 1800 s (30 min)

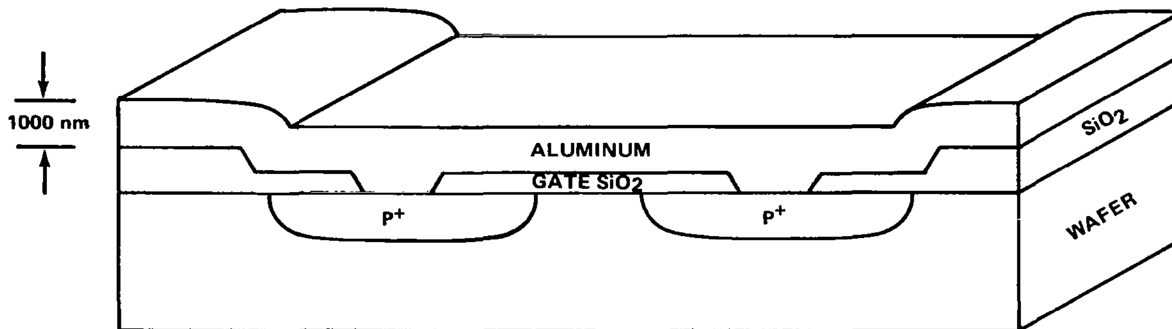

Figure 21. Aluminum deposition.

3. PR with Mask 4

   a. Apply PR

   b. Spin at 100 rps — 15 s

   c. Prebake in N_2 at 343°K (70°C) — 1200 s (20 min)

   d. Align Mask 4

   e. Expose with UV light — 3 s

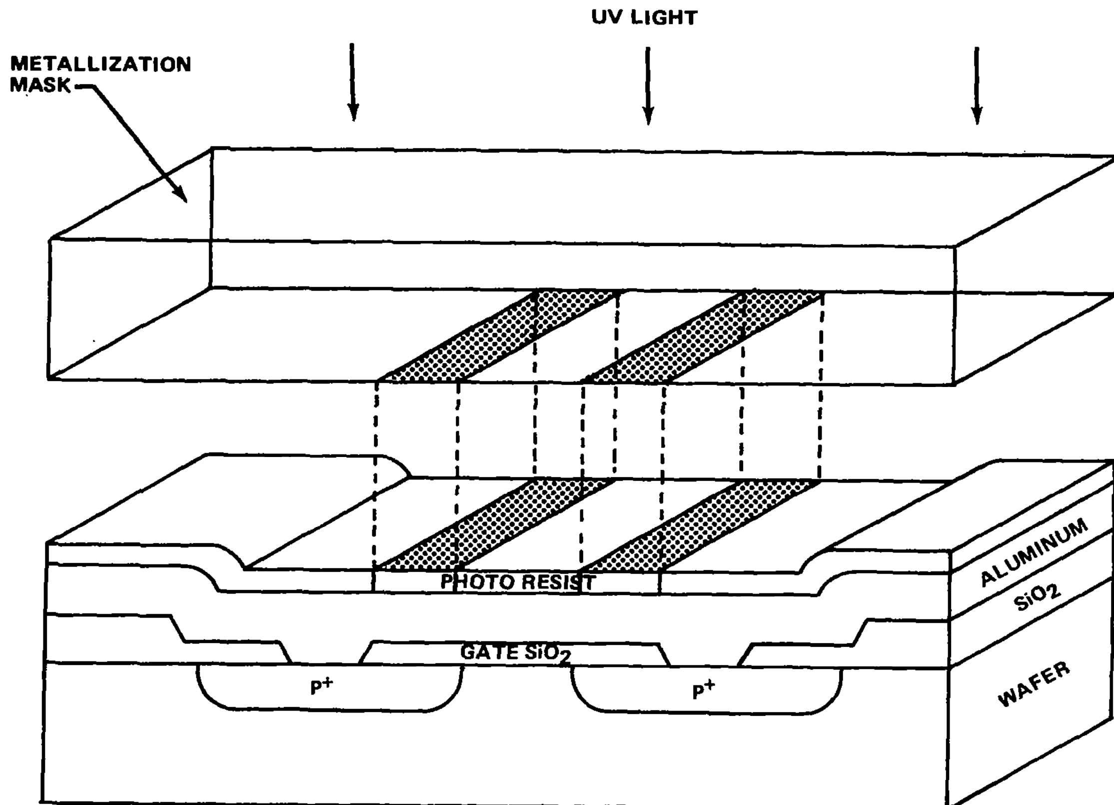

Figure 22. Metallization photoresist.

f. Develop with PR developing solution — 30 s

g. Rinse with PR rinsing solution — 30 s

h. Blow dry with N_2

i. Post-bake in N_2 at 413°K (140°C) — 1800 s (30 min)

4. Aluminum Etch

a. Etch in aluminum etchant at 323°K (50°C) — 120 s (2 min)

b. Rinse in H_2O — 600 s (10 min)

5. PR Removal

a. Aluminum-compatible PR remover at 298 ± 5°K (25 ± 5°C) — 1800 s (30 min)

b. Rinse in H_2O — 600 s (10 min)

6. Pre-Sinter Clean

   a. Ultrasonic clean in ACE — 300 s (5 min)

   b. Rinse in H_2O — 600 s (10 min)

   c. Blow dry with N_2

7. Sinter — 743°K (470°C)

   a. N_2 — 31 cm^3/s — 1200 s (20 min)

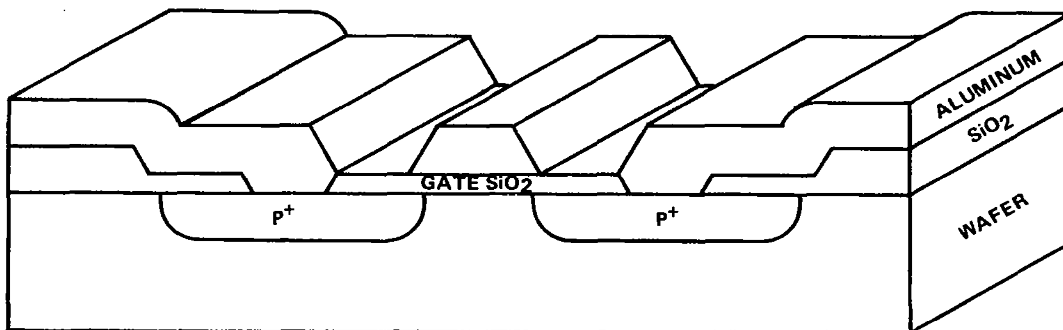

Figure 23. Aluminum definition and sinter.

F. Passivation

1. Pre-Passivation Clean

   a. Ultrasonic clean in ACE — 300 s (5 min)

   b. Rinse in H_2O — 600 s (10 min)

   c. Blow dry with N_2

2. Passivation — 800 nm — 673°K (400°C)

   a. O_2 — 3.5 cm^3/s

      SiH_4 — 3 cm^3/s — 1920 s (32 min)

3. PR with Mask 5

   a. Apply PR

   b. Spin at 100 rps — 15 s

c. Prebake in N_2 at 343°K (70°C) 1200 s (20 min)

d. Align Mask 5

e. Expose with UV light 3 s

f. Develop with PR developing solution 30 s

g. Rinse with PR rinsing solution 30 s

h. Blow dry with N_2

i. Postbake in N_2 at 413°K (140°C) 1800 s (30 min)

4. Passivation Etch

a. Etch in passivation etchant

b. Rinse in H_2O 600 s (10 min)

5. PR Removal

a. Aluminum-compatible PR remover at 298 ± 5°K (25 ± 5°C) 1800 s (30 min)

b. Rinse in H_2O 600 s (10 min)

6. Final Clean

a. Ultrasonic clean in ACE 300 s (5 min)

b. Rinse in H_2O 600 s (10 min)

c. Blow dry with N_2

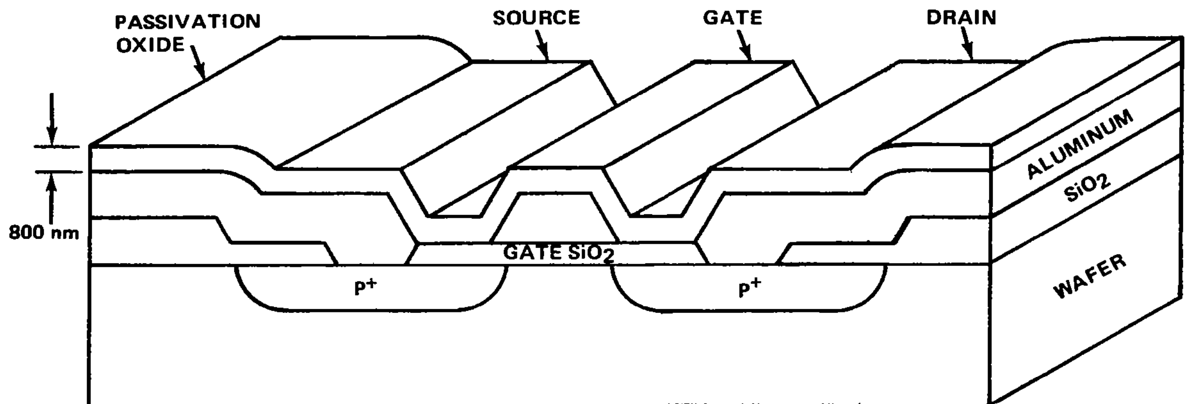

Figure 24. Passivated completed device.

V. EXPLANATION OF P-MOS PROCESS

The P-MOS process is explained in general detail to provide a general conception of the work required to create P-MOS IC. A brief description of the facility requirements is provided. The two ambients, room environment and water, to which the wafer is primarily exposed during processing are critical to the electrical parameters and processing yields of P-MOS IC.

A. Water

The water used in the processing of P-MOS IC is required to be extremely free of contaminants and to exhibit an extremely high resistivity. The production of the water for use in all processing steps at MSFC begins with a high pressure steam source. Steam from this source is sent through a heat exchanger to condense the steam into water which has approximately 3 parts per million (ppm) total dissolved solids (tds) content. The water then passes through a 3 μm filter and enters a two-bed (cation-anion) demineralizer where the water leaving has approximately 1/2 ppm tds and 3 Mohm resistivity. A mix-bed (cation-anion) deionizer is then used to obtain water with approximately 1/4 ppm tds and 18 Mohm resistivity. Filtered through a 1 μm filter, the water enters another mix-bed deionizer which supplies water to the processing laboratory with an extremely low particulate count and an extremely high resistivity.

B. Cleanroom

Processing of P-MOS IC must be performed in a cleanroom environment [8]. In a cleanroom, the internal air pressure is positive with respect to the exterior air pressure so that air leaks in the facility will not contaminate the interior. The air is completely exchanged every 2 min with clean filtered air. The temperature is controlled to be approximately 294°K (21°C) with the humidity controlled to be approximately 45 percent.

C. Wafers

The silicon wafers used in this P-MOS process are typically 38 mm (1.5 in.) in diameter and from 0.18 to 0.25 mm (7 to 10 mils) thick. One side of the wafer is mechanically and chemically polished while the other side is chemically etched to relieve stresses. The bulk material for the higher V_T process is (111) orientation single crystal silicon while the bulk material for the lower V_T process is (100) orientation single crystal silicon. Each wafer has a (110) orientation flat to which the IC patterns are aligned parallel and perpendicular to the crystal planes. This alignment later allows the IC to be

separated accurately. The wafers are doped with phosphorus ions N-type to a concentration of approximately 1×10^{15} atoms/cm^3 having a resistivity between 3 and 5 ohm-cm. Wafers to the previously given specifications may be ordered from silicon wafer manufacturers.

D. Field Oxide

The first procedure is to clean the initial wafers and prepare them for the thick field oxide to be grown. The wafers are placed in a carrier called a "wafer holder" capable of holding several wafers as they are processed in different solutions described in Appendix A. They are then rinsed in overflowing cascade water baths to remove most of the loose particles which may have adhered to their surfaces. The wafers are then placed in an ultrasonic bath of acetone to remove the water and dissolve any organic contaminants such as grease or oil from the surfaces. Acetone, which is soluble in water and trichloroethylene, functions as a buffer for the ultrasonic bath of trichloroethylene which is not soluble in water. Trichloroethylene also dissolves organic contaminants. The wafers are placed back into an acetone bath before being rinsed again. After a short period of time or after the water regains its initial purity, the wafers are placed into a heated bath of sulfuric and nitric acids which react with the inorganic contaminants to dissolve them away from the surface. The wafers are again rinsed in water to remove the acid and contaminants, then blown dry with filtered dry nitrogen gas.

The wafers are now prepared for oxidation by loading them into a quartz carrier called a "boat" and placing them into a quartz tube in an accurately controlled, high temperature cylindrical furnace. Accurately controlled flows of high purity gases from liquid or gas sources are injected into the furnace tube. Oxygen reacts with the silicon to produce a silicon dioxide layer of glass on the surfaces of the wafers. The oxygen atoms diffuse through the existing oxide layer to the silicon-silicon dioxide interface where the oxidation occurs. Steam is used to increase the rate at which the reaction occurs. Curves for growth rate of silicon dioxide on silicon according to orientation, temperature, and ambient are provided in Appendix B. The steam is produced by bubbling oxygen through temperature-controlled water. Dry oxygen is again used alone to produce a high quality silicon dioxide layer at the interface between the silicon dioxide and the silicon. Nitrogen is used at the end of the oxidation sequence to anneal the silicon dioxide by allowing the uncombined atoms of oxygen trapped in the silicon dioxide to react with the remaining silicon. The field oxide is used during processing to define the diffusion areas and after completion of the IC prevents the formation of parasitic transistors.

E. Boron P^+ Diffusion

The wafers, immediately from the furnace, are placed on a rapid acceleration spinner where they are held on a chuck by a vacuum. Photoresist, a light sensitive liquid plastic polymer, is applied to the surface of the wafer from a dropper bottle. The wafer is rapidly accelerated creating a thin coating of uniform thickness while the excess is

removed by centrifugal force. The coated wafers are then prebaked in a forced nitrogen oven to remove excess solvents and promote adhesion. Using mask 1 which has opaque and clear patterns, a mask aligner is used to align the mask to the wafer within a 1/2 μm tolerance. The mask aligner is equipped with a split-field microscope which enables the operator to view both sides, left and right, of the wafer simultaneously during alignment. The wafers are then exposed through the mask with high intensity ultraviolet light source which transfers the image on the mask to the photoresist. This photographic process is commonly termed, in the microelectronics industry, photolithography.

The exposed photoresist patterns are then developed using an appropriate developing solution and rinsed using an appropriate rinsing solution. The unwanted photoresist is washed away leaving the remainder to protect the oxide while etching to define the necessary pattern. The wafers are then postbaked to remove most of the remaining solvents, to harden, and to ensure adhesion of the photoresist to the wafer surface. The wafers are now prepared so that cutouts may be etched for the boron P^+ diffusions. The wafers are placed into a carefully controlled heated bath of buffered oxide etchant which etches away the unprotected silicon dioxide but does not rapidly attack the silicon underneath. This heating of the etch causes "controlled uncutting" creating smooth slopes in the oxide in which aluminum crosses without breakage. The angle of slope is dependent upon the etch rate as described in Appendix D. The wafers are again rinsed in water to remove excess etching solution remaining on the surface. Since the photoresist is no longer needed, it is removed in the SN solution used to clean the wafers. This solution is rinsed away with water before a short etch in the HF solution is performed. Again the wafers are rinsed in water and blown dry with nitrogen.

The boron nitride diffusion boat has slots in which the silicon wafers are placed a fixed distance from the surface of the boron nitride wafers. The boat is placed into a high temperature furnace where the boron nitride wafers act as a source of boron ions which diffuse into the unprotected silicon windows. A curve for the diffusion of boron nitride is provided in Appendix C. Nitrogen is used as the ambient gas to prevent the growth of an excess amount of oxide on the silicon which will prevent the diffusion. Some borosilicate glass is grown, however, from the oxidized boron nitride wafers and must be completely removed. The buffered oxide etchant will remove most, but not all, of this oxide. Jacobson's etchant is used to soften this very thin, heavily boron doped glass so that it can be etched away by the buffered oxide etchant. A second oxide is now grown to promote the adhesion of the photoresist in the next step.

F. Gate Oxide

The photolithographic process is repeated using mask 2 to define the areas where the gate oxide is to be grown. Mask 2 is aligned to the pattern on the wafer from the first photolithographic and etching procedure. After the wafers are etched, the photoresist is removed by the procedure previously given omitting the drying step and

proceeding into the pre-gate clean. The wafers are cleaned in hot nitric acid which grows a thin protective oxide layer over the gate area. They are rinsed, blown dry, and placed into a high temperature furnace where the gate oxide is grown. An excess amount (10 to 15 percent) of gate oxide is grown which will be removed later. This excess is grown because most of the mobile ion contamination is in the top of the oxide which will be removed when the gate oxide thickness is defined.

G. Metal Contacts

The photolithographic process is repeated using mask 3 to define the areas in which the metal will make contact to the boron P^+ diffusions. Mask 3 is aligned to the pattern on the wafer. After the wafers are etched, the photoresist is removed by the procedure previously given but omitting the drying step and proceeding into the gate thickness definition etch. The wafers are etched to obtain a final gate oxide thickness between 100 and 105 nm.

H. Metallization

The wafers are cleaned immediately before deposition of aluminum which will become the metal lines and bonding pads to interconnect the circuit. A direct current, low power, hollow cathode sputtering system is used to deposit aluminum. The wafers are placed on a rotating platform and the system is placed under a vacuum of 0.005 μm of Mercury. The pressure is then raised to 5 μm of Mercury by a controlled leak of argon gas. After shuttering the aluminum from the wafers for 2 min, aluminum is sputtered onto the wafers for 20 min. Immediately after removal from the aluminum system, the wafers go through the photolithographic process again using mask 4 which is aligned to the pattern on the wafer. The wafers are then etched in aluminum etchant to define the metal interconnect lines in the circuits. After a water rinse, the photoresist is removed in a bath of aluminum-compatible photoresist remover which does not rapidly attack the aluminum. After a water rinse and cleaning procedure, the aluminum is sintered to the silicon wafer in a high temperature furnace in a nitrogen ambient to prevent the growth of aluminum oxide. The sintering procedure alloys the aluminum to the silicon thereby reducing the series resistance between them.

I. Passivation

The wafers are cleaned immediately before passivation in an ultrasonic bath of acetone. They are then rinsed, dried, and loaded into a chemical vapor deposition system. The temperature is raised and allowed to stabilize. Oxygen and silane (four percent silane in argon) are injected into the system simultaneously. Silicon dioxide is deposited onto the surface of the wafer. The system is allowed to cool and the wafers are removed. The wafers are immediately coated with photoresist and go through the photolithographic

process using mask 5 which is aligned to the pattern on the wafer. A proprietary passivation etch which does not adversely affect the surface of the aluminum is used to etch the silicon dioxide from the bonding pads. This etch prevents the difficulty in bonding encountered when other oxide etches are used. The photoresist is removed using the aluminum-compatible photoresist remover before the wafers are given a final clean. The wafers are now ready to begin the testing phase.

VI. CONCLUDING REMARKS

A. P-MOS Process

The P-MOS process described in this report has been used successfully at MSFC to produce IC that have been functioning consistently in active systems for years while exhibiting a low failure rate. Since this P-MOS process has been proven successful at MSFC, it can therefore be utilized by industry, universities, other NASA centers, and other agencies of the government in the production of P-MOS IC. The process is given in detail to aid in its utilization, while the explanation is given to aid those people unfamiliar with IC processing toward a general understanding of how and why certain steps are performed. A detailed explanation of all phases of processing is not within the scope of this report since many books and papers have been written on these subjects.

B. MSFC Facility

The brief description of the IC facility at MSFC, given to demonstrate an overall view of the requirements of IC production, shows the capabilities in microelectronics which MSFC has in-house. This facility has the capability of producing many types of IC other than P-MOS while serving three important functions for NASA.

1. Research and Development. Much research and development work is performed in the Electronics Development Division of MSFC. Technology development at the state-of-the-art level of MOS microelectronics is accomplished by in-house innovation and following closely the trends of the industry. The establishment and verification of new processes or processing methods are major tasks of this division. In some cases, new technologies are developed and verified which are then provided to industry to establish new and improved products.

2. Education. The training of personnel in NASA, other agencies of government, industry, and universities is another major function that is performed. Many personnel in NASA and other governmental agencies have been trained in microelectronics technology so that they can establish requirements for industries which supply microcircuits for their applications. Industries providing devices for NASA applications are required to have their

processing facilities certified by NASA. Other NASA personnel have received training when such training proved useful in their scope of work. Much written information has been provided to other NASA centers, governmental agencies, universities, and industries in addition to training. Tours and informal conferences are often held for the benefit of industry personnel or for university professors and students who have a need or desire for information concerning microelectronics. Research contracts with industries and universities provide another means of increasing the state of the technology.

3. Circuits. In experiments or direct NASA applications, small quantities of research and developmental circuits (which are not needed in sufficient quantities to make them commercially feasible) are produced. These circuits are specifically designed to meet the user's exact requirements to fulfill a necessary function. Specialized circuits, necessary for the support and completion of university research contracts and technology performance studies, have been produced. Other specialized circuits have been produced for university professors on special assignment with NASA for experiments on the physics of semiconductor devices. Other circuits have been produced to prevent the loss of a ground support computer. In the future, many types of research and development circuits needed by NASA can be produced to fulfill program goals. These capabilities are the culmination of a total effort in the Electronics Development Division to possess the required technology to produce IC from conceptual design through final testing.

George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Marshall Space Flight Center, Alabama 35812, February 1976

APPENDIX A

CHEMICAL SOLUTIONS USED IN P-MOS PROCESS

Several chemical solutions used in the processing of P-MOS IC require that they be mixed by the processor. Some solutions cannot be readily found in the mixed form while others should be mixed immediately before use. All chemicals used in processing should be reagent grade, electronic grade, or equivalent to prevent contamination of the wafers.

Sulfuric Acid – Nitric Acid Solution

2 ml	H_2SO_4	Sulfuric Acid (≈ 98%)
1 ml	HNO_3	Nitric Acid (≈ 70%)

Buffered Oxide Etchant

5 g	NH_4F	Ammonium Flouride – Crystal
2 ml	HF	Hydroflouric Acid (≈ 49%)
8 ml	H_2O	Water

Hydroflouric Acid Solution

1 ml	HF	Hydroflouric Acid (≈ 49%)
10 ml	H_2O	Water

Jacobson's Etchant

25 ml	H_2O	Water
5 ml	HCl	Hydrochloric Acid (≈ 37%)
5 ml	HNO_3	Nitric Acid (≈ 70%)
1 ml	H_2SO_4	Sulfuric Acid (≈ 98%)

Aluminum Etchant

25 ml	H_3PO_4	Phosphoric Acid (≈ 85%)
5 ml	CH_3COOH	Acetic Acid-Glacial (≈ 100%)
1 ml	HNO_3	Nitric Acid (≈ 70%)

Aluminum Compatible Photoresist Remover

55 g	H_2SO_4	Sulfuric Acid (≈ 98%)
1 g	CrO_3	Chromic Acid Anhydride-Crystal

Passivation Etchant

(Proprietary)

APPENDIX B

SILICON DIOXIDE GROWTH RATES

Silicon dioxide growth rates vary according to several factors. The most prevalent are silicon crystal orientation, ambient, time and temperature. The silicon used in the P-MOS process is either (111) or (100) orientation. Silicon dioxide on (111) orientation silicon grows approximately 1.4 times faster than (100) orientation for relatively thin layers. As the thickness increases, the growth rates for both orientations become slower and closer together. Silicon exposed to a steam ambient with an oxygen carrier gas will grow faster than silicon in a dry oxygen ambient. Silicon dioxide will increase in thickness when exposed for longer periods of time, and the growth rate increases as the temperature of the reaction is increased. The graphs [9] are oxide thickness versus time graphs for various temperatures on (111) orientation silicon in the given ambient (Figs. B-1 and B-2).

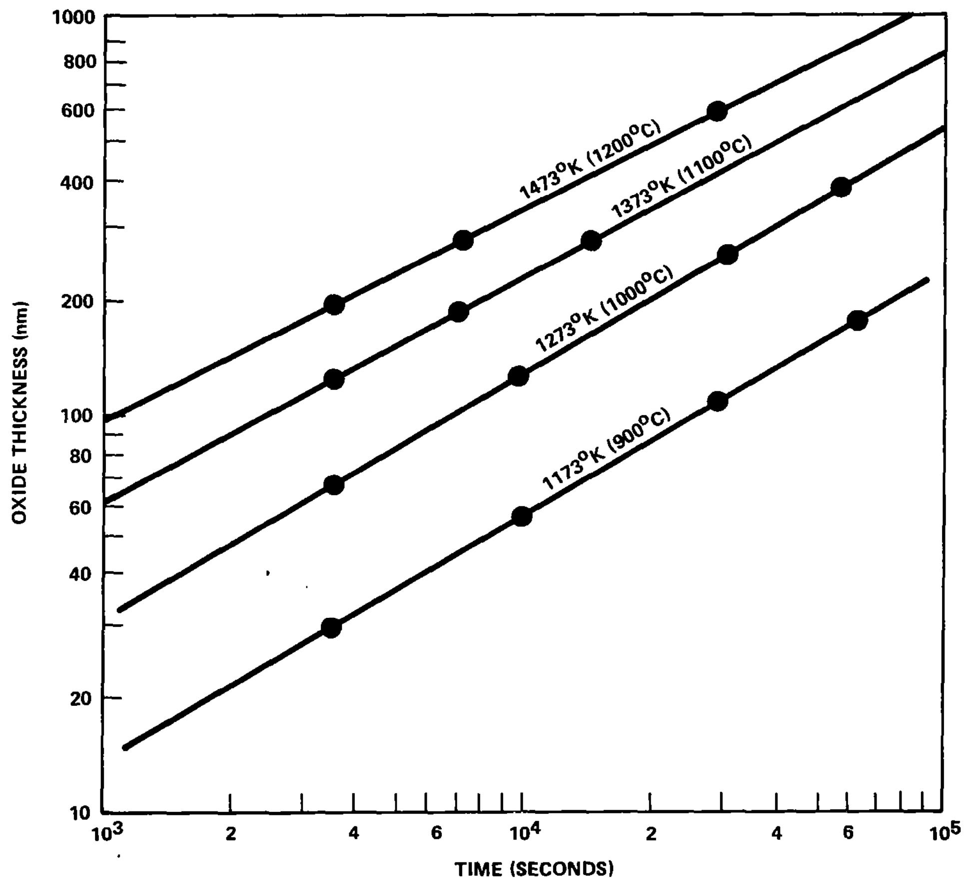

Figure B-1. Silicon dioxide growth rate curve for O_2.

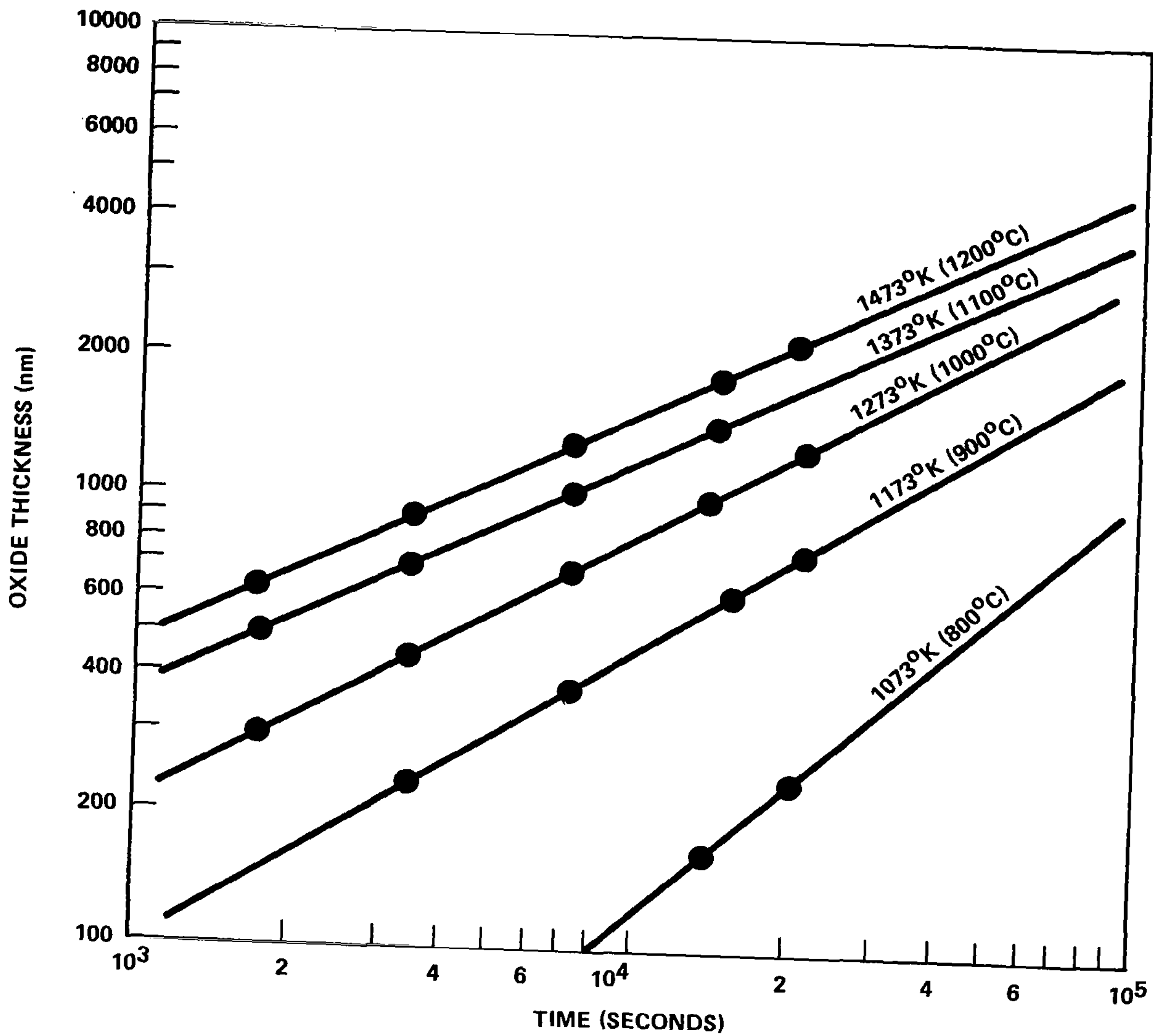

Figure B-2. Silicon dioxide growth rate curve for steam.

APPENDIX C

BORON NITRIDE DIFFUSIONS

Boron nitride (grade A) diffusions are primarily dependent upon time and temperature. Figure C-1 presents sheet resistance versus time for 1253°K (980°C). Sheet resistance is defined in units of ohms per square unit of area (□) because it is a function of geometry.

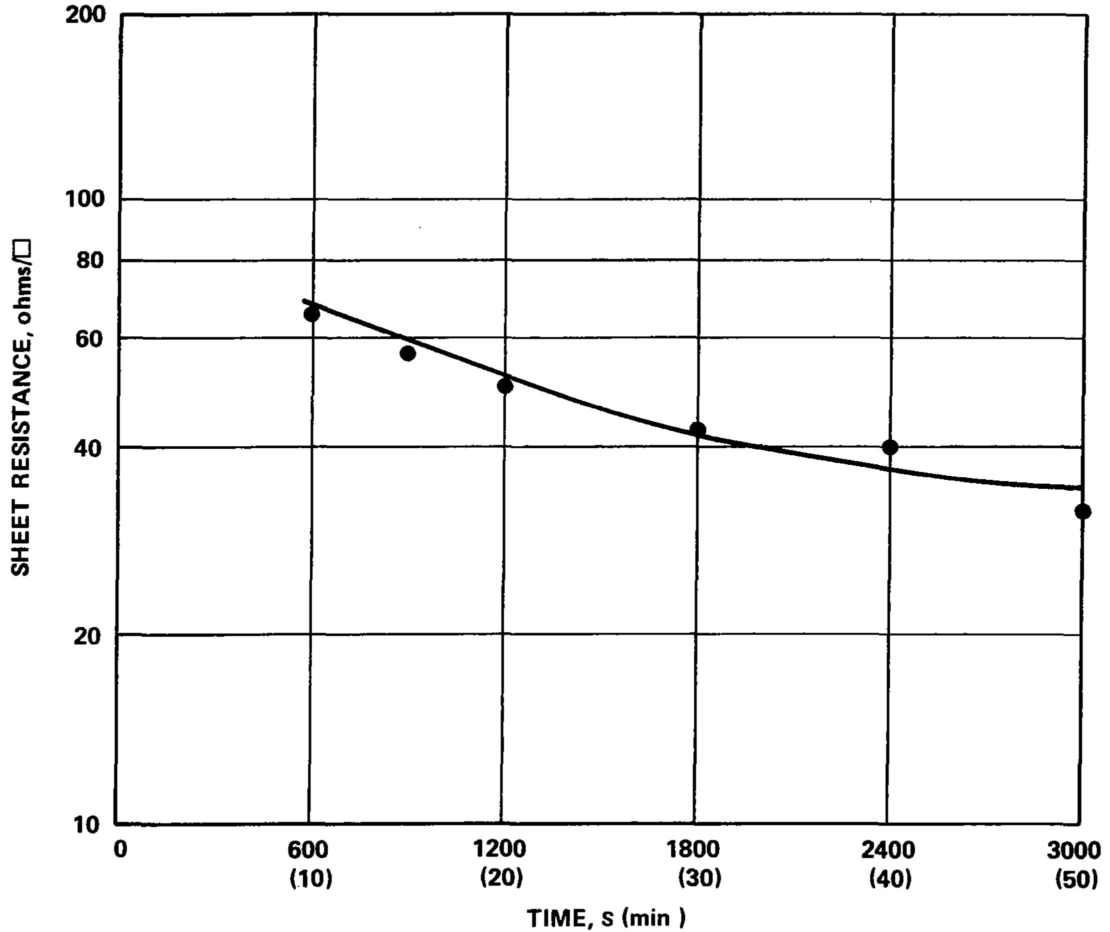

Figure C-1. Boron nitride diffusion curve.

APPENDIX D

OXIDE ETCH RATES

Silicon dioxide can be etched by hydroflouric acid which is the main ingredient in most oxide etchants. The two oxide etchants used in P-MOS are the HF solution and the Buffered Oxide Etchant described in Appendix A. HF solution is used when careful control of the thickness of oxide to be etched is required. At 298°K (25°C), HF solution etches at approximately 0.5 nm/s. Buffered Oxide Etchant is used over a wide range of temperatures to vary the etch rate and the amount of "controlled undercutting" needed to produce smooth slopes in the oxide for the aluminum lines to cross. The etch rate versus temperature is given in Figure D-1.

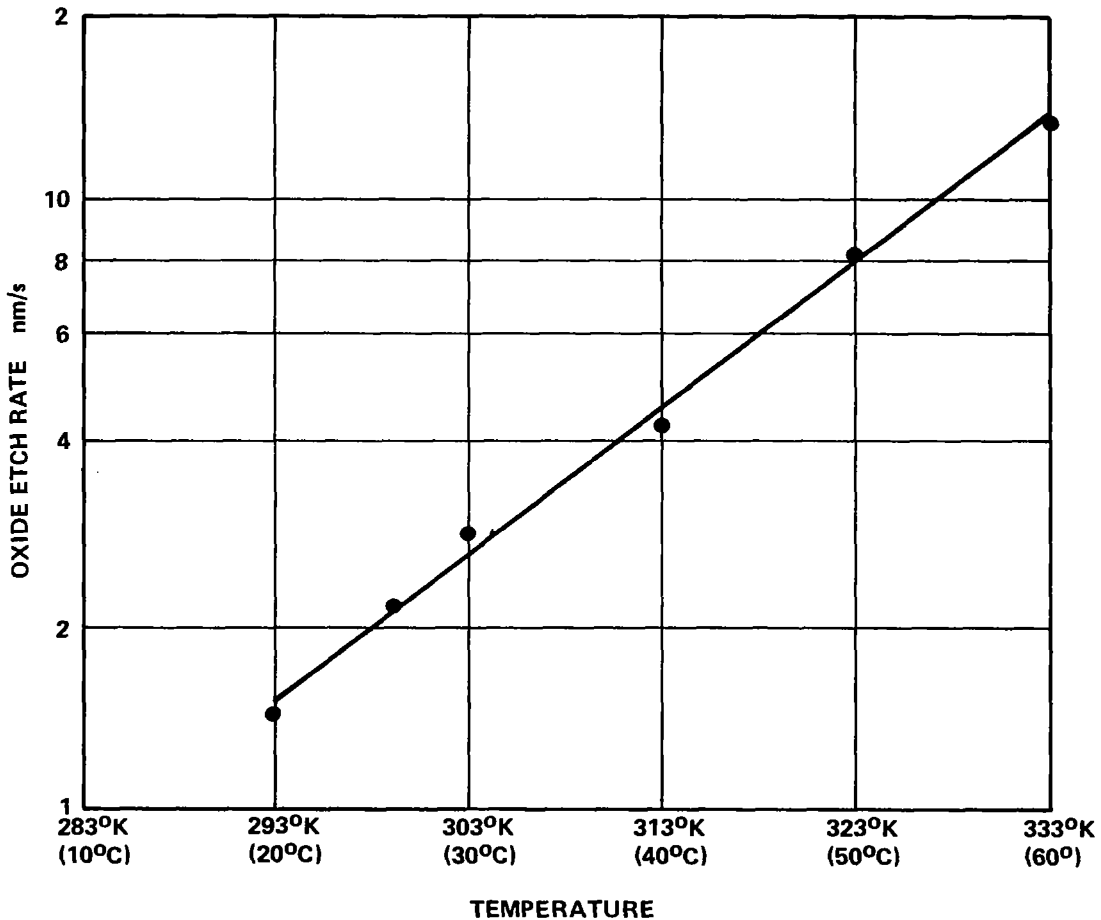

Figure D-1. Oxide etch rate curve.

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