W.W. GAERTNER RESEARCH INC.

NASA CR-
147827

A STUDY OF DISCRETE CONTROL SIGNAL FAULT CONDITIONS IN THE SHUTTLE DPS

CONTRACT NO. NAS9-14703

PROJECT NO. 4052

FINAL REPORT

(NASA-CR-147827) A STUDY OF DISCRETE CONTROL SIGNAL FAULT CONDITIONS IN THE SHUTTLE DPS Final Report (Gaertner Research, Inc.) 116 p HC $5.50 CSCL 14B G3/19

N76-28334

Unclas
47998

DATE: JUNE 30, 1976

PREPARED FOR: NASA LYNDON B. JOHNSON SPACE CENTER
HOUSTON, TEXAS 77058

DATE OF CONTRACT: JUNE 27, 1975

PREPARED BY: S. S. REDDI
C. T. RETTER
W. W. GAERTNER RESEARCH, INC.
205 SADDLE HILL ROAD
STAMFORD, CONNECTICUT 06903
(203) 322-3673

- TABLE OF CONTENTS -

- LIST OF ILLUSTRATIONS -

- LIST OF ILLUSTRATIONS -
(continued)

- LIST OF ILLUSTRATIONS -
(continued)

- LIST OF TABLES -

1. INTRODUCTION

The space shuttle represents a pioneering effort in avionics history. Its primary goals are to provide low-cost transportation to and from earth orbit and to offer a platform for conducting experiments in space. It will also enable deployment and recovery of free flying or automated satellites. The shuttle complex is controlled by a Digital Processing Subsystem (DPS)* which consists of five identical general-purpose digital computers, each capable of controlling and/or communicating with other shuttle subsystems such as Main Propulsion; Reaction Control; Guidance, Navigation and Control; Flight Instrumentation. The DPS is intended to satisfy the stringent reliability requirements imposed by the space mission and its design ensures fail-safe and fail-soft performance.

Figure 1 shows a block diagram of the space shuttle avionics system. The five computer systems, GPC1 through GPC 5, comprise the DPS and control the other avionic subsystems through twenty-eight data-bus channels. Each GPC consists of a CPU and an IOP; the CPU performs mainly computation whereas the IOP is responsible for interfacing the CPU with the bus channels. The GPCs communicate their status or mode of computation to each other through signals on 40 input and 32 output IOP discretes [2]. These discretes are of principal interest to this investigation. An analysis was conducted to determine the impact a fault on these discretes may have on system performance in terms of reliability and fail-safeness. The propagation of hardware discrete faults into software and applications program logic was traced and recommendations were developed to curtail the propagation as soon as possible and to minimize any adverse consequences.

The following items were accomplished by W. W. Gaertner Research, Inc. during its contract with NASA-JSC.

1) Identification and functional description of IOP discretes.

2) Identification of operating system (FCOS) modules that use IOP discretes and the manner of usage.

3) Analysis of the effects of faults on IOP discretes in terms of system degradation (e.g., loss of a GPC from the redundant set).

4) Determination of the time that may elapse before a fault on IOP discretes is detected.

5) Recommendations to prevent/detect faults on IOP discretes and suggestions for future research.

---

* A List of Acronyms is attached to this report.

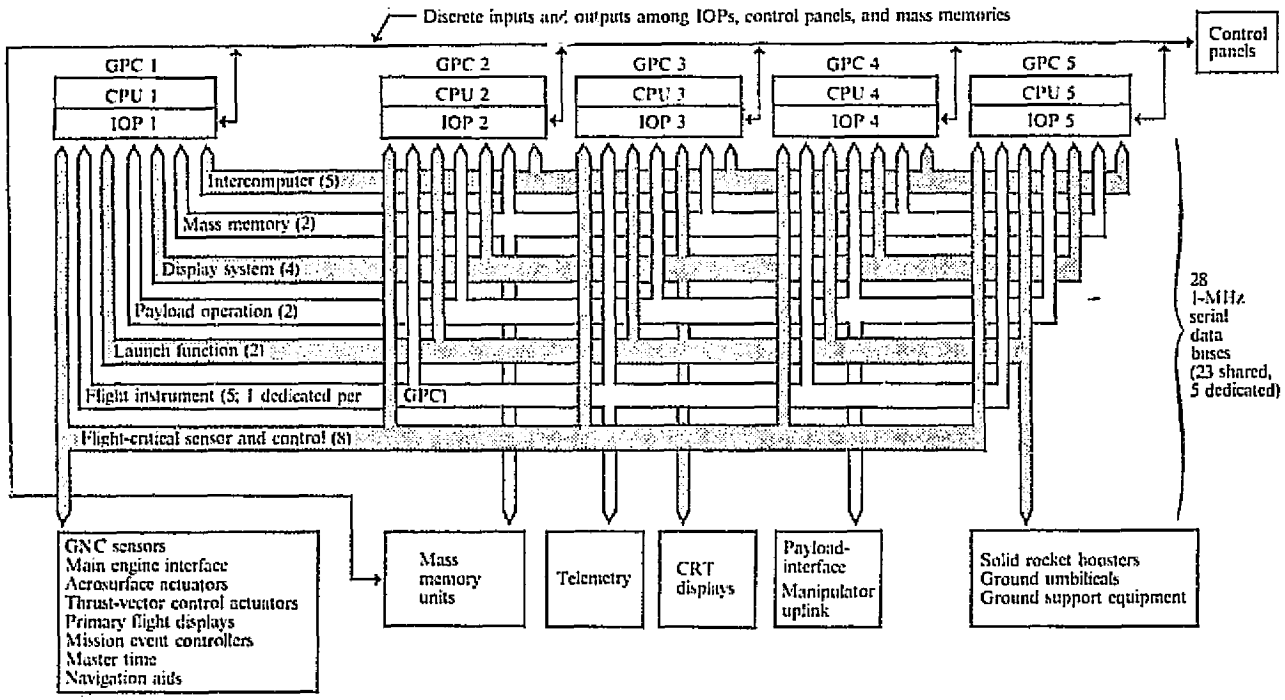


Figure 1. Space Shuttle avionics system block diagram [1]

The organization of the report is as follows. Chapter 2 is exclusively devoted to item (1). Items (2), (3) and (4) are treated in detail in Chapter 3. Chapter 4 discusses probabilistic aspects of IOP discrete fault occurrences and presents an assessment of system failure rate. In Chapter 5 methods of prevention/detection of IOP discrete faults and recommendations are made that may be incorporated into system hardware/software to improve mission reliability. Chapter 6 presents methods of recovering GPCs lost because of non-synchronization during OFT phase. This chapter also discusses alternative approaches to the design of redundant avionic computer systems and future work.

The initial phase of this Contract was monitored by Mr. Curtis D. Warnick and the final phase by Mr. Allen E. Brandli, both of NASA-JSC, Houston, Texas. They were extremely helpful in procuring technical documents on the space shuttle and arranging conferences with appropriate technical personnel. Discussions with the following individuals were beneficial in gaining insight into the space shuttle data processing: Messrs. Charles Floyd, Sam Ankney and Ed Dalke of NASA-JSC; and Jerry Johnson and Vic Harrison of Rockwell International Space Division. This report was prepared with the assistance of Mona G. Adams, Marilyn B. Kommritz and Marianne P. Gaertner.

2. FUNCTIONAL DESCRIPTION OF IOP DISCRETES

In this chapter each IOP discrete is identified in terms of the label of specification used in System Level Description, Hardware, CPDS, Volume 1, Book 1 [3] and the IOP pin numbers used in the actual hardware construction of the IOPs [4]. This allows traceability of IOP discretes from their functional specifications to their physical locations, a feature useful for trouble-shooting and design alterations. Then the function for which each IOP discrete is intended is described. This functional description gives an overview of the important and critical role played by the discretes in the overall data and control management.

The IOP discretes of a GPC serve one of the following functions:

(a) Local control and status indication of the GPC,

(b) Synchronization status communication to other GPCs, and

(c) Redundancy management.

The discretes that perform function (a) issue commands such as halt, standby, run and IPL initiate and indicate the mode of the GPC, e.g., halt, standby and IPL-in-progress. The discretes assigned to function (b) are vital to synchronous performance of the GPCs. They indicate whether a particular GPC is in a redundant set and enable synchronization of GPCs after I/O transactions, supervisory calls and timer interrupts. Discretes that perform (c) are used to indicate the assessment of each GPC regarding the functional behavior of other GPCs. Voting logic is incorporated in these discretes to decide whether a particular GPC is functioning correctly.

As may be noted, discretes performing (b) and (c) are not needed if the GPC is intended to be operated alone as a backup flight control system. Accordingly the discretes for GPC 5 are wired differently from the others. In Table 1 IOP discretes are shown for GPCs 1 to 4 with their labels, pin numbers, functional identifications, sources and destinations. Table 2 shows the discretes for GPC 5.

LABEL	IOP PINS	FUNCTION	I/O	FROM/TO
		IDENTIFICATION		
DO30	J3-57,58	GPC ID source	output	IOP N
DI32	J3-74,75	GPC ID bit 0 (binary 1)	input	IOP N
DI33	J3-116,123	GPC ID bit 1 (binary 2)	input	IOP N
DI34	J3-107,122	GPC ID bit 2 (binary 4)	input	IOP N
		REDUNDANCY MANAGEMENT		
DRI03	J5-36,37	GPC N+1 fail vote in	input	IOP N+1
DRI04	J5-35,47	GPC N+2 fail vote in	input	IOP N+2
DRI05	J5-33,34	GPC N+3 fail vote in	input	IOP N+3
DR000	J5-46,58	GPC fail indicator	output	panels
DR007	J5-44,45	GPC N+1 fail vote out	output	IOP N+1
DR008	J5-42,43	GPC N+2 fail vote out	output	IOP N+2
DR009	J5-40,41	GPC N+3 fail vote out	output	IOP N+3
		SYNCHRONIZATION		
DI20	J3-80,91	GPC N+1 sync bit 1	input	IOP N+1
DI21	J3-92,104	GPC N+2 sync bit 1	input	IOP N+2
DI22	J3-103,114	GPC N+3 sync bit 1	input	IOP N+3
DI24	J3-113,121	GPC N+1 sync bit 2	input	IOP N+1
DI25	J3-112,128	GPC N+2 sync bit 2	input	IOP N+2
DI26	J3-101,111	GPC N+3 sync bit 2	input	IOP N+3
DI28	J3-119,126	GPC N+1 sync bit 3	input	IOP N+1
DI29	J3-99,109	GPC N+2 sync bit 3	input	IOP N+2
DI30	J3-118,125	GPC N+3 sync bit 3	input	IOP N+3
DO20	J3-43,44	GPC N sync bit 1	output	3 IOPs
DO24	J3-34,35	GPC N sync bit 2	output	3 IOPs
DO28	J3-46,47	GPC N sync bit 3	output	3 IOPs
		CONTROLS AND INDICATORS		
DO07	J3-36,48	I/O active indicator	output	panel
DO09	J3-25,37	GPC ready indicator	output	panel
DO31	J3-67,68	GPC IPL indicator	output	panel
DI00	J5-1,2	GPC halt command	input	panel
DI01	J5-3,4	GPC standby command	input	panel
DI02	J5-5,6	GPC run command	input	panel
DI03	J5-7,8	GPC IPL activate command	input	panel
DI04	J5-8,9	MM1 IPL select command	input	panel
DI05	J5-10,11	MM2 IPL select command	input	panel
DI12	J5-25,26	I/O terminate command A	input	panel
DI13	J5-27,28	I/O terminate command B, BFCS	input	panel
EXCIT	J3-110	+ 5 volts	output	panels
S	J3-100	Signal return	output	panels
		MASS MEMORY		
DO12	J3-8,16	MM1 reset	output	MM1
DO13	J3-17,27	MM2 reset	output	MM2
DI06	J5-12,13	MM1 ready	input	MM1
DI07	J5-15,16	MM2 ready	input	MM2
		BFCS		
DI11	J5-23,24	BFCS engage command	input	BFCS

Table 1. IOP Discretes for GPC N (Orbiter 101, GPC 1-4)

Note: GPC N+i indicates GPC N+i (mod 4)

LABEL	TOP PINS	FUNCTION IDENTIFICATION	I/O	FROM/TO
D030	J3-57,58	GPC ID source	output	IOP 5
DI32	J3-74,75	GPC ID bit 0 (binary 1)	input	IOP 5
DI33	J3-116,123	GPC ID bit 1 (binary 2)	input	IOP 5
DI34	J3-107,122	GPC ID bit 2 (binary 4)	input	IOP 5
		REDUNDANCY MANAGEMENT		
DR000	J5-46,58	GPC fail indicator	output	panels
		CONTROLS AND INDICATORS		
D009	J3-25,37	GPC ready indicator	output	panel
DI00	J5-1,2	GPC halt command	input	panel
DI01	J5-3,4	GPC standby command	input	panel
DI02	J5-5,6	GPC run command	input	panel
EXCIT	J3-110	+ 5 volts	output	panels
S	J3-100	Signal return	output	panels
		BFCS		
DI13	J5-27,28	I/O terminate command B inverse	input	BFCS
DI11	J5-23,24	BFCS engage command	input	BFCS
DI15	J3-66,67	BFCS engage command	input	BFCS
DI16	J3-88,89	BFCS engage command	input	BFCS
D008	J3-61,62	BFCS fail	output	BFCS

Table 2. IOP Discretes (Orbiter 101, GPC 5)

In the following, the primary function of each discrete is described in detail. The above functional classification is used to clarify its role.

2.1 Identification Discretes

Each computer contains three ID discrete inputs, which are used to allow the computer to determine the position in which it has been installed. The 3-bit binary code which identifies each computer position is formed by wiring the constant differential output of the ID Source line driver to each ID input bit with the appropriate polarity. For example, the computer in Forward Avionics Bay III is GPC 3, so the connector for IOP J3 at that position must have ID bits 0 and 1 wired directly to the ID Source and ID bit 2 wired to the ID Source with inverted polarity. The connections between the ID Source differential output and the three ID differential inputs are as follows [4]:

LOCATION	COMPUTER	ID BIT 2	ID BIT 1	ID BIT 0
Forward Avionics Bay I	GPC 1	inverted	inverted	direct
	GPC 4	direct	inverted	inverted
Forward Avionics Bay II	GPC 2	inverted	direct	inverted
	GPC 5	direct	inverted	direct
Forward Avionics Bay III	GPC 3	inverted	direct	direct

The identification discretes serve function (a) and are primarily used in the initialization routine. In this routine the GPC number is read from the discretes and stored in internal software tables (Compool and CVT) and thereafter these tables are consulted for GPC identification numbers. The identification numbers are used to select the prime computer system as well as to track the GPCs that failed to synchronize in a redundant set.

2.2 Redundancy Management Discretes

Three input and four output discretes are assigned to the redundancy management function. Signals on three of the output discretes (DR007, 08, 09) are issued from one GPC to other GPCs to indicate failure votes. A failure vote is issued under software control by one GPC to another when there is a mismatch between their computed results. The fourth output discrete (DR000) is a GPC fail indicator.

It indicates that the GPC has detected a BITE self-test failure or has been voted out of the GPC voting set. The signal is automatically issued upon IOP hardware detection of two or more failure votes from other IOPs of the voting set, expiration of the watchdog timer, or detection of GPC self-test failure (providing these functions have been enabled or initiated by GPC software). It should be noted that the CPU is not reset upon GPC/IOP failure determination, and CPU instruction execution is still possible after a GPC failure. The IOP hardware reset of all GPC outputs, however, prevents the GPC from participating in the control of the Space Shuttle vehicle.

The GPC fail indicator output signal from each GPC terminates at two units: a 5-by-5 computer (failure) status display matrix, and the caution/warning electronics unit. In addition, at the 5-by-5 display, the GPC fail indicators are amplified and sent to operational instrumentation where they are sampled for downlink transmission.

The caution/warning electronics unit accepts the GPC fail indicator signals and retransmits them to a caution/warning status display (120 indicators). The GPC fail indicator signal from each GPC may be monitored at this display. The electronic unit also transmits the logical OR of all five GPC fail indicator signals to the caution/warning annunciator display where a single light is turned on. When this signal is issued, it is accompanied by an audible alarm that remains on until manually reset from either of two master alarm reset switches located at the forward station.

The 5-by-5 computer (failure) status display is driven by all five redundancy management output signals from each IOP (four failure votes and one failed condition). Since there are five GPCs, there are a total of 25 indicators. The GPC fail indicator for a given GPC lies along the matrix diagonal from the upper left to the lower right. All other indicators represent fail votes. The 5-by-5 display matrix allows visual observation of the failure status of all five GPCs [2].

The redundancy management function is invoked after every SSIP cycle at forty millisecond intervals. The GPCs transfer data to each other on Inter-Computer Communication (ICC) bus units so that they can compare and vote on each other.

2.3 Synchronization Discretes

These discretes convey the status of GPCs to each other so that they can be run in synchrony. Each GPC has three output discretes which indicate its synchronization status. Table 3 gives the synchronization codes used in the space shuttle complex. Logic 0s on all the output discretes indicate that the GPC is not operative and does not participate in computation or control. The I/O codes (010 and 011) indicate that the GPC completed its I/O transactions with or without encountering errors in data transmission. The timer and SVC interrupts indicate that the GPC was interrupted by a time-out indication from one of its timers and by supervisory call from an application or FCOS program respectively. SSIP synchronization code is used to synchronize the GPCs in the common set at every SSIP cycle. Logic 1s on the output discretes indicate that the GPC is either running or expecting other GPCs to synchronize.

The synchronization discretes are used quite often (at rates of approximately 300 times/sec) and the manner in which they are used depends to a large extent on the application programmer.

SYNCHRONIZATION CODES [5]

Number	Binary	Meaning
0	000	Halt/Off/Failed
1	001	Spare
2	010	I/O Complete, with error (IPR)
3	011	I/O Complete, no error (IOC)
4	100	SSIP sync (common set)
5	101	Timer Interrupt
6	110	SVC Interrupt
7	111	Null/Run

Table 3

2.4 Control and Indicator Discretes

These discretes are primarily used to control and indicate the status of the GPC they are associated with. They perform function (a) and play a critical part in interfacing the GPC and the crew.

2.4.1 GPC Halt/Standby/Run Command Discretes

These discretes are controlled by a three-position toggle mode switch from Cockpit Panel O7. A separate switch is provided for each GPC.

Each switch provides three input signals (Halt, Standby, or Run) to the respective discrete. The three signals are interlocked in IOP hardware logic so that only one switch state is possible regardless of any switch bounce that is encountered. For example, when the switch is moved from one position to another, the switch leaves the first position, encounters an open-circuit, and then makes contact at the second position. During the open-circuit transition, the previous switch state is maintained in hardware latches in the IOP. Open-circuit signals do not change the state of these latches.

When the switch completes the open-circuit transition and finally makes contact at the next position, the new state is detected and stored by the interlocked latches. At this point, should switch bounce be encountered, producing momentary open-circuit conditions, the hardware latches guarantee that the switch state just established will be retained. The IOP logic thus guards against switch bounce.

When the Halt Command discrete is set, an automatic reset of both the CPU and IOP is caused. In this reset state, normal macro instructions cannot be executed in the CPU and IOP; however the GPC can support IPL, and Halt is the only state in which IPL can be performed.

When the Standby discrete is set, the GPC is able to operate in an off-line mode, not synchronized to other GPCs. The Standby mode is identical to the Run mode except that it does not completely utilize the memory and configuration tables. In the Standby mode, application programs can be run, thus making it possible to test and diagnose system operation. The GPC in Standby mode has less priority than a GPC in Run more in order to prevent IOP bus contentions when one or more GPCs are in Standby [6].

The Run mode is used during normal GPC operations. However, this mode can be overridden by software in which case the GPC Ready Talkback indicator will indicate barberpole rather than gray.

2.4.2 GPC Ready Indicator Discrete

This discrete drives a barberpole/gray flag indicator to indicate the GPC status. When the discrete bit (D009) is set true, the indicator is driven to the gray position to indicate that the GPC is ready for normal processing. The IPL discrete can also drive this indicator to gray when IPL is in progress. The GPC 5 Ready indicator for ALT phase indicates that backup flight control capability is resident and can be processed by engaging BFCS switch.

When the discrete bit is false, the indicator is driven to barberpole to indicate that the GPC is not ready. This indication is present when the GPC detects a hardware or software error. Some of the hardware detected errors are IOP timing fault, power supply failure/off, and parity errors within the CPU. Also a Halt mode and Command can cause this indication.

2.4.3 GPC IPL and IPL Activate Discretes

The GPC IPL discrete when true indicates that the GPC is performing IPL. The IPL Activate discrete is driven by a momentary pushbutton switch on the cockpit panel. Depression of the switch sets the IPL Activate discrete true and causes IPL to be performed. The IPL discrete as mentioned before will drive the Ready talkback indicator gray to indicate IPL-in-progress. The IPL Activate command will be effective only when the GPC is in a Halt state.

2.4.4 I/O Active Indicator Discrete

This discrete indicates the status of the GPC as to whether it can perform I/O on its data buses. A true output indicates that the GPC is ready to perform I/O after GPC initialization whereas a false output indicates either that the GPC is powered off or that the GPC, though powered on, is unable to perform I/O because of its IOP reset state or non completion of GPC initialization.

2.4.5 I/O Terminate Command Discretes

There are two discretes assigned for I/O terminate function. The I/O Terminate Command A discrete is derived from one pole of a double-pole output terminate switch on Panel 07. (The other pole issues the IOP Terminate Command B discrete). This Command causes immediate disable of four MIA transmitters for buses FC 1 through FC 4. The discrete input is always accompanied by the IOP Terminate Command B discrete.

The IOP Terminate Command B discrete is controlled by the second pole of the output terminate switch and when this command is received, eight MIA transmitters are immediately disabled to halt data transmission over flight-critical buses FC 5 through FC 8, payload buses PL 1 and PL 2 and launch data buses LDB 1 and LDB 2. The Backup Flight Control (BFC) switches on panels F 2 and F 4 also control the IOP Terminate Command B discrete.

2.4.6 MM IPL Select Command Discretes

These discretes specify which Mass Memory unit has been selected for IPL operation of the GPC.

2.5 Mass Memory Discretes

Each Mass Memory generates a ready signal and controls the state of the MM Ready discrete of each GPC. A ready signal, when enabled, indicates to the GPC that the MM is in the standby mode and is capable of accepting commands. If not enabled, it indicates that either the MM primary power is off or that the MM is performing an operation. In the latter case, it will stay in the not-ready state until the operation being performed is complete.

Reset discrete signals, one from each GPC, can interrupt the operation of the Mass Memory unit. When interrupted by the reset signal, the MM will halt its operation at the end of the current data block, stop the tape in the next subfile, and write protect all tracks. When these operations are completed, the ready signal is enabled to the GPCs. If the MM is already in the ready state, no action will occur as a result of the reset.

2.6 Backup Flight Control System Engage Command Discrete

When this discrete is true, it means that the BFC Engage switch on panels F 2 or F 4 is on and that the flight control is to be transferred from the Primary to the Backup Control System. When the discrete is false, it indicates that the BFC Engage switch is in 'off' position and that

flight control is handled by the Primary system.

2.7 Discretes of GPC 5, the Backup System

GPC 5 is used for the Backup Flight Control System (BFCS). The BFCS can be engaged by pressing one of the two BFC Engage switches. When one of these switches is pushed, the BFCS Control Unit sends the I/O Terminate Command B to all of the computers. However, the polarity of this signal is reversed for GPC 5, with the result that GPCs 1-4 have their flight-critical outputs disabled, and GPC 5 has its outputs enabled, when a BFC switch is pushed. BFC Engage indicators, located in the BFC switches, are controlled by MDM FF5.

The discrete signals for GPC 5 are listed in Table 2. (Since GPC 5 is not used in conjunction with the other four computers, there are no Fail Votes or synchronization signals to or from GPC 5). In addition to the Fail Votes and synchronization signals, several other discrete control signals are not used in GPC 5. No I/O Terminate switch exists for GPC 5, so the I/O Terminate Command A discrete input is not used. Since the BFCS does not use the Mass Memories, there are no Mass Memory Ready, Reset, or IPL Select signals connected to GPC 5; there is no IPL Activate switch/indicator and, therefore, the corresponding discrete signals are not used. The functions of the remaining discrete signals are as previously described.

3. PRIMARY AND SECONDARY EFFECTS OF FAULTS ON DISCRETES

In this Chapter the primary and secondary effects of faults on the IOP discretes are discussed. First the Flight Computer Operating System (FCOS) modules that use these discretes and the manner of their usage are identified. This enables one to trace the propagation of errors from hardware to software. Secondly, each of these FCOS modules is analyzed to determine the effects of misinterpretation of the logic levels on the discretes due to single bit errors. This information will be useful in recovering GPCs that are lost due to discrete failures either in the OFT or post-mission phase. It is also useful for modifying software modules so that the impact of discrete failures on system performance is minimized. Thirdly, the impact of each discrete failure on the total system is described. This will give an assessment of the relative criticality of each discrete. Finally, the minimum time before the detection of a discrete failure is estimated and suggestions are made to further reduce this time.

The FCOS is a set of code blocks which manages the DPS computer hardware complex and allocates its resources to all OFP functions. It is responsible for the control services and allocation of computer resources, as well as the supervision of all computing processes in the OFP. It also provides a number of service functions, such as input/output, interrupt supervision and time/event services. The FCOS is a tool used by the application programmer and, when taken by itself, does not provide a mission software design. The FCOS does not partition or specify how software functions are divided between computers or within a computer. The FCOS does, however, provide the structure for controlling individual software functions to meet individual mission requirements [6].

Thus the FCOS serves as the interface between the hardware and the application programmer and represents the first stage in Control transition from hardware to software. Some of the FCOS modules interpret and act on the logic signals they read on the discretes. The flow-charts of these modules are shown in Figures 3-1 to 3-22. (They are extracted from Reference [5]).

The modules that issue commands which cause logic level transitions on the discrete lines are analyzed to determine the effects of single-bit discrete errors. The flow-charts of these modules are shown in Figures 3-23 to 3-31. They indicate the correct commands to be issued (shown enclosed by double lines) as well as the incorrect commands that may be issued due to a single discrete failure (shown enclosed by a single line). Thus

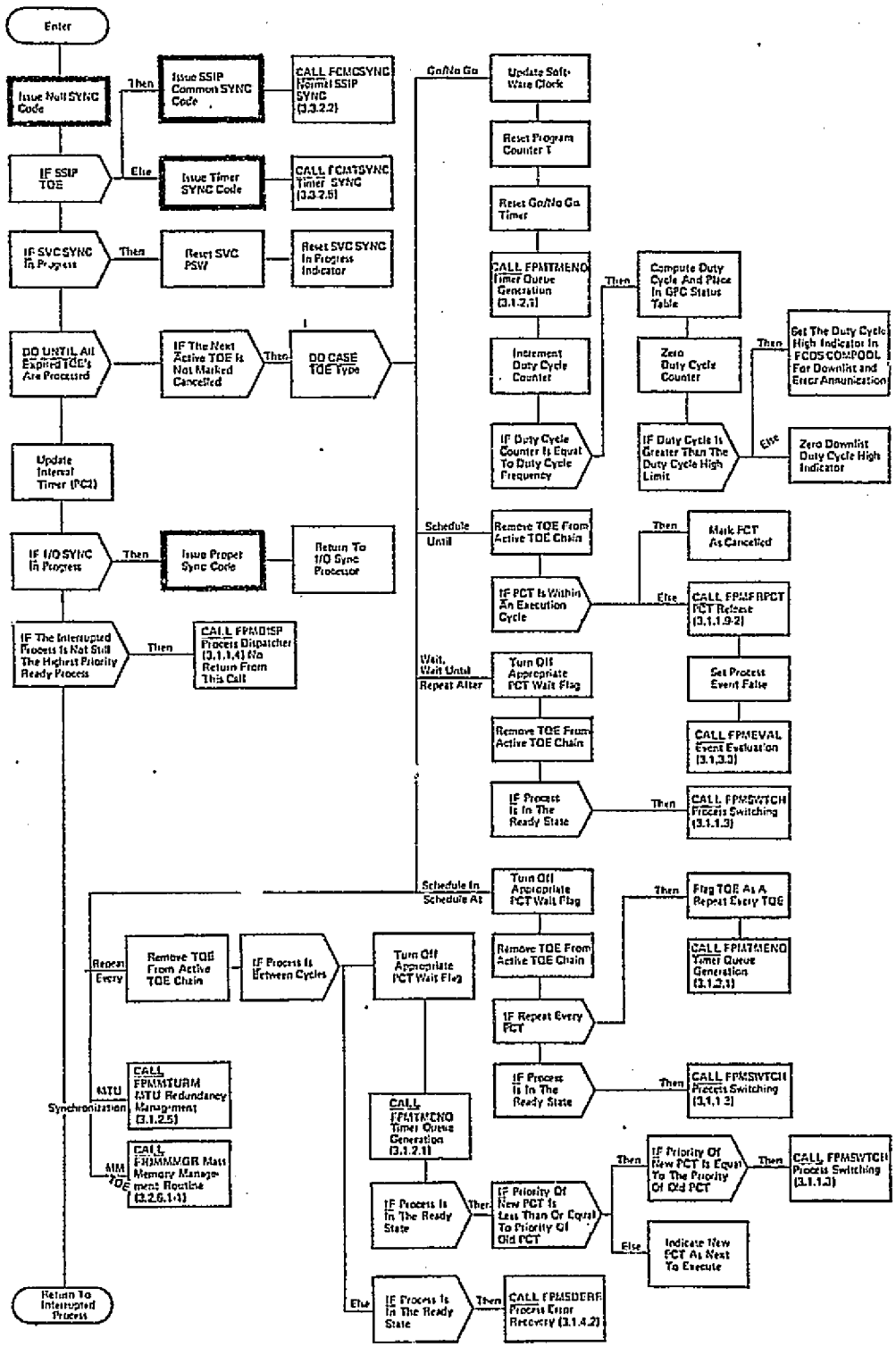


Figure 3-1. Timer Queue Element Expiration (FPMIHPC2)

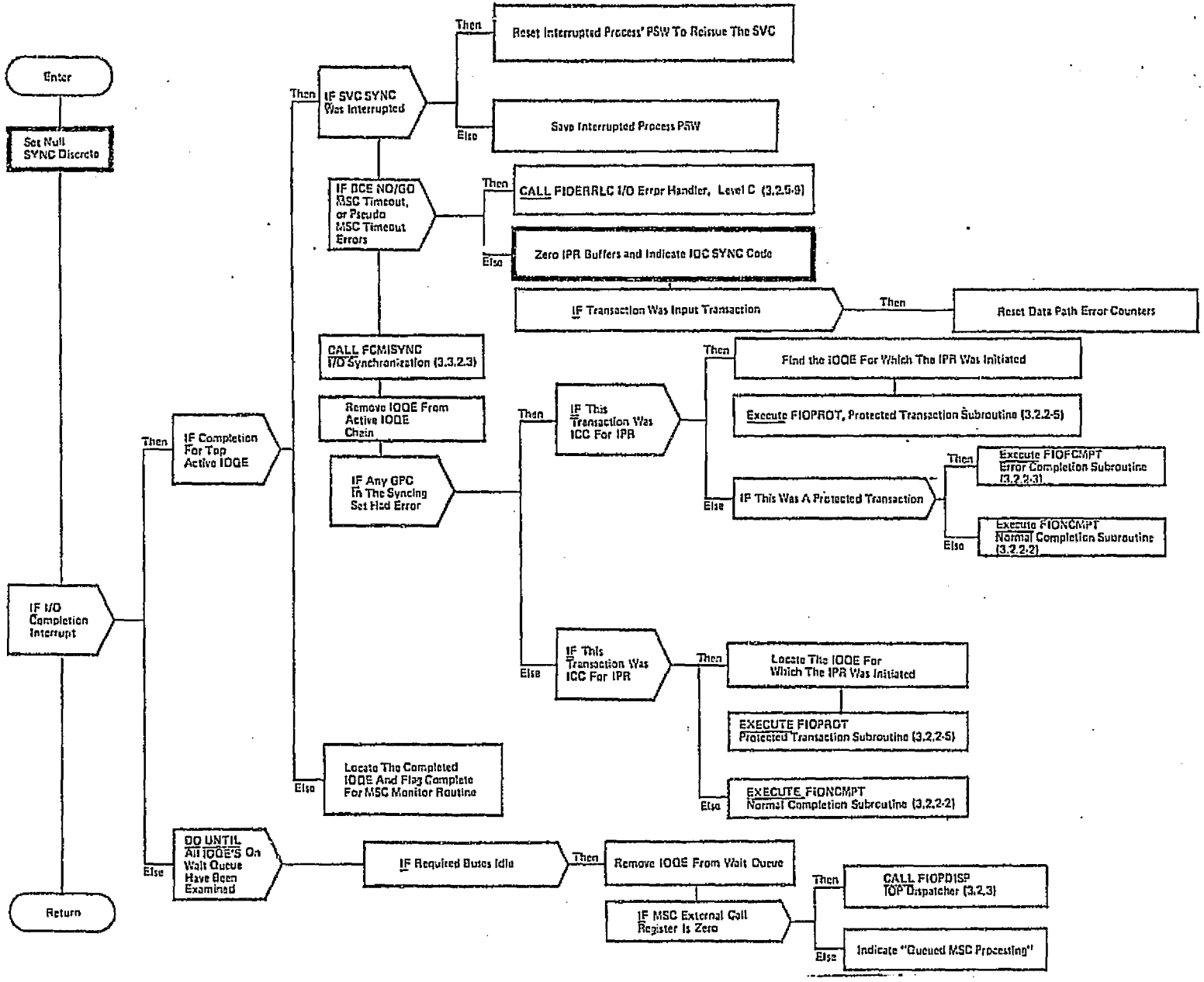


Figure 3-2. I/O Completion Processor (FIOCMPLT)

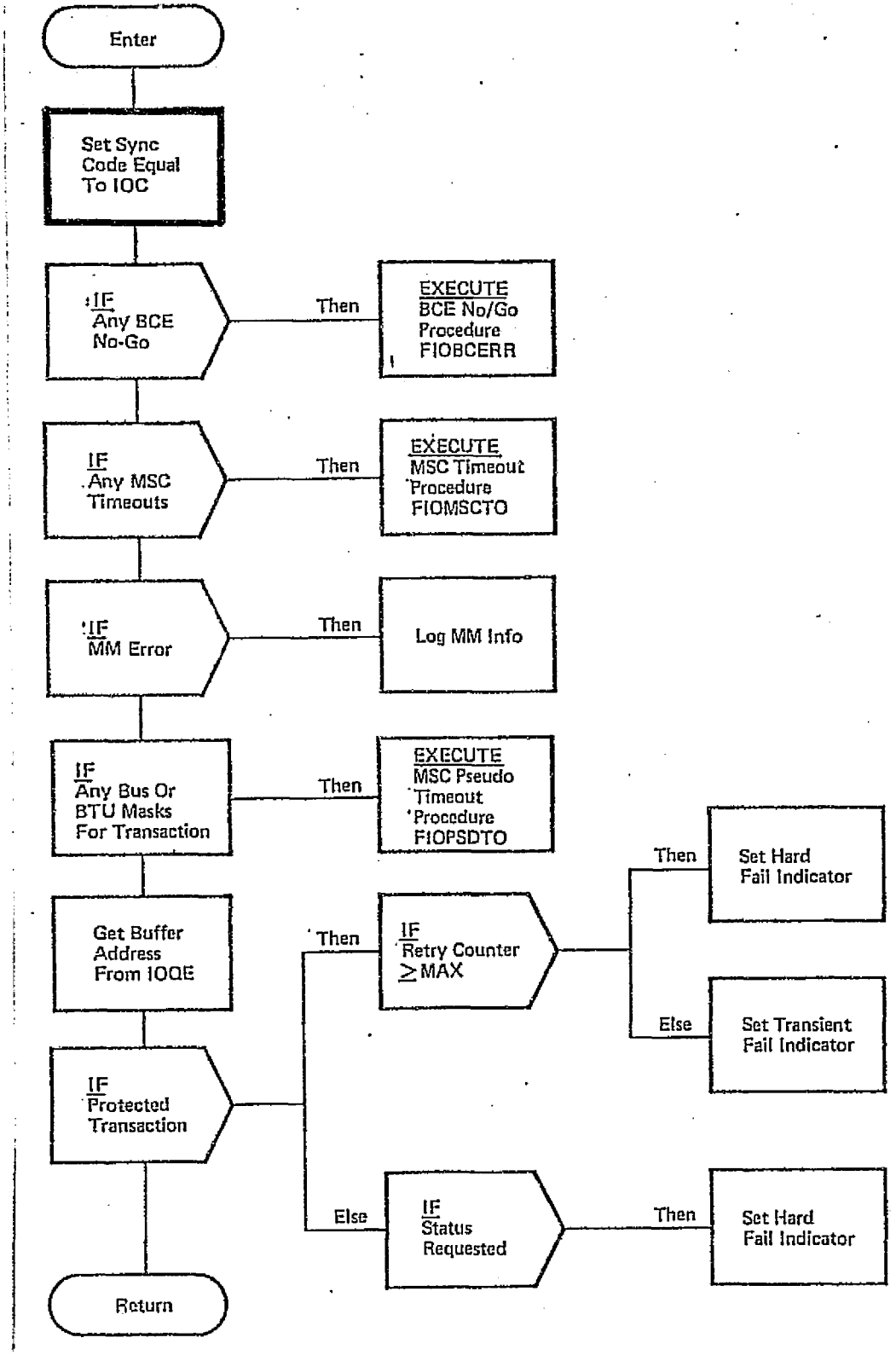


Figure 3-3. I/O Error Handler, Level C (FIOERRLC)

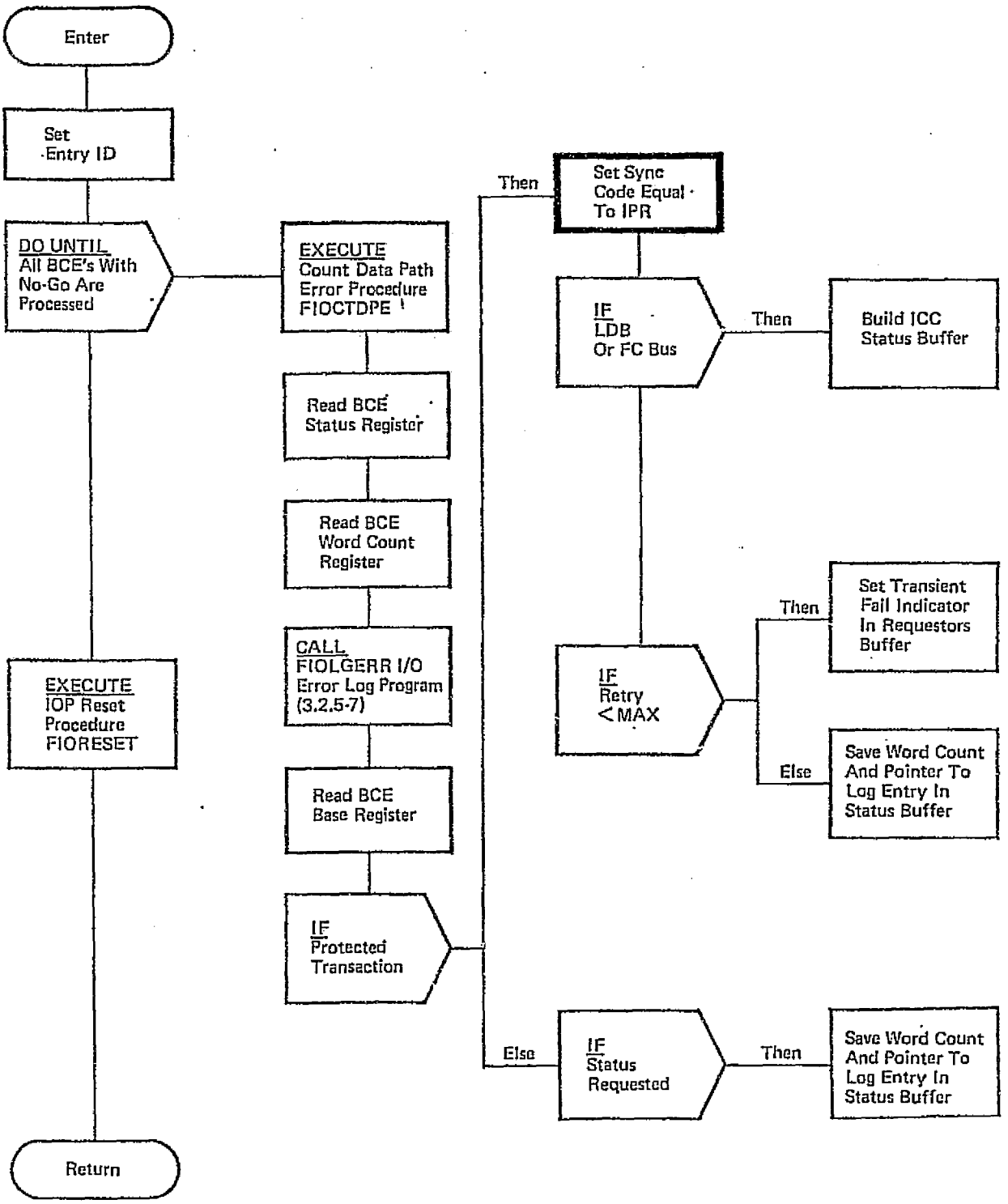


Figure 3-4. BCE No/Go Procedure (FIOBCERR)

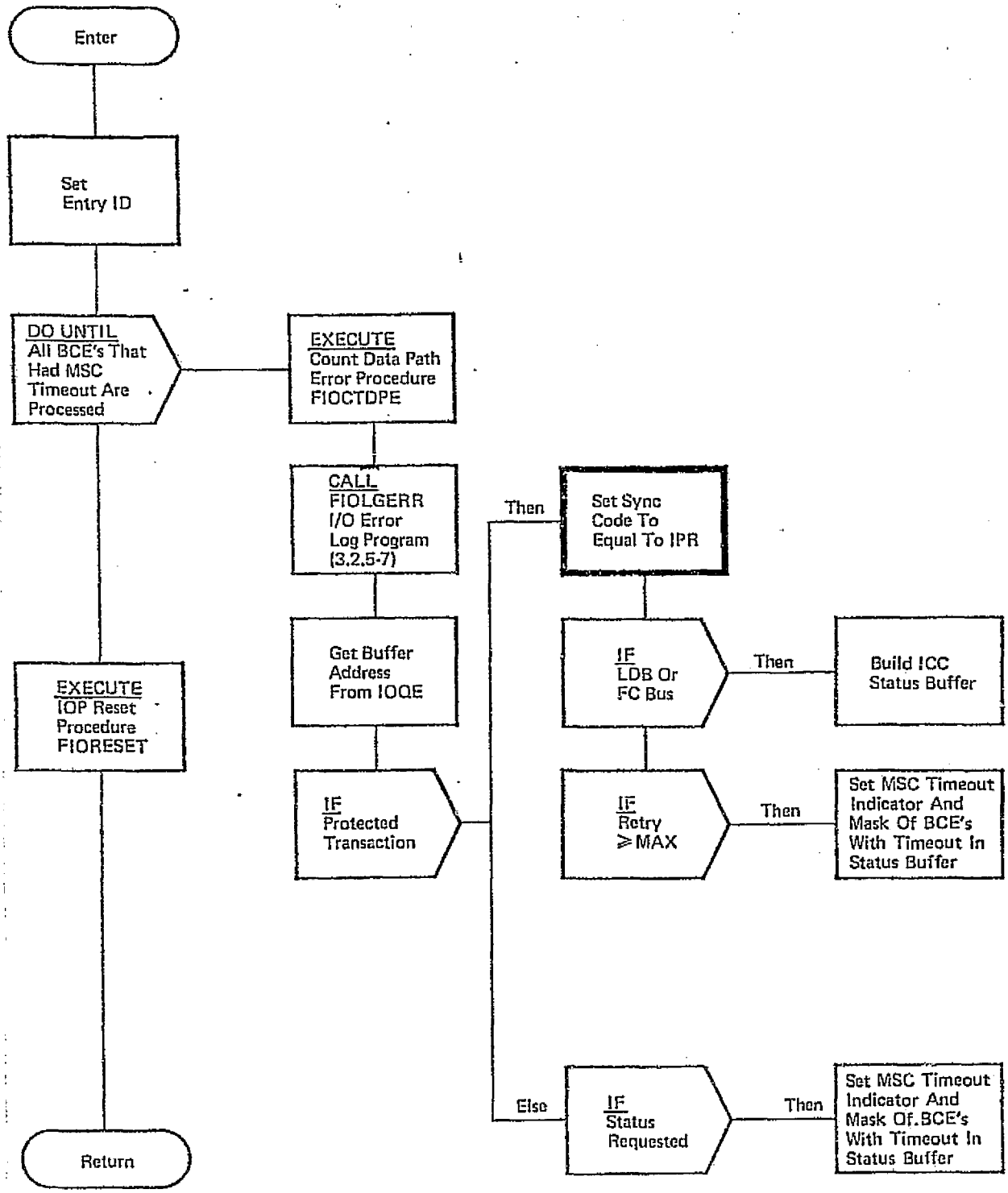


Figure 3-5. MSC Timeout Procedure (FIOMSCTO)

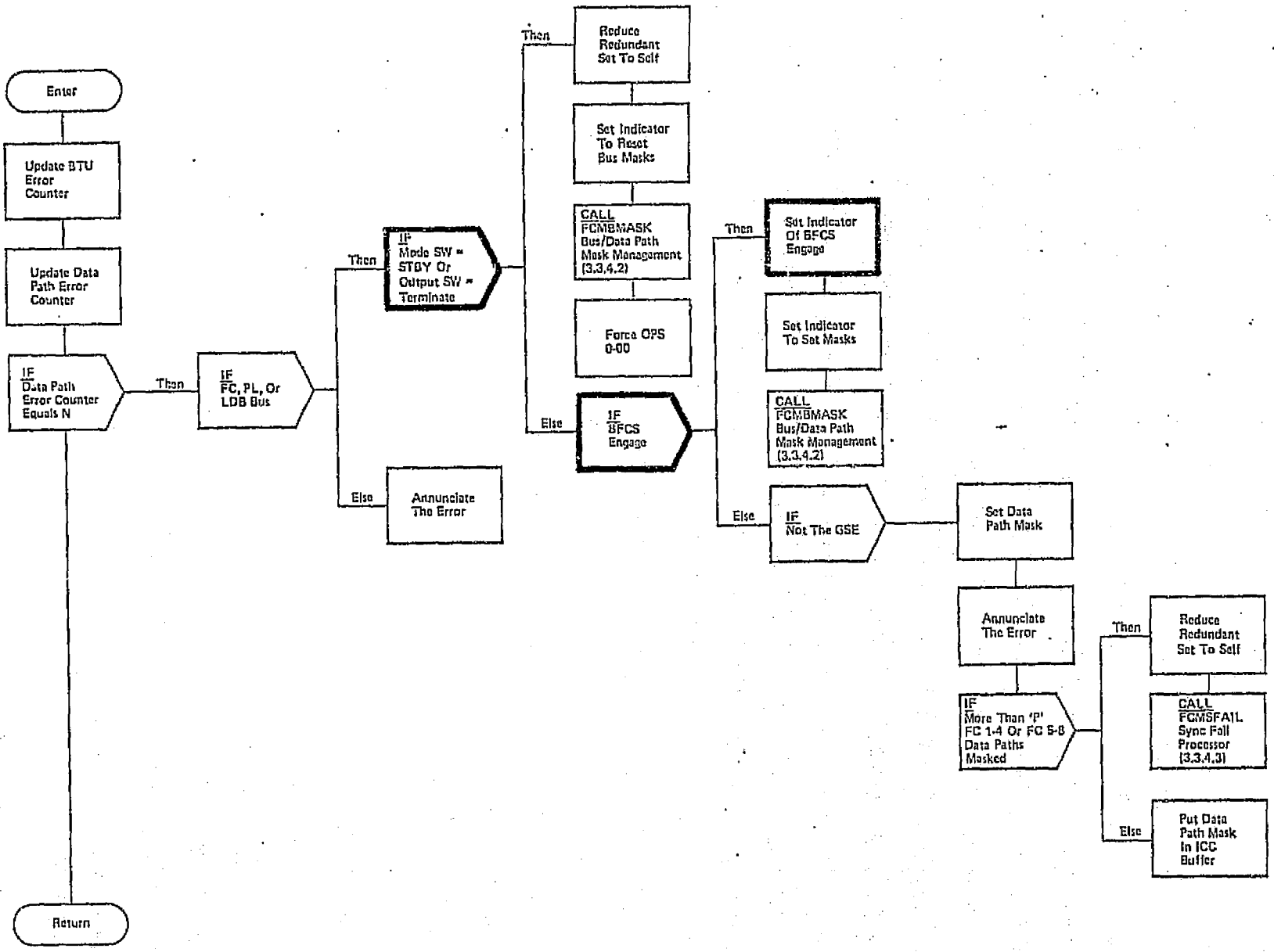


Figure 3-6. Count Data Path Error Procedure (FIOCTDPE)

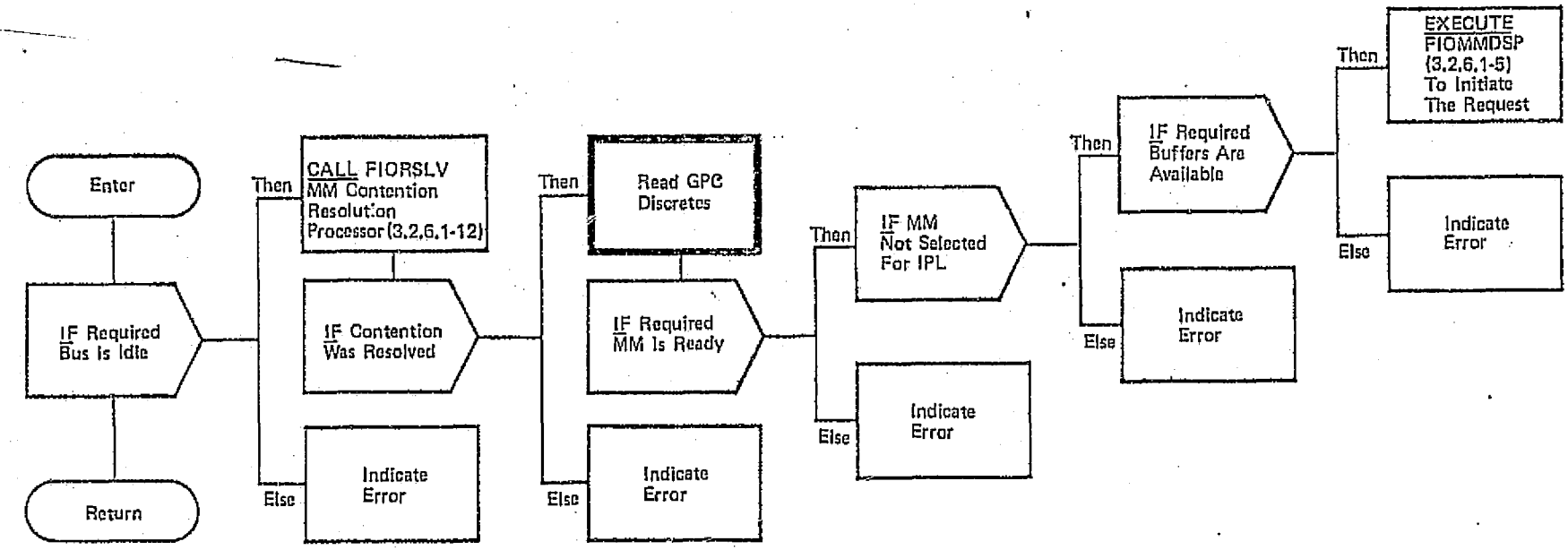


Figure 3-7. MM Management Subroutine FIOMMSTR

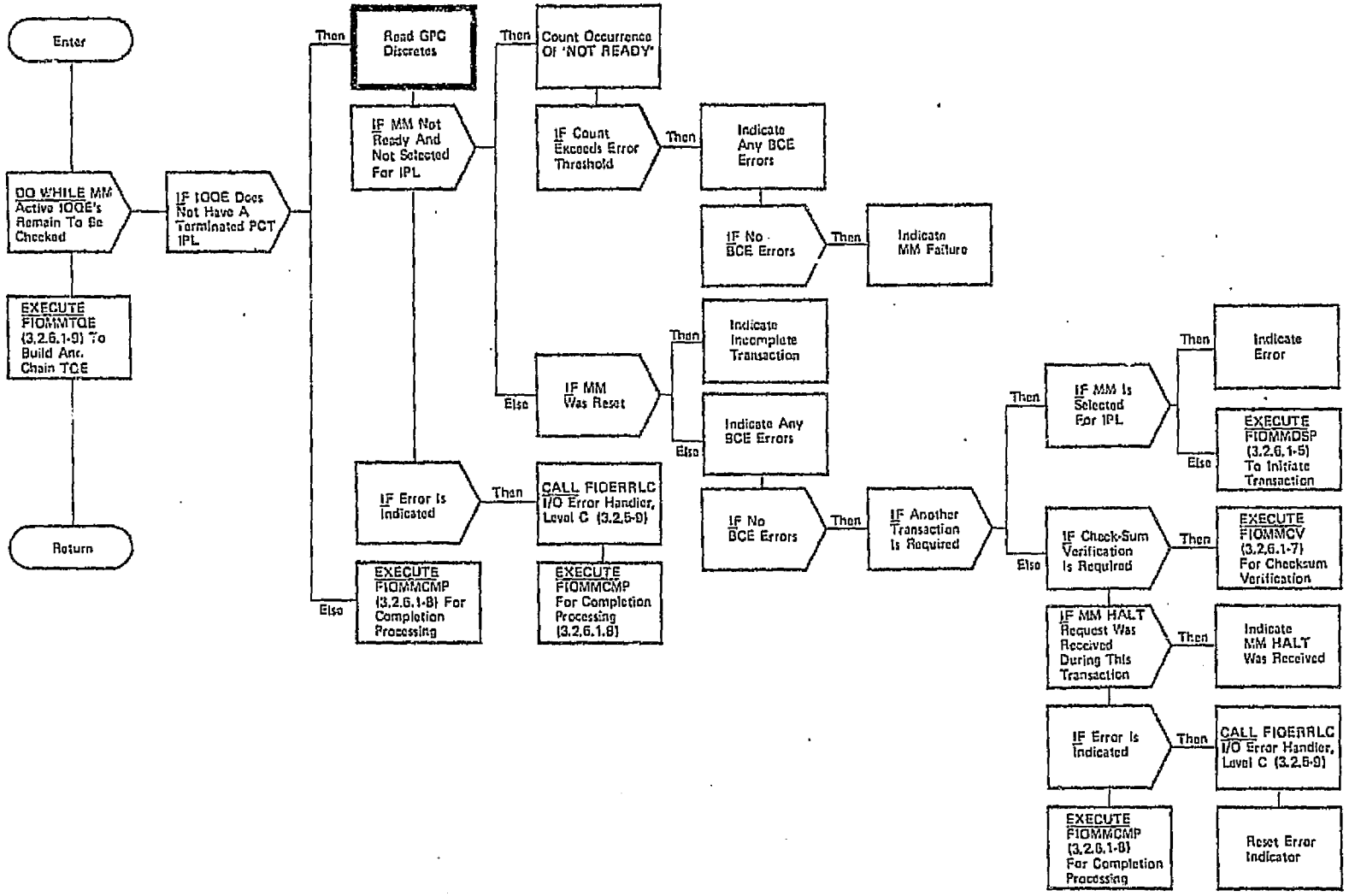


Figure 3-8. MM Management Subroutine FIOMMTMR

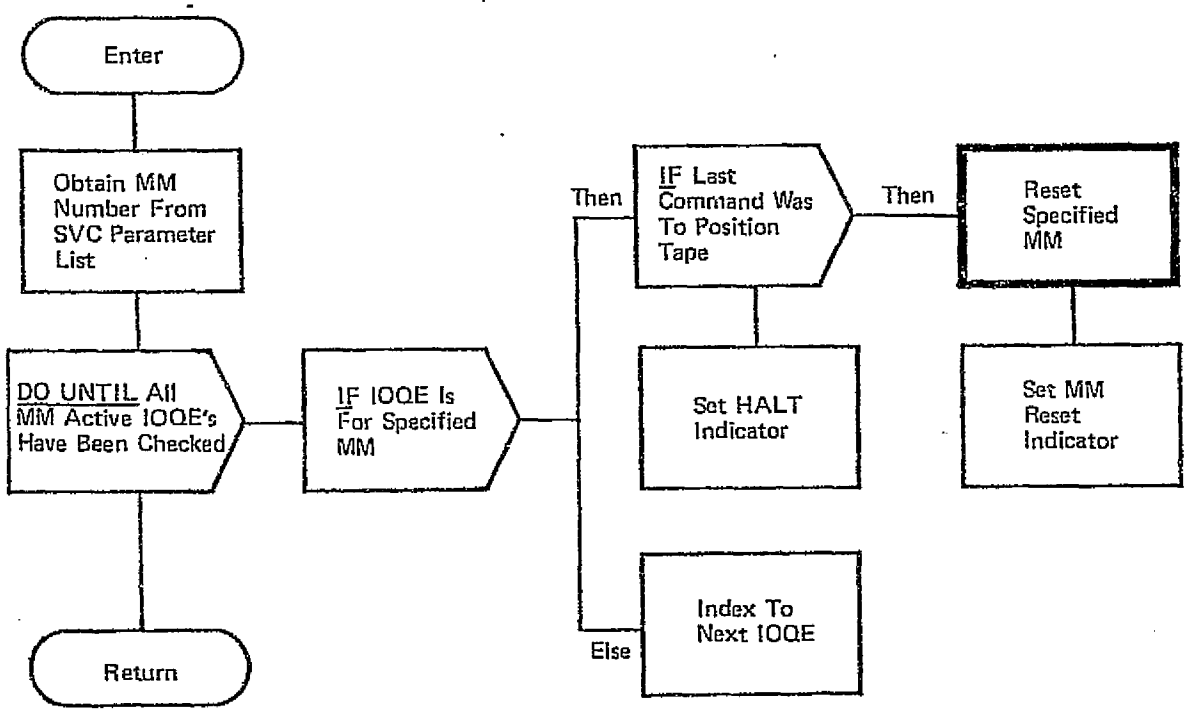


Figure 3-9. Mass Memory Halt Processor (FIOHLTMM)

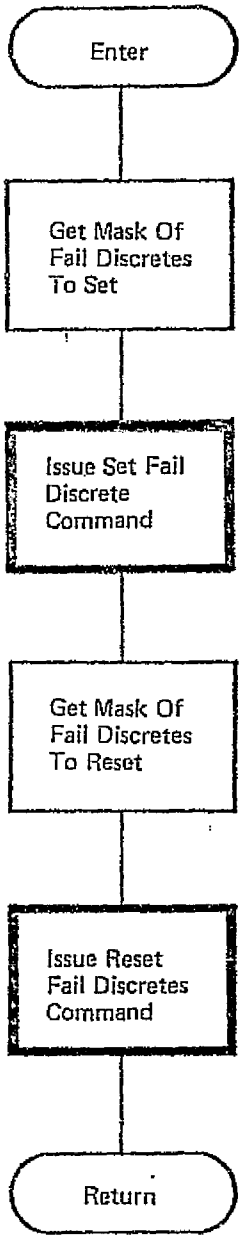


Figure 3-10. MSC Set Fail Discretes Program (FIOMSFD)

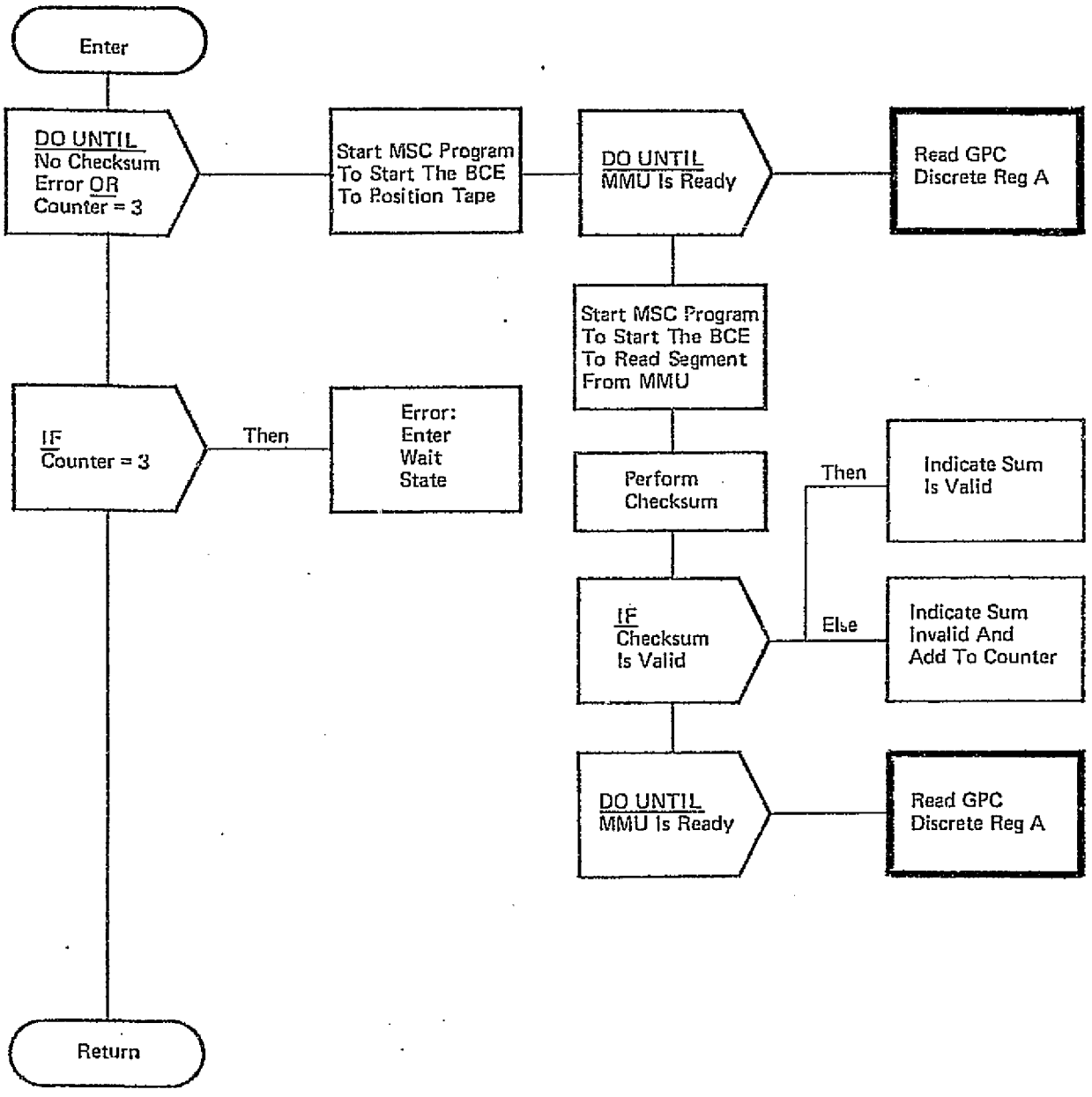


Figure 3-11. Read Blocks from Mass Memory Routine (FCMINMMR)

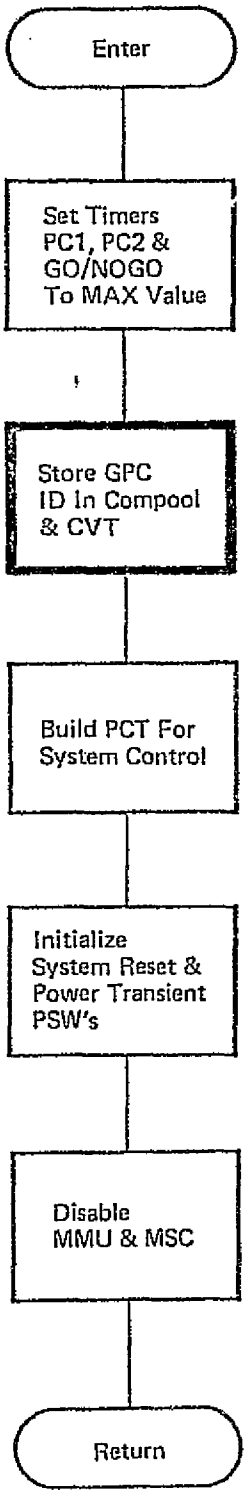


Figure 3-12. One Time Initialization Routine (FCMLINIT)

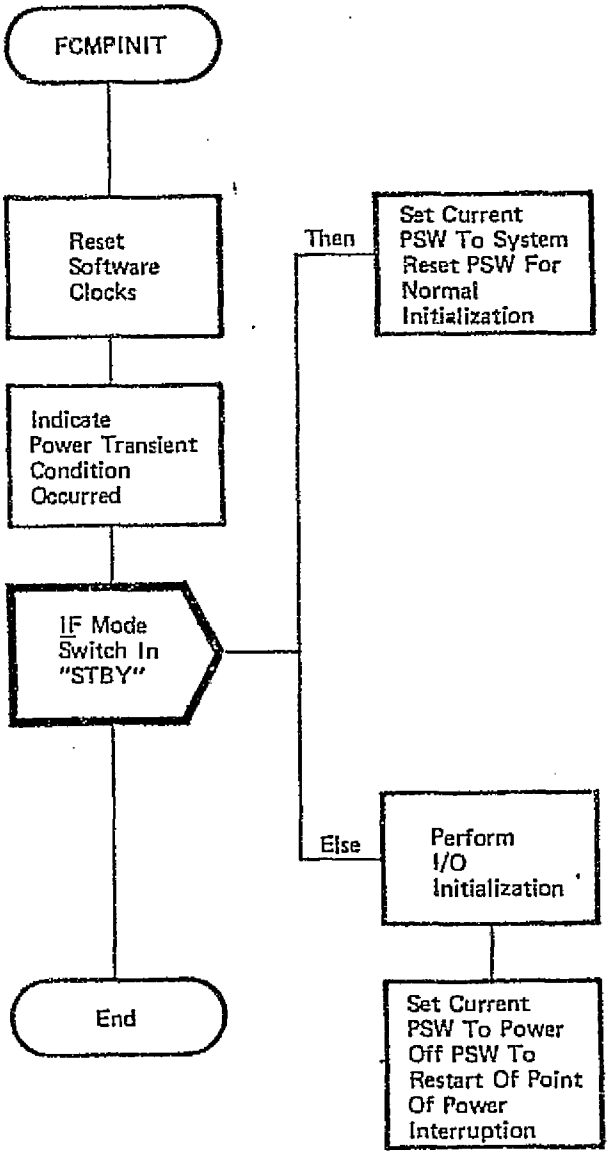


Figure 3-13. Power Transient Initialization Flowchart (FCMPINIT)

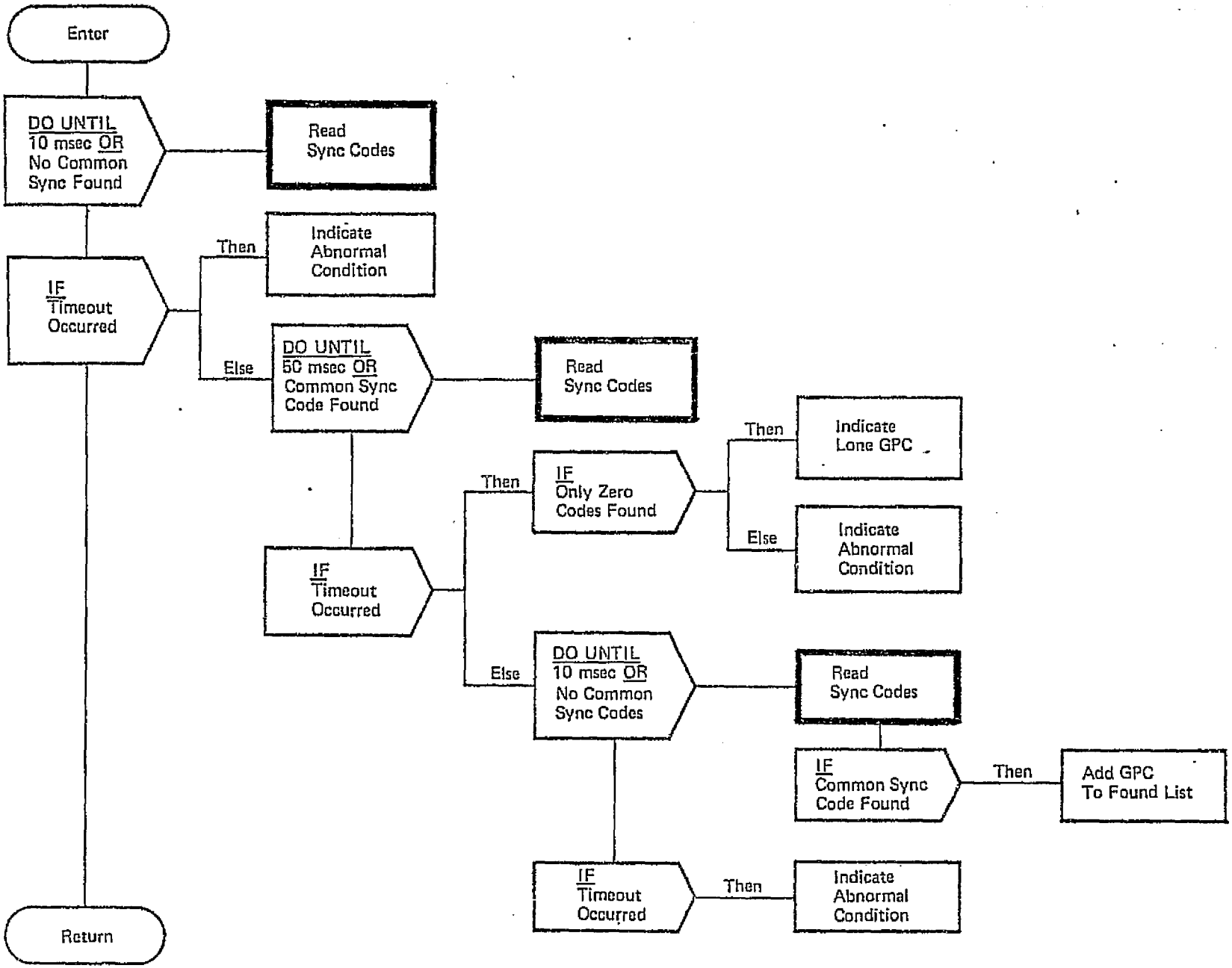


Figure 3-14. Initial SSIP Synchronization (FCMASYNC)

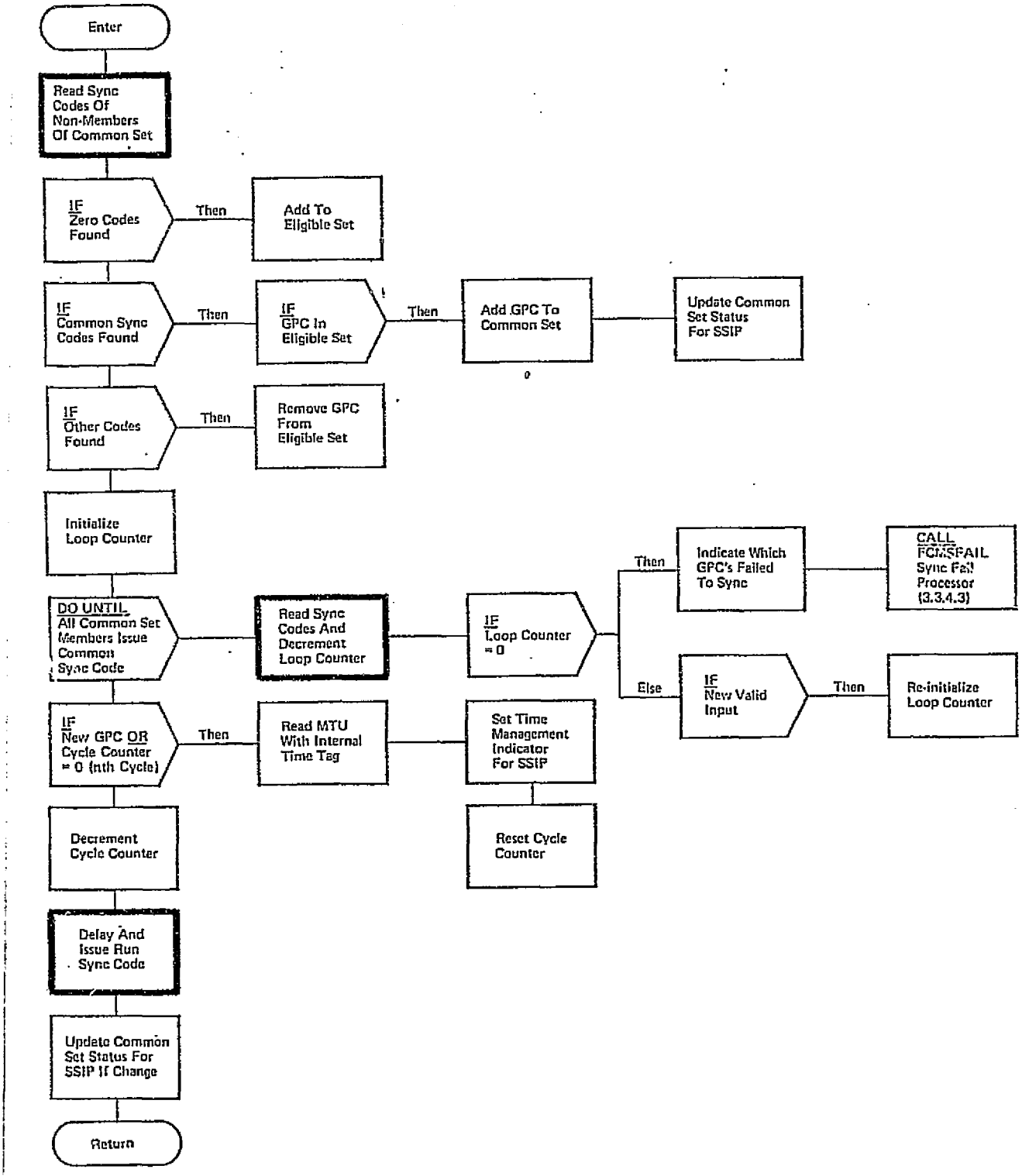


Figure 3-15. Normal SSIP Synchronization (FCMSYNC)

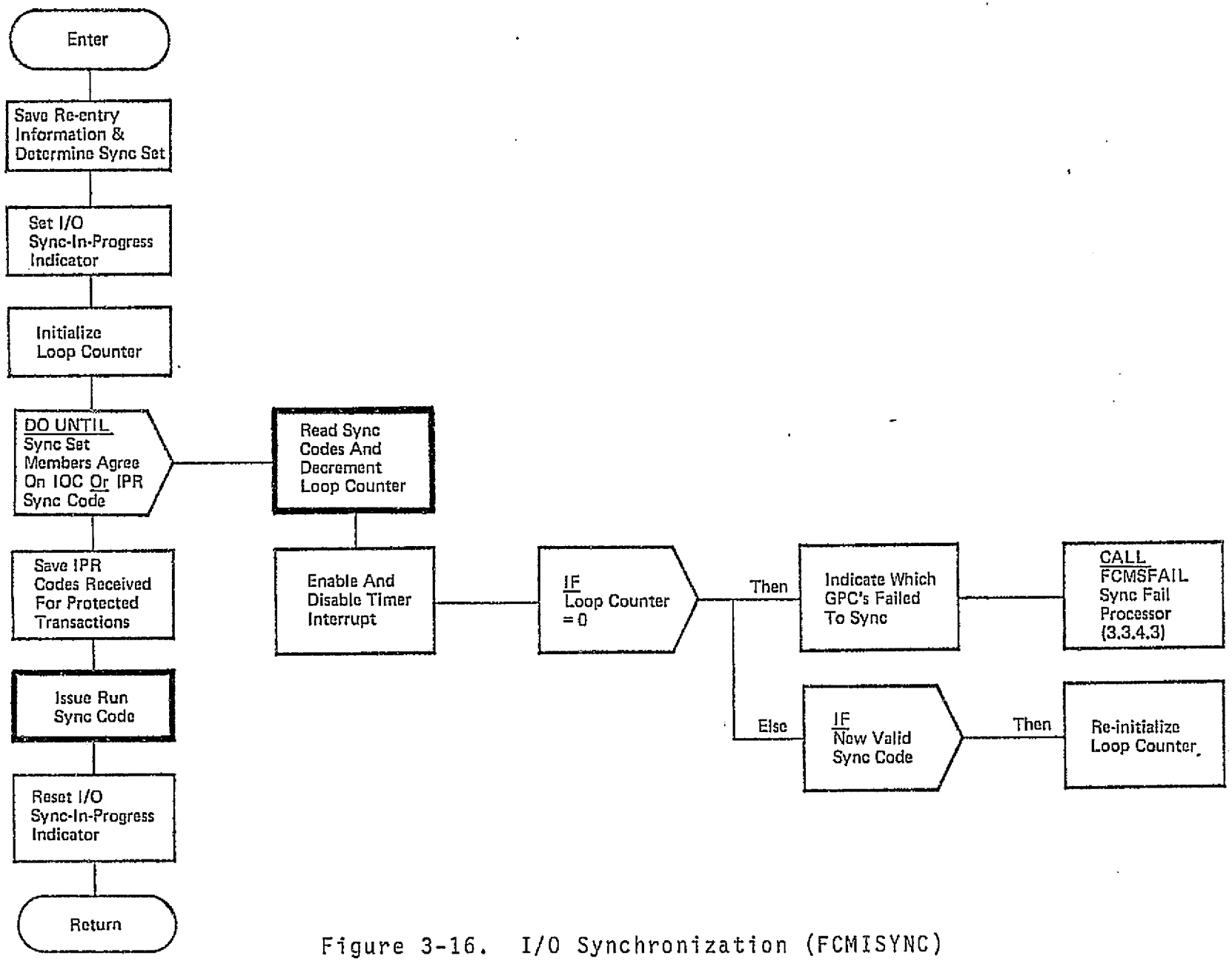


Figure 3-16. I/O Synchronization (FCMISYNC)

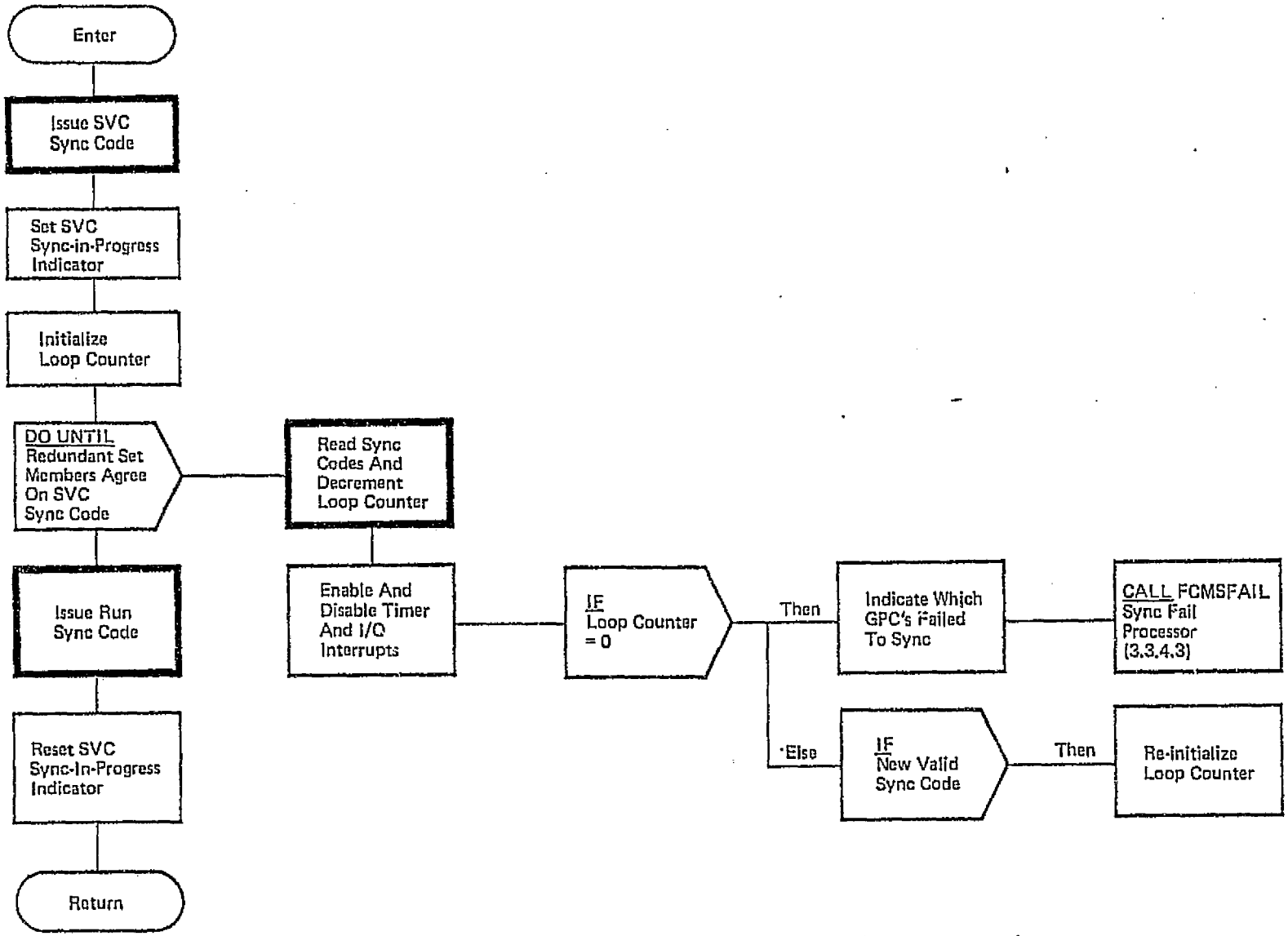


Figure 3-17. SVC Synchronization (FCMMSSYNC)

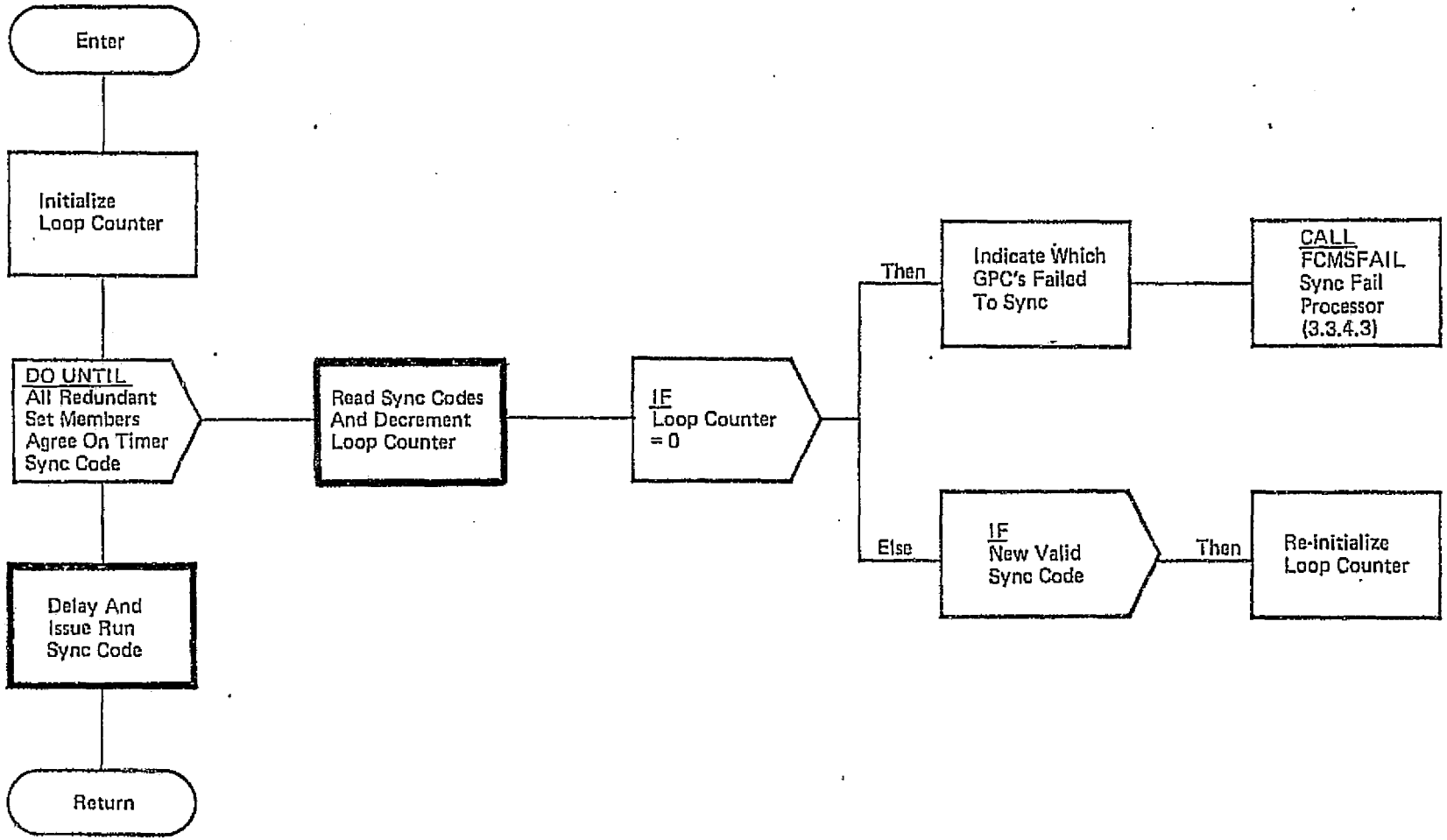


Figure 3-18. Timer Synchronization (FCMSSYNC)

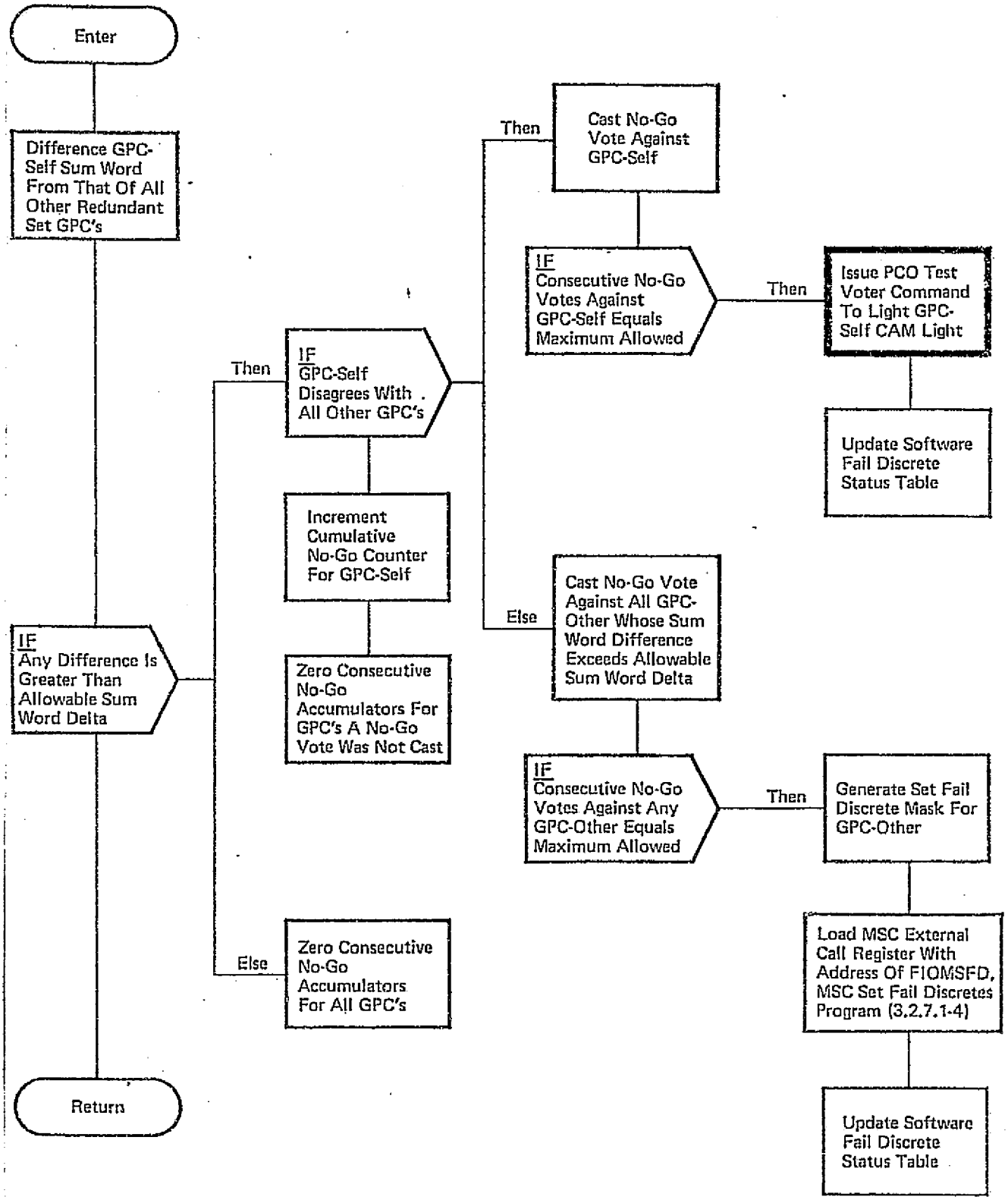


Figure 3-19. Fault Detection Identification (FCMFDI)

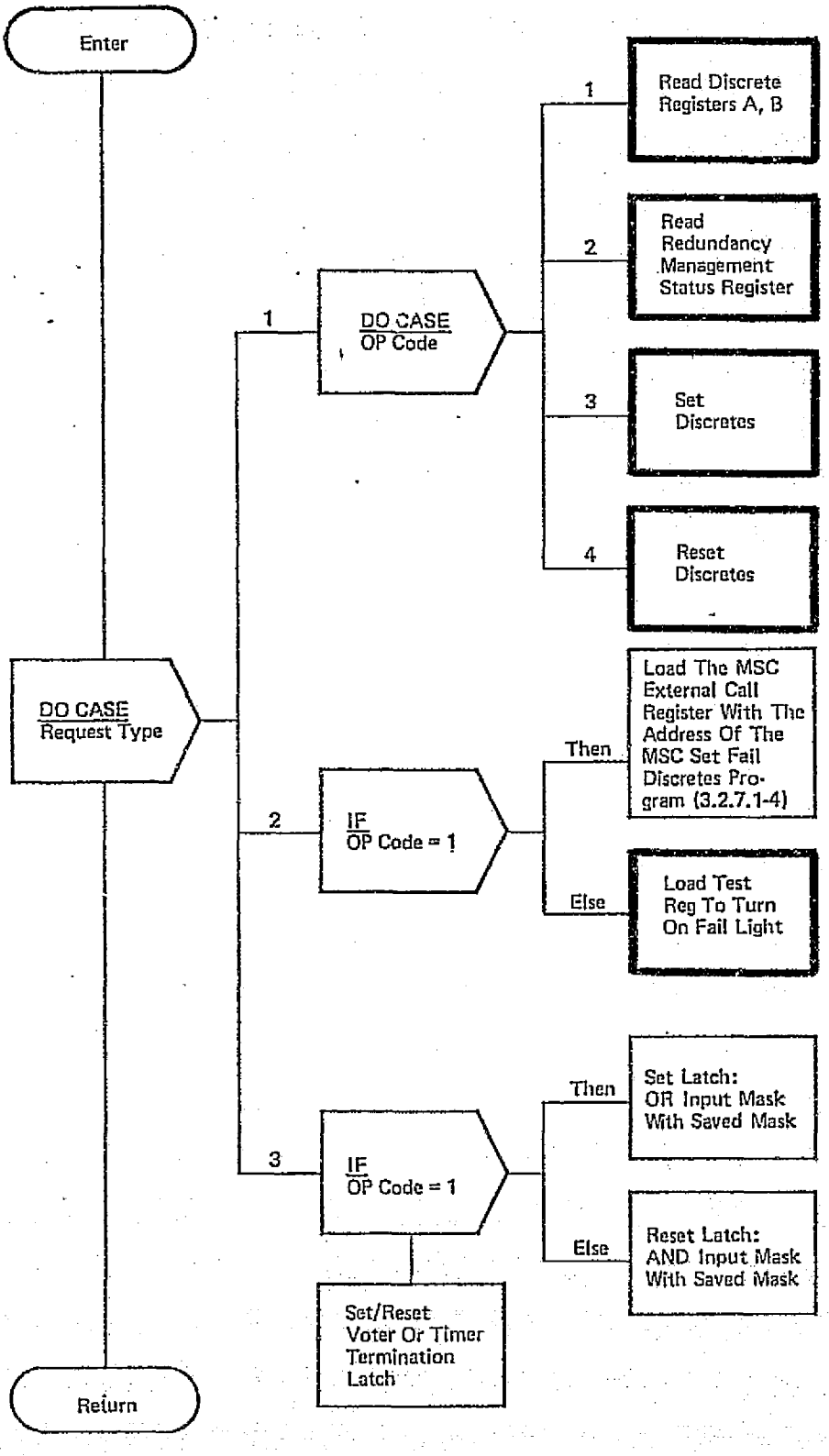


Figure 3-20. Configuration Management SVC Servicing (FCMSVC)

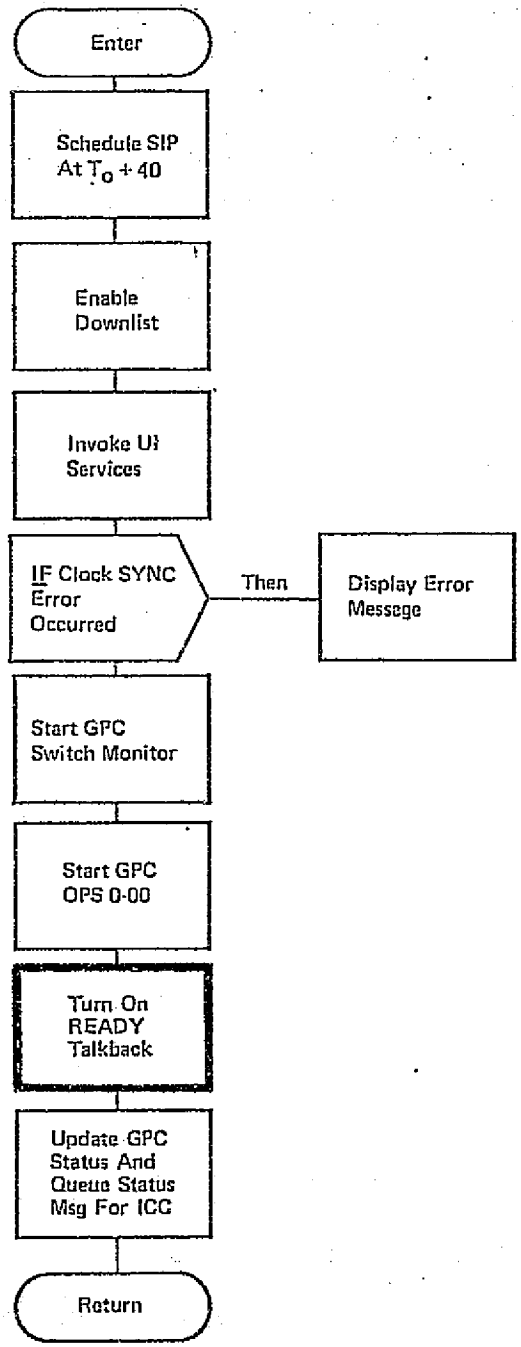


Figure 3-21. GPC Startup (AIC_GPC_STARTUP)

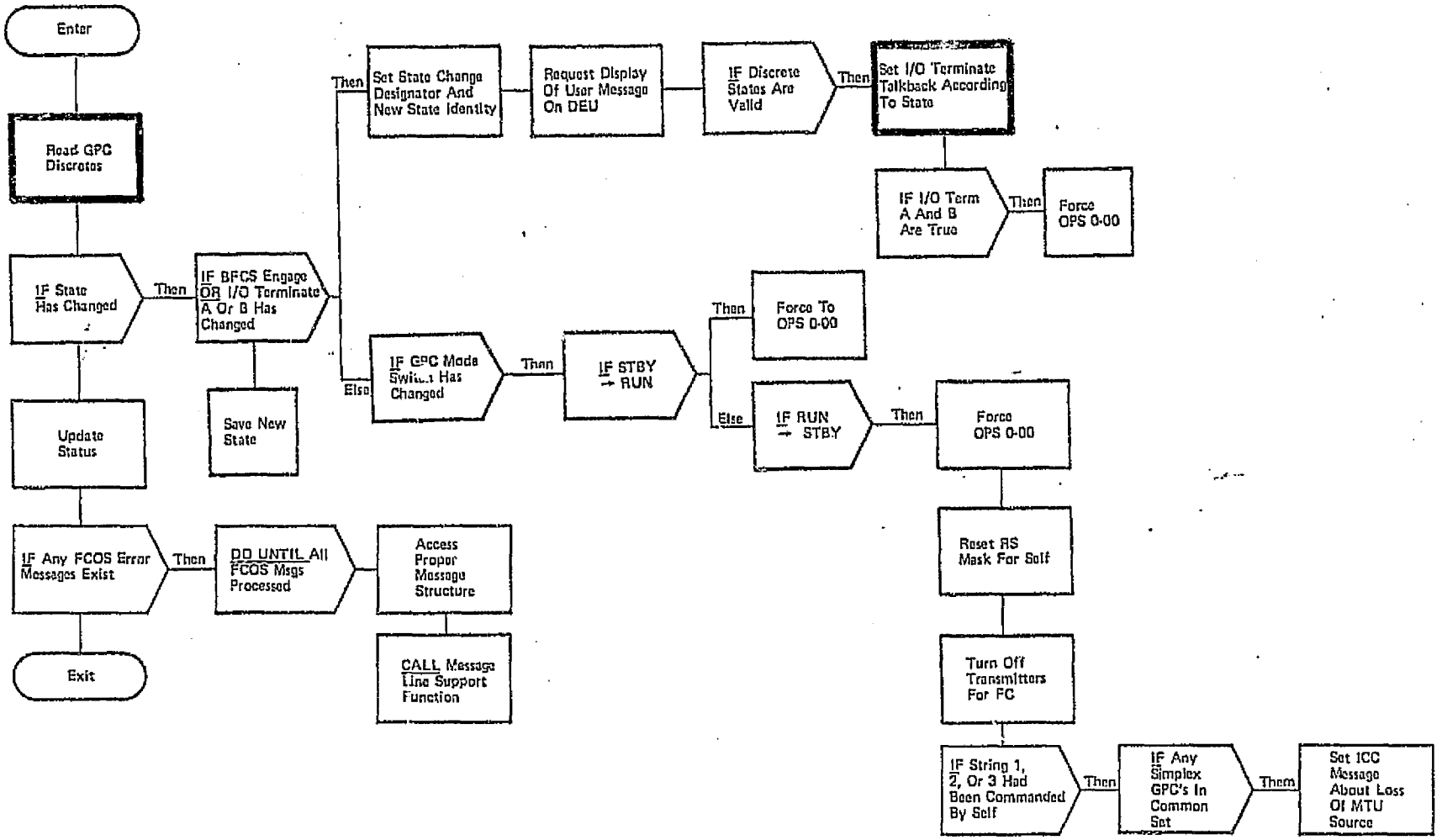


Figure 3-22. GPC Switch Monitor (ARA_GPC_SWITCH)

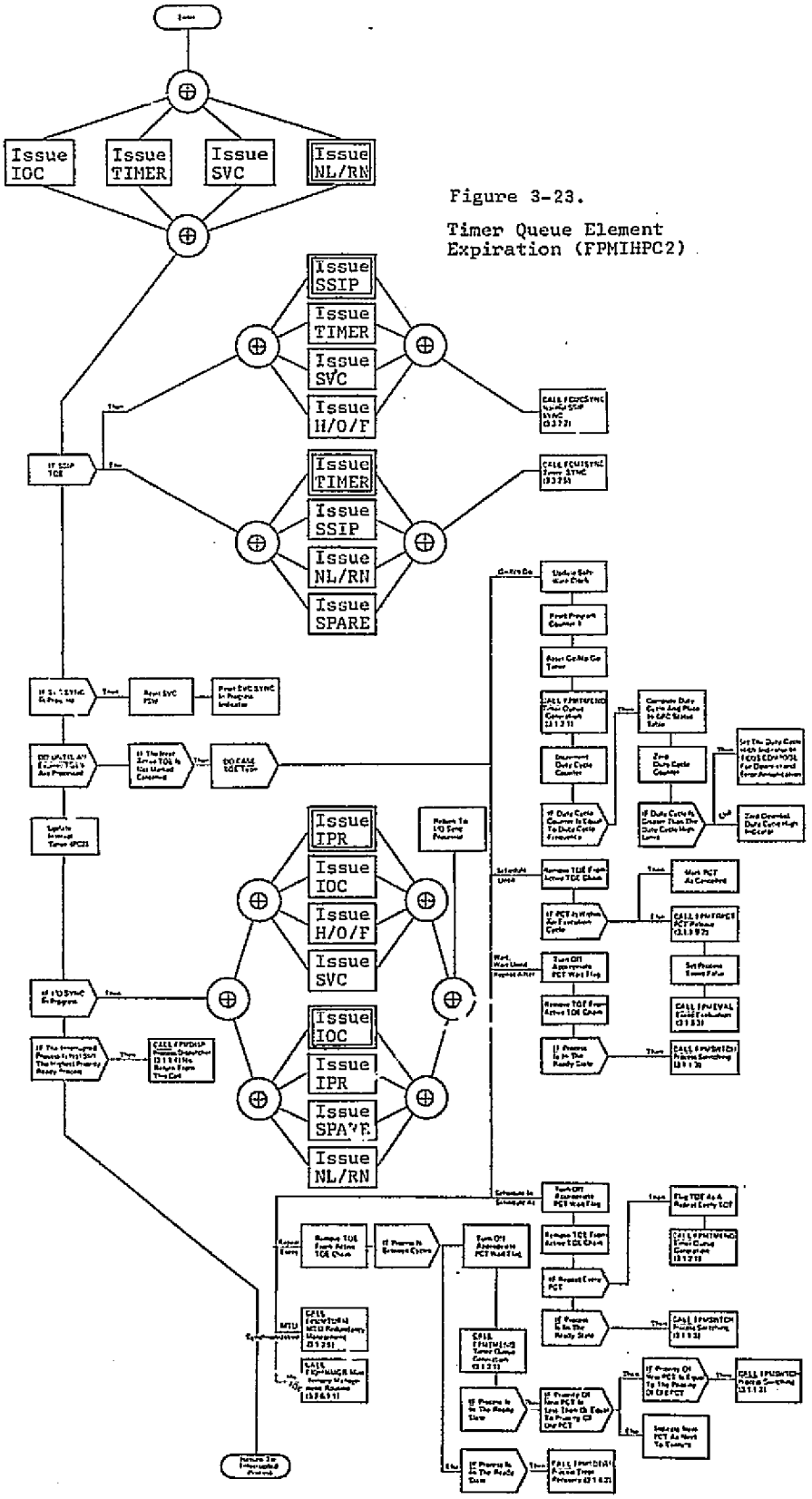


Figure 3-23.

Timer Queue Element Expiration (FPMIHPC2)

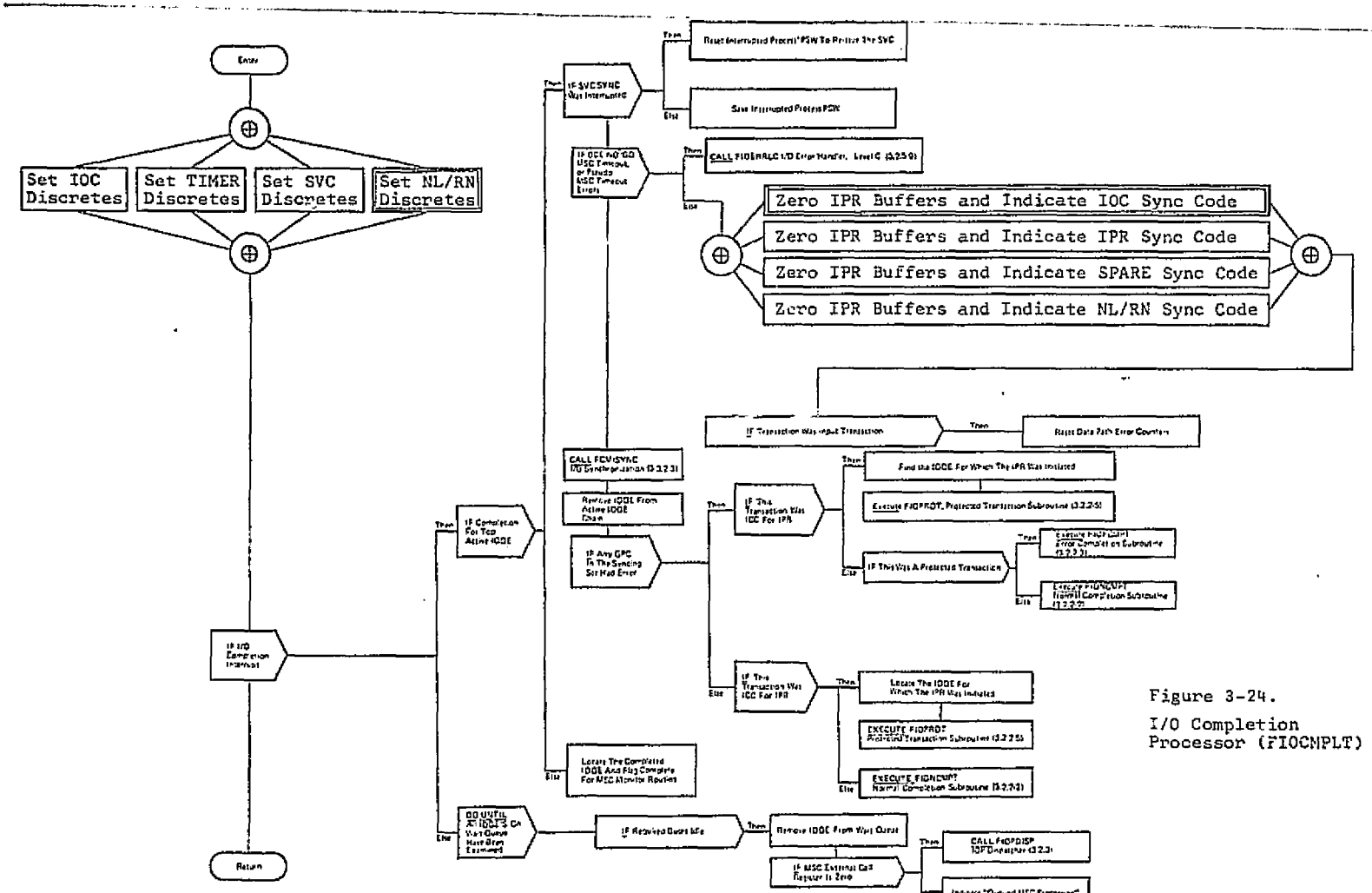


Figure 3-24.

I/O Completion Processor (FIOCNPLT)

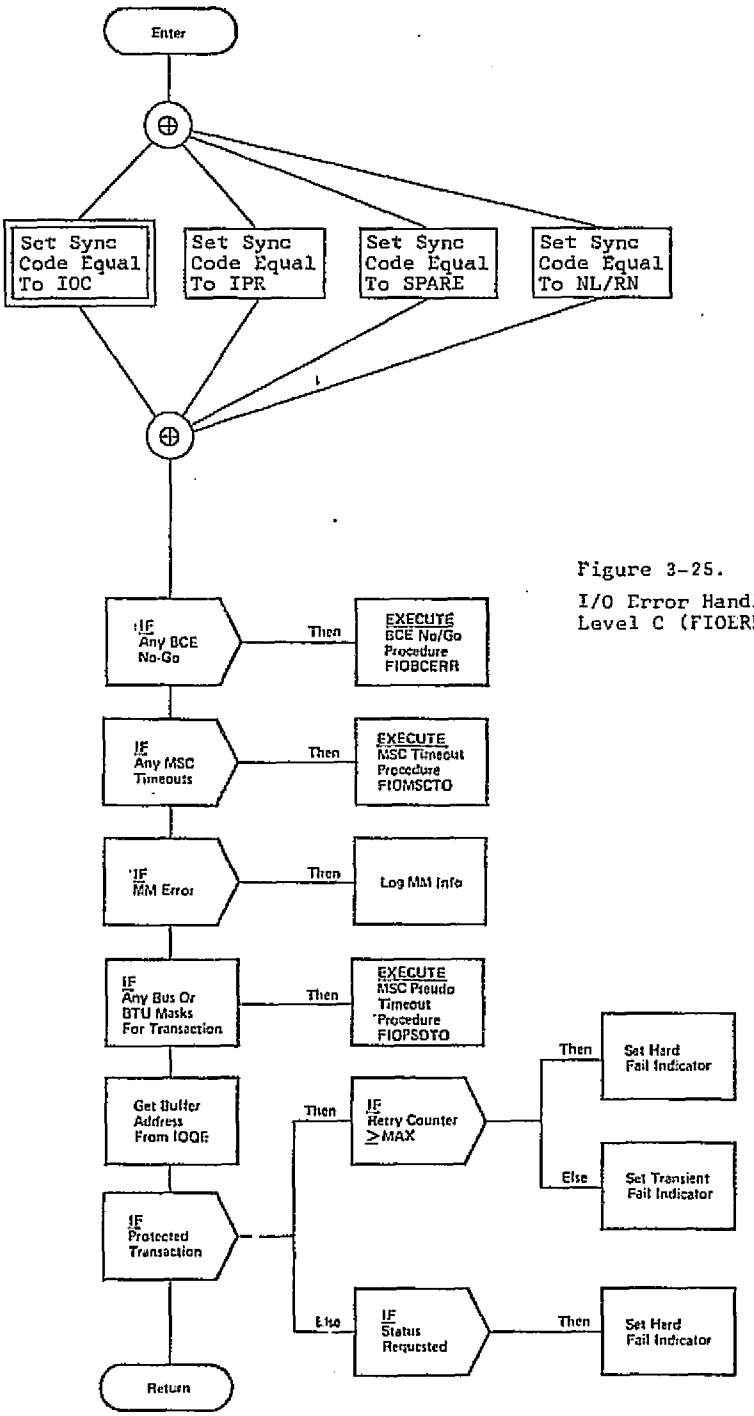


Figure 3-25.
I/O Error Handler, Level C (FIOERRLC)

Figure 3-26.

BCE No Go Procedure
(FIOBCERR)

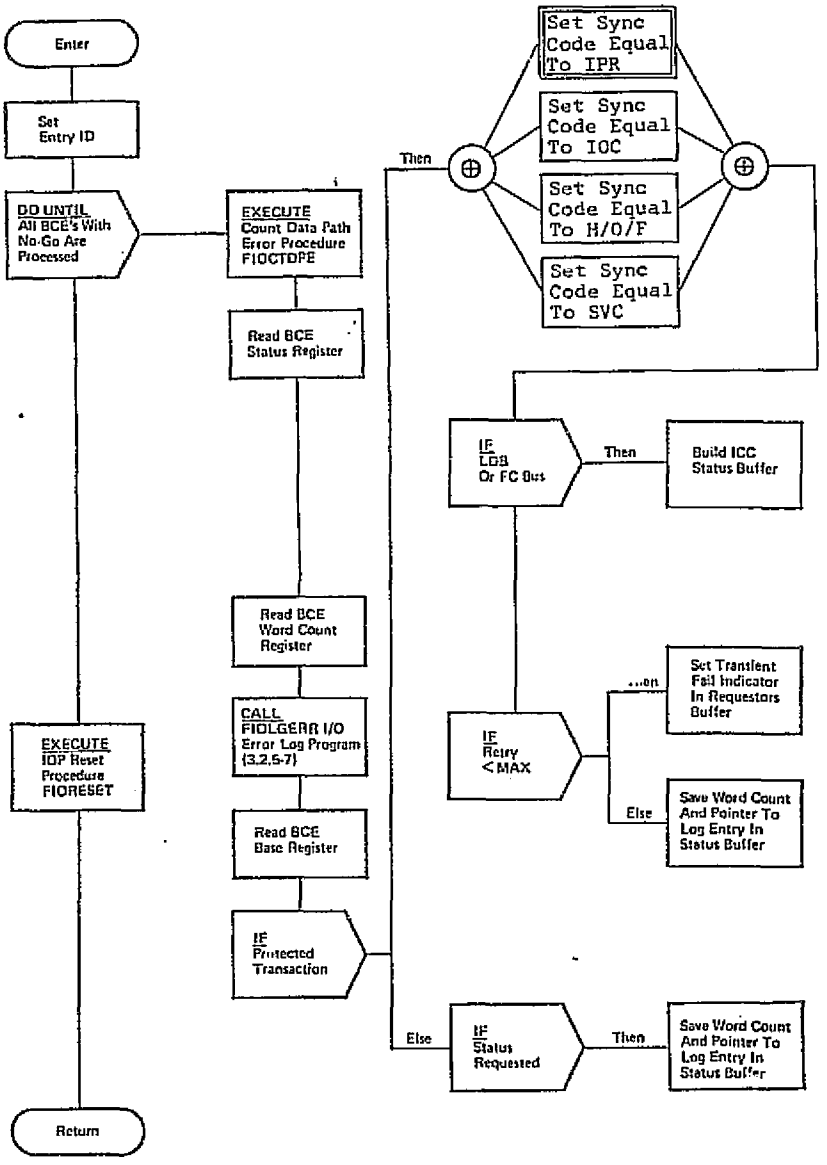
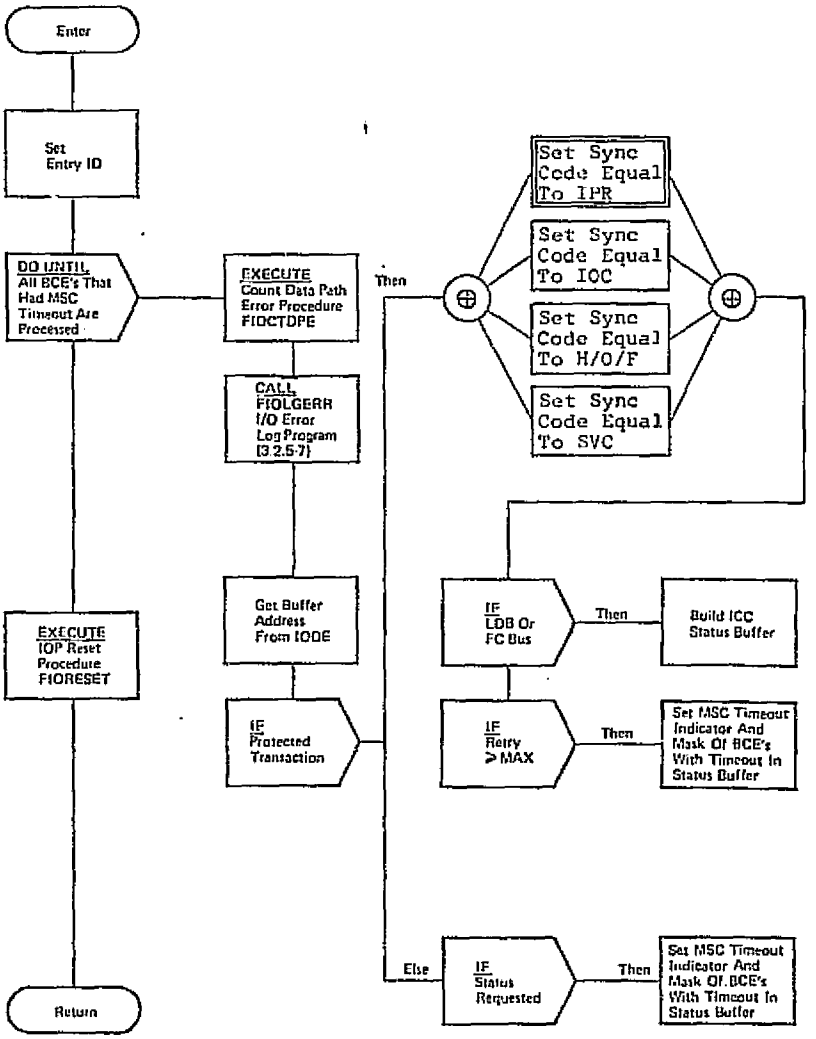


Figure 3-27.
MSC Timeout Procedure (FIOMSCTO)



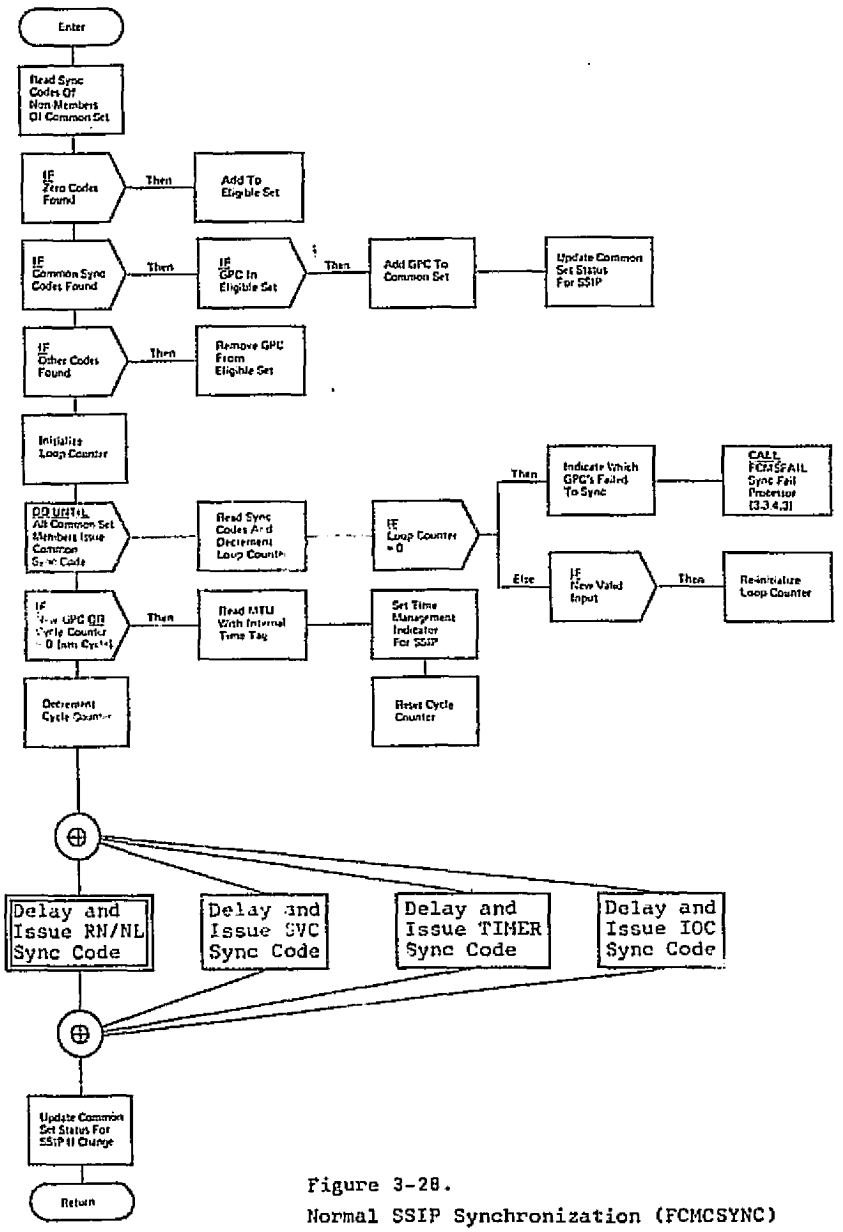


Figure 3-28.
Normal SSIP Synchronization (FCMCSYNC)

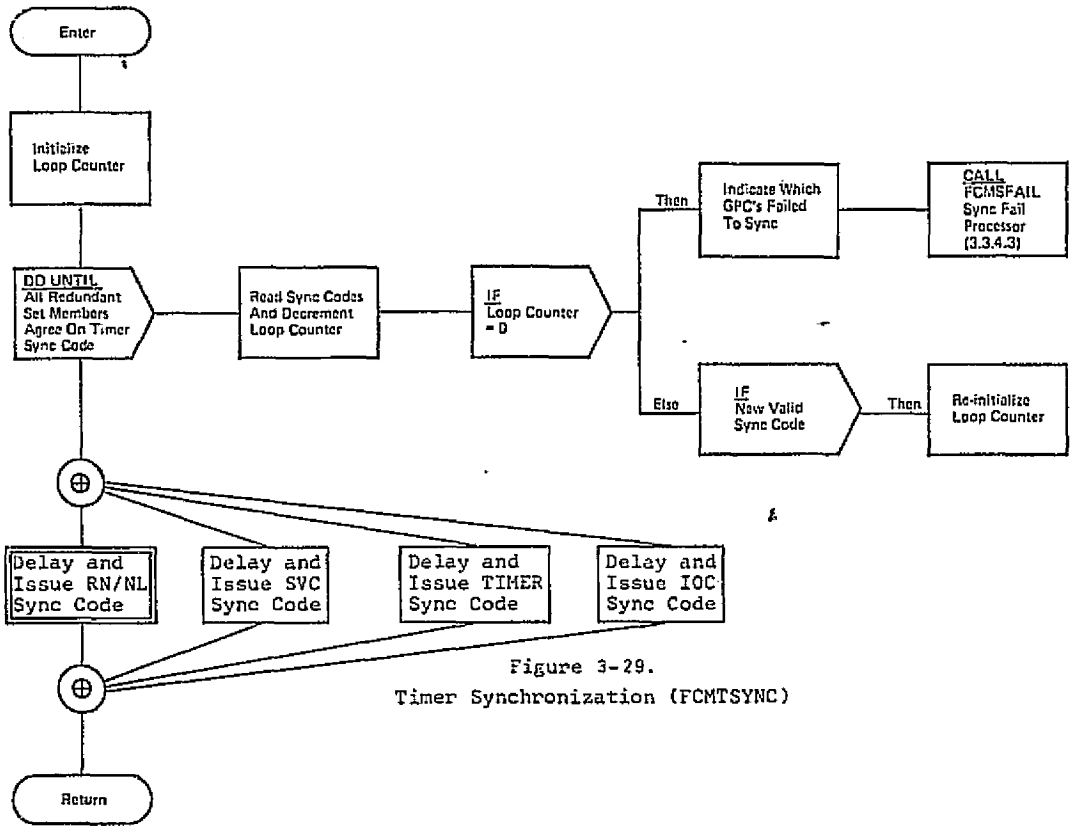


Figure 3-29.
Timer Synchronization (FCMTSYNC)

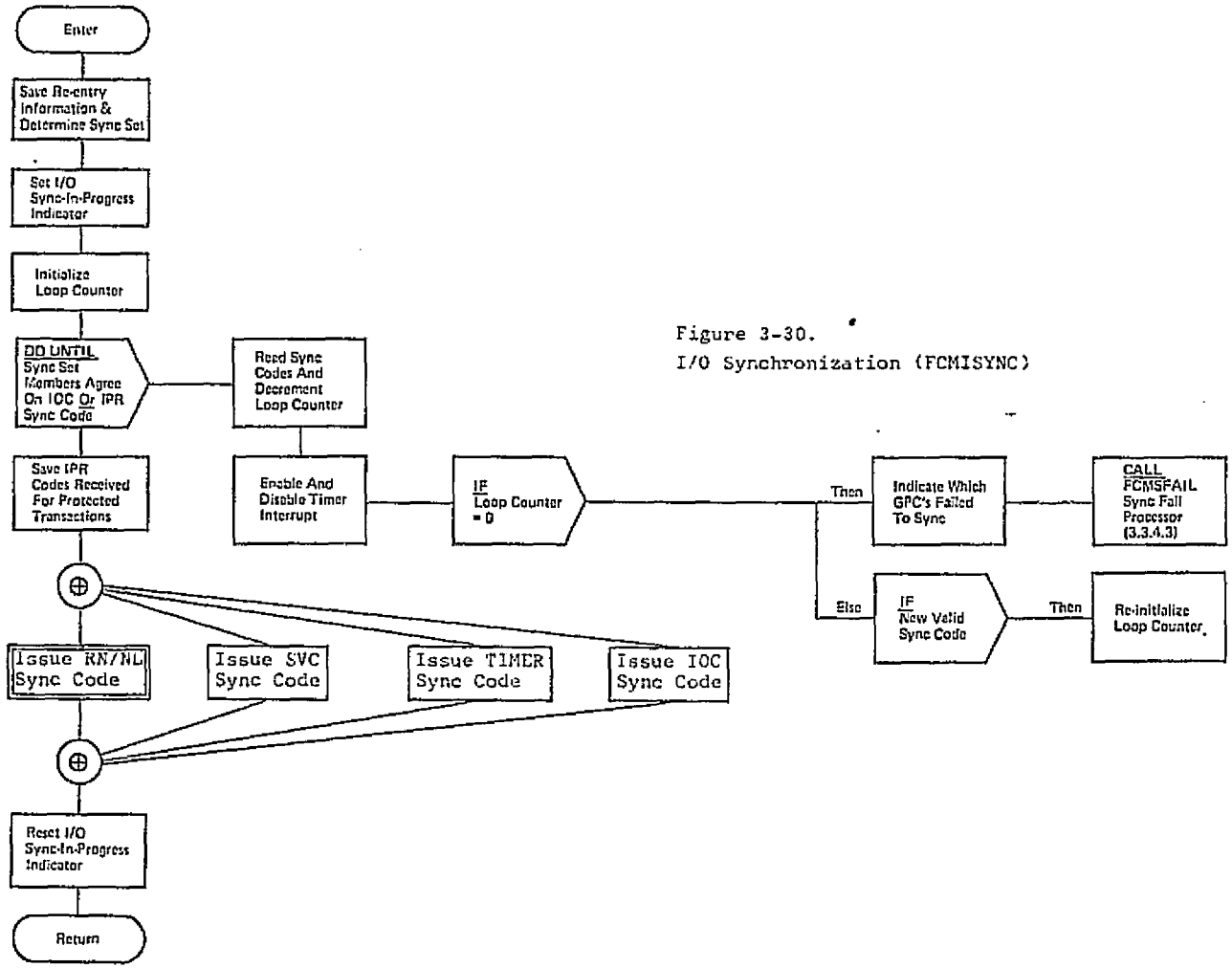


Figure 3-30.
I/O Synchronization (FCMISYNC)

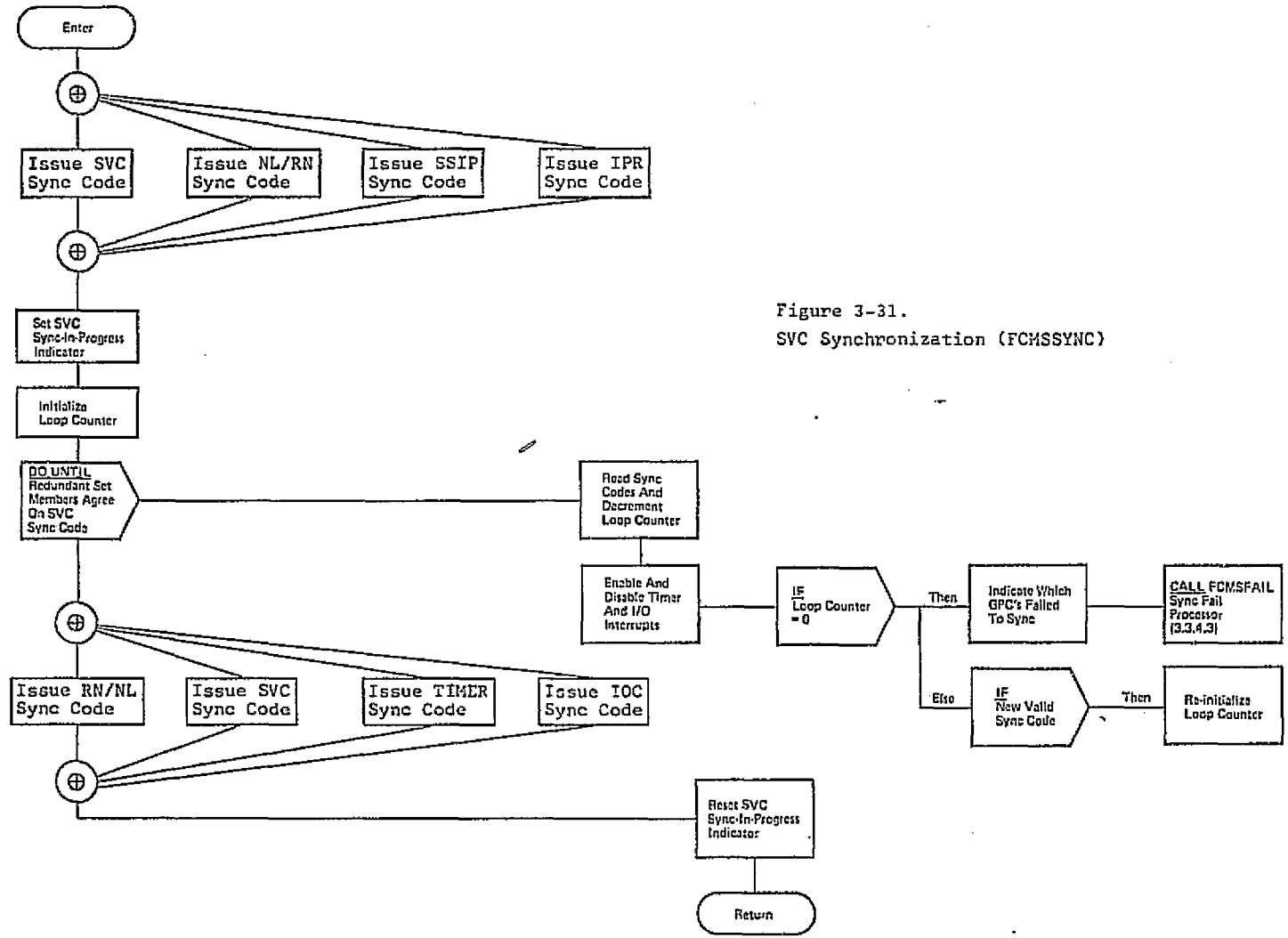


Figure 3-31.
SVC Synchronization (FCMSSYNC)

in the flow-chart of the Timer Queue Element Expiration (FPMIHPC2) module, at the beginning instead of issuing the NL/RN synchronization command, the module may issue IOC, TIMER or SVC synchronization commands. Table 4 summarizes the effects of single discrete errors on the FCOS modules by listing each module that uses/issues discretes along with the manner of invocation of the module and the discretes (identified by their labels and pin numbers) that the module uses/issues. It also lists the possible misinterpretation of discretes due to single bit discrete errors.

In the following, each discrete is considered individually to analyze its precise role in the DPS and how its failure can affect the system performance. The discussion will be qualitative and establish the relative criticality of each discrete. The discrete is analyzed by listing the FCOS modules it is used in, describing qualitatively the manner in which the discrete is used in software logic, and depicting consequences that may ensue because of the discrete failure. In addition, an estimate is given of the time that may elapse before the failure is detected.

3.1 Identification Discrete Failures

These discretes are used by the following software modules directly or indirectly:

Module	Page No. [5]	Usage
FIOMMRLV	3.2-61, Part 1	Indirect
FCMLINIT	3.3-11, Part 1	Direct
FCMDSSTR	3.3074, Part 1	Indirect
FCMRELST	3.3-75, Part 1	Indirect
FCMENSTR	3.3-77, Part 1	Indirect
FCMSATCN	3.3-81, Part 1	Indirect
FCMSFAIL	3.3-89, Part 1	Indirect
ARC_GPC_RECONFIG	3.2-19, Part 2	Indirect

The hardware discretes are read directly by the One Time Initialization Routine, FCMLINIT, and the identification number of the GPC is stored in COMPOOL and CVT. Thereafter, the identification number is fetched whenever needed from these two tables. This number is used in software mostly to select the prime GPC among the Redundant Set. At hardware level, the identification number is used to assign proper control of data buses to the GPC. For example, the five ICC buses, each dedicated to one GPC, are physically

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR IS-SUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTER-PRETED AS
			1						NULL SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	1 1 1	3 IOPS	SPARE IPR SYNC SSIP SYNC
			2						SSIP SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	0 0 1	3 IOPS	TIMER SYNC SVC SYNC HLT/OFF/FL
1-3.1-49	FPMIHPC2	PSW SWAP FROM HARDWARE VIA PROG. CNTR. 2 INTERRUPT	2	NONE	N/A	N/A	N/A	N/A	TIMER SYNC	OR DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	1 0 1	3 IOPS	SSIP SYNC NULL/RUN SPARE
			3						IOC SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	1 1 0	3 IOPS	IPR SYNC SPARE NULL/RUN
			3							OR DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	0 1 0	3 IOPS	IOC SYNC HLT/OFF/FL SVC SYNC

Table 4. List of discretes used/issued by the FCOS modules

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR ISSUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTERPRETED AS
1-3.2-12A	FIOCMPLT	SOFTWARE GENERATED HARDWARE IOP IRPT	1	NONE	N/A	N/A	N/A	N/A	NULL SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	1 1 1	3 IOPS	SPARE IPR SYNC SSIP SYNC
			2						IOC SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	1 1 0	3 IOPS	IPR SYNC SPARE NULL/RUN
1-3.2-34	FIOERRLC	CALL FROM FIOCMPLT OR FIOMMMGR	1	NONE	N/A	N/A	N/A	N/A	IOC SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	1 1 0	3 IOPS	IPR SYNC SPARE NULL/RUN
1-3.2-37	FIOBCERR	EXECUTED FROM FIOERRLC	1	NONE	N/A	N/A	N/A	N/A	IPR SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	0 1 0	3 IOPS	IOC SYNC HLT/OFF/FL SVC SYNC
1-3.2-39	FIOMSCTO	EXECUTED FROM FIOERRLC	1	NONE	N/A	N/A	N/A	N/A	IPR SYNC	DO20 DO24 DO28	J3-43,44 J3-34,35 J3-46,47	0 1 0	3 IOPS	IOC SYNC HLT/OFF/FL SVC SYNC
1-3.2-43	FIOCTDPE	EXECUTED FROM FIOBCERR OR FIOMSCTO	1	STANDBY	DI01	J5-3,4	1	PANEL	NONE	N/A	N/A	N/A	N/A	N/A
			2	TERMINATE	DI00	J5-1,2	1	PANEL						
			3	BFCS ENGAGE	DI11	J5-23,24	1	PANEL						

Table 4 (continued). List of discretes used/issued by the FCOS modules

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR IS-SUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTER-PRETED AS
1-3.2-52	FIOMMSTR	EXECUTED FROM FIOMMPII	1	MM1 READY	DI06	J5-12,13	?	MM1	NONE	N/A	N/A	N/A	N/A	N/A
			1	MM2 READY	DI07	J5-15,16	?	MM2						
			2	MM1 IPL SEL	DI04	J5-8,9	?	PANEL						
			2	MM2 IPL SEL	DI05	J5-10,11	?	PANEL						
1-3.2-54	FIOMMTMR	EXECUTED FROM FIOMMMGR	1	MM1 READY	DI06	J5-12,13	?	MM1	NONE	N/A	N/A	N/A	N/A	N/A
			1	MM2 READY	DI07	J5-15,16	?	MM2						
			2	MM1 IPL SEL	DI04	J5-8,9	?	PANEL						
			2	MM2 IPL SEL	DI05	J5-10,11	?	PANEL						
1-3.2-59	FIOHLTMM	CALL FROM FPMSVC	1	NONE	N/A	N/A	N/A	N/A	MM1 RESET	DO12	J3-8,16	?	MM1	CONTINUE
			1						MM2 RESET	DO13	J3-17,27	?	MM2	CONTINUE
1-3.2-80	FIOMSFD	CALL FROM FCMSVC OR FCMFDI	1	NONE	N/A	N/A	N/A	N/A	N+1 FAIL	DR007	J5-44,45	?	IOP N+1	NOT FAILED
			1						N+2 FAIL	DR008	J5-42,43	?	IOP N+2	NOT FAILED
			1						N+3 FAIL	DR009	J5-40,41	?	IOP N+3	NOT FAILED
			1						GPC FAIL	DR000	J5-46,58	?	PANEL	NOT FAILED
1-3.3-10	FCMINMMR	EXECUTED FROM FCMINSSL	1	MM1 READY	DI06	J5-12,13	?	MM1	NONE	N/A	N/A	N/A	N/A	N/A
			1	MM2 READY	DI07	J5-15,16	?	MM2						
1-3.3-11	FCMLINIT	EXECUTED FROM FCMINSSL	1	GPC ID BIT0	DI32	J3-74,75	?	IOP N	NONE	N/A	N/A	N/A	N/A	N/A
			1	GPC ID BIT1	DI33	J3-116,123	?	IOP N						
			1	GPC ID BIT2	DI34	J3-107,122	?	IOP N						

Table 4 (continued). List of discretes used/issued by the FCOS modules

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR ISSUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTERPRETED AS
1-3.3-17	FCMPINIT	POWER ON WITH MODE SWITCH IN RUN OR STDBY	1	STANDBY	DI01	J5-3,4	1	PANEL	NONE	N/A	N/A	N/A	N/A	N/A
1-3.3-23	FCMASYNC	FPMSVC CALL	1	GPC N+1 SB1	DI20	J3-80,91	?	IOP N+1						
			1	GPC N+2 SB1	DI21	J3-92,104	?	IOP N+2						
			1	GPC N+3 SB1	DI22	J3-103,114	?	IOP N+3						
			1	GPC N+1 SB2	DI24	J3-113,121	?	IOP N+1						
			1	GPC N+2 SB2	DI25	J3-112,128	?	IOP N+2	NONE	N/A	N/A	N/A	N/A	N/A
			1	GPC N+3 SB2	DI26	J3-101,111	?	IOP N+3						
			1	GPC N+1 SB3	DI28	J3-119,126	?	IOP N+1						
			1	GPC N+2 SB3	DI29	J3-99,109	?	IOP N+2						
			1	GPC N+3 SB3	DI30	J3-118,125	?	IOP N+3						
1-3.3-25	FCMCSYNC	FPMIHPC2 CALL	1	GPC N+1 SB1	DI20	J3-80,91	?	IOP N+1						
			1	GPC N+2 SB1	DI21	J3-92,104	?	IOP N+2						
			1	GPC N+3 SB1	DI22	J3-103,114	?	IOP N+3						
			1	GPC N+1 SB2	DI24	J3-113,121	?	IOP N+1						
			1	GPC N+2 SB2	DI25	J3-112,128	?	IOP N+2						
			1	GPC N+3 SB2	DI26	J3-101,111	?	IOP N+3						
			1	GPC N+1 SB3	DI28	J3-119,126	?	IOP N+1						
			1	GPC N+2 SB3	DI29	J3-99,109	?	IOP N+2						
			1	GPC N+3 SB3	DI30	J3-118,125	?	IOP N+3						
			2						GPC N SB1	DO20	J3-43,44	1	3 IOPS	SPARE
			2						GPC N SB2	DO24	J3-34,35	1	3 IOPS	IPR SYNC
			2						GPC N SB3	DO28	J3-46,47	1	3 IOPS	SSIP SYNC

Table 4 (continued). List of discretes used/issued by the FCOS modules

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR ISSUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTERPRETED AS
			1	GPC N+1 SB1	DI20	J3-80,91 ?		IOP N+1						
			1	GPC N+2 SB1	DI21	J3-92,104 ?		IOP N+2						
			1	GPC N+3 SB1	DI22	J3-103,114?		IOP N+3						
			1	GPC N+1 SB2	DI24	J3-113,121?		IOP N+1						
			1	GPC N+2 SB2	DI25	J3-112,118?		IOP N+2						
1-3.3-29	FCMISYNC	CALL FROM FIOCMPLT OR FIOMMMGR	1	GPC N+3 SB2	DI26	J3-101,111?		IOP N+3						
			1	GPC N+1 SB3	DI28	J3-119,126?		IOP N+1						
			1	GPC N+2 SB3	DI29	J3-99,109 ?		IOP N+2						
			1	GPC N+3 SB3	DI30	J3-118,125?		IOP N+3						
			2						GPC N SB1	DO20	J3-43,44	1	3 IOPS	SPARE
			2						GPC N SB2	DO24	J3-34,35	1	3 IOPS	IPR SYNC
			2						GPC N SB3	DO28	J3-46,47	1	3 IOPS	SSIP SYNC

Table 4 (continued). List of discretes used/issued by the FCOS modules

PAGE REF. NO. 35	MODULE	INVOCATION	SEQ OF USE OR IS-SUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTER-PRETED AS
			1							DO20	J3-43,44	0		NULL/RUN
			1						SVC SYNC	DO24	J3-34,35	1	3 IOPS	SSIP SYNC
			1							DO28	J3-46,47	1		IPR SYNC
			2	GPC N+1 SB1	DI20	J3-80,91 ?		IOP N+1						
			2	GPC N+2 SB1	DI21	J3-92,104 ?		IOP N+2						
		CALL FROM	2	GPC N+3 SB1	DI22	J3-103,114?		IOP N+3						
		SEVERAL MODS.	2	GPC N+1 SB2	DI24	J3-113,121?		IOP N+1						
1-3.3-35	FCMSSYNC	LISTED IN	2	GPC N+2 SB2	DI25	J3-112,128?		IOP N+2						
		REF.52,3.3-28	2	GPC N+3 SB2	DI26	J3-101,111?		IOP N+3						
		FCOS	2	GPC N+1 SB3	DI28	J3-119,126?		IOP N+1						
			2	GPC N+2 SB3	DI29	J3-99,109 ?		IOP N+2						
			2	GPC N+3 SB3	DI30	J3-118,125?		IOP N+3						
			3						GPC N SB1	DO20	J3-43,44	1	3 IOPS	SPARE
			3						GPC N SB2	DO24	J3-34,35	1	3 IOPS	IPR SYNC
			3						GPC N SB3	DO28	J3-46.47	1	3 IOPS	SSIP SYNC

Table 4 (continued). List of discretes used/issued by the FCOS modules

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR ISSUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTERPRETED AS
			1	GPC N+1 SB1	DI20	J3-80,91	?	IOP N+1						
			1	GPC N+2 SB1	DI21	J3-92,104	?	IOP N+2						
			1	GPC N+3 SB1	DI22	J3-103,114	?	IOP N+3						
			1	GPC N+1 SB2	DI24	J3-113,121	?	IOP N+1						
			1	GPC N+2 SB2	DI25	J3-112,128	?	IOP N+2						
			1	GPC N+3 SB2	DI26	J3-101,111	?	IOP N+3						
1-3.3-37	FCMTSYNC	FPMIHPC2 CALL	1	GPC N+1 SB3	DI28	J3-119,126	?	IOP N+1						
			1	GPC N+2 SB3	DI29	J3-99,109	?	IOP N+2						
			1	GPC N+3 SB3	DI30	J3-118,125	?	IOP N+3						
			2						GPC N SB1	DO20	J3-43,44	1	3 IOPS	SPARE
			2						GPC N SB2	DO24	J3-34,35	1	3 IOPS	IPR SYNC
			2						GPC N SB3	DO28	J3-46,47	1	3 IOPS	SSIP SYNC
1-3.3-39	FCMFDI	FIOCMPLT CALL	1	NONE	N/A	N/A	N/A	N/A	GPC FAIL	DRO00	J5-46,58	1	PANEL	NOT FAILED
			?	GPC N+1 FLI	DRI03	J5-36,37	?	IOP N+1	GPC N+1 FLO	DRO07	J5-44,45	?	IOP N+1	
1-3.3-93	FCMSVC	FPMSVC CALL	?	GPC N+2 FLI	DRI04	J5-35,47	?	IOP N+2	GPC N+2 FLO	DRO08	J5-42,43	?	IOP N+2	
			?	GPC N+3 FLI	DRI05	J5-33,34	?	IOP N+3	GPC N+3 FLO	DRO09	J5-40,41	?	IOP N+3	
									GPC N FLO	DRO00	J5-46,58	?	IOP N	

Table 4 (continued). List of discretes used/issued by the FCOS modules

PAGE REF. NO. 5	MODULE	INVOCATION	SEQ OF USE OR IS-SUE	DISCRETES USED	LABEL	PIN NUM.	LOG VAL	INPUT FROM	DISCRETES ISSUED	LABEL	PIN NUM	LOG VAL	OUTPUT TO	SINGLE BIT ERRORS WILL CAUSE DISCRETES TO BE INTER-PRETED AS
3-3.1-15	AIC_GPC_	GPC STARTUP	1	NONE	N/A	N/A	N/A	N/A	GPC READY	D009	J3-25,37	1	PANEL	NOT READY
			1	GPC RUN	DI02	J5-5,6	?	PANEL						
			1	GPC STANDBY	DI01	J5-3,4	?	PANEL						
			1	BFCS ENGAGE	DI11	J5-23,24	?	PANEL						
3-3.25	ARA_GPC_ SWITCH	SWITCH MONIT	1	I/O TERM.A	DI12	J5-25,26	?	PANEL						
			1	I/O TERM.B	DI13	J5-27,28	?	PANEL						
									I/O TERM.A	DI12	J5-25,26	?	PANEL	
									I/O TERM.B	DI13	J5-27,28	?	PANEL	

Table 4 (continued). List of discretes used/issued by the FCOS modules

connected to all the GPCs. When GPCi desires to communicate with other GPCs through the ICC buses, it selects ICCi with the aid of the identification number stored in CVT and COMPOOL.

The requirement that each GPC correctly records and maintains the identification number is crucial to space shuttle operation; if this requirement is not met, either because of discrete failure or faulty core locations, the ensuing consequences will be unpredictable. When two GPCs have the same identification number and attempt to transmit information on a common bus, signal interference results. If this bus is not flight-critical or an ICC bus unit, data bus I/O failures will be recorded and this may eventually lead to bus masking and its removal. However, if this bus happens to be either critical or an ICC bus, the GPCs in command of the bus will force themselves to synchronization failures. Thus the two GPCs will drop out from the redundant as well as the common set. If they attempt to communicate their synchronization failures and use the same data bus for doing so, signal interference once again results with the consequence that the crew may not be notified. At this point, the situation becomes unpredictable and may even lead to loss of spacecraft control.

The CPDS requirements stipulate that the software shall support a display which monitors the operational status of each GPC in Redundant Set, simplex, failed or OFF/HALT mode [6]. Thus the crew may note from the display that the two GPCs are not functioning properly and may engage the Backup Flight Control Switch.

The time that might elapse before detection of the identification discrete failure is variable. Since the identification discretes are read on the ground prior to the mission, any discrete failures at this time will be immediately noticeable. Once the discretes are read, the identification number is fetched only from the internal GPC tables and hence the identification failure may result due to core memory location faults. If this happens, the time of detection is unpredictable and depends to a large extent on the crew action.

A quantitative assessment of the identification failure will be given in the next chapter.

3.2 Synchronization Discrete Failures

Synchronization discretes are used by the following software modules directly or indirectly:

Module	Page No. [5]	Usage
FPMIHPC2	3.2-49, Part 1	Direct
FIOCMPLT	3.2-12a, Part 1	Direct
FIOERRLC	3.2-34, Part 1	Direct
FIOBCERR	3.2-37, Part 1	Direct
FIOMSCTO	3.2-39, Part 1	Direct
FCMASYNC	3.3-23, Part 1	Direct
FCMCSYNC	3.3-25, Part 1	Direct
FCMISYNC	3.3-29, Part 1	Direct
FCMSSYNC	3.3-35, Part 1	Direct
FCMTSYNC	3.3-37, Part 1	Direct
FCMBMAN	3.3-63, Part 1	Indirect
FIOSVC	3.2-9, Part 1	Indirect
FIOSVCP	3.2-12, Part 1*	Indirect
FPMCANCL	3.1-35, Part 1	Indirect
FPMCLOSE	3.1-27, Part 1	Indirect
FPMIEPCT	3.1-39, Part 1	Indirect
FPMOPSCN	3.1-38a, Part 1	Indirect
FPMRES	3.1-19, Part 1	Indirect
FPMRESET	3.1-67, Part 1	Indirect
FPMSCHED	3.1-9, Part 1	Indirect
FPMSET	3.1-68, Part 1	Indirect
FPMSIGNL	3.1-69, Part 1	Indirect
FPMSTAT	3.1-25, Part 1	Indirect
FPMTERM	3.1-31, Part 1	Indirect
FPMTMHAL	3.1-63, Part 1	Indirect
FPMUPRIO	3.1-23, Part 1	Indirect
FPMWAIT	3.1-17, Part 1	Indirect
FCMPMOD	3.3-53, Part 1	Indirect
FCMBCEMD	3.3-55, Part 1	Indirect
FCMPOVLY	3.3-49, Part 1	Indirect
FJOHLTMM	3.2-71, Part 1*	Indirect
FPMUPMTU	3.1-55, Part 1	Indirect
FPMMTURM	3.1-73, Part 1*	Indirect

*Reference [7]

The software modules listed under direct usage issue commands that directly change the status of the synchronization discretes and use these discretes in their logic. The indirect-usuage modules invoke the direct-usage modules

in order to achieve software synchronization through the synchronization discretes. As can be noted, these discretes are used extensively by the software to operate the GPCs in the Redundant and Common Sets in synchrony with each other and minimize the data skew which exists because of the redundant operation of the GPCs.

A synchronization discrete failure will cause the removal of the GPC it is associated with from the Redundant and Common Sets, even though the GPC may be functioning properly. The outcome of this type of failure is the loss of a GPC, and the crew is immediately notified of the synchronization failure through the Computer Annunciation Matrix. Since the synchronization discretes are used as often as 300 times/second by application programs, the failure of these discretes is immediately observed. Also, since the SSIP and Fast-Cycle Execution programs use synchronization at every 40 ms interval, the upper bound on the time of detection of synchronization discrete failures is approximately 20-30 ms.

3.3 Redundancy Management Discrete Failures

The following modules can alter the state of redundancy management discretes:

Module	Page No. [5]	Usage
FCMSVC	3.3-93, Part 1	Direct
FCMFDI	3.3-39, Part 1	Direct
FCMVOTE	3.2-83, Part 1*	Direct
FPMSVC	3.1-2, Part 1	Indirect
FIOCMPLT	3.2-129, Part 1	Indirect

*Reference [7]

The direct usage modules can change the status of fail discretes that drive the Computer Annunciation Matrix. The indirect usage modules invoke the direct-usage modules. When a failure occurs on one of these discretes, the light driven by the faulty discrete may be lit. However, this may not have any undesirable consequences since the crew, by observing the other three lights in the same row, can deduce whether the light is energized due to a discrete failure or to a GPC failure. The situation with the GPC5 fail discrete is different; GPC5 performs self testing to see whether it is functioning properly and is not involved in cooperative testing. Thus, when the light connected to the GPC5 fail discrete is energized, the crew may not know whether this is due to a discrete failure or due to the Backup Computer System failure. In this situation, the consequences are dependent on the crew action. In the worst case, the crew may assume the loss of Backup System even though this system may be functional. Any failure on the redundancy management discretes is immediately noticeable.

3.4 Control and Indicator Discrete Failures

The GPC Standby/Run Command discretes are monitored by the ARA_GPC_ SWITCH module (Page 3.3-25, Part 3 [5]) once per every second whereas the GPC Ready indicator is controlled by the AIC_GPC_STARTUP module (Page 3.1-15, Part 3 [5]). The Halt indicator has hardware control on the GPC operation and thus is not used in software logic. When a Standby or Halt discrete is set erroneously due to transient or permanent faults, the GPC stops participating actively in computation and control of the space shuttle, thus resulting in a GPC loss. Within seconds, the crew will be notified of the loss of the GPC and its status, and thereafter the action of the crew decides the consequences. The Run Command is accepted by the GPC only when it has been initialized and is in a Standby state. Thus, a Run Command discrete, when it is set prematurely, may cause the GPC to start computation before it is expected to do so. However, this should not have any adverse consequences.

When the GPC IPL discrete is prematurely set false when IPL is being performed, the crew may be under the impression that the GPC is IPL'ed and ready to go. However, since the IPL operation takes of the order of milliseconds, this type of discrete failure does not cause any severe problems. The IPL Activate discrete, if affected by transient failures, also does not cause adverse problems. However, permanent faults on these discretes mean the loss of the GPC and reduced computational power.

The I/O Active indicator discrete falls into the same category as the preceding two, in that its transient failure does not cause adverse consequences. If the discrete is erroneously set true indicating that the IOP is ready to accept crew commands where, in actuality, this may not be so, the crew may initiate commands which may be lost. Here again, the resulting consequences depend on the crew interpretation of the situation.

Transient errors on the I/O Terminate Command A and B discretes can cause data path errors logged againt the flight-critical buses. When this happens, the software module FIOCTDPE is invoked to see if there is any change in the status of the Standby/Halt or BFCS Engage switches. If these switches do not indicate any changes and more than P (nominally two) FC 1-4 or FC 5-8 data paths are masked, the GPC forces itself to a synchronization failure and removes itself from the Redundant Set. Whenever a data path is masked due to an error, the data path error is annunciated

to the user. Thus the net effect of I/O Terminate discrete failures can be the loss of a GPC. The crew may not be able to deduce whether the GPC loss is due to I/O Terminate discrete failures or to the GPC failure.

The MM IPL Select Command discrete transient failures can cause a wrong MM to be selected for IPL. These failures are not critical, and in the worst case the GPC will not be IPL'ed. Transient failures on the Mass Memory discretes have similar effects on the IPL of the GPC. Also, the uplink/downlink capabilities to/from the MMUs will be temporarily affected by the transient failures.

The BFCS Engage Command discrete, when set true erroneouly, can cause invocation of the software module FCMBMASK and this may lead to data path masking. Thus a failure on this discrete can cause the loss of GPC.

For the Backup Control System, any single transient failure on the BFCS discretes does not cause the BFCS to be engaged. The three BFCS Engage Commands and the IOP Terminate Command B Inverse discrete are majority voted to decide when the Backup System is to be engaged. The BFCS Fail discrete failure can cause the crew to think that the BFCS control unit is not operational whereas, in actuality, this may not be so. As mentioned before, the GPC Fail indicator discrete failure may misinform the crew as to the operational status of the BFCS.

3.5 Discrete Failure Analysis

In the preceding sections the effects of a fault on each discrete is discussed individually; in the present section this discussion is extended to transient and permanent discrete failures and their effects on the entire system. The discussion is summarized in Table 5, which lists each discrete failure, transient and permanent, together with information regarding recoverability from this failure and consequences in the worst case.

The redundancy management and synchronization discretes are used when the GPC is included in the Redundant Set and hence permanent failures of any of these discretes imply that the GPC cannot be used in a redundant computation. On the other hand, the GPC can be used to compute by itself and thus these failures are not critical for self-operation. Transient failures on the synchronization discretes result in the loss of the GPC from the Common and Redundant Sets as mentioned before in the previous sections; however the GPC can be recovered by re-initialization. Transient failures on the redundancy management discretes do not have any effects on the DPS; however, if these failures are misinterpreted by the crew, this may cause the loss of the GPC once again. The GPC 5 Fail discrete, if it malfunctions due to a transient error, can cause an alarm, and here again the resulting consequences are decided by the crew action.

The control and indicator discretes are necessary for proper operation of the GPC and permanent failure of any of these discretes imply permanent loss of the GPC. Transient errors on these discretes may or may not have an effect on the system performance depending on the crew interpretation of the situation. Thus if the IOP Indicator discrete fails for a short time, the crew may attempt to use the GPC after awhile or disable the GPC from further computation. If the IPL discretes are not functioning properly because of transient errors, the crew may decide to try IPL repeatedly or once again remove the GPC from computation.

The BFCS is designed so that transient and single errors on the BFCS discretes do not have any effect. The BFCS Engage Command and I/O Terminate Command discretes are majority-voted and tested for stability before any action is attempted. Thus only multiple simultaneous faults which persist for over two consecutive minor cycles can cause engagement of the BFCS. If other GPCs are not properly disabled from their data buses, totally unpredictable consequences may ensue.

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
Identification	Transient Permanent	If the failure occurs in the preinitialization phase on the ground, the failure can be detected by monitoring the displays and recovered. If the failure occurs after one-time initialization, no effect on the system.	If the identification discrete failure is not noticed on the ground (which is unlikely) the entire DPS will be non-functional.	Immediate, by observing the displayed status of the GPCs.
Redundancy Management	Transient	Single transient errors do not have any effects. Multiple simultaneous transient errors can cause disablement of correctly operating GPCs by the crew. A transient error on the GPC 5 Fail discrete indicates the BFCS is not ready to take over.	Loss of a GPC depending on the crew action.	Immediate
	Permanent	Single permanent errors do not have any effects. Multiple errors lead to the loss of the GPC. The GPC can be operated in a self mode.	Loss of a GPC from the Redundant Set.	Immediate

Table 5. Discrete failure analysis.

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
Synchronization Discretes	Transient	Transient errors cause removal of the GPC from the Redundant and Common Sets. The GPC can be recovered by forming a new Redundant Set.	Loss of a GPC from the Redundant and Common Sets.	Synchronization discretes are used at every 20 ms intervals in SSIP and Fast Cycle Processor Phases and in GN&C as many times as 300 per second. The time of detection is immediate.
	Permanent	Permanent errors imply that the GPC cannot be operated in a redundant mode; but it can be operated in a self mode with self-testing to improve reliability.	Loss of a GPC from cooperative and redundant computation.	

Table 5 (continued). Discrete failure analysis

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
GPC Halt/Standby/ Run Command Discretes	Transient	Transient errors on the GPC Halt/Standby Command discretes force an operating GPC into a Halt or Standby mode. Errors on Run Command discrete have an effect only in Standby mode. The GPC can be recovered by performing an IPL and placing it in proper mode.	Forced termination of a correctly operating GPC.	These Command discretes are monitored once a second and the status of the GPCs is displayed on monitors. Time of detection is immediate.
	Permanent	Permanent errors have the same effect as transient errors. The GPC cannot be recovered as in the transient error case.	Forced termination of a correctly operating GPC and the permanent loss of a GPC.	

Table 5 (continued). Discrete failure analysis

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
GPC Ready Indicator	Transient	If the Ready Indicator comes on prematurely while performing the IPL and the crew initiates commands, the GPC may not respond. To recover from this error, the crew should reinitiate their commands instead of disabling the GPC.	Loss of a GPC because of the crew action. (This is unlikely because IPL takes of order .5 ~ .75 seconds.)	Immediate
	Permanent	Effects are the same as in the transient case. The GPC cannot be brought to a Halt state and reinitialized.	Permanent loss of a GPC when it is brought to the Halt state.	Immediate
IPL Discretes	Transient	Transient errors on IPL discretes cause improper IPL. To recover from these errors IPL has to be performed again.	Loss of a GPC depending on the crew action.	Immediate
	Permanent	Effects are the same as in the transient case. Permanent errors on IPL discretes imply that the GPC cannot be re-IPLed properly.	Permanent loss of a GPC if it is brought to the Halt state.	Immediate

Table 5 (continued). Discrete failure analysis

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
I/O Active Indicator	Transient	A transient or permanent failure can cause an erroneous indication that does not reflect the true status of the IOP. Transient errors can be ignored but a permanent failure means that the GPC cannot be used again.	Disablement of a GPC depending on the crew action.	Immediate
	Permanent		Loss of a GPC.	Immediate
I/O Terminate Command discretes	Transient	Transient errors cause disablement of data buses from the GPC and possibly its ultimate removal from the Redundant Set. The GPC can be recovered by reinitialization and formation of a new Redundant Set.	Loss of a GPC from the Redundant Common Sets.	Depends on data bus activity. In all cases the detection will be immediate and within seconds.
	Permanent	Permanent failures imply the loss of the GPC from further computation.	Permanent loss of a GPC from further computation and control.	

Table 5 (continued). Discrete failure analysis

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
Mass Memory Discretes	Transient	Transient faults can cause IPL not to be performed properly in the IPL phase. Transactions involving MMUs may not be completed properly. The MMUs can be recovered by re-tries.	Loss of a GPC depending on the crew action.	Immediate in the IPL phase. At other times, dependent on the frequency of MMU usage.
	Permanent	Same as in the transient case. Permanent failures imply the loss of MMU(s) and software modules and consequently the entire DPS.	Permanent loss of MMU(s) and possibly the entire DPS.	
BFCS Engage Discrete (GPC 1 - 4)	Transient	Transient failures can cause disablement of data buses from the GPC and force the GPC to a synchronization failure. The GPC can be recovered by re-initialization.	Loss of a GPC from the Redundant and Common Sets.	Dependent on data bus activity. In all cases time of detection will be within seconds.
	Permanent	Effects are the same as in the transient case. The GPC cannot be recovered from this failure and hence it is not available for computation.	Permanent loss of a GPC.	

Table 5 (continued). Discrete failure analysis.

Discrete Type	Failure Type	Effects and Recoverability	Worst-Case Consequence	Time of Detection
BFCS Engage and I/O Terminate Command Discretes	Transient	Only multiple simultaneous transients that last for two minor cycles on these discretes can have an effect.	Engagement (or disengagement) of BFCS.	Immediate
	Permanent	A single permanent failure does not have any effect. Multiple failures can cause unreliable and unpredictable DPS performance.		
BFCS Fail	Transient	Transient failures can be ignored since they do not have any effect on the DPS.		Immediate
	Permanent	A permanent failure means that the BFCS is not operational.	Loss of BFCS.	Immediate

Table 5 (continued). Discrete failure analysis.

4. PROBABILISTIC ANALYSIS OF DISCRETE FAILURES

In this chapter, a probabilistic analysis of discrete failures is given. The anlysis is necessarily limited because of the lack of detailed information regarding the circuit and component reliabilities. An exponential failure law is assumed in the analysis throughout.

4.1 Identification Failures

Identification failures will be due either to the identification discrete failures or to the core memory location failures. Since the former type of failure is detectable on the ground and thus correctable, only core memory failures will be considered in the following. (Although the scope of the present Contract covers only the effects of discrete failures, the criticality of the situation necessitates the consideration of core memory failures). Each core element* follows the reliability law $R_c = e^{-\lambda_c t}$ where $1/\lambda_c$ is the mean life of the element. The identification numbers of the four primary GPCs can be changed or misread due to the unreliable operation of core elements. For simplicity of analysis, it is assumed that once this happens, catastrophy ensues because of the resulting conflicts for data buses. (The software can possibly detect certain identification number errors, such as the number being equal to 000 or greater than 100). Then the probability P_c of obtaining correct identification numbers can be given as

$$P_c = e^{-12\lambda_c t} \qquad (1)$$

and the mean time to the catastrophic error as

$$T_c = .0833/\lambda_c \qquad (2)$$

The probability of catastrophic error can be minimized by using a redundant or coding approach. In the redundant approach each identification number is stored in three memory locations and majority voting is performed to obtain the correct identification number, assuming as before a failure rate of λ_c for each core element. The probability that the correct identification number is generated is

*In the following the term core element refers to the magnetic core and its associated read/write circuitry.

$$p_{cor} = p_c^9 + \binom{3}{1}\binom{3}{1}p_c^8(1-p_c)$$

$$+\binom{3}{1}\binom{3}{2}p_c^7(1-p_c)^2 + \binom{3}{1}\binom{3}{3}p_c^6(1-p_c)^3$$

where p_c is the probability that the core element is functioning properly. Since

$$p_c(t) = e^{-\lambda_c t}$$

it follows

$$R_c(t) = 3e^{-6\lambda_c t} - 2e^{-9\lambda_c t}$$

The probability of catastrophic failure occurrence due to identification number error can now be determined as

$$p_c' = \left\{R_c(t)\right\}^4 = 81e^{-24\lambda_c t} - 216e^{-27\lambda_c t}$$

$$+ 216e^{-30\lambda_c t} - 96e^{-33\lambda_c t} + 16e^{-36\lambda_c t} \qquad (3)$$

The following coding approach may also be used to reduce system unreliability. Assume that six bits are assigned (instead of three) for each identification number in the following manner:

GPC1 : 00 00 00
GPC2 : 01 01 01
GPC3 : 10 10 10
GPC4 : 11 11 11

Each identification number is at least three units of distance from other identification numbers and hence this coding can correct one and detect two core element failures in each identification number location. The probability of identification numbers being correct can be derived as

$$P_{cor} = \left\{p_c^6 + 6p_c^5(1-p_c) + 3p_c^4(1-p_c)^2\right\}^4$$

$$= 81p_c^{16} - 216p_c^{18} + 216p_c^{20} - 96p_c^{22} + 16p_c^{24}$$

Assuming p_c to be exponential as before, the reliability of correct generation of identification numbers can be found as

$$P_c(t) = 81e^{-16\lambda_c t} - 216e^{18\lambda_c t} + 216e^{-20\lambda_c t} + 96e^{-22\lambda_c t} + 16e^{-24\lambda_c t} \quad \text{(4)}$$

The failure rate for the entire 64K x 36-bit GPC memory is approximately 500 failures/million hours.* Assuming that when a core element fails, it is due to the read/write amplifier circuitry, λ_c can be determined approximately as .75 failures/10^6 hours. When $\lambda_c t$ is small,

$$P_c \simeq 1-12\lambda_c t \quad \text{(1')}$$

$$P_c' \simeq 1-108(\lambda_c t)^2 \quad \text{(3')}$$

$$P_c'' \simeq 1-48(\lambda_c t)^2 \quad \text{(4')}$$

*Private communication from Mr. Paul Sollock of NASA-JSC.

It follows that the unreliabilities can be given as

$$Q_c = 1-P_c \simeq 12\lambda_c t \qquad \_\_\_\_ (5)$$

$$Q_c' = 1-P_c' \simeq 108(\lambda_c t)^2 \qquad \_\_\_\_ (6)$$

$$Q_c'' = 1-P_c'' \simeq 48(\lambda_c t)^2 \qquad \_\_\_\_ (7)$$

The improvements in system reliability using the redundant and coding approaches can be given as

$$F_R = Q_c/Q_c' \simeq 1/9(\lambda_c t)^2 \qquad \_\_\_\_ (8)$$

$$F_C = Q_c/Q_c'' \simeq 1/4(\lambda_c t)^2 \qquad \_\_\_\_ (9)$$

Figures 4.1 and 4.2 show P_c, P_c' and P_c'' for $\lambda_c = 10^{-7}$, 2×10^{-7}, 5×10^{-7} and 10^{-6} failures/hour as t varies from .15 to 2.1 hours, whereas Figure 4.3 shows the improvements in system reliability using coding and redundant approaches.

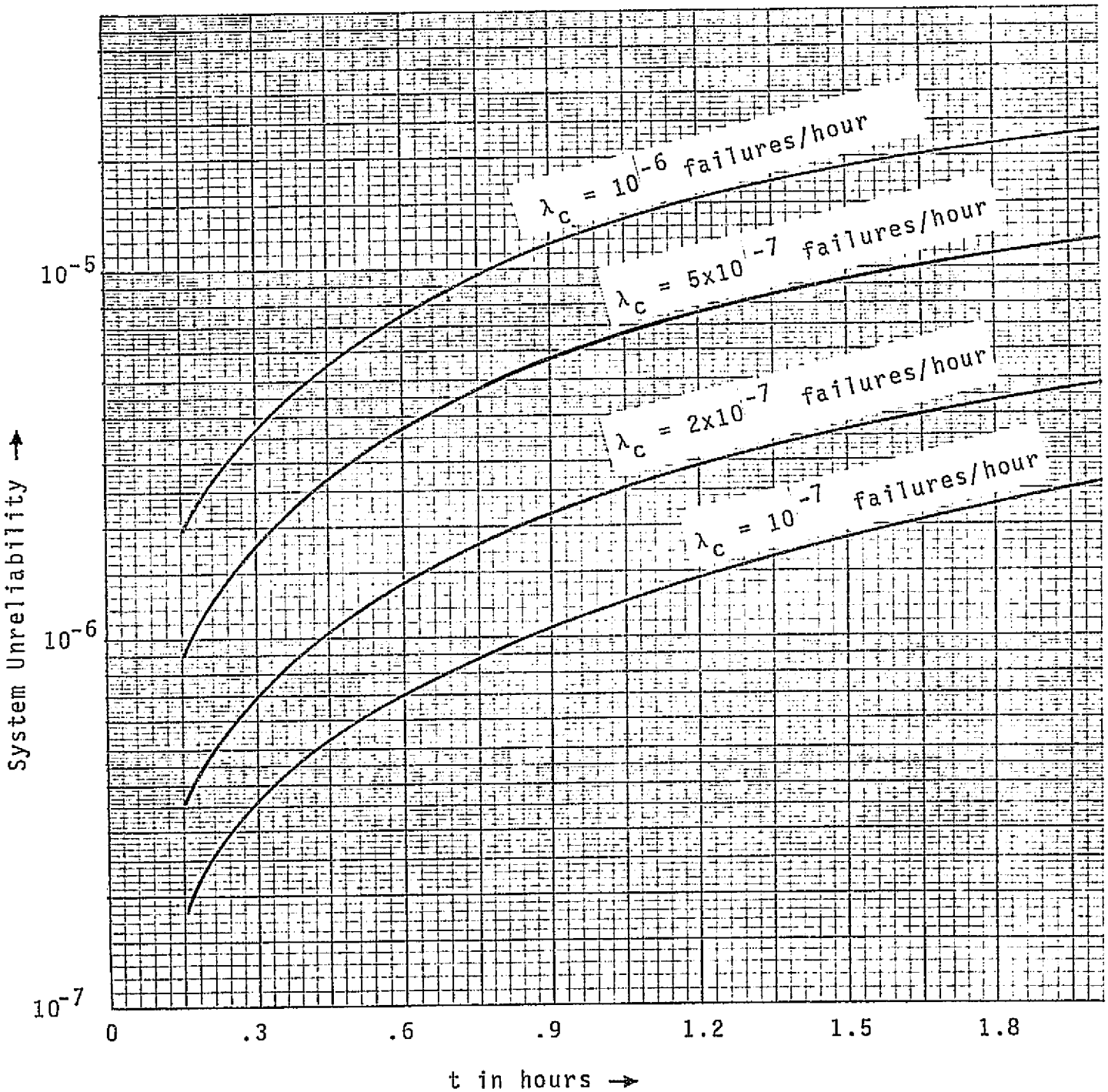


Figure 4-1. System unreliability due to identification number failure versus time in hours.

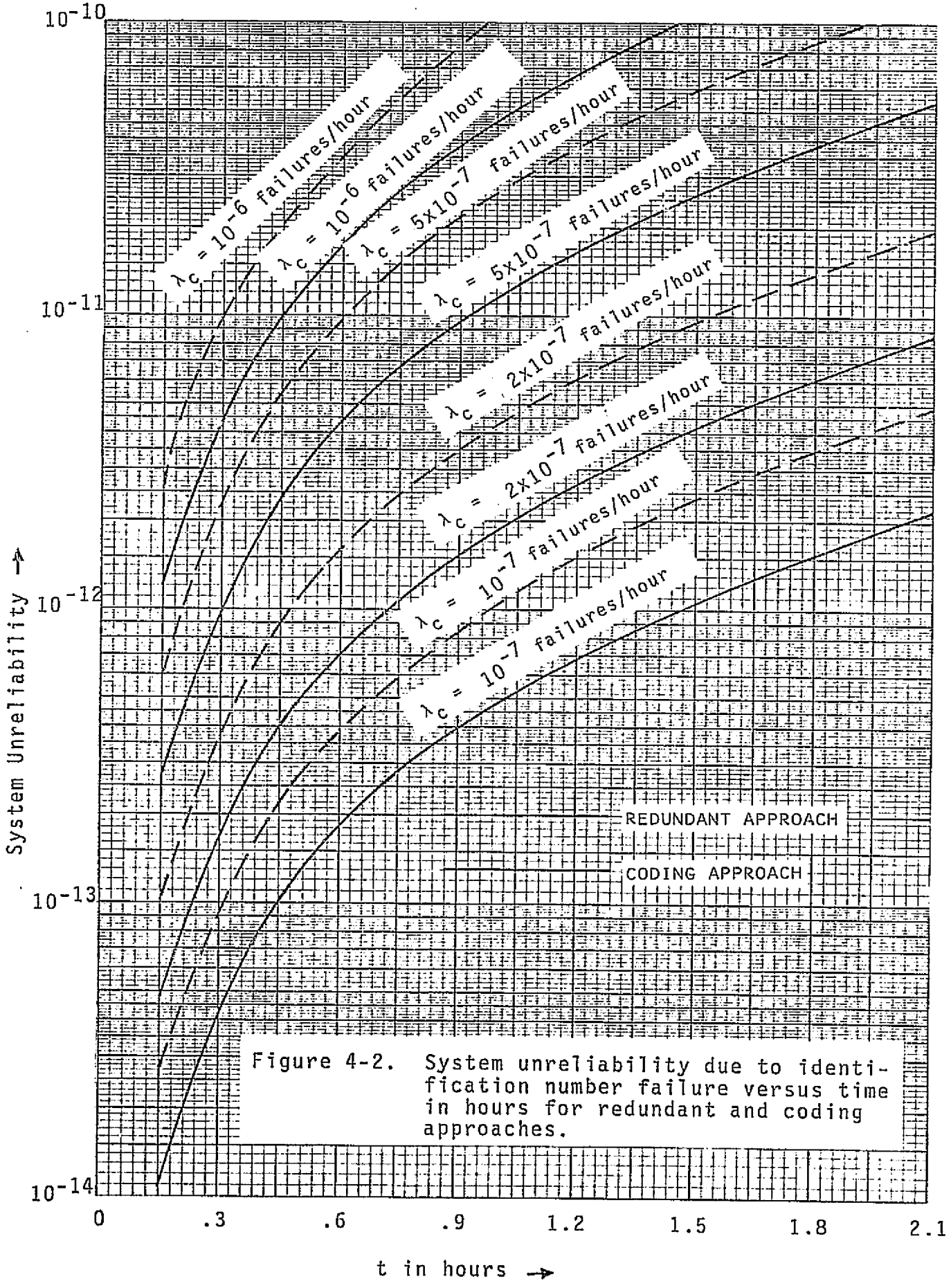


Figure 4-2. System unreliability due to identification number failure versus time in hours for redundant and coding approaches.

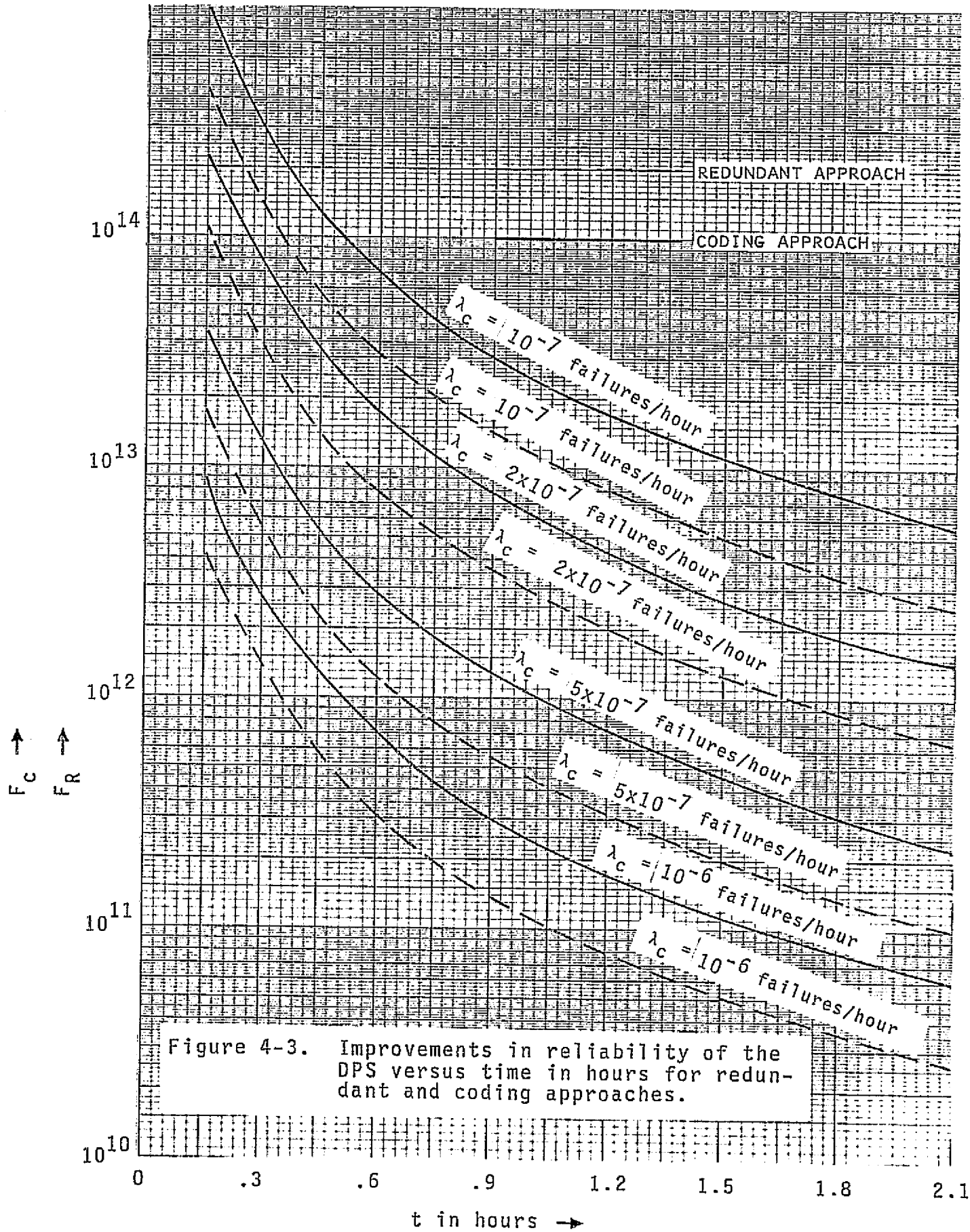


Figure 4-3. Improvements in reliability of the DPS versus time in hours for redundant and coding approaches.

4.2 Effects of Discrete Failures on System Reliability

In this section, a quantitative analysis of the effects of discrete failures on the entire system reliability is attempted. The mission duration time, during which the Primary Control System is effective, is established.

The following effective failure rates are assumed for the IOP discretes:

Discretes	Effective Failure Rate
Redundancy Management	$\pi_{RM} \cdot \lambda_{RM}$
Synchronization	$\pi_{SYNC} \cdot \lambda_{SYNC}$
I/O Active Indicator	$\pi_{IOA} \cdot \lambda_{IOA}$
GPC Ready Indicator	$\pi_{GPCR} \cdot \lambda_{GPCR}$
GPC IPL Indicator	$\pi_{GPCI} \cdot \lambda_{GPCI}$
GPC Halt	$\pi_{GPCH} \cdot \lambda_{GPCH}$
GPC Standby	$\pi_{GPCS} \cdot \lambda_{GPCS}$
GPC Run	$\pi_{GPCR} \cdot \lambda_{GPCR}$
MMi IPL Select	$\pi_{MMiI} \cdot \lambda_{MMiI}$
I/O Terminate A	$\pi_{IOTA} \cdot \lambda_{IOTA}$
I/O Terminate B	$\pi_{IOTB} \cdot \lambda_{IOTB}$
MMi Reset	$\pi_{MMiS} \cdot \lambda_{MMiS}$
MMi Ready	$\pi_{MMiR} \cdot \lambda_{MMiR}$
BFCS Engage	$\pi_{BFCE} \cdot \lambda_{BFCE}$

The value of π for a given discrete can be chosen 1 or 0 depending on whether a fault on this discrete causes the crew to remove the GPC associated with it. Thus if the IPL Indicator discrete fails but the crew chooses to ignore it π_{GPCI} can be set to 0. The failure rate for each GPC is

$$\lambda_{GPC} = \sum_{Discrete} \pi_{Discrete} \cdot \lambda_{Discrete}$$

where Discrete runs through all the discretes listed above.

The probability of correct operation of the DPS can be given as

$$\begin{aligned} P_{cor} = {} & p(\text{correct operation} \mid \text{non-standby}) \cdot \\ & p(\text{non-standby}) + \\ & p(\text{correct operation} \mid \text{standby}) \cdot \\ & p(\text{standby}) \end{aligned}$$

$$= \binom{4}{2} p_c^2 (1-p_c)^2 + p_B \cdot \left[1 - \binom{4}{2} p_c^2 (1-p_c^2)^2 \right]$$

where p_c and p_B are the probabilities that the primary and backup systems are working properly. Assuming a failure rate of λ_B for the Backup System, one has for the reliability of the entire computing system

$$R_c(t) = \left\{ 6\, e^{-2\lambda_{GPC} t} - e^{-4\lambda_{GPC} t} \right\} \cdot \left\{ 1 - e^{-\lambda_B t} \right\}$$

$$+ e^{-\lambda_B t}$$

$$= 6e^{-2\lambda_{GPC} t} - 6e^{-4\lambda_{GPC} t} - 6e^{-(2\lambda_{GPC} + \lambda_B) t}$$

$$+ 6e^{-4\lambda_{GPC} + \lambda_B) t} + e^{-\lambda_B t}$$

and the mean time to the first failure of the DPS as

$$T_c = \frac{3}{2\lambda_{GPC}} - \frac{12\lambda_{GPC}}{(2\lambda_{GPC}+\lambda_B)(4\lambda_{GPC}+\lambda_B)} + \frac{1}{\lambda_B}$$

Letting $\rho = \lambda_{GPC}/\lambda_B$, T_c becomes

$$T_c = \frac{1}{\lambda_{GPC}} \left\{ \frac{16\rho^3+24\rho^2+20\rho+3}{16\rho^2+12\rho+2} \right\}$$

In determing λ_{GPC}, the value of π for a given discrete can be chosen 1 or 0, depending on whether a fault on this discrete causes the crew to remove the GPC associated with it. Thus if the IPL Indicator discrete fails but the crew chooses to ignore it, π_{GPCI} can be set to 0.

The unreliability of the entire DPS, $Q_c(t)$ is shown in Figures 4-4 through 4-7. The values of λ_{GPC} are selected to be 100, 200, 500 and 1000 failures/10^6 hours and ρ varies from 1 to 100. Figure 4-8 shows the variation of successful mission time with respect to the ratio T_c/T_{GPC} where $T_{GPC} = 1/\lambda_{GPC}$. It is interesting to note that this ratio is nearly proportional to ρ.

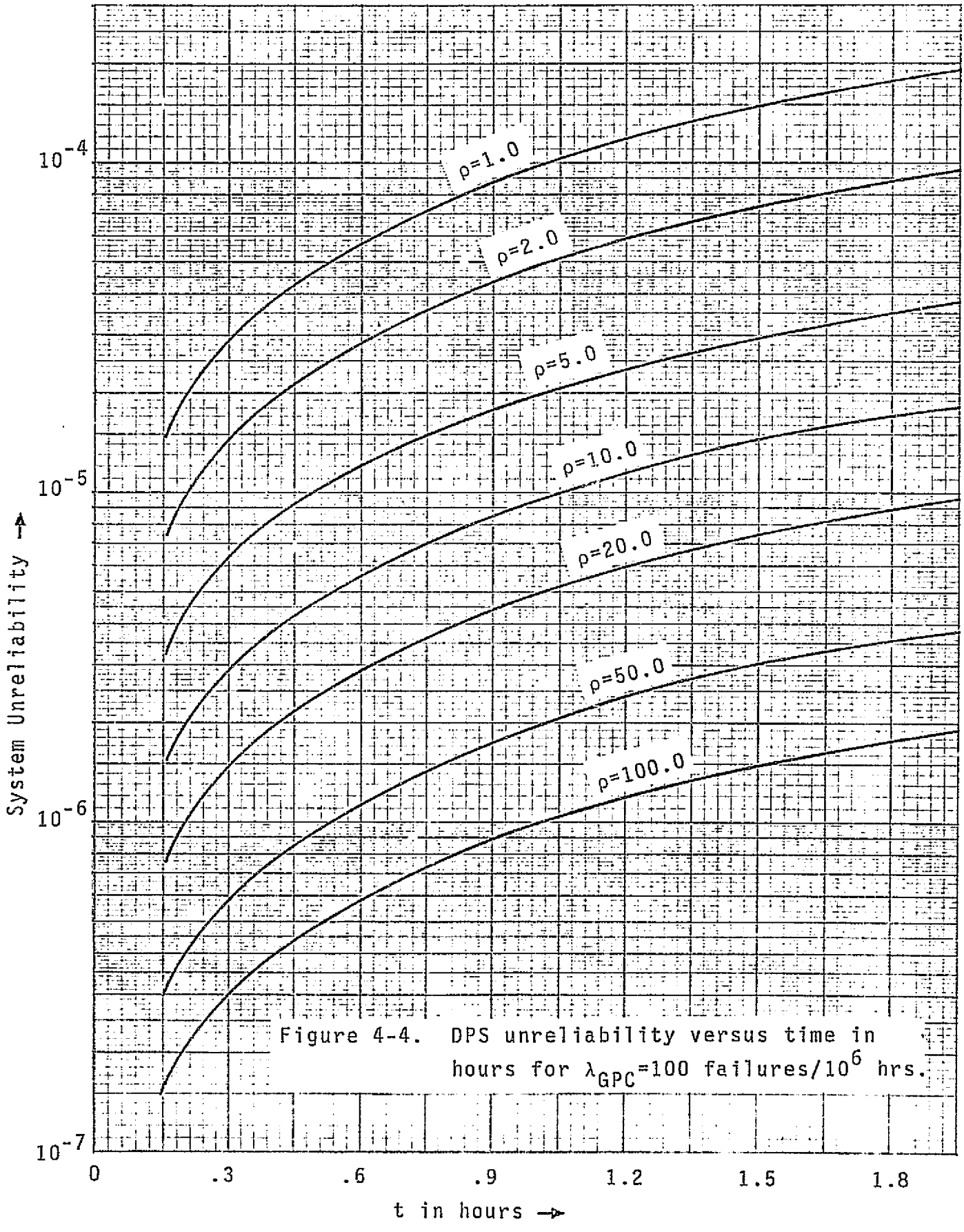


Figure 4-4. DPS unreliability versus time in hours for λ_{GPC}=100 failures/10^6 hrs.

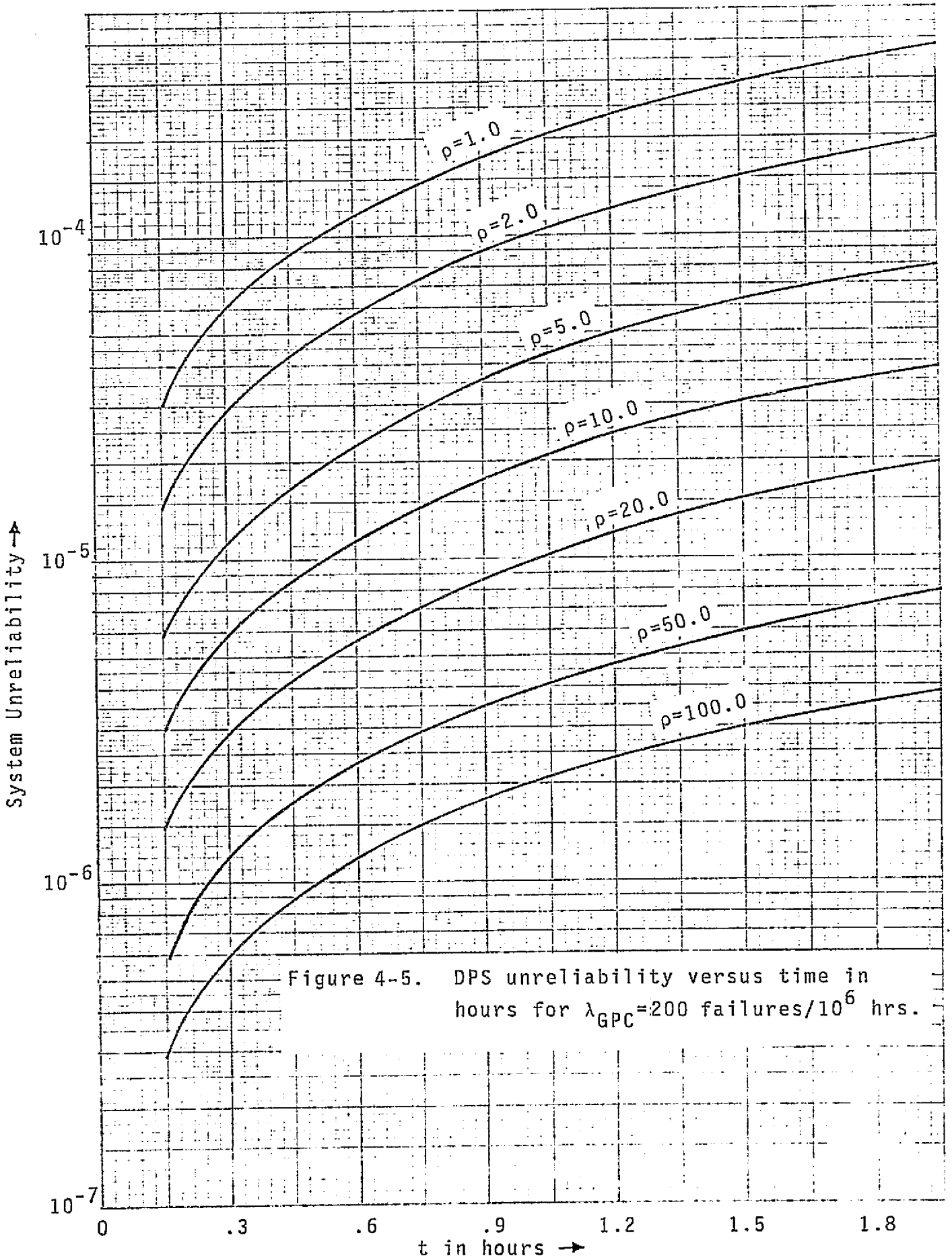


Figure 4-5. DPS unreliability versus time in hours for λ_{GPC}=200 failures/10^6 hrs.

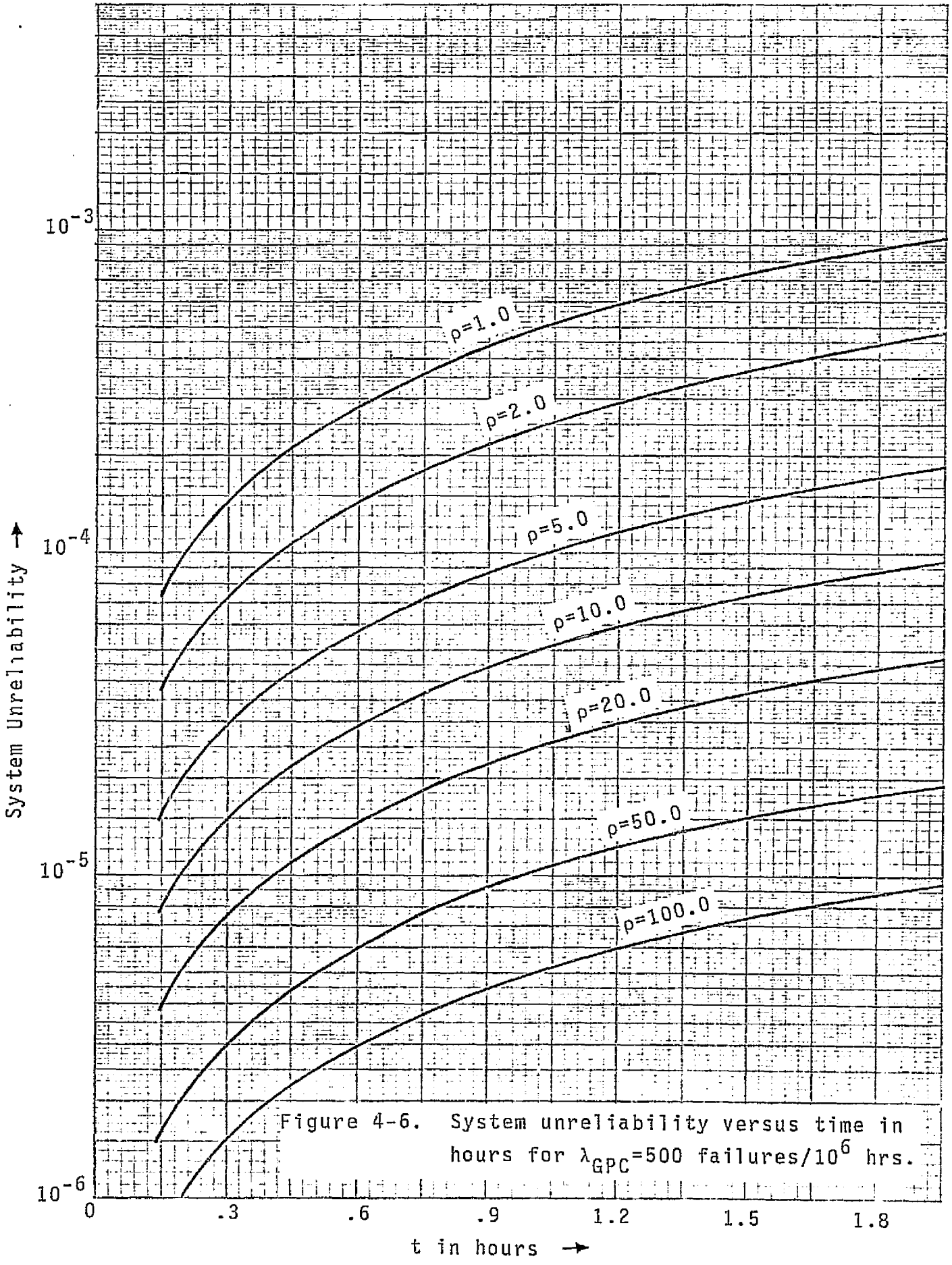


Figure 4-6. System unreliability versus time in hours for λ_{GPC}=500 failures/10^6 hrs.

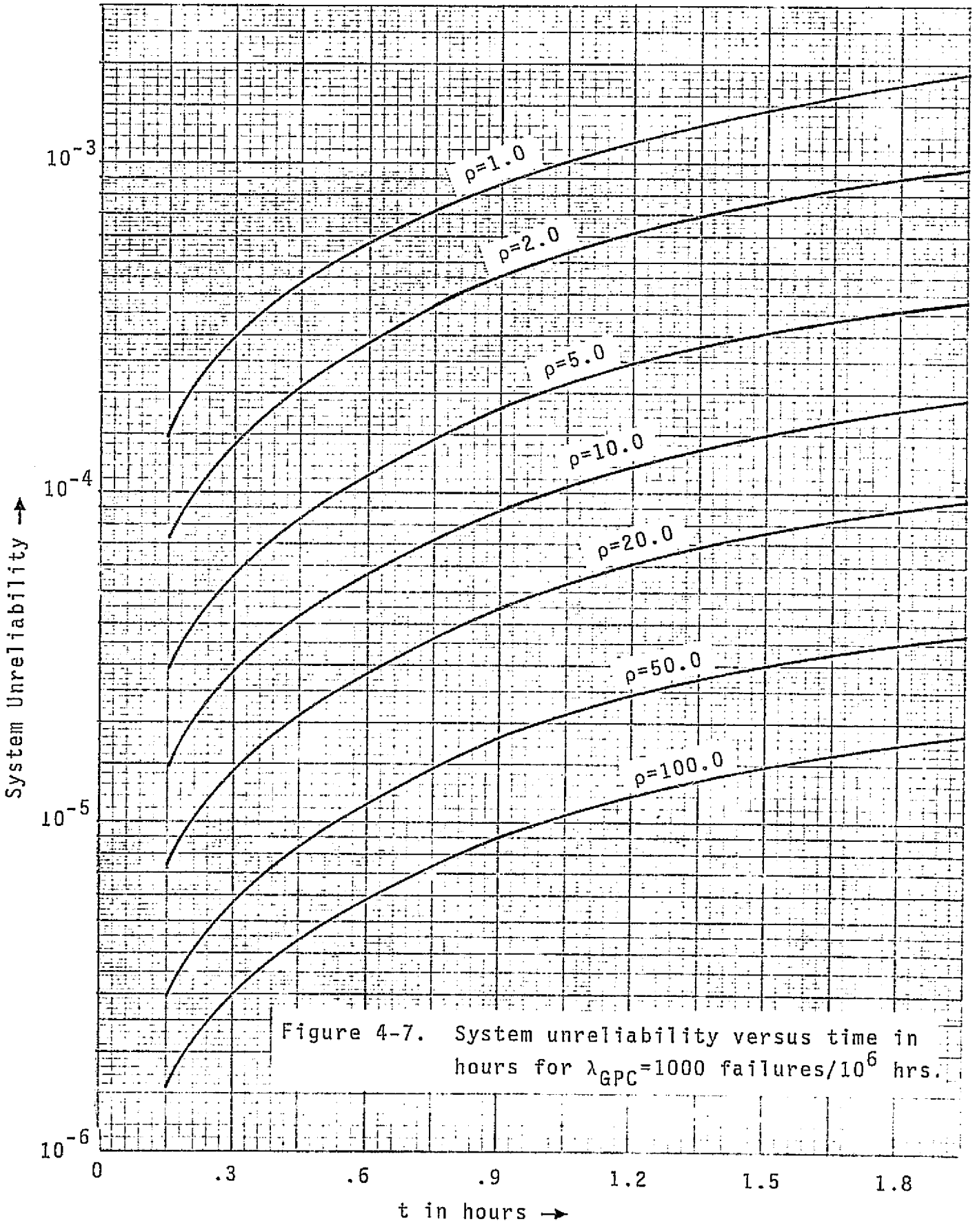


Figure 4-7. System unreliability versus time in hours for λ_{GPC}=1000 failures/10^6 hrs.

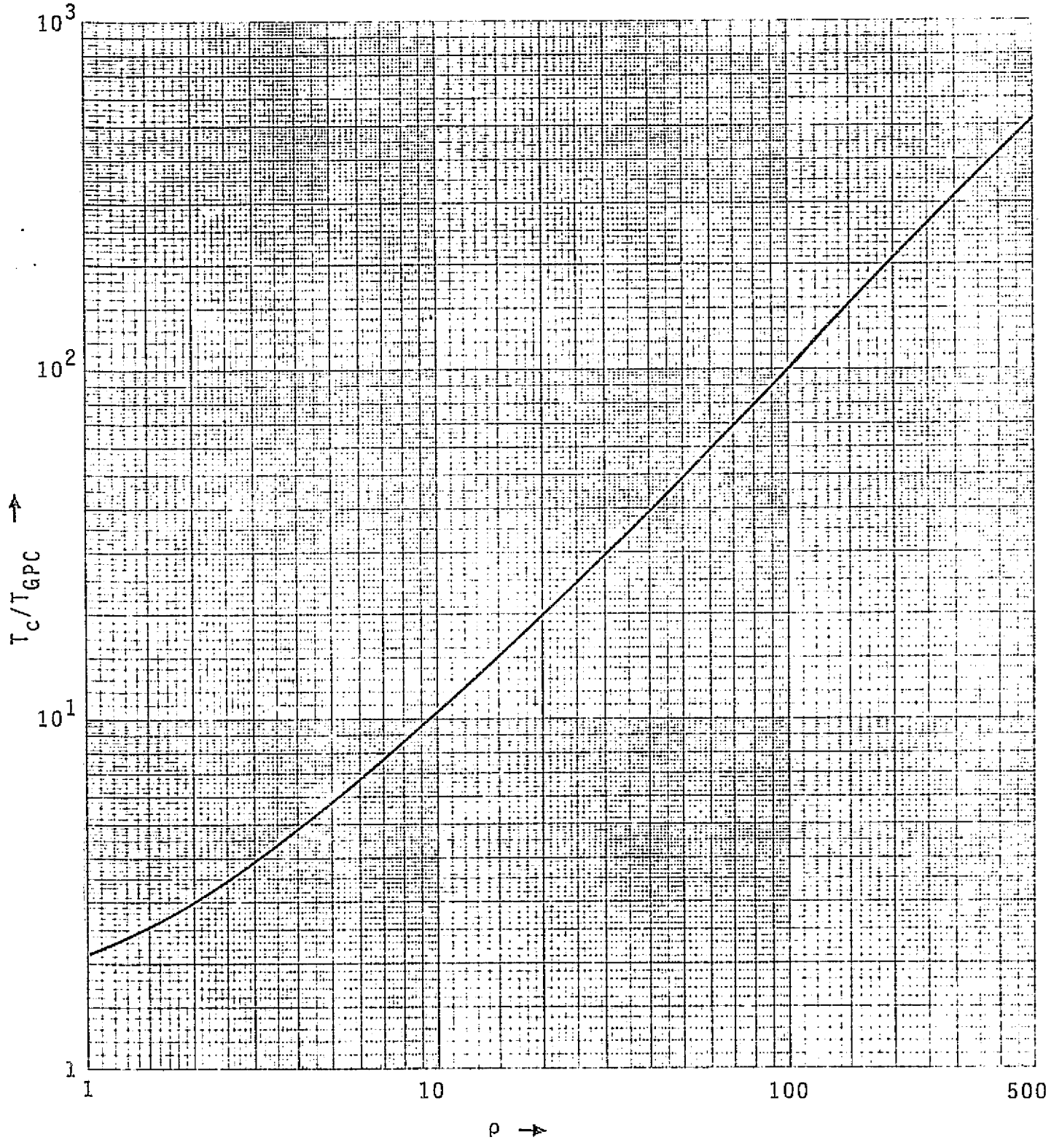


Figure 4-8. Graph showing T_c/T_{GPC} with respect to $\rho = \lambda_{GPC}/\lambda_B$.

5. RECOMMENDATIONS

Based on the investigation carried out under this contract, the following recommendations are made to improve the reliability of the DPS.

1) Because of the critical nature of identification failures, it is strongly recommended that the software design incorporate coding and/or redundant approaches in accessing identification numbers from the core memory. These approaches not only prevent catastrophic failures occurring due to single core element failures but also detect when a correct identification number is generated. Such detection can be used to inform the GPCs to turn themselves off instead of creating interferences on data buses.

2) The synchronization discretes are used at rates of 300/second and because of their vital importance in keeping the computer systems in synchrony, it is strongly suggested that hardware redundancy be incorporated in these discretes. Though software to support synchronization discrete redundancy is a possibility, this does not appear to be a practical solution in view of the rates at which these discretes are used. It is recommended that each synchronization discrete be triplicated with majority voting and possibly a spare discrete. (There are many spare discretes that are not used in the IOP 40/32 discretes.)

3) After a careful review of the other discretes and the manner they are incorporated into the system design, it is concluded that no further significant improvements can be made to the existing design. The present design requirements and implementations support direct/indirect monitoring of the status of the discretes that makes it possible to detect malfunctions. The crew, by observing the information displayed, can deduce the operational status of the discretes such as the Halt/Standby Run discretes, IPL discretes, etc.

The following tests are recommended to test and improve the reliability of the space shuttle:

1) Test the reliability of the synchronization discretes and evaluate their failure rates. Simulate the situation, by means of software, where one or more synchronization discretes fail in each GPC and determine the consequences. Check whether the crew can successfully switch the control to the Backup System within safe time limits.

2) Simulate core memory failures to generate wrong identification numbers and determine the consequences. Test whether the crew can detect the malfunction of the DPS and develop a list of symptoms that the crew can observe to detect identification number failures.

3) Conduct experiments on the discrete circuits to determine the failure rates of the IOP discretes so that the failure rate of the entire DPS due to discrete failures can be determined.

4) Determine the rate of transient synchronization failures by observing the number of retries attempted at each synchronization point.

5) Simulate faults (permanent or transient) on the control and indicator discretes and determine the crew's reaction to these faults. Develop a list of actions that the crew should perform when these faults are observed in flight.

6) Determine the ratio λ_{GPC}/λ_B and see whether λ_B can be improved with better and more reliable circuitry.

6. CONCLUSION

This report presented an analysis of the effects of discrete failures on the Data Processing Subsystem. The analysis included a functional description of each discrete together with a list of software modules that use this discrete. A qualitative description of the consequences that may ensue due to discrete failures is given followed by a probabilistic reliability analysis of the Data Processing Subsystem. Based on the investigation conducted, recommendations were made to improve the reliability of the subsystem.

In the following, some methods are suggested for recovering GPCs lost because of synchronization as well as other discrete failures. Since in the ALT phase no attempts are made to recover the lost GPCs, these methods are applicable only in the OFT phase. Rollback and roll-forward techniques can be profitably used to recover GPCs out of synchrony and include them in Redundant or Common Set computation. In the rollback technique, whenever a GPC is lost from the Redundant or Common Set due to transient errors, during the SSIP phase all the GPCs reset their status to a common reference point in the past whose status has been stored either in Mass Memory units or GPC memory, and resume their computation. This technique slows down computation rates and is preferred only when speed is not critical. In the roll-forward technique, when a GPC fails due to synchronization, instead of removing the GPC from the Redundant or Common Set, the correctly operating GPCs transmit their status and data to this GPC, and then all the GPCs resume their computation. This technique also has the advantage of recovering the GPCs lost due to transient errors, and is faster. These techniques can be easily incorporated in the present software design of the space shuttle to increase the reliability of the Redundant and Common Sets.

REFERENCES

[1] Sklaroff, J. R. , "Redundancy Management Technique for Space Shuttle Computers", IBM J. Res. Develop., Vol. 20, No. 1, pp. 20-28, January 1976

[2] Rockwell International, Data Processing Subsystem Description and Performance Document, SD 74-SH-0230A, Space Division, Downey, California.

[3] NASA, Computer Program Development Specification, Vol. I, Book 1, System Level Description, Hardware, SS-P-0002-110A, Lyndon B. Johnson Space Center, Houston, Texas, June 1975

[4] Rockwell International, Computer, General Purpose Orbiter, Specification, MC615-0001, Space Division Downey, California, August 1974

[5] IBM, Space Shuttle Orbiter Avionics Software, Approach and Landing Test Functional Design Specification, Vol. II - Systems Software, 75-SS-0714, Federal Systems Division, Houston, Texas, 1975

[6] NASA, Computer Program Development Specification, Vol. I, Book 2, System Level Requirements, Software, SS-P-0002-120A, Lyndon B. Johnson Space Center, Houston, Texas, 1975

[7] IBM, System Software Design Specification Part II, ALT Detailed Design Specification, FCOS, UI and SC, 76-SS-0929, Federal Systems Division, Houston, Texas, 1976

BIBLIOGRAPHY

Documents on the Space Shuttle:

NO.	TITLE		DOCUMENT NO.
0001	DATA PROCESSING SUBSYSTEM DESCRIPTION AND PERFORMANCE DOCUMENT (5/75)	RW	SD 74-SH -0230A
0002	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION LEVEL A HARDWARE (6/75)	NASA	SS-P-0002 -110A
0003	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION LEVEL A SOFTWARE (6/75)	NASA	SS-P-0002 -120A
0004	SPECIFICATION - GENERAL PURPOSE COMPUTER (REVISED 10/25/74)	RW	MC615-0001C
0005	SPACE SHUTTLE MULTIFUNCTION CRT DISPLAY SUBSYSTEM DESIGN REVIEW (4/75)	IBM	PO M4J3XMS -483027
0006	SPACE SHUTTLE SOFTWARE ICD: HAL/SDL REV 5 (12/74)	IBM	74-SS-0390
0007	SHUTTLE AVIONICS BLOCK DIAGRAM (REVISED 6/5/75)	NASA	
0008	VIEWGRAPH PRESENTATION	RW	114SSV28-
0009	GPC DISCRETE I/O INTERFACE REQUIREMENTS (11/13/74)	RW	IL382-100 -74-120
0010	INTERFACING WITH GPC DISCRETE INPUTS AND OUTPUTS (10/28/74)	RW	IL383-74 -422
0011	BIASED RECEIVER INTERFACE OPERATION (6/75)	NASA	
0012	SPECIFICATION - MASS MEMORY (REVISED 2/17/75)	RW	MC615-0005B
0013	IBM ADVANCED SYSTEM/4 pi MODEL AP-101 CENTRAL PROCESSING UNIT TECHNICAL DESCRIPTION (3/31/75)	IBM	75-A97-001
0014	IBM ADVANCED SYSTEM/4 pi MODEL AP-101 C/M COMPUTER PRINCIPLES OF OPERATION (12/15/74)	IBM	6246156
0015	SPACE SHUTTLE ADVANCED SYSTEM/4 pi INPUT/OUTPUT PROCESSOR (IOP) (PROTOTYPE MODEL) (12/74)	IBM	6246556
0016	MULTIFUNCTION CRT DISPLAY SET (MCDS) (PROTOTYPE) PRINCIPLES OF OPERATION (4/74) (PRELIMINARY)	IBM	74-67-001

Documents on the Space Shuttle (continued):

NO.	TITLE	DOCUMENT NO.
0017	SPACE SHUTTLE ADVANCED SYSTEM/4 pi INPUT/OUTPUT PROCESSOR (IOP) (PROTOTYPE) FUNCTIONAL DESCRIPTION	IBM 74-A31-016
0018	HAL/S LANGUAGE SPECIFICATION (11/22/74)	IM IR-61-5
0019	HAL/S-FC COMPILER SYSTEM FUNCTIONAL SPECIFICATION	IM IR-59-3
0020	HAL/FCOS INTERFACE CONTROL DOCUMENT (12/16/74)	IBM 74-SS-0390
0021	ADVANCED SYSTEM/4 pi MODEL AP-101 COMPUTER SOFTWARE SYSTEMS MANUAL (2/28/75)	IBM 622-8004H
0022	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION ALT GN&C LEVEL B	NASA SS-P-0002 -410
0023	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION ALT SM LEVEL B	NASA SS-P-0002 -430
0024	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION ALT VEHICLE UTILITY LEVEL B	NASA SS-P-0002 -450
0025	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION OFT GN&C LEVEL B	NASA SS-P-0002 -510
0026	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION OFT SM LEVEL B	NASA SS-P-0002 -530
0027	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION OFT VEHICLE UTILITY LEVEL B	NASA SS-P-0002 -550
0028	COMPUTER PROGRAM DEVELOPMENT SPECIFICATION OFT PL LEVEL B	NASA SS-P-0002 -570
0029	SPECIFICATION - CAUTION AND WARNING ELECTRONICS UNIT	RW MC409-0012B
0030	AMENDMENTS D-04, D-05, D-06 plus any more recent amendments to GPC SPECIFICATION	RW MC615-0001
0031	SPACE SHUTTLE ORBITER BASIC APPROACH & LANDING TEST REFERENCE MISSIONS DOCUMENT (4/14/75)	NASA JSC-09450
0032	GPC DISCRETE LINE ANALYSIS (9/03/75)	McD 1.3-TM-C0304 -131

Documents on the Space Shuttle (continued):

NO.	TITLE	DOCUMENT NO.
0033	SPACE SHUTTLE ADVANCED SYSTEMS/4 pi INPUT/OUTPUT PROCESSOR (IOP) (DEVELOPMENT) FUNCTIONAL DESCRIPTION (5/6/74)	IBM 74-A31-001
0034	SPACE SHUTTLE ORBITER AVIONICS SOFTWARE APPROACH AND LANDING TEST (ALT) FUNCTIONAL DESIGN SPECIFICATION, VOLUME II - SYSTEMS SOFTWARE (July 1975)	IBM 75-SS-0714
0035	ALT CREW ACTIVITY TIMELINE, REVISION B AND APPLICABILITY OF ALT DROP FLIGHT 8 TIMELINE TO OTHER DROP FLIGHTS (3/20/75	McD TM-1.6-F0202-57
0036	PRELIMINARY CREW ACTIVITY TIMELINE FOR APPROACH AND LANDING TEST, DROP FLIGHT 4 (5/12/75)	McD TM-1.6-F0202-71
0037	ORBITER FLIGHT DECK OV101 DISPLAY PANEL CONFIGURATION (2 DRAWINGS) REV. F (6/11/75)	NASA VL70-730101
	INTERCONNECTION DRAWINGS:	NASA VS70-
0038	D&C SUBSYSTEM (7/9/75)	730101
0039	MASS MEMORY & COMPUTER INTERFACE (10/13/75)	720211
0040	COMPUTER POWER & CONTROLS (8/14/75)	720221
0041	COMPUTER SYNCHRONIZATION AND FAIL STATUS (5/29/75)	720231
0042	COMPUTER DATA BUS INTERFACE (5/22/75)	720241
0043	COMPUTER IOP/CPU INTERFACE (10/17/75)	720251
0044	BACKUP FLIGHT CONTROL SYSTEM FLIGHT PROGRAM PROGRAM REQUIREMENTS DOCUMENT, VOLUME I (10/1/75)	RW ML0400-0010
0045	PROGRAM REQUIREMENTS DOCUMENT, VOLUME II (10/1/75)	RW ML0400-0010-001
0046	GPC DISCRETE I/O MECHANIZATION FOR OFT	RW
0047	SPECIFICATION CONTROLLER, BACKUP FLIGH.	RW MC615-0019A
0048	IOP DISCRETE RECEIVER CIRCUIT FOLLOW UP INFORMATION (6/19/75)	IBM C69-75-167
0049	ALT FAILURE MODE EFFECTS ANALYSIS DISPLAYS AND CONTROLS SUBSYSTEM (9/12/75)	RW SD74-SH--0068A
0050	ALT FAILURE MODE EFFECTS ANALYSIS INSTRUMENTATION SUBSYSTEM (9/12/75)	RW SD74-SH-0069A

Documents on the Space Shuttle (continued):

NO.	TITLE	DOCUMENT NO.
0051	ALT FAILURE MODE EFFECTS ANALYSIS DATA PROCESSING & SOFTWARE SUBSYSTEM (9/12/75)	RW SD74-SH -0071A
0052	SYSTEM SOFTWARE DESIGN SPECIFICATION PART II: ALT DETAILED DESIGN SPECIFICATION FCOS, USER INTERFACE, AND SYSTEM CONTROL (1/30/76)	IBM 76-55-0929
0053	UPDATE TO REF. 0052.(2/16/76)	IBM 76-55-0929
0054	IN-HOUSE TESTING OF GPC I/O DISCRETE CIRCUITS	NASA INTERNAL NOTE 75-EG-15

Papers/Reports on the Space Shuttle:

Cooper, A. E. and Chow, W. T., "Shuttle Computer Complex", Report No. 74Z000486, IBM Federal Systems Division, Owego, New York 13827.

Ehlers, H. L. and Peller, J. B., "Space Shuttle Guidance, Navigation and Control Overview", SAE Aerospace Control and Systems Committee Meeting No. 33, Paradise Valley, Arizona, May 1976.

Minott, G. M. and O'Hern, E. A., "Space Shuttle Orbiter Guidance and Control System Design", SAE National Aerospace Engineering and Manufacturing Meeting, San Diego, California, October 1976.

Minott, G. M., Peller, J. B., and Cox, K. J., "Space Shuttle Digital Flight Control System", Report No. SD74-SH-0243, Space Division, Rockwell International, Downey, California, 1974.

O'Hern, E. A., "Space Shuttle Avionics Redundancy Management", AIAA Digital Avionics Systems Conference, Boston, Massachusetts, 1975

Padinha, H. A., "Divergence in Redundant Guidance, Navigation and Control Systems", Report No. 73200401, IBM Federal Systems Division, Owego, New York, 1973.

Rubenstein, S. Z. and Shroyer, L. O., "Digital Processing Subsystem for the Space Shuttle", National Aviation Electronics Conference (NAECON), May 1974.

Sklaroff, J. R. "Redundancy Management Technique for Space Shuttle Computers", IBM Journal of Research and Development, Vol. 20, No. 1, pp. 30-28, January 1976.

LIST OF SPACE SHUTTLE ACRONYMS

```
A           - LEFT INPUT TO ALU
A&P         - ATTITUDE AND POINTING
A/A         - AIR TO AIR
A/C         - AIRCRAFT
A/D         - ANALOG-TO-DIGITAL
A/L         - APPROACH AND LANDING
AA          - ACCELEROMETER ASSEMBLY
ACC         - ACCUMULATOR
ACE         - ACCEPTANCE CHECKOUT EQUIPMENT
ACM         - AQUISITION AND CONTROL MODULE
ACT         - ACTION
ADB         - AUXILIARY MEMORY DATA OUTPUT BUS
ADC         - ANALOG TO DIGITAL CONVERTER
ADC         - AIR DATA COMPUTER
ADI         - ATTITUDE DIRECTOR INDICATOR
ADL         - AVIONICS DEVELOPMENT LABORATORY
ADP         - AUTOMATIC DATA PROCESSING
ADS         - AIR DATA SYSTEM
ADT         - AIR DATA TRANSDUCER
ADTA        - AIR DATA TRANSDUCER ASSEMBLY
ADVANCE     - MEMORY DATA AVAILABLE SIGNAL
AGE         - AIR/GROUND EQUIPMENT
AHP         - PITCH AXIS ATTITUDE HOLD
AI          - ALTITUDE INDICATOR
AIB_GPC_LOCATOR          GPC LOCATOR (SYSTEM CONTROL MODULE)
AIC_GPC_STARTUP          GPC STARTUP (SYSTEM CONTROL MODULE)
AID         - ANALOG INPUT DIFFERENTIAL
AIE_SIP                  SYSTEM INTERFACE PROCESSOR (SYSTEM CONTROL MODULE)
AIG_DEU_LOADER           DEU LOADER (SYSTEM CONTROL MODULE)
AIU         - AVIONICS INTERFACE UNIT
ALC         - AUTOMATIC LIGHT CONTROL
ALPHA       - ANGLE OF ATTACK
ALT         - APPROACH AND LANDING TEST
ALU         - ARITHMETIC/LOGIC UNIT
AMEC        - AFT MASTER EVENTS CONTROLLER
AMI         - ALPHA/MACH CONTROLLER
AMI         - AIRSPEED/MACH INDICATORS
AMT         - APPLICATIONS MODING TABLE
AN          - ALPHANUMERIC
AOA         - ANGLE OF ATTACK
AOD         - ANALOG OUTPUT DIFFERENTIAL
APP         - APPLICATIONS SOFTWARE
APU         - AUXILIARY POWER UNIT
APV         - ATTACH POINT VOLTAGE
ARA_GPC_SWITCH           GPC SWITCH MONITOR (SYSTEM CONTROL MODULE)
ARB_IDLE_OPS             IDLE OPERATIONAL SEQUENCE (SYSTEM CONTROL MODULE)
ARC_GPC_RECONFIG         GPC RECONFIGURATION (SYSTEM CONTROL MODULE)
ARD_BUS_CHG              BUS CONFIGURATION CHANGE (SYSTEM CONTROL MODULE)
ARE_GPC_TABLE_CHG        GPC RECONFIGURATION TABLE CHANGE (SYSTEM CONTROL MODULE)
ARF_OPS_CONFIG_ITEM      OPS CONFIGURATION ITEM PROCESSOR (SYSTEM CONTROL MODULE)
ARG_RECONFIG_MSG      GPC RECONFIGURATION MESSAGE HANDLER (SYSTEM CONTROL MODULE)
ARH_SEC_GPC_RECONFIG     SECONDARY GPC RECONFIGURATION (SYSTEM CONTROL MODULE)
ASA         - AEROSURFACE SERVO AMPLIFIER ASSEMBLY
ASA_IDLE_SPEC         IDLE SPECIALIST FUNCTION - SPEC 0-00 (SYSTEM CONTROL MODULE)
ASB_RD/WRT               READ/WRITE SPECIALIST FUNCTION (SYSTEM CONTROL MODULE)
```

ASC_TIME_MGMT — TIME MANAGEMENT SPECIALIST FUNCTION (SYSTEM CONTROL MODULE)
ASD_DATA_CONTROL — DATA CONTROL SPECIALIST FUNCTION (SYSTEM CONTROL MODULE)
ASELN — AUXILIARY SELECT SIGNAL
ASI — AIRSPEED INDICATOR
ASLCN — AUXILIARY SAR LOAD CLOCK
ASP — AEROSURFACE POSITION
ASPI — AEROSURFACE POSITION INDICATOR
ATA — AVIONICS TEST ARTICLE
ATP — ACTIVATION TEST PROGRAM
ATVCD — ASCENT THRUST VECTOR CONTROL DRIVER
AVVI — ALTITUDE VERTICAL VELOCITY INDICATOR
B* — RIGHT INPUT TO ALU
BA — BOUNDARY ALIGNMENT
BAI — BAROMETRIC ALTITUDE INDICATOR
BCE — BUS CONTROL ELEMENT (IN IOP)
BCH — BOSE, CHAUDHURI, AND HOCQUENGHEM
BCL — BIT COUNT LATCHED (MIA SIGNAL)
BCMUX — BUS CONTROL MULTIPLEXER
BCPTN — EXTERNAL MEMORY ADDRESS PARITY ERROR SIGNAL
BDDSN — BCE DISABLE DISCRETE
BDHI — BEARING AND DISTANCE HEADING INDICATOR
BETA — ANGLE OF SIDE SLIP
BFC — BACKUP FLIGHT CONTROL
BFCS — BACKUP FLIGHT CONTROL SYSTEM
BFCSED — BACKUP FLIGHT CONTROL ENGAGE DISCRETE
BIT — BUILT-IN TEST
BITE — BUILT-IN TEST EQUIPMENT
BMAS — BODY-MOUNTED ACCELEROMETER SYSTEM
BOF — BEGINNING OF FILE
BOT — BEGINNING OF TAPE
BP — "READY" RESET
BPS — BIT PER SECOND
BR — BRANCH
BSR — BRANCH SECTOR REGISTER
BSR — BITE STATUS REGISTER
BSR — BRANCH SECTOR REGISTER
BSYN — MEMORY BUSY SIGNAL
BTE — BTU ERROR TABLE
BTO — BLOCK TIME OUT
BTU — BUS TERMINAL UNIT
BU — BRANCH UNCONDITIONAL
BU — BACKUP
BUN — BITE UPDATE NOTICE
BUOU — BACKUP OPTICAL UNIT
BUSY — MEMORY BUSY SIGNAL
C — CONTROL
C&T — COMMUNICATIONS AND TRACKING
C&W — CAUTION AND WARNING
C-BUS — COMPUTER DATA BUS
C/M — CONTROL MONITOR
C/T — CONTROL AND TIMING
C/W — CAUTION AND WARNING
CAB — COMPUTER ADDRESS BIT
CAB — COMPUTER ADDRESS BUS
CADE — CONTROLLER/ATTITUDE DIRECTOR ELECTRONICS

CALC	– CALCULATE
CAM	– COMPUTER ANNUNCIATION MATRIX
CAPRI	– CAPACITOR RESET INTEGRATOR
CAPRI	– CAPACITOR RATE INTEGRATOR
CARR	– CUSTOMER ACCEPTANCE READINESS REVIEW
CAS	– COMMAND AUGMENTATION SYSTEM
CC	– CROSS-COUPLE
CC	– CHANNEL CONTROLLER
CC	– COMMUNICATIONS CONTROL
CCAT	– CMPTR/CRT ASSIGNMENT TABLE
CCD	– CONSTANTS CHANGE DISPLAY
CCP	– COMMAND COMPUTER (?)
CCR	– CROSS-COUPLE REGISTER
CCT	– CURRENT CONFIGURATION TABLE
CCTV	– CLOSED CIRCUIT TELEVISION
CD	– COMMAND DECODER MDM
CDB	– COMPUTER DATA BUS
CDD	– CONTIGUOUS DATA DESCRIPTOR TABLE
CDR	– COMMANDER
CDR	– COMMAND DESIGN REVIEW
CDW	– COMMAND DATA WORD
CG	– CENTER OF GRAVITY
CGD	– CYCLIC GROUP DESCRIPTOR
CI	– CONFIGURATION INSPECTION
CI	– CREW INTERFACE
CIA	– CONTROL INTERFACE ASSEMBLY
CIA	– COMPUTER INTERFACE ADAPTER
CM	– CONTROL MONITOR
CM	– CONFIGURATION MANAGEMENT
CMD	– COMMAND
CMOS	– COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR
CMPTR	– COMPUTER
COMPOOL	– COMMON DATA POOL AREA
COMSEC	– COMMUNICATIONS SECURITY
CONTN	– CONTINUE SIGNAL
CP	– CLOCK PULSE
CPDS	– COMPUTER PROGRAM DEVELOPMENT SPECIFICATION
CPEI	– COMPUTER PROGRAM END ITEM
CPU	– CENTRAL PROCESSING UNIT
CPUFN	– CPU FAIL SIGNAL
CPUPR	– CPU PRIORITY FOR BUS ACCESS
CR	– CARD READER
CRT	– CATHODE RAY TUBE (IN DU)
CS	– CREW STATION
CSE	– COMPUTER SUPPORT EQUIPMENT
CSECT	– CONTROL SECTION
CSN	– CHANNEL SELECT NOT (SIGNAL TO MIA)
CSS	– CONTROL STICK STEERING
CTS	– COMPUTER TEST SET
CVT	– COMMUNICATION VECTOR TABLE
CW	– CONTROL WORD
CW	– COMMAND WORD
CWEU	– CAUTION AND WARNING ELECTRONICS UNIT
D	– DISCRETE
D&C	– DISPLAY AND CONTROL

```
DAR         - DISPLAY INITIATION AND RESPONSE
D/A         - DIGITAL TO ANALOG
D/C         - DISPLAY AND CONTROL
DACBU       - DIGITAL ACQUISITION AND CONTROL BUFFER UNIT (PCM MASTER)
DAP         - DIGITAL AUTO PILOT
DB          - DATA BUFFER
DB          - DATA BUS
DBC         - DATA BUS COUPLER
DBG         - DATA BUS GROUP
DBI         - DATA BUS INTERFACE UNIT - LAUNCH
DBIA        - DATA BUS ISOLATION AMPLIFIER
DBN         - DATA BUS NETWORK
DC          - DISPLAY COUPLER
DCD_DOWNLIST            GPC DOWNLIST FORMATTER (USER INTERFACE MODULE)
DCI_CON_DATA            DATA CONVERSION (USER INTERFACE MODULE)
DCI_CYC_DISPLAY         CYCLIC DISPLAY PROCESSING (USER INTERFACE MODULE)
DCI_FMT_DATA            DATA FORMATTING (USER INTERFACE MODULE)
DCM         - DISPLAY AND CONTROL MODULE
DCS_SYNC              GPC/PCMMU DATA CYCLE SYNCHRONIZER (USER INTERFACE MODULE)
DD          - DECODER DRIVER
DD&CS       - DEDICATED DISPLAY & CONTROL SYSTEMS
DDL_DWN_LST_CONTROLS    GPC DOWNLIST DATA CONTROLS PROCESSOR (UIM)
DDDU        - DISPLAY DECODER DRIVER UNIT
DDI         - DISCRETE DIGITAL INPUTS
DDM         - DATA DISPLAY MODULE
DDMAN       - DISABLE DMA SIGNAL
DDO         - DISCRETE DIGITAL OUTPUT
DDS         - DETAIL DESIGN SPECIFICATION
DDU         - DIGITAL DISPLAY UNIT
DDU         - DISPLAY DRIVER UNIT
DEG         - DEGREES
DET         - DIGITAL EVENT TIMER
DEU         - DISPLAY ELECTRONICS UNIT (IN MCDS)
DF          - DATA FLOW
DFB         - DISPLAY FORMAT BUFFER
DFI         - DEVELOPEMENT FLIGHT INSTRUMENTATION
DFT         - DISPLAY FORMAT TABLES
DGI_LDB_IO              LDB I/O PROCESSOR (USER INTERFACE MODULE)
DGO_LDB_COORD           LDB OUTPUT MESSAGE COORDINATOR (USER INTERFACE MODULE)
DI          - DISCRETE INPUT
DIA         - DISCRETE I/O REGISTER (OF GPC)
DIH         - DISCRETE INPUT HIGH
DIL         - DISCRETE INPUT LOW
DIM_ICC_COLLECTOR       ICC MESSAGE COLLECTOR (USER INTERFACE MODULE)
DIN         - DIRECT-IN INSTRUCTION
DIPL        - DISPLAY INITIAL PROGRAM LOAD
DIS_PLAY                DISPLAY PRESENTATION AND CONTROL (USER INTERFACE MODULE)
DISP        - DISPLACEMENT
DISP        - DISPLAY FUNCTION
DIT         - DEU INPUT TABLE
DLC         - DATA LOAD CLOCK
DLC         - DELAY LINE CONTROL
DLCN        - DATA LOAD CLOCK (TO LOAD SDR)
DLM_LDB_ROUT            LDB MESSAGE ROUTER (USER INTERFACE MODULE)
DLT         - DEU LOAD TABLE
```

```
DLY         - DELAY
DM          - DIODE MATRIX
DMA         - DIRECT MEMORY ACCESS
DMAIN       - DMA REQUEST SIGNAL
DMC_APP_INT              APPLICATION CONTROL INTERFACE (USER INTERFACE MODULE)
DMC_MCDS_CNT              MCDS DISPLAY CONTROL (USER INTERFACE MODULE)
DMC_NEW_DISPLAY           NEW DISPLAY PROCESSING (USER INTERFACE MODULE)
DMC_SEQ_REQ_PROC          SEQUENCE REQUEST PROCESSING (USER INTERFACE MODULE)
DMC_SUPER               USER INTERFACE CONTROL SUPERVISOR (USER INTERFACE MODULE)
DME         - DISTANCE MEASURING EQUIPMENT
DME_ICC_ROUT              ICC MESSAGE ROUTER (USER INTERFACE MODULE)
DMI_MCDS_IN               MCDS INPUT PROCESSOR (USER INTERFACE MODULE)
DMM_MCDS_PROCESS          MCDS MESSAGE PROCESSOR (USER INTERFACE MODULE)
DMMD        - DISPLAY FORMAT MASS MEMORY DIRECTORY
DMP_MM_MSG_PROC           MASS MEMORY MESSAGE PROCESSOR (USER INTERFACE MODULE)
DMS         - DOCKING MODULE SUBSYSTEM
DMS_MSG_LSF             MESSAGE LINE SUPPORT FUNCTION (USER INTERFACE MODULE)
DNX_BMS                 APPLICATION MODING AND SEQUENCING (USER INTERFACE MODULE)
DO          - DISCRETE OUTPUT
DOD         - DEPARTMENT OF DEFENSE
DOL         - DISCRETE OUTPUT LOW
DP&S        - DATA PROCESSING AND SOFTWARE
DPDC        - DOWNLIST PARAMETER DUMP CONTROL TABLE
DPE         - DATA PATH ERROR TABLE
DPM         - DATA PATH MASK TABLE
DPS         - DATA PROCESSING SUBSYSTEM OR DATA PROCESSING SYSTEM
DR          - DATA REGISTER
DRO         - DESTRUCTIVE READOUT
DSELN       - DELAYED SELECT SIGNAL
DSKY        - DISPLAY AND KEYBOARD
DSR         - DATA SECTOR REGISTER
DSR         - DATA SECTOR REGISTER
DTACN       - DATA ACKNOWLEDGE SIGNAL
DTH_TIME_HOMO     TIME HOMOGENEOUS DATA REQUEST PROCESSOR (USER INTERFACE MODULE)
DTRQN       - DATA REQUEST SIGNAL
DTS         - DATA TRANSFER SYSTEM
DTVC        - DATA TRANSMISSION AND VERIFICATION CONVERTER
DU          - DISPLAY UNIT (IN MCDS)
DWIM        - MICRO ASSIST HARDWARE
E           - SOURCE (MEMORY DRIVER)
E/I         - SOURCE/SINK (MEMORY DRIVER)
E/W         - ENERGY TO WEIGHT RATIO
EA          - EFFECTIVE ADDRESS
EACFM       - ENGAGE ACTUATOR COMMAND FADING MODULE
EACGM       - ELEVON ACTUATOR COMMAND GENERATION MODULE
EAS         - EQUIVALENT AIR SPEED
EC          - EVENTS CONTROLLER
ECI         - EARTH CENTERED INERTIALS
ECLSS       - ENVIRONMENTAL CONTROL AND LIFE SUPPORT SYSTEM
ECRV        - EXPONENTIALLY CORRELATED RANDOM VARIABLES
EDB         - EXTERNAL DATA BUS
EH          - ERROR HANDLING
EIU         - ENGINE INTERFACE UNIT
EMI         - ELECTROMAGNETIC INTERFERENCE
EMU         - EXTENDED MEMORY UNIT
```

EOF - END OF FILE
EOR - END OF REFRESH
EOT - END OF TAPE
EOWN - END OF WORD NOT (SIGNAL FROM MIA TO LRU)
EP/MCM - EXTENDED PERFORMANCE/MODULAR CORE MEMORY
EPS - ELECTRICAL POWER SYSTEM
EQE - EVENT QUEUE ELEMENT
ET - EXTERNAL TANK
ET - ELAPSED TIME
ET - ELAPSED TIME
ETI - ELAPSED TIME INDICATOR
EU - ENGINEERING UNIT
EU - ELECTRONICS UNIT
EVA - EXTRAVEHICULAR ACTIVITY
EXEC - EXECUTE
EXEC - EXECUTIVE
EXTPR - EXTERNAL PRIORITY FOR BUS ACCESS
F - FLOATING POINT
FA - FLIGHT AFT
FAA - FALSE ALARM AVOIDANCE
FACI - FIRST ARTICLE CONFIGURATION INSPECTION
FAT - FLIGHT ATTITUDE TABLE
FC - FLIGHT CONTROL
FC - FLIGHT COMPUTER
FCHL - FLIGHT CONTROL HYDRAULICS LABORATORY
FCMASYNC - INITIAL SSIP SYNCHRONIZATION (FCOS MODULE)
FCMBCEMD - USER MODIFICATION OF BCE CHAINS (FCOS MODULE)
FCMBMAN - USER/GROUND REQUESTED RECONFIGURATION (FCOS MODULE)
FCMBMASK - BUS/DATA PATH MASK MANAGEMENT (FCOS MODULE)
FCMBUSCM - USER/GROUND REQUESTED RECONFIGURATION (FCOS MODULE)
FCMCSYNC - NORMAL SSIP SYNCHRONIZATION (FCOS MODULE)
FCMDISAB - DISABLE TRANSMITTER RECEIVER SUBROUTINE
FCMDISTR - DISABLE TRANSMITTER SUBROUTINE
FCMDSSTR - DISABLE STRING SUBROUTINE
FCMENRCV - ENABLE RECEIVER SUBROUTINE
FCMENSTR - ENABLE STRING SUBROUTINE
FCMENTR - ENABLE TRANSMITTER SUBROUTINE
FCMFDI - FAULT DETECTION IDENTIFICATION (FCOS MODULE)
FCMINMMR - READ BLOCK FROM MM ROUTINE
FCMINSSL - SYSTEM SOFTWARE LOADER (FCOS MODULE)
FCMISYNC - I/O SYNCHRONIZATION (FCOS MODULE)
FCMLINIT - ONE TIME INITIALIZATION ROUTINE
FCMMDSTR - MODE STRING SUBROUTINE
FCMMEPM - MEC-EIU PORT MANAGEMENT SUBROUTINE
FCMNINIT - NORMAL INITIALIZATION (FCOS MODULE)
FCMPINIT - POWER TRANSIENT INITIALIZATION (FCOS MODULE)
FCMPMOD - PROGRAM MODIFICATION (FCOS MODULE)
FCMPOVLY - PROGRAM OVERLAY (FCOS MODULE)
FCMRELST - RELEASE STRINGS SUBROUTINE
FCMSATCN - NOMINAL STRING ASSIGNMENT SUBROUTINE
FCMSFAIL - SYNC FAIL PROCESSOR (FCOS MODULE)
FCMSSYNC - SVC SYNCHRONIZATION (FCOS MODULE)
FCMSVC - CONFIGURATION MANAGEMENT SVC SERVICING (FCOS MODULE)
FCMTSYNC - TIMER SYNCHRONIZATION (FCOS MODULE)
FCOS - FLIGHT COMPUTER OPERATING SYSTEM

FCOS	- FLIGHT CONTROL OPERATIONAL SOFTWARE
FCS	- FLIGHT CONTROL SYSTEM
FCSM	- FLIGHT CONTROL SUBROUTINE MODULE
FCW	- FORMAT CONTROL WORD (FOR DISPLAY)
FD	- FAULT DETECTION
FDA	- FAULT DETECTION ANNUNCIATION
FDBK	- FEEDBACK
FDI	- FAULT DETECTION AND IDENTIFICATION
FDIR	- FAULT DETECTION IDENTIFICATION AND RECOVERY
FDM	- FREQUENCY DIVISION MULTIPLEXER
FDS	- FUNCTIONAL DESIGN SPECIFICATION
FEID	- FLIGHT EQUIPMENT INTERFACE DEVELOPEMENT
FET	- FIELD-EFFECT TRANSISTOR
FF	- FLIGHT FORWARD
FHF	- FIRST HORIZONTAL FLIGHT
FI	- FAULT IDENTIFICATION
FIFO	- FIRST-IN-FIRST-OUT
FIOBCERR	- BCE NO/GO PROCEDURE
FIOCIPR	- IPR SUBROUTINE
FIOCMPLT	- COMPLETION PROCESSING (FCOS MODULE)
FIOCTDPE	- COUNT DATA PATH ERROR PROCEDURE
FIOERRLA	- I/O ERROR HANDLER, LEVEL A (FCOS MODULE)
FIOERRLB	- I/O ERROR HANDLER, LEVEL B (FCOS MODULE)
FIOERRLC	- I/O ERROR HANDLER, LEVEL C (FCOS MODULE)
FIOFCMPT	- ERROR COMPLETION SUBROUTINE
FIOHLTMM	- MASS MEMORY HALT PROCESSOR (FCOS MODULE)
FIOICCF	- ICC FAILURE SUBROUTINE
FIOLGERR	- I/O ERROR LOG PROGRAM (FCOS MODULE)
FIOMCINT	- MSC I/O MONITOR ENTRY POINT
FIOMCMPT	- MSC I/O MONITOR ENTRY POINT
FIOMCNTL	- MSC CONTROL PROGRAM (FCOS MODULE)
FIOMMCMP	- MM COMPLETION PROCESSING SUBROUTINE
FIOMMCV	- MM CHECKSUM VERIFICATION SUBROUTINE
FIOMMDSP	- MM INITIATE REQUEST SUBROUTINE
FIOMMMGR	- MASS MEMORY MANAGEMENT ROUTINE (FCOS MODULE)
FIOMMMSC	- MASS MEMORY MSC ROUTINE (FCOS MODULE)
FIOMMPII	- MM PROCESS INCOMING IOQE'S SUBROUTINE
FIOMMSTR	- MM ATTEMPT TO START REQUEST SUBROUTINE
FIOMMTHR	- MM MONITOR OUTSTANDING REQUESTS SUBROUTINE
FIOMMTQE	- MM BUILD AND CHAIN TQE SUBROUTINE
FIOMNTR	- MSC I/O MONITOR PROGRAM (FCOS MODULE)
FIOMPSDO	- MSC PSEUDO BUSY PROGRAM (FCOS MODULE)
FIOMRAW	- MSC I/O MONITOR ENTRY POINT
FIOMSCTO	- MSC TIMEOUT PROCEDURE
FIOMSETB	- MSC BCE RESET PROGRAM (FCOS MODULE)
FIOMSFD	- SET FAIL DISCRETES PROGRAM (FCOS MODULE)
FIONCMPT	- NORMAL COMPLETION SUBROUTINE
FIOPDISP	- IOP DISPATCHING (FCOS MODULE)
FIOPROT	- PROTECTED TRANSACTION SUBROUTINE
FIOPSDTO	- MSC PSEUDO TIMEOUT PROCEDURE
FIOPURGE	- TERMINATION PROCESSING (FCOS MODULE)
FIORESET	- IOP RESET PROCEDURE
FIORSLV	- MASS MEMORY CONTENTION RESOLUTION ROUTINE (FCOS MODULE)
FIOSVC	- I/O SVC SERVICING (FCOS MODULE)
FKB	- FLIGHT DISPLAY KEYBOARD

FLR	– FLIGHT LOG RECORDER
FM	– FREQUENCY MODULATION
FMEC	– FORWARD MASTER EVENTS CONTROLLER
FO/FS	– FAIL OPERATIONAL/FAIL SAFE
FOF	– FIRST OPERATIONAL FLIGHT
FOV	– FIELD OF VIEW
FP	– FIXED POINT
FP	– FLOATING POINT
FPMCANCL	– CANCEL PROCESSING (FCOS MODULE)
FPMCLOSE	– CLOSE PROCESSING (FCOS MODULE)
FPMDISP	– PROCESS DISPATCHING (FCOS MODULE)
FPMERLOG	– ERROR LOGGING (FCOS MODULE)
FPMEVAL	– EVENT EVALUATOR (FCOS MODULE)
FPMEVDEQ	– EVENT DEQUEUE PROCESSING (FCOS MODULE)
FPMEVENQ	– EVENT QUEUE GENERATION (FCOS MODULE)
FPMFCLOS	– FORCED CLOSE PROCESSING (FCOS MODULE)
FPMIEPCT	– INHIBIT/ENABLE APPLICATION PROCESSES (FCOS MODULE)
FPMIHIM	– INSTRUCTION MONITOR INTERRUPT HANDLER (FCOS MODULE)
FPMIHMC	– MACHINE CHECK INTERRUPT HANDLER (FCOS MODULE)
FPMIHPC2	– TIMER QUEUE ELEMENT EXPIRATION (FCOS MODULE)
FPMIHPGM	– PROGRAM INTERRUPT HANDLER (FCOS MODULE)
FPMMTURM	– MTU REDUNDANCY MANAGEMENT (FCOS MODULE)
FPMOPSCN	– OPS CANCEL PROCESSING (FCOS MODULE)
FPMREL	– RELEASE RESOURCE LOCK (FCOS MODULE)
FPMRES	– RESERVE RESOURCE LOCK (FCOS MODULE)
FPMRESET	– SET EVENT STATE TO FALSE (FCOS MODULE)
FPMSCHED	– PROCESS SCHEDULING (FCOS MODULE)
FPMSDERR	– PROCESS ERROR RECOVERY (FCOS MODULE)
FPMSET	– SET EVENT STATE TO TRUE (FCOS MODULE)
FPMSIGNL	– PULSE EVENT STATE (FCOS MODULE)
FPMSTAT	– PRIO FUNCTION (FCOS MODULE)
FPMSTAT	– APPLICATION ERROR NUMBER REQUEST (FCOS MODULE)
FPMSVC	– SVC HANDLING (FCOS MODULE)
FPMSWTCH	– PROCESS SWITCHING (FCOS MODULE)
FPMTERM	– TERMINATE PROCESSING (FCOS MODULE)
FPMTMDEQ	– TIMER DEQUEUE PROCESSING (FCOS MODULE)
FPMTMENQ	– TIME QUEUE GENERATION (FCOS MODULE)
FPMTMHAL	– APPLICATIONS REQUESTS FOR TIME AND DATE (FCOS MODULE)
FPMUPMTU	– MASTER TIMING UNIT UPDATES (FCOS MODULE)
FPMUPRIO	– UPDATE PRIORITY FUNCTION (FCOS MODULE)
FPMWAIT	– WAIT PROCESSING (FCOS MODULE)
FRL	– FRAME REFERENCE LINE
FRT	– FLIGHT READINESS TEST
FRT	– FREQUENCY RESPONSE TEST
FS	– FAULT SUMMARY
FS	– FULL SCALE
FSP	– FAULT SUMMARY PAGE
FSRR	– FLIGHT SOFTWARE READINESS REVIEW
FSSR	– FUNCTIONAL SUBSYSTEMS SOFTWARE REQUIREMENTS DOCUMENT
FSW	– FLIGHT SOFTWARE PACKAGE
FTP	– FUNCTIONAL TEST PROGRAM
FVF	– FIRST VERTICAL FLIGHT
FW	– FULLWORD
G	– GRAVITY
G&C	– GUIDANCE AND CONTROL

GLN	- GUIDANCE AND NAVIGATION
GC	- GENERAL COMPUTER
GCWN	- GATE COMMAND WORD SIGNAL
GLKON	- GATED LOCKOUT SIGNAL (IPL MODE)
GMT	- GREENWICH MEAN TIME
GN&C	- GUIDANCE, NAVIGATION AND CONTROL
GND	- GROUND
GPC	- GENERAL PURPOSE COMPUTER (CPU AND IOP)
GPTE	- GENERAL PURPOSE TEST EQUIPMENT
GPIN	- GRANT PRIORITY I TO DMA
GRON	- GATE TRI-STATE DRIVERS SIGNAL
GRT	- GPC RECONFIGURATION TABLE
GSE	- GROUND SUPPORT EQUIPMENT
GSIU	- GROUND STANDARD INTERFACE UNIT
GST	- GPC STATUS TABLE
H/W	- HARDWARE
HAC	- HEADING ALIGNMENT CYLINDER
HAL/S	- PROGRAMMING LANGUAGE
HFT	- HORIZONTAL FLIGHT TEST
HGA	- HIGH GAIN ANTENNA
HSI	- HORIZONTAL SITUATION INDICATION
HSP	- HYDRAULIC SYSTEM PRESSURE
HW	- HALFWORD
I	- SINK (MEMORY DRIVER)
I/O	- INPUT/OUTPUT
IA	- INDIRECT ADDRESS
IA	- INPUT AXIS
IAS	- INDICATED AIRSPEED
IBCMUX	- INNER BUS CONTROL MULTIPLEXER
IBM	- INTERNATIONAL BUSINESS MACHINES
IC	- INSTRUCTION COUNTER
ICC	- INTERCOMPUTER COMMUNICATIONS
ICC	- INTERCOMPUTER CHANNEL
ICC	- INTER-COMPUTER CHANNEL (FCOS MODULE)
ICD	- INTERFACE CONTROL DOCUMENT
ID	- INSIDE DIAMETER
ID	- IDENTIFICATION NUMBER
IDPS	- INTERFACE DIGITAL PROCESSOR
IMM	- IMMEDIATE
IMS	- INHIBIT MAIN STORE
IMS/POR	- INHIBIT MAIN STORE/POWER ON RESET SIGNALS
IMT	- ICC MESSAGE TABLE
IMU	- INERTIAL MEASUREMENT UNIT
INTRPT	- INTERRUPT
IOA	- I/O ADAPTER
IOB	- I/O BUX
IOM	- INPUT/OUTPUT MODULE
IOP	- INPUT/OUTPUT PROCESSOR
IOPIMS	- INPUT/OUTPUT PROCESSOR INHIBIT MAIN STORE
IOPT	- PCMMU I/O PARAMETER TABLE
IOQE	- INPUT/OUTPUT QUEUE ELEMENT
IPL	- INITIAL PROGRAM LOAD
IPLC	- INITIAL PROGRAM LOAD COMPLETE
IPLS	- INITIAL PROGRAM LOAD START
IPR	- INPUT PROBLEM REPORT

IRIG — INTER-RANGE INSTRUMENTATION GROUP TELEMETRY STANDARDS
ISS — INHIBIT/OVERRIDE SUMMARY SNAPSHOT DISPLAY
ITA — INTEGRATED TEST AREA
ITO — INITIAL TIMEOUT
IU — INTERFACE UNIT
IUA — INTERFACE UNIT ADDRESS
IVA — INTRAVEHICULAR ACTIVITY
JCL — JOB CONTROL LANGUAGE
JED — JULIAN EPHEMERIS DATA
KB — KEYBOARD
KBPS — KILOBITS PER SECOND
KBU — KEYBOARD UNIT (IN MCDS)
KBUA — KEYBOARD UNIT ADAPTER
KM/HR — KILOMETER/HOUR
KOPS — THOUSANDS OF OPERATIONS PER SECOND
KVT — KEYBOARD VERIFICATION TABLE
KYBD — KEYBOARD
L/D — LIFT TO DRAG
LBR — LOAD BASE REGISTER
LC — INDUCTOR-CAPACITOR
LCC — LOAD CROSS-COUPLE REGISTER
LCMD — LRU COMMAND SIGNAL TO MIA
LCOM — LOGIC CONTROL OUTPUT MODULE
LDA — LRU DATA AVAILABLE SIGNAL TO MIA
LDB — LAUNCH DATA BUS
LDS — LANDING/DECELERATION SUBSYSTEM
LGT — LOCK GROUP TABLE
LIB — LEFT INBOARD
LOB — LEFT OUTBOARD
LPS — LAUNCH PROCESSOR SYSTEM
LPS — LOAD PROGRAM STATUS
LRE — LRU RECEIVE ENABLE SIGNAL TO MIA
LRECL — LOGICAL RECORDS OF FIXED LENGTH
LRM — LRU RESET SIGNAL TO MIA
LRU — LINE REPLACEABLE UNIT
LS — LOCAL STORE
LS — LAUNCH SEQUENCE PROCESSOR
LSB — LEAST SIGNIFICANT BIT
LSI — LARGE-SCALE INTEGRATION
LTE — LRU TRANSMIT ENABLE SIGNAL TO MIA
LTOR — LOAD TIMEOUT REGISTER
LVDT — LINEAR VOLTAGE DIFFERENTIAL TRANSFORMER
M — METERS
MA — MICRO ARCHITECTURE
MA — MILLIAMPERE
MACH — VELOCITY RELATIVE TO THE SPEED OF SOUND
MACRO — MERGE AND CORRELATE RECORDED OUTPUT
MACT — MISCELLANEOUS APPLICATION CONTROL TABLE
MAEP — MINIMUM AUTOLAND ENTRY POINT
MAL — MALFUNCTION
MAT — MCDS ALLOCATION TABLE
MBUS — MAIN BUS
MC — MACHINE CHECK INTERRUPT
MCDS — MULTIFUNCTION CATHODE RAY TUBE DISPLAY SYSTEM
MCHRN — MACHINE RESET SIGNAL

MCIU	- MANIPULATOR CONTROLLER INTERFACE UNIT
MCIU	- MASTER CONTROLLER INTERFACE UNIT
MCM1N	- EXTERNAL MEMORY CONFIGURATION DISCRETE
MCM2N	- EXTERNAL MEMORY CONFIGURATION DISCRETE
MC14N	- EXTERNAL MEMORY CONFIGURATION DISCRETE
MC15N	- EXTERNAL MEMORY CONFIGURATION DISCRETE
MDB	- MAIN MEMORY, DATA OUTPUT BUS
MDM	- MODULATOR DEMODULATOR
MDM	- MULTIPLEXER/DEMULTIPLEXER
MDR	- MIA DATA READY SIGNAL TO LRU
ME	- MAIN ENGINE
MEC	- MASTER EVENTS CONTROLLER
MECO	- MAIN ENGINE CUTOFF
MET	- MISSION ELAPSED TIME
MF	- MAJOR FUNCTION
MFO	- MULTIFUNCTION OVERLAY
MIA	- MULTIPLEXER INTERFACE ADAPTER
MIB	- MULTILAYER INTERCONNECTION BOARDS
MM	- MASS MEMORY
MMHG	- MILLIMETERS OF MERCURY
MML	-
MMU	- MASS MEMORY UNIT
MOM	- MOMENTARY
MPOR	- MASTER POWER-ON RESET
MPS	- MODULAR POWER SUPPLY
MPS	- MAIN PROPULSION SYSTEM
MSB	- MOST SIGNIFICANT BIT
MSBLS	- MICROWAVE SCAN BEAM LANDING SYSTEM
MSC	- MASTER SEQUENCE CONTROLLER (IN IOP)
MSC	- MODING, SEQUENCE AND CONTROL
MSG	- MESSAGE
MSI	- MEDIUM-SCALE INTEGRATION
MSS	- MISSION SPECIALIST STATION
MSU	- MASS STORAGE UNIT
MT	- MISSION TIME
MTC	- MASTER THRUST CONTROLLER
MTO	- BCE MAXIMUM TIMEOUT
MTS	- MICROPROGRAMMED TEST SYSTEM
MTS	- MAGNETIC TAPE SYSTEM
MTU	- MASTER TIMING UNIT
MUBN	- MIA BUSY NOT SIGNAL TO LRU
MUX	- MULTIPLEXER
N/A	- NOT APPLICABLE
N/L	- NORMAL/LATERAL
NAS	- NONAVIONICS SIMULATORS
NASA	- NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
NAV	- NAVIGATION
NEP	- NORMAL ENTRY POINT
NMI	- NAUTICAL MILES
NOP	- NO OPERATION
NRZ	- NON-RETURN-TO-ZERO
NSAT	- NOMINAL STRING ASSIGNMENT TABLE
NSP	- NETWORK SIGNAL PROCESSOR
NWS	- NOSEWHEEL STEERING
OASCB	- ORBITER AVIONICS SOFTWARE CONTROL BOARD

OCC – OVERCURRENT COMPARATOR
OD – OUTSIDE DIAMETER
ODG – OUTPUT DATA GATE (?)
ODR – OUTPUT DATA REDUNDANCY
OF – ORBITAL FLIGHT
OFI – OPERATIONAL FLIGHT INSTRUMENTATION
OFP – OPERATIONAL FLIGHT PROGRAM
OFST – OFFSET
OFT – ORBITAL FLIGHT TEST
OI – OPERATIONAL INSTRUMENTATION
OMS – ORBITER MANEUVERING SUBSYSTEM
OP – OPERATION
OPS – OPERATIONAL SEQUENCE
OVC – OVERVOLTAGE COMPARATOR
P/L – PAY LOAD
P/N – POSITIVE/NEGATIVE
P/S – POWER SUPPLY
P/S – PARALLEL TO SERIAL CONVERTERS
PACM – PITCH AXIS CONTROL MODULE
PBAN – POLYBUTADIENE ACRYLONETRILE
PBI – PUSHBUTTON INDICATOR
PC – PROGRAM COUNTER
PCB – PRINTED CIRCUIT BOARD
PCI – PROGRAM CONTROLLED INPUT
PCM – PULSE CODE MODULATION
PCMMU – PULSE CODE MODULATION MASTER UNIT
PCO – PROGRAM CONTROLLED OUTPUT
PCSM – PITCH AXIS CONTROL SUBMODULE
PCT – PROCESS CONTROL TABLE
PDE – PROCESS DIRECTORY ENTRY
PDI – PAYLOAD DATA INTERLEAVER
PDR – PRELIMINARY DESIGN REVIEW
PE – PROGRAM EXCEPTION INTERRUPT
PE – PARITY ERROR
PEA – PRELIMINARY EFFECTIVE ADDRESS
PET – PHASED TIME ELAPSED
PFCR – PRIMARY FLIGHT CONTROL RESET
PFCS – PRIMARY FLIGHT CONTROL SYSTEM
PGS – POWER GENERATION SUBSYSTEM
PHS – PAYLOAD HANDLING STATION
PI – PUT-AWAY INITIALIZATION
PIC – PYRO INITIATOR CONTROLLER
PL – PAYLOAD
PLD – PAYLOAD
PLD – PROGRAM LISTING DOCUMENT
PLM – PAYLOAD MANAGEMENT
PLM – PAYLOAD MONITORING
PLT – PILOT
PM – PERFORMANCE MONITOR
PM – PERFORMANCE MANAGEMENT
PMAD – PERFORMANCE MONITOR ANNUNCIATOR DRIVER
PMIA – PARALLEL MULTIPLEXER INTERFACE ADAPTER
PMS – PERFORMANCE MONITORING SYSTEM
PMU – PCM (PULSE CODE MODULATION) MASTER UNIT
PO – POWER ON

PD	–
POD	– PARAMETER OVERRIDE DISPLAY
POI	– POWER ON/OFF INTERRUPT
POID	– POWER OFF INTERRUPT DELAYED
POIL	– POWER SUPPLY INHIBIT LINE
POR	– POWER-ON RESET
PRD	– PROGRAM REQUIREMENTS DOCUMENT
PRF	– PULSE REPETITION FREQUENCY
PRI	– PRIMARY
PRIO	– PRIORITY FUNCTION
PRO	– PROCEED
PROM	– PROGRAMMABLE READ-ONLY MEMORY
PS	– POWER SUPPLY
PSA	– PREFERRED STORAGE AREA
PSA	– PREFERRED STORAGE AREA
PSBIT	– POWER SUPPLY BUILT-IN TEST
PSP	– PAYLOAD SIGNAL PROCESSOR
PSW	– PROGRAM STATUS WORD
PTD	– PROGRAM TESTING DOCUMENT
PUT	– POWER UP TRIGGER (?)
PVT	– PRESSURE VOLUME TEMPERATURE
PWR	– POWER INTERRUPT
R	– REPEAT
R/M	–
R/W	– READ/WRITE
RA	– RADAR ALTIMETER
RACM	– ROLL AXIS CONTROL MODULE
RAD	– RADIANS
RAI	– RADAR ALTIMETER INDICATOR
RALT	– RADAR ALTIMETER
RAM	– RANDOM ACCESS MEMORY
RAW	– REPEAT UNTIL ALL BCES ARE WAITING
RC	– RESISTOR-CAPACITOR
RCC	– REDUNDANCY CONNECTION CONTROL
RCS	– RECEIVED COMMAND SYNC SIGNAL FROM MIA TO LRU
RCS	– REACTION CONTROL SYSTEM
RDD	– REQUIREMENT DEFINITION DOCUMENT
RDL	– RECEIVE DATA LONG (FORMAT)
RDP	– REQUIREMENTS DEVELOPEMENT PLAN
RDS	– RECEIVE DATA SHORT (FORMAT)
RDW	– RESPONSE DATA WORD (FROM DEU)
REC	– RECEIVE
REGCLK	– REGISTER CLOCK SIGNAL FROM MIA TO LRU
RET	– RETURN
RF	– RADIO FREQUENCY
RFD	– REQUIREMENT FORMULATION DOCUMENT
RFI	– RADIO FREQUENCY INTERFERENCE
RG	– RATE GYRO
RGA	– RATE GYRO ASSEMBLY
RGT	– RATE GROUP TABLE
RHC	– ROTATIONAL HAND CONTROLLER
RI	– REGISTER IMMEDIATE
RIB	– RESET INDICATOR BIT
RIB	– RIGHT INBOARD
RICC	– REMOTE INTERCOMPUTER COMMUNICATIONS INTERFACE

RJDA – REACTION JET DRIVER AFT
RJDF – REACTION JET DRIVER FORWARD
RJOD – REACTION JET OMS DRIVER
RM – REDUNDANCY MANAGEMENT
RMC – REDUNDANCY MANAGEMENT CONTROL
ROB – RIGHT OUTBOARD
ROM – READ-ONLY MEMORY
ROS – READ-ONLY STORE
ROSAR – READ ONLY STORE ADDRESS REGISTER
ROSBR – MICROPROGRAM LINK REGISTER
ROSDR – READ ONLY STORE DATA REGISTER
RPM – REVOLUTIONS PER MINUTE
RPTA – RUDDER PEDAL TRANSDUCER ASSEMBLY
RR – REGISTER TO REGISTER
RR – RENDEZVOUS RADAR
RREU – RENDEZVOUS RADAR ELECTRONICS UNIT
RS – REGISTER TO STORAGE
RS – REDUNDANT SETS
RS – REDUNDANCY STATUS
RSIFN – RESET INTERFACE SIGNAL
RTC – REAL-TIME COMMAND
RTCE – ROTATION AND TRANSLATION CONTROL ELECTRONICS
RTLS – RETURN TO LAUNCH SITE
RWM – READ/WRITE MEMORY
S – SIGN BIT
S – POWER TRANSIENT FLAG (IN KOH)
S/C – SIGNAL CONDITIONER
S/D – SKELETON/DYNAMIC
S/W – SOFTWARE
SACS – SYSTEM SOFTWARE AVIONICS COMMAND SUPPORT
SAIL – SHUTTLE AVIONICS INTEGRATION LABORATORY
SAR – STORAGE ADDRESS REGISTER
SAT – STRING ASSIGNMENT TABLE
SATS – SHUTTLE AVIONICS TEST SYSTEM
SB – SPEEDBRAKE
SBAS – S-BAND ANTENNA SWITCH
SBHC – SPEEDBRAKE HAND CONTROLLER
SBMC – SPEEDBRAKE MANUAL CONTROL
SBTC – SPEEDBRAKE THRUST CONTROLLER
SC – SUPERVISOR CALL INTERRUPT
SC – STORAGE COMPLETE (FOR POWER DOWN)
SC – SYSTEM CONTROL SOFTWARE
SCB – SOFTWARE CONTROL BOARD
SCC – SCM COMPARISON DISPLAY
SCLN – STORAGE ADDRESS REGISTER LOAD LOCK
SCM – SUBSYSTEM CONFIGURATION MANAGEMENT
SCM – SUBSYSTEM CONFIGURATION MONITORING
SCM – SYSTEM CONTROL MODULE
SCSN – SPLIT CYCLE STORE COMMAND LINE
SCT – SUBCOM TABLE
SCU – SEQUENCE CONTROL UNIT
SCW – SEARCH COMPLETE WORD
SDAN – BIT COUNT ERROR SIGNAL FROM MIA TO LRU
SDF – SIMULATION DATA FILE
SDL – SOFTWARE DEVELOPMENT LABORATORY

SDR	- STORAGE DATA REGISTER
SDR	- SERIES DISSIPATIVE REGULATOR
SDR	- SOFTWARE DESIGN REQUIREMENTS
SDS	- SHUTTLE DYNAMICS SIMULATOR
SDT	- STRING DEFINITION TABLE
SELN	- SELECT (MEMORY INITIATE SIGNAL)
SEQNG	- SEQUENCING
SEV	- MESSAGE VALIDITY TEST
SF	- SCALE FACTOR
SF	- SELECTION FILTER
SFC	- SELCTION FILTER CONTROL
SG	- SYMBOL GENERATION
SGLS	- SPACE-GROUND LINK SUBSYSTEM
SHS	- SIMULATION HARDWARE SYSTEM
SI	- STORAGE IMMEDIATE
SIB	- SET INDICATOR BIT
SIM	- SIMULATION
SIO	- SERIAL I/O
SIP	- SYSTEM INTERFACE PROCESSOR
SM	- SYSTEM MANAGEMENT
SMCM	- SMALL MODULAR CORE MEMORY (IN DEU)
SMRD	- SPIN MOTOR RUN DIRECTOR/DIRECTION
SMSC	- SOFTWARE MODING, SEQUENCING AND CONTROL
SMT	- STRING MODE TABLE
SOCS	- SUBSYSTEM OPERATING AND CHECKOUT SYSTEM
SOP	- SOFTWARE OPERATING PROGRAM
SOW	- STATEMENT OF WORK
SPDBK	- SPEEDBRAKE
SPEC	- SPECIALIST FUNCTION
SPGAI	- SURFACE POSITION GIMBAL ANGLE INDICATOR
SPI	- SURFACE POSITION INDICATOR
SPL	- SCRATCH PAD LINE
SPU	- SMALL PROCESSOR (IN DISPLAY CONTROLLER)
SQ	- SUPER QUEUE
SRB	- SOLID ROCKET BOOSTER
SRM	- SOLID ROCKET MOTOR
SRS	- SHORT REGISTER TO STORAGE
SRU	-
SSAD	- SOFTWARE SYSTEM ANALYSIS DOCUMENT
SSC	- STORE STATUS AND CLEAR
SSD	- SPACECRAFT SOFTWARE DIVISION
SSDD	- SOFTWARE SYSTEM DESIGN DOCUMENT
SSIP	- SYSTEMS SOFTWARE INTERFACE PROCESSING
SSL	- SYSTEM SOFTWARE LOADER
SSO	- SYSTEMS SOFTWARE OFFICE
SSW	- STORE STATUS AND WAIT
ST	- STAR TRACKER
STADU	- SYSTEM TERMINATION AND DISPLAY UNIT
STDN	- SPACE TRACKING AND DATA NETWORK
STP	- SELF-TEST PROGRAM
STP1N	- STOP CONTROL SIGNAL
STP2N	- STOP CONTROL SIGNAL
STRCN	- DMA STORE CONTROL SIGNAL
STRN	- PURE STORE CONTROL SIGNAL (EXTERNAL MEMORY)
STRPN	- STORE PROTECT SIGNAL

SVC	- SUPERVISOR CALL INSTRUCTION
SYRN	- SYSTEM RESET SIGNAL
SYS	- SYSTEM INTERRUPT
T/F	- TRUE/FALSE
T/R	- TRANSMIT/RECEIVE
TAC	- TACAN INPUT CARD
TACAN	- TACTICAL AIR NAVIGATION
TACFM	- TAKEOVER ACTUATOR COMMAND FADING MODULE
TAEM	- TERMINAL AREA ENERGY MANAGEMENT
TAS	- TRUE AIRSPEED
TAT	- TOTAL AIR TEMPERATURE
TATI	- TOTAL AIR TEMPERATURE INDICATOR
TB	- TALKBACK
TBD	- TO BE DETERMINED
TCS	- TRANSMIT COMMAND SYNC
TCS	- TEST CALL SUPERVISOR
TCS-S	- TEST CONTROL SUPERVISOR SEQUENCE PROCESSOR
TCS-1	- TEST CONTROL SUPERVISOR SINGLE COMMAND PROCESSOR
TCV	- TEMPERATURE-CONTROLLED VOLTAGE REGULATORS
TDL	- TRANSMIT DATA LONG (FORMAT)
TDRS	- TRACKING AND DATA RELAY SATELLITE
TDRSS	- TRACKING AND DATA RELAY SATELLITE SYSTEM
TDS	- TRANSMIT DATA SHORT (FORMAT)
TFL	- TELEMETRY FORMAT LOAD
TFOV	- TOTAL FIELD OF VIEW
TFS	- TELEMETRY FORMAT SELECTION
TGAP	- INTERWORD GAP TIME (?)
THC	- TRANSLATIONAL HAND CONTROLLER
THCB	- TIME HOMOGENEOUS DATA SET CONTROL/BUFFER TABLE
THXR	- TIME HOMOGENEOUS DATA SET CROSS REFERENCE TABLE
TICM	- TEST INTERFACE CONTROL MODULE
TLM	- TELEMETRY
TMP	- TIME MANAGEMENT PROCESSOR
TO	- TIMEOUT
TOC	- TEST OPERATIONS CENTER
TQE	- TIMER QUEUE ELEMENT
TR	- TRANSMITTER/RECEIVER
TRANS	- TRANSFER
TRSD	- TEST REQUIREMENTS SPECIFICATION DOCUMENT
TSEN	- TRISTATE REGISTER ENABLE NOT SIGNAL FROM MIA TO LRU
TSW	- TEST SOFTWARE PACKAGE
TTL	- TRANSISTOR/TRANSISTOR LOGIC
TTY	- TELETYPEWRITER
TV	- TELEVISION
TVC	- THRUST VECTOR CONTROL
TVCD	- THRUST VECTOR CONTROL DRIVER
UCP	- USER-WRITTEN CONTROL PROGRAM
UDF	- UTILITY AND DATA FLOW
UDSB	- UI DOWNLIST STORAGE BUFFER
UHF	- ULTRA-HIGH FREQUENCY
UI	- USER INTERFACE SOFTWARE
UIM	- USER INTERFACE MODULE
UTC	- UNIVERSAL TIME COMPENSATED
UTE	- UNIVERSAL TEST EQUIPMENT
UT1	- UNIVERSAL TIME 1

V - VALIDITY FLAG (IN RDH)
VCO - VOLTAGE-CONTROLLED OSCILLATOR
VDS - VEHICLE DYNAMIC SIMULATOR SYSTEM
VGMCM - VERTICAL GYRO MISALIGNMENT COMPENSATION MODULE
VREF - VOLTAGE REFERENCE
VSI - VERTICAL SPEED INDICATOR
W/P1 (OR 2) - WAY POINT 1 (OR 2)
WAT - WAIT
WBD - WIDE BAND
WBFDM - WIDE BAND FREQUENCY DIVISION MULTIPLEXER
WDAL - WHEELS DOWN AND LOCKED
WIX - WAIT FOR INDEX INSTRUCTION
WONG - WEIGHT ON NOSE GEAR
WOW - WEIGHT ON WHEELS
WR - WORKING REGISTER
WSC - WIDE BAND SIGNAL CONDITIONER
XDDSN - TRANSMIT DISABLE DISCRETE
XFER - TRANSFER
XMT - TRANSMITTER
YACM - YAW AXIS CONTROL MODULE
54HXX - HIGH SPEED SN5400 TTL CIRCUITS
54MXX - STANDARD SPEED SN5400 TTL CIRCUITS
54SXX - HIGHEST SPEED SN5400 TTL CIRCUITS