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(NASA-CF-148766) A MEMORY-MAPPED OUTPUT
INTERFACE: OMEGA NAVIGATION OUTPUT DATA
FROM THE JOLT (TM) MICROCOMPUTER (Ohio
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A MEMORY-MAPPED OUTPUT INTERFACE: OMEGA NAVIGATION
OUTPUT DATA FROM THE JOLT(TM) MICROCOMPUTER

A hardware interface which allows both digital and analog data output from the JOLT microcomputer is described in context of the Ohio University software-based Omega Navigation Receiver.

by

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I. INTRODUCTION

During the development of the Ohio University software-based Omega receiver prototype (see Ref. 1,2), an output device interface became necessary so as to compare software outputs with similar outputs of former hardware modules. The software receiver is being compared with the Ohio University Omega receiver prototype produced for NASA.*

The interface hardware described in this paper is designed for output of six (or eight with simple extensions) bits of binary output in either digital or analog form in response to a memory store command from the JOLT(TM) microcomputer being designed into the receiver.

The interface has been produced in breadboard form and is operational as an evaluation aid for the software Omega receiver.

II. CIRCUIT DESCRIPTION

Figure 1 illustrates the circuit diagram for the output interface. Address selection is performed via the CD4002 NOR gate. When the JOLT address bus contains address 9XXX, the NOR enables CD4011 NAND gate. When the JOLT *WRITE line goes high during the second JOLT clock phase, the inverted NAND gate output fires the latch CD4508. The latch captures JOLT data bus outputs at the instant it is enabled. In the breadboard unit, only the six high-order bits are transferred; the low order two bits are available with minor modifications.

Digital output can be drawn off at the latch outputs, with buffering considered desirable to avoid loading down the latch outputs. A resistor network provides the high-impedance analog output, suitable for driving a high-Z meter or a 0-100 microamp movement through a series resistor for scaling.

III. PROGRAMMING NOTES

This interface latches output data onto the analog and digital output lines automatically when address 9XXX is referenced by the JOLT in a Store Accumulator operation. Since the address seen by the interface comes directly from the address bus and is the JOLT effective address after address computation, the interface will react to all appropriate addressing modes (indexed, indirect, etc.). The store operation itself performs the output operation. The output data remains static (at the last accumulator value stored at 9XXX) until another store operation to 9XXX is performed by the JOLT.

In practice, a Rustrak(TM) 0-100 microamp chart recorder has been used successfully with the unit, using the series 100K potentiometer as a scaling device.

*

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Using an oscilloscope at the analog output terminal (the common tiepoint of the D/A resistors), the following JOLT program can be used to test the interface. Output should be a sawtooth wave as the analog output is driven in a ramp through its 64 stages as the memory location 0050 is incremented from zero to 255 and wraps around on overflow. Each output state is held for four counts at 0050 since only the high-order six bits are converted to analog in this interface design.

| <u>Program Counter</u> | <u>Op Code</u> | <u>Remark</u> |
|------------------------|----------------|-----------------------|
| 0000 | AD 50 00 | Get 0050 |
| 0003 | 8D 90 00 | Store in output latch |
| 0006 | EE 50 00 | Increment 0050 |
| 0009 | 4C 00 00 | Loop |

IV. REFERENCES

- [1] Lilley, Robert W. and Richard J. Salter, Jr., "Simulation Analysis of a Microcomputer-Based, Low-Cost Omega Navigation System", NASA TM No. 26, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, May, 1976.
- [2] Lilley, Robert W. and Richard J. Salter, Jr., "A Microcomputer-Based Low-Cost Omega Navigation System", NASA TM No. 34, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, August, 1976.