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NTRAN USER'S MANUAL

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16. ABSTRACT

Presented herein is the User's Manual for NTRAN (Network TRANslator), a program written in FORTRAN that provides a means for generating input files for the LOGSIM and LASAR programs from PRF and PR2D input decks. The program technical description, input instructions, and deck setup instructions for the Sigma 5 computer, are presented to familiarize the reader with the software.

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1. INTRODUCTION

NTRAN was developed to provide the users of the MSFC Banning Design Automation System a means for generating input for the LOGSIM and LASAR programs that is representative of the logic circuitry included in a layout produced by the PRF or PR2D programs. NTRAN utilizes a PRF or PR2D input deck and a "library" file to produce output formatted as input for either of the target programs (LOGSIM or LASAR). The library file consists of a model in terms of the target program for each of the standard patterns utilized in the design. The library file is in card image format and is easily prepared and maintained utilizing standard system software.

NTRAN was designed to maintain, to the extent possible, the original identity of the information as it is transformed into the required form. This goal was realized by adopting a "cell-pin" convention for the signal names in the network. The "cell" portion of the name indicates the PRF (or PR2D) cell number that the signal is associated with and the "pin" identifies the pin name within the pattern type that the signal is associated with. The definition of a pin is extended to include all logic nodes of the pattern type whether the node is a true pin or not. A convention is employed that allows the user to readily ascertain the nature of the pin by using numeric names for true pins and non-numeric names for nodes that are internal to the pattern. For example, signal 100-AA is recognized as an internal node of PRF cell number 100. The "cell-pin" signal name convention is maintained throughout all phases of the process for LOGSIM translations, but must be abandoned for the final output of LASAR translations.

Since neither LOGSIM nor LASAR is programmed to handle the unique properties of transmission gate logic, NTRAN generates a reasonable approximation of a transmission gate network with a ROM for LOGSIM and a sum of products network for LASAR. A transmission gate network consisting of as many as 15 transmission gates can be handled by the program (see Section 2.2).

Under certain conditions, it is possible that NTRAN will generate incorrect data for the design that is being translated. An example of this is the situation in which bonding pads for chip inputs and outputs use the same standard pattern number. If the pad is in a net that contains both input and output pins from other cells it is uncertain whether the pad is a chip input or chip output. A similar situation exists with respect to transmission gate networks, i.e., the function (input or output) of a pin is not always determinable from the network topology. The solution to this problem is to provide a means for the user to interact with NTRAN at specific stages in the process. It is accomplished by writing an output file in card image format at the end of each major step in the process, and by designing NTRAN to restart execution at any one of these major steps. The user can, therefore, modify the intermediate output files in such a manner as to cause NTRAN to arrive at a solution that is most representative of the design being processed.

The final output of NTRAN is a file that will require a slight amount of modification before being used as input to the LOGSIM or LASAR programs. These modifications consist of inserting program control options, input generator patterns, etc., the type of information that NTRAN is unable to inject. Also, for LASAR the output file must be split into two separate segments (model cards and illegal cards) for input to separate load modules of the LASAR system.

2. NTRAN TECHNICAL DESCRIPTION

As previously stated, NTRAN operates with two input files (PRF deck and library) to produce an input file for either LOGSIM or LASAR. The process consists of two distinct phases for LOGSIM and three distinct phases for LASAR. The first and second phases consist of the initial translation and of the transmission gate analysis, respectively, for both LOGSIM and LASAR. A third phase is required for LASAR in which the net names are assigned numerical values and pre-ordered to force LASAR to arrive at identical "user" and "LASAR" node numbers. At the end of each phase in the program an output file is written that reflects the current state of the translation process. Interim output files are used to support a restart feature in which the user modifies the partially completed translation to cause NTRAN to arrive at a final result that is most representative of the circuit design being processed.

2.1 Phase 1 - Initial Translation

The first step in the initial translation process consists of reading the input deck and searching the library for the required pattern numbers. NTRAN will automatically determine if a PRF or PR2D deck is being used. As each pattern is found, entries are made in NTRAN internal storage reflecting the cell number and the pattern pin number to which the entry belongs. For example, if cell number 100 is an inverter with output taken from pin 2 and input applied at pin 3, an inverter (1 input NAND) will be entered whose output name is 100-2 with an input named 100-3. Once all cells are entered, the PRF netlist is examined to determine the chip inputs and outputs and to interconnect the elements in the network.

NTRAN is programmed to deal with several categories of bonding pads. Dual purpose pads (used for both input and output) and single purpose pads, both modeled and not modeled are acceptable. Bonding pads that perform a logical function (usually inversion for buffering) are required to be modeled and entered in the pattern library while non-buffered bonding pads are not included in the library. Both types must have a pattern number that is greater than or equal to 9000. Provision is made for the user to indicate if a pad is to be used only as input or only as output in the library. Absence of such an indication implies that the pad can function either way. In summary, the following types of pads may be accommodated:

- Non-modeled dual purpose,
- Modeled dual purpose,
- Non-modeled single purpose, and/or
- Modeled single purpose.

NTRAN will invariably determine the function of the last three types of pads correctly but may have difficulty with the first type. NTRAN assumes that a dual purpose pad is an output pad if the pad is connected to a pattern output pin. The circuit configuration shown in Figure 2-1 demonstrates a situation in which NTRAN may improperly identify a pad. If the pad were intended to be wire-or'd with the inverter, NTRAN would mistakenly identify the pad as an output.

Figure 2-1 illustrates the desirability of the restart feature. The user can modify the output file of phase 1 such that the function of the pad is properly identified and re-execute the remainder of NTRAN.

Since some standard pattern designs use internally bussed clock lines (e.g., Banning PMOS), a means for indicating their presence in the pattern models has been provided. This is accomplished by reserving pin names of the form "Cn" to indicate clocks. As a final step in the determination of chip inputs and outputs, NTRAN will scan the network for pins so named and assign each unique one found as a chip input.

The final step in the initial translation process is that in which the elements are interconnected in accordance with the PRF (or PR2D) netlist. As previously stated, the network entries are initially generated with output names and input names reflecting the cell number and the pattern pin number to which the entry belongs. The connecting process will scan the PRF netlist, determine the cell-pin that is the output pin in the net, and change all other cell-pin names in the net to the output cell-pin so found. All element input names will, therefore, bear the cell-pin identity of the element that drives the input. If multiple outputs are found in the net a wired-or is automatically generated to tie the outputs together, and all inputs in the net are connected to the output of the wired-or. Provision has been made to account for pattern edge inputs and outputs found in shift register strings. This is accomplished by reserving pin names of the form "On" and "In" (O for outputs, I for inputs) to indicate cell edge outputs and inputs in the pattern. NTRAN interconnects such entries by scanning the network for "On" pin names and when so found, examining the adjacent cell for a matching "In" pin name. As matches are found NTRAN replaces the "In" name with the "On" name. If a match cannot be made, a warning message is issued.

Completion of the interconnect process marks the end of phase 1 of NTRAN. The current state of the translation is formatted for the appropriate target processor, output to logical unit 10, and listed on the printer. NTRAN may be re-started following this point using the output of unit 10 modified to the user's liking.

2.2 Phase 2 - Transmission Gate Analysis

Phase 2 involves the process whereby the behavior of transmission gate networks are determined. NTRAN first searches the network for a group of interconnected transmission gates. The gates may be interconnected in any

DUAL PURPOSE PAD PARADOX

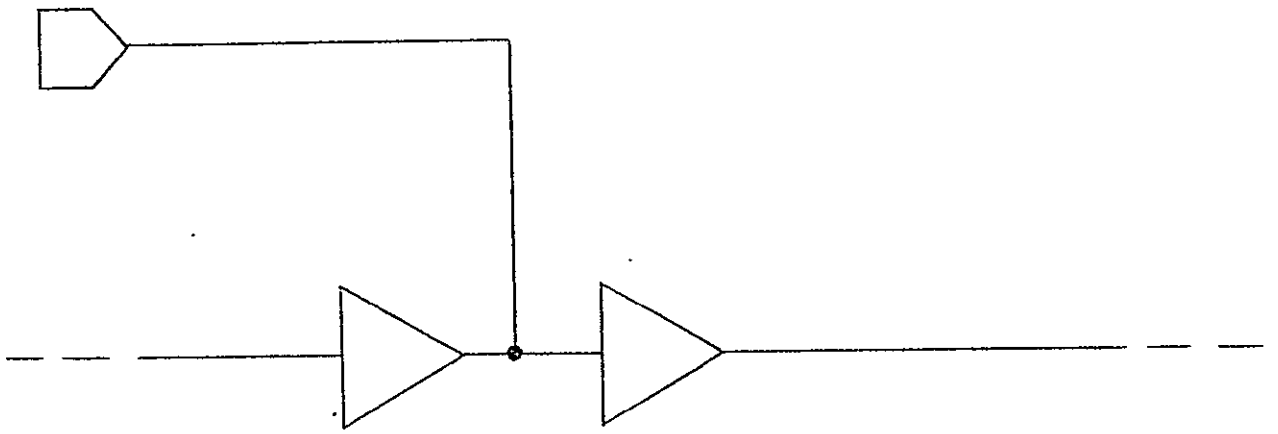


Figure 2-1

manner, so long as all clock (gating) terminals are driven by a buffered logic element (i.e., one that is not a transmission gate). Once a group is found, NTRAN attempts to find the "input" and "output" terminals of the transmission gate network. This process, like the identification of the chip inputs and outputs, gives improper results under certain conditions. Since the input and output pins of a transmission gate are interchangeable, the determination of a pin function rests solely on the nature of the other pins in the net. That is, if a transmission gate is in a net that contains only input pins, it is safe to assume that the transmission gate pin is acting as an output. Also, if the transmission gate pin is in a net containing only output pins it is likely acting as an input. If, however, the transmission gate is in a net containing both input and output pins, it is uncertain whether the pin is to be used as an output or an input. NTRAN assumes that the pin is to be used as the transmission gate input. Again, the restart feature may be utilized to force the transmission gate pins into the proper roles by modifying the interim output file.

Once the transmission gate network input and output terminals are identified, NTRAN builds a truth table for each output terminal in the network based on the interconnect structure. For LOGSIM translations a set of technology design rules also influence the truth table values. These rules specify the output of a transmission gate when disconnected (holding or indeterminate) and the result of two or more transmission gates driving the same node with conflicting signals (indeterminate, logic 1, logic 0). Note that the inherent feedback mechanism of transmission gates is not accounted for by NTRAN. If the user specifies that two or more transmission gates may drive the same node simultaneously with conflicting signals, NTRAN does not account for the fact that the input terminal of one or more transmission gates may be pulled up or down as the result of such a condition. Due to the complex NAND gate networks that would result in attempting to simulate the hold state for LASAR translations, NTRAN ignores the design rules input by the user and forces disconnected transmission gates to output indeterminates. Also, to further simplify the LASAR networks, transmission gates are not allowed to drive the same node simultaneously.

Once the truth table is built, NTRAN constructs a ROM if the target processor is LOGSIM and a sum of products network if the target processor is LASAR. The inputs to the ROM consist of the input terminals of the transmission gate network and of the clock terminals of all the transmission gates in the network. For the sum of products network, each product term consists of the clock terminals of those gates that produce a valid connecting path between an input terminal and the output, and of the input terminal itself. A product term is generated for each valid clock combination for the transmission gate network. The sum of products is simulated by using NAND gates for the product terms and for the summing operation. Input combinations for which the output is indeterminate are reflected to the LASAR program by generating illegal specifications for the network. The illegals are generated first from the clock combinations that do not provide a path from input to output, and then by those clock combinations that cause any two or more input terminals to be interconnected.

Completion of the transmission gate analysis marks the end of phase 2 of NTRAN, and for LOGSIM translations the end of the process. The current state of the translation is formatted for the appropriate target processor, written on logical unit 11 and listed on the printer. For LASAR translations, NTRAN may be restarted following Phase 2 using as input the data written on logical unit 11 with the appropriate modifications.

2.3 Phase 3 - Minimum Feedback Ordering

Since the LASAR program cannot utilize the cell-pin signal names output by NTRAN at the end of the first and second phases, a third phase is required to replace them with purely numeric names. The assignment of node numbers to cell-pin names could be done in an arbitrary manner, but would give the user two cross-reference tables to deal with. These would be the NTRAN cell-pin name-to-user node number cross reference table, and the user node number-to-LASAR node number cross reference table. Since these two tables would make it difficult for the user to relate the LASAR node numbers to the original PRF elements, NTRAN assigns the node numbers based on minimum feedback order just as LASAR does. Therefore, when LASAR performs the minimum feedback ordering, the node numbers will be unchanged so long as element expansion into NAND gates is not required. Element expansion is avoided by restricting the library model elements to NAND gates and transmission gates. NTRAN will replace the transmission gates with NAND equivalents thereby presenting a pure NAND network to the minimum feedback ordering process. The net result, of course, will be a single table consisting of the NTRAN cell-pin names-to-LASAR node numbers cross reference.

Completion of the minimum feedback ordering process marks the end of LASAR translations. The final output is recorded on logical unit 12 and listed on the line printer.

(BLANK)

3. OPERATING INSTRUCTIONS

To use NTRAN, a library file must be prepared that consists of network models for the standard cells involved in the translation. Once prepared the library may be used repeatedly, requiring modification only when additional standard cells are to be used. A different library must be prepared for each of LOGSIM and LASAR, and for each of the applicable process technologies. For example, if translations are to be made to LASAR and LOGSIM for CMOS and PMOS technologies, four libraries will be ultimately required. Only one library, however, is required for any one run of NTRAN.

3.1 Preparation of Library File

In general, preparation of the library consists of modeling each of the standard LSI cells in terms of the target processor. For the LOGSIM library the user may utilize DTMR, DTMF, DCTM, NEWGATE, ROM, and NET cards to characterize his model. Any LOGSIM logic element type may be used in the model, along with the user-defined transmission gate element. As mentioned previously, for the sake of maintaining visibility of the design being translated, the LASAR library element types are restricted to NAND's and transmission gates.

3.1.1 Modeling Rules

- Model card images are to be prepared precisely in the format of the target processor.
- Model card images for each pattern must be consecutive in the library file.
- The transmission gate clock terminal must be the second input terminal.
- Wired-or's internal to the pattern must be resolved by the user (except for transmission gates).
- "Illegal" cards are allowed as part of a LASAR model and must immediately follow the model cards for the pattern to which they apply.
- "MODEL/" must appear in the first six columns of the first card for each pattern and not on any of the other cards for the pattern in a LASAR library.
- Logic elements are restricted to NAND's and transmission gates in a LASAR library.
- Dual outputs may not be used in LASAR models.

- Model signal names are limited to 2 characters.
- Numeric signal names indicate that the signal is connected to a pin.
- Non-numeric names identify signals that are not connected to a pin and are interpreted as follows:

  L0 - signal is logic zero

  L1 - signal is logic one

  Cn - signal is internally bussed clock no. n

  On - signal is cell edge output no. n

  In - signal is cell edge input no. n

  All other names have no particular significance and are to be used to interconnect logic elements within the pattern.

3.1.2 Card Formats

Presented in Table 3-1 is the format for the card images that make up the model library. The first two cards are invariably required while the remainder are required only to the extent demanded by the design being processed. All "I" format entries must be right-justified in the field while "A" format entries must be left-justified.

3.1.3 Sample Libraries

Presented in Figures 3-1, 3-2, and 3-3 are sample libraries for CMOS-LOGSIM, CMOS-LASAR, and PMOS-LOGSIM, respectively. These three libraries were constructed to be used for NTRAN checkout purposes and as such do not include all of the standard cells for either technology. Also, the delay and decay times illustrated do not reflect the actual response times associated with the cells. The network topology, however, is believed to be accurate.

3.2 Description of Output

As previously stated, NTRAN creates an output file at the end of each of the defined major phases of the process, and also lists that file on the printer. Additional printer output is produced during each phase of the process to inform the user of the actions of NTRAN.

MODEL LIBRARY CARD FORMAT

CARD NUMBER	COLS.	FORMAT	DESCRIPTION
1	1-8	A8	"LOGSIM" or "LASAR" (Identifies Target Processor)
	9-12	A4	Process Technology (CMOS, PMOS, Etc.)
	13-14	I2	Number of Pattern Types That Are To Be Excluded From Translation (Protective Diodes, Killer Gates, Etc.)
	15-26	3I4	Pad Pattern Numbers That Are To Be Used Only as Outputs
	27-38	3I4	Pad Pattern Numbers That Are To Be Used Only as Inputs
	39-42	A4	Name That is Being Used to Indicate Transmission Gates in This Library File
	43	I1	= Zero; Transmission Gate Activation Level is Logic Zero
			= Non-Zero; Logic One
	44	I1	= Zero; Transmission Gate Output is Indeterminate When Disconnected
			= Non-Zero; Output "HOLDS"
	45	I1	= Zero; Output is Indeterminate For Two or More Transmission Gates Driving Same Node Simultaneously
			= Non-Zero; Output is Determinate

Table 3-1

MODEL LIBRARY CARD FORMAT
(Continued)

CARD NUMBER	COLS.	FORMAT	DESCRIPTION
1	46	I1	(Used Only If Card Column 45 is Non-Zero) = Zero; Output is Logic Zero For Two or More Transmission Gates Driving Same Node With Conflicting Signals = Non-Zero; Output is Logic One
2	1-80	20I4	Pattern Numbers of The Cell Types That Are to be Excluded (Blank Required if There Are None)
3-N	1-72	*	Model Cards as Required to Describe Each Pattern in Library
	77-80	I4	Pattern to Which the Model Card Belongs

* See LOGSIM and LASAR User Manuals.

Table 3-1
(Continued)

```
CARD    0000000001111111111122222222233333333334444444444555555555566666666667777777778
COLUMN: 1234567890123456789012345678901234567890123456789012345678901234567890123456789
        LOGSIM  CM0501903090010    9020        TGTE                                    1110
        1210                                                                          1110
        DTMR    1,10                                                                  1110
        DTMF    1,5                                                                   1120
        NET     2          NAND * 1,1          3                                      1120
        DTMR    1,10                                                                  1120
        DTMF    1,10                                                                  1120
        NET     2          NOR  * 1,1          3,4                                    1220
        DTMR    1,15                                                                  1220
        DTMF    1,10                                                                  1220
        NET     2          NAND * 1,1          3,4                                    1230
        DTMR    1,33                                                                  1230
        DTMF    1,19                                                                  1230
        NET     2          NAND * 1,1          3,4,5                                  1240
        DTMR    1,25                                                                  1240
        DTMF    1,37                                                                  1240
        NET     2          NAND * 1,1          3,4,5,6                                1290
        DTMR    1,10                                                                  1290
        DTMF    1,10                                                                  1290
        DTMF    1,10                                                                  1290
        NET     6          NAND *              7                                      1290
        NET     7          NAND * 1,1,1        AA,BB                                  1290
        NET     BB         NAND *              4,7                                    1290
        NET     AA         NAND *              3,5                                    1310
        DTMR    1,25                                                                  1310
        DTMF    1,19                                                                  1310
        NET     2          NAND * 1,1          3                                      1320
        DTMR    1,10                                                                  1320
        DTMF    1,10                                                                  1320
        NET     4          TGTE * 1,1          2,3                                    1430
        DTMR    1,20                                                                  1430
        DTMF    1,20                                                                  1430
        DCTM    1,100                                                                 1430
```

Figure 3-1

```
CARD       00000000011111111112222222222333333333344444444445555555555666666666677777777778
COLUMN.    12345678901234567890123456789012345678901234567890123456789012345678901234567890
-------------------------------------------------------------------------------------------
          ROM     1   41430******01**0101HH                                            1430
          NET     6           1430 * 1,1,1        3,4,7,AA                             1430
          NET     9           TGTE *              8,10                                 1430
          NET     AA          TGTE *              2,3                                  1430
          NET     AA          TGTE *              5,4                                  1430
          NET     AA          TGTE *              6,7                                  1430
          DTMR    1,44                                                                 1620
          DTMF    1,54                                                                 1620
          NET     2           AND  * 1,1          3,4                                  1620
          DTMR    1,31                                                                 1640
          DTMF    1,31                                                                 1640
          NET     2           AND  * 1,1          3,4,5,6                              1640
          DTMR    1,44                                                                 1870
          DTMF    1,54                                                                 1870
          NET     6           NØR  * 1,1          AB,CD                                1870
          NET     AB          AND  * 1,1          2,3                                  1870
          NET     CD          AND  * 1,1          4,5                                  1870
          DTMR    1,33                                                                 1890
          DTMF    1,37                                                                 1890
          NET     6           NØR  * 1,1          AB,CD,EF                             1890
          NET     AB          AND  * 1,1          2,3                                  1890
          NET     CD          AND  * 1,1          4,5                                  1890
          NET     EF          AND  * 1,1          6,7                                  1890
          DTMR    1,31                                                                 2310
          DTMF    1,37                                                                 2310
          NET     2           EXØR * 1,1          3,4                                  2310
```

Figure 3-1
(continued)

SAMPLE CMOS-LASAR LIBRARY

```
CARD     0000000001111111111222222222333333333344444444445555555555666666666677777777778
COLUMN   1234567890123456789012345678901234567890123456789012345678901234567890123456789
-------------------------------------------------------------------------------------------
         LASAR   CMOS01930909010     9020        TGTE
         1210                                                                          1110
         MODEL/1,A/3/2/                                                                1120
         MODEL/1,A/A,B/2/2NA/A,B/AB/1NA/3/A/1NA/4/B/                                   1220
         MODEL/2,A/3,4/2/                                                              1230
         MODEL/3,A/3,4,5/2/                                                            1240
         MODEL/4,A/3,4,5,6/2/                                                          1290
         MODEL/1,A/7A5/2,A/AA,BB/7/2NA/3,5/AA/2NA/4,7/BB/                              1310
         MODEL/1,A/3/2/                                                                1320
         MODEL/TGTE/B,3/4/                                                             1430
         MODEL/TGTE/2,3/AA/TGTE/5,4/AA/TGTE/6,7/AA/2NA/AA,8/BB/2NA/BB,L1/8/            1430
               TGTE/A,10/9/                                                            1620
         MODEL/2,A/3,4/AA/1NA/AA/2/                                                    1640
         MODEL/4,A/3,4,5,6/AA/1NA/AA/2/                                                1870
         MODEL/2,A/2,3/AA/2NA/4,5/BB/2NA/AA,BB/CC/1NA/CC/6/                            1890
         MODEL/2,A/2,3/AA/2NA/4,5/BB/2NA/6,7/CC/3NA/AA,BB,CC/8/                        2240
         MODEL/2,A/2,3/AA/1NA/4/AB/2NA/AA,AB/AC/1NA/AC/AD/2NA/AD,C2/AE/1NA/C2/AF/      2240
               3NA/AC,AF,5/AG/2NA/AE,AG/5/                                             2310
         MODEL/1,A/3/AA/1NA/4/BB/2,A/AA,4/CC/2NA/BB,3/DD/2NA/CC,DD/2/
```


Figure 3-2

```
CARD.  . . 0000000001111111111222222222333333333344444444445555555555566666666667777777778
COLUMNS    1234567890123456789012345678901234567890123456789012345678901234567890123456789
           LOGSIM  PMOSF1                          TGTE1
           5020                                                                          2240
           DTMR    1,10                                                                  2240
           DTMF    1,20                                                                  2240
           LCTM    1,100                                                                 2240
           NET     AA      AND  *                  2,3                                   2240
           NET     AB      NOR  *                  AA,4                                  2240
           NET     AC      AND  *                  AB,C2                                 2240
           NET     AD      NAND *                  C2                                    2240
           NET     AE      MCLK *  1,1,1           5,C2                                  2240
           NET     AF      AND  *                  AB,AD,AF                              2240
           NET     5       OR   *                  AC,AF                                 2240
           DTMR    1,10                                                                  4020
           DTMF    1,13                                                                  4020
           NET     3       NAND *                  A1,A2                                 4020
           NET     A1      NAND *                  3,A3,A4                               4020
           NET     A2      NAND *                  A4,C2                                 4020
           NET     A3      NAND *                  C2                                    4020
           NET     A4      NAND *                  2                                     4020
           DTMR    1,10                                                                  4360
           DTMF    1,10                                                                  4360
           SUB     1  34360H0H1H1H1H900H100                                              4360
           NET     4       4360 * 1,1              4,3,2,C2                              4360
           DTMR    1,10                                                                  4380
           DTMF    1,10                                                                  4380
           NET     4       MCLK *  1,1             BB,C2                                 4380
           NET     BB      NAND * 1,1              3                                     4380
           NET     3       MCLK *  1,1             AA,C1                                 4380
           NET     AA      NAND * 1,1              2                                     4380
           DTMR    1,5                                                                   6020
           DTMF    1,15                                                                  6020
           LCTM    1,150                                                                 6020
           NET     3       MCLK * 1,1,1            2,C2                                  6020
```

Figure 3-3

SAMPLE PMOS-LOGSIM LIBRARY
(continued)

```
CARD-  --0000000011111111112222222223333333333444444444555555555566666666677777777778
COLUMNS 12345678901234567890123456789012345678901234567890123456789012345678901234567890
          DTMR    1,17                                                              6200
          DTMF    1,7                                                               6200
          DCTM    1,113                                                             6200
          NET     01      MCLK  * 1,1,1       CC,C2                                 6200
          NET     CC      NAND  * 1,1         BB                                    6200
          NET     BB      MCLK  * 1,1,1       AA,C1                                 6200
          NET     AA      NAND  * 1,1         2                                     6200
          DTMR    1,17                                                              6220
          DTMF    1,7                                                               6220
          DCTM    1,113                                                             6220
          NET     01      MCLK  * 1,1,1       CC,C2                                 6220
          NET     CC      NAND  * 1,1         BB                                    6220
          NET     BB      MCLK  * 1,1,1       AA,C1                                 6220
          NET     AA      NAND  * 1,1         I1                                    6220
          DTMF    1,17                                                              6240
          DTMF    1,7                                                               6240
          DCTM    1,113                                                             6240
          NET     3       MCLK  * 1,1,1       CC,C2                                 6240
          NET     CC      NAND  * 1,1         BB                                    6240
          NET     BB      MCLK  * 1,1,1       AA,C1                                 6240
          NET     AA      NAND  * 1,1         I1                                    6240
          DTMR    1,5                                                               6280
          DTMF    1,7                                                               6280
          DCTM    1,127                                                             6280
          NET     4       TGTE  * 1,1,1       2,3                                   6280
          DTMR    1,47                                                              6060
          DTMF    1,77                                                              6060
          NET     3       NAND  * 1,1         2                                     6060
```

Figure 3-3
(continued)

3.2.1 Phase 1 - Initial Translation

The first output printed by Phase 1 is a program header page that identifies the run parameters. These parameters consist primarily of the information supplied on the first two cards of the library file by the user. The PRF (or PR2D) input deck is also echoed on the printer to provide the user a convenient means with which to cross check the results of the translation.

If tied together outputs (transmission gates excepted) are detected in the network, NTRAN automatically generates an AND gate and inserts it into the network to combine the outputs. For LOGSIM translations the gate output is named "WOR-n" where n is sequenced beginning with 1 for each wired-or generated. Since LASAR is restricted to use only NAND gates, two are required to implement the AND function. The first will be named "WOR-n" as above and the second will be named "INV-n" with n being the same number. For each of LOGSIM and LASAR translations, a message is output identifying the elements constituting wired-or and the network elements added to simulate it.

Additional output may be produced by NTRAN during Phase 1 processing and is generally self-explanatory.

3.2.2 Phase 2 - Transmission Gate Analysis

As discussed previously NTRAN generates a ROM or a sum of products network to simulate the behavior of transmission gates that are present in the design. In either case, a truth table is first constructed from which the equivalents are derived. NTRAN prints the truth table in the normal engineering format as each truth table is constructed, identifying the constituent transmission gates, the output terminal, the input terminals, and the clock terminals. This printout provides the engineer with a representation of the transmission gate network behavior that is more easily interpreted than the LOGSIM ROM cards and the LASAR model cards that are eventually inserted to simulate the truth table.

Following the printout of the truth table, NTRAN lists the elements that were added to simulate the transmission gate network. The ROM cards and the accompanying net card are output for LOGSIM translations in which the ROM's are named "ROM-n" with n sequenced beginning with 1 as each ROM is generated.

For LASAR translations, significantly greater additions to the network description are required than are for LOGSIM translations. A product gate is generated for each legal combination of clock inputs; a summing gate is generated to tie the product gates together; and illegal specification cards are generated to prevent erroneous stimulus generation by LASAR. Also, if the transmission gate activation level is logic zero, an inverter gate is required for each clock input. The summing NAND gate will retain the original signal name of the transmission gate network output terminal as its output signal name. Product gate output signal names will be coded "PRn-m" where n is sequenced beginning with 1 for each sum of products network and m is a sequence number identifying a product

gate within the sum of products. For example, "PR02-03" is the third product gate in the second sum of products network. If clock inverters are required, their output signal names are coded "*CLKNAM" where CLKNAM is the original clock input name.

3.2.3 Phase 3 - Minimum Feedback Ordering

The only printed output produced during Phase 3 in addition to output file listing is the signal name to LASAR node number cross reference table. This table should be retained to correlate the node numbers in LASAR output with the original PRF elements.

Note that in the final output file, NTRAN will have assigned sequence numbers to the NAND gates that match their output signal node numbers. This operation should further reduce the difficulty of relating LASAR output to the original PRF data.

3.2.4 Error Messages

Throughout the execution of NTRAN, situations may arise in which the data being processed appears to be in error, or a situation may materialize for which NTRAN cannot continue. For the former condition, a self-explanatory warning message is printed, and for the latter, the program is aborted with an attendant message of the form "PROGRAM CONTINGENCY ERROR IN XXXXX-Y." The "XXXXX" corresponds to the NTRAN subroutine name and the "Y" to a checkpoint within the subroutine at which the error occurred. Table 3-2 displays all of the possible abort error codes, their probable cause, and the possible remedy.

3.3 Deck Setup Instructions

Presented in Sections 3.3.1 through 3.3.5 are the deck setups for the Xerox Sigma 5 computer required to execute NTRAN in each of the five possible modes. Deck setups are illustrated with which to run a LOGSIM translation, restart a LOGSIM translation, run a LASAR translation, and restart a LASAR translation in each of two modes. A Type 1 LASAR restart allows the user to re-execute the transmission gate analysis and minimum feedback ordering sections with a modified output file from Phase 1. A Type 2 LASAR restart allows the user to re-execute the minimum feedback ordering section with a modified output file from Phase 2. Note that each of the deck setups are practically identical and require little change to switch from one setup to the other.

For the user who is unfamiliar with the Sigma 5, the files required to run NTRAN are described in Table 3-3 in a general manner.

NTRAN ABORT ERROR CODES.

CODE	PROBABLE CAUSE	POSSIBLE REMEDY
CHIPIO-1	Too Many Chip Inputs (Max. = 50)	Enlarge "CHIPS" Array and Recompile Program
CHIPIO-2	Too Many Chip Outputs (Max. = 50)	Enlarge "CHOPS" Array and Recompile Program
CODILL-1	Signal Name on Model Illegal Card Not in Model	Check Model Library File for Inconsistencies
FINDIO-1	No Output Terminal Found in Transmission Gate Network	Check PRF Netlist for Errors
FINDIO-2	No Input Terminal Found in Transmission Gate Network	Check PRF Netlist for Errors
FINDIO-3	Too Many Transmission Gates and Input Terminals in Transmission Gate Group (NTGS+NINS>16)	Partition Transmission Gate Network if Possible and Rerun
GROUP-1	Transmission Gate Clock Terminal is Being Driven by Another Transmission Gate	Modify PRF Netlist
INSERT-1	Too Many Logical Elements in Design (Max = 3000)	Enlarge "NET" Arrays and Recompile Program
LASGEN-1	Pattern Number in PRF Deck is Not in Model Library File	Add Required Pattern to Model Library File
LASTGA-1	Not Enough Room in "NET" Array to Build Sum of Products Network	Enlarge "NET" Array and Recompile Program
LASIN-1	No Network Elements Found on LASAR Restart File	Ascertain Validity of Restart File

Table 3-2

NTRAN ABORT ERROR CODES (Continued)

CODE	PROBABLE CAUSE	POSSIBLE REMEDY
LASIN-2	No "INPUT/" Cards Found on LASAR Restart File	Ascertain Validity of Restart File
LASIN-3	No "OUTPUT/" Cards Found on LASAR Restart File	Ascertain Validity of Restart File
LOGIN-1	No Network Elements Found on LOGSIM Restart File	Ascertain Validity of Restart File
LOGIN-2	No "GEN" Cards Found on LOGSIM Restart File	Ascertain Validity of Restart File
LOGIN-3	No "PNT" Cards Found on LOGSIM Restart File	Ascertain Validity of Restart File
LOGGEN-1	Pattern Number in PRF Deck Not in Model Library File	Add Required Pattern to Library File
MAIN-1	Model Library File Has Neither LOGSIM nor LASAR in First Record	Ascertain Validity of Model Library File
ORDER-1	Illegal Card Signal Name Not in Network Array	Call Programmer
ORDER-2	Too Many Network Elements for LASAR to Handle (Maximum = 999)	Partition Design and Run in Two or More Parts
PRNET-1	Pattern Model Too Large to Fit in Staging Buffer	Enlarge Array "STGBFR" and Recompile Program
PUSH-1	"STACK" Array Too Small	Enlarge "STACK" Array and Recompile Program
RDPR2D-1	PR2D Netlist Too Large For PRFNET" Array	Enlarge "PRFNET" Array and Recompile Program
RDPR2D-2	Indicated Netlist Continuation Card Missing	Correct PR2D Input Deck

Table 3-2
(Continued)

NTRAN ABORT ERROR CODES (Continued)

CODE	PROBABLE CAUSE	POSSIBLE REMEDY
RDPRF-1	PRF Netlist too Large for "PRFNET" Array	Enlarge "PRFNET" Array and Recompile Program
RDPRF-2	Indicated Netlist Continuation Card Missing	Correct PRF Input Deck
RFFAN-1	Excessive Signal Name Length	Check Model Library for Syntax Errors
STAGE-1	Illegal Card Type in LOGSIM Model Library File	Make Sure That Library File Has Only DTMR, DTMF, DCTM, NEWGATE, ROM and NET Cards
STGLSR-1	"MODEL/" Missing on First Pattern Model Card in LASAR File	Assure That All Patterns Have "MODEL/" In Columns 1-6 on First Model Card
STGLSR-2	Syntax Error in LASAR Model Card	Assure That All Model Cards Obey The LASAR Syntax Rules
STGLSR-3	LASAR Model Too Large for Staging Buffer	Enlarge Array "STGBFR" and Recompile Program
WFFIX-1	Field Width Violation While Writing LOGSIM Output File	Call Programmer

Table 3-2
(Continued)

NTRAN FILE REQUIREMENTS

LOGICAL UNIT NO.	DEVICE TYPE	MODE	FORMAT	CONTENTS
1	DISK, TAPE	INPUT	CARD IMAGES	MODEL LIBRARY
2	DISK, TAPE	SCRATCH		
5	CARD, DISK, TAPE	INPUT	CARD IMAGES	PRF OR PR2D INPUT DECK
6	PRINTER	OUTPUT		NTRAN LIST OUTPUT
10	DISK, TAPE	OUTPUT*	CARD IMAGES	INTERIM OUTPUT FILE FOR BOTH LOGSIM AND LASAR TRANSLATIONS
11	DISK, TAPE	OUTPUT*	CARD IMAGES	1. FINAL OUTPUT FOR LOGSIM TRANSLATIONS 2. INTERIM OUTPUT FOR LASAR TRANSLATIONS
12	DISK, TAPE	OUTPUT*	CARD IMAGES	FINAL OUTPUT FOR LASAR TRANSLATIONS

THESE FILES ARE ALSO USED AS SCRATCH FILES PRIOR TO BEING WRITTEN AS INDICATED.

Table 3-3

3.3.1 Run LOGSIM Translation

```
!JOB
!LIMIT (TIME,5), (CORE,50)
!ASSIGN F:1,(FILE,LOGLIB),(IN)
!ASSIGN F:2,(FILE,TEMP),(OUTIN)
!ASSIGN F:5,(DEVICE,CR),(IN)
!ASSIGN F:6,(DEVICE,LP),(OUT)
!ASSIGN F:10,(FILE,PHASE 1),(OUTIN),(SAVE)
!ASSIGN F:11,(FILE,PHASE 2),(OUTIN),(SAVE)
!RUN (LMN,NTRAN)
!DATA
      o      PRF or PR2D Input Deck
!EOD
!FIN
```

where:

LOGLIB is the LOGSIM library prepared by the user.

PHASE 1 is the output from the first phase of NTRAN.

PHASE 2 is the final output of NTRAN.

TEMP is a scratch file.

3.3.2 Restart LOGSIM Translation

```
!JOB
!LIMIT (TIME,5), (CORE,50)
!ASSIGN F:1,(FILE,LOGLIB),(IN)
!ASSIGN F:2,(FILE,TEMP),(OUTIN)
!ASSIGN F:5,(DEVICE,CR),(IN)
!ASSIGN F:6,(DEVICE,LP),(OUT)
!ASSIGN F:10,(FILE,PHASE 1),(IN)
!ASSIGN F:11,(FILE,PHASE 2),(OUTIN),(SAVE)
!RUN (LMN, NTRAN)
!FIN
```

where:

LOGLIB is the LOGSIM library.

PHASE 1 is a file previously created by NTRAN using Setup 3.3.1 and modified by the user.

PHASE 2 is the final output file.

TEMP is a scratch file.

3.3.3 Run LASAR Translation

```
!JOB
!LIMIT (TIME,5), (CORE,50)
!ASSIGN F:1,(FILE,LASLIB),(IN)
!ASSIGN F:2,(FILE,TEMP),(OUTIN)
!ASSIGN F:5,(DEVICE,CR),(IN)
!ASSIGN F:6,(DEVICE,LP),(OUT)
!ASSIGN F:10,(FILE,PHASE 1),(OUTIN),(SAVE)
!ASSIGN F:11,(FILE,PHASE 2),(OUTIN),(SAVE)
!ASSIGN F:12,(FILE,PHASE 3),(OUTIN),(SAVE)
!RUN (LMN, NTRAN)
!DATA
      o      PRF or PR2D Input Deck
!EOD
!FIN
```

where:

LASLIB is the LASAR library prepared by the user.

PHASE 1 is the output from the first phase of NTRAN.

PHASE 2 is the output from the second phase of NTRAN.

PHASE 3 is the final output of NTRAN.

TEMP is a scratch file.

3.3.4 Restart LASAR Translation - Type 1

```
!JOB
!LIMIT (TIME,5), (CORE,50)
!ASSIGN F:1,(FILE,LASLIB),(IN)
!ASSIGN F:2,(FILE,TEMP),(OUTIN)
!ASSIGN F:5,(DEVICE,CR),(IN)
!ASSIGN F:6,(DEVICE,LP),(OUT)
!ASSIGN F:10,(FILE,PHASE 1),(IN)
!ASSIGN F:11,(FILE,PHASE 2),(OUTIN),(SAVE)
!ASSIGN F:12,(FILE,PHASE 3),(OUTIN),(SAVE)
!RUN (LMN, EDIT)
!FIN
```

where:

LASLIB is the LASAR library.

PHASE 1 is a file previously created by NTRAN on logical unit 10 and modified by the user.

PHASE 2 is the output from the second phase of NTRAN.

PHASE 3 is the final output of NTRAN.

TEMP is a scratch file.

3.3.5 Restart LASAR Translation - Type 2

```
!JOB
!LIMIT (TIME,5), (CORE,50)
!ASSIGN F:1,(FILE,LASLIB),(IN)
!ASSIGN F:2,(FILE,TEMP),(OUTIN)
!ASSIGN F:5,(DEVICE,CR),(IN)
!ASSIGN F:6,(DEVICE,LP),(OUT)
!ASSIGN F:10,(FILE,PHASE 2),(IN)
!ASSIGN F:12,(FILE,PHASE 3),(OUTIN),(SAVE)
!RUN (LMN, NTRAN)
!FIN
```

where:

LASLIB is the LASAR library.

PHASE 2 is a file previously created by NTRAN on logical unit 11 and modified by the user.

PHASE 3 is the final output of NTRAN.

TEMP is a scratch file.

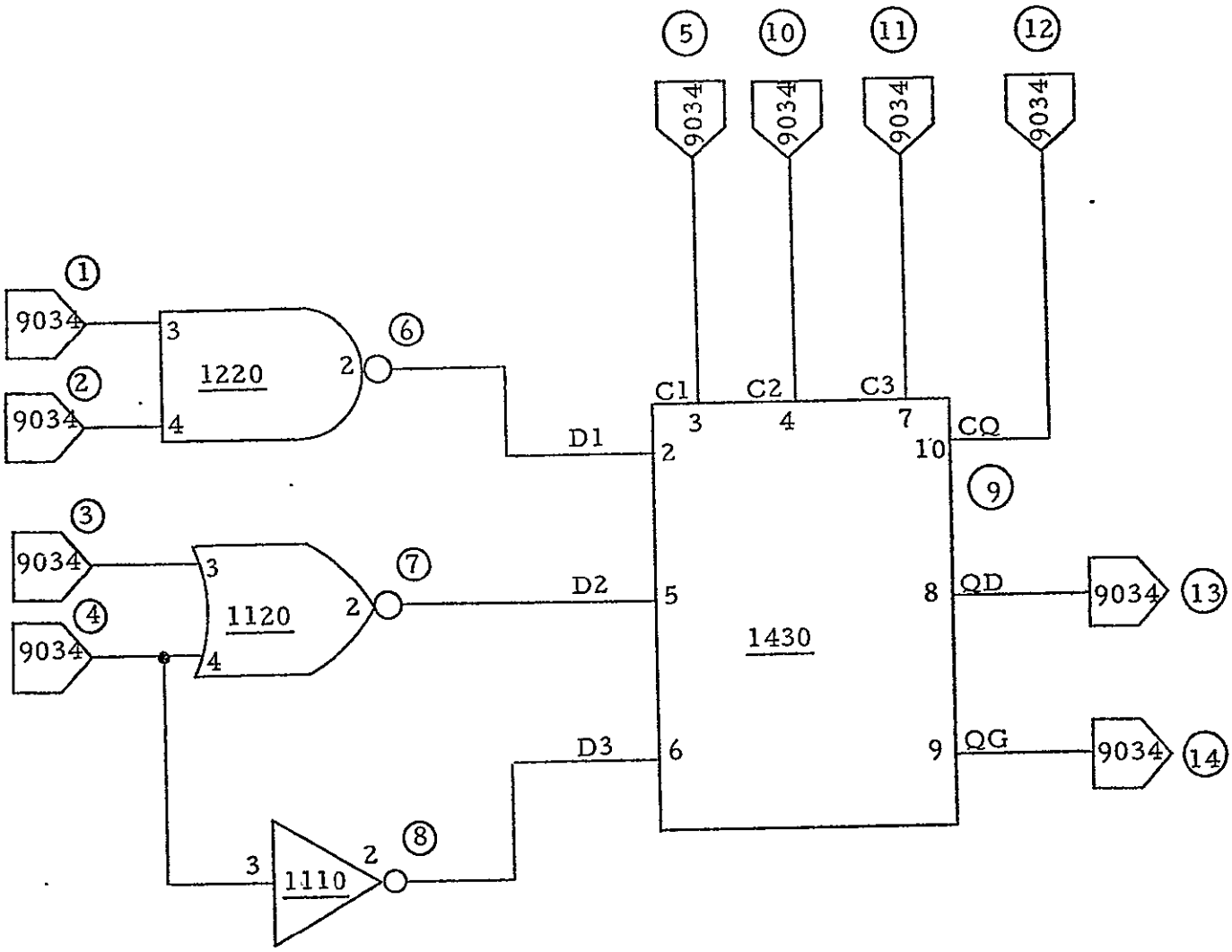
APPENDIX A

SAMPLE PROBLEM

APPENDIX A

This appendix is presented to illustrate the proper use of NTRAN in translating a PRF input deck to its equivalent LOGSIM and LASAR forms. Shown in Figure A-1 is the schematic of the design translated. Pages 30 through 42 show a copy of the computer printout of a run in which a LOGSIM library is created and NTRAN is executed to obtain a translation. Pages 43 through 56 illustrate a similar run in which a LASAR translation is obtained.

DEMONSTRATION SCHEMATIC



n = PRF Cell Numbers

n = Pattern Numbers

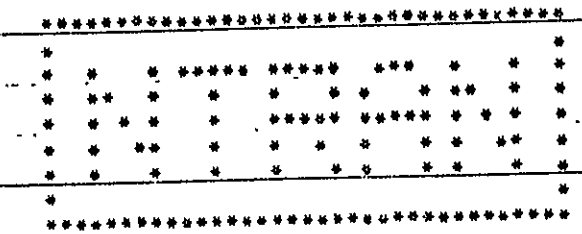
Figure A-1

```
 08135 JUL 28,'75 JD=0127
JAB MS03,EC45001(BAST/CAD),,1
LIMIT (TIME,5),(CARE,50),(ORDER)
PCL
 COPY CR TO LAGLIB
COPY LAGLIB TO LP
LAGSIM  CM8S0190309010    9020        TGTE
1210
DTMR    1,10                                                    1110
DTMF    1,5                                                     1110
NET     2         NAND * 1,1        3                           1110
DTMR    1,10                                                    1120
DTMF    1,10                                                    1120
NET     2         NAND * 1,1        3,4                         1120
DTMR    1,15                                                    1220
DTMF    1,10                                                    1220
NET     2         NAND * 1,1        3,4                         1220
DTMR    1,33                                                    1230
DTMF    1,19                                                    1230
NET     2         NAND * 1,1        3,4,5                       1230
DTMR    1,25                                                    1240
DTMF    1,37                                                    1240
NET     2         NAND * 1,1        3,4,5,6                     1240
DTMR    1,10                                                    1290
DTMF    1,10                                                    1290
NET     6         NAND *            7                           1290
NET     7         NAND * 1,1,1      AA,BB                       1290
NET     BB        NAND *            4,7                         1290
NET     AA        NAND *            3,5                         1290
DTMR    1,20                                                    1310
DTMF    1,19                                                    1310
NET     2         NAND * 1,1        3                           1310
DTMR    1,10                                                    1320
DTMF    1,10                                                    1320
NET     4         TGTE * 1,1        2,3                         1320
DTMR    1,20                                                    1430
DTMF    1,20                                                    1430
DCTM    1,100                                                   1430
ROM     1  +1430*****01**0101HH                                 1430
NET     8         1430 * 1,1,1      3,4,7,AA                    1430
NET     9         TGTE *            8,10                        1430
NET     AA        TGTE *            2,3                         1430
NET     AA        TGTE *            5,4                         1430
NET     AA        TGTE *            6,7                         1430
DTMR    1,44                                                    1620
DTMF    1,54                                                    1620
NET     2         AND  * 1,1        3,4                         1620
DTMR    1,31                                                    1640
DTMF    1,31                                                    1640
NET     2         AND  * 1,1        3,4,5,6                     1640
DTMR    1,44                                                    1870
```

```
DTMF    1,54                                                    1870
NET     8       NAR   * 1,1       AB,CD                       1870
NET     AB      AND   * 1,1       2,3                         1870
NET     CD      AND   * 1,1       4,5                         1870
DTMR    1,33                                                  1890
DTMF    1,37                                                  1890
NET     8       NAR   * 1,1       AB,CD,EF                    1890
NET     AB      AND   * 1,1       2,3                         1890
NET     CD      AND   * 1,1       4,5                         1890
NET     EF      AND   * 1,1       6,7                         1890
DTMR    1,31                                                  2310
DTMF    1,37                                                  2310
NET     2       EXOR  * 1,1       3,4                         2310
```

END
JCL PROCESSING TERMINATED

```
ASSIGN F11,(FILE,LAGLIB),(IN)
ASSIGN F12,(FILE,TEMP),(BUTIN)
ASSIGN F15,(DEVICE,CR),(IN)
ASSIGN F16,(DEVICE,LP),(BUT)
ASSIGN F110,(FILE,PHASE1),(BUTIN),(SAVE)
ASSIGN F111,(FILE,PHASE2),(BUTIN),(SAVE)
RUN (LMN,NTRAN)
```



PROGRAM FUNCTION: NETWORK TRANSLATOR (GENERATES EQUIVALENT LASSIM AND LASAR INPUT FROM PRE AND PRED INPUT DECKS

DEVELOPED BY: MAS COMPUTING INC., HUNTSVILLE ALABAMA

PROGRAM EXECUTION MODE : START

TARGET PROCESSOR : LASSIM

PROCESS TECHNALOGY : CMOS

EXCLUDED PATTERN NUMBERS : 1210

INPUT PAD PATTERN NUMBERS : 9030 9010 0

OUTPUT PAD PATTERN NUMBERS : 9020 0 0

TRANSMISSION GATE MNEMONIC : TGTE

TRANS. GATE ACTIVATION LEVEL : LOGIC 0

TRANS. GATE ANALYSIS RULE1 : 0

TRANS. GATE ANALYSIS RULE2 : 0

TRANS. GATE ANALYSIS RULE3 : 0

INPUT DECK TYPE : PRE

*** INPUT DECK ECHO ***

```
PLACTAPE
TEST TEST TEST TEST TEST
 PARAMETERS
   4                                                    9034
 INITIAL PLACEMENT
   6
   7
   8
   9
 ASSIGNMENT OF GATES TO PATTERNS
  14
   19034    29034    39034    49034    59034    61220    71120    81110    91430
  109034   119034   129034   139034   149034
 NET LIST
  13
    1    1    2    6    3
    1    2    2    6    4
    1    3    2    7    3
    1    4    2    7    4    8    3
    1    5    2    9    3
    1    6    2    9    2
    1    7    2    9    5
    1    8    2    9    6
    1    9    8   13    2
    1    9    9   14    2
    1   10    2    9    4
    1   11    2    9    7
    1   12    2    9   10
```

*** END OF INPUT DECK ***

*** BEGIN TRANSLATION PROCESS ***

```
*** END OF TRANSLATION PROCESS. THE FOLLOWING FILE HAS BEEN RECORDED ON FORTRAN LOGICAL UNIT 10 ***

  1       TEST TEST TEST TEST TEST
  2       DTMR    1,10
  3       DTMR    2,15
  4       DTMR    3,20
  5       DTMF    1,5
  6       DTMF    2,10
  7       DTMF    3,20
  8       DCTM    1,100
  9       REM     1  41430******01**0101HH
 10       NET     8=2       NAND * 1,1,0,0        4=2
 11       NET     7=2       NOR  * 1,2,0,0        3=2,4=2
 12       NET     6=2       NAND * 2,2,0,0        1=2,2=2
 13       NET     9=8       1430 * 3,3,1,0        5=2,10=2,11=2,9=AA
 14       NET     9=9       TGTE * 0,0,0,0        9=8,12=2
 15       NET     9=AA      TGTE * 0,0,0,0        6=2,5=2
 16       NET     9=AA      TGTE * 0,0,0,0        7=2,10=2
 17       NET     9=AA      TGTE * 0,0,0,0        8=2,11=2
 18       GEN     1=2
 19       GEN     2=2
 20       GEN     3=2
 21       GEN     4=2
 22       GEN     5=2
 23       GEN     10=2
 24       GEN     11=2
 25       GEN     12=2
 26       PAT     9=8     9=9

*** END OF FILE 10 ***
```

*** BEGIN TRANSMISSION GATE ANALYSIS ***

***** TRANSMISSION GATE NETWORK DETECTED AND ANALYZED, DESCRIPTION FOLLOWS *****

OUTPUT TERMINAL: OUT=9=9

INPUT TERMINALS: D1=9=8

CLOCK TERMINALS: C1=12=2

TRUTH TABLE:

D1	C1	OUT
0	0	0
0	1	*
1	0	1
1	1	*

*** THE FOLLOWING ROM SPECIFICATION HAS BEEN GENERATED TO SIMULATE THE PRECEDING TRANSMISSION GATE NETWORK.

```
ROM    1  2TG  0=1*
```

***** TRANSMISSION GATE NETWORK DETECTED AND ANALYZED, DESCRIPTION FOLLOWS *****

OUTPUT TERMINAL: OUT=9=AA

INPUT TERMINALS: D1=6=2
D2=7=2
D3=8=2

CLOCK TERMINALS: C1=5=2
C2=10=2
C3=11=2

TRUTH TABLE:

D1	D2	D3	C1	C2	C3	OUT
0	0	0	0	0	0	*
0	0	0	0	0	1	*
0	0	0	0	1	0	*
0	0	0	0	1	1	0
0	0	0	1	0	0	*
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	*
•	•	•	•	•	•	•
0	0	1	0	1	0	*
0	0	1	0	1	1	0
0	0	1	1	0	0	*
0	0	1	1	0	1	0
0	0	1	1	1	0	1
0	0	1	1	1	1	*
•	•	•	•	•	•	•
0	1	0	0	1	0	*
0	1	0	0	1	1	0
0	1	0	1	0	0	*
0	1	0	1	0	1	1
0	1	0	1	1	0	0
0	1	0	1	1	1	*
•	•	•	•	•	•	•
0	1	1	0	1	0	*
0	1	1	0	1	1	0
0	1	1	1	0	0	*
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	*
•	•	•	•	•	•	•
1	0	0	0	1	0	*
1	0	0	0	1	1	1
1	0	0	1	0	0	*
1	0	0	1	0	1	0
1	0	0	1	1	0	0
1	0	0	1	1	1	*
•	•	•	•	•	•	•
1	0	1	0	1	0	*

1	0	1	0	1	1	:	1
1	0	1	1	0	0	:	*
1	0	1	1	0	1	:	0
1	0	1	1	1	0	:	1
1	0	1	1	1	1	:	*
.	.	.	.	.	.	:	.
1	1	0	0	1	0	:	*
1	1	0	0	1	1	:	1
1	1	0	1	0	0	:	*
1	1	0	1	0	1	:	1
1	1	0	1	1	0	:	0
1	1	0	1	1	1	:	*
.	.	.	.	.	.	:	.
1	1	1	0	1	0	:	*
1	1	1	0	1	1	:	1
1	1	1	1	0	0	:	*
1	1	1	1	0	1	:	1
1	1	1	1	1	0	:	1
1	1	1	1	1	1	:	*

*** THE FOLLOWING ROM SPECIFICATION HAS BEEN GENERATED TO SIMULATE THE PRECEDING TRANSMISSION GATE NETWORK

```
ROM     1   6TG01***0*00****0*01****0*10****0*11****1*00****1*01****1*10*
ROM     2   6TG01***1*11*
```

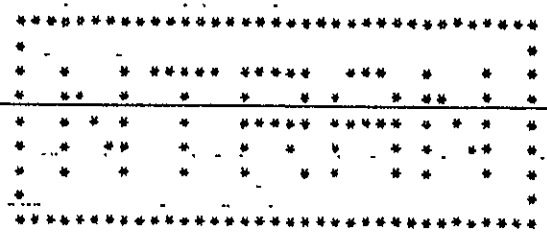
```
*** END OF TRANSMISSION GATE ANALYSIS. THE FOLLOWING FILE HAS BEEN RECORDED ON FORTRAN LOGICAL UNIT 11 ***
    1       TEST TEST TEST TEST TEST
    2       DTMR    1,10
    3       DTMR    2,15
    4       DTMR    3,20
    5       DTMF    1,5
    6       DTMF    2,10
    7       DTMF    3,20
    8       DCTM    1,100
    9       RBM     1  41430******01**0101HH
   10       RBM     1  2TG  0*1*
   11       RBM     1  6TG01***0*00****0*01****0*10****0*11****1*00****1*01****1*10*
   12       RBM     2  6TG01***1*11*
   13       NET     8-2       NAND * 1,1,0,0        4-2
   14       NET     7-2       NOR  * 1,2,0,0        3-2,4-2
   15       NET     6-2       NAND * 2,2,0,0        1-2,2-2
   16       NET     9-8       1430 * 3,3,1,0        5-2,10-2,11-2,9-AA
   17       NET     9-9       TG     0,0,0,0        9-8,12-2
   18       NET     9-AA      TG01   0,0,0,0        6-2,7-2,8-2,5-2,10-2,11-2
   19       GEN     1-2
   20       GEN     2-2
   21       GEN     3-2
   22       GEN     4-2
   23       GEN     5-2
   24       GEN     10-2
   25       GEN     11-2
   26       GEN     12-2
   27       PAT     9-8     9-9

*** END OF FILE 11 ***
*STOP* 0
```

```
 10:33 JUL 25,'75 ID* OFC
JOB ?C03,FC4R001(PAST/CAD),1
LIMIT (TIME,5),(CORE,60),(ORDER)
PCL
 COPY C? TO LASLIB
 COPY LASLIB TO LP
LASAR   C?7S0190300C1?     9020          TGTE
1210
MODEL/1 A/3/2/                                                    1110
MODEL/1 A/4?/2/2NA/4,?/AB/1NA/3/A/1NA/4/B/                        1120
MODEL/2 A/3,4/2/                                                  1220
MODEL/3 A/3,4,5/2/                                                1230
MODEL/4 A/3,4,5,6/2/                                              1240
MODEL/1 A/7/6/2NA/AA,BB/7/2NA/3,5/AA/2NA/4,7/BB/                  1290
MODEL/1 A/3/2/                                                    1310
MODEL/? ?/2,3/4/                                                  1320
MODEL/1 A/3/A?/2NA/4/?B/3NA/7/AC/4NA/2,AA/BA/5NA/5,AB/BB/6NA/6,AC/BC/  1430
      7 A/BA,BB,BC/8/TGTE/3,10/9/                                 1430
ILL        3      4      7      8                                 1430
ILL        3      4      7     -8                                 1430
ILL       -3     -4      7      8                                 1430
ILL       -3     -4      7     -8                                 1430
ILL       -3      4     -7      8                                 1430
ILL       -3      4     -7     -8                                 1430
ILL        3     -4     -7      8                                 1430
ILL        3     -4     -7     -8                                 1430
MODEL/2 A/3,4/AA/1NA/AA/2/                                        1620
MODEL/4 A/3,4,5,6/AA/1NA/AA/2/                                    1640
MODEL/2 A/2,3/AA/2NA/4,5/BB/2NA/AA,BB/CC/1NA/CC/6/                1870
MODEL/2 A/2,3/AA/2NA/4,5/BB/2NA/6,7/CC/3NA/AA,BB,CC/8/            1890
MODEL/2 A/2,3/AA/1NA/4/A?/2NA/AA,AB/AC/1NA/AC/AD/2NA/AD,C2/AE/1NA/C2/AF/  2240
      3 A/AD,AF,5/AG/2NA/AF,AG/5/                                 2240
MODEL/1 A/3/AA/1NA/4/BB/2NA/AA,4/CC/2NA/BB,3/DD/2NA/CC,DD/2/      2310
```

43

```
ASSIGN FI1,(FILE,LASLIB),(IN)
ASSIGN FI2,(FILE,TEMP),(SUTIN)
ASSIGN FI4,(DEVICE,CR),(IN)
ASSIGN FI5,(DEVICE,LP),(OUT)
ASSIGN FI10,(FILE,PHASE1),(SUTIN),(SAVE)
ASSIGN FI11,(FILE,PHASE2),(SUTIN),(SAVE)
ASSIGN FI12,(FILE,PHASE3),(SUTIN),(SAVE)
RUN (LAS, TAP)
```



PROGRAM FUNCTION: NETWORK TRANSLATOR (GENERATES EQUIVALENT LOGSIM AND LASAR INPUT FROM PRF AND PR2D INPUT DECKS

DEVELOPED BY: MBS COMPUTING INC., HUNTSVILLE ALABAMA

PROGRAM EXECUTION MODE : START

TARGET PROCESSOR : LASAR

PROCESS TECHNOLOGY : CMOS

EXCLUDED PATTERN NUMBERS : 1210

INPUT PAD PATTERN NUMBERS : 9030 9010 0

OUTPUT PAD PATTERN NUMBERS : 9020 0 0

TRANSMISSION GATE MNEMONIC : TGTF

TRANS. GATE ACTIVATION LEVEL : LOGIC 0

TRANS. GATE ANALYSIS RULE1 : 0

TRANS. GATE ANALYSIS RULE2 : 0

TRANS. GATE ANALYSIS RULE3 : 0

INPUT DECK TYPE : PRF

*** INPUT DECK ECHO ***

```
PLACTAPE
TEST TEST TEST TEST TEST
 PARAMETERS
   4                                                    9034
 INITIAL PLACEMENT
   6
   7
   8
   9
 ASSIGNMENT OF GATES TO PATTERNS
  14
    19034   29034   39034   49034   59034   61220   71120   81110   91430
   109034  119034  129034  139034  149034
 NET LIST
  13
    1   1   2   6   3
    1   2   2   6   4
    1   3   2   7   3
    1   4   2   7   4   8   3
    1   5   2   9   3
    1   6   2   9   2
    1   7   2   9   5
    1   8   2   9   6
    1   9   8  13   2
    1   9   9  14   2
    1  10   2   9   4
    1  11   2   9   7
    1  12   2   9  10
```

*** END OF INPUT DECK ***

*** BEGIN TRANSLATION PROCESS ***

```
*** END OF TRANSLATION PROCESS. THE FOLLOWING FILE HAS BEEN RECORDED ON FORTRAN LOGICAL UNIT 10.***

      1        NAME=TEST TEST TEST TEST TEST
      2
      3
      4        NAMEL/
      5         1=A/4=2/8=2/
      6         1=A/7=AA/7=2/
      7         2=A/7=A,7=B/7=AB/
      8         1=A/3=2/7=A/
      9         1=A/4=2/7=A/
     10         2=A/1=2,2=2/4=2/
     11         1=A/5=2/9=AA/
     12         2=A/1=2/9=AB/
     13         3=A/11=2/9=AC/
     14         4=A/6=2,0=AA/9=BA/
     15         5=A/7=2,9=AA/9=BB/
     16         6=A/8=2,9=AC/9=BC/
     17         7=A/9=AA,9=BA,9=BC/9=B/
     18         TGTF/0=4,12=2/9=9/
     19
     20        INPUT/
     21        1=2,2=2,4=2,6=2,8=2,10=2,11=2,12=2/
     22
     23        OUTPUT/
     24        9=A,9=B/
     25        ILL 5=2      10=2      11=2      9=A
     26        ILL 5=2      10=2      11=2      =9=A
     27        ILL =5=2     =10=2     11=2      9=A
     28        ILL =5=2     =10=2     11=2      =9=A
     29        ILL =5=2     10=2      =11=2     9=A
     30        ILL =5=2     10=2      =11=2     =9=A
     31        ILL 5=2      =10=2     =11=2     9=A
     32        ILL 5=2      =10=2     =11=2     =9=A

*** END OF FILE 10 ***
```

*** BEGIN TRANSMISSION GATE ANALYSIS ***

***** TRANSMISSION GATE NETWORK DETECTED AND ANALYZED, DESCRIPTION FOLLOWS *****

OUTPUT TERMINAL: OUT=9=9

INPUT TERMINALS: D1=9=8

CLOCK TERMINALS: C1=12=2

TRUTH TABLE:

D1	C1	: OUT
0	0	: 0
0	1	: *
1	0	: 1
1	1	: *

*** EQUIVALENT AND NETWORK AND ILLEGALS FOR PRECEDING TRANSMISSION GATE NETWORK ***

```
INA/12=2/*12=2/
PNA/9=2/*12=2/PRO1=1/
INA/PRO1=1/9=9/
ILL 12=2     9=9
ILL 12=2     *9=9
```

```
*** END OF TRANSMISSION GATE ANALYSIS, THE FOLLOWING FILE HAS BEEN RECORDED ON FORTRAN LOGICAL UNIT 11 ***
      1        NAME=TEST TEST TEST TEST TEST
      2
      3
      4        MODEL/
      5         1=A/4=2/8=2/
      6         1=A/7=A1/7=2/
      7         2=A/7=A,7=B/7=AB/
      8         1=A/3=2/7=A/
      9         1=A/4=2/7=A/
     10         2=A/1=2,2=2/6=2/
     11         1=A/5=2/9=AA/
     12         2=A/10=2/9=AB/
     13         3=A/11=2/9=AC/
     14         4=A/6=2,9=AA/9=BA/
     15         5=A/7=2,9=A1/9=BB/
     16         6=A/8=2,9=AC/9=BC/
     17         7=A/9=BA,9=B1,9=BC/8=B/
     18         1=A/12=2/,12=2/
     19         2=A/9=B,,12=2/PR01=01/
     20         1=A/PR01=01/9=9/
     21
     22        INPUT/
     23         1=2,2=2,3=2,4=2,5=2,10=2,11=2,12=2/
     24
     25        OUTPUT/
     26         9=B,9=9/
     27         ILL 5=2     10=2     11=2     9=B
     28         ILL 5=2     10=2     11=2     =9=B
     29         ILL =5=2    =10=2    11=2     9=B
     30         ILL =5=2    =10=2    11=2     =9=B
     31         ILL =5=2    10=2     =11=2    9=B
     32         ILL =5=2    10=2     =11=2    =9=B
     33         ILL 5=2     =10=2    =11=2    9=B
     34         ILL 5=2     =10=2    =11=2    =9=B
     35         ILL 12=2    9=9
     36         ILL 12=2    =9=9

*** END OF FILE 11 ***
```

*** [illegible] FEEDBACK ORDERING PROCESS ***

*** CELL-PIN NAME TO LASER NODE NUMBER CROSS REFERENCE TABLE ***

1	1-2	2-2	3-2	4-2	5-2	10-2	11-2	12-2	8-2	7-A	
11	7-2	6-2	9-AA	9-AB	9-AC	*12-2	7-AB	9-BA	9-BC	PRO1-01	
21	7-2	9-AB	9-B	9-9							

```
*** END OF MINIMUM FEEDBACK PROBING PROCESS, THE FOLLOWING FILE HAS BEEN STORED ON FORTRAN LOGICAL UNIT 12 ***

      1        NAME*TEST TEST TEST TEST TEST
      2
      3
      4        MODEL/
      5         9\A/4/9/
      6         10\A/3/10/
      7         11\A/4/11/
      8         12\A/1,2/12/
      9         13\A/5/13/
     10         14\A/6/14/
     11         15\A/7/15/
     12         16\A/8/16/
     13         17\A/10,11/17/
     14         18\A/12,13/18/
     15         19\A/9,15/19/
     16         20\A/23,14/20/
     17         21\A/17/21/
     18         22\A/21,14/22/
     19         23\A/14,22,19/23/
     20         24\A/21,23/
     21
     22        INPUT/
     23        1,2,3,4,5,6,7,8/
     24
     25        OUTPUT/
     26        23,24/
     27        ILL     5    6    7   23        5    6    7  *23        *5   *6    7
     28        ILL    *3        *5   *6    7  *23             *5    6   *7   23        *5
     29        ILL     6   *7  *23         5   *6   *7   23         5   *6   *7  *23
     30        ILL         8   24         8  *24        23         5   *6   *7  *23

*** END OF FILE 12 ***
*STOP* 0
```

APPENDIX B

LIST OF NTRAN SUBROUTINES

NTRAN SUBROUTINES

SUBROUTINE NAME	FUNCTION
1. MAIN	FORTRAN "MAIN" program - controls and sequences execution of the major NTRAN subroutines.
2. BLOAD	Retrieves 2-bit byte from packed truth table.
3. BSTORE	Stores 2-bit byte in packed truth table.
4. CHGSIG	Changes all signal names in specified net to indicated value.
5. CHIPIO	Finds and identifies the chip inputs and outputs
6. CODILL	Codes pattern model illegals specifications such that they may be filed; then retrieved and correlated with their respective elements downstream in the translation process.
7. CONECT	Connects network elements according to PRF netlist.
8. CPACK	Converts hybrid signal names (half Hollerith, half integer) to pure Hollerith and left-justifies result.
9. DEGAS	Removes blank network entries created by transmission gate analysis to provide room for new network entries.
10. ERROFF	Writes indicated error message and terminates NTRAN execution.
11. FINDIO	Identifies the input and output terminals of a transmission gate network.
12. FMTBIN	Formats integer word for output in binary.
13. FNDPIN	Finds network entry address of specified cell-pin.
14. GROUP	Identifies group of interconnected transmission gates.

Table B-1

NTRAN SUBROUTINES
(continued)

SUBROUTINE NAME	FUNCTION
15. ILGEN1	Generates illegals for a transmission gate network that reflect clock combinations that do not connect an input terminal to the output.
16. ILGEN2	Generates illegals for a transmission gate network that reflect clock combinations that cause two or more input terminals to be connected.
17. ILLIN	Handles input from coded illegals temporary file.
18. ILLOUT	Handles output to coded illegals temporary file.
19. INSERT	Inserts copy of currently staged pattern model into network array and attaches PRF cell number to it.
20. LASCI	Creates card image in LASAR format for specified network entry.
21. LASGEN	Controls execution of a group of subroutines to generate initial network entries from a PRF deck and LASAR library.
22. LASIN	Reads interim LASAR output file to reestablish internal definition of data being processed (used for restarts).
23. LASOUT	Outputs network in LASAR format.
24. LASTGA	Controls execution of subroutines used to analyze transmission gate networks for LASAR translations.
25. LOGGEN	Controls execution of a group of subroutines to generate initial network entries from a PRF deck and LOGSIM library.
26. LOGIN	Reads interim LOGSIM output file to reestablish internal definition of data being processed (used for restarts).

Table B-1
(continued)

NTRAN SUBROUTINES
(continued)

SUBROUTINE NAME	FUNCTION
27. LOGOUT	Outputs network in LOGSIM format.
28. LOGTGA	Controls execution of subroutines used to analyze transmission gate networks for LOGSIM translations.
29. OPACK	Reformats numeric signal names assigned by subroutine ORDER for compatibility with LASOUT subroutine.
30. ORDER	Performs minimum feedback ordering process.
31. PLACE	Enters computed ROM in network for LOGSIM translations.
32. PNBCD	Converts PRF netlist pin numbers to BCD.
33. POP	"Pops" partially completed network trace out of simulated stack.
34. PRDGEN	Generates product gates for LASAR transmission gate analyses.
35. PRNET	Processes LOGSIM "NET" cards when reading pattern model from library.
36. PRNWGT	Processes LOGSIM "NEWGATE" cards when reading pattern model from library.
37. PRROM	Processes LOGSIM "ROM" cards when reading pattern model from library.
38. PRTMCD	Processes LOGSIM "DTMR," "DTMF," and "DCTM" cards when reading pattern model from library.
39. PUSH	"Pushes" partially completed network trace onto simulated stack.
40. RDPRF	Reads PRF input deck.
41. RDPR2D	Reads PR2D input deck.

Table B-1
(continued)

NTRAN SUBROUTINES
(continued)

SUBROUTINE NAME	FUNCTION
42. REFORM	Using subroutine CPACK, reformats network signal names to be pure Hollerith.
43. REXPAT	Removes excluded pattern numbers from PRF netlist.
44. RFFAN	Reads "Free Field" alphanumeric data.
45. RFFFX	Reads "Free Field" fixed point data.
46. RFMILL	Reformats pattern model illegals from a coded form to a form usable for LASAR input.
47. ROMGEN	Generates ROM to simulate transmission gate network for LOGSIM translations.
48. ROMOUT	Generates output in LOGSIM format to describe ROM generated by transmission gate analysis.
49. SCAN	"Scans" input records in LASAR format and extracts input and output signal names.
50. SPGEN	Generates sum of products network to simulate transmission gate network for LASAR translations.
51. SPOUT	Generates output in LASAR format to describe sum of products network generated by transmission gate analysis.
52. STAGE	Sets up pattern model in core for multiple insertion in the network array for LOGSIM translations.
53. STGLSR	Sets up pattern model in core for multiple insertion in the network array for LASAR translations.
54. SUMGEN	Generates summing gate for LASAR transmission gate analyses.

Table B-1
(continued)

NTRAN SUBROUTINES
(continued)

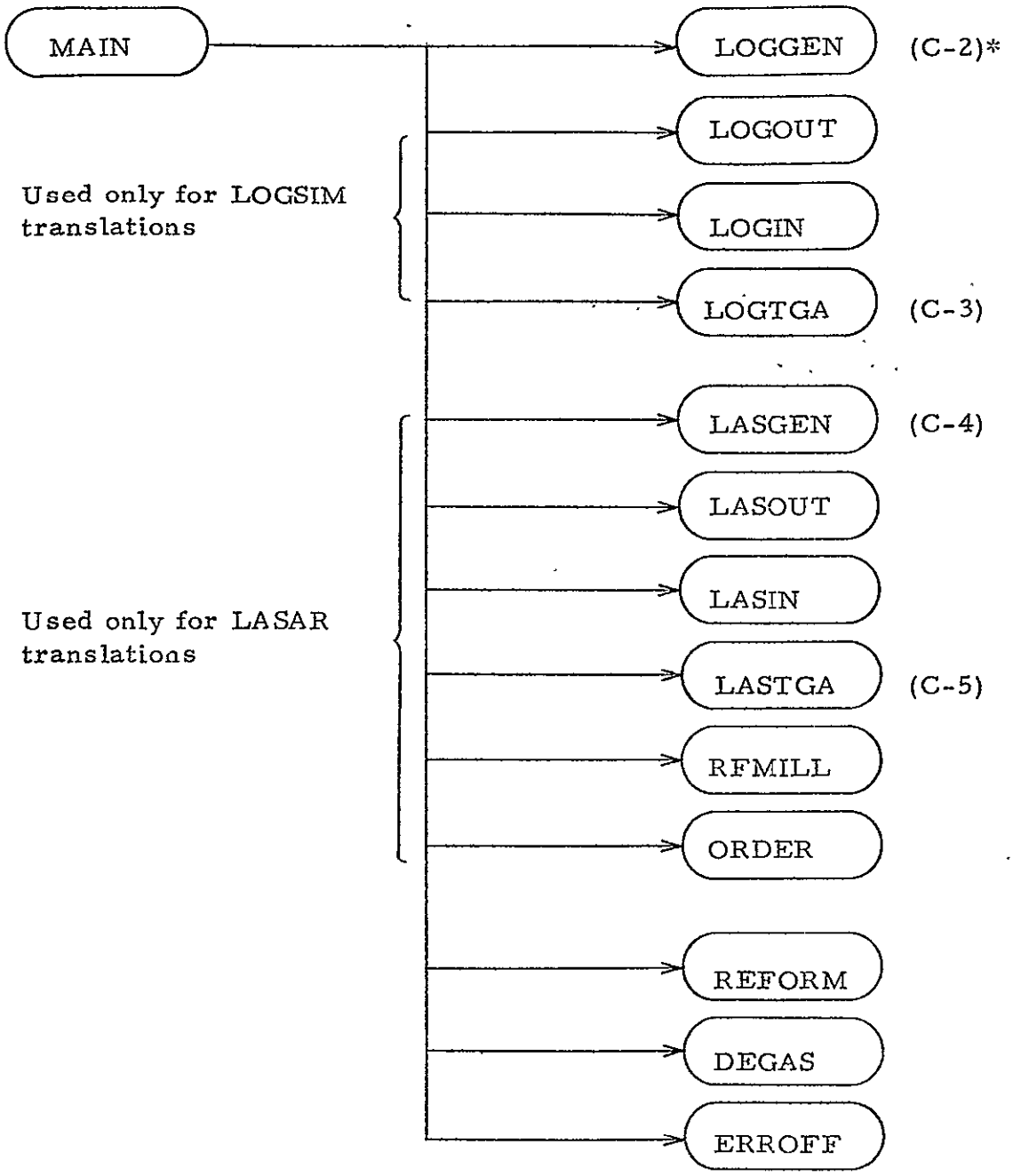
SUBROUTINE NAME	FUNCTION
55. TRACE	"Traces" a transmission gate network to find all possible paths of connection betweer an input terminal and an output terminal.
56. TTDISP	Displays truth table generated for transmission gate network.
57. TTGEN	Makes truth table entries reflecting connecting paths through transmission gate network.
58. TTINIT	Initializes truth table.
59. TTMOD	Modifies truth table reflecting cross connected input terminals.
60. WFFIX	Formats fixed point data for "Free-Form" output.

Table B-1
(continued)

APPENDIX C

NTRAN FUNCTIONAL HIERARCHY

MAIN PROGRAM



* Module is detailed in indicated figure.

Figure C-1

SUBROUTINE LOGGEN

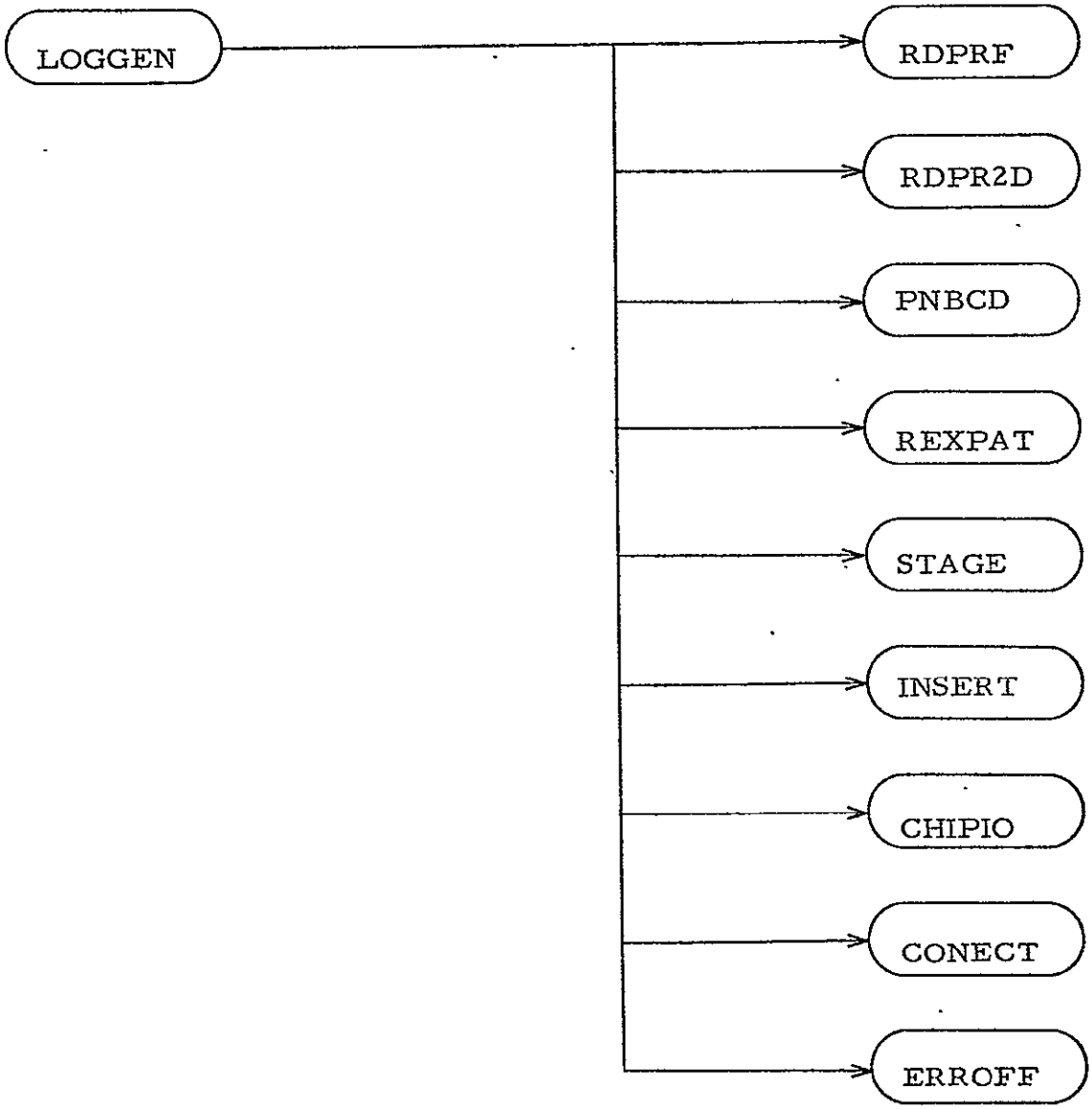


Figure C-2

SUBROUTINE LOGTGA

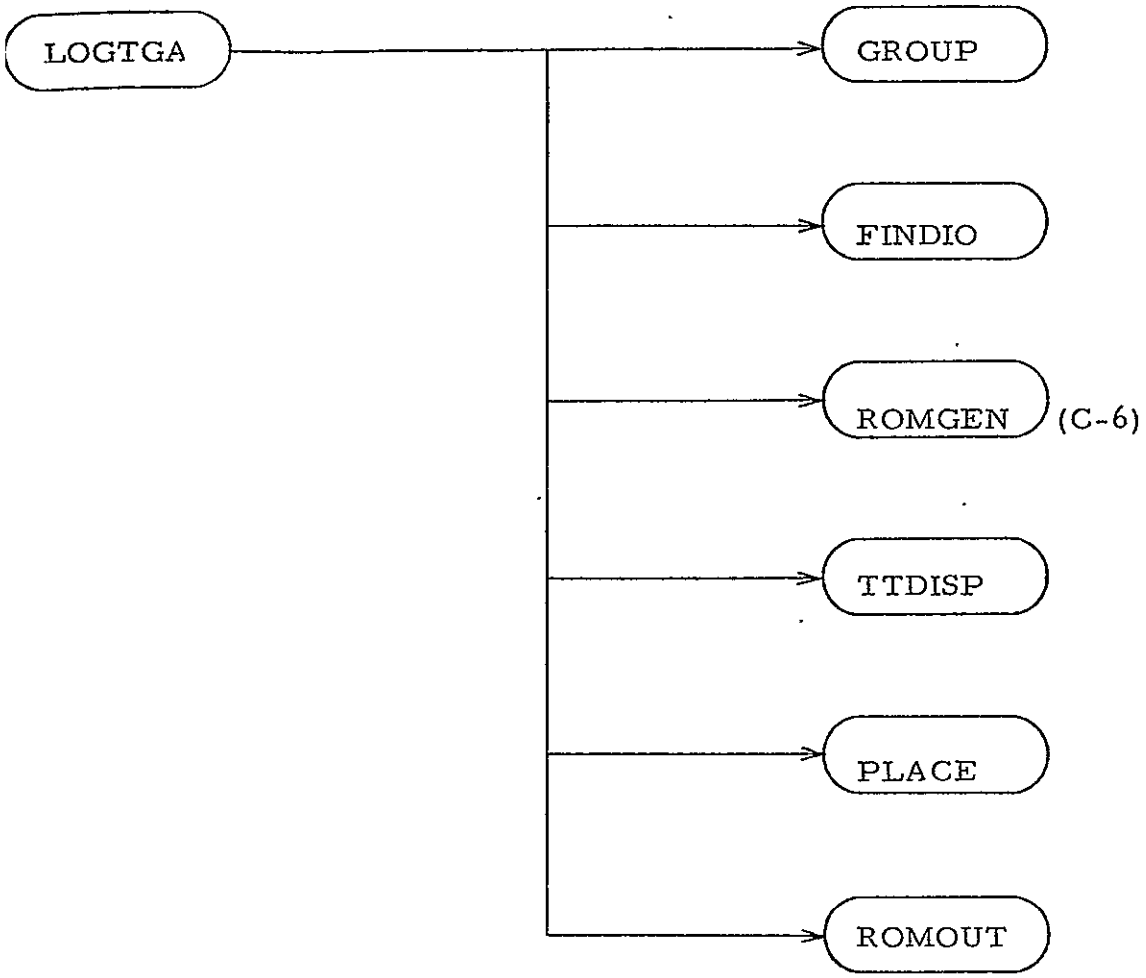


Figure C-3

SUBROUTINE LASGEN

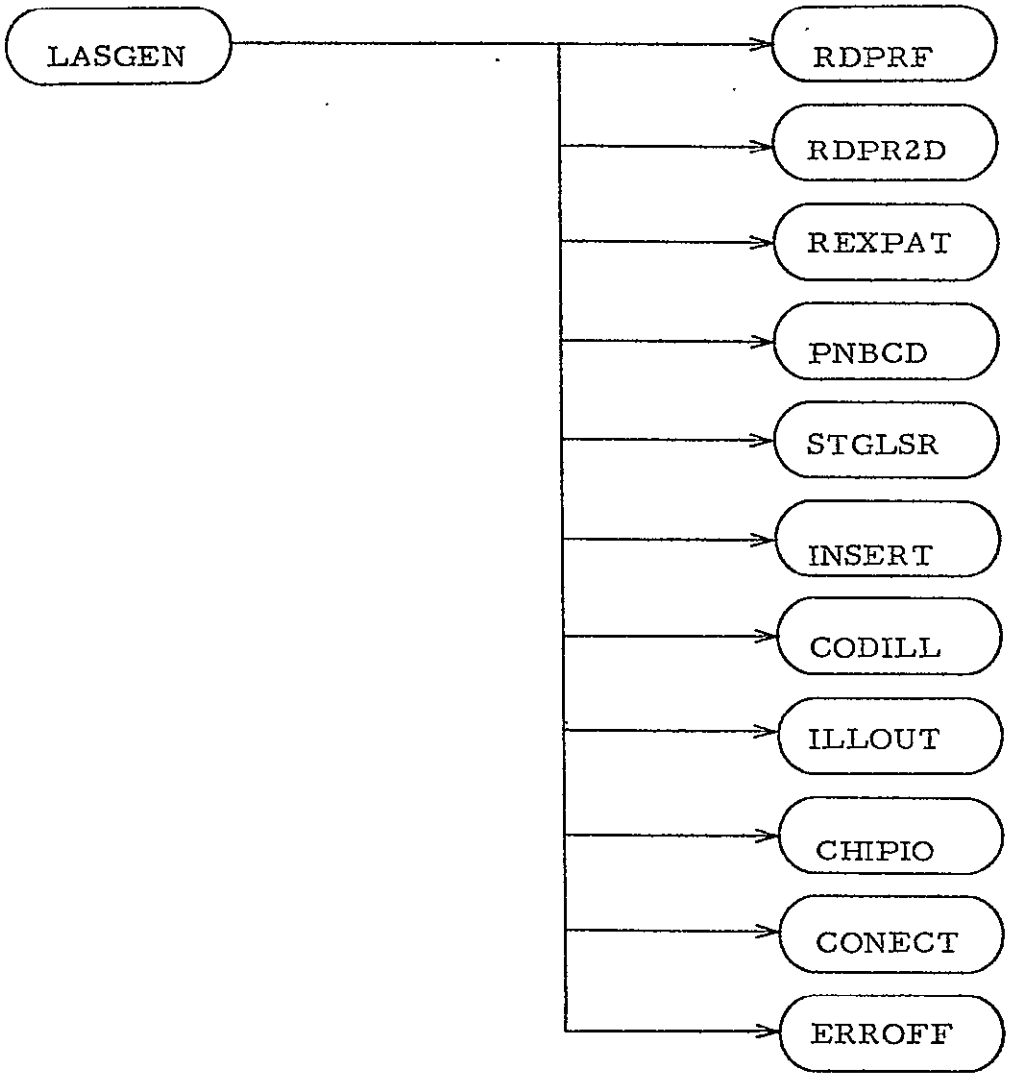


Figure C-4

SUBROUTINE LASTGA

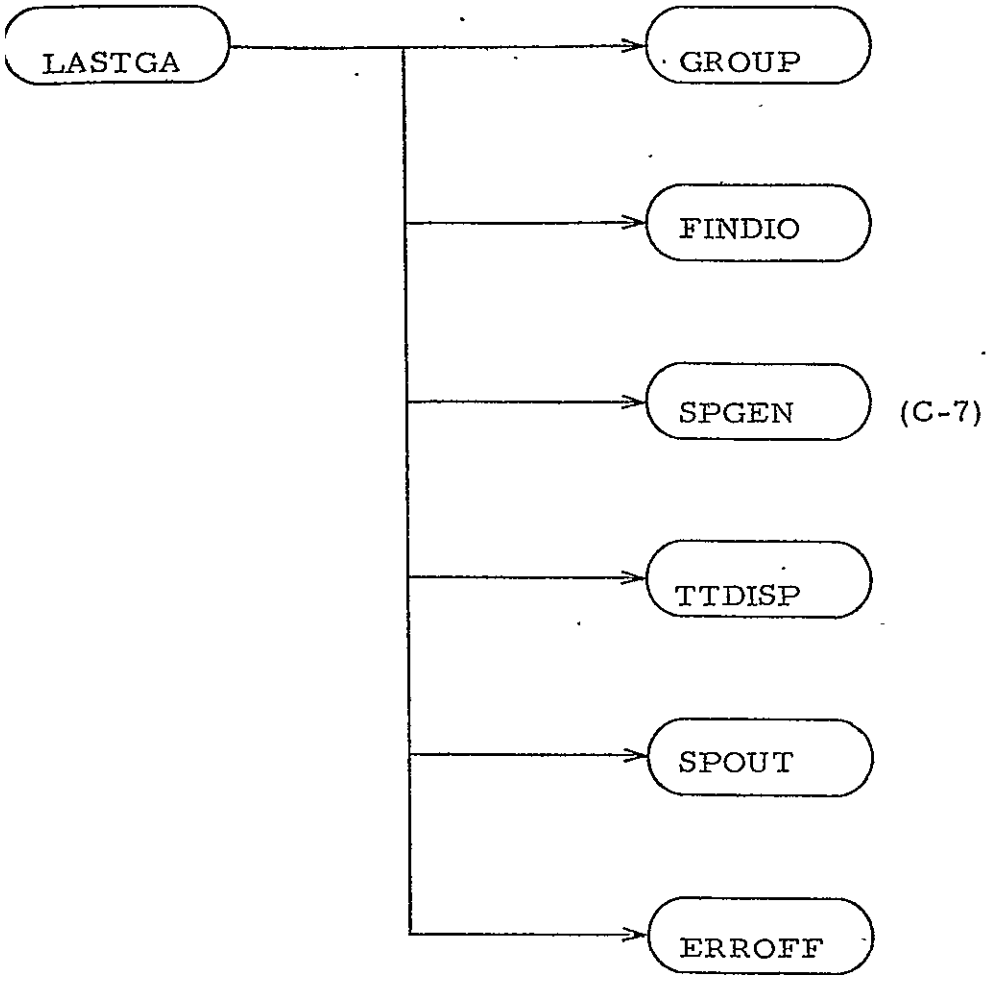


Figure C-5

SUBROUTINE ROMGEN

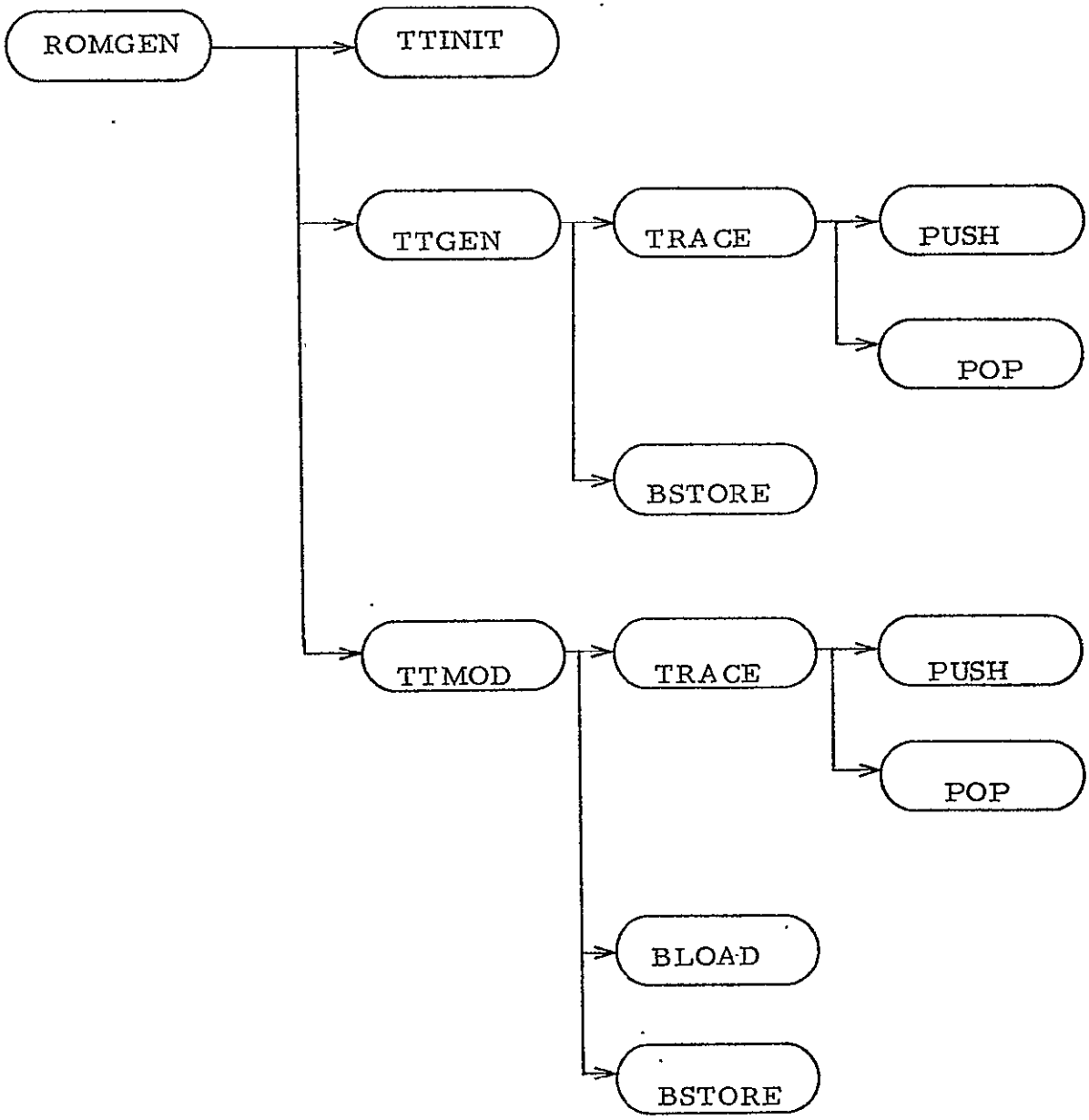


Figure C-6

SUBROUTINE SPGEN

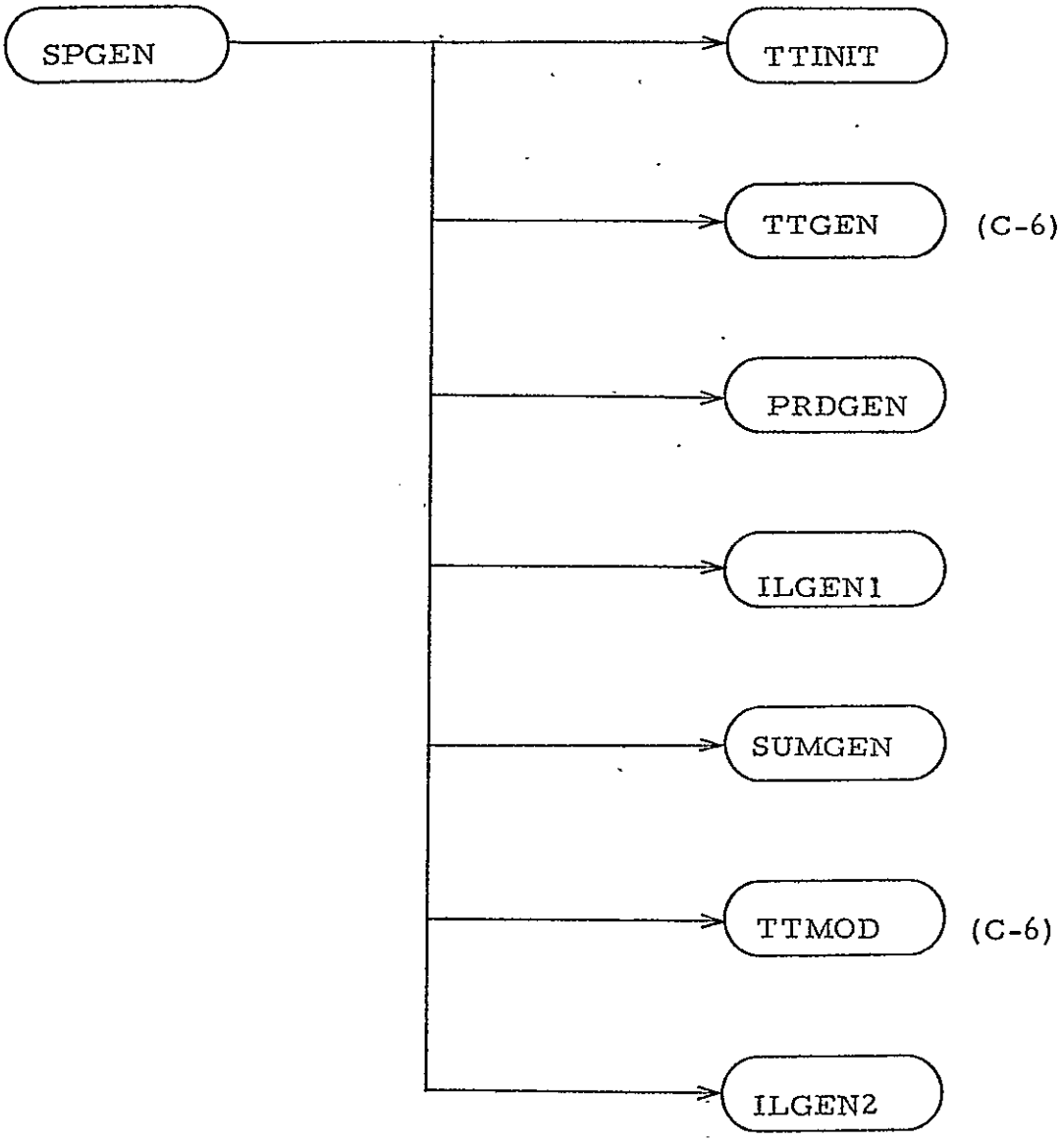


Figure C-7

☆ U.S. GOVERNMENT PRINTING OFFICE 1976—641-255/566 REGION NO. 4