ERDA/JPL/954289-75/1
QR-10042

DEVELOPMENT OF METHODS AND PROCEDURES FOR HIGH RATE LOW ENERGY EXPENDITURE FABRICATION OF SOLAR CELLS

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QUARTERLY PROGRESS REPORT NO. 1
JANUARY 1976

JPL CONTRACT NO. 954289
PERIOD COVERED 27 SEPT. – 31 DEC. 1975

THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION UNDER CONTRACT NAS7–100.

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ABSTRACT

The objective of this program is to develop high rate, energy efficient solar cell processing techniques based around ion implantation and elimination of all conventional thermal operations. Cells have been fabricated using an abbreviated series of vacuum process operations performed at room temperature.

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1.0 INTRODUCTION

The silicon solar cell as a semiconductor device has a relatively simple structure. This structure is deceptive in that, in spite of its basic simplicity, it has required relatively difficult and carefully controlled production processing to achieve high performance and environmental stability. Adaptation for terrestrial applications of production technology developed for spacecraft solar cells must be questioned. The needs for far higher production rates at drastically reduced costs probably using lower quality starting materials but without substantial relaxation of performance or reliability goals demands not alterations of existing methods but entirely new processing concepts.

Under this program for Development of Methods and Procedures for High Rate, Low Energy Expenditure Fabrication of Solar Cells, Simulation Physics is attempting to determine simple, fast and economical cell processing based around the use of ion implantation and electron beam technologies. It is assumed that resulting methods should be compatible with any form of silicon wafer, sheet or ribbon which may become available. The processing is defined to consist of a small number of inherently fast steps all of which must if possible be achievable at room temperature in a vacuum environment.

2.0 TECHNICAL DISCUSSION

2.1 Method and Objectives

Starting with a clean, properly surfaced silicon wafer the following is a very simple sequence for fabrication of an antireflected ion implanted N^+/P cell:

1. Implant 10^{15} cm^{-2} P^{31+}

2. Anneal implant damage (750°C/30 min)

3. Evaporate front contact

4. Evaporate back contact

5. Evaporate antireflective coating

6. Sinter contacts and antireflective coating (400 - 600°C/10 min).

Ion implantation and contact/AR coating deposition can be rapid. Present generation implanters are available with several milliamperes of scanned beam current. Assuming 10^{15} cm^{-2} fluence for cell junction formation, a 1 mA beam will process 6 cm^2 of cell wafer per second. Vacuum evaporation steps also require seconds. The two thermal processes dominate the time required for performing the simple fabrication sequence. These two steps also are generally not performed in a vacuum environment and because they are the only operations not conducted at room temperature, they involve most of the energy expenditure associated with cell processing. The processing parameters are summarized below:

Process	Environment	Process Time	Energy Consumption
Implant	Room Temp - Vacuum	Seconds	Small
Anneal	750°C - Forming Gas	30 min.	Large
Evaporate Contacts and AR Coating	Room Temp - Vacuum	Seconds	Small
Sinter	400-600°C - Forming Gas	10 min.	Large

Simulation Physics is attempting to develop a simple cell processing sequence comparable to that given above, but with replacement of the furnace operations by some alternative procedure which can be fast, which will involve little energy consumption and if possible can be performed under vacuum in order to be consistent with other steps in the sequence. A beam of low energy electrons from an electron beam generator operated in a pulse mode is being utilized to produce processing effects to substitute for those of the furnace anneal and sintering steps. Development of satisfactory electron beam parameters is being performed by Simulation Physics under Air Force Aero Propulsion Laboratory Contract F33615-75-C-2006 which is also related to advanced solar cell development and results from that effort are being adapted to the simple processing concept.

Figure 1 shows the spatial energy deposition profile in silicon resulting from typical electron beam parameters. A wafer 2 inches in diameter can be processed with electron beam duration less than one microsecond and with beam fluence less than 1 cal/cm^2. Calculated temperature profiles in the silicon as functions of time following completion of electron beam exposure are given in Figure 2 for representative beam conditions. Transient high temperatures in the surface region being processed relax in a period of a few microseconds.

By combining electron beam and ion implantation methods, a procedure is being developed which will allow cell fabrication under the following constraints:

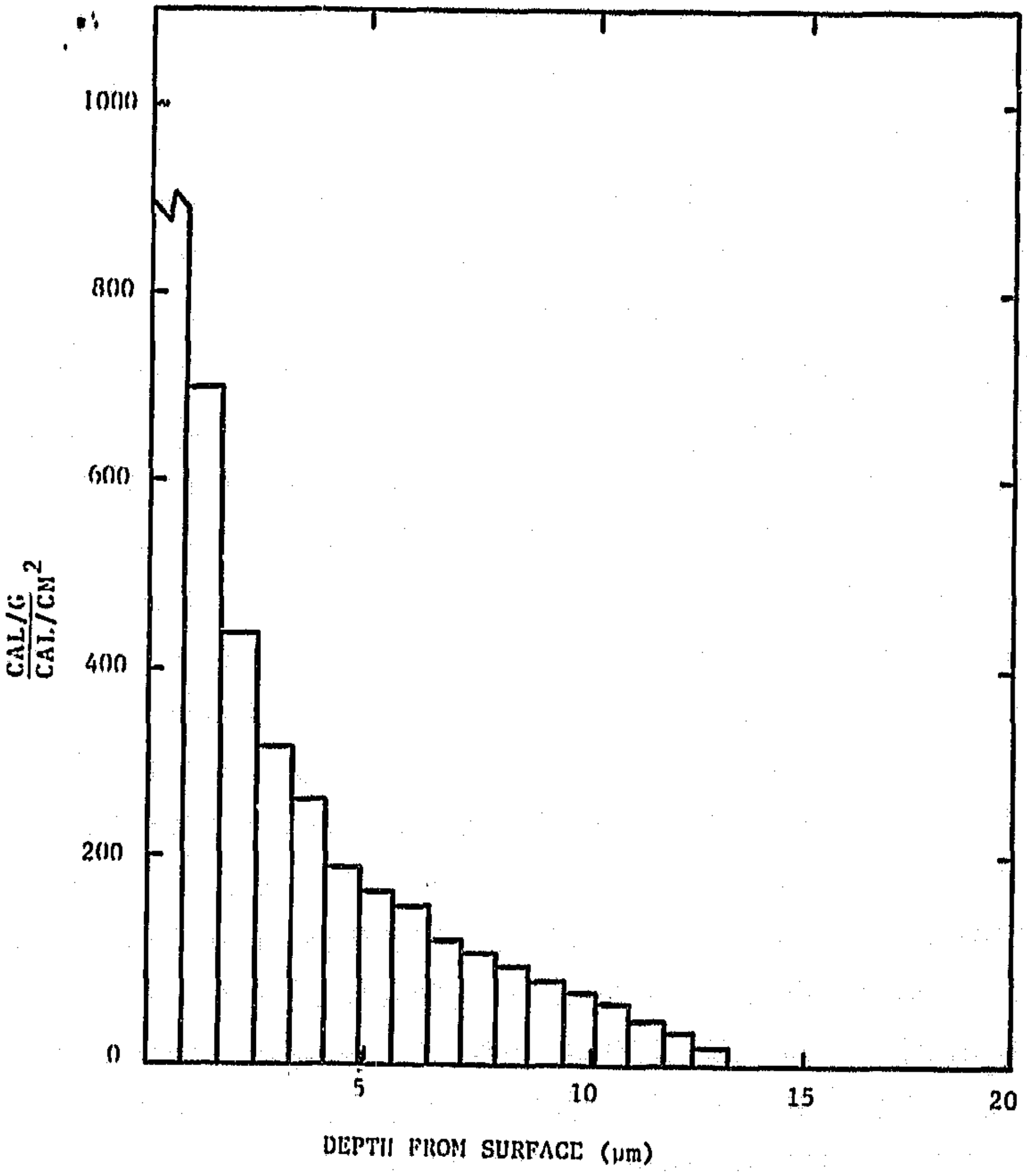

FIGURE 1. ELECTRON PULSE DOSE VERSUS DEPTH PROFILE FOR SILICON

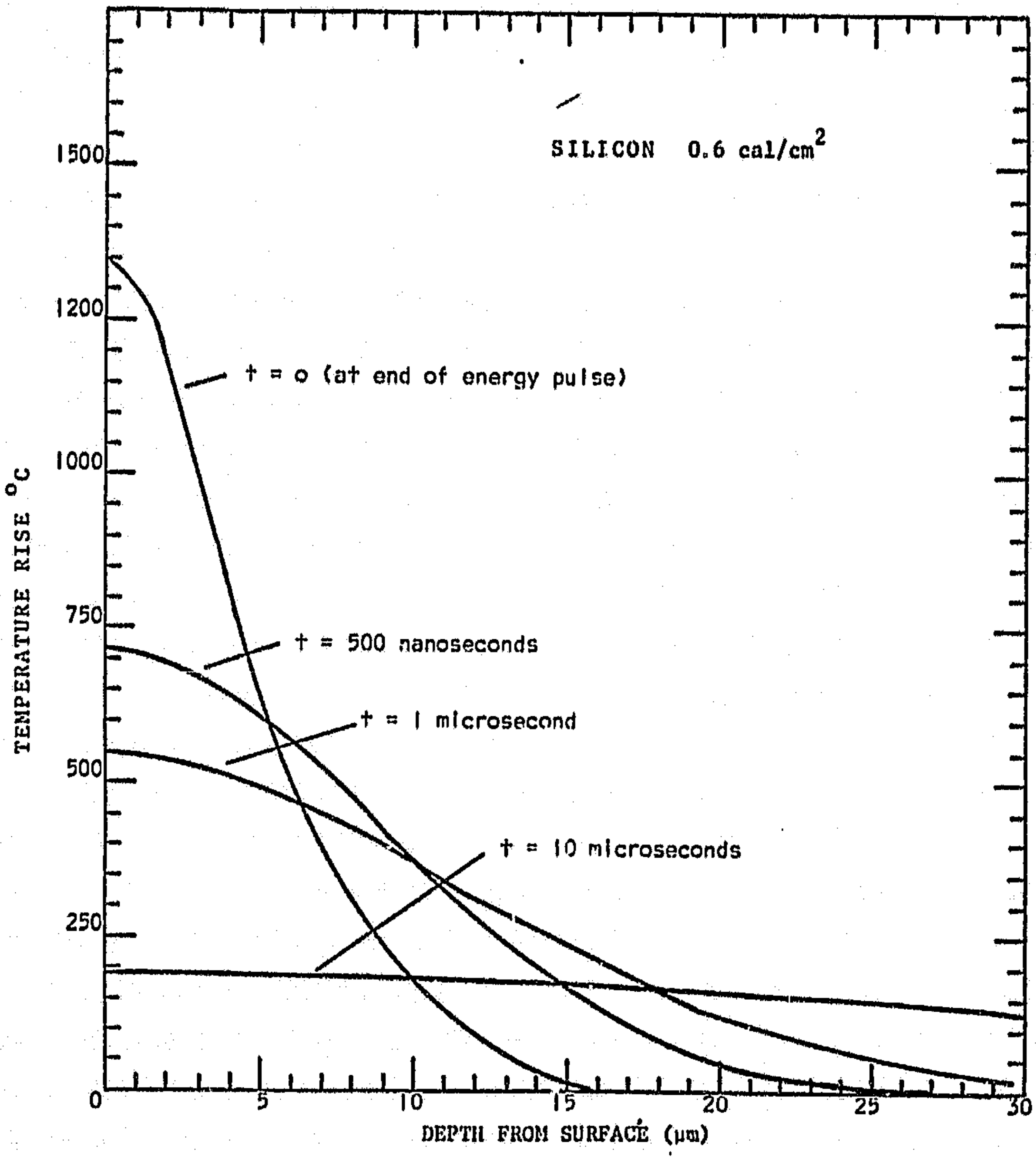

FIGURE 2. PREDICTED TE... TURE RISE PROFILES

(1) No etching or cleaning operations.

(2) No batch process operations.

(3) No nonvacuum operations.

(4) No conventional thermal operations.

(5) No consumable materials other than those as cell components.

(6) General applicability to a wide variety of silicon material forms.

(7) Direct processing energy less than 5 cal/cm^2.

(8) Total processing time (silicon wafer to finished cell) less than 30 seconds/cm^2.

Requirements (7) and (8) regarding process energy and time are area dependent. Demonstration under this program is to be conducted using 2 x 2 cm cells. Direct process energy (energy incident upon the cell surface) will be less than 20 calories total and processing time will be less than 2 minutes for the cell.

2.2 Technical Status

In order to determine parmeters for minimized process fabrication of ion implanted cells it is necessary to evaluate ion implanted cells processed without concern for simplification. Performance of these cells can be considered a goal to be demonstrated using a simple process sequence subject to the constraints which have been listed above. Figure 3 shows the AMO I-V characteristic of a 10 ohm-cm N^+/PP^+ cell fabricated using

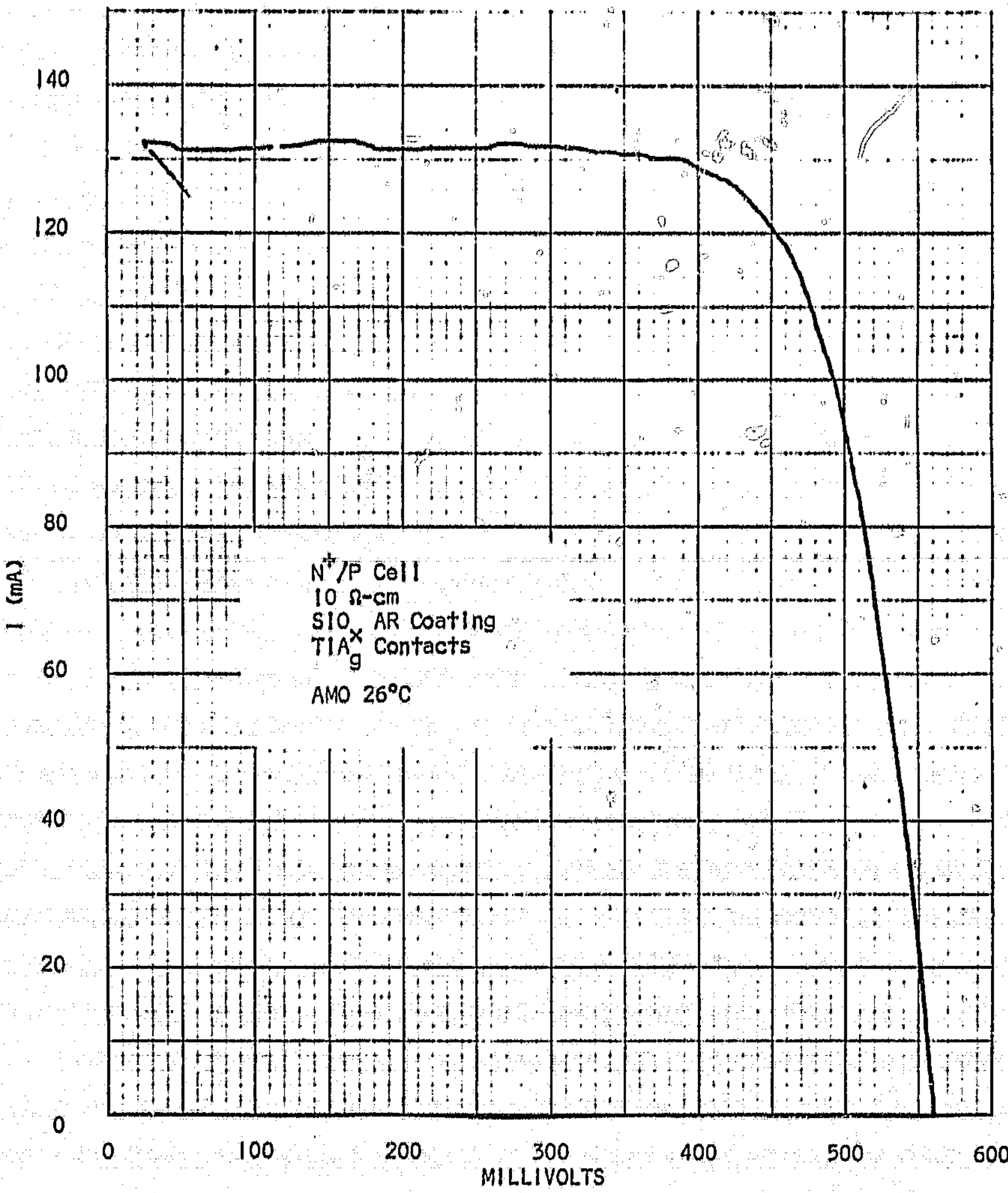

FIGURE 3. AMO I-V CHARACTERISTIC OF CELL FABRICATED WITH ION IMPLANTATION AND CONVENTIONAL PROCESSING.

implantation through an oxide to improve the junction profile and using conventional heating for anneal and sintering operations. The cell of Figure 3 has maximum power output of 54 mW under 135 mW/cm^2 AMO illumination which is 10% efficiency. Additional optimization of the junction and reduction of series resistance should result in efficiency beyond 11% AMO.

The use of the electron beam for implant anneal and contact sintering is being successfully employed in cell fabrication. The results of a comparison of furnace and electron beam annealing of 10^{15} cm^{-2} P^{31+} 25 keV implants into 10 ohm-cm N-type silicon are as follows:

Anneal	Measured Sheet Resistance
None	>5000 Ω/□
Furnace 750°C/60 min	85 - 110
Electron Beam 0.3 cal/cm^2	45 - 72

The AMO I-V characteristic of the best cell fabricated to date using ion implantation, simple vacuum-only processing, and electron beam replacement for thermal operations is shown in Figure 4. This particular cell had aluminum contacts and no antireflective coating. The cell exhibits high shunt resistance, reasonably low series resistance and good curve factor. Open circuit voltage is approximately 20 mV lower than that exhibited by similar 10 Ω-cm cells fabricated using conventional thermal procedures.

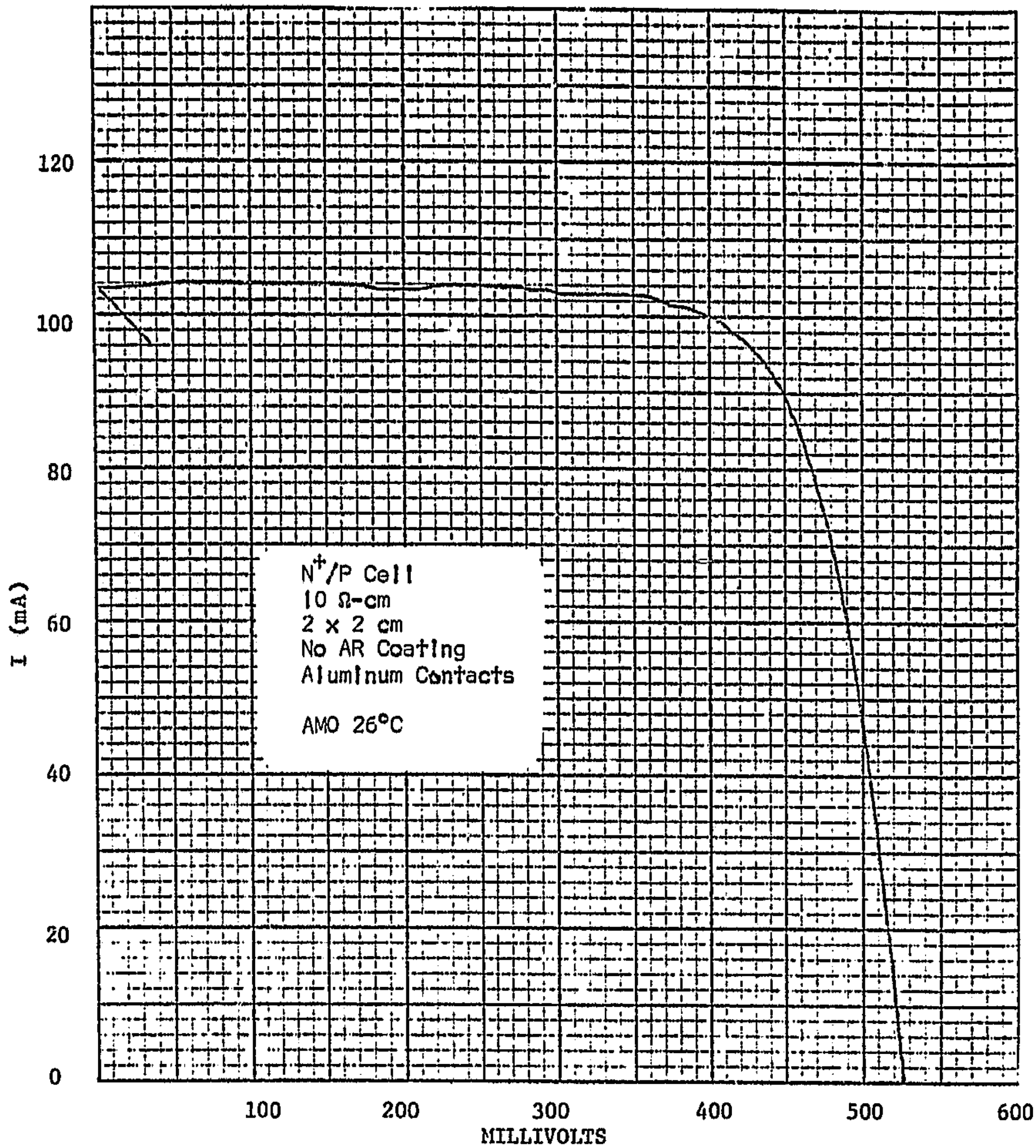

FIGURE 4. AMO I-V CHARACTERISTIC OF CELL FABRICATED WITH ION IMPLANTATION/ELECTRON BEAM PROCESSING

3.0 CONCLUSIONS AND RECOMMENDATIONS

Solar cells are being fabricated using only vacuum operations with the cell wafer held essentially at room temperature throughout processing. It is this capability which is necessary for successful achievement of program objectives. Cell performance must be improved. The program is proceeding according to plan.

4.0 APPENDICES

4.1 New Technology

No new technology has been identified during the period of this report.

4.2 Program Plan

An updated program schedule is given in Table I.

4.3 Man Hours and Costs

Total man-hours and costs for the period from program inception to 31 December 1975 were 1565 hours and $35,286 respectively.

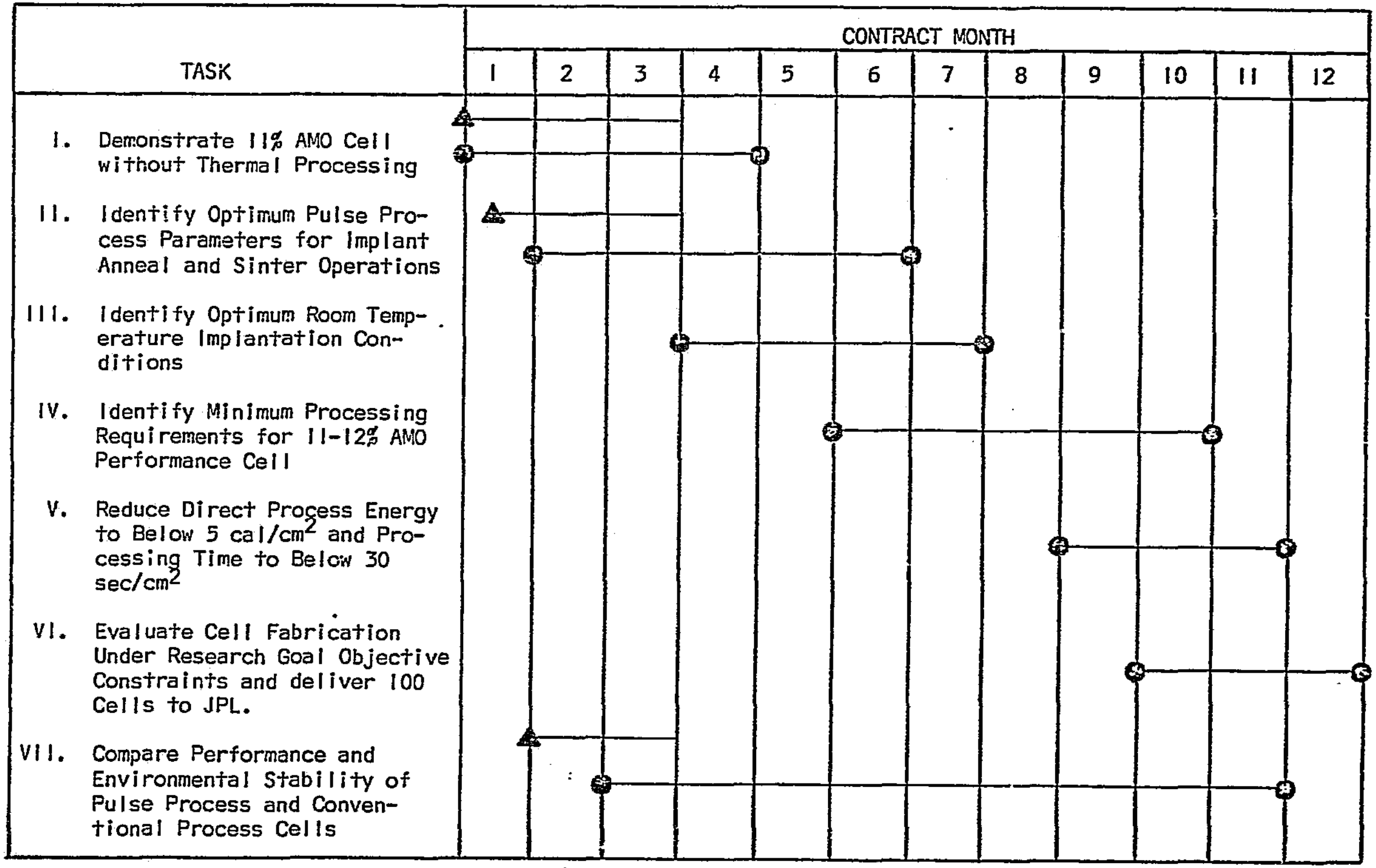

Table I. Program Schedule.