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EFFECT OF INTERFACIAL OXIDE LAYERS ON THE

CURRENT-VOLTAGE CHARACTERISTICS OF Al-Si CONTACTS

Report Prepared for NASA Contract #NAS8-26379

by

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ABSTRACT

An experimental study has been made of aluminum-silicon contacts with very thin interfacial oxide layers (15 ~ 100 Å) and various surface impurity concentrations (10^{16} ~ 10^{20} atoms/cm^3) for both n and p-type silicon. To determine the surface impurity concentrations on p^{+}-p and n^{+}-n structures, a modified C-V technique is utilized. Effects of interfacial oxide layers and surface impurity concentrations on current-voltage characteristics are discussed based on the energy band diagrams from the conductance-voltage plots. The interfacial oxide and aluminum layer causes image contrasts on X-ray topographs.

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CHAPTER I

INTRODUCTION

It has long been known that when a metal is placed in contact with a semiconductor, a rectifying contact often results. The first rectifying metal-semiconductor point contact was discovered by Braun (1) in 1874. Braun properly identified the origin of the rectification as the interface itself. In the 1930's, Schottky (2) developed the first acceptable theory of rectification for metal-semiconductor contacts. Schottky suggested that the potential barrier could arise from stable space charges in the semiconductor and the barrier height is simply the difference between the metal work function and the electron affinity of the semiconductor and is independent of the semiconductor doping. However, in 1947 Bardeen (3) proposed an extension of the theory to take surface states into account. Bardeen showed that if the density of localized surface states having energies distributed in the semi-conductor energy gap is sufficiently high, a double layer at the free surface of a semiconductor is formed from a net charge of electrons in the surface states. Further, a space charge of opposite sign along with this double layer tends to make the work function independent of the Fermi level in the interior (which in turn depends on the impurity content). The difference in work function between a metal and a semi-conductor is compensated by surface state charges, rather than by space charges. Thus, the rectification characteristics of the metal-semi-conductor contacts are practically independent of the metal. Surface

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The citations on the following pages follow the style of the *Journal of Electrochemical Society*.

states can occur either from the termination of the periodic structure

of the semiconductor crystal at the surface or from the presence of

absorbed foreign atoms on the surface. Mead (4) has reviewed an

extensive series of data and concluded that semiconductors can be

grouped into two broad classes: (a) On the covalent semiconductors,

such as Si, Ge, and GaAs, the barrier energies do not depend very

strongly upon which metal is placed on the semiconductor surface, and

are thus largely a property of the semiconductor itself. The barrier

energies would be about two-thirds of the band gap. (b) By contrast,

on the more ionic semiconductors such as Cds, ZnS, and ZnO barrier

energies are a function of both the work function of the metal and of

the semiconductor.

Schottky diodes have been studied more extensively for their

scientific interest since the demand for higher frequency devices and

higher speed switching devices has increased. On the other hand, de-

spite the great importance of ohmic contacts to the semiconductor

industry, relatively few studies have been published on ohmic contacts.

One good review (5) was carefully organized. A number of inherent

difficulties associated with ohmic contract studies are: (a) Little is

known about the work functions of thin metal films. The work function

depends on the condition of the metal surface which is often very

difficult to define. (b) The presence of a native SiO_2 skin, or con-

tamination on the silicon contact surface, further complicates the

situation. (c) Relatively little is known about the effect of surface

states. "Ohmic" contacts between a metal and a semiconductor are de-

fined as those which exhibit linear current-voltage characteristics.

However, if the contact can supply the required current density with a voltage drop that is sufficiently small compared with the drop across the active region of the device, the current-voltage behavior of the contact may not be strictly linear (7). This rectification is a result of an energy barrier between the metal and the semiconductor. In order to form ohmic contacts, two general approaches (8) can be applied: (a) choose a metal which makes a low Schottky barrier with the semiconductor, or (6) highly dope the semiconductor near the contact so that the barrier will be thin enough to be easily penetrated by tunneling. General techniques of providing a highly doped surface-layer are alloy regrowth, in-diffusion of a dopant contained in the contact material, epitaxial regrowth, shallow diffusion and ion-implantation.

It is a common practice in the industry to use a short dip in an oxide etchant just prior to aluminum evaporation in order to remove any native oxide. The existance of an intervening oxide layer is one of the major causes of poor ohmic contacts. Nevertheless, the oxide layer must play an essential part in any theory of metal-semiconductor contacts. For instance, the ageing of current-voltage characteristics of Al-Si contacts has been reported by Northrop (9). Turner (10) has obtained the experimental result that chemically prepared surfaces give lower barrier heights than cleaved surfaces. The barrier height lowering is due to the image force which is attributed to the presence of a thin oxide layer between the metal and the semiconductor (11). A theoretical and experimental study has been made of silicon Schottky diodes in which the metal and semiconductor are separated by a thin interfacial film. It is possible, over a range of bias voltages, to

increase the reverse current in tunnel MOS diodes by increasing the thickness of the interfacial oxide layer (12,13). Ohmic contacts of aluminum to both n and p-type silicon are tunneling dominated (14). Quantum mechanical tunneling is the dominant mechanism for current flow in metal-insulator-semiconductor structures with insulating layers of about 10Å to 100Å(15). Tunneling into states at the insulator-semiconductor interface was considered by Gray (16), Waxman et al. (17) as well as Dahlke and Sze (18). The latter found experimentally, and explained qualitatively, a marked dependence of the d.c. tunneling current on the interface state density. These interface states could be expected to act either as available energy states in the otherwise forbidden energy gap or as recombination centers for the electrons tunneling from the metal. A surface state distribution in thin-oxide MOS structures has been studied by Hunter et al. (19) and Kar (20,21). They have observed a strong influence of metal diffusion through the oxide on interface-state formation. For thick thermally grown silicon dioxide (ᵥ1000Å), a space-charge - limited flow (22) as well as Fowler-Nordheim emission (23) were found to be the current conduction mechanisms.

It is well known that the presence of any interfacial oxide layer causes poor ohmic contacts. However, a useful application of one of the effects of interfacial oxides was recently reported (24). Silicon-Schottky-barrier solar cells having a carefully grown oxide layer increased the open-circuit voltage. Also, the minority-carrier injection efficiency of silicon-Schottky diodes were increased by a similar thin-oxide film (25,26).

This thesis investigates the d.c. current-voltage characteristics

with the oxide thickness and the surface impurity concentration as parameters. This aspect of the study has received comparatively little attention in the published literature. X-ray topography is also used to study the oxide and aluminum thickness effects on the crystal lattice.

CHAPTER II

THEORY OF TUNNELING THROUGH AN INSULATING FILM

Electrical conduction in thin insulating films has been the subject of numerous experimental investigations. A good review of the electrical conduction mechanisms has been reported by Lamb (27) and he suggested five possible separate conduction mechanisms through thin insulating films. These five possibilities are i) ionic conduction, ii) space-charge-limited flow, iii) tunneling, iv) Schottky emission and v) impurity conduction. However, the dominant current flow mechanism in a metal-insulator-semiconductor structure with insulating layers of about 10Å to 100Å is tunneling (15). A review of the derivation of the conduction current with an interfacial layer by Card (12) follows.

Using the result of Harrison (28), the expression for a one-dimensional tunneling current is:

$$J_x = \frac{4\pi q}{\hbar} \sum_{k_t} \int_o^\infty |M_{sm}|^2 \, \rho_s \rho_m \, (f_s - f_m) dE_x \qquad [2.1]$$

where M_{sm} is the matrix element for the transition from the semiconductor to the metal, ρ_s and ρ_m are the density of states at the semiconductor and metal respectively, f_s and f_m are the Fermi functions and k_t is the crystal momentum component transverse to the barrier. Gray (16) converted the sum over k_t to an integral:

$$\sum_{k_t} \rightarrow \frac{1}{(2\pi)^2} \int dk_y dk_z \longrightarrow \frac{1}{2\pi} \int k_t dk_t \longrightarrow \frac{1}{2\pi} \frac{m_t}{h^2} \int dE_t \qquad [2.2]$$

where $E_t = (\dfrac{\hbar^2 k_t^2}{2m_t})$ and m_t is the cyclotron effective mass for a mag-
netic field in the X direction. Applying the transformation Eq. [2.2]
to Eq. [2.1], the one-dimensional tunneling current becomes:

$$J_x = \frac{2m_t q}{\hbar^3} \int_0^\infty \int^{E_{max}} |M_{sm}|^2 \, \rho_s \rho_m (f_s - f_m) dE_t dE_x \qquad [2.3]$$

Assuming that tunneling through the Schottky barrier is negligible and
the current is for a forward bias, the lower limit on these integrals
can be chosen as the semiconductor conduction band at the surface.
Using the WKB (Wentzel-Kramers-Brillouin) approximation for the trans-
mission coefficient, the matrix element is expressed as:

$$|M_{sm}|^2 = (\frac{\hbar^2}{2m})^2 \frac{(k_x)_s}{L_s} \frac{(k_x)_m}{L_m} \quad \exp\left\{-2\left(\int_{X_s}^{X_m} |k_x| \, dx\right)\right\} \qquad [2.4]$$

where X_s and X_m are the classical tunneling points. The one-dimensional-
density of states factor is given by,

$$\rho_i = \frac{mL_i}{\pi \hbar^2 (k_x)_i} \qquad [2.5]$$

where k_x is the component of the momentum in the x direction, L_i is the
length of either the semiconductor or the metal. Substituting Eq. [2.5]
into Eq. [2.4] yeilds,

$$|M_{sm}|^2 = \frac{1}{\rho_s \rho_m} \frac{1}{(2\pi)^2} \quad \exp \left(-2\int_{X_s}^{X_m} |k_x| \, dx\right) \qquad [2.6]$$

A rectangular barrier of height W is assumed independent of x.
$W - E_x \simeq \psi (\text{ev})$, the distance from the conduction band edge of the semi-
conductor to that of the insulator in Fig. 2.1.

$$k_x = \left\{ \frac{2m}{h^2} \ (W - E_x) \right\}^{\frac{1}{2}} \tag{2.7}$$

The film thickness is defined as: $\delta \ (\overset{\circ}{A}) = X_m - X_s$, thus

$$\left| M_{sm} \right|^2 = \frac{1}{\rho_s \rho_m} \ \frac{1}{(2\pi)^2} \ \exp \left\{ - \frac{4\pi}{h} \ (2m\psi)^{\frac{1}{2}} \delta \right\}$$

$$= \frac{1}{\rho_s \rho_m (2\pi)^2} \ \exp \ (- 1.01 \psi^{\frac{1}{2}} \delta) \ . \tag{2.8}$$

For forward bias, $f_m \simeq 0$ and from the Boltzman's approximation for non-degenerate materials,

$$f_s \simeq \exp \left\{ - \frac{E_x + E_t - E_{fs}}{kT} \right\} \tag{2.9}$$

where E_{fs} is the energy of the semiconductor at the Fermi level, k is a Boltzman's constant and T is the absolute temperature. Eq. [2.3] becomes:

$$J_x \simeq \frac{m_t q}{2\pi^2 h^3} \int_0^\infty \int_0^\infty \exp \ (- \psi^{\frac{1}{2}} \delta) \ \exp \ (- \frac{E_x + E_t - E_{fs}}{kT}) dE_x dE_t$$

$$= \frac{4\pi m_t q}{h^3} \ \exp \ (- \psi^{\frac{1}{2}} \delta) \ \exp \ (\frac{E_{fs}}{kT}) \int_0^\infty \int_0^\infty \exp \ (- \frac{E_x}{kT}) \ \exp \ (- \frac{E_t}{kT}) \ dE_x dE_t$$

$$= \frac{4\pi m_t q}{h^3} \ (kT)^2 \ \exp \ (\frac{E_{fs}}{kT}) \ \exp \ (- \psi^{\frac{1}{2}} \delta) \tag{2.10}$$

Also:

$$E_{fs} = -q \ (V_D + \phi n) \tag{2.11}$$

Eq. [2.10] becomes:

$$J_x = \frac{4\pi m_t q}{h^3} \ (kT)^2 \ \exp \ (- \psi^{\frac{1}{2}} \delta) \ \exp \left\{ - \frac{q}{kT} \ (V_D + \phi n) \right\} \tag{2.12}$$
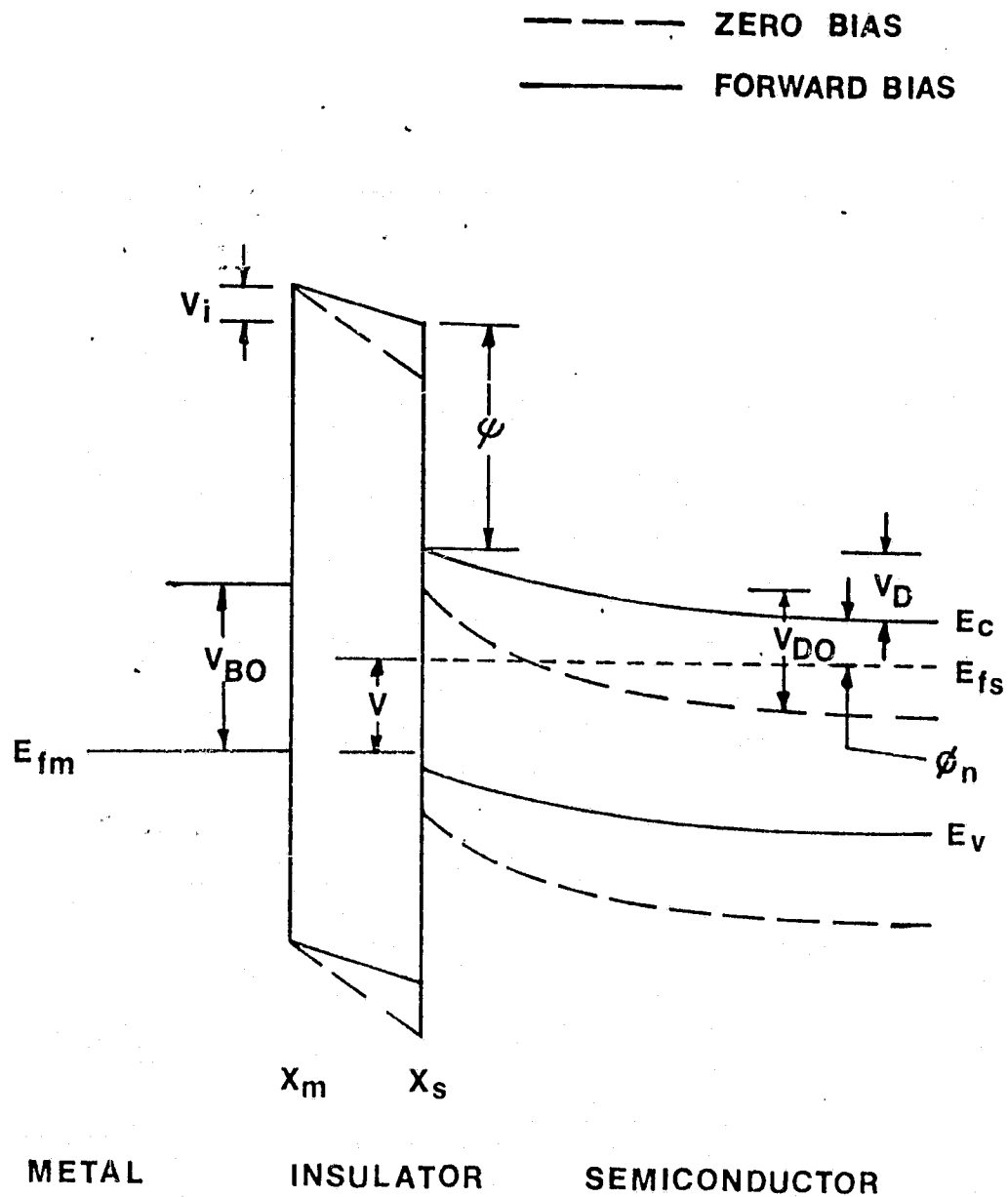
9

Fig.2.1 Energy band diagram of metal-insulator-
semiconductor contact.

The change in surface potential may be related to the applied voltage
by:

$$n = -\frac{V}{\Delta V_D}$$ [2.13]

where ΔV_D is the change in surface potential as a result of the applied
bias V.

Thus

$$V_D = V_{DO} + \Delta V_D = V_{DO} - \frac{V}{n}$$ [2.14]

where V_D is the surface potential and V_{DO} is the zero-bias value of the
surface potential.

$$V_{DO} + \phi_n = V_{BO}$$ [2.15]

where V_{BO} is the Schottky barrier height and ϕ_n is the Fermi potential
relative to the conduction band edge in the bulk in Fig. 2.1, so
Eq. [2.12] becomes:

$$J_x = AT^2 \; exp \; (- \psi^{\frac{1}{2}}\delta) \; exp \; (- \frac{qV_{BO}}{kT}) \; exp \; (\frac{qV}{nkT})$$ [2.16]

where $A = (\frac{4\pi m_t q}{h^3}) k^2$.

The assumptions of Eq. [2.16] are:

(i) The equation holds only for forward bias V>3kT since the reverse
current contribution is neglected.

(ii) The transmission coefficient of the film is constant over the
range of bias.

(iii) The current is dominated by the majority carriers.

(iv) Effects of image-force lowering of the semiconductor barrier are
ignored.

(v) The tunneling through the semiconductor depletion region is ignored.

CHAPTER III

EXPERIMENTAL PROCEDURE

This experiment has two major variable parameters which are the surface impurity concentration, both phosphorous and boron, and the thickness of the interfacial oxide layer. The $n^+ - n$ and $p^+ - p$ structures were chosen to make the process simple.

Primary Experiment

Interfacial Oxide Layer

Silicon has a strong affinity for oxygen and Raider (29) reported that the equilibrium oxide thickness in air at room temperature is less than 14Å. To vary the thickness of the oxide layer a thermal oxidation is required and a 900°C - dry oxygen oxidation was chosen. N-type silicon wafers with $\langle 111 \rangle$ orientation, 1.5 in. dia., 10 mils thick and 2Ω-cm resistivity were used. After initial cleaning they were exposed to a temperature of 900°C under a dry oxygen flow-rate of 2.4 l/min.. To obtain different oxide thicknesses the wafers were oxidized for varying time periods. In order to accurately determine the thickness of the oxide for each wafer, an optical method was used. The oxides were partially etched using a photolithographic technique. Aluminum was evaporated on the wafers, making the silicon surfaces highly reflective, and a Varian Å - Scope Interferometer was used. The microscopic view through the interferometer, simulated in Fig. 3.1, shows the width between two fringe lines and is equal to one half of the sodium wavelength (2946Å). The oxide thickness was determined as the geometric ratio comparing the width of the two fringe lines, L, to the step width, x, such that:
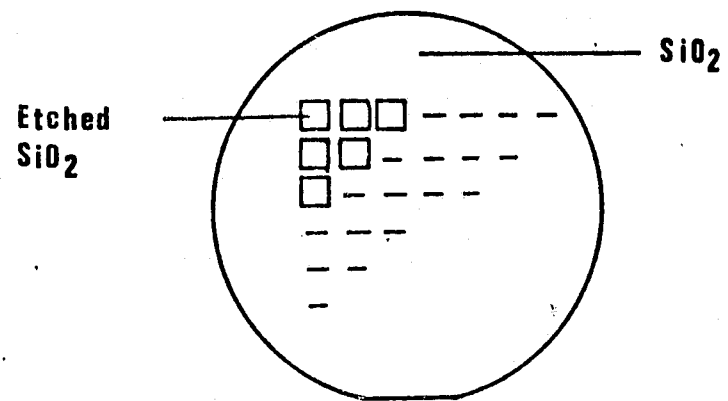
Oxide Etched Pattern
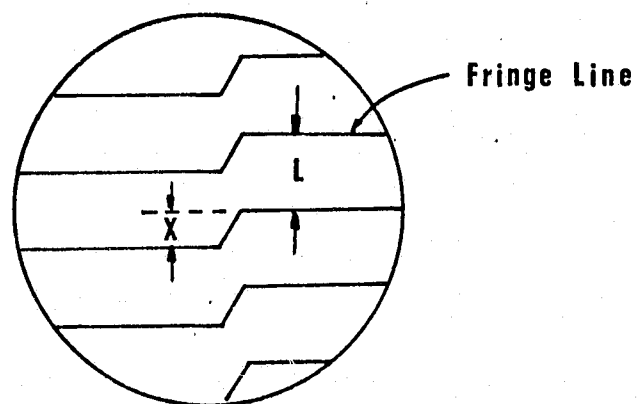
Microscopic View
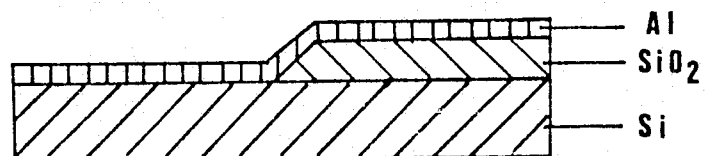
Cross-section

Fig. 3.1 Oxide thickness measurement.

thickness of oxide $= 2946x \frac{X}{L}$ (Å). The relationship between the grown oxide thickness and the required oxidation times are shown in Fig. 3.2 and Fig. 3.3.

Surface Impurity Concentration

C-V Technique. Common techniques which employ Irvin (30) curves, knowing the surface sheet resistance and the junction depth, cannot be used to determine the surface impurity concentration because of the n^+-n and p^+-p structures. Zaininger (31) has utilized the C-V technique to determine the impurity concentration. For this study his minimum MOS capacitance method was modified as described below.

The maximum depletion layer depth is given by:

$$\lambda_d = \left\{ \frac{2\epsilon_s}{qN} (1.11 - 2\Delta) \right\}^{\frac{1}{2}} \tag{3.1}$$

where

ϵ_s = dielectric constant of silicon

Δ = energy difference between the Fermi level and the valence (or conduction band)

N = impurity concentration in the silicon

q = magnitude of an electron charge

From Eq. [3.1] N can be expressed by:

$$N = \frac{2\epsilon_s (1.11 - 2\Delta)}{q \lambda_d^2} \tag{3.2}$$

The minimum space-charge capacitance per unit area is given by:

$$C_{sc}(min) = \frac{\epsilon_s}{\lambda_d} \tag{3.3}$$

Combining Eq. [3.2] and Eq. [3.3], one obtains

$$N = \frac{2C_{sc}^2 (min) (1.11 - 2\Delta)}{q\epsilon_s} \tag{3.4}$$
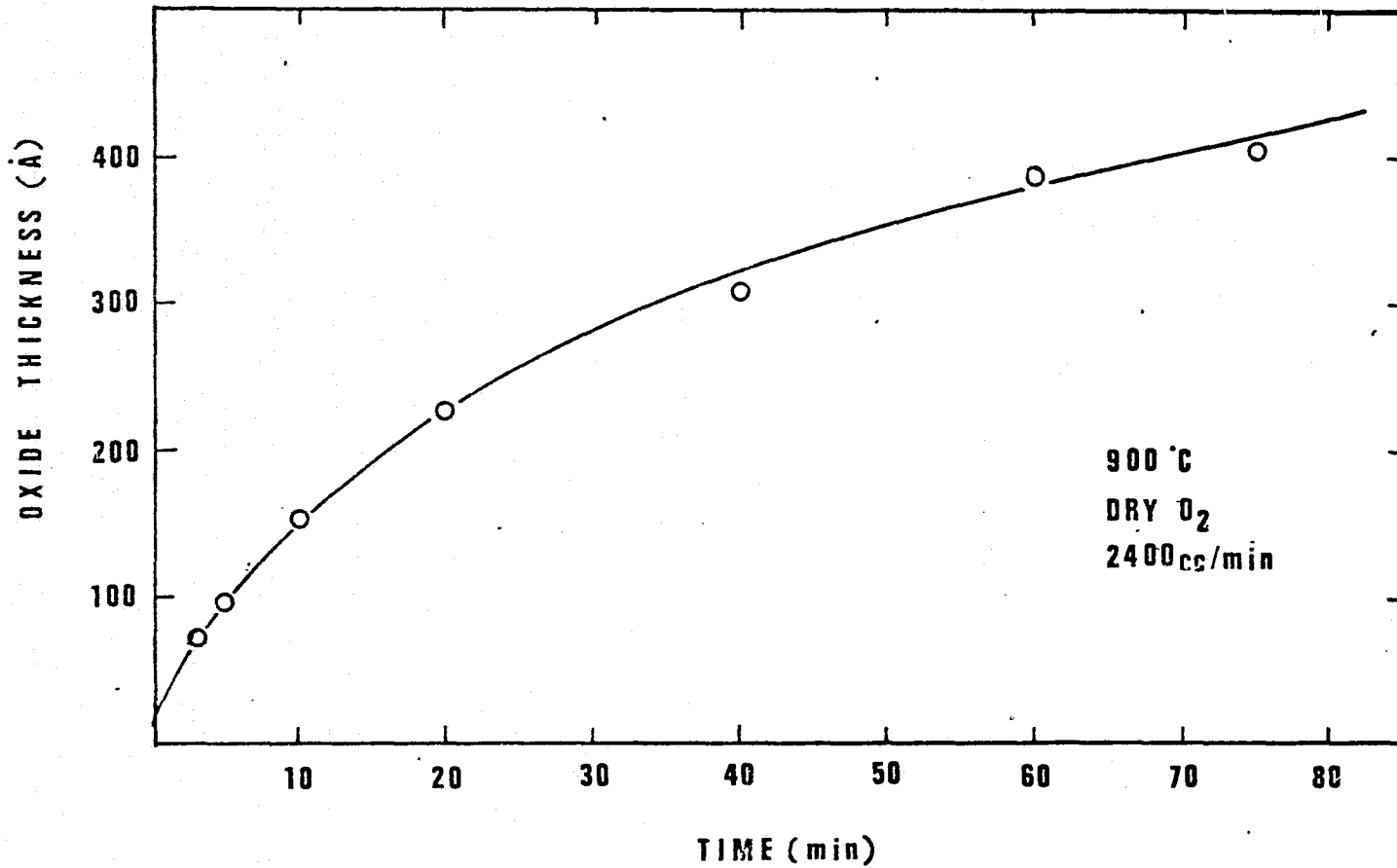
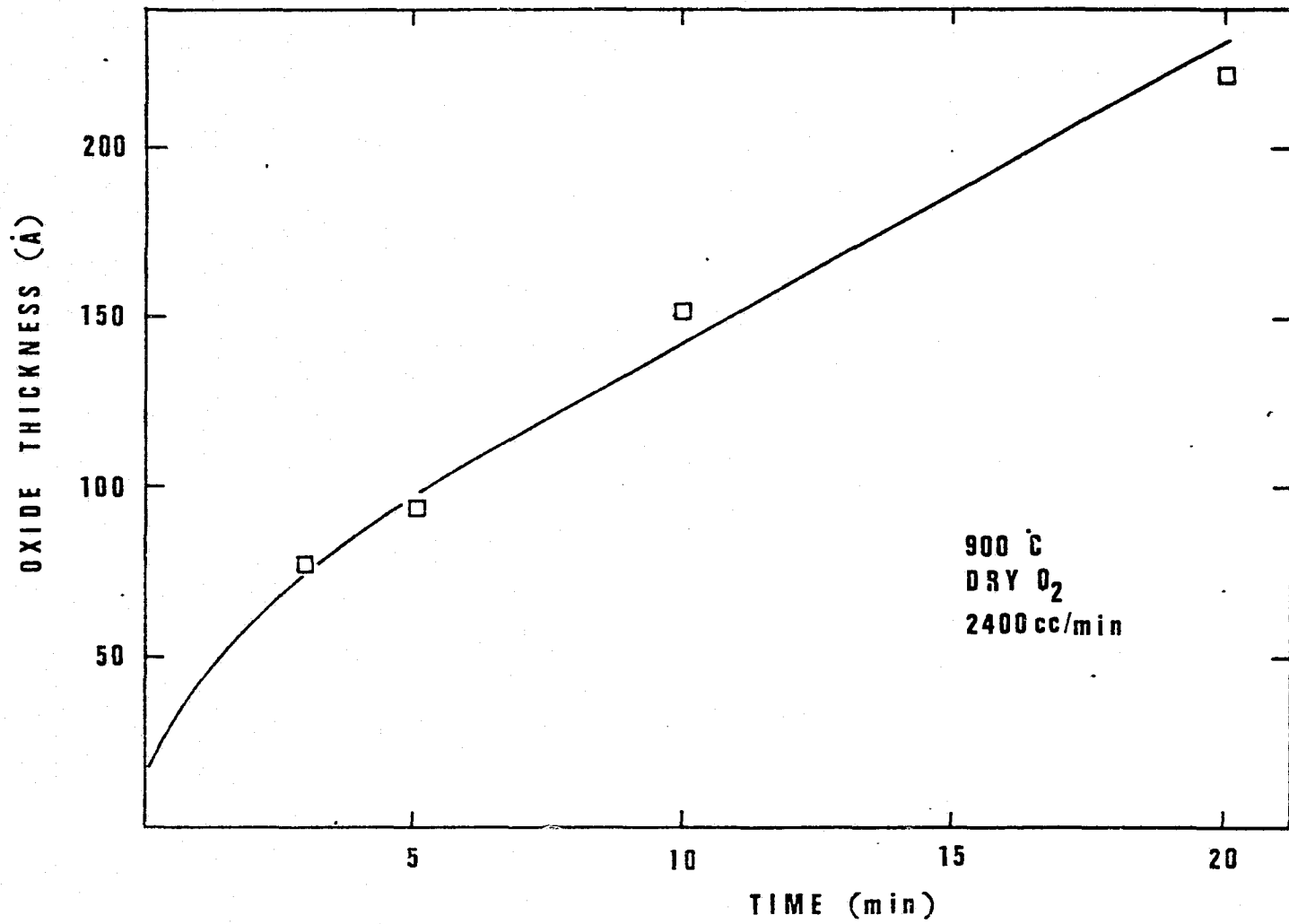Fig. 3.2 Growth of oxide film (~400Å) on silicon.

Fig. 3.3 Growth of oxide film (~200Å) on silicon.

The total MOS capacitance is a series combination of the oxide capacitance and the space-charge capacitance of the silicon which is shown in Fig. 3.4. The total capacitance therefore is:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}}$$

$$C = \frac{C_{ox}C_{sc}}{C_{ox} + C_{sc}} \qquad [3.5]$$

where

C_{ox} = capacitance of the oxide

C_{sc} = capacitance of space-charge in the silicon

C = total MOS capacitance

At the accumulation region

$$C = C_{ox}$$

at the depletion region C_{sc} (min) $\ll C_{ox}$

thus

$$C(min) \approx C_{sc}(min)$$

The capacitance of the space-charge in silicon is given by:

$$C_{sc} = \frac{C_{ox}}{\frac{C_{ox}}{C} - 1}$$

$$C_{sc}(min) = \frac{C_{ox}}{\frac{C_{ox}}{C_{min}} - 1} \qquad [3.6]$$

where

$C_{sc}(min)$ = minimum capacitance of the space-charge in the silicon

C_{min} = minimum total MOS capacitance

Substituting Eq. [3.6] into Eq. [3.4], one obtains

$$N = \frac{2(1.11-2\Delta)}{q\epsilon_s} \left(\frac{C_{ox}}{\frac{C_{ox}}{C_{min}} - 1} \right)^2 \qquad [3.7]$$
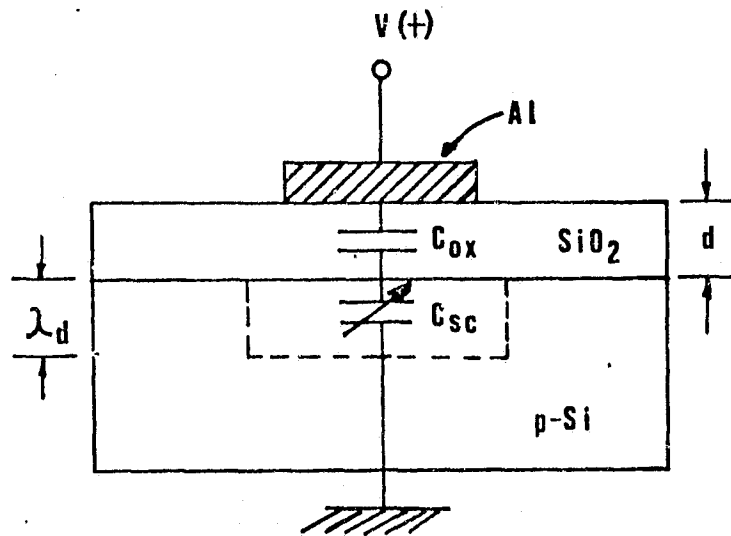
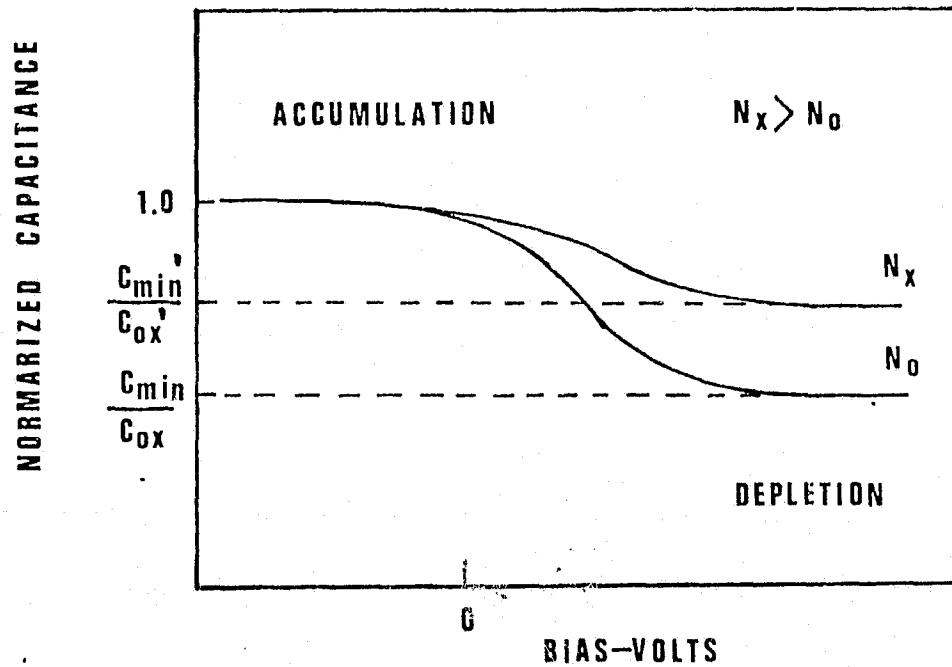17

Fig. 3.4 MOS capacitance structure.

Fig. 3.5 Capacitance-voltage curves on MOS.

$\dfrac{C_{ox}}{C_{min}}$ can be obtained from the C-V curves in Fig. 3.5. To understand how this technique is applied, consider a uniformly doped silicon wafer whose impurity concentration (N_o) can be measured by the four point probe and whose C-V curve can be plotted. Now consider another silicon wafer whose impurity concentration (N_x) is unknown and must be determined. Plot another C-V curve for the second wafer and compare it with the first C-V curve. The unknown impurity concentration N_x can be obtained in the following manner:

Using Eq. [3.7]

$$N_o = \frac{2(1.11 - 2\Delta)}{q \epsilon s} \left(\frac{C_{ox}}{\dfrac{C_{ox}}{C_{min}} - 1} \right)^2 \tag{3.8}$$

$$N_x = \frac{2(1.11 - 2\Delta')}{q \epsilon s} \left(\frac{C_{ox}'}{\dfrac{C_{ox}'}{C_{min}'} - 1} \right)^2 \tag{3.9}$$

where

N_o = known impurity concentration

N_x = unknown impurity concentration

Δ', C_{ox}', C_{min}' = Δ, C_{ox} C_{min} respectively

for N_x

Providing that the thickness of the oxide for both wafers is equal ($C_{ox} = C_{ox}'$), $\dfrac{N_x}{N_o}$ is given by:

$$\frac{N_x}{N_o} = \frac{(1.11 - 2\Delta')}{(1.11 - 2\Delta)} \frac{\left(\dfrac{C_{ox}}{C_{min}} - 1\right)^2}{\left(\dfrac{C_{ox}'}{C_{min}'} - 1\right)^2} \tag{3.10}$$

$\dfrac{C_{ox}}{C_{min}}$ and $\dfrac{C_{ox}'}{C_{min}'}$, can be measured from the C-V curves but $\dfrac{1.11 - 2\Delta'}{1.11 - 2\Delta}$ will vary slightly depending upon the impurity concentration.

$1.11 - 2\Delta$ also can be expressed as:

$$1.11 - 2\Delta = E_g - 2\,(E_c - E_f)$$
$$= 2\,(E_f - E_i) \qquad\qquad [3.11]$$

where

E_g = energy gap in the silicon (1.11ev)

E_f = energy at the Fermi level

E_i = energy at the intrinsic Fermi level

E_c = energy at the conduction band edge

Eq. [3.10] becomes:

$$N_x = N_o \; \frac{(E_f' - E_i)}{(E_f - E_i)} \left(\frac{\frac{C_{ox}}{C_{min}} - 1}{\frac{C_{ox}'}{C_{min}'} - 1} \right)^2 \qquad [3.12]$$

where

E_f' = unknown energy at the Fermi level

let $\dfrac{E_f' - E_i}{E_f - E_i} = \alpha$

At $300°K$, if 10^{16} atoms/cm^3 for N_o is chosen, α will vary from 1.0 to 1.68 for values of N_o in the range of $10^{16} \sim 10^{20}$ atoms/cm^3. Assuming $\alpha \simeq 1.0$, N_x is given by:

$$N_x \simeq 10^{16} \left(\frac{\frac{C_{ox}}{C_{min}} - 1}{\frac{C_{ox}'}{C_{min}'} - 1} \right)^2 \qquad [3.13]$$

Apparatus. Zaininger has designed an automatic display (32)
which gives rapid measurement of capacitance-versus-bias characteristics
of metal-insulator-semiconductor structures at 1MH$_z$ over a wide range
of biases and sweep speeds. A schematic of the basic measuring circuit
is shown in Fig. 3.6. If a constant a.c. voltage is applied across
the MOS (C_x) diode, then the current is essentially determined by the
reactance of the diode. The voltage across the resistor R_m (which must
be small with respect to the diode reactance) can be used as a measure
of the capacitance. In particular, if the conditions

$$R_m \ll \frac{1}{\omega C_x} \ll R_b$$

.and

$$C_b \gg C_x$$

are satisfied, the magnitude of the a.c. voltage appearing across R_m is

$$|V_m| = |V| \omega R_m C_x$$

Here, C_x is the equivalent parallel capacitance of the MOS diode, C_b
is a blocking capacitor, and ω is the frequency of operation. $|V|$ is
the magnitude of the a.c. signal from the oscillator which is adjusted
to be constant. $|V_m|$ is proportional to C_x. Detailed circuit
diagrams of the automatic display are shown in Fig. 3.7. Also the
entire schematic of the measuring apparatus which was used in this
experiment is shown in Fig. 3.8.

Measurement. In order to obtain the relationship between the
surface impurity concentration and the drive-in time, the drive-in
times were varied after a phosphorous or boron deposition. The
silicon wafers used had ⟨111⟩ orientation, 1.5 in. diameter, 10 mils
thick and 1∼2 Ω-cm resistivity. Prior to diffusion the wafers were

C_x = SAMPLE
C_b = 0.01 μF
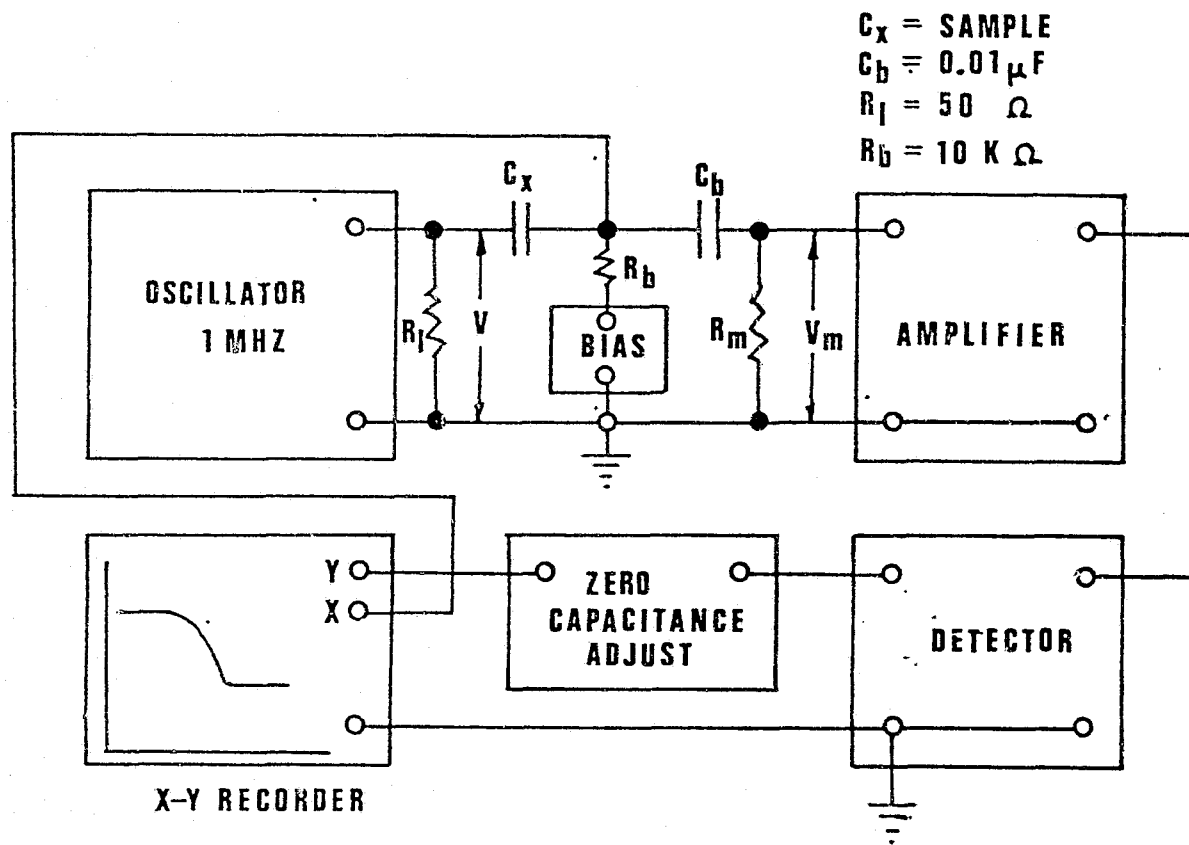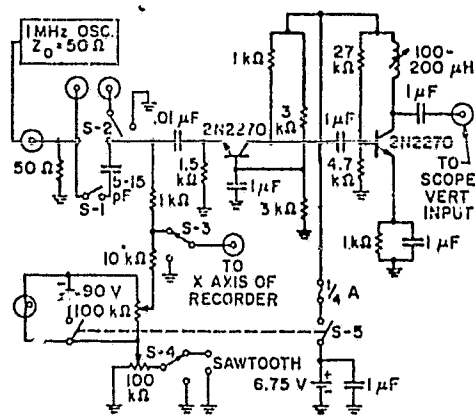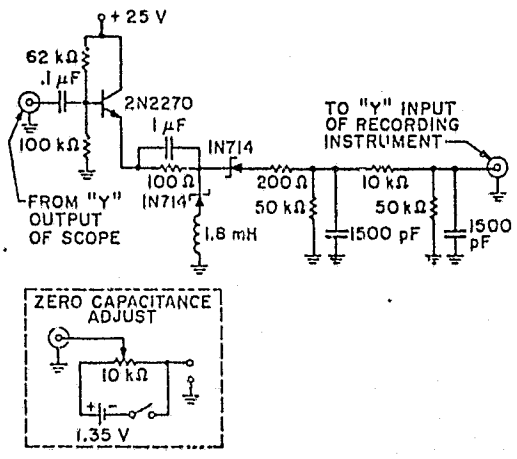R_l = 50 Ω
R_b = 10 K Ω

Fig. 3.6 Simplified schematic of C-V measuring apparatus.

(a)

(b)

Fig. 3.7 Detailed schematic of C-V measuring apparatus.
(a) Measuring circuit with bias supply and first two
stages of amplification. (b) Last stage of amplification,
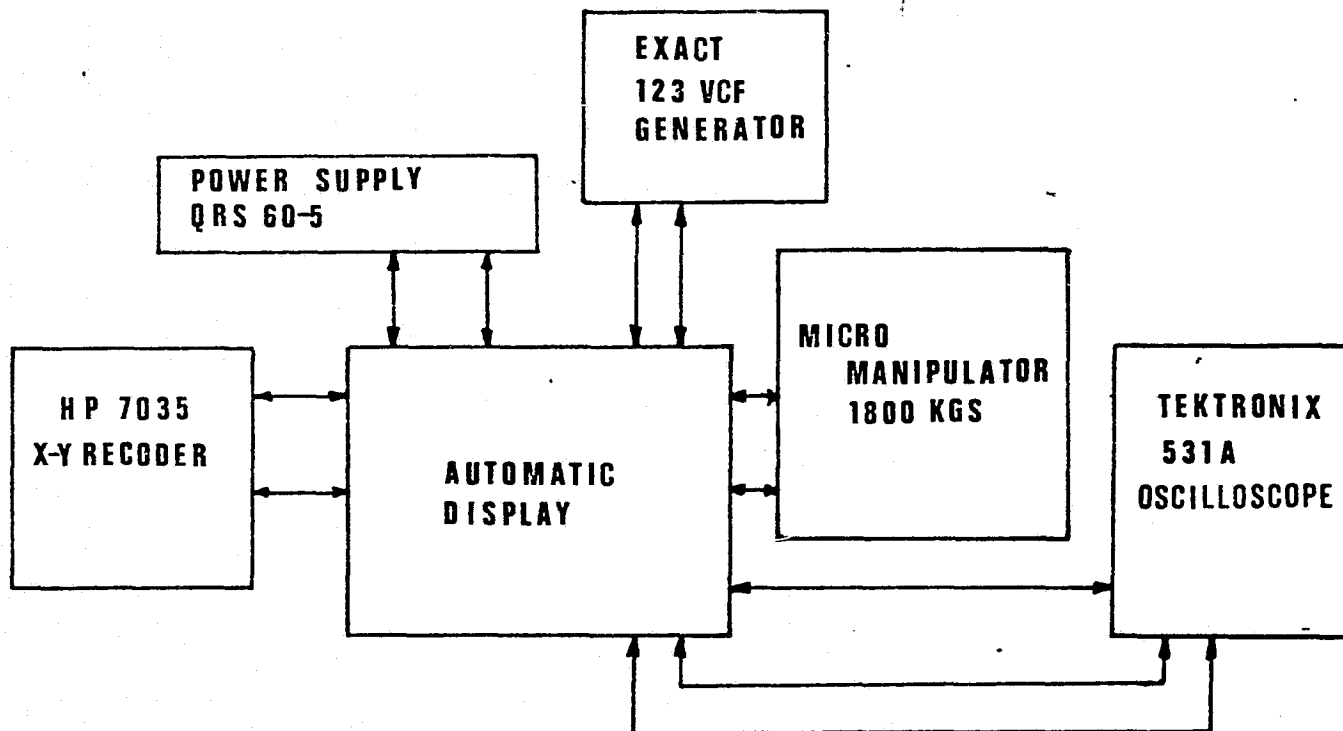detection, and zero-capacitance adjust circuit. (Ref.32)

Fig. 3.8   Block diagram of C-V measurement.

chemically cleaned by standard techniques. Liquid deposition sources, BBr_3 and $POCl_3$, were used at $900°C$ for p and n-type wafers, respectively. The n-type deposition times were 70 sec. and 90 sec. and the p-types were 90 sec. and 28 min.. To provide the different surface impurity concentration the drive-in times were varied between 5 min. and 120 min. at $1100°C$ for each deposition time used. The oxides were grown at $1100°C$ using a dry O_2 flow and the oxidation time, 60 sec., was chosen to provide the maximum deflection in the C-V curves. The oxide thickness was about $140Å$. After oxidation the wafers were placed in a vacuum ($5x10^{-6}$ torr.). Following the aluminum evaporation the C-V curves were plotted for each silicon wafer. The drive-in time is shown in Fig. 3.9 and Fig. 3.10.

Sample Preparation and Measurement

After chemically cleaning, an oxide was grown on the n-type silicon wafers which were 1.5 in. in diameter, ⟨111⟩ orientation and 12 mils thick. Following the oxidation the backside oxide was removed with a 10% HF solution. Phosphorus was diffused into the silicon wafers to provide a highly doped surface on the backside. Next, the oxide on the frontside was removed and another phosphorus diffusion was performed to provide various frontside surface impurity concentrations (10^{20}, 10^{19}, 10^{18}, and 10^{17} atoms/cm^3) according to Fig. 3.9 and Fig. 3.10 which were previously obtained. To vary the interfacial oxide layers' thickness between $15Å$ and $100Å$, the oxides were grown at $900°C$ in a dry oxygen flow. Fig. 3.3 was used for each wafer to determine the oxide thickness. Following oxidation 24 mils diameter aluminum dots were evaporated in a medium vacuum ($5x10^{-6}$ torr.) on the frontside of the silicon wafers.
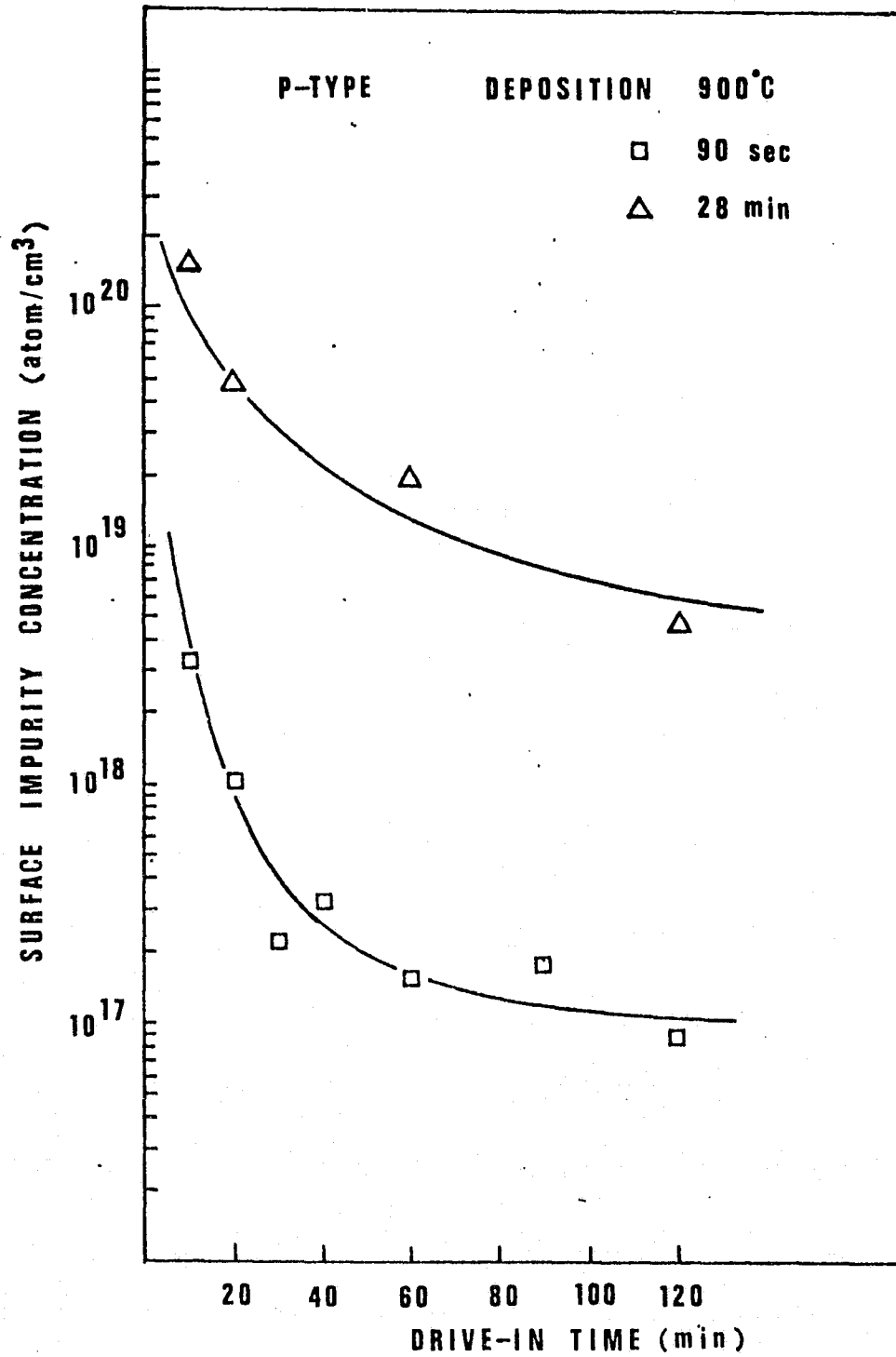
Fig. 3.9 Surface impurity concentration vs drive-in time at 1100°C for P-type silicon.
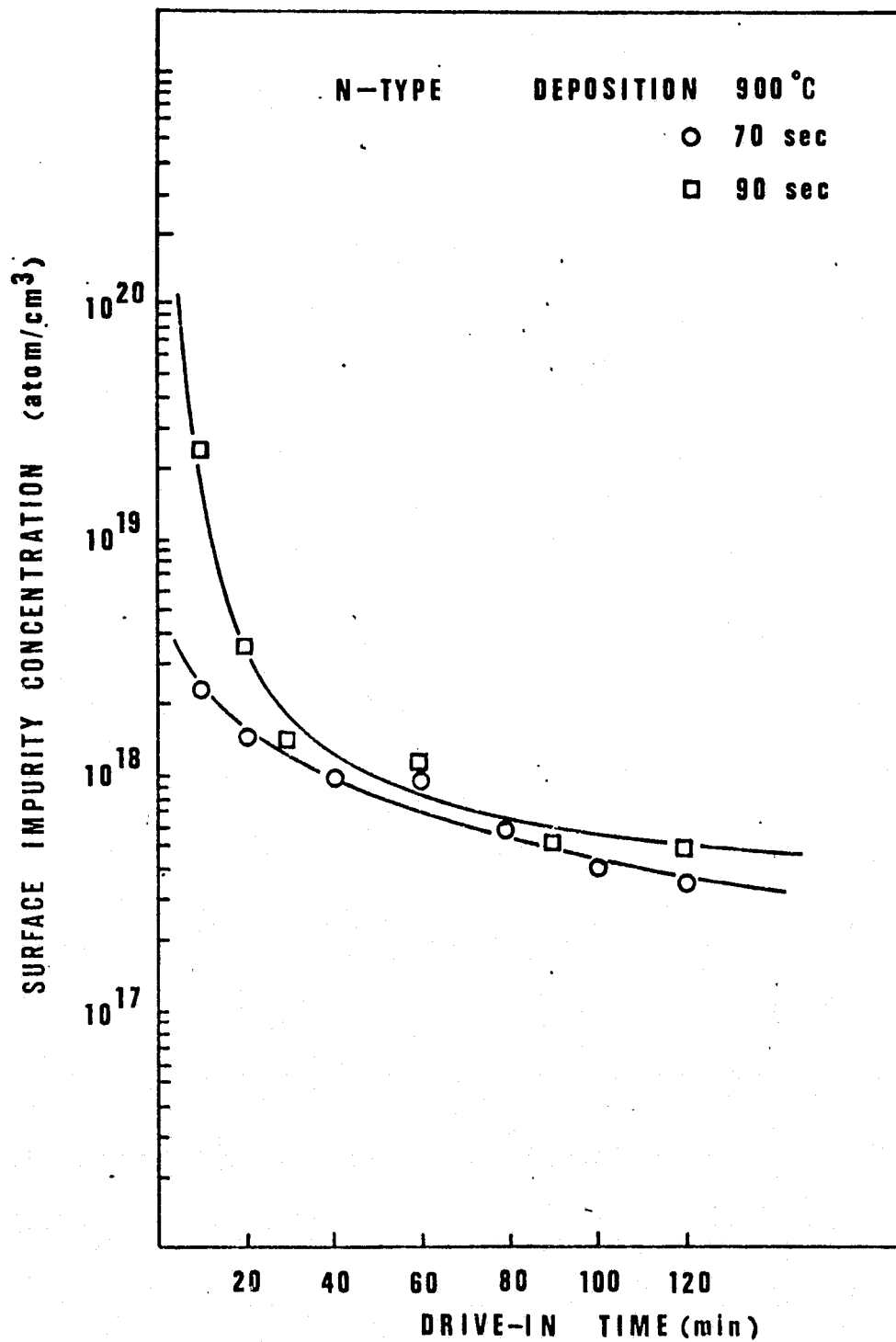
Fig. 3.10 Surface impurity concentration vs drive-in time at 1100°C for N-type silicon.

Another aluminum evaporation was performed on the backside of the silicon wafers to make good contacts. Furthermore, to make contacts ohmic the silicon wafers were annealed for 15 min. at 490°C in a nitrogen ambient. Similar processes were performed to provide specific surface impurity concentrations and the interfacial oxide layers' thickness for p-type silicon wafers. The schematic of Al-SiO$_2$-Si sample structure is shown in Fig. 3.11.

The current through each sample and the voltage across it is measured using the simple circuit shown in Fig. 3.12.

X-ray Topography

The samples were prepared by growing an oxide on the n and p-type silicon wafers with $\langle 111 \rangle$ and $\langle 100 \rangle$ orientation. These four silicon wafers having a 2 in. diameter, 18 mils thick and 10^{15} atoms/cm^3 impurity concentration were used. The thickness of the oxides was 100Å, which was obtained using Fig. 3.3 and one half of the silicon wafers on the left hand side were etched to a thickness of the native oxide. Following the oxide etch 24 mils diameter aluminum dots 0.3μ thick were evaporated in a medium vaccum (5 x 10^{-6} torr.). The aluminum dots on the bottom half of the silicon wafers were etched to 0.15μ thick. Consequently, each wafer was divided into four regions having different aluminum and oxide thickness combinations. A schematic of the sample is shown in Fig. 3.13.

X-ray topographs were taken using a Rigaku X-ray generator with a high speed X-ray topographic camera (33) shown in Fig. 3.14 and Fig. 3.15. Kodak Dental Film Type DF46 (2$\frac{1}{4}$ x 3 in.) was used with a 30 sec. exposure.
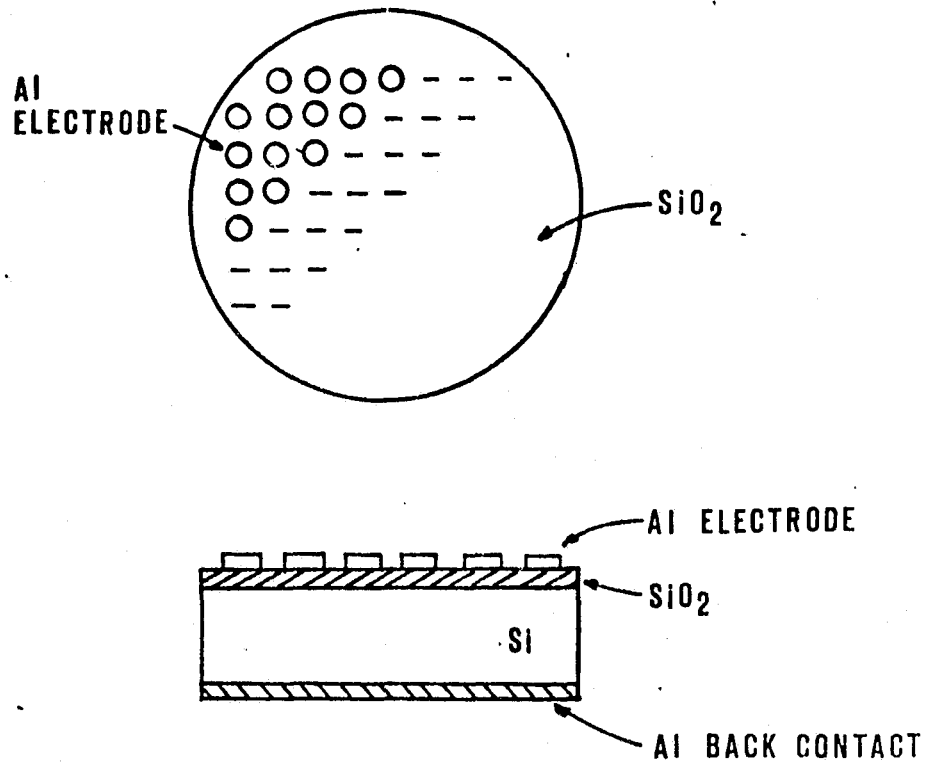
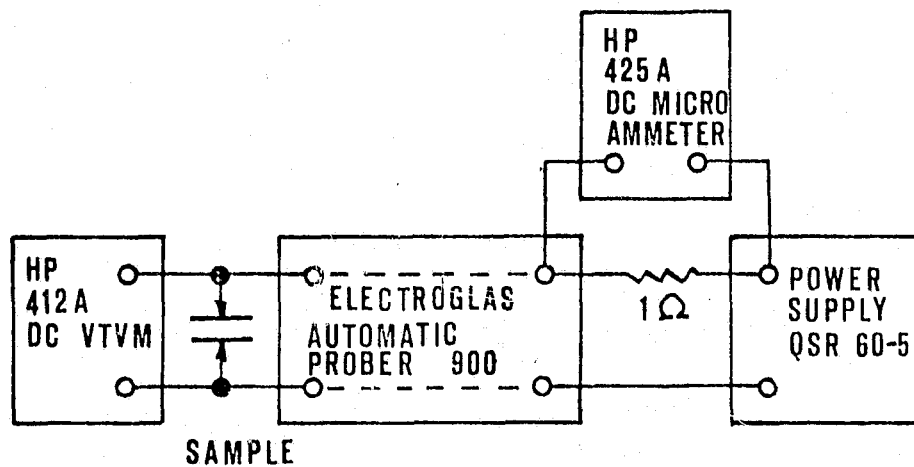Fig. 3.11   Schematic of Al-SiO$_2$-Si sample structure.

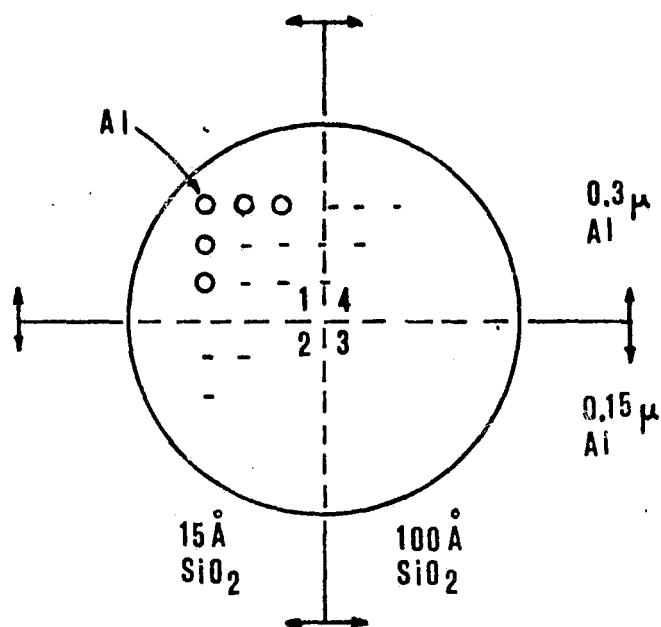Fig. 3.12   Block diagram of current-voltage measurement.
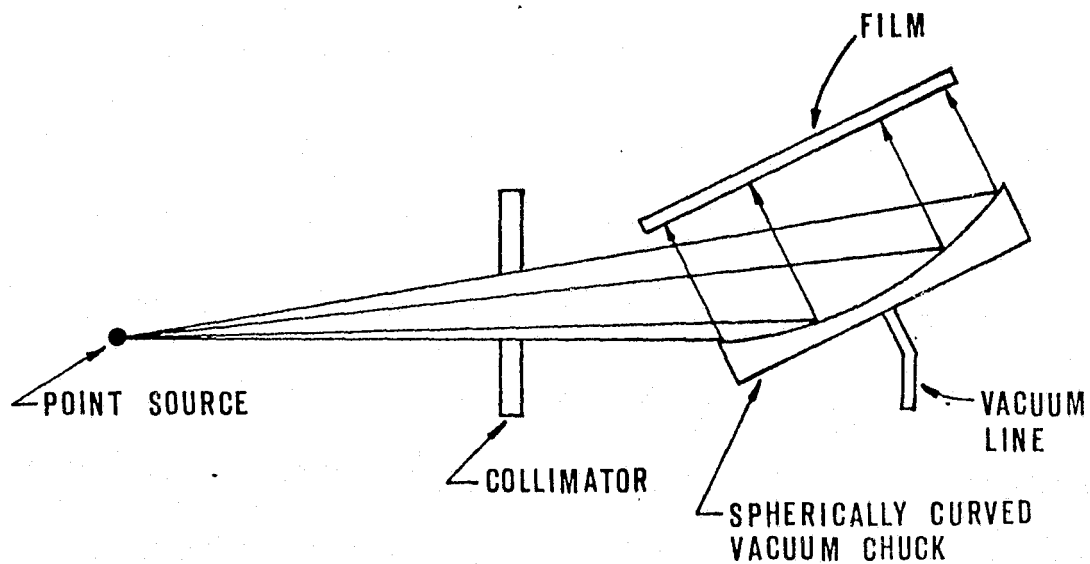
Fig. 3.13   Schematic of sample for X-ray topography.
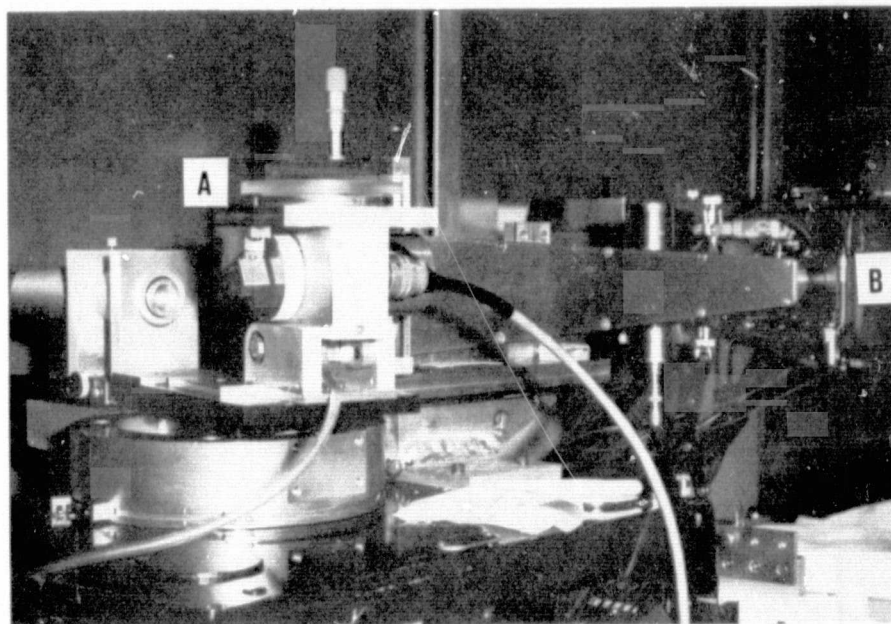

Fig. 3.14   Schematic of X-ray camera. (Ref.33)

Fig. 3.15 High speed X-ray topographic camera. (A):
vacuum chuck, (B): point source.

CHAPTER I.V

RESULTS AND DISCUSSION

Electrical Characteristics

For both n and p-type silicon wafers, the current-voltage characteristics were measured varying the surface impurity concentration between 10^{16} atoms/cm^3 and 10^{20} atoms/cm^3 and also varying the interfacial oxide thickness between the native oxide (15Å) and 100Å. A nonlinearity of the current-voltage characteristics can be easily seen by plotting the static conductance-voltage graphs. The horizontal line relationship between the conductance and voltage demonstrates .the linear ohmic current-voltage relationship of the contact. The conductance-voltage characteristics having different surface impurity concentrations are shown in Fig. 4.1 - 4.5 and in Fig. 4.7 - 4.11 for p and n-type silicon, respectively. Fig. 4.6 and Fig. 4.12 shows the resistance-oxide thickness characteristics. Because of the complex mechanism and uncertainty of the parameters, a qualitative analysis instead of a quantitative analysis is discussed here. Significant behaviors are basically described using the energy band diagram based on Fig. 4.13 (34,35). Forward bias is defined as negative on the aluminum top contact for p-type silicon and positive for n-type silicon.

Considering p-type silicon wafers having various oxide thickness and surface impurity concentrations, Fig. 4.1 - 4.5 show that both the forward and reverse current-voltage characteristics are ohmic at bias voltages below 0.1v. Exceeding a bias of 0.1v, the forward current-voltage characteristics become nonlinear; the conductance increases.
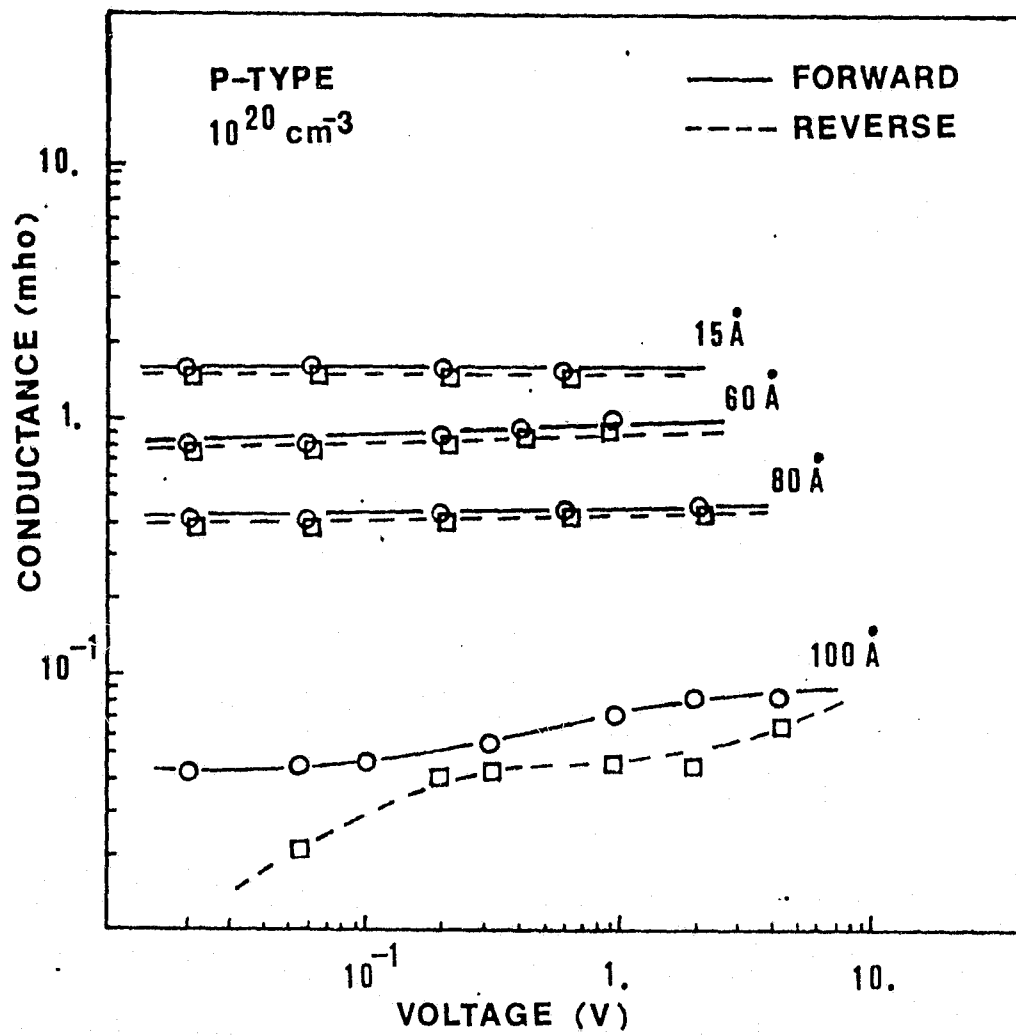
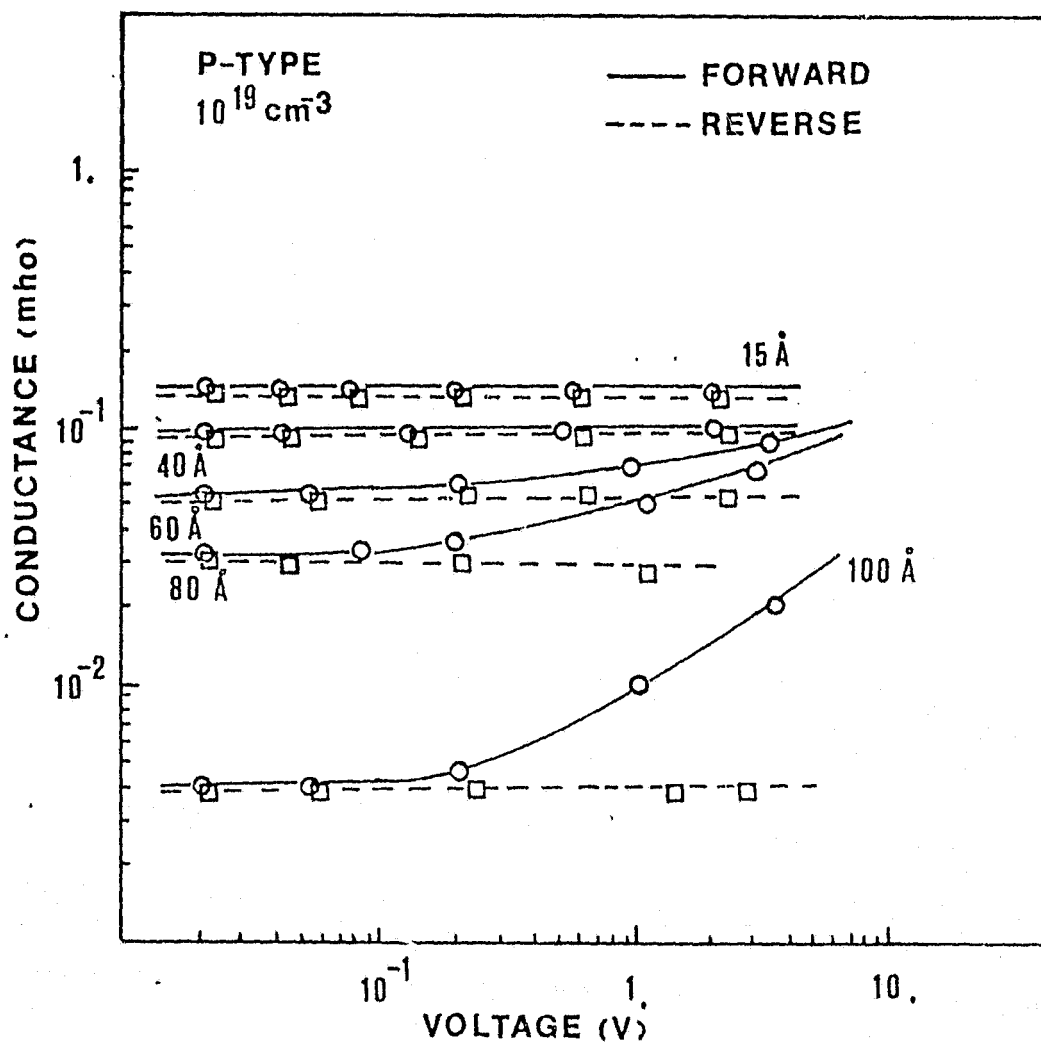Fig. 4.1 Conductance vs voltage at surface impurity concentration, 10^{20} atoms/cm^3 for p-type silicon.

Fig. 4.2 Conductance vs voltage at surface impurity concentration, 10^{19}atoms/cm^3 for p-type silicon.

Fig. 4.3 Conductance vs voltage at surface impurity concentration, 10^{18} atoms/cm^3 for p-type silicon.
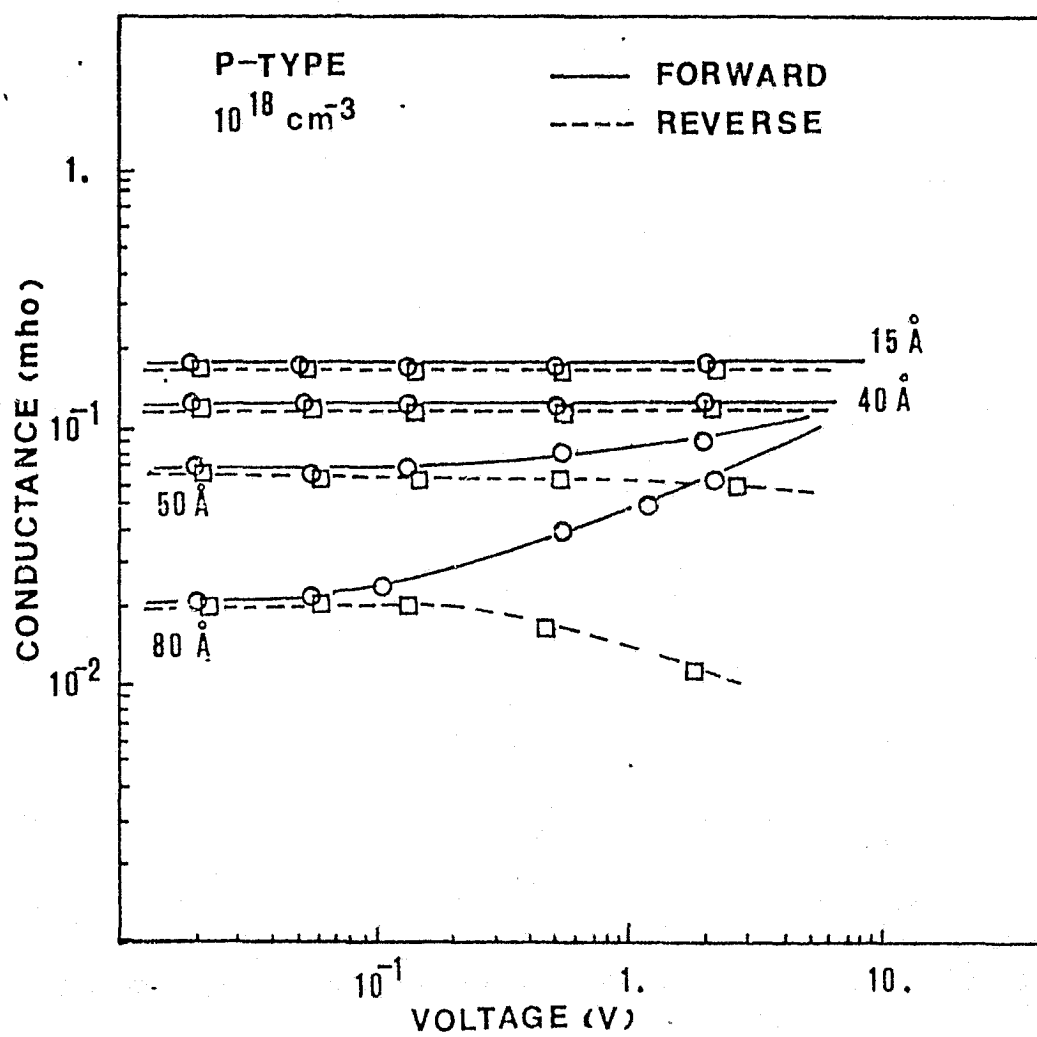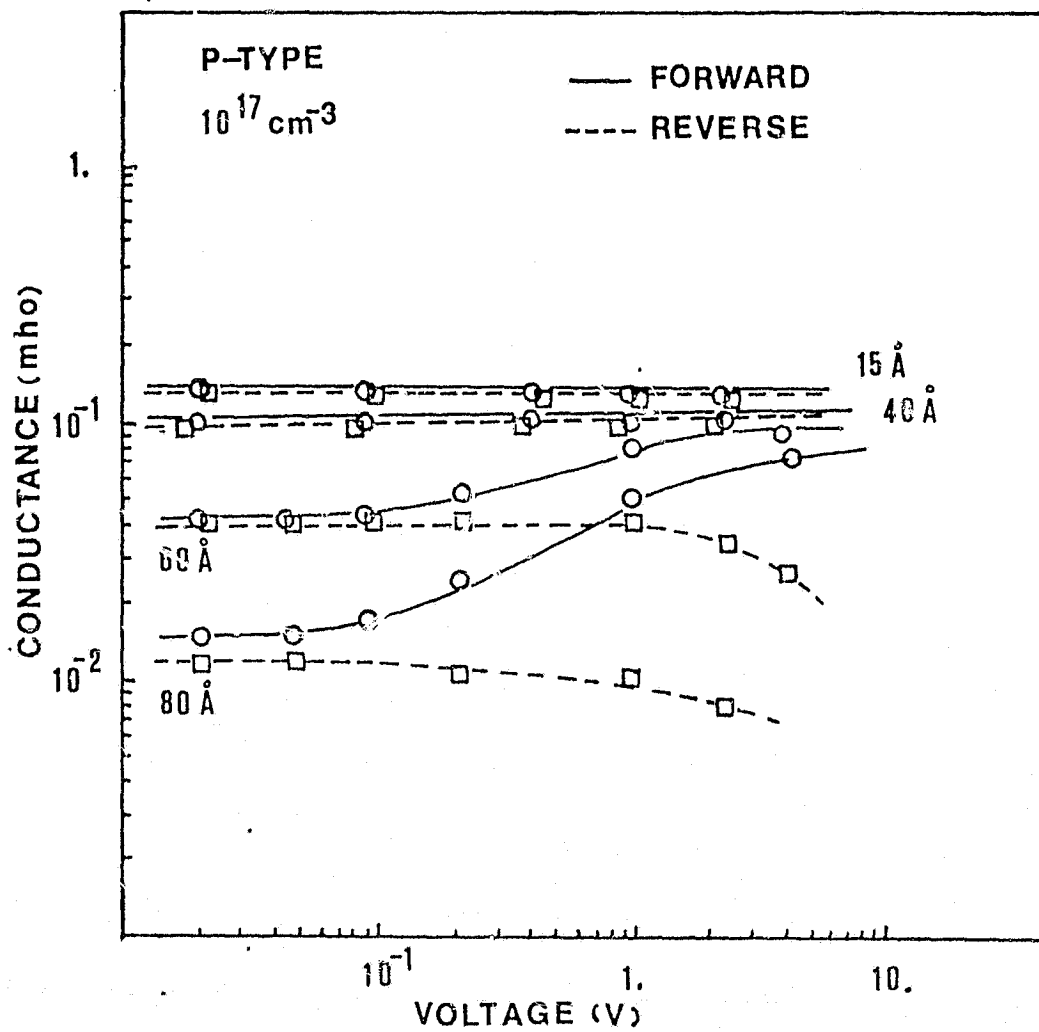
35

Fig. 4.4 Conductance vs voltage at surface impurity concentration, 10^{17}atoms/cm^3 for p-type silicon.
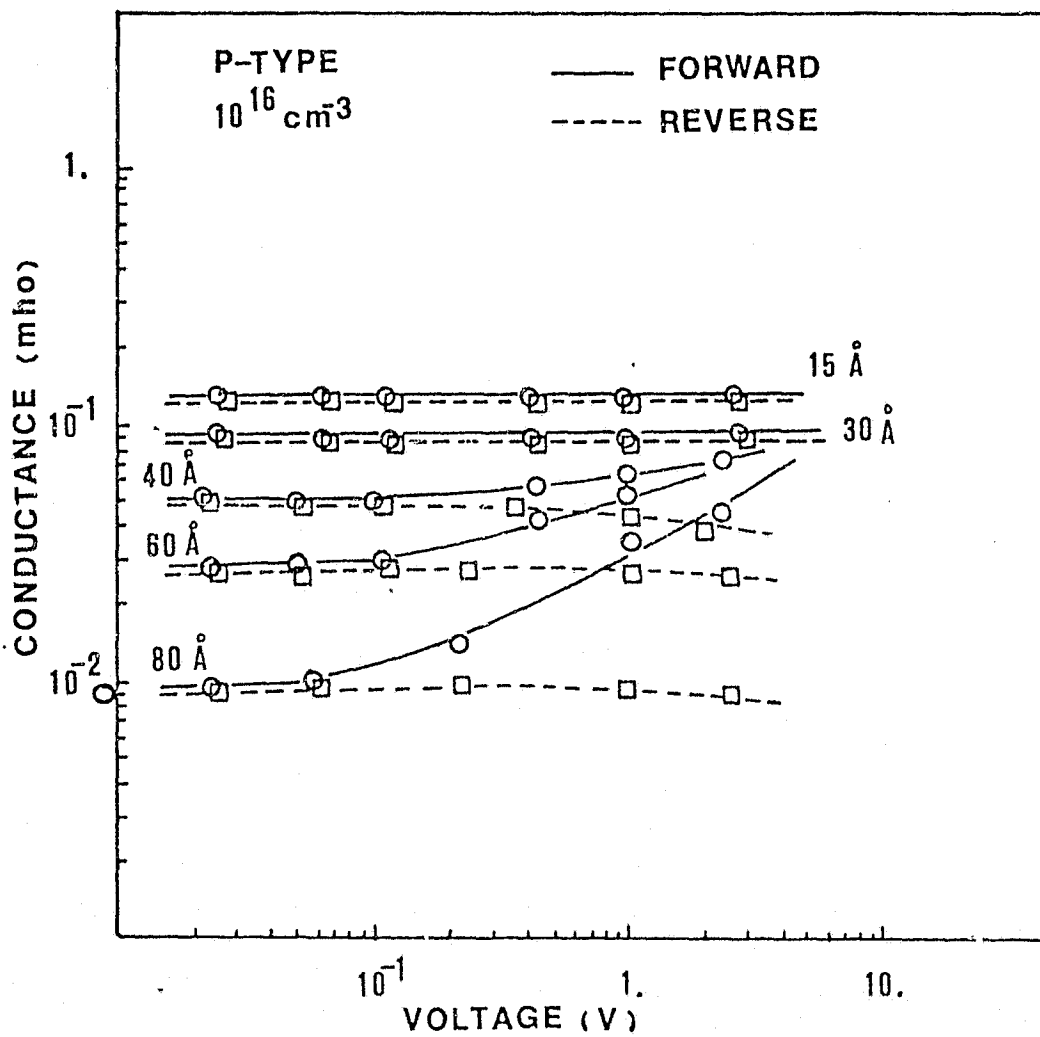
Fig. 4.5 Conductance vs voltage at surface impurity concentration, 10^{16} atoms/cm^3 for p-type silicon.

Fig. 4.6 Resistance vs oxide thickness with various surface impurity concentrations for P-type silicon.

Fig. 4.7 Conductance vs voltage at surface impurity
concentration, 10^{20}atoms/cm^3 for n-type silicon.

Fig. 4.8 Conductance vs voltage at surface impurity concentration, 10^{19}atoms/cm^3 for n-type silicon.

Fig. 4.9 Conductance vs voltage at surface impurity concentration, 10^{18}atoms/cm^3 for n-type silicon.

Fig. 4.10 Conductance vs voltage at surface impurity concentration, 10^{17}atoms/cm^3 for n-type silicon.

Fig. 4.11 Conductance vs voltage at surface impurity
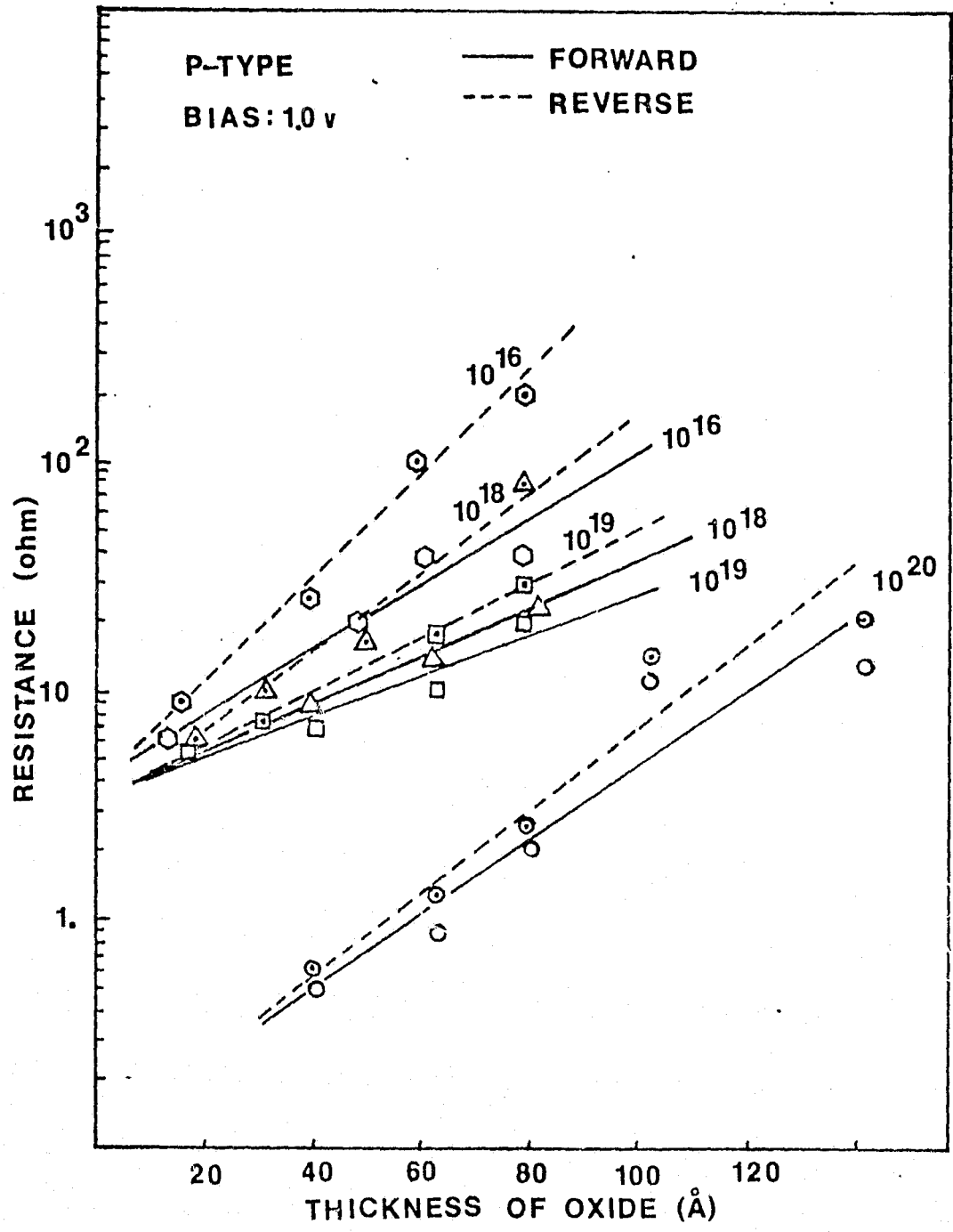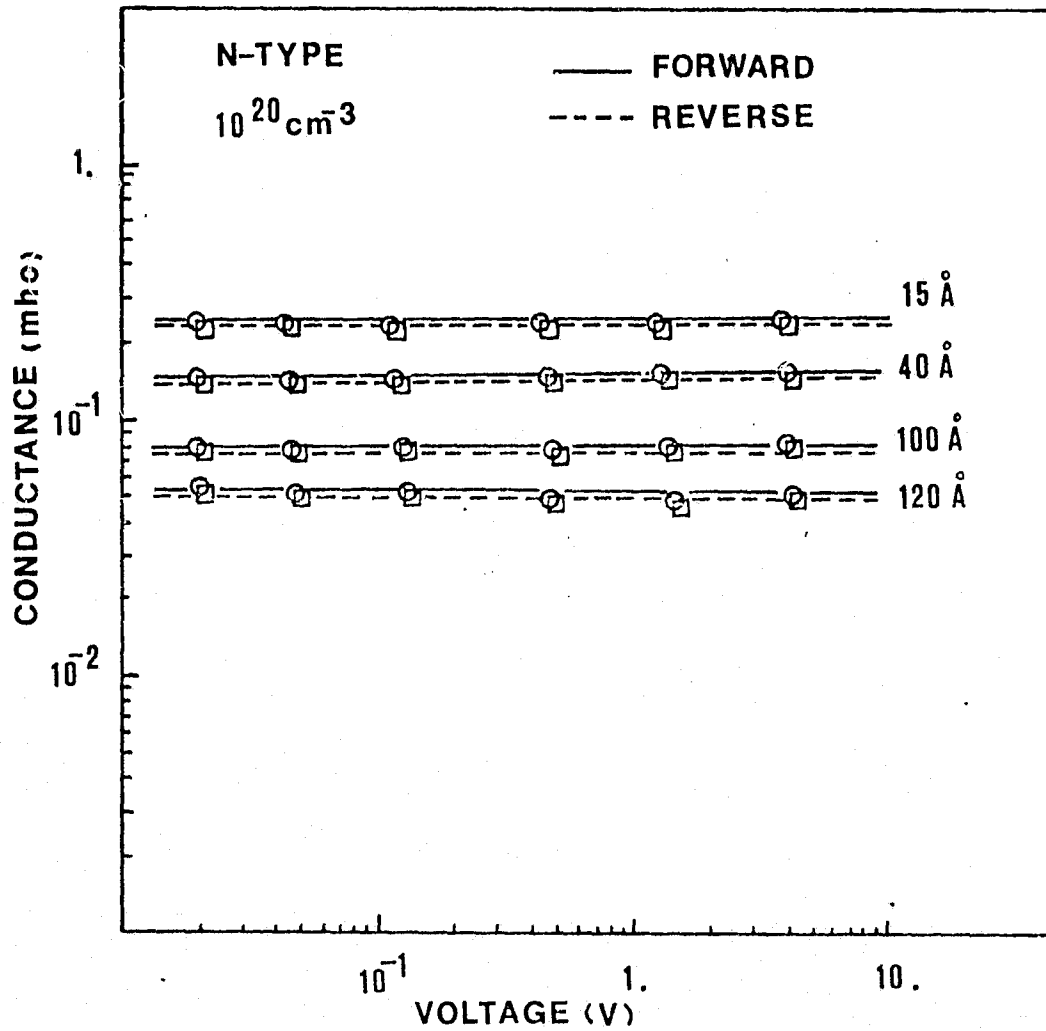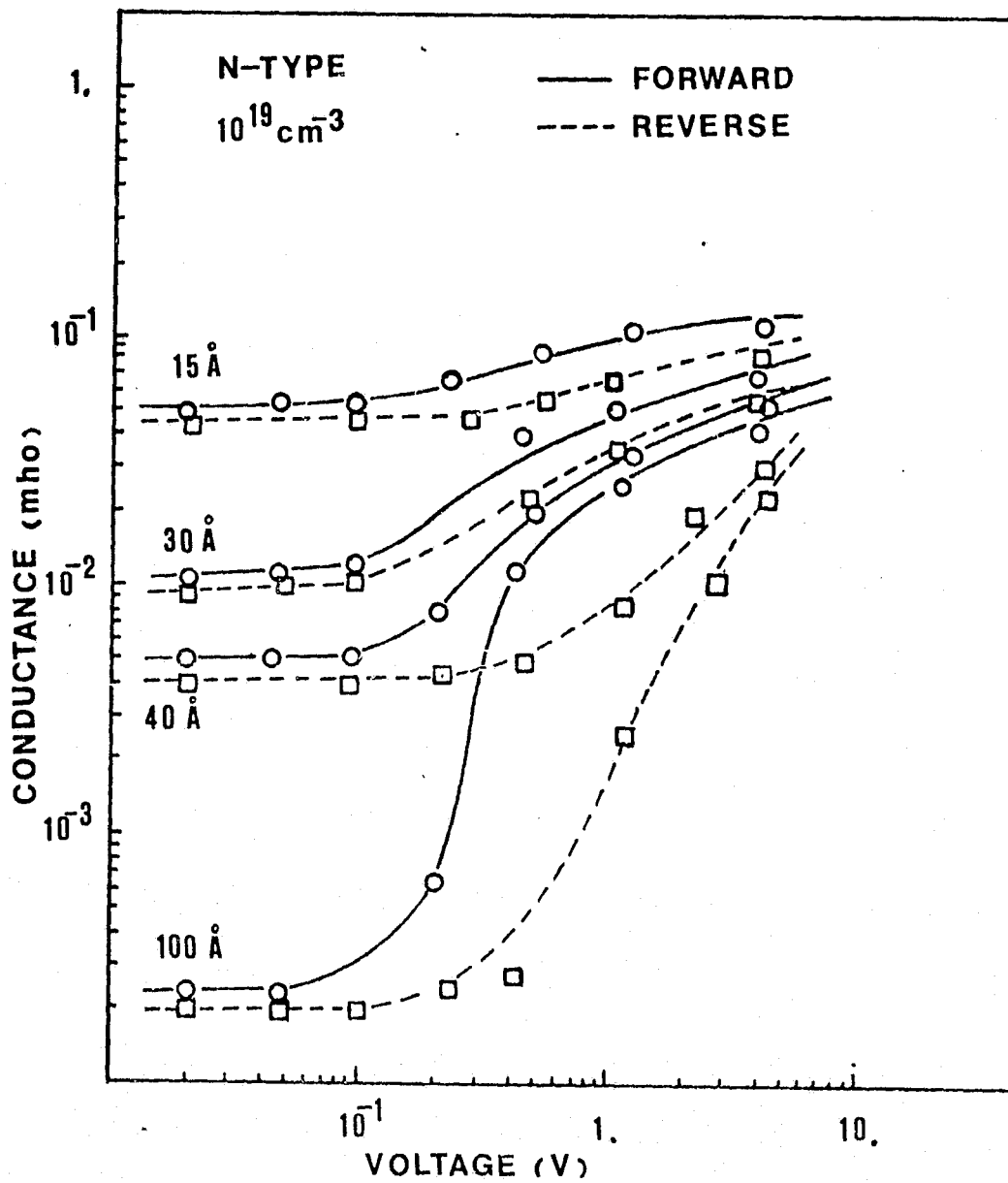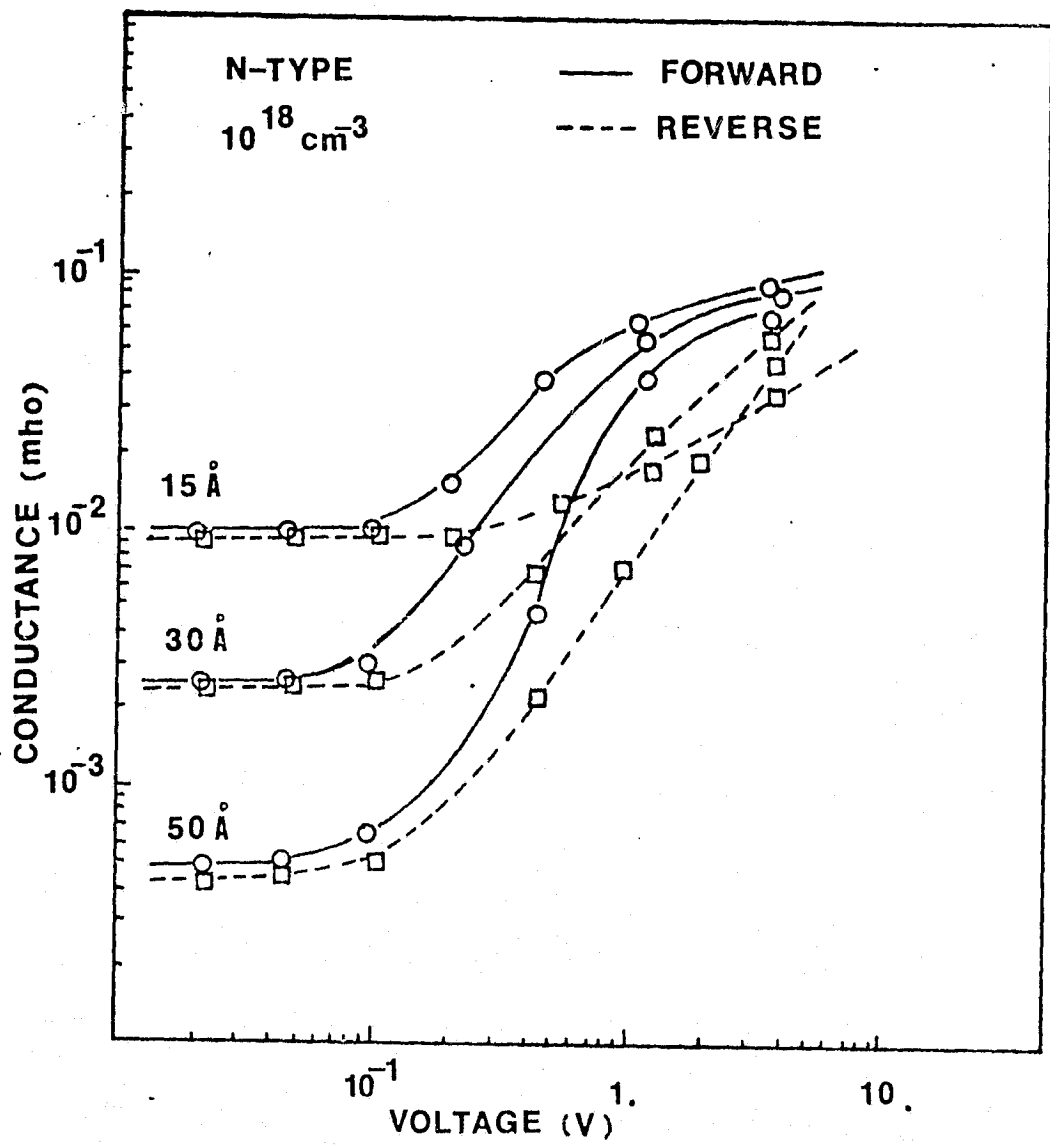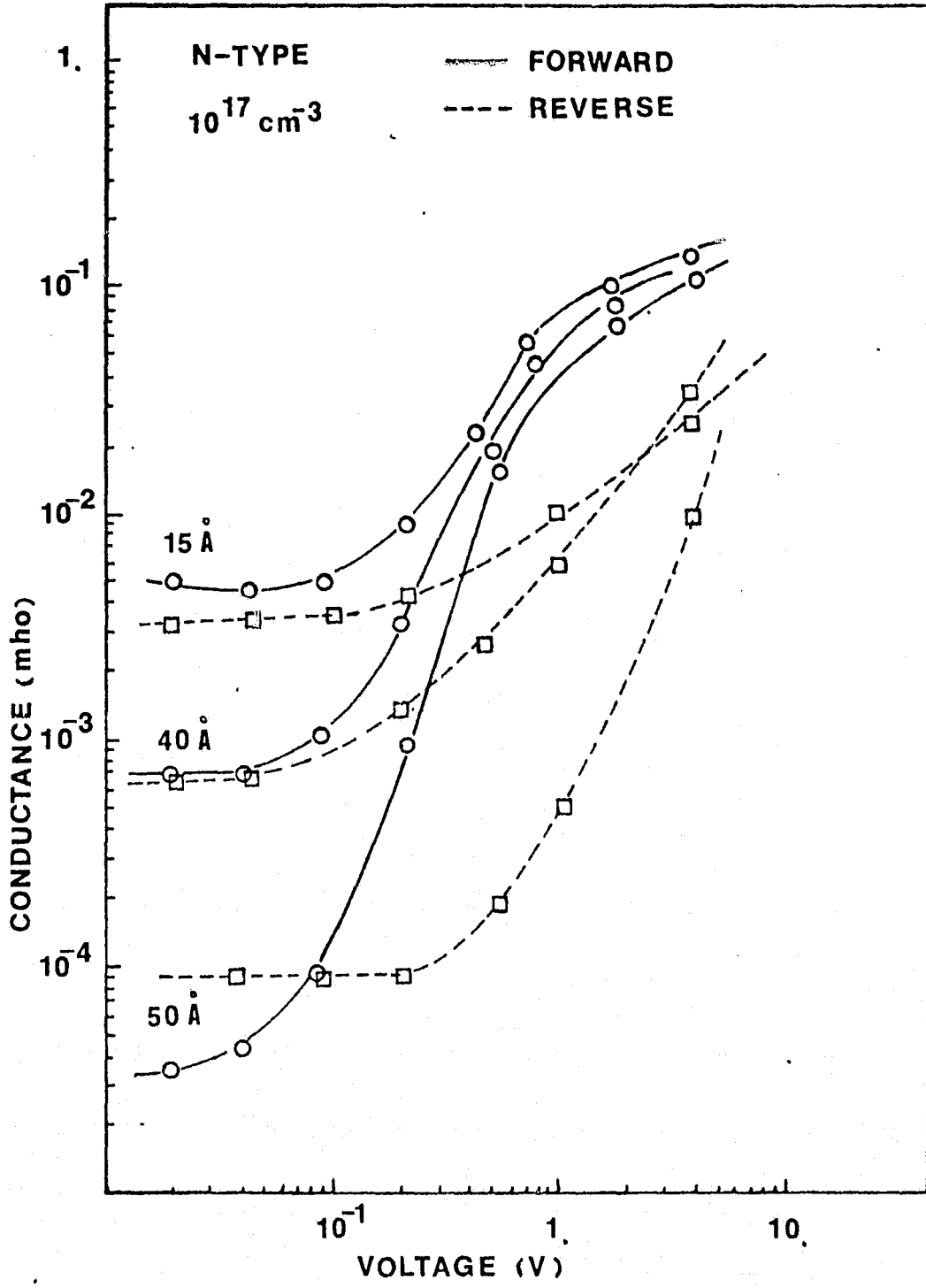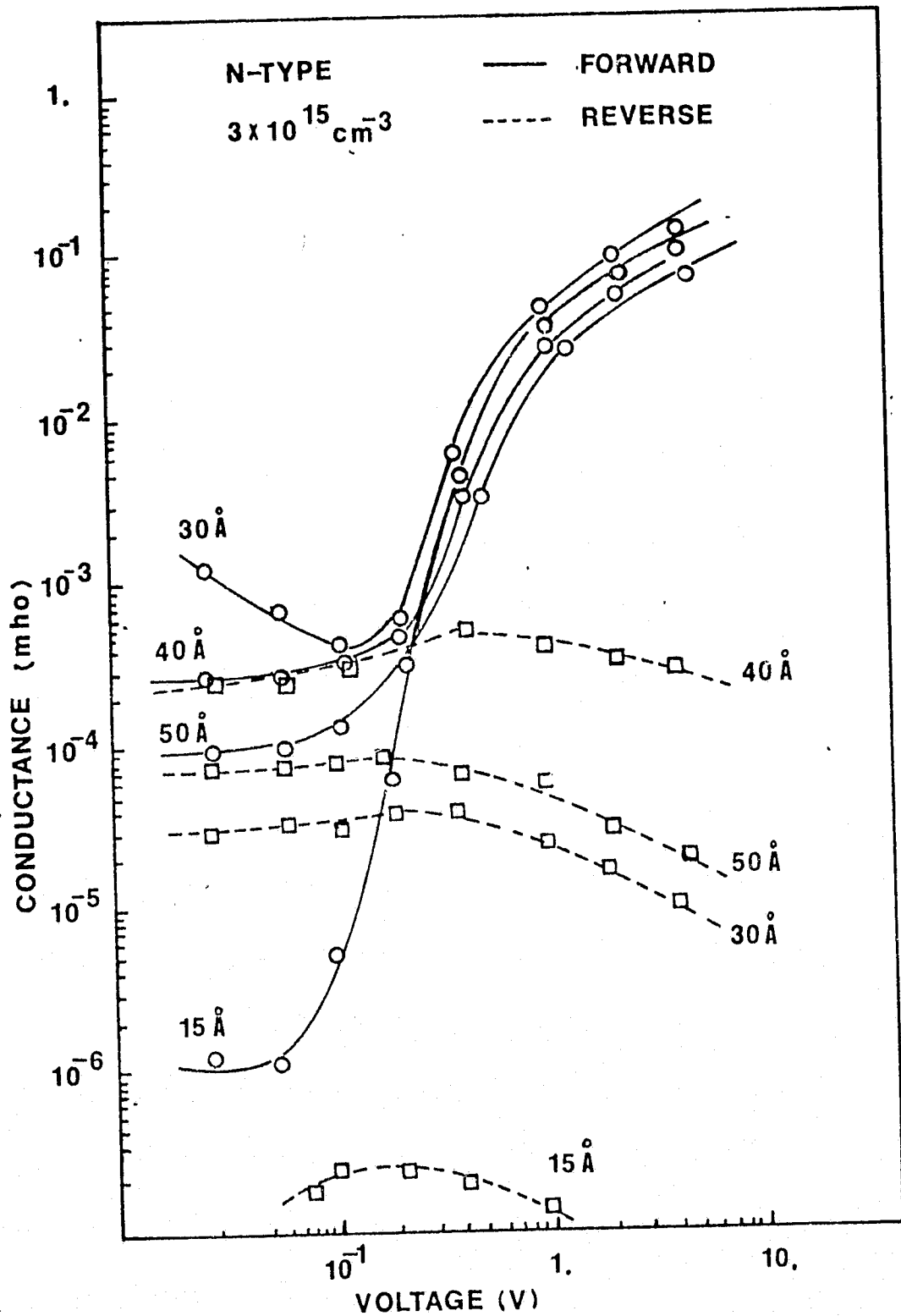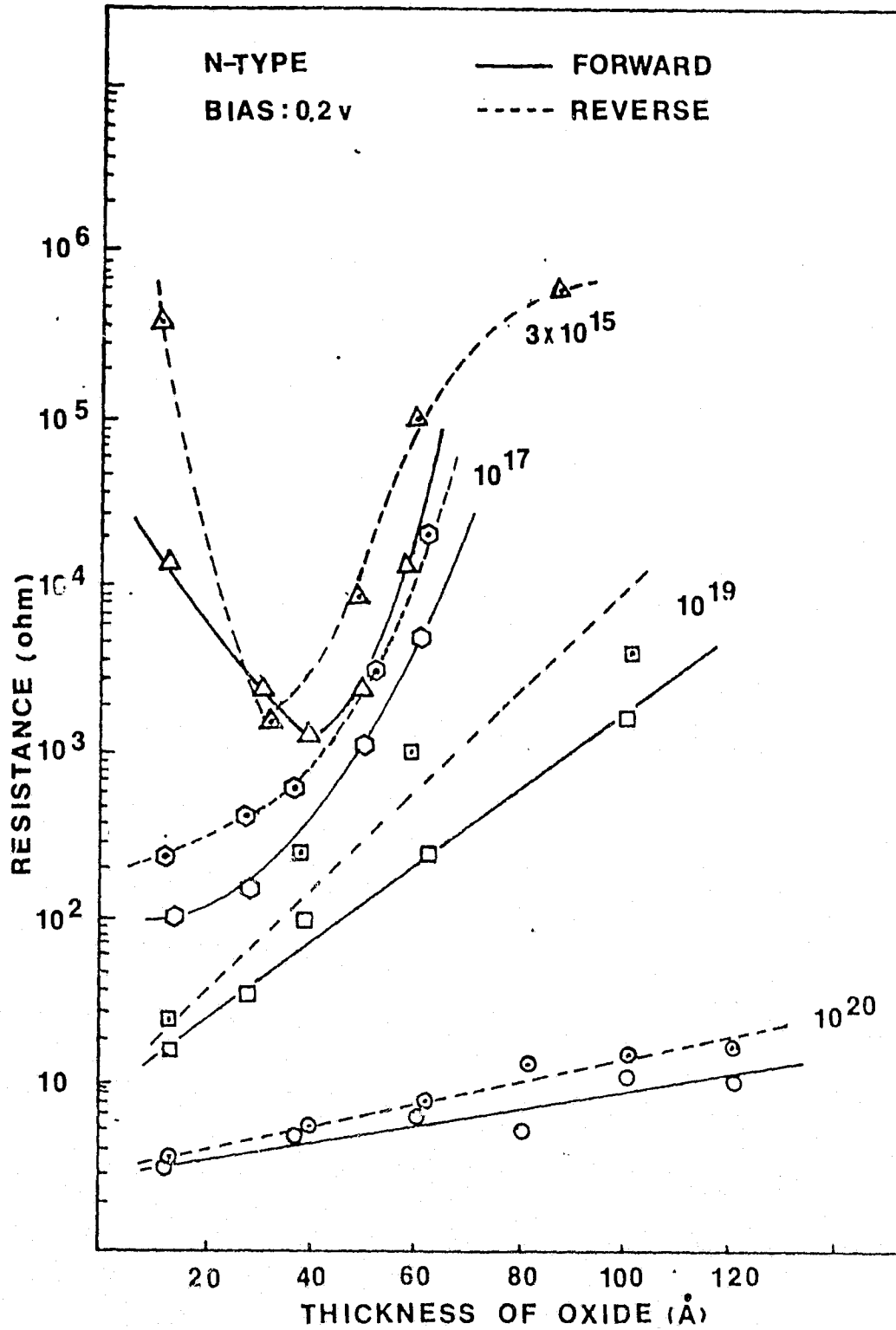concentration, 3 X 10^{15}atoms/cm^3 for n-type silicon.

Fig. 4.12 Resistance vs oxide thickness with various surface impurity concentrations for N-type silicon.
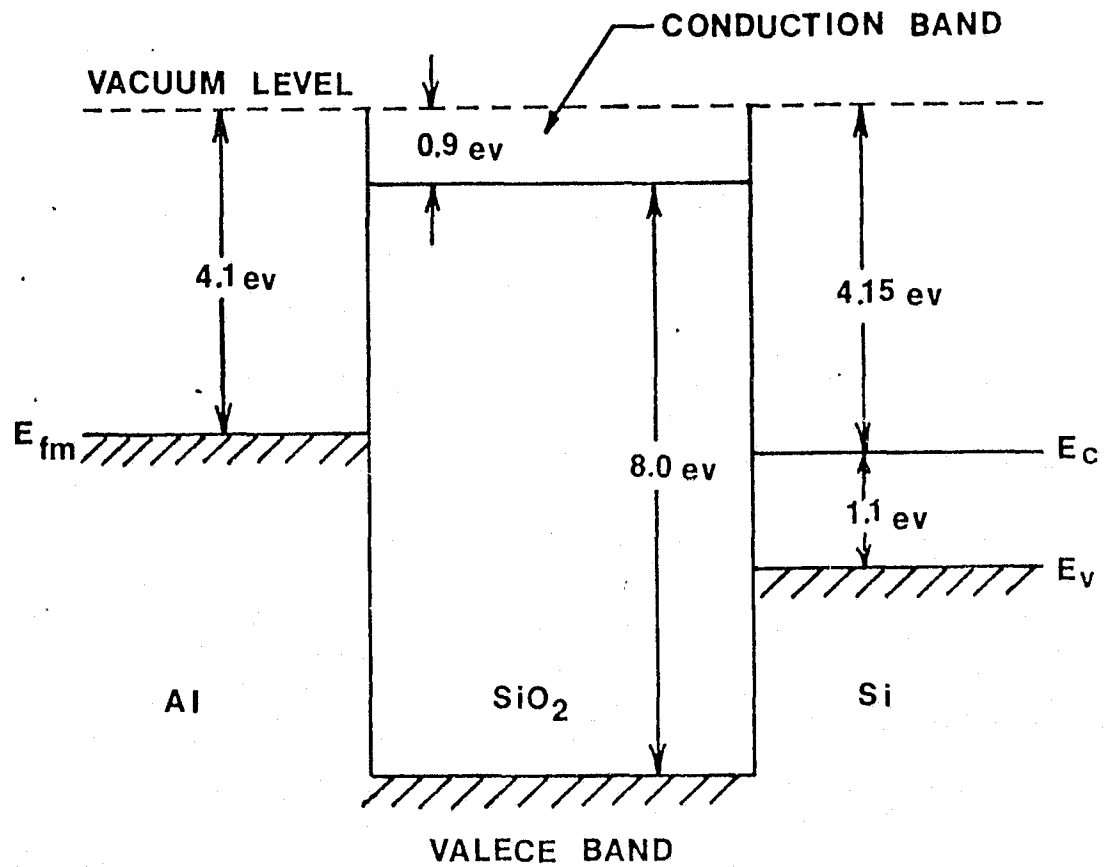
Fig. 4.13 Energy band diagram of Al-SiO$_2$-Si system.

However, the reverse current-voltage characteristics remain about linear.
To explain this behavior consider a perfect trap-free insulator with no
intrinsic carriers of a thickness S carrying a current J. Let the
field at a distance X from the surface be $E(X)$ and let $n(X)$ be the
member of free electrons per unit volume. Then at equilibrium the
current is given by:

$$J = ne\mu E(X) - De\left(\frac{dn}{dx}\right) \qquad [4.1]$$

where μ is the mobility and D is the diffusion coefficient. Neglecting
the diffusion term and assuming $E(X) = \frac{V}{s}$, Eq. [4.1] becomes

$$J = en\,\mu\left(\frac{V}{s}\right) \qquad [4.2]$$

At low voltage where the injected carrier density is less than N_o, the
thermally generated free carriers, Ohm's law will be obeyed (27), thus

$$J = en_o\,\mu\left(\frac{V}{s}\right) \qquad [4.3]$$

Eq. [4.3] may be an explanation for Ohmic regions on the current-voltage
characteristics. Fig. 4.14 shows the energy band diagrams of
Al-SiO$_2$-p-Si structure under different bias conditions. As the forward
bias increases the Fermi level (E_{fs}) in the silicon is shifted downward.
When the Fermi level is below the valence band edge at the silicon sur-
face, the holes in the valence band can "see" many empty states in the
valence band of the aluminum. Therefore the hole tunneling current in-
creases rapidly as shown in Fig. 4.14(b). This may explain why the con-
ductance increases at the bias above 0.1v. The Schottky barrier height
(ϕ_{bp}) is expected to be in the neighborhood of 0.1ev and Card (36) has
reported that the Schottky barrier height on p-type silicon is less than
0.35 ev. On the other hand, when a reverse bias shifts the Fermi level
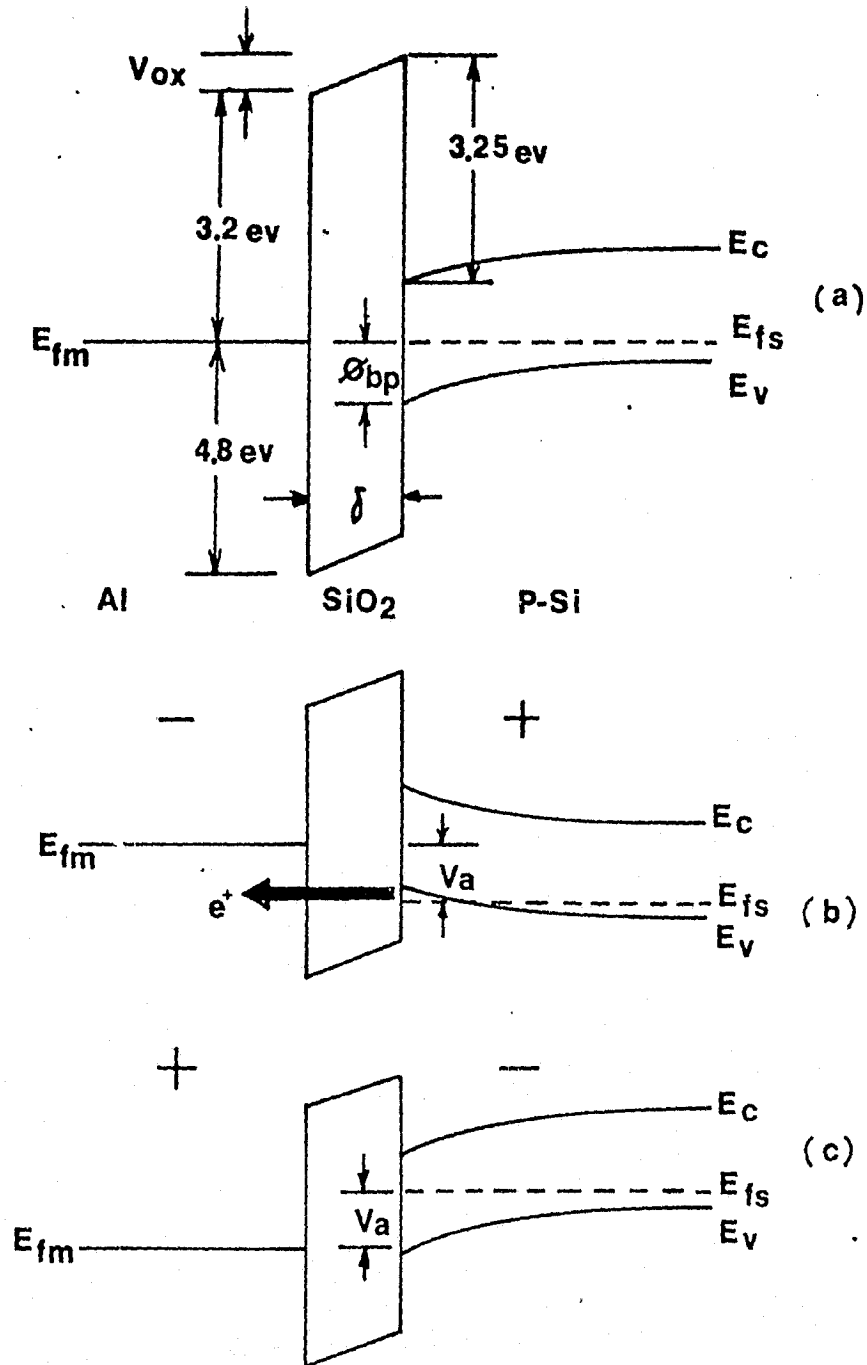upward there is no particular tunneling current taking place as shown in

P-TYPE

Fig. 4.14 Energy band diagram of Al-SiO$_2$-P-Si
system under different bias: (a) zero bias, (b) forward
bias, (c) reverse bias.

Fig. 4.14(c).

The oxide influence on the current-voltage characteristics can be seen from the conductance-voltage plots. At a forward bias above 0.1v thicker oxides give more conductance change for the same surface impurity concentration. This behavior may be explained by Fig. 4.15 which shows a difference of oxide thickness on the energy band diagrams. The thicker the oxide layer that exists at the aluminum-silicon interface, the more voltage appears across the oxide and the Fermi level in the aluminum is shifted upward. Thus the tunneling current from the valence band of the silicon to the unoccupied states of the valence band in the aluminum increases.

Considering the n-type silicon wafers, both the forward and reverse current-voltage characteristics in Figs. 4.7 - 4.11 show ohmic as well as the p-type silicon wafers at biases below 0.1v. The ohmic characteristics remain for various oxide thickness and surface impurity concentrations except for a lightly doped surface. This behavior can be explained is the same manner as the p-type silicon. Exceeding the bias voltage above 0.1v, the forward bias conductance starts to increase; the Fermi level (E_{fs}) shown in Fig. 4.16 (b) locates above the conduction band edge (E_c) at the silicon surface. The electrons in the conduction band of the silicon can "see" many empty states in the valence band of the aluminum. The Schottky barrier height (ϕ_{bn}) is expected to be in the neighborhood of 0.1ev. However, 0.7~0.9ev of the Schottky barrier height for n-type silicon has been reported by Card (36). The reverse current-voltage characteristics are different from that of the p-type silicon; the conductance also increases as the reverse bias increases instead of being constant as is the case for p-type silicon. This

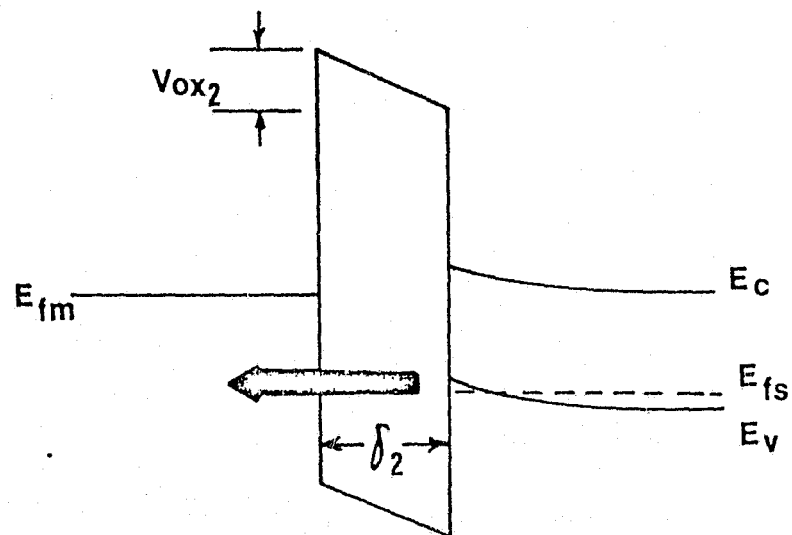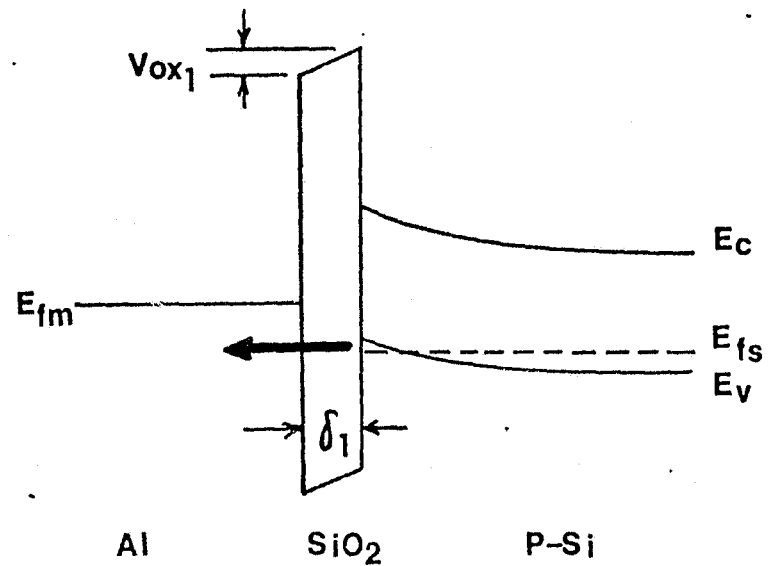**P-TYPE**

FORWARD BIAS

Fig. 4.15 Energy band diagram of $Al-SiO_2-P-Si$ system with different oxide thickness.
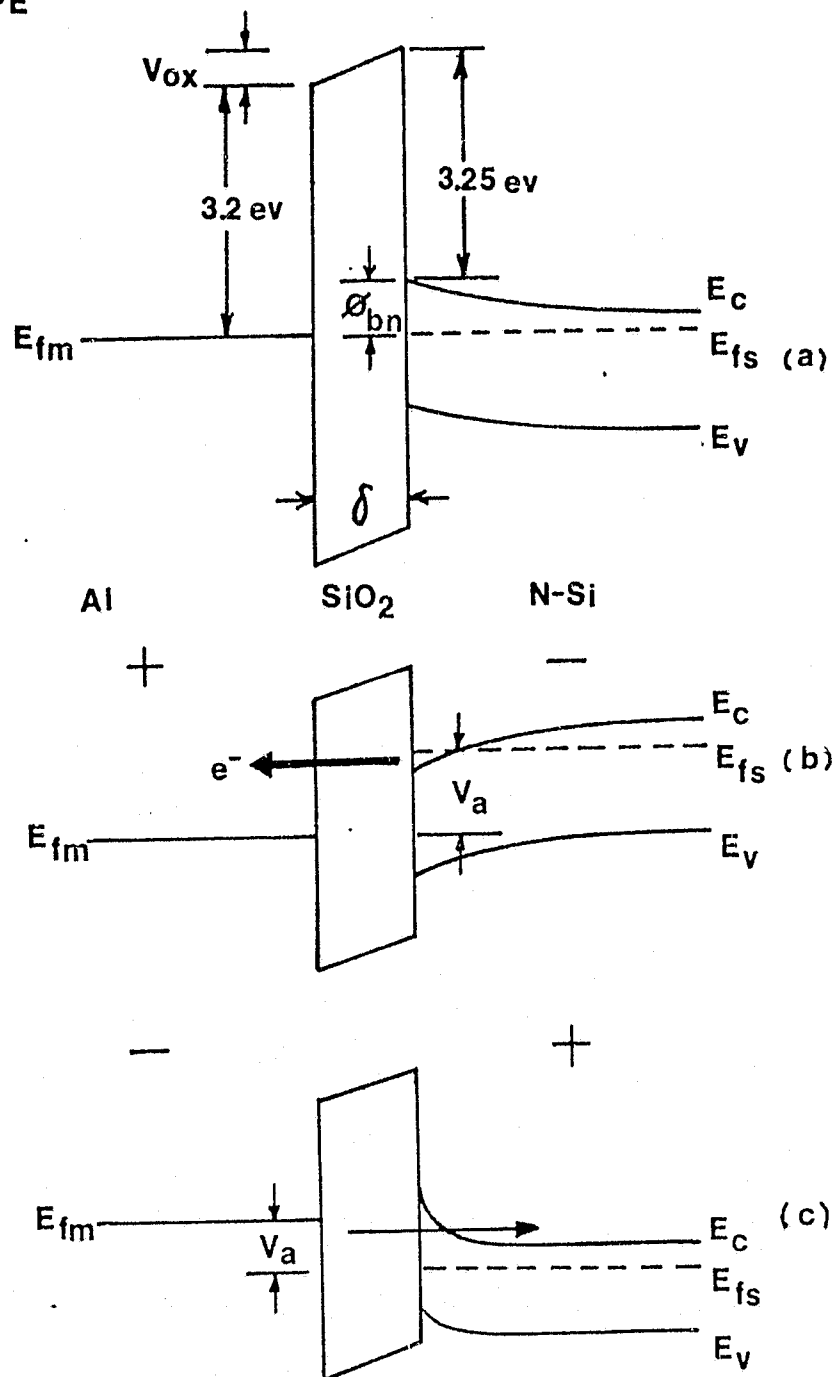
Fig. 4.16 Energy band diagram of Al-SiO$_2$-N-Si system under different bias: (a) zero bias,(b) forward bias, (c) reverse bias.

discrepancy may be explained as follows. Because of its diffusion
property, phosphorus tends to pile up in the silicon side at the
Si-SiO$_2$ interface. The depletion region in the silicon may become
thin enough for tunneling, thus the electrons in the valence band of
the aluminum can even tunnel through the depletion region in the
silicon. As the reverse bias increases the Fermi level in the silicon
is shifted downward as shown in Fig. 4.16(c).

The effect of the oxide thickness on the current-voltage
characteristics can be seen here as well as on the p-type silicon. In
Fig. 4.17 the Fermi level of the aluminum is shifted downward due to a
larger induced voltage across the oxide layer for thicker oxide layers.
As a result tunneling of electrons increases from the conduction band
of the silicon to the unoccupied states in the conduction band of the
aluminum.

The resistance of Al-SiO$_2$-Si structures increases exponentially
as the oxide thickness increases as shown in Fig. 4.6 and Fig. 4.12.
However, an unexpected behavior of the resistance and oxide thickness
characteristics can be observed for lightly doped (3 x 10^{15} atoms/cm^3)
n-type silicon. In particular, the reverse bias current increases as
the oxide thickness increases for silicon having oxide thicknesses below
40Å. Card (13) has reported a similar behavior in that the minimum
resistance of the reverse bias occured at the oxide thickness of 35Å
on a Au-SiO$_2$-n-Si structure. Fig. 4.18 may explain this behavior.
The thicker oxide layer induces more voltage across it and the Fermi
level in the aluminum is shifted upward. Therefore the tunneling of
electrons from the conduction band of the aluminum to the conduction
band of the silicon increases. Further, an increase of the oxide

N-TYPE
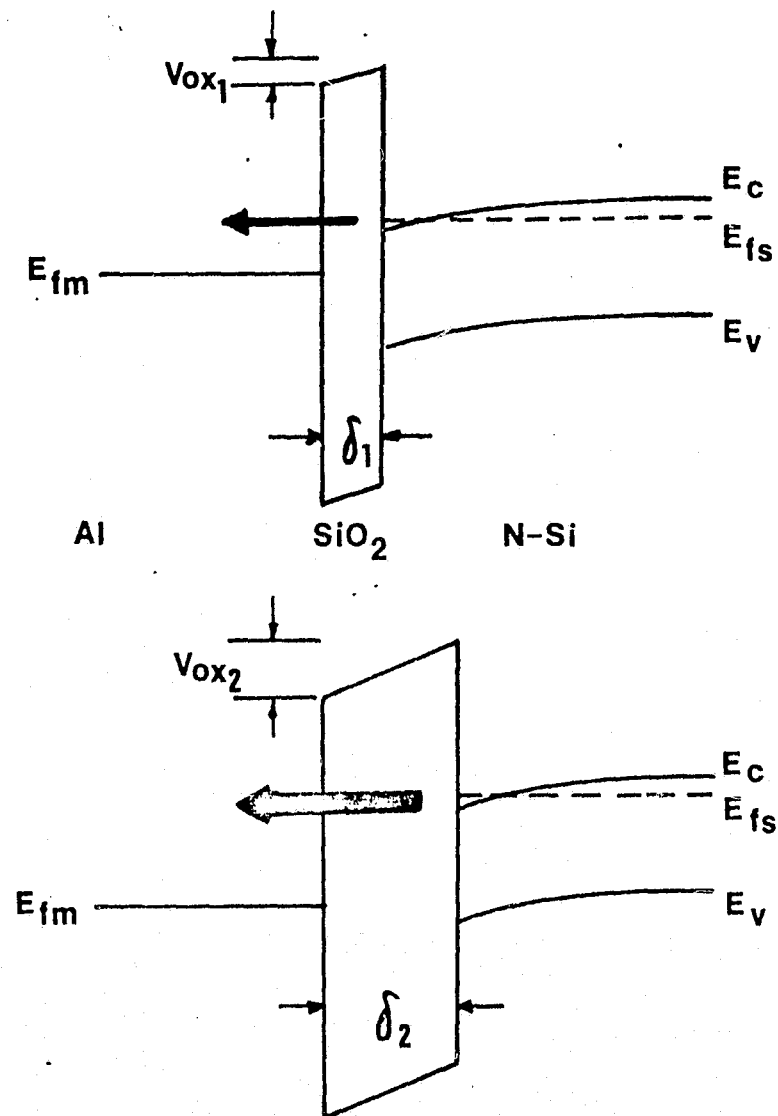
FORWARD BIAS

Fig. 4.17 Energy band diagram of Al-SiO_2-N-Si system with different oxide thickness.
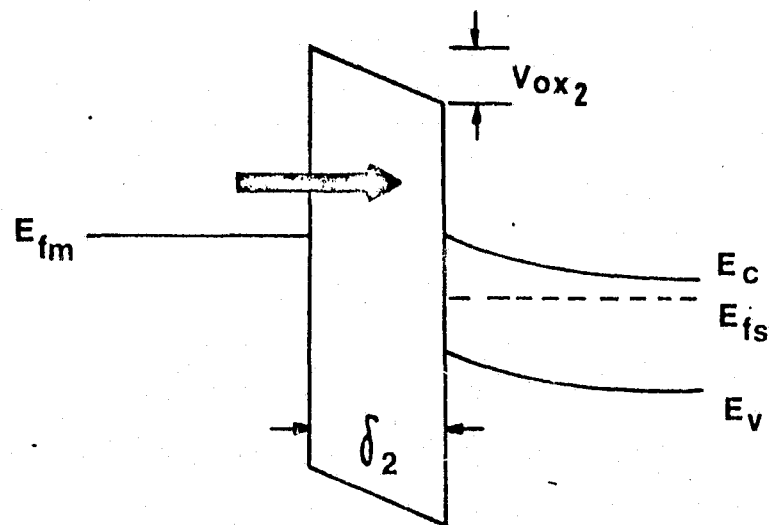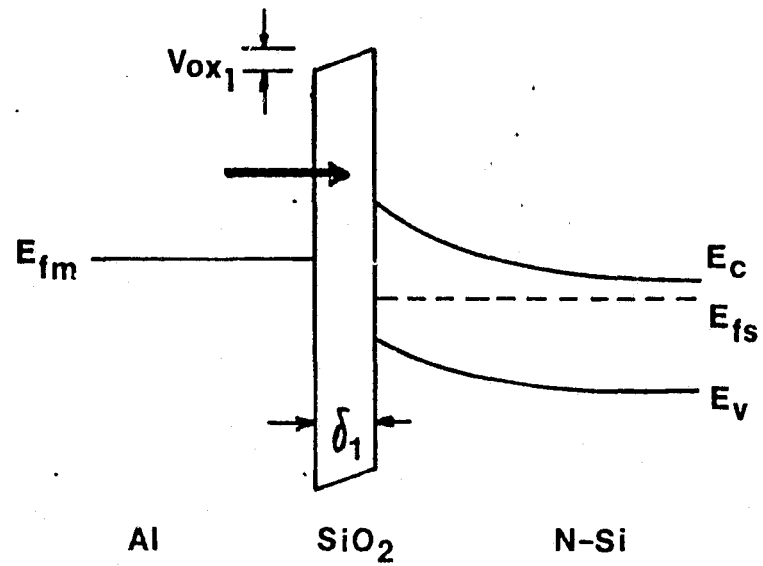
N-TYPE

REVERSE BIAS

Fig. 4.18   Energy band diagram of Al-SiO$_2$-N-Si system with different oxide thickness at reverse bias.

thickness reduces the tunneling probability exponentially and the effect of shifting the Femi level becomes neglegibly small.

For both p and n-type silicon the surface impurity concentration affects the current-voltage characteristics as well as the interfacial oxide. In particular, a highly doped silicon surface makes the current-voltage characteristics ohmic and provides large current conduction. Possible reasons for this behavior are expected to be: (i) an oxide on the highly doped surface may have large thermally generated free carriers, then the injected carrier density in still smaller than the thermally generated free carrier and ohmic characteristics can be maintained, (ii) a large amount of impurity in the oxide keeps the injected carrier density small as the electric field increases, (iii) a total voltage is dominated by the voltage across the oxide layer, the effective oxide barrier height is reduced due to a Schottky lowering, (iv) a depletion region in the silicon becomes thin enough for electrons to tunnel through.

In order to make good ohmic contacts, an annealing process is required. Before heat treatment Al-Si contacts clearly showed diode characteristics, even those having the highly doped surface. Following the heat treatment, the Al-Si contacts became ohmic for p-type silicon. Unless the surface was highly doped ($>10^{19}$ atoms/cm^3), the Al-Si contacts showed diode characteristics for n-type silicon. It is well known that aluminum is an acceptor impurity in silicon. The diffusion coefficient of silicon in aluminum ($\approx 4 \times 10^{-8}$ cm^2/sec.) is much larger than that of aluminum in silicon ($\approx 10^{-19}$ cm^2/sec.) at 550°C (37). In the heated junction, silicon becomes dissolved in the aluminum up to its solid solubility limit ($\approx 1\%$ at 550°C). Then the

junction cools, the dissolved silicon recrystallizes on the silicon surface. This newly formed silicon layer contains aluminum at the solubility limit appropriate to the temperature at which the silicon recrystallized. Card (37) also has reported that after heat treatment at 550°C, the aluminum tail in the silicon surface indicated the existence of a p^+ region (the recrystallized region) of width 100-200Å and the acceptor concentration 10^{19} atoms/cm^3 was determined by using Auger electron spectroscopy. An Al-SiO$_2$ reaction is known to occur quite rapidly at temperatures in excess of 500°C. Shanable et al. (38) have reported that shorting occured through a 300Å SiO$_2$ layer after 20 min. of heat treatment at 525°C. In this experiment after removing the aluminum and a 100Å thick oxide layer many pits have been seen on the silicon surface. These pits are expected to be a silicon precipitation. Consequently, an Al-p^+-p-Si and an Al-p^+-n-Si junction can be expected to form at the interface. Specifically aluminum on n-type silicon results in a p-n junction; Al-n-Si contacts are more sensitive to the oxide layer and the surface impurity concentration on the current voltage characteristics than Al-p-Si contacts are.

In addition, the current conduction may not be only due to a tunneling current but also a leakage current. Lepselter et al. (39) have reported the "edge effect" where a high-field concentration gives rise to excess leakage current and a low breakdown voltage.

X-ray Topography

Fig. 4.19 shows X-ray topographs of Al-SiO$_2$-Si structures whose sample preparation was described previously. Regions 1,2,3 and 4 corresponds to 0.3μ Al-15Å SiO$_2$, 0.15μ Al-15Å SiO$_2$, 0.15μ Al-100Å SiO$_2$ and 0.3μ Al-100Å SiO$_2$, respectively. Before heat treatment only a slight
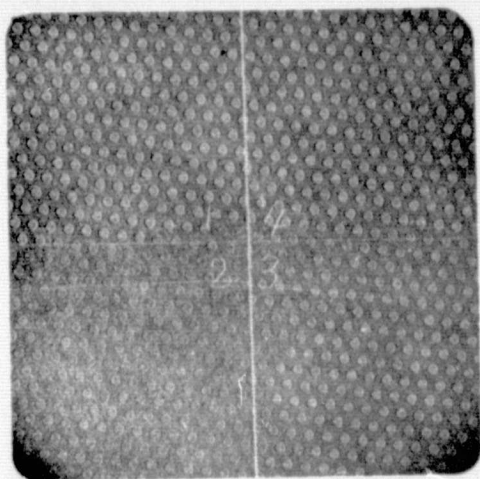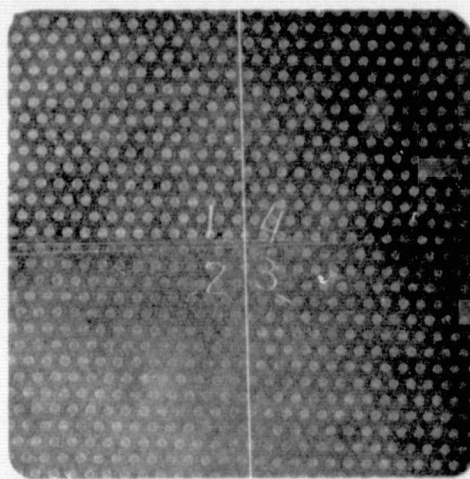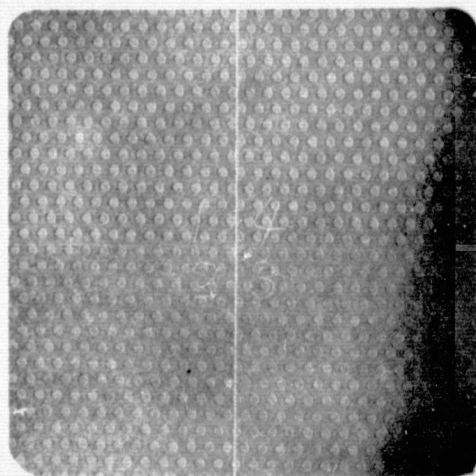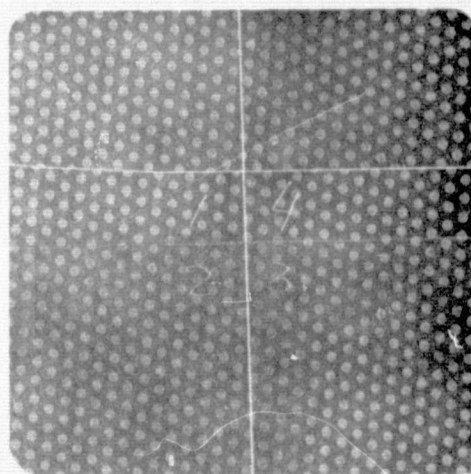
N-TYPE ⟨111⟩

N-TYPE ⟨100⟩

P-TYPE ⟨111⟩

P-TYPE ⟨100⟩

Fig. 4.19 X-ray topographs of Al–SiO₂–Si system.

image of the aluminum dot patterns was observed for both p and n-type silicon. Following the heat treatment, the image of the aluminum patterns became very clear. Comparing the images for each region, one observes that the images of regions 1 and 4 (0.3μ Al), have more contrast than those of regions 2 and 3 (0.15μ Al) for both p and n-type silicon. However, the contrast of the regions is more distinct for n-type silicon. Further, the orientation difference, $\langle 111 \rangle$ and $\langle 100 \rangle$, and the oxide thickness difference, 15Å and 100Å, having 0.3μ Al does not cause a noticeable difference in the image contrast. Therefore, it can be expected that the stress at the silicon surface is created by (i) Al-Si interdiffusion due to the heat treatment, (ii) the oxide layer. In addition, the stress due to the oxide layer is much smaller than the one due to the aluminum layer.

CHAPTER V

CONCLUSION

Ohmic characteristics can be observed at low forward and reverse
bias ($< 0.1v$) for both n and p-type silicon for an $Al-SiO_2-Si$ structure
with various oxide layers' thickness ($15 \sim 100 \overset{\circ}{A}$) and various surface
impurity concentrations ($10^{20} \sim 10^{16}$ atoms/cm^3) except for lightly
doped ($< 10^{17}$ atoms/cm^3) n-type silicon. Above a bias of 0.1v, nonlinear
current-voltage characteristics appear for both n and p-type silicon.
A rapid change in conductance is probably due to tunneling current.
The influence of the interfacial oxide layer as well as the surface
impurity concentration on the current-voltage characteristics is large.
In general, the current conduction mechanism on an $Al-SiO_2-Si$ structure
can be explained using an energy band diagram where the dominant
tunneling conduction can be expected through a very thin oxide layer.
In particular an extremely highly doped silicon surface can have some
oxide layer ($\sim 100 \overset{\circ}{A}$) and maintains a linear current-voltage characteri-
stic. For an $Al-SiO_2-Si$ structure the current-voltage characteristic
of n-type silicon are more affected by the interfacial oxide layer
and the surface impurity concentration than for p-type silicon.
Aluminum behaves as an acceptor in silicon forming an $Al-p^+-SiO_2-n-Si$
or an $Al-p^+-SiO_2-n-Si$ by interdiffusion and recrystallization at the
interface. It is possible to increase the reverse current in an
$Al-SiO_2-n-Si$ structure by increasing the thickness of the interfacial
oxide layer.

X-ray topography shows that the stress at the silicon surface is generated by: (i) heat treatment, (ii) interfacial oxide layers.

Finally, it is recommended in order to confirm the current conduction mechanism that a temperature dependence on current-voltage characteristics has to be examined along with a guard-ring which eliminates the edge effect. Also an Auger electron spectroscopy analysis is recommended to identify the interdiffusion at the interface.

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