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A COMPLEMENTARY MOS PROCESS

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16. Abstract

The complete sequence used by the Goddard Space Flight Center, Microelectronics Facility to manufacture complementary metal oxide semiconductor (CMOS) integrated circuits is described. The fixed-gate array concept is presented as a means of obtaining CMOS integrated circuits in a fast and reliable fashion. Examples of CMOS circuits fabricated by both the conventional method and the fixed-gate array method are included. The electrical parameter specifications and characteristics are given along with typical values used by the Microelectronics Facility to produce CMOS circuits. Temperature-bias stressing data illustrating the thermal stability of devices manufactured by this process are presented. Results of a preliminary study on the radiation sensitivity of circuits manufactured by this process are discussed. Some process modifications are given which have improved the radiation hardness of our CMOS devices. A formula description of the chemicals and gases along with the gas flow rates is also included.

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A COMPLEMENTARY MOS PROCESS

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INTRODUCTION

This document presents the process used at the Goddard Space Flight Center (GSFC) to manufacture complementary metal oxide semiconductor (CMOS) integrated circuits. The processing steps, chemicals, and equipment used will be discussed as applied to the fabrication of the basic CMOS transistor pair. Electrical characterization, thermal burn-in data, and preliminary radiation hardness measurements are also included. In addition, process modifications found to improve radiation hardness of metal oxide semiconductor (MOS) integrated circuits will be mentioned.

The Microelectronics Development Section of GSFC has been providing flight quality p-channel MOS (PMOS) circuits for space applications since 1965. All design, processing, flight and nonflight testing, and packaging are performed in-house. The actual masks (working plates) are made under contract at Westinghouse Electric Corporation, Advanced Technology Labs (ATL), Baltimore, Maryland. Radiation measurements are performed with the Cobalt 60 (Co 60) source at the GSFC radiation facility.

AN OVERVIEW OF CMOS INTEGRATED CIRCUIT FABRICATION

The circuits produced at GSFC are designed to meet unique requirements which cannot be met with commercially available integrated circuits (IC) or which require an inordinate number of commercial parts to do so.

The advantages and disadvantages of CMOS are well documented (Reference 1). The CMOS inverter consists of an n-channel and a p-channel MOS transistor interconnected as shown in figure 1.

No resistors are used in the CMOS except for input protection. When properly operated, ground potential at the input will turn the p-channel transistor on, the n-channel transistor off, and direct the output to V_{DD}. Similarly, a voltage equal to V_{DD} at the input will turn the n-channel transistor on, the p-channel transistor off, and change the output to ground potential. For any particular logic input level, only one transistor is on. The other transistor is off and a negligible amount of current flows. This leads to extremely low static power dissipation; however, as the inverter switches, a pulse of current will flow. This occurs

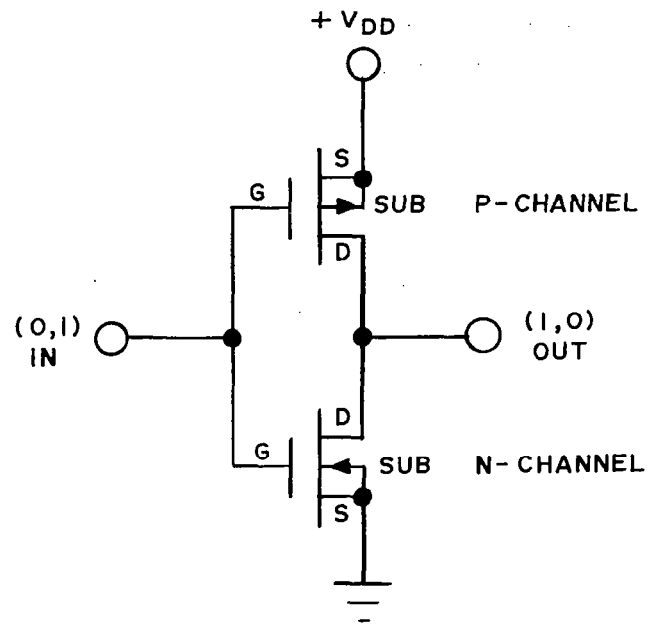

Figure 1. CMOS inverter circuit.

because both transistors are in a conductive state for an instant when the switching occurs. As the frequency of operation increases, the dynamic power dissipation due to these current pulses increases and becomes prohibitively high in the low megahertz range.

The threshold voltage of each transistor is an important parameter in the switching characteristic and must be accurately controlled. Another important parameter is the leakage current, the current that flows when the inverter is in a static state. It must be minimized to ensure low power dissipation. Generally, the leakage current is in the low nanoampere range per inverter. As the chip complexity increases, so does the leakage current.

CMOS IC DESIGN

The CMOS family of circuits used at GSFC are primarily fabricated using a standard fixed-gate array similar to the Radio Corporation of America (RCA) concept. This design consists of alternating arrays of n-channel transistors, p-channel transistors, and feed-through tunnels. The transistor channel lengths are 7.62×10^{-3} mm (0.3 mils) and the total chip size is 4.77 mm (188 mils) by 4.80 mm (189 mils). The first step in developing an integrated circuit is to determine what transistor configuration is required to perform the necessary electrical function. Once this has been done, the circuit is normally converted into the proper masking sequence. However, in the fixed-gate array configuration, the transistors and tunnels are already arranged in a specific pattern. Consequently, the mask designer

need only define the metal interconnect pattern conforming to the transistor circuit configuration. This phase consists of superimposing the metal interconnect pattern on a mylar sheet having the exact gate configuration of the fixed-gate array chip. Once the pattern's accuracy has been verified, the mask is coded on computer cards. The coding defines the shape and length of every segment which will appear on the final mask. This coding is then converted to a magnetic tape compatible with the mask generating system at Westinghouse, where the working plates are made.

There are some important benefits of the fixed-gate array concept that should be noted. The basic array consists of a proven configuration that need not be reproduced for each circuit. This particular feature of the fixed-gate array saves substantial design time, circumvents needless troubleshooting and mask regeneration, and offers a rapid turnaround time from design to IC. In addition, if the circuit performs incorrectly, the errors are confined to the metallization mask since it is the only design variable.

Many of the CMOS circuits are designed around the fixed-gate array, but this does not in any way preclude conventional (all masks) methods for CMOS design and fabrication. A microphotograph of the premetal deposition fixed-gate array is shown in figure 2. The p-channel transistors are larger than the n-channel transistors to compensate for the difference between the electron and hole mobilities. Two examples of circuits developed in the array fashion are shown in figure 3. An octal inverter fabricated in the conventional manner is also shown to illustrate the difference in design techniques.

CMOS PROCESSING

An advantage of the fixed-gate array is that wafers can be processed up to and including the metal deposition. At this point the wafers can be stored until a certain circuit is desired and only then is the correct metallization pattern defined. This allows stockpiling of processed wafers and ensures rapid turnaround time from design to finished product. The processing steps, presented in the following section, are the same whether a fixed-gate array wafer or some other CMOS circuit is fabricated. Once the wafers are completed, electrical evaluation is performed on individual n- and p-channel transistors.

Electrical Testing

Table 1 defines the specifications for the individual transistor parameters. Five areas of the wafer (the center and four extremities) are probed. Both the n- and p-channel parameters must be within specification in at least three areas for the wafer to be acceptable. Figure 4 shows the electrical configuration used to check each parameter. Once a wafer is accepted, dynamic testing is performed to ensure that the circuit is functioning correctly. A minicomputer is programmed to simulate input pulses and sense the outputs of the chip. The operation of the circuit is automatically checked and the bad chips are inked. The wafers are now ready to be diced and packaged.

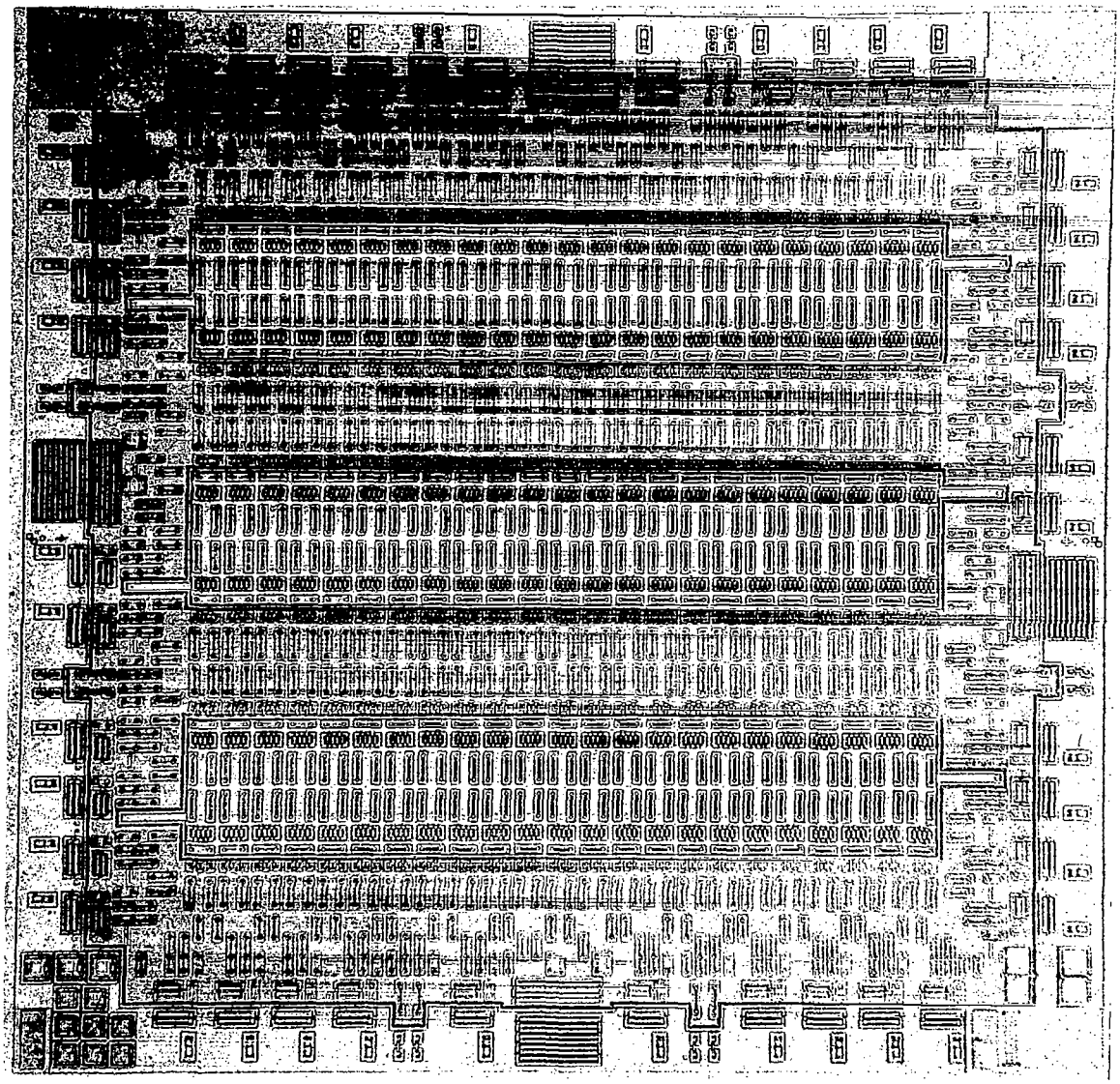

Figure 2a. Premetal deposition, fixed-gate array, 30x.

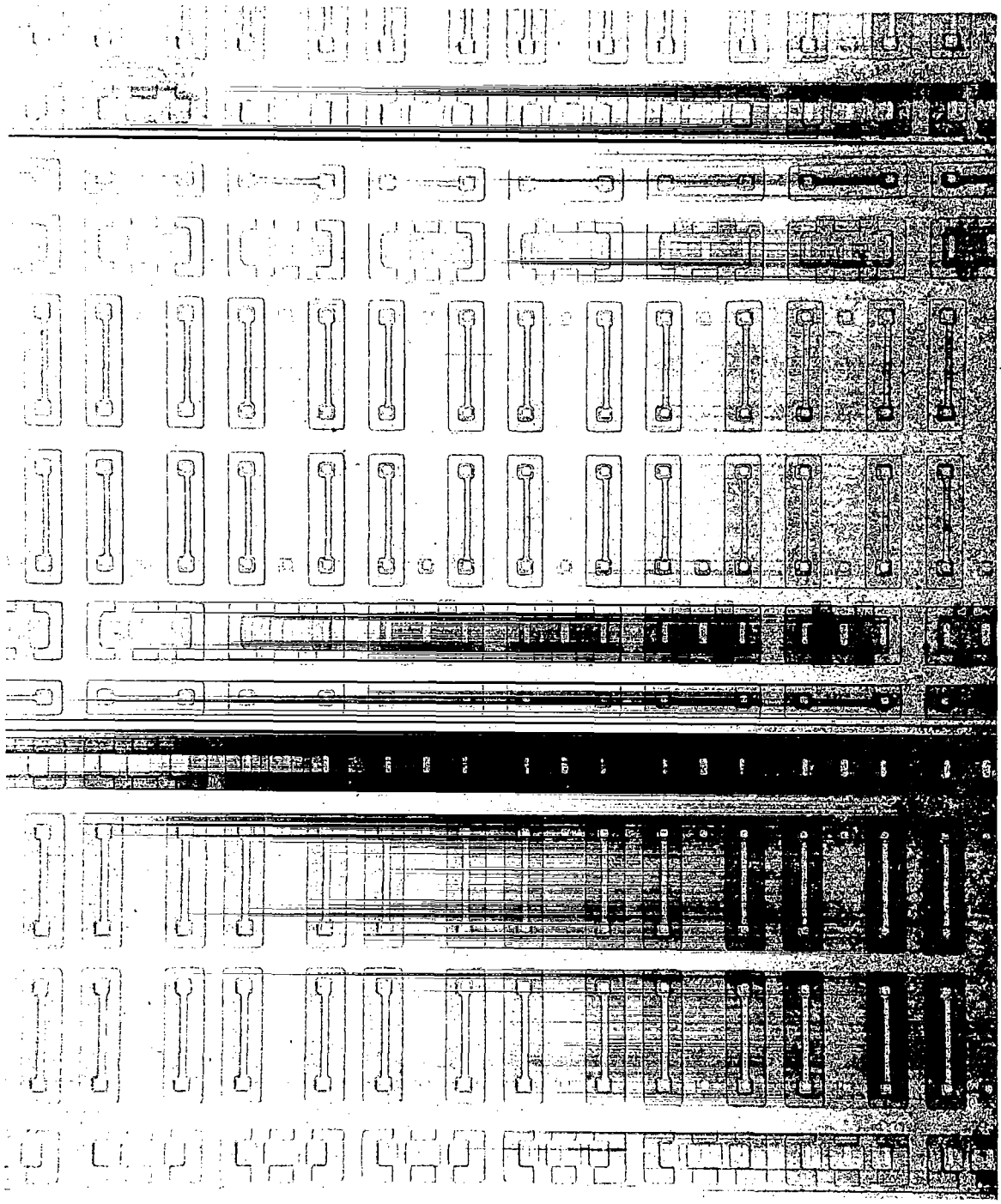

Figure 2b. Premetal deposition, fixed-gate array, 60x (enlarged portion of 2a).

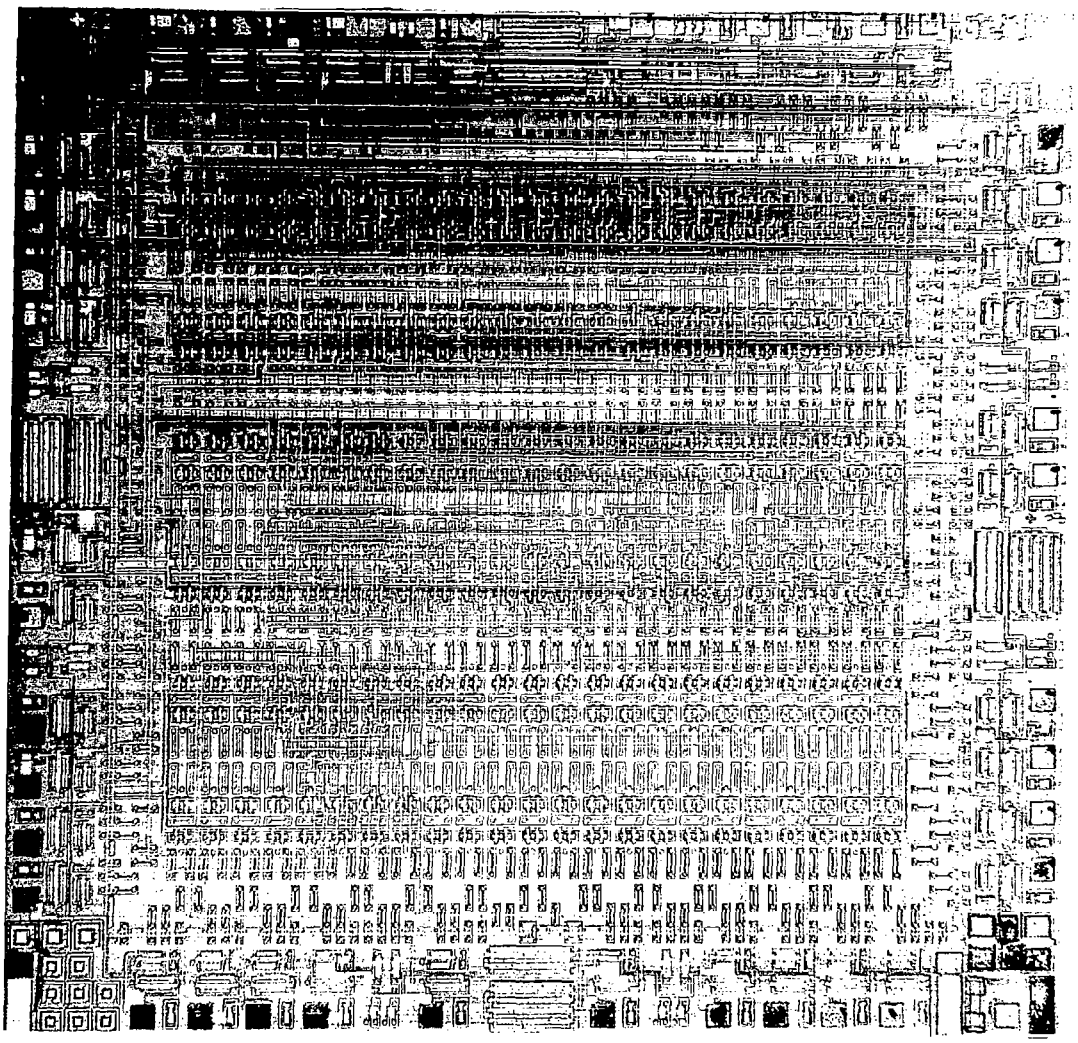

Figure 3a. Examples of CMOS circuits, type 627—CMOS nine-bit synchronous counter, 30x.

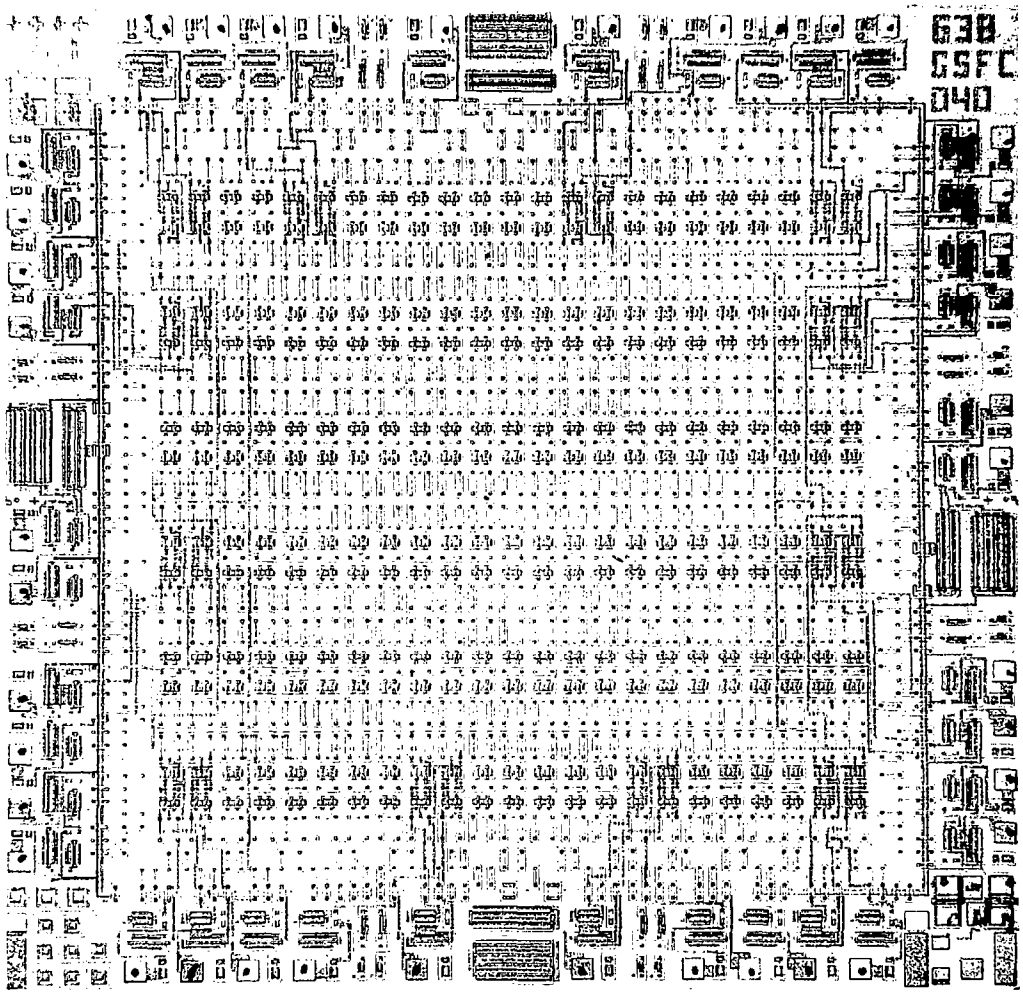

Figure 3b. Examples of CMOS circuits, type 638—CMOS tri-state driver, 30x.

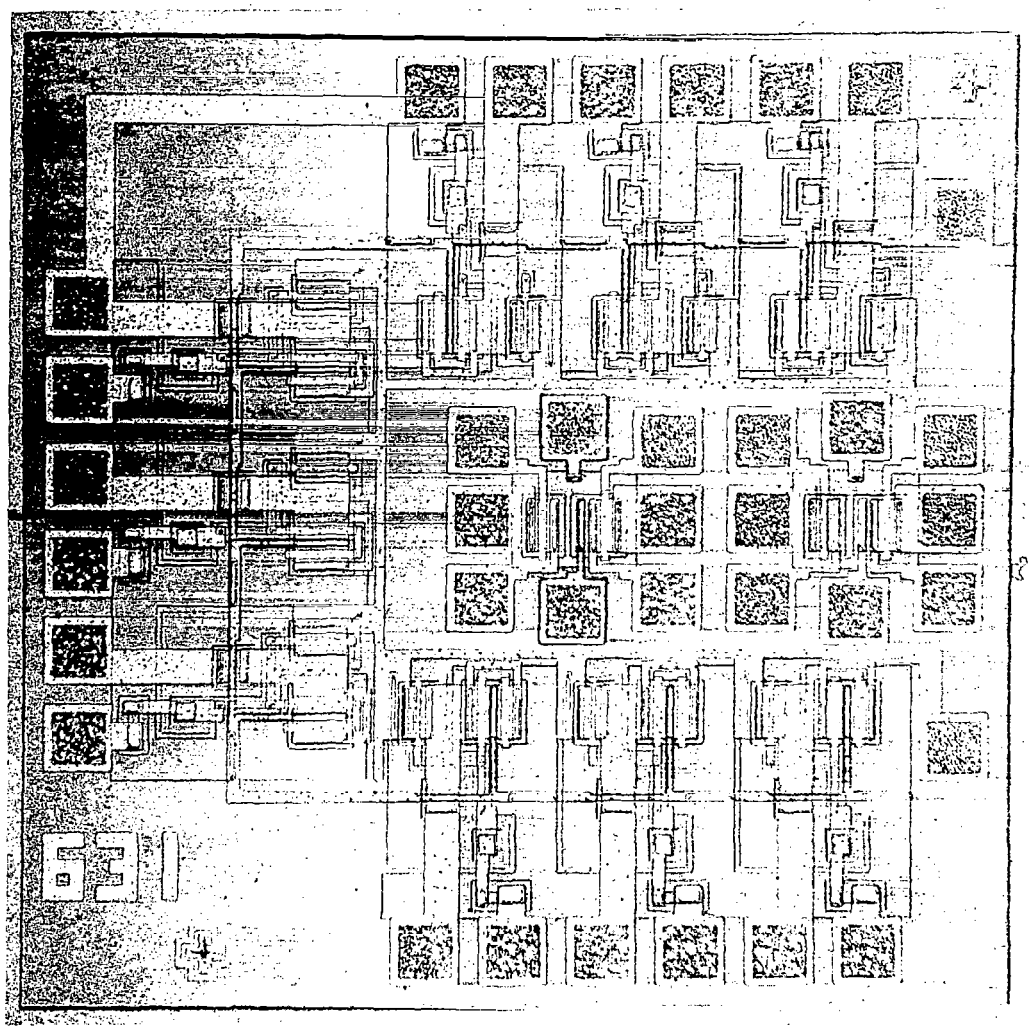

Figure 3c. Examples of CMOS circuits, type 631—CMOS conventional octal inverter, 30x.

Table 1
Individual Transistor Parameters

P-Channel Transistor					
	Figure 4*	Minimum	Maximum	Typical	Units
V_{TP}	A	-0.9	-2.2	-1.5	V
I_{DSS}	B	2.0	No limit	3	mA
BV_{DSS}	C	25	No limit	25	V
$BV_{P}+_{N}-$	D	25	No limit	60	V
BV_{OX}	E	60	No limit	120	V
I_L	F	–	50	5	nA
N-Channel Transistor					
	Figure 4**	Minimum	Maximum	Typical	Units
V_{TN}	A	0.8	2.1	1.5	V
I_{DSS}	B	3.0	No limit	7	mA
BV_{DSS}	C	25	No limit	32	V
$BV_{N}+_{P}-$	D	25	No limit	32	V
BV_{OX}	E	60	No limit	120	V
I_L	F		50	5	nA

*The letters shown in this column refer to the corresponding circuits shown in figure 4.

**Similar configurations are used to measure the n-channel transistor parameters, but the voltage polarities are reversed where necessary.

Packaging

Once the bad chips have been inked, the wafer is scribed and the die are separated. The bad chips are discarded and the good chips are thoroughly cleaned with Freon 12. The good chips are carefully inspected under 200x magnification for topographical defects. Circuits for flight use must conform to MIL-STD-883. The chips are then eutecticly die-attached in either TO cans or flatpacks ranging from 10- to 40-lead capability. For the CMOS fixed-gate array, a 34-lead flatpack is used. The connections from the chip bonding pad to the package

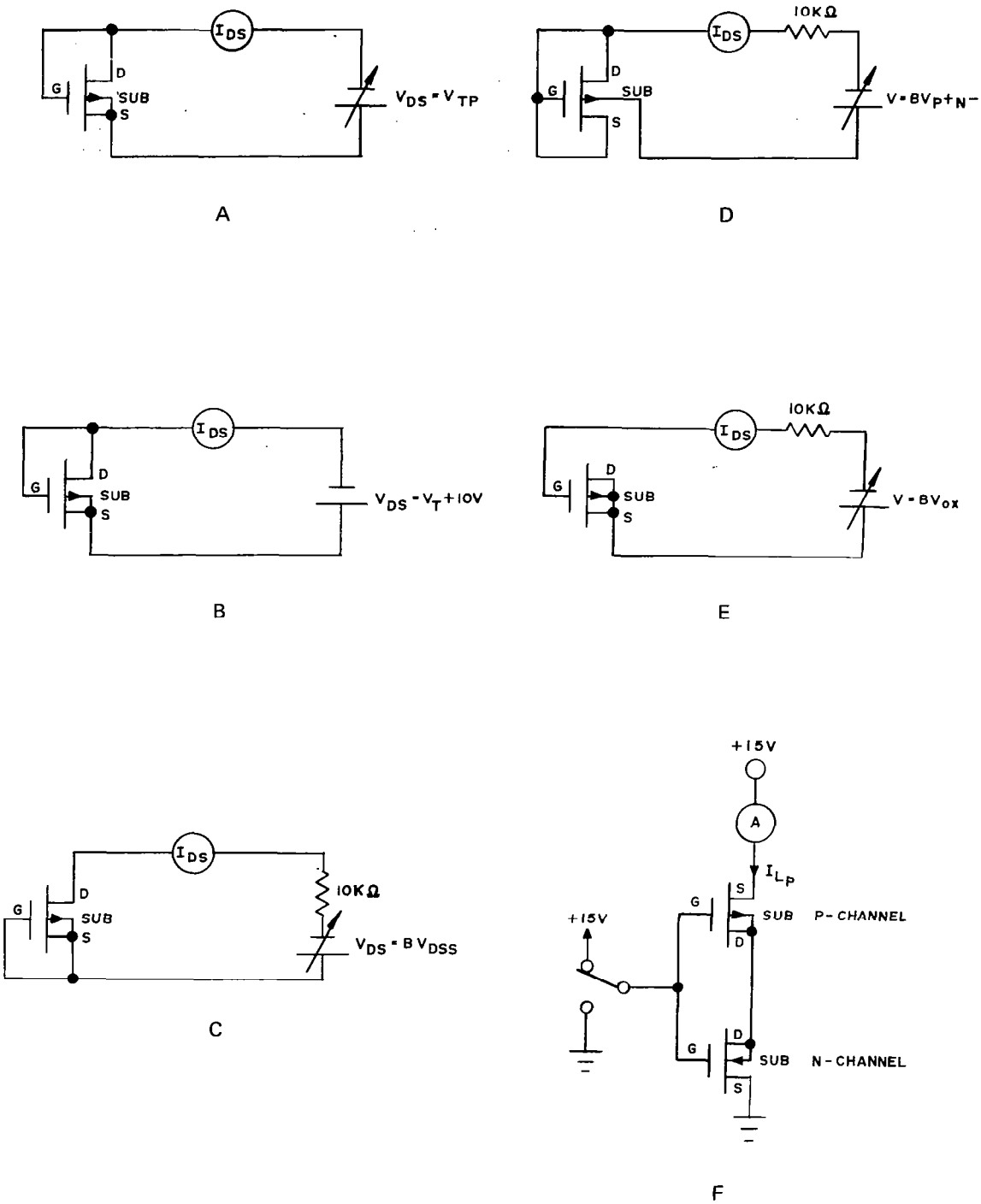

Figure 4. Testing configurations (see table 1).

are made either ultrasonically with aluminum wire or ball-bonded with gold wire. At this point, the chips are optically inspected by Quality Control in accordance with MIL-STD-883. After this phase is completed, wire-pull testing is performed on a test package, again in accordance with MIL-STD-883. The packages are hermetically sealed in dry nitrogen. Finally, helium fine-leak testing is done to ensure that the package is hermetically sealed.

Functional Retesting and Thermal Burn-In

Once the chips are packaged they are functionally rechecked by computer to verify proper circuit operation.

From each run twelve n-channel and twelve p-channel transistors are bonded in TO-5 cans. The turn-on, or threshold, voltage is checked on each device and recorded. The transistors are then subjected to temperature bias stressing. The procedure is to bias half of each type of transistor with +15 V between gate and substrate and the other half with -15 V. The transistors are heated to 125° C for a minimum of 100 hours. The devices are cooled and the threshold voltage is again measured. The difference between the pre- and post-burn-in threshold voltage is a direct measure of ionic impurity content in the gate oxide which may cause device instabilities. Figures 5 and 6 present data from six runs (randomly chosen) illustrating the threshold voltage shifts for n- and p-channel transistors. Excellent thermal stability has been accomplished primarily through the use of phosphyoxychloride ($POCl_3$) on the gate oxide. The actual CMOS integrated circuits are similarly burned-in, but only operational checks are made.

Radiation Testing

The sensitivity of PMOS and CMOS circuits to gamma radiation is currently being studied. Different processing techniques (Reference 2) have a profound effect on the radiation hardness of MOS devices. Studies are now being performed concerning the effects of several crucial processing steps. These include ion implantation, gate $POCl_3$, gate regrowth temperature and thickness, anneal temperature and time, metal deposition process, and metal alloy temperature and time. The results of this study will be presented elsewhere. However, as a start, some CMOS inverters have been made with some radiation hard processing modifications. These modifications of the process presented in the next section are:

- Use of boron nitride (p-dopant source) wafers instead of the p-well implant, avoiding a later n-channel transistor implant for increasing the V_T to enhancement mode operation.
- The gate oxide was grown at 1000° C in oxygen for 2 hours giving about 9.5×10^{-8} m (950 A). Annealing was performed at 850° C with nitrogen for 1 hour.
- No gate $POCl_3$.
- No ion implant for threshold voltage adjustment.

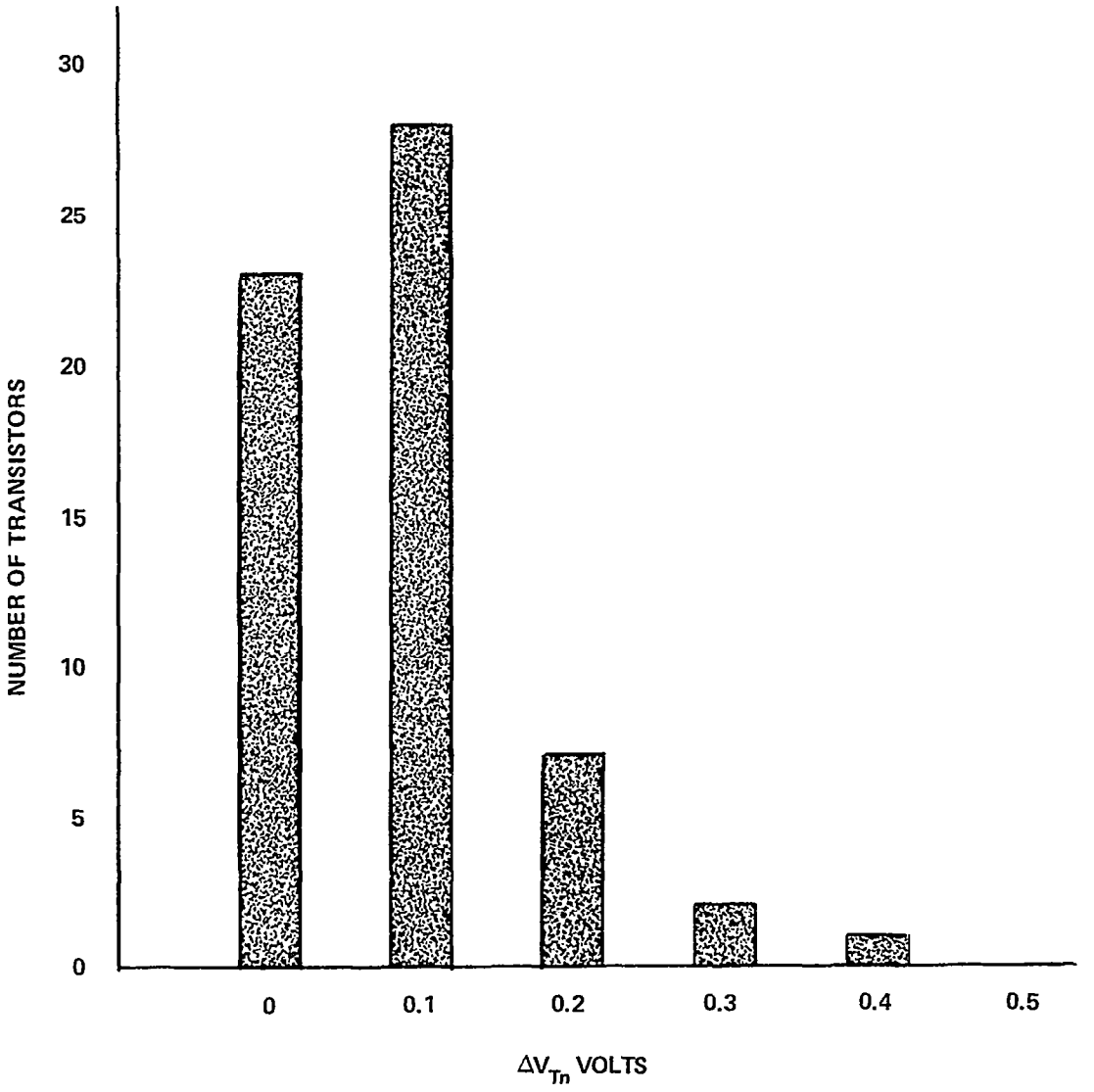

Figure 5. Data from six randomly chosen runs illustrating threshold voltage shifts for n-channel transistors.

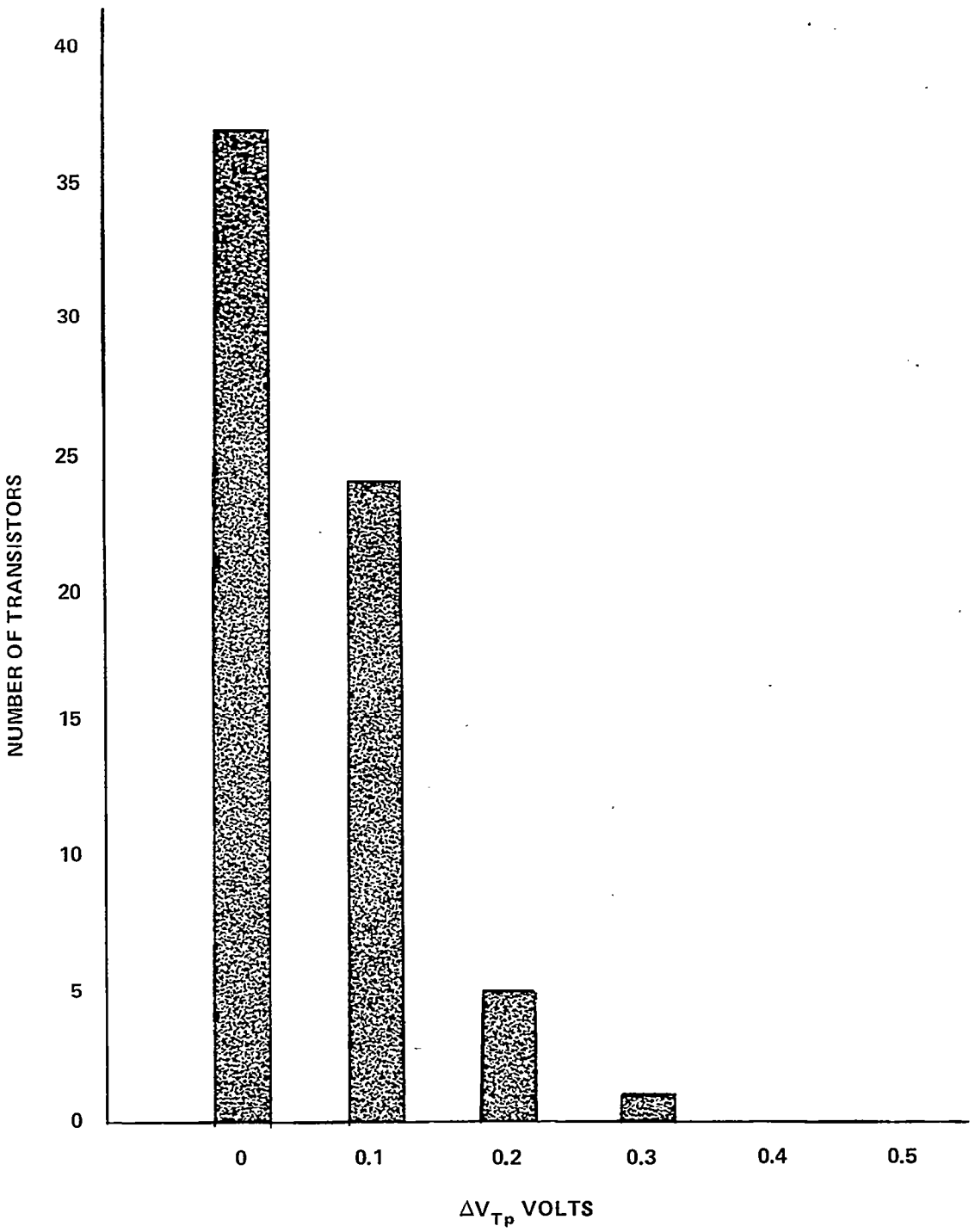

Figure 6. Data from six randomly chosen runs illustrating threshold voltage shifts for p-channel transistors.

The modifications listed previously were tested against the standard CMOS process. The threshold voltages were monitored as a function of the radiation dosage in rads. The radiation source was Cobalt 60 and the dose rate was 20 k rads/hr. A summary of radiation effects on threshold voltage is given in table 2. Since the main concern is the shift in threshold voltage as a function of the total radiation dose, only ΔV_T values are presented. Eight devices were sampled in each category of table 2, all with initial threshold voltages between 1 and 2.5 V. The increase in hardness is readily apparent. At 250,000 rads, the p-channel devices of the hardened process shifted about as much as the standard device had shifted at 15,000 rads, indicating a substantial increase in hardness. In our process the n-channel transistors are not affected as severely by gamma radiation as the p-channel transistors. However, at 250,000 rads, a shift of about 1 V occurs.

Table 2
Summary of Co 60 Radiation Effects on the
Standard and Modified CMOS Processes

	Threshold Voltage Shift Due to Radiation (in volts)			
	Standard Process		Modified Process	
	15 k rads	25 k rads	25 k rads	250 k rads
$\Delta\overline{V}_{TP}$	1.6	2.4	0.45	1.6
$\sigma\Delta V_{TP}$	0.11	0.23	0.08	0.23
$\Delta\overline{V}_{TN}$	0.15	0.15	0.09	1.1
$\sigma\Delta V_{TN}$	0.13	0.13	0.08	0.27

An attempt is being made to increase the hardness of these devices with a minimal amount of process variation. The preceding example indicates what can readily be achieved with a few process variations. Further investigation will likely reveal steps which can be easily eliminated, yet increase hardness considerably.

THE CMOS PROCESS

This section describes the step-by-step procedure used at GSFC to manufacture CMOS integrated circuits.

The starting material is n-type silicon. The crystal orientation is <1, 0, 0> and the substrate is uniformly doped with phosphorus to a concentration of about 9×10^{14} ions/cm^3 (a resistivity of 5 to 10 ohm-cm). The first step is to clean the wafers in boiling deionized water. The wafers are then subjected to a temperature of 1200° C in an oxygen atmosphere. The oxygen reacts with the silicon and 5.5×10^{-7} m (5500 A) of silicon oxide (SiO_2) is grown (figure 7). This reaction can be accelerated by passing the gas through heated water (H_2O).

Procedures

Field Oxide

1. Initial Cleaning
   a. Boiling Deionized Water (DIW) — 15 min
   b. Nitrogen Blow Dry (N_2 dry)
2. Oxidation 5.5×10^{-7} m (5500 A)
   a. 1000°C Oxygen through DIW (97° C) ($O_2 \cdot H_2O$) — 75 min
   b. 1000°C N_2 — 45 min

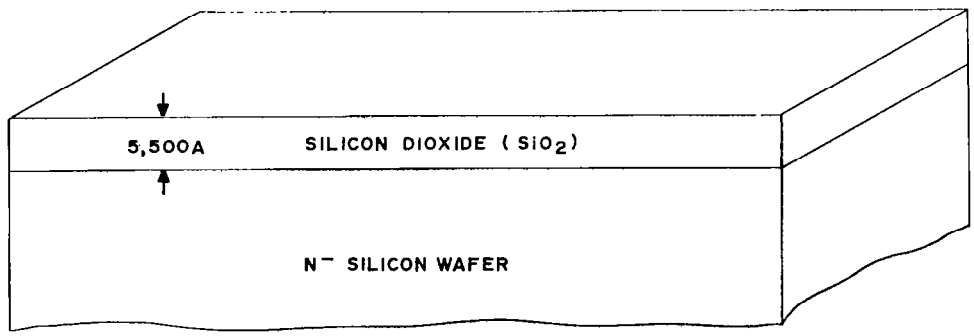

Figure 7. Silicon wafer after initial oxidation.

Once the SiO_2 is grown, the wafers are coated with liquid photoresist and spun at 6000 rpm. This ensures a uniform layer 6×10^{-7} m (6000 A) thick. This photoresist is sensitive to ultraviolet (UV) light. When exposed the resist polymerizes and when developed it becomes hardened. In this state the photoresist is resistant to many chemicals; however, if the photoresist is not exposed, it can be easily rinsed off. Once the silicon wafers are coated, a glass mask consisting of clear and blackened regions is placed against the wafer surface. Both wafer and plate are exposed to ultraviolet (UV) light for 3 seconds and the image on the plate (the p^- regions) is then photographed onto the resist (figure 8). The photoresist in the p^- regions is removed, exposing the SiO_2 underneath. The wafer is placed in a buffered hydrofluoric acid solution which dissolves the SiO_2, but does not react with the hardened resist. Once the SiO_2 is removed and the bare silicon surface reached, the vertical reaction stops and proceeds only laterally, an undesirable effect. Consequently, it is important to know exactly when to remove the wafers from the etch to minimize this undercutting. Finally, the hardened photoresist is stripped in hot chromic acid and the wafer appears as in figure 9.

P^- Well Mask

1.	Apply negative photoresist, 6×10^{-7} m (6000 A) thick, spin @ 6 K rpm	30 s
2.	Bake on a 70° C hot plate	15 min
3.	Expose P^- mask (UV light)	
4.	Develop, rinse, and dry	

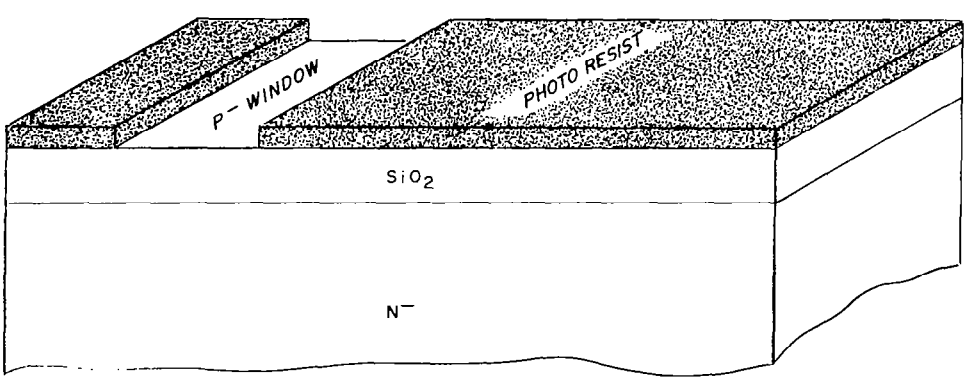

Figure 8. Wafer with the p^- regions defined by the photoresist.

5. Post bake on a 120°C hot plate — 30 min
6. Etch until oxide is removed in buffered hydrofluoric acid solution
7. Cold DIW rinse

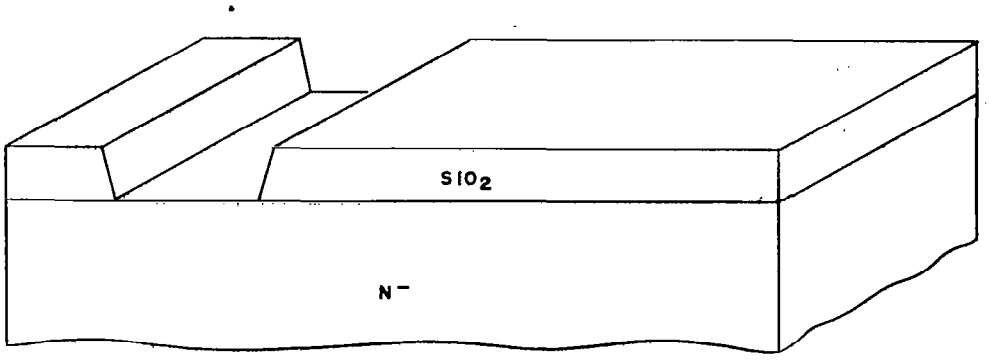

Figure 9. Wafer after SiO_2 removal in buffered hydrofluoric acid and photoresist removal in chromic acid.

8. Remove photoresist in warm chromic acid ($H_2SO_4 \cdot CrO_3$) — 10 min
9. Boiling DIW — 15 min

Once the p^- regions are defined, the impurity dopant must be introduced. For the low concentration p^- well, the technique of ion implantation is the most reproducible and controllable means of introducing the dopant. Boron ions are accelerated to an energy of 50 keV. The ion current is integrated and the number of ions reaching the wafer is accurately monitored. The dose used in the CMOS process is 1.13×10^{13} ions/cm^2 (figure 10). When this dose is diffused to a depth of 1×10^{-5} m (10 μ), the number of ions/cm^3 will be about 10^{16}. This dose is sufficiently large to counter-dope the n-type silicon, yet low enough to ensure high breakdown voltages between the n^+ p^- junctions. After implantation the ions are diffused into the silicon by means of a high temperature drive-in (figure 11).

P⁻ Predeposition and Drive-In

1. Ion Implant $^{11}B^{+}$ @ 52 keV total dose of $1.13 \times 10^{13}/cm^2$
2. Warm chromic acid — 10 min

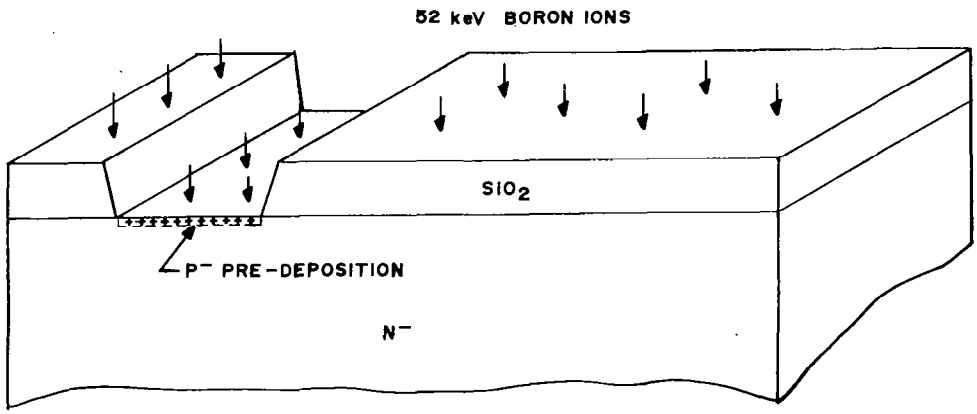

Figure 10. P⁻ deposition by implantation of boron ions.

3. Boiling DIW — 15 min
4. a. 1000°C Oxygen thru H_2O (97°C) ($O_2 \cdot H_2O$) — 70 min
   b. 1200°C N_2 — 16 hrs
   c. 1000°C O_2 thru H_2O (97°C) — 1 hr, 50 min

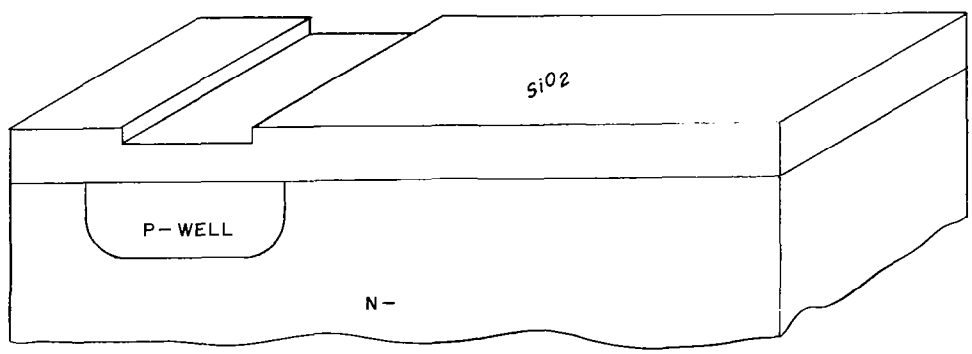

Figure 11. The p-dopant is driven in and the wafer is oxidized.

The next step (figures 12 and 13) is to define the p^+ regions corresponding to the source and drain of the p-channel transistors. The process of: (1) coating with photoresist; (2) mask alignment and exposure; (3) SiO_2 etching; and finally, (4) photoresist removal is repeated.

Since the source and drain are high concentration impurity regions, an alternate source of doping is used. Nitrogen gas is bubbled through boron tribromide (BBr_3) and routed into the furnace tube. A much higher dopant concentration is achieved in this manner (figure 14). The silicon wafers are placed in the middle of the tube. As the gas travels to the wafers, ionized boron is uniformly deposited. At this point the p^+ guard bands around the p^- regions (not shown) are created. The guard bands prevent leakage paths from one n-channel transistor to another. These paths arise from the low field threshold voltage associated with the <100> wafers.

P^+ Mask

1. Apply photoresist, 6×10^{-6} m (6000 A) thick
2. Bake on a 70°C hot plate — 15 min
3. Expose p^+ mask (UV light)
4. Develop, rinse, N_2 dry
5. Measure channel length, 7.62×10^{-6} m $\pm 7.62 \times 10^{-7}$ m (0.3 mil ±0.03 mil)
6. Post bake on a 120°C hot plate — 30 min

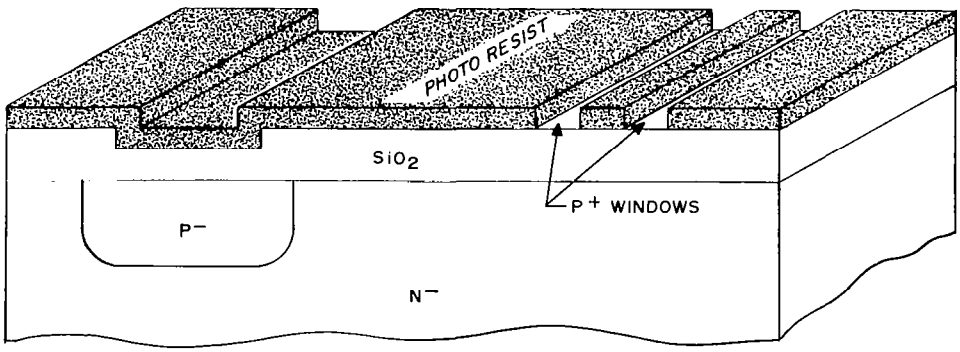

Figure 12. Photoresist deposition and the subsequent p^+ region definition.

7. Etch until oxide removed
8. Chromic acid 10 min
9. Boiling DIW 15 min

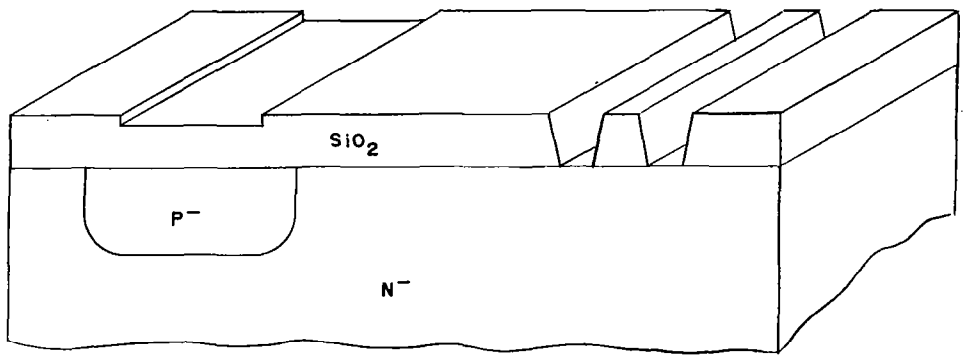

Figure 13. The oxide is etched and the photoresist is removed.

P^+ Predeposition

1. Pre-dope 980°C furnace tube with O_2 and N_2 bubbled through BBr_3 source 5 min
2. Turn off BBr_3, leave N_2 and O_2 on 5 min
3. Wafers placed in the tube for warm-up 5 min
4. BBr_3 turned on 2 min
5. BBr_3 off 5 min
6. Pull wafers

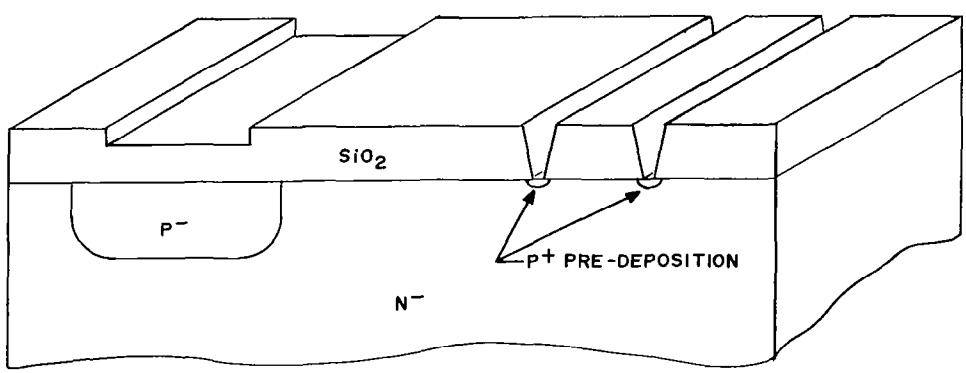

Figure 14. The p^+ regions are doped.

7. Wafers in 1200°C N_2 $C_S = 4 \times 10^{20}/cm^3$ 3 min

8. Wafers in 1000°C $O_2 \cdot H_2O$ 30 min

A layer of SiO_2 is grown over the doped p^+ regions (figure 15) and the windows for the n-channel source and drain are defined with the standard photolithographic technique (figures 16 and 17).

For the n-dopant, a $POCl_3$ source is used and phosphorus ions are deposited in a similar procedure to the boron predeposition (figure 18). The n^+ guard bands surrounding the p-channel transistors are introduced (not shown) to prevent leakage between p-channel transistors.

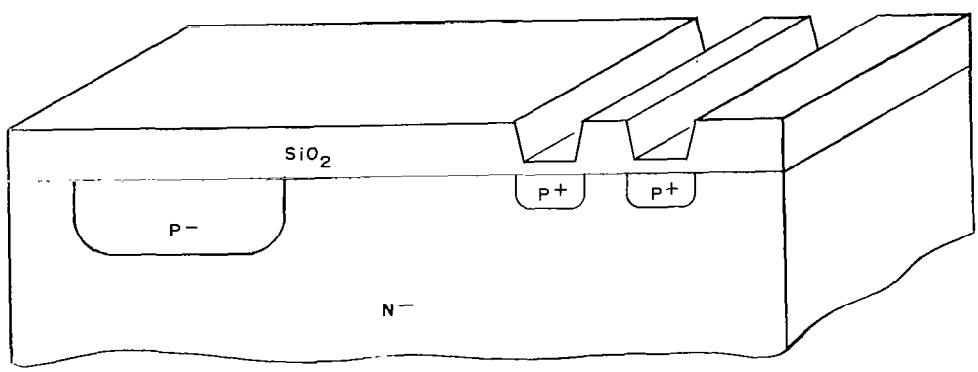

Figure 15. The p^+ regions are diffused and then oxidized.

N^+ Mask

1. Apply resist 6×10^{-7} m (6000 A) thick
2. Bake on a 70°C hot plate — 15 min
3. Expose N^+ mask
4. Develop, rinse, and N_2 dry

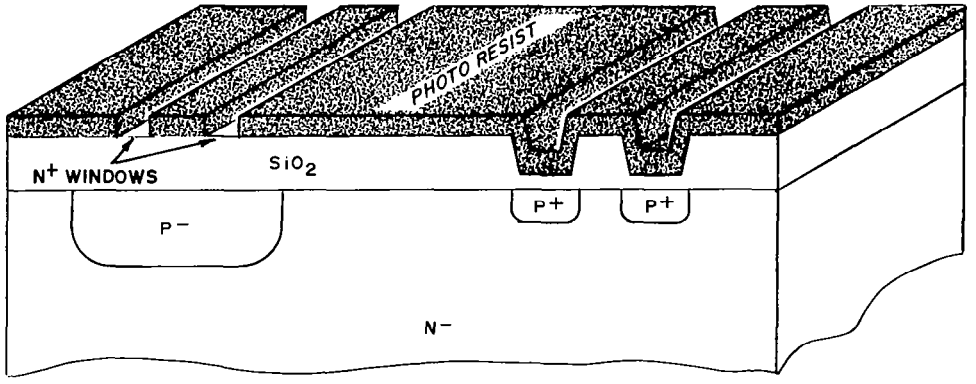

Figure 16. Wafers are coated with resist and the n^+ regions are defined.

5. Measure channel length 7.62×10^{-6} m $\pm 7.62 \times 10^{-7}$ m (0.3 mil ±0.03 mil)
6. Post bake on a 120°C hot plate — 30 min
7. Etch until oxide removed
8. Chromic acid — 10 min
9. Boiling DIW — 15 min

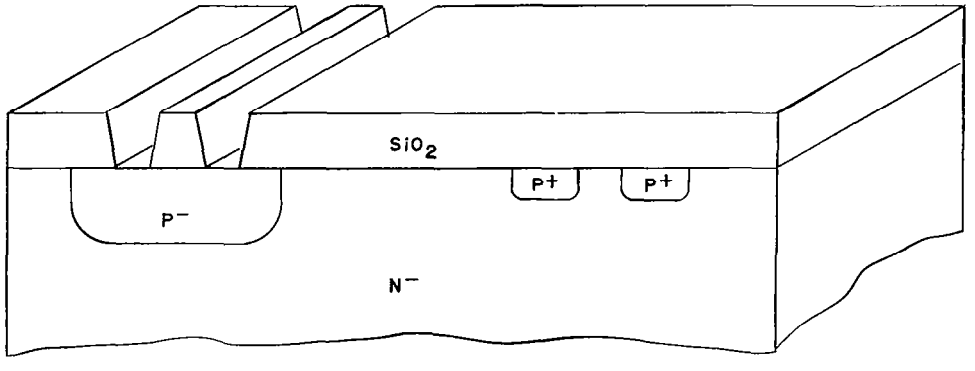

Figure 17. Wafers are etched and resist is stripped.

N^+ Predeposition

1.	Pre-dope 1000°C furnace tube with N_2 through $POCl_3$ and dry O_2	10 min
2.	Turn $POCl_3$ off	5 min
3.	Wafers placed in tube	1 min
4.	Turn $POCl_3$ on	1 min, 15 sec
5.	Turn $POCl_3$ off	3 min
6.	Turn O_2 off and turn N_2 on; $C_s = 1.5 \times 10^{20}/cm^3$	12 min
7.	Etch in buffered hydrofluoric acid	5 sec
8.	Boiling DIW	10 min
9.	Wafers in 1000°C $O_2 \cdot H_2O$	30 min

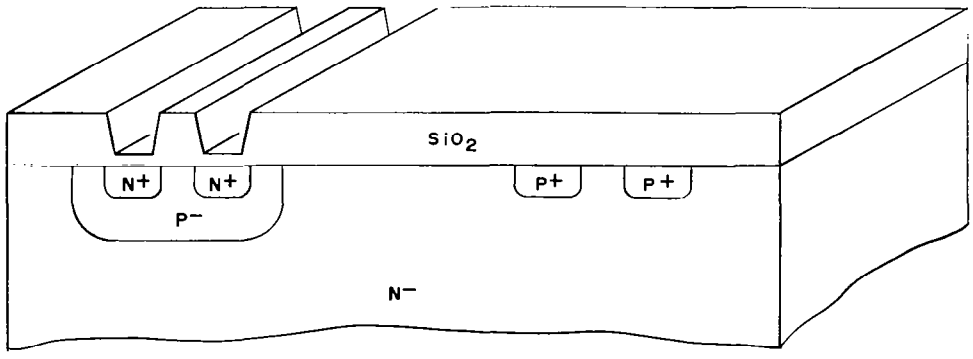

Figure 18. The n^+ regions are doped, diffused, and oxidized.

At this point, all the active regions have been properly defined and doped. The next step is to define the gate region area (figure 19) and grow the gate oxide. The entire active region is etched back to the silicon as shown in figure 20. An oxide 1.5×10^{-7} m (1500 A) thick is grown and removed to eliminate many of the impurities which result from the processing. The gate oxide is then grown in dry oxygen (figure 21). An annealing step follows which repairs much of the damage caused by the growth process occurring at the SiO_2 interface. Once the gate oxidation is completed, all that need be done is to expose the source and drain contact regions, evaporate aluminum, and define the metal interconnects.

Gate Etch Back Mask

1. Apply resist 6×10^{-7} m (6000 A) thick
2. Bake on a 70°C hot plate — 15 min
3. Expose etch back mask
4. Develop, rinse, and dry

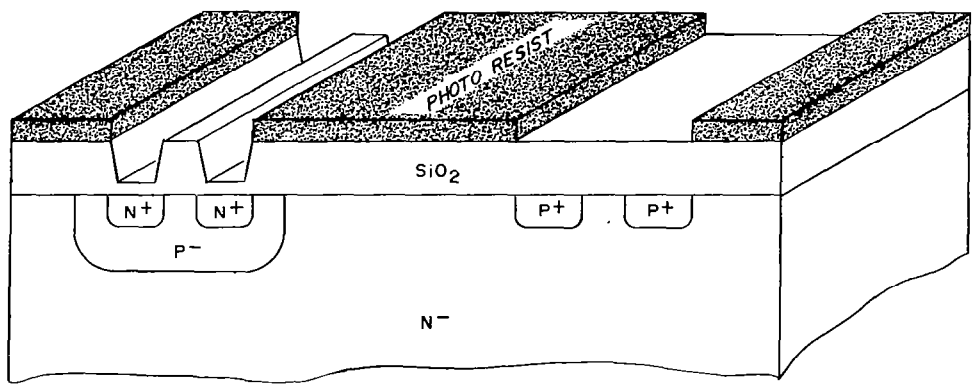

Figure 19. Photoresist is applied and the gate etch mask is exposed.

5. Post bake on a 120°C hot plate — 30 min
6. Etch until regions are clean plus an additional 16 min of undercutting
7. Chromic acid — 10 min
8. Boiling DIW — 15 min

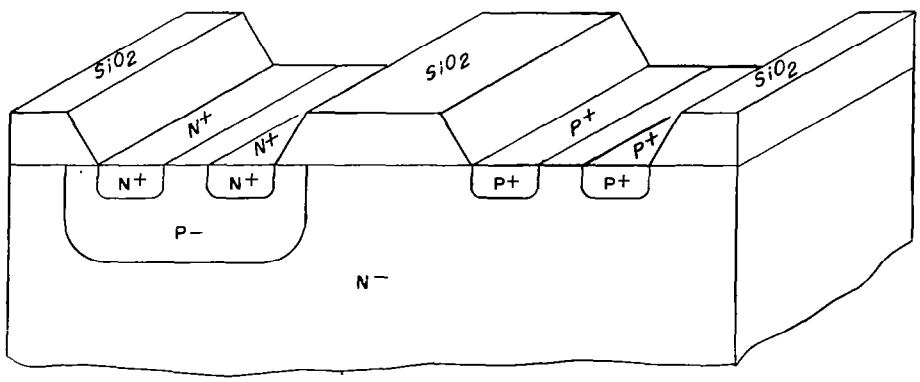

Figure 20. Wafers are etched and the resist is removed.

Pre-Gate Oxidation Clean-Up

1. Wafers in 1000°C O_2 · H_2O — 15 min
2. Etch wafers until backs are clean
3. Boiling DIW — 15 min

Gate Oxidation

1. a. 1000°C O_2 — 3 hrs
   b. 1000°C N_2 anneal — 45 min

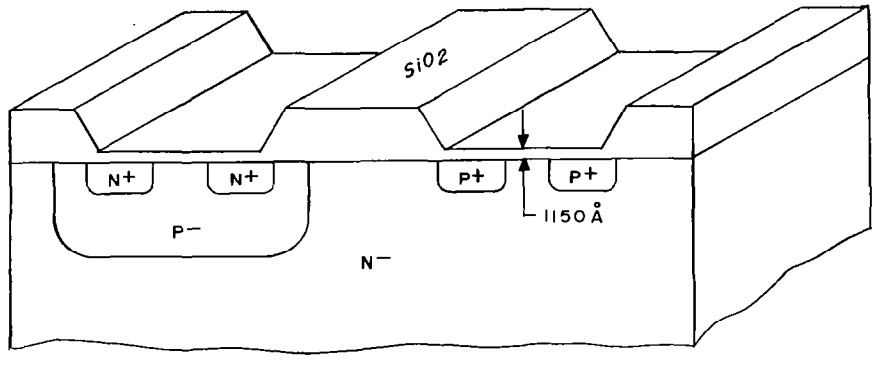

Figure 21. The gate oxide is grown.

It is at this point, after the gate oxidation, that thermal stability and correct threshold voltages are ensured. Thermal instabilities arise from impurities such as sodium and hydronium ions lodged in the gate oxide region. As the temperature is increased, these ions become mobile. When voltage is applied to the gate, these ions will migrate in the oxide electric field. If the sample is then cooled, these charges become fixed and may alter the threshold voltage. To counter this effect, phosphorus is introduced into the gate oxide, forming a phosphosilicate glass which traps the contaminants in the gate oxide and renders them immobile. The ion mobility is thereby reduced to an almost undetectable level.

There resides at the gate Si-SiO_2 interface, a fixed positive charge that tends to shift the threshold voltage of both transistors to a more negative value. In the case of the n-channel transistor, this can often lead to a depletion transistor: an entirely unacceptable situation. Ion implantation of boron through the gate oxide counters the effect of the positive oxide charge and increases the threshold voltage. Through accurate control of the implanted dose, the desired threshold voltage can be easily obtained. The ions are developed from a BF_3 gas source and are subjected to an accelerating potential of 52 keV. Approximately 37 keV is

required to penetrate the 11.5×10^{-8} m (1150 Å) gate oxide. The remaining 15 keV propels the ions about 8×10^{8} m (800 A) into the silicon crystal. Ions are only implanted where the oxide is thin enough to permit penetration. At 52 keV about 1.7×10^{-7} m (1700 A) of SiO_2 will mask the silicon from the ion beam. The total dose is controlled by integrating the beam current until the required charge is implanted. The dose can be controlled to within 1 percent of the desired value.

Normally, the n-channel transistor requires almost twice the dose needed for the p-channel transistor. The procedure then is to implant the entire silicon wafer with 2.16×10^{11} B^+ ion/cm^2. Once the first implant is accomplished the wafers are coated with 8×10^{-7} m (8000 A) photoresist. The p^- mask (the first mask) is printed but no etching occurs. This procedure reveals only the n-channel transistors leaving photoresist on the p-channel devices (figure 22). The wafers are then subjected to a second implant of 1.7×10^{11} ions/cm^2. The photoresist absorbs the ions, masking the p-channel devices from the beam. This technique is very effective in achieving individual n- and p-channel threshold control.

Application of Gettering Agent ($POCl_3$)

1.	Pre-dope 1000°C tube with N_2 bubbled through $POCl_3$ and O_2	10 min
2.	Turn $POCl_3$ off	5 min
3.	Place wafers in furnace	1 min
4.	$POCl_3$ on	1 min
5.	Turn $POCl_3$ off	10 min
6.	Turn O_2 off and N_2 on for 20 min as wafers are pulled from tube at one inch per min	

P- and N-Channel Transistor Implant for Threshold Voltage Adjustment

1.	Ion implant $^{11}B^+$ with 2.16×10^{11} ions/cm^2 @ 52 keV	
2.	Chromic rinse	10 min
3.	Boiling DIW	10 min
4.	1000°C N_2	1 min

N^+ Channel Transistor Implant

1.	Apply resist 8×10^{-7} m (8000 A) thick, 4K rpm	30s
2.	Bake on a 70°C hot plate	15 min

3. P^- mask exposure
4. Develop, rinse, and dry

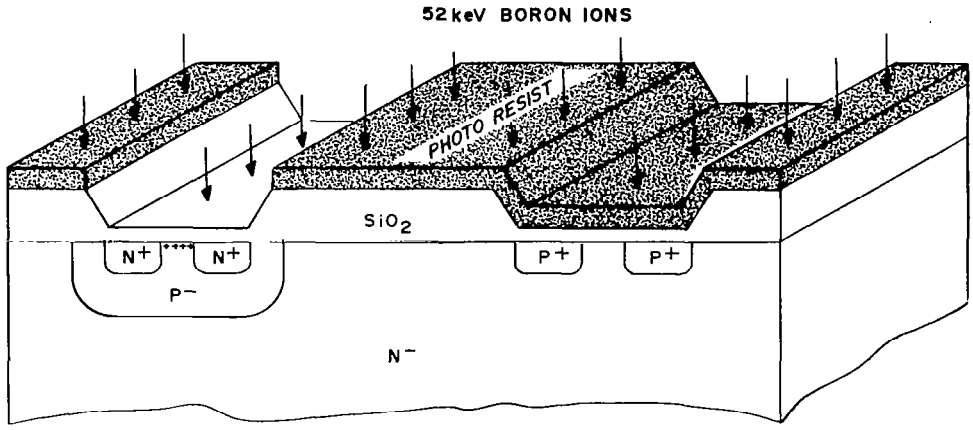

Figure 22. The p^- mask is used for n-channel implant.

5.	Post bake on a 120°C hot plate	30 min
6.	Ion implant $^{11}B^+$ with 1.7×10^{11} ion/cm^2 @ 52 keV	
7.	Chromic wash	10 min
8.	Boiling DIW	15 min
9.	Anneal oxide damage @ 850°C N_2	25 min

After the second implant the resist is stripped and the wafers are annealed to remove damage caused by the ions passing through the oxide. The contact mask is used to define the areas where the metal will contact the diffusions. The same photolithographic process is repeated exposing the silicon as shown in figures 23 and 24. The wafers are cleaned in a chelating agent to remove any heavy metals that may be present.

Contact Mask

1. Apply resist 6×10^{-7} m (6000 A) thick
2. Bake on a 70°C hot plate — 15 min
3. Contact mask exposure
4. Develop, rinse, and dry

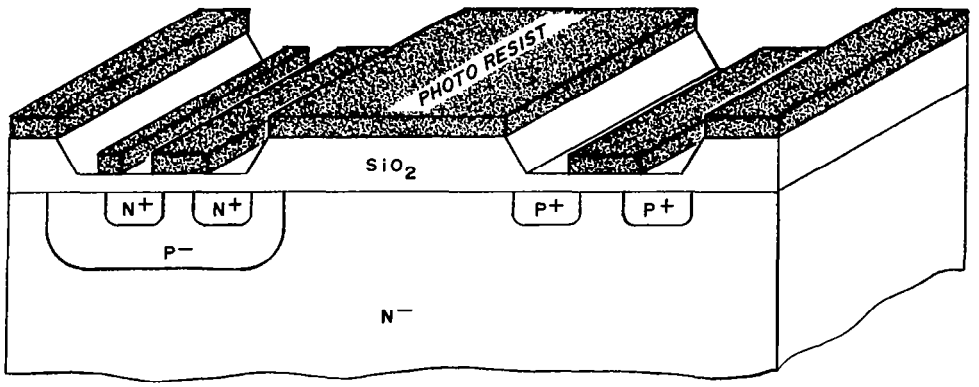

Figure 23. Resist is applied and the contact areas are exposed.

5. Post bake on a 120°C hot plate — 30 min
6. Etch until back is clean
7. Chromic acid — 10 min
8. Boiling DIW — 5 min
9. Immersion in chelating agent — 15 min

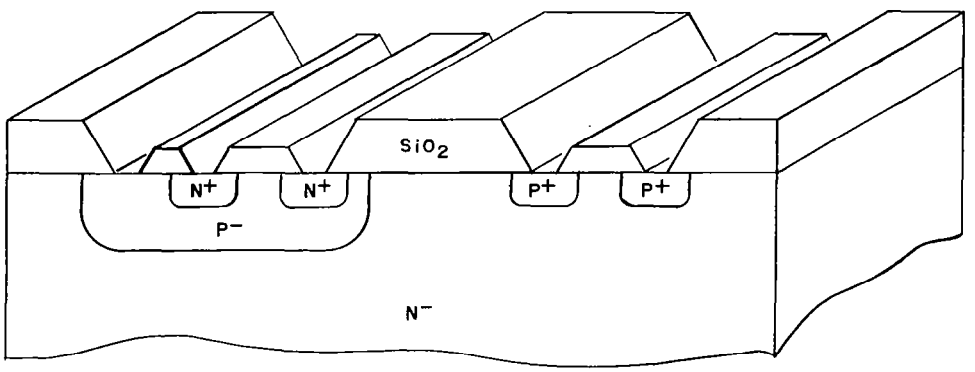

Figure 24. Contact areas are etched and the resist is removed.

The final step is the aluminum deposition (figure 25). The wafers are placed in a vacuum system and pumped down to 1.33×10^{-4} m (10^{-6} torr). Aluminum is heated by an electron beam and evaporates onto the wafers. As evaporation occurs, the wafers are rotating in a planetary motion. After the correct thickness is deposited, about 11×10^{-7} m (11,000 A), the wafers are removed and stored until the desired metal pattern is needed. When ready to define the metallization, the photographic process is repeated (figure 26) and the metal is etched using Metex Aurostrip, a cynanide-based compound. The photoresist is removed by strong agitation in warm chromic acid for a short time. After rinsing in cold deionized water, the wafers are alloyed to ensure good ohmic contact.

The individual electrical parameters are checked on each wafer and those that are acceptable are coated with a 3×10^{-7} m (3000 A) layer of silox (deposited SiO_2). Only the bonding pads are exposed leaving a passivation layer on the rest of the circuit. The integrated circuits are then ready for functional testing.

Metal Deposition

1. E-beam evaporation or flash evaporation of aluminum
   @ 2.67×10^{-4} m (2×10^{-6} torr), 1.05×10^{-6} m (10,500 A) thick

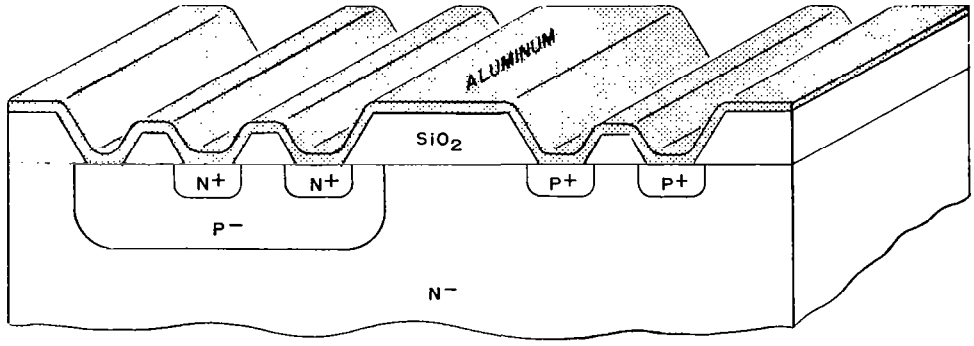

Figure 25. The wafers are coated with aluminum.

2. Store fixed-gate array wafers in N_2 cabinet until needed. When needed, proceed as follows:

Metal Definition

1.	Apply resist 4×10^{-7} m (4000 A) thick, spin @ 8000 rpm	30 s
2.	Bake on a 70°C hot plate	
3.	Expose appropriate metal mask (low UV intensity, long exposure time)	
4.	Develop, rinse, and dry	
5.	Bake on a 120°C hot plate	30 min
6.	Etch in aurostrip until aluminum is removed	
7.	Rapid dips in warm chromic acid	1 min
8.	Cold DIW rinse	5 min
9.	Alloy @ 490°C in N_2	10 min

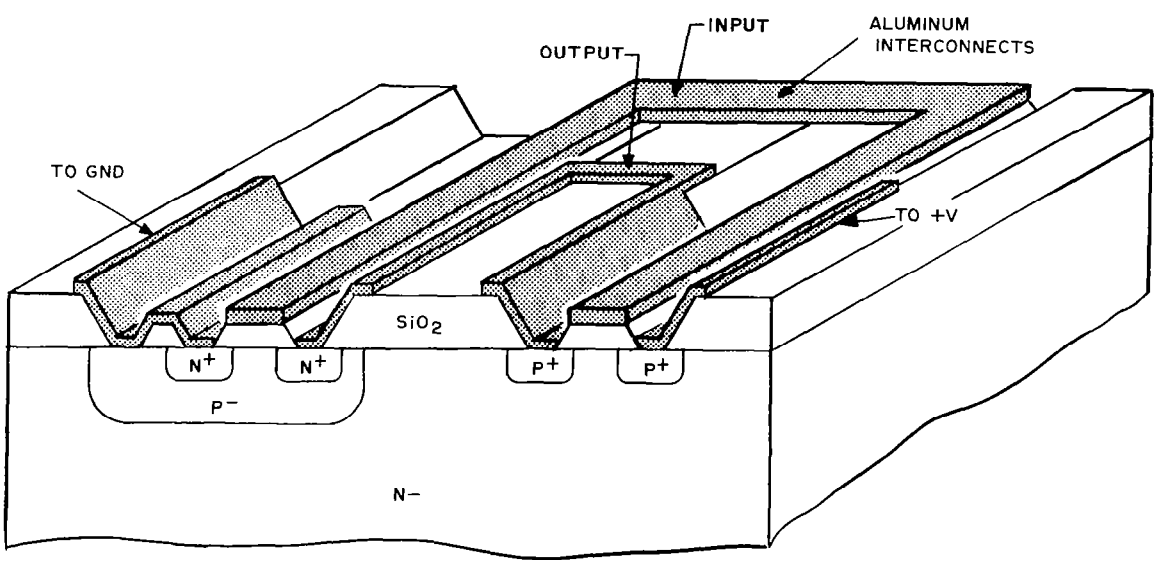

Figure 26. The metal pattern is defined and the aluminum is etched away, forming the CMOS inverter.

Passivation

1.	Heat wafers to 450°C	
2.	Deposit n-doped silox, 3×10^{-7} m (3000 A)	
3.	Apply resist 6×10^{-7} m (6000 Å) thick	
4.	Bake on a 70°C hot plate	15 min
5.	Expose glass passivation mask (exposing bonding pads only)	
6.	Develop, rinse and dry	
7.	Post bake on a 120°C hot plate	30 min
8.	Etch until silox removed	2 min
9.	Remove photoresist	

CONCLUSION

Using this CMOS process, 2-inch wafers with large scale integration, e.g., fixed-gate array circuits, have been fabricated with circuit yields of up to 60 percent. Circuit yields of over 90 percent have been achieved for small scale integration, e.g., a 631 octal inverter. This process has consistently produced thermally stable, parametrically acceptable wafers for the past eighteen months. Further investigation is expected to result in a similar CMOS process with a substantial improvement in radiation hardness.

In addition to CMOS, the Microelectronics Development Section at GSFC is undertaking many other semiconductor projects. Silicon gate charge-coupled devices have been developed and are being studied for signal processing and imaging applications. Double-diffused MOS (DMOS) and V-groove MOS (VMOS) transistors have also been developed and are currently being evaluated as a supplement to the CMOS integrated circuit family where high-speed, radiation-hard devices are required. Another area being studied is millimeter wave devices such as gallium arsenide Schottky barrier diodes. These diodes have application in high-frequency radiometric studies.

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National Aeronautics and Space Administration
Greenbelt, Maryland

REFERENCES

1. COS/MOS Integrated Circuits, RCA, 1975 Data Book Series.

2. Dawes, W. R., G. E. Derbenwick, and B. L. Gregory, *J. of Solid State Circuits*, SC-11, 459, 1976.

APPENDIX

CHEMICAL SOLUTIONS AND GAS FLOWS

Chemicals

Buffered HF	435×10^{-6} m^3 (435 ml) HF + 1.27 kg NH_3F + 1.9 kg H_2O
Chromic acid	80 gm CrO_3 + 4.08 kg H_2SO_4
Chelating agent and Aluminum etchant	Metex Aurostrip (Proprietary) 64 gm Aurostrip in 1 ℓ H_2O
Photoresist	Kodak 747 microresist
Developer	Kodak microresist developer
Rinse	Kodak microresist rinse
Deionized water	18 megohm-cm

Gases

Boron (P-dopant)	
BN wafers	Grade A type. N_2 flow of 425 cc/min. BN wafers are oxidized in O_2 , 425 cc/min for 15 min every 2 weeks.
BBr_3	10 cc/min N_2 bubbled through BBr_3 . 1720 cc/min N_2 and 2 cc/min O_2 are used as carrier gases.
Phosphorus (n-dopant)	
$POCl_3$	39 cc/min of N_2 bubbled through $POCl_3$. 700 cc/min N_2 and 136 cc/min O_2 used as carrier gases.
Silox Deposition (n-doped)	3.2% SiH_4 in N_2 total flow of 656 cc/min; 400 cc/min O_2 ; 45 ℓ/min N_2 ; 200 cc/min Phosphine (PH_3).
O_2 for oxidation	425 cc/min
N_2 for anneal	425 cc/min