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TECHNICAL MEMORANDUM NASA 46

ANALYSIS OF A FIRST ORDER PHASE LOCKED LOOP  
IN THE PRESENCE OF GAUSSIAN NOISE

A first-order digital phase locked loop is analyzed by application of a Markov chain model. Steady-state loop error probabilities, phase standard deviation and mean loop transient times are determined for various input signal-to-noise ratios. In addition, results for direct loop simulation are presented for comparison.

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March 1977



Supported by

National Aeronautics and Space Administration  
Langley Research Center  
Hampton, Virginia  
Grant NGR 36-009-017

## I. CONCLUSIONS AND OBSERVATIONS

A specific first-order phase locked loop has been modeled as a first-order Markov process and the appropriate analysis carried out to determine the steady-state probabilities of the loop's phase states, the standard deviation of the loop's output phase and the mean time to lock for some known initial phase offset. The comparison of these values for a particular loop configuration with values obtained by simulation of the loop indicate that the proposed model is valid. The state diagram itself is not limited to the case of independent input samples but the analysis would have to be carried out for an  $n^{\text{th}}$  order Markov process if the samples are not statistically independent.

The model as presented is limited to a first-order phase locked loop by the fact that the state diagram allows transitions only to adjacent states. If the state diagram allowed transitions to states other than only the adjacent states then a second-order loop results. However, the transition probabilities must be such that the matrix of transition probabilities is stochastic if the analytic techniques described in the previous sections are to be of value.

## II. INTRODUCTION

Digital phase locked loops are of particular interest because of the inherent ease with which they can be designed and constructed. However, little is known about the output phase characteristics of DPLL's when the input signal is corrupted by noise. In [1], a class of DPLL's was subjected to a noise analysis but simplifying assumptions made limit the usefulness of the results to small values of phase error only. In [2] and [3], specific DPLL configurations were analyzed utilizing random-walk techniques. A DPLL is described in the following that achieves the same statistical curve characteristics but less physical complexity than that described in [3].

The following deals with a specific first-order DPLL configuration and utilizes the theory of first order Markov processes in the analysis. The specific loop configuration used is that of the Ohio University MAPLL [4] with the exception that the loop is assumed to operate continuously instead of in a gated manner. The main thrust of this paper is to present a method of analysis for this loop configuration (and many similar loop configurations) and not necessarily to provide a detailed design for any particular DPLL application. As an example of the usefulness of the approach, results are provided for a DPLL whose output phase is quantized to 32 distinct values. Results are also provided for a DPLL simulation as a check on the correctness of the analytic method.

## III. MARKOV CHAIN MODEL FOR A DPLL

Consider the first-order digital phase locked loop of Figure 1. For this loop, the reference clock is the same frequency as the incoming signal  $s(t)$  and can take on  $N$  distinct phases defined between 0 and  $2\pi$ . These values are spaced  $2\pi/N$  radians apart. The operation of the phase detector is to sample the incoming signal at a time coincident

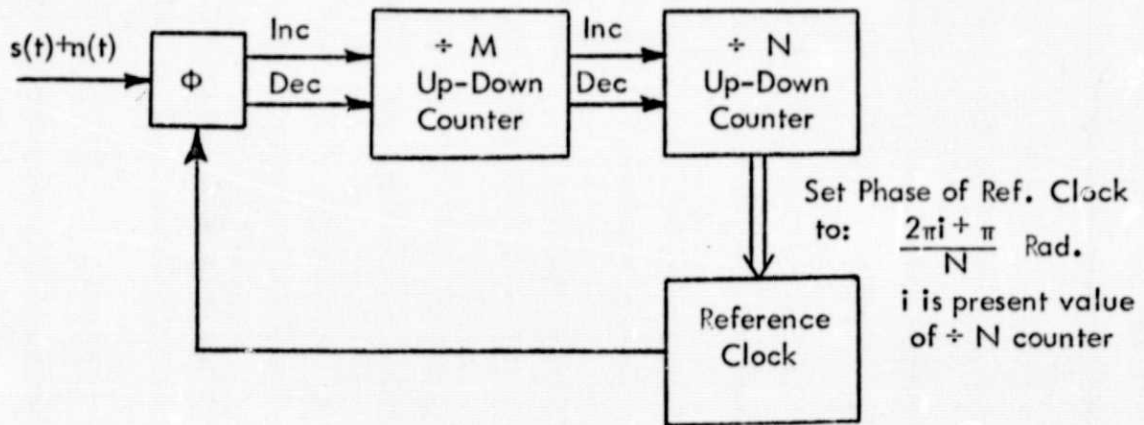


Figure 1. Block Diagram of First-Order DPLL.

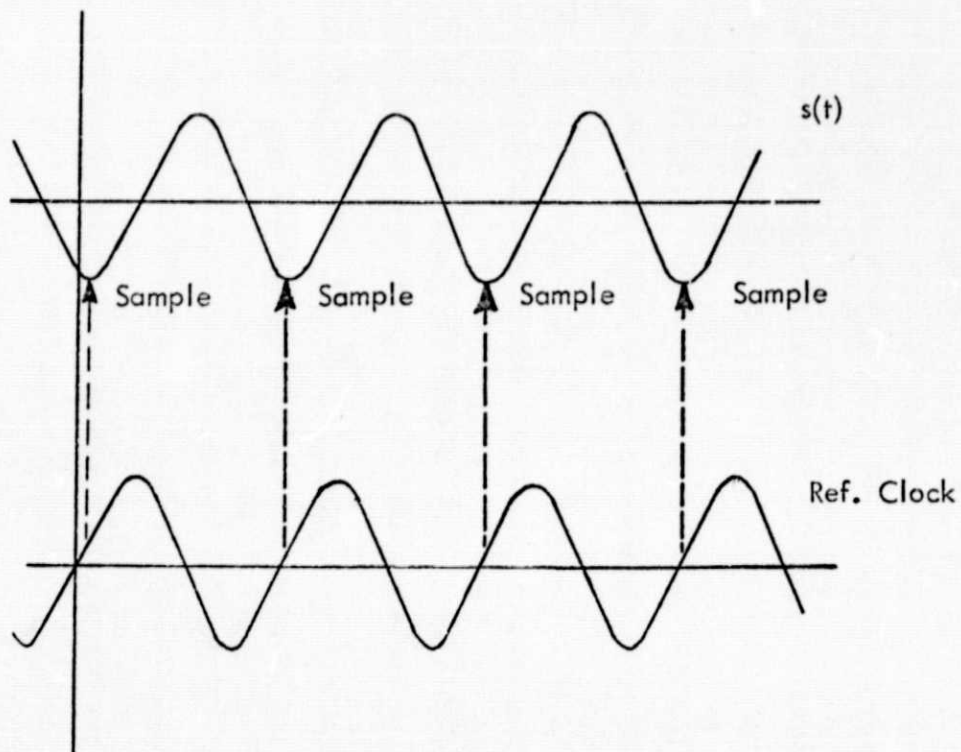


Figure 2. DPLL Waveform Sampling.

with the positive going zero crossing of the reference clock and provide an output based on the sign of the sampled value. See Figure 2. If the sample value of the incoming signal is less than zero, the phase detector provides an increment output and if the sample value is greater than zero, a decrement output. Assume that the divide-by M and the divide-by N counters are initially zero and the random noise is zero and the incoming signal phase lags the reference clock phase. The sampled value then is less than zero so that the phase detector output causes the divide-by M counter to increment one count. Since the value of the divide-by N counter does not change, the next sample will also be less than zero again causing the divide-by M counter to increment one count. This continues until the divide-by M counter overflows and thus increments the divide-by N counter by one count which in turn retards the phase of the reference clock by  $2\pi/N$  radians. The divide-by N counter is thus successively incremented until the reference clock phase lags the incoming signal phase at which time the phase detector samples are now positive causing the divide-by M counter to decrement one count for each such sample taken. The loop then is in lock and the reference clock phase is equal to the incoming signal phase within the quantization error.

From the preceding, it is obvious that to change the phase of the reference clock it is necessary for the divide-by M counter to cycle through its M distinct states to either an overflow or underflow condition. Thus while the phase output takes on N distinct states, the loop itself has  $M \times N$  distinct states. A state diagram for the loop is given in Figure 3 where the  $p_i$ 's and the  $q_j$ 's are the probabilities associated with the indicated state changes. More will be said about these values in a moment. Several things are worth noting about this state diagram. First, for any present state, when a new sample is taken a new state will result; and second, the new state will always be "adjacent" to the previous state. Also, for a given reference clock state the transitions occur uniformly with time but, following a transition from one reference clock state to another, the time interval to the next sample is either longer or shorter than the time interval between the previous two samples depending on whether the reference clock phase was advanced or retarded as it passed from the previous reference clock state to the present reference clock state.

Assume that the input to the DPLL is

$$s_r(t) = s(t) + n(t) \\ = A_c \cos(\omega_c t + \psi) + x(t)\cos \omega_c t + y(t)\sin \omega_c t$$

where  $A_c$  is the carrier amplitude and  $x(t)$  and  $y(t)$  are zero mean independent gaussian distributed random processes of bandwidth B and variance  $\sigma_x^2 = \sigma_y^2 = \sigma^2$ . That is, the input to the DPLL is some signal plus narrowband noise. The input can also be written in the form:

$$s_r(t) = x^e(t)\cos \omega_c t + y^e(t)\sin \omega_c t$$

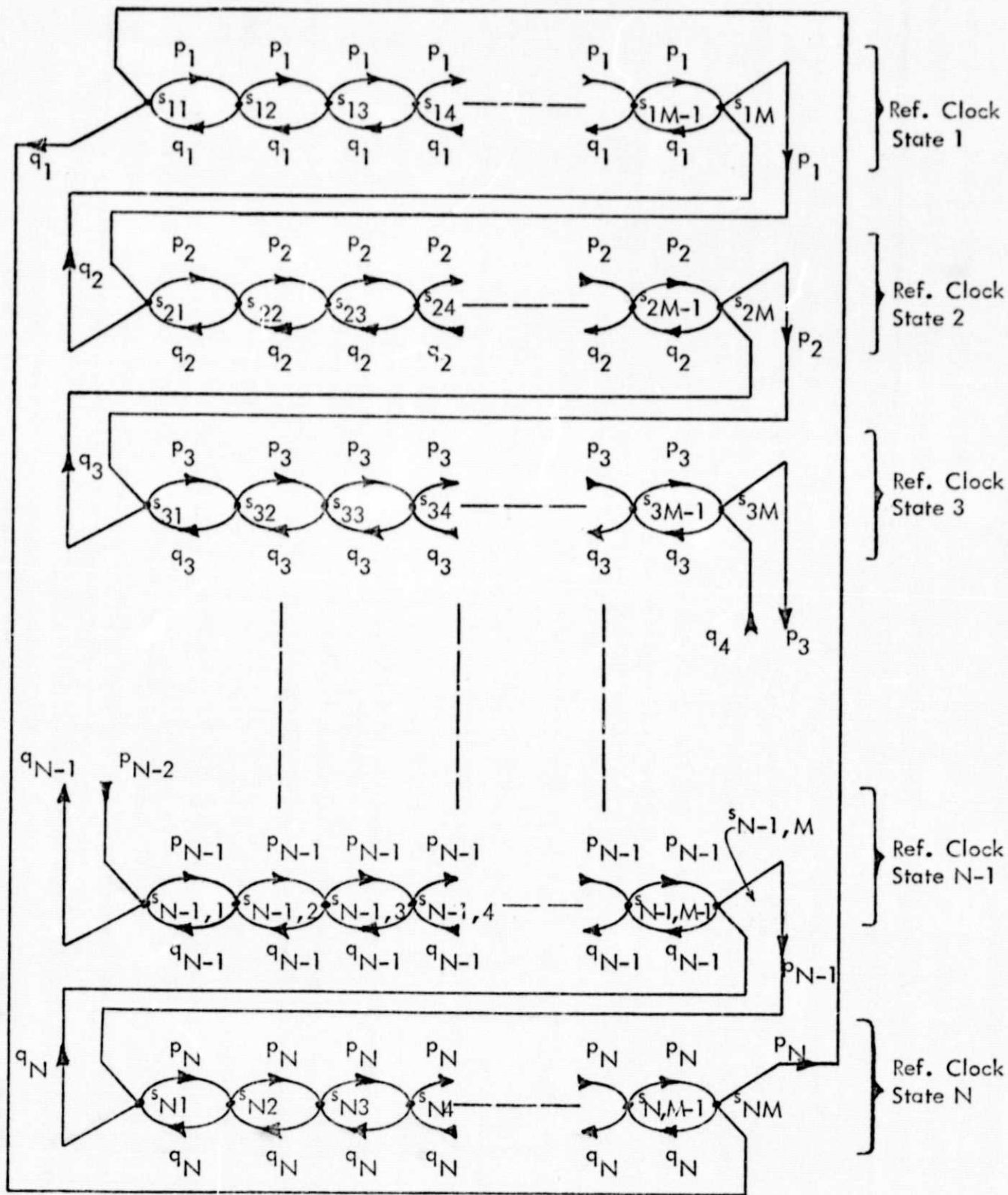


Figure 3. First-Order DPLL State Diagram.

where

$$\begin{aligned}x'(t) &= x(t) + A_c \cos \psi \\y'(t) &= y(t) + A_c \sin \psi\end{aligned}$$

The positive going zero crossing is always assumed to be the correct phase of the signal  $s(t)$ . That is, the reference clock is always assumed to be in phase lock with the signal  $s(t)$ , and the error signal generated by the phase detector is used to tell the loop differently. Therefore, the loop always assumes the samples of the incoming signal occur at:

$$\omega_c t_i = (1 + 2i)\pi/2 \quad i = 0, 1, 2, \dots$$

so that

$$\cos \omega_c t = 0$$

$$\sin \omega_c t = 1$$

giving

$$s_r(t) = y(t) + A_c \sin \psi$$

where  $\psi$  is the phase difference between  $s(t)$  and the reference clock. Note that as the loop approaches lock,  $\psi$  approaches 0. Also, the reference clock can take on only  $N$  distinct values so that  $\psi$  too can take on only  $N$  distinct values  $\psi_i, i = 1, 2, \dots, N$ . From earlier  $y(t)$  is a gaussian distributed random process so that the probability density function for  $s_r(t)$  is:

$$p(s_r) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{1}{2} \frac{(y + A_c \sin \psi_i)^2}{\sigma^2}}$$

From the state diagram of Figure 3, the  $p_i$ 's are the probability that the sampled value of  $s_r(t)$  is less than zero and can be found from:

$$\begin{aligned}p_i &= \int_{-\infty}^0 p(s_r | \psi_i) ds_r \\ &= \frac{1}{\sqrt{2\pi\sigma^2}} \int_{-\infty}^0 e^{-\frac{1}{2} \left[ \frac{y + A_c \sin \psi_i}{\sigma} \right]^2} dy \\ &= \text{probability that } s_r(t) \leq 0\end{aligned}$$





Or,

$$[P] [a] = [a]$$

where P is called the matrix of transition probabilities. The non-trivial solution to this system of homogeneous, linear equations is the one that satisfies:

$$\sum_{i=1}^N \sum_{j=1}^M a_{ij} = 1$$

and, from the characteristics of Markov chains, represents the steady-state probabilities for the loop states. That is, at any given instant of time the probability of observing the loop in state  $s_{ij}$  is given by  $a_{ij}$ . The steady-state probabilities for the reference clock states,  $S_i$ , are given by:

$$S_i = \sum_{j=1}^M a_{ij} \quad i = 1, 2, \dots, N$$

Once the steady-state reference clock state probabilities are known, it is possible to find the variance of the reference clock phase from:

$$\sigma_{\psi}^2 = \sum_{i=1}^N S_i [(\pi/N)(1 + 2i)]^2$$

where it has been assumed that the phase of the incoming signal  $s(t)$  is  $\pi$  radians.

Another quantity useful for the evaluation of a DPLL is the mean time to lock-up for some initial phase offset. To evaluate this, the Markov chain approximation is again used. Let  $p_{ij}$  be the  $ij^{\text{th}}$  element of [P] and renumber the loop states  $s_{ij}$  by consecutively numbered subscripts as:

$$\begin{aligned} s_{11} &= s_1 \\ s_{12} &= s_2 \\ &\vdots \\ &\vdots \\ s_{NM} &= s_{(N*M)} \end{aligned}$$

Then if the system starts in state  $s_i$ , the waiting time up to the first passage through state  $s_j$  has a distribution  $f_{ij}^{(n)}$ . That is,  $f_{ij}^{(n)}$  is the probability that starting in state  $s_i$ , the first occurrence of state  $s_j$  is at time  $n$ . The values of  $f_{ij}^{(n)}$  can be found from:

$$f_{ij}^{(1)} = p_{ij}$$

and

$$f_{ij}^{(n)} = p_{ij}^{(n)} - \sum_{k=1}^{n-1} f_{ij}^{(n-k)} p_{ij}^{(k)}$$

where  $p_{ij}^{(k)}$  is the  $ij$ <sup>th</sup> element of  $P^k$ . The mean time to the first occurrence of  $s_j$  if the initial state is  $s_i$  then is:

$$\mu_{ij} = \sum_{n=1}^{\infty} n f_{ij}^{(n)}$$

For the dimension of the square matrix  $P$  on the order of 500X500 (for instance  $N = 64$  and  $M = 8$ ) the determination of the elements of  $P^k$  directly is time consuming even when implemented for computer solution. Therefore, alternate methods to determine  $p_{ij}^{(k)}$  are desired. One method of solution is to form a generating function as outlined by Feller [5]. While this method results in a function that allows the evaluation of  $p_{ij}^{(k)}$  as a function of  $k$ , it involves the solution of two sets of  $n \times n$  simultaneous equations and the determination of the roots of a  $n^{\text{th}}$  order polynomial. Another method of solution would be to find the eigenvalues and eigenvectors of matrix  $P$  and convert it to Jordan canonical form by similarity transforms. Then the higher powers of the Jordan canonical form matrix could be easily found with  $p_{ij}^{(k)}$  determined from the inverse transform. Note, it is not required to find all the elements of  $P^k$ . This method is attractive from the standpoint that literature concerning the determination of eigenvalues and eigenvectors is readily available.

A more direct method for finding the mean time to the occurrence of  $s_j$  given present state  $s_i$  is suggested by Feller [5] and derived by Cessna and Levy [3]. As in [3], let  $T_o(i)$  be the expected value of time to reach minimum phase error when the initial state is state  $i$ . Then  $T_o(i)$  satisfies the following difference equation:

$$T_o(i) = T(i) + p(i) * T_o(i-1) + q(i) * T_o(i+1)$$

with boundary conditions  $T_o(0) = 0$  and  $T(i)$  the expected duration of state  $i$ . For the State diagram of Figure 3,  $T(i) = 1$ . Thus, a set of non-homogeneous linear simultaneous equations has been defined, the solution of which is readily found.

#### IV. APPLICATION OF THE MARKOV CHAIN MODEL

The steady-state probabilities for different values of  $M$  and  $N$  were found by a successive approximation algorithm in a computer program. An envelope of the steady-state probabilities for  $N = 32$  and  $M = 4$  is shown in Figure 4 for signal-to-noise ratios of 0 dB and -20 dB. Notice that at the decreased signal-to-noise ratio the density function's peak is down and the function has "flattened out" considerably. This is expected since the noise has become more significant making the steady-state probabilities more nearly equal.

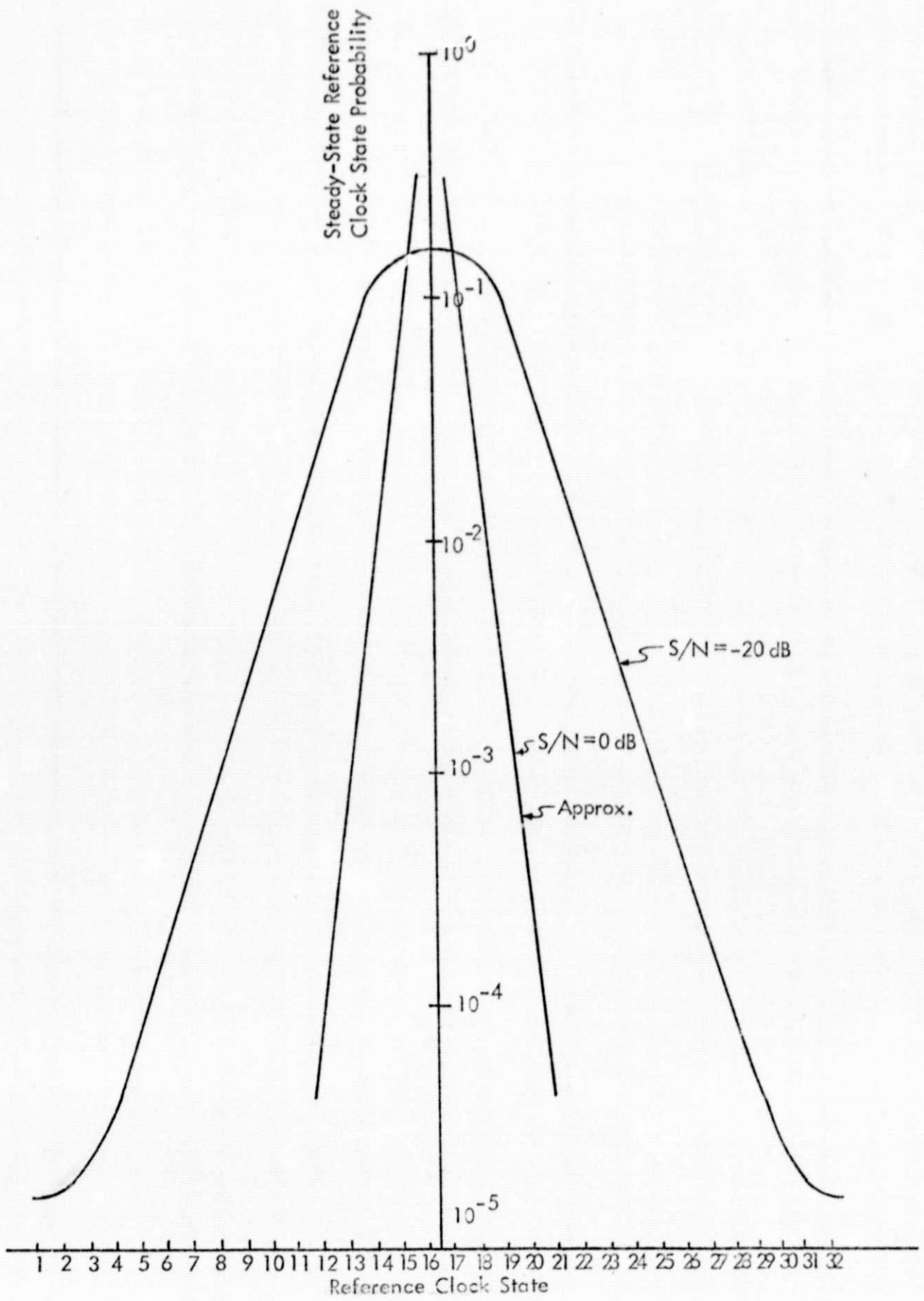


Figure 4. First-Order DPLL Output Phase Probability Density Function.

Once the steady-state probabilities are determined the phase variance (or standard deviation) can be easily calculated. For  $N = 32$  and  $M = 4, 8, \text{ and } 16$ , the phase standard deviation versus signal-to-noise ratio were calculated. The results are plotted in Figure 5. Note, these curves are plotted for noise-to-signal ratios. For low values of noise-to-signal ratio, the curves are asymptotic to a value fixed by  $N$ , the quantization level of the reference clock phase. For high values of noise-to-signal ratio the curves are asymptotic to the standard deviation of a uniform phase distribution. This is caused by the flattening of the phase density function as the noise-to-signal ratio increases. Simulation results for  $N = 32$ ,  $M = 4$  are also provided in Figure 5. These show close agreement to the theoretical results.

The mean time to loop lock-up in terms of the number of samples required was determined by solving the difference equation given previously. The values of  $M$  and  $N$  were fixed to 4 and 32, respectively, so that the loop had 128 states and the incoming signal phase was assumed to be  $\pi$  radians so that loop lock occurred in either states  $s_{64}$  or  $s_{65}$ . The boundary conditions for the difference equations then are  $T_0(64)$  and  $T_0(65)$  equals zero. This set of difference equations was solved by a successive approximation technique for different values of signal-to-noise ratio and the results are plotted in Figure 6. As expected for a given initial phase offset, the mean number of samples required to achieve phase lock increases as signal-to-noise ratio decreases. Notice that for a 20 dB signal-to-noise ratio that the expected time to lock is very nearly that of the noiseless case. That is, for the maximum error between the input phase and the DPLL, the DPLL would have to step through 63 transitions to reach the lock state and Figure 6 indicates that for 20.0 dB the expected number of samples required is 64.2. Figure 7 is a similar plot except that the signal-to-noise ratio was held constant and the value of  $M$  was set to both 4 and 8. From this plot, for a fixed signal-to-noise ratio and a fixed phase offset, the mean time to lock increases as the number of states increases. Simulation results are also provided in Figure 6 for  $M = 4$ ,  $N = 32$ . The mean time to lock for the simulation shows close agreement with the theoretical results.

## V. REFERENCES

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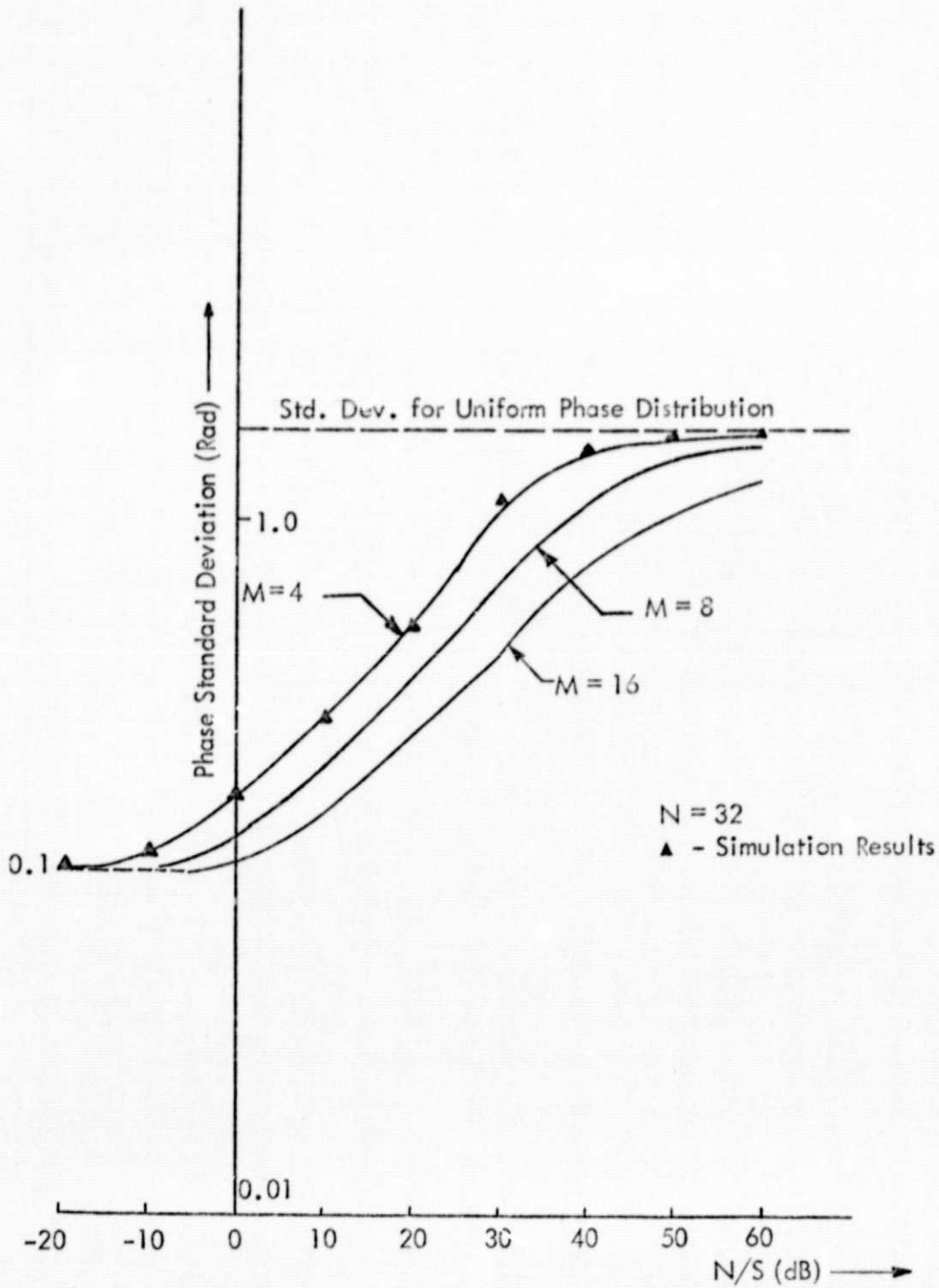


Figure 5. Standard Deviation of Phase Output of DPLL.

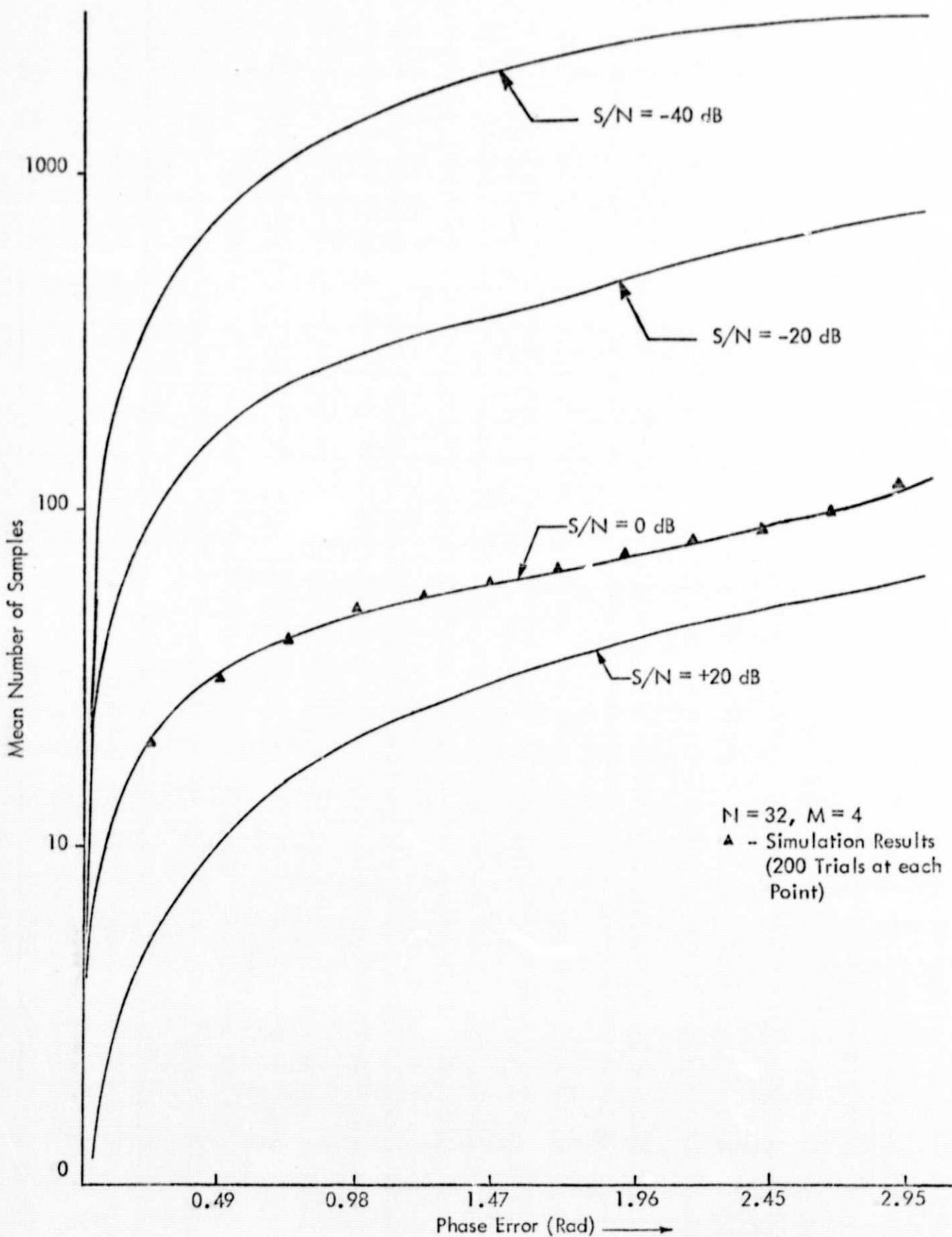


Figure 6. Mean Time to Loop Lock-Up Versus Initial Phase Error.

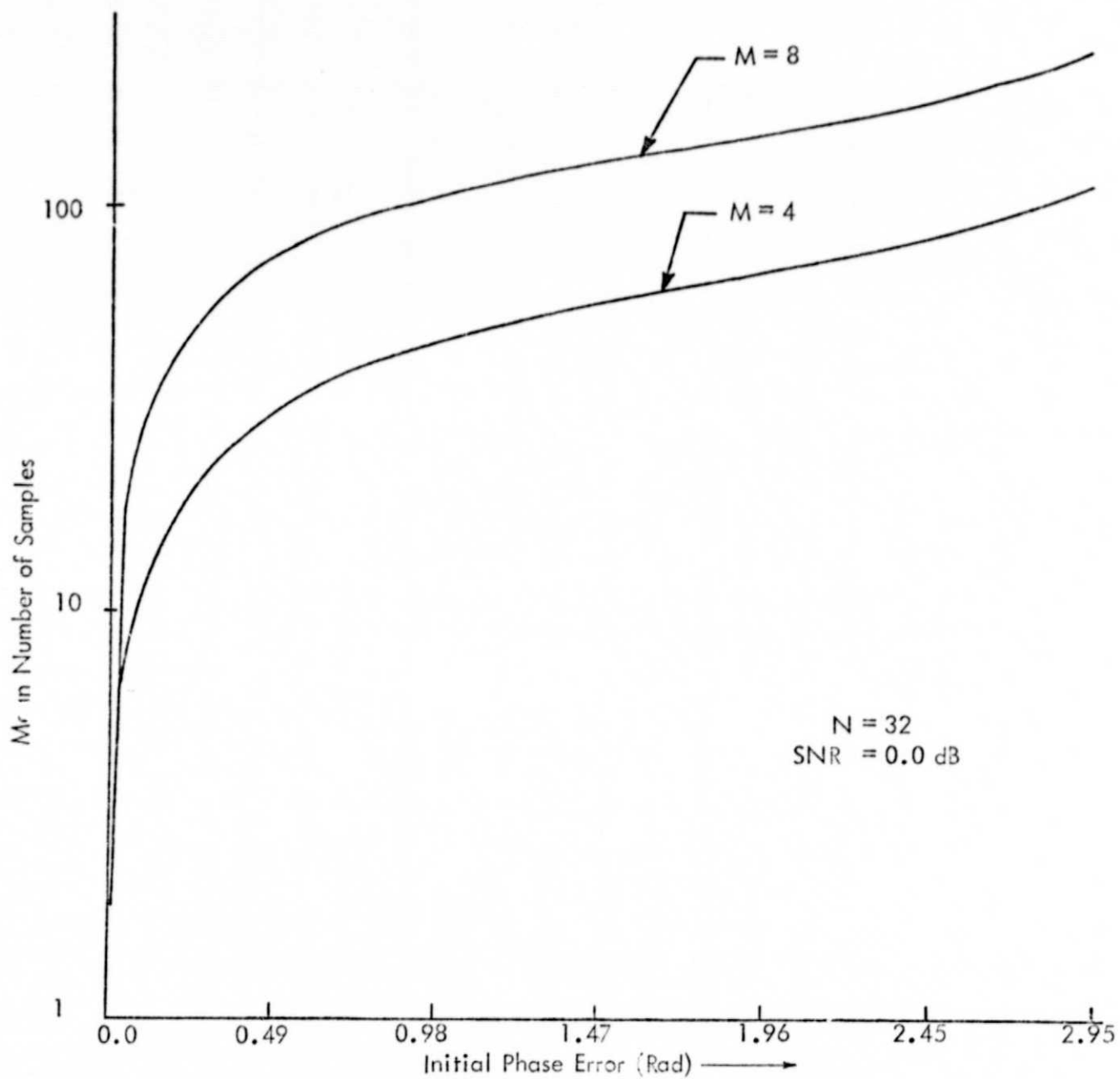


Figure 7. Mean Time to Loop Lock-Up Versus Initial Phase Error.