ACCELERATED LIFE TESTING EFFECT ON CMOS MICROCIRCUIT CHARACTERISTICS

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ACCELERATED LIFE TESTING EFFECTS ON CMOS MICROCIRCUIT CHARACTERISTICS

Phase I Report

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By

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Prepared By

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ABSTRACT

This report describes the work performed under NASA contract NAS8-31905 by the RCA Solid State Division, Somerville, N.J. facility and the integrated-circuits manufacturing facility in Findlay, Ohio. This report covers Phase I of the contract and the time period from May 1976 to December 1976.

In order for the results from Phase I (250°C) to be meaningful, data generated from Phase II (200°C) and Phase III (125°C) must be considered. This data, although preliminary, is included in this report. Subsequent reports will tie the data from all three phases of this contract together so that meaningful analyses and recommendations can be made.

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SECTION I
INTRODUCTION

The need for a practical short-term test program, the results of which can be meaningfully interpreted to predict the long-term reliability of CMOS microcircuits, has been recognized. Many months if not years are required to run a life test under conditions reflecting actual applications and requirements of Class A devices. The impracticality of such a test led to the reliance by the industry on long-term reliability predictions based on interpolations of results gathered from accelerated life tests. It is essential to run long (thousands of hours) 125°C life tests to confirm experimentally the validity of such interpolations for CMOS devices. There is a definite possibility that accelerated tests cause the temperature thresholds of a device to be exceeded, thus triggering failure mechanisms unrelated to a device's operation within its specified ratings. The somewhat arbitrary limits established for the use of accelerated life tests must be either experimentally confirmed or revised in accordance with experimental data. The varying complexity of present day CMOS devices should be recognized as a factor in reliability predictions.

The purpose of this program is to determine the consistency of the CMOS microcircuit activation energy between the range of 125°C to 200°C and the range of 200°C to 250°C. Also, this program will determine the relationship of accelerated life-test failures to rated temperature operation and develop a test specification for accelerated life tests within the scope of the M38510 specifications.

The program encompasses three phases. Phase I is the 250°C accelerated life test, Phase II is the 200°C accelerated life test, and Phase III is the 125°C accelerated life test.

SECTION II
OBJECTIVE

The objective of Phase I of this program is:

1. To conduct an accelerated life test of sufficient duration to generate a minimum of 50% cumulative failures in each lot of devices. This data coupled with data generated in Phase II and Phase III should provide a basis for determining the consistency of the activation energy among the three temperatures (250°C, 200°C, and 125°C).
2. To provide a basis for recommendations of conditions and limits to be used as part of a microcircuits qualification procedure.
3. To determine whether any thresholds are exceeded during the high temperature testing, which could trigger failure mechanisms unique to that temperature.
4. To determine the usefulness of the 250°C temperature life test as a predictor of long-term reliability.

SECTION III
DEVICE SELECTION

The choice of microcircuit devices for this program was made according to the following criteria:

1. High-reliability Class A devices.
2. Varying degree of complexity representing the product line.
3. Availability.

The following microcircuit types were chosen for this program:

MIL DESIGNATIONS	GENERIC NAMES	FUNCTION
M38510/05001ADX	CD4011A	Two-input quadruple logic gate
M38510/05101ADX	CD4013A	"D"-type flip-flop
M38510/05605ADX	CD4024A	Seven-stage binary counter.

The devices are in flat packs with weldable leads. Solder-dipped leads could not be used at temperatures above the solder melting point. These devices were tested to the individual M38510/50 specifications. Table III of these specifications is attached to this report as Table I (CD4011A), Table II (CD4013A), and Table III (CD4024A). The table specifies the electrical parameters' test conditions and limits for the group A testing for individual microcircuits. Subgroups 1,2,3,7, and 8 were performed at each measurement point throughout the test program and are the basis for the consequent data analysis.

TABLE III Group A inspection for device type 01
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 Method	Case All	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		Unit
		Symbol	1A	1B	1Y	2Y	2B	2A	V_{SS}	3A	3B	3Y	4Y	4B	4A	V_{DD}		Min	Max	Min	Max	Min	Max	
		Test No.																						
V_{IC} (POS)		1 2 3 4 5 6 7 8	1 mA	1 mA			1 mA	1 mA	GND	1 mA	1 mA			1 mA	1 mA	GND	1A 1B 2B 2A 3A 3B 4B 4A		1 5					Vdc
V_{IC} (NEG)		9 10 11 12 13 14 15 16	-1 mA	-1 mA			-1 mA	-1 mA	GND	-1 mA	-1 mA			-1 mA	-1 mA	GND	1A 1B 2B 2A 3A 3B 4B 4A		-6 0					Vdc
I_{SS}	3005	17 18 19	GND 15 0 V 15 0 V	15 0 V 15 0 V GND			15 0 V 15 0 V GND	GND 15 0 V 15 0 V	GND	GND 15 0 V 15 0 V	15 0 V 15 0 V GND			15 0 V 15 0 V GND	GND 15 0 V 15 0 V	15 0 V	V_{SS}		-25 0		-750 0			nA
V_{OH1}	3006	20 21 22 23 24 25 26 27	V_{IL1} 5 0 V GND	5 0 V V_{IL1} GND	I_{OH1} I_{OH1}	I_{OH1} I_{OH1}	GND GND V_{IL1} 5 0 V GND	GND GND 5 0 V V_{IL1} GND	GND	GND V_{IL1} 5 0 V GND GND	GND 5,0 V V_{IL1} GND GND	I_{OH1} I_{OH1}	I_{OH1} I_{OH1}	GND V_{IL1} 5,0 V	GND 5 0 V V_{IL1}	5 0 V	1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y	4 2		4 2		4 2		Vdc
V_{OH2}	3006	28 29 30 31 32 33 34 35	V_{IL1} 5 0 V GND	5 0 V V_{IL1} GND			GND GND V_{IL1} 5 0 V GND	GND GND 5,0 V V_{IL1} GND	GND	GND V_{IL1} 5 0 V GND GND	GND 5,0 V V_{IL1} GND GND			GND V_{IL1} 5 0 V	GND 5,0 V V_{IL1}	5 0 V	1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y	4 95		4 95		4 95		Vdc
V_{OH3}	3006	36 37 38 39	V_{IL2} 12 5 V GND GND	12 5 V V_{IL2} GND GND			GND GND V_{IL2} 12 5 V	GND GND 12 5 V V_{IL2}	GND	GND	GND			GND	GND	12 5 V	1Y 1Y 2Y 2Y	11 25		11 25		11 25		Vdc

TABLE I - Device: CD4011A, M38510/05001ADX, Group A inspection.

TABLE III Group A inspection for device type 01 (cont)
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 Method	Case All	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits Subgroup 1 T_A = 25°C Min	Subgroup 1 T_A = 25°C Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 T_A = 125°C Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 T_A = -55°C Max	Unit
		Symbol	1A	1B	1Y	2Y	2B	2A	V_{SS}	3A	3B	3Y	4Y	4B	4A	V_{DD}								
		Test No																						
V_{OH3}	3006	40	GND	GND			GND	GND	GND	V_{IL2}	12 5 V			GND	GND	12 5 V	3Y	11 25		11 25		11 25		Vdc
		41								12 5 V	V_{IL2}			GND	GND		3Y							
		42								GND	GND			V_{IL2}	12 5 V		4Y							
		43								GND	GND			12 5 V	V_{IL2}		4Y							
V_{OL1}	3007	44	V_{IH1}	V_{IH1}	I_{OL1}		GND	GND	GND	GND	GND			GND	GND	5 0 V	1Y		0 5		0 5		0 5	Vdc
		45	GND	GND		I_{OL1}	V_{IH1}	V_{IH1}		GND	GND						2Y							
		46					GND	GND		V_{IH1}	V_{IH1}	I_{OL1}					3Y							
		47					GND	GND		GND	GND		I_{OL1}	V_{IH1}	V_{IH1}		4Y							
V_{OL2}	3007	48	V_{IH1}	V_{IH1}			GND	GND	GND	GND	GND			GND	GND	5 0 V	1Y		0 05		0 05		0 05	Vdc
		49	GND	GND			V_{IH1}	V_{IH1}		GND	GND						2Y							
		50					GND	GND		V_{IH1}	V_{IH1}						3Y							
		51					GND	GND		GND	GND			V_{IH1}	V_{IH1}		4Y							
V_{OL3}	3007	52	V_{IH2}	V_{IH2}			GND	GND	GND	GND	GND			GND	GND	12 5 V	1Y		1 25		1 25		1 25	Vdc
		53	GND	GND			V_{IH2}	V_{IH2}	GND	GND	GND			GND	GND	12 5 V	2Y							
		54	GND	GND			GND	GND	GND	V_{IH2}				GND	GND	12 5 V	3Y							
		55	GND	GND			GND	GND	GND	GND	GND			V_{IH2}	V_{IH2}	12 5 V	4Y							
I_{IH1}	3010	56	15 0 V	15 0 V			15 0 V	15 0 V	GND	15 0 V	15 0 V			15 0 V	15 0 V	15 0 V	All together		8 0					nA
I_{IH2}	3010	57	15 0 V	GND			GND	GND	GND	GND	GND			GND	GND	15 0 V	1A				45 0			nA
		58	GND	15 0 V			GND										1B							
		59		GND			15 0 V										2B							
		60					GND	15 0 V									2A							
		61						GND		15 0 V	15 0 V						3A							
		62								GND	GND						3B							
		63									GND			15 0 V	15 0 V		4B							
		64									GND			GND			4A							
I_{IL1}	3009	65	GND	GND			GND	GND	GND	GND	GND			GND	GND	15 0 V	All together		-8 0					nA
I_{IL2}	3009	66	GND	GND			GND	GND	GND	GND	GND			6ND	6ND	15 0 V	1A				-45 0			nA
		67															1B							
		68															2B							
		69															2A							
		70															3A							
		71															3B							
		72															4B							
		73															4A							

TABLE I - Device. CD4011A, M38510/05001ADX, Group A inspection (Continued).

TABLE III Group A inspection for device type 01 (cont.)
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 Method	Case All	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits Subgroup 4 T_A = 25°C Min	Subgroup 4 T_A = 25°C Max	Unit
		Symbol	1A	1B	1Y	2Y	2B	2A	V_{SS}	3A	3B	3Y	4Y	4B	4A	V_{DD}				
		Test No																		
C_i	3012	74 75 76 77 78 79 80 81	F				F	F	GND	F	F			F		GND	1A 1B 2B 2A 3A 3B 4B 4A		12.0	pF
																		Subgroup 9 T_A = 25°C Min	Subgroup 9 T_A = 25°C Max	
																		Subgroup 10 T_A = 125°C Min	Subgroup 10 T_A = 125°C Max	
																		Subgroup 11 T_A = -55°C Min	Subgroup 11 T_A = -55°C Max	
t_{PHL}	3003 Fig. 7	82 83 84 85 86 87 88 89	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1A to 1Y 1B to 1Y 2A to 2Y 2B to 2Y 3A to 3Y 3B to 3Y 4A to 4Y 4B to 4Y	20	175	30	250	15	140	ns
t_{PLH}	3003 Fig. 7	90 91 92 93 94 95 96 97	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1A to 1Y 1B to 1Y 2A to 2Y 2B to 2Y 3A to 3Y 3B to 3Y 4A to 4Y 4B to 4Y	20	150	30	215	15	120	ns
T_{THL}	3004 Fig. 7	98 99 100 101 102 103 104 105	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y	30	250	45	360	25	200	ns
T_{TLH}	3004 Fig. 7	106 107 108 109 110 111 112 113	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y	40	300	60	430	30	240	ns

TABLE I - Device: CD4011A, M38510/05001ADX, Group A inspection (Continued).

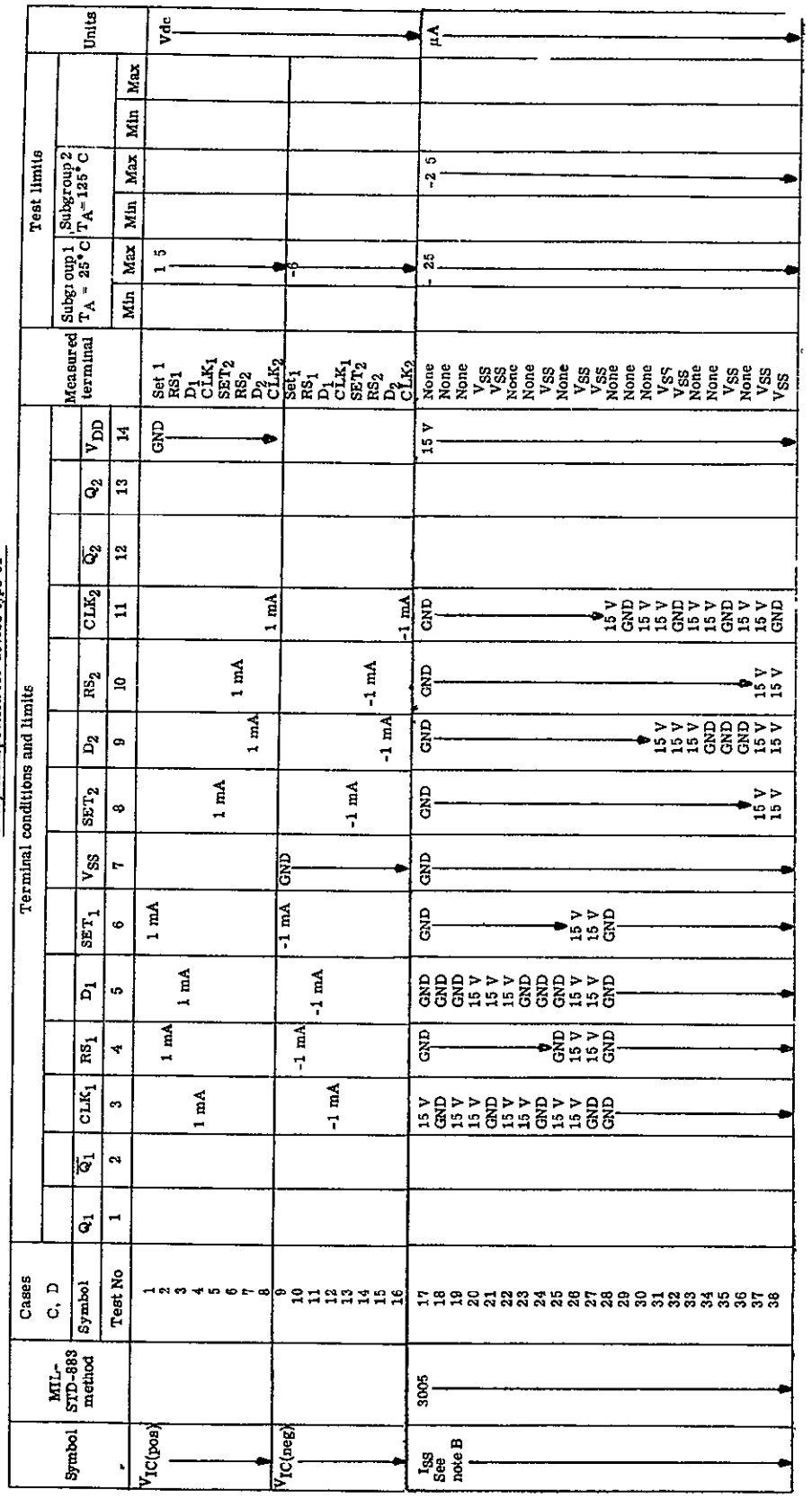


TABLE II - Device: CD4013A, M38510/05101ADX, Group A inspection.

TABLE III Group A inspection for device type 01 -Continued

Symbol	MIL-STD-883 method	Cases C, D	Terminal conditions and limits														Measured terminal	Test limits						Units
																		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
		Symbol	Q_1	$\overline{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\overline{Q}_2$	Q_2	V_{DD}								
		Test No	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
V_{OH1}	3006	39	I_{OH}	I_{OH}	GND	V_{IL1}	GND	V_{IH1}	GND	GND	GND	GND	GND			5 0 V	Q_1	4 5		4 5		4 5		Vdc
		40				V_{IH1}		V_{IL1}		GND		GND					$\overline{Q}_1$							
		41				GND		GND		V_{IH1}		V_{IL1}					Q_2							
		42				GND		GND		V_{IL1}		V_{IH1}		I_{OH}	I_{OH}		$\overline{Q}_2$							
V_{OH2}		43				V_{IL1}		V_{IH1}		GND		GND					$\overline{Q}_1$	4 95		4 95		4 95		
		44				V_{IH1}		V_{IL1}		GND		GND					$\overline{Q}_1$							
		45				GND		GND		V_{IH1}		V_{IL1}					Q_2							
		46				GND		GND		V_{IL1}		V_{IH1}					$\overline{Q}_2$							
V_{OH3}		47				V_{IL2}		V_{IH2}		GND		GND				12 5 V	$\overline{Q}_1$	11 25		11 25		11 25		
		48				V_{IH2}		V_{IL2}		GND		GND					$\overline{Q}_1$							
		49				GND		GND		V_{IH2}		V_{IL2}					Q_2							
		50				GND		GND		V_{IL2}		V_{IH2}					$\overline{Q}_2$							
V_{OL1}	3007	51	I_{OL}	I_{OL}		V_{IH1}		V_{IL1}		GND		GND				5 0 V	$\overline{Q}_1$		0 5		0 5		0 5	
		52				V_{IL1}		V_{IH1}		GND		GND					$\overline{Q}_1$							
		53				GND		GND		V_{IL1}		V_{IH1}					Q_2							
		54				GND		GND		V_{IH1}		V_{IL1}		I_{OL}	I_{OL}		$\overline{Q}_2$							
V_{OL2}		55				V_{IH1}		V_{IL1}		GND		GND					$\overline{Q}_1$		0 5		0 5		0 5	
		56				V_{IL1}		V_{IH1}		GND		GND					$\overline{Q}_1$							
		57				GND		GND		V_{IL1}		V_{IH1}					Q_2							
		58				GND		GND		V_{IH1}		V_{IL1}					$\overline{Q}_2$							
V_{OL3}		59				V_{IH2}		V_{IL2}		GND		GND				12 5 V	$\overline{Q}_1$		1 25		1 25		1 25	
		60				V_{IL2}		V_{IH2}		GND		GND					$\overline{Q}_1$							
		61				GND		GND		V_{IL2}		V_{IH2}					Q_2							
		62				GND		GND		V_{IH2}		V_{IL2}					$\overline{Q}_2$							
V_{OH4}		63			I	GND	V_{IL1}	I		GND		GND				5 0 V	$\overline{Q}_1$	4 95		4 95		4 95		
V_{OL4}		64			I		V_{IL1}	I		GND							$\overline{Q}_1$		0 05		0 05		0 05	
V_{OH4}		65			GND		GND	GND		I	V_{IL1}		I				Q_2	4 95		4 95		4 95		
V_{OL4}		66			GND		GND	GND		I	V_{IL1}		I				$\overline{Q}_2$		0 05		0 05		0 05	
V_{OL4}		67			I		V_{IH1}	I		GND	GND		GND				Q_1		0 05		0 05		0 05	
V_{OH4}		68			I		V_{IH1}	I		GND	GND		GND				$\overline{Q}_1$	4 95		4 95		4 95		
V_{OL4}		69			GND		GND	GND		I	V_{IH1}		I				Q_2		0 05		0 05		0 05	
V_{OH4}		70			GND		GND	GND		I	V_{IH1}		I				$\overline{Q}_2$	4 95		4 95		4 95		
V_{ICL1}		71			J		J	J		GND	GND		GND				CLK_1, J		V_{IH1}		V_{IH1}		V_{IH1}	
V_{ICL1}		72			J		J	J		GND	GND		GND				CLK_1, J	V_{IL1}		V_{IL1}		V_{IL1}		
V_{ICL2}		73			GND		GND	GND		J	J		J				CLK_2, J		V_{IH1}		V_{IH1}		V_{IH1}	
V_{ICL2}		74			GND		GND	GND		J	J		J				CLK_2, J	V_{IL1}		V_{IL1}		V_{IL1}		

TABLE II - Device: CD4013A, M38510/05101ADX, Group A inspection. (Continued)

TABLE III Group A inspection for device type 01 - Continued

Symbol	MIL-STD-883 method	Cases C D	Terminal conditions and limits														Measured terminal	Test limits						Units
																		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
		Symbol	Q_1	$\bar{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\bar{Q}_2$	Q_2	V_{DD}								
		Test No	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
I_{IH1} See note K	3010	75			15 V	15 V	15 V	15 V	GND	15 V	15 V	15 V	15 V			15 V	All inputs together		8					nA
I_{IH2}		76 77 78 79 80 81 82 83															CLK_1 RS_1 D_1 SET_1 SET_2 D_2 RS_2 CLK_2		1 0		45			
I_{IL1} See note K	3009	84			GND	GND	GND	GND		GND	GND	GND	GND				All inputs together		-8 0					
I_{IL2}		85 86 87 88 89 90 91 92															CLK_1 RS_1 D_1 SET_1 SET_2 D_2 RS_2 CLK_2		-1 0		-45			
																		Subgroup 4 T_A = 25°C						
C_i	3012	93 94 95 96 97 98 99 100			L	L	L	L	GND	L	L	L	L			GND	CLK_1 RS_1 D_1 SET_1 SET_2 D_2 RS_2 CLK_2		12					pF

TABLE II - Device. CD4013A, M38510/05101ADX, Group A inspection. (Continued)

TABLE III Group A inspection for device type 01 -Continued

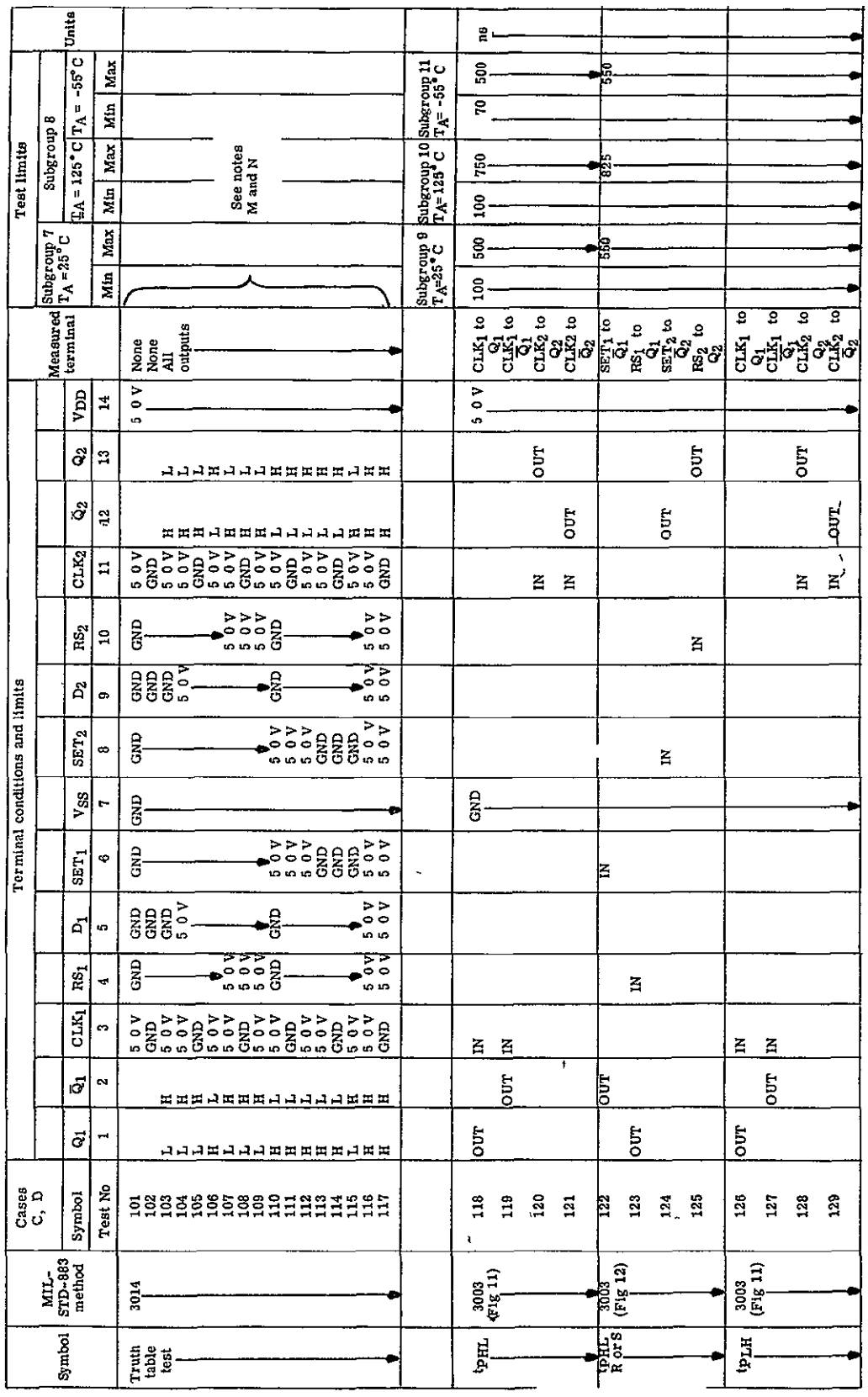


TABLE II - Device. CD4013A, M38510/05101ADX, Group A inspection. (Continued)

TABLE III Group A inspection for device type 01 -Continued

Symbol	MIL-STD-883 method	Cases C D	Terminal conditions and limits														Measured terminal	Test limits						Units
																		Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
		Symbol	Q_1	$\overline{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\overline{Q}_2$	Q_2	V_{DD}								
		Test No	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
t_{PLH} R or S	3003 (Fig 12)	130	OUT					IN	GND							5 0 V	SET_1 to Q_1	100	420	100	630	70	420	ns
		131		OUT		IN											RS_1 to $\overline{Q}_1$							
		132								IN					OUT		SET_2 to Q_2							
		133										IN		OUT			RS_2 to $\overline{Q}_2$							
t_{THL}	3004 (Fig 11)	134	OUT		IN												Q_1	30	300	40	450	25	300	
		135		OUT	IN										OUT		$\overline{Q}_1$							
		136											IN				Q_2							
		137											IN	OUT			$\overline{Q}_2$							
t_{TLH}	3004 (Fig 11)	138		OUT	IN												Q_1		350		525		350	
		139	OUT		IN												$\overline{Q}_1$							
		140											IN	OUT			Q_2							
		141											IN		OUT		$\overline{Q}_2$							
f_{CL} (max) See note O	(Fig 11)	142	OUT		IN								IN		OUT		CLK_1		0 67		1 0		0 67	µs
		143															CLK_2		0 67		1 0		0 67	µs
t_{TLHCL} (Max) See note P	(Fig 11)	144	OUT		IN												CLK_1	15		15		10		µs
		145											IN		OUT		CLK_2	15		15		10		µs
tp See note Q	(fig 11)	146	OUT		IN												CLK_1		300		450		300	ns
		147											IN		OUT		CLK_2		300		450		300	
t_{SHL}	(Fig 13)	148			IN		IN										D_1 to CLK_1		150		225		150	
t_{SHL}		149									IN		IN				D_2 to CLK_2							
t_{SLH}		150			IN		IN										D_1 to CLK_1							
t_{SLH}		151									IN		IN				D_2 to CLK_2							
t_{HHL}	(Fig 14)	152			IN		IN										D_1 to CLK_1							
t_{HHL}		153									IN		IN				D_2 to CLK_2							
t_{HLH}		154			IN		IN										D_1 to CLK_1							
t_{HLH}		155									IN		IN				D_2 to CLK_2							

NOTES

A Pins not designated may be "high" level logic, "low" level logic or open

B Test numbers 17 thru 38 shall be run in sequence

C I_{OH} = -0 25 mA at 25°C, -0 175 mA at 125°C, -0 31 mA at -55°C

D V_{IH1} = 3 8 V at 25°C, 3 6 V at 125°C, 3 95 V at -55°C

E V_{IH2} = 9 5 V at 25°C, 9 25 V at 125°C, 9 75 V at -55°C

F I_{OL} = 0 5 mA at 25°C, 0 35 mA at 125°C, 0 65 mA at -55°C

G V_{IL1} = 1 1 V at 25°C, 0 8 V at 125°C, 135 V at - 55°C

H V_{IL2} = 2 8 V at 25°C, 2 55 V at 125°C, 3 0 V at -55°C

I For input conditions see Figure 9

J For input voltage conditions see Figure 10

K The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together

L See 4 4 1(c)

M Test numbers 101 thru 117 shall be run in sequence and the functional tests shall be performed with V_{IH} and $V_{DD} \leq$ 5 0 V and $\geq$ 15 0 V

N L = 0 5 V maximum and H = 4 5 V minimum

O The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column

P Pulse repetition period = 100 µ sec, 50 percent duty cycle The maximum clock transition time (t_{TLHCL}) requirement is considered met if proper output state changes occur with the rise time set to that given in the limits column

Q The minimum clock pulse width (t_p) requirement is considered met if proper output state changes occur with the pulse width set to that given in the limits column

TABLE III Group A inspection for device type 05

Symbol	MIL-STD-883 method	Case C D	Terminal conditions (pins not designated are open)														Meas terminal	Test limits						Units
			1	2	3	4	5	6	7	8	9	10	11	12	13	14		Subgroup 1 T_A = 25°C		Subgroup 2 T_A=125°C		Subgroup 3 T_A= -55°C		
		Test No	Input	Reset	Q_7	Q_6	Q_5	Q_4	V_{SS}	NC	Q_3	NC	Q_2	Q_1	NC	V_{DD}		Min	Max	Min	Max	Min	Max	
I_{IH}	3010	1	15 0 V	GND					GND							15 V	1		1 0		10		1 0	nAdc
I_{IH}	3010	2	GND	15 0 V													2							
I_{IL}	3009	3	GND	GND													1							
I_{IL}	3009	4	GND	GND													2							
V_{OL2}	3007	5	A	A													A		10		50		10	mVdc
V_{OH2}	3006	6	A	A													A	14 99		14 95		14 99		Vdc
V_{OH1}	3006	7	B	B	C	C	C	C			C		C	C		5 0 V	B	4 20		4 20		4 20		Vdc
V_{OL1}	3007	8	B	B	D	D	D	D			D		D	D			B		500		500		500	mVdc
$V_{I\overline{CL}}$		9	E	E													E		3 50		3 25		3 65	Vdc
V_{IR}		10	F	F													F	1 50		1 25		1 75		Vdc
I_{SS}	3005	11	H	H												15 V	7		500		5000		500	nAdc
I_{SS}	3005	12	15 V	15 V												15 V	7		500		5000		500	nAdc
																		Subgroup 4 T_A = 25°C						
																		Min	Max					
C_i	3012	13	L						GND							GND	1		7 0					pF
C_i	3012	14		L					GND							GND	2		7 0					pF
																		Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
																		Min	Max	Min	Max	Min	Max	
t_{PHL1}	3003	15	J	GND	G	G	G	G	GND		G		G	G		5 0 V	12		0 44		0 56		0 33	µs
		16															11		0 88		1 12		0 66	
		17															9		1 32		1 68		0 99	
		18															6		1 76		2 24		1 32	
		19															5		2 20		2 80		1 65	
		20															4		2 64		3 36		1 98	
		21															3		3 10		4 00		2 31	
t_{PLH}		22															12		0 44		0 56		0 33	
		23															11		0 88		1 12		0 66	
		24															9		1 32		1 68		0 99	
		25															6		1 76		2 24		1 32	
		26															5		2 20		2 80		1 65	
		27															4		2 64		3 36		1 98	
		28															3		3 10		4 00		2 31	
t_{THL}	3004	29															J		430		550		325	ns
t_{TLH}	3004	30															I		430		550		325	ns
t_{PHL2}	3003	31	K	K													K		0 90		1 16		0 68	µs
Subgroup 7 Verify truth table, figure 3 @ $V_{DD} \leq$ 5 0 Vdc and $\geq$ 15 0 Vdc V_{OL} = V_{SS} + 0 50 Vdc V_{OH} = V_{DD} -0 50 Vdc T_A = 25°C																								
Subgroup 8 Same test, terminal conditions and limits as subgroup 7 except T_A = 125°C and -55°C																								

NOTES

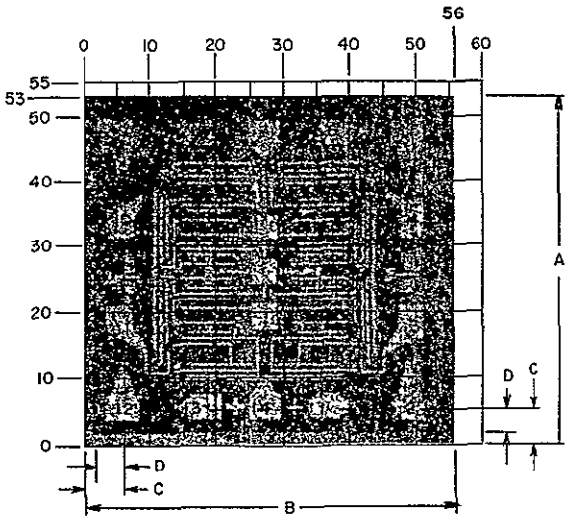
A Each output shall be measured using the timing diagram of figure 26
B Each output shall be measured using the timing diagram of figure 27
C I_{OH} 150 µAdc @ 25°C -105 µAdc @ 125°C 185 µAdc @ -55°C
D I_{OL} = 250 µAdc @ 25°C, 175 µAdc @ 125°C 310 µAdc @ -55°C
E See figure 28 timing diagram
F See figure 29 timing diagram
G Load conditions C_L = 50 pF R_L = 200 kΩ
H Check I_{SS} for each count state (i.e., 2^{8-1} and 2^6) (See figure 26.)
See figure 41 for test circuit and measurement points
See figure 42 for test circuit and measurement points
See figure 43

TABLE III - Devices CD4024A, M38510/05605ADX, Group A inspection.

Further detailed description of these microcircuits is given in Figs. 1 through 7. Photographs of chips with dimensions grid, magnified photographs with detail visibility, logic diagrams, and circuit diagrams in these figures provide a basis for comparison of the chip sizes and complexities of the microcircuits involved.

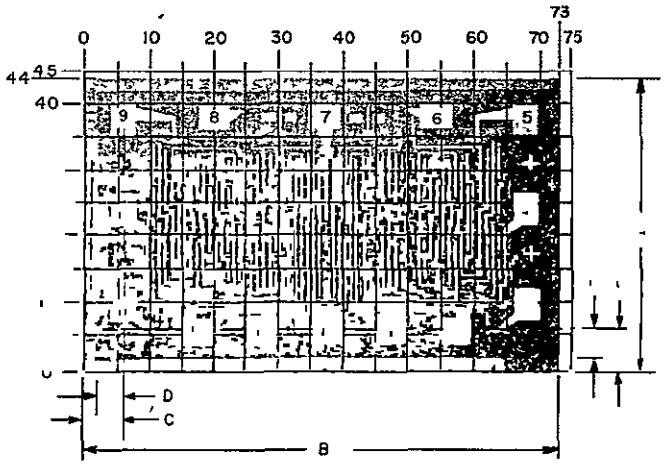
The table below summarizes these factors.

Type	Si Area	No. of active elements	Number of inputs	Number of outputs
CD4011A	1.9 mm^2	13	8	4
CD4013A	2.1 mm^2	64	8	4
CD4024A	4.2 mm^2	134	2	7



CD4011AH

92CS-22078

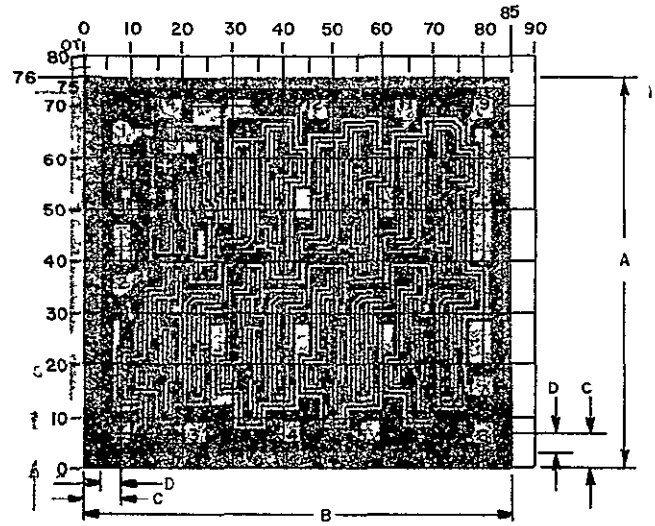


CD4013AH

92CS-22080

Grid Graduations Are In Mils (10^{-3} Inch)

TYPE	A*		B*		C		D		CHIP THICKNESS	
	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters
CD4011AH	50 – 58	1 270 – 1 473	53 – 61	1 347 – 1 549	4 – 10	0 102 – 0 254	3 3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 228
CD4012AH	50 – 58	1 270 – 1 473	53 – 61	1 347 – 1 549	↕	↕	↕	↕	↕	↕
CD4013AH	41 – 49	1 042 – 1 244	70 – 78	1 778 – 1 981						
CD4014AH	79 – 87	2 007 – 2 209	81 – 89	2 058 – 2 260	4 – 10	0 102 – 0 254	3 3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 228



CD4024AH

92CS-22090

Grid Graduations Are In Mils (10^{-3} Inch)

TYPE	A*		B*		C		D		CHIP THICKNESS	
	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters
CD4023AH	53 – 61	1 347 – 1 549	53 – 61	1 347 – 1 549	4 – 10	0 102 – 0 254	3 3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 288
CD4024AH	73 – 81	1 855 – 2 057	82 – 90	2 083 – 2 286	↕	↕	↕	↕	↕	↕
CD4025AH	49 – 57	1 245 – 1 447	51 – 59	1 297 – 1 498						
CD4026AH	89 – 97	2 261 – 2 463	89 – 97	2 261 – 2 463	4 – 10	0 102 – 0 254	3 3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 228

** The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip Therefore the isolated chip is actually 7 mils (0 17 mm) larger in both the A and B dimensions*

Fig. 1 - Dimensions of microcircuit chips.

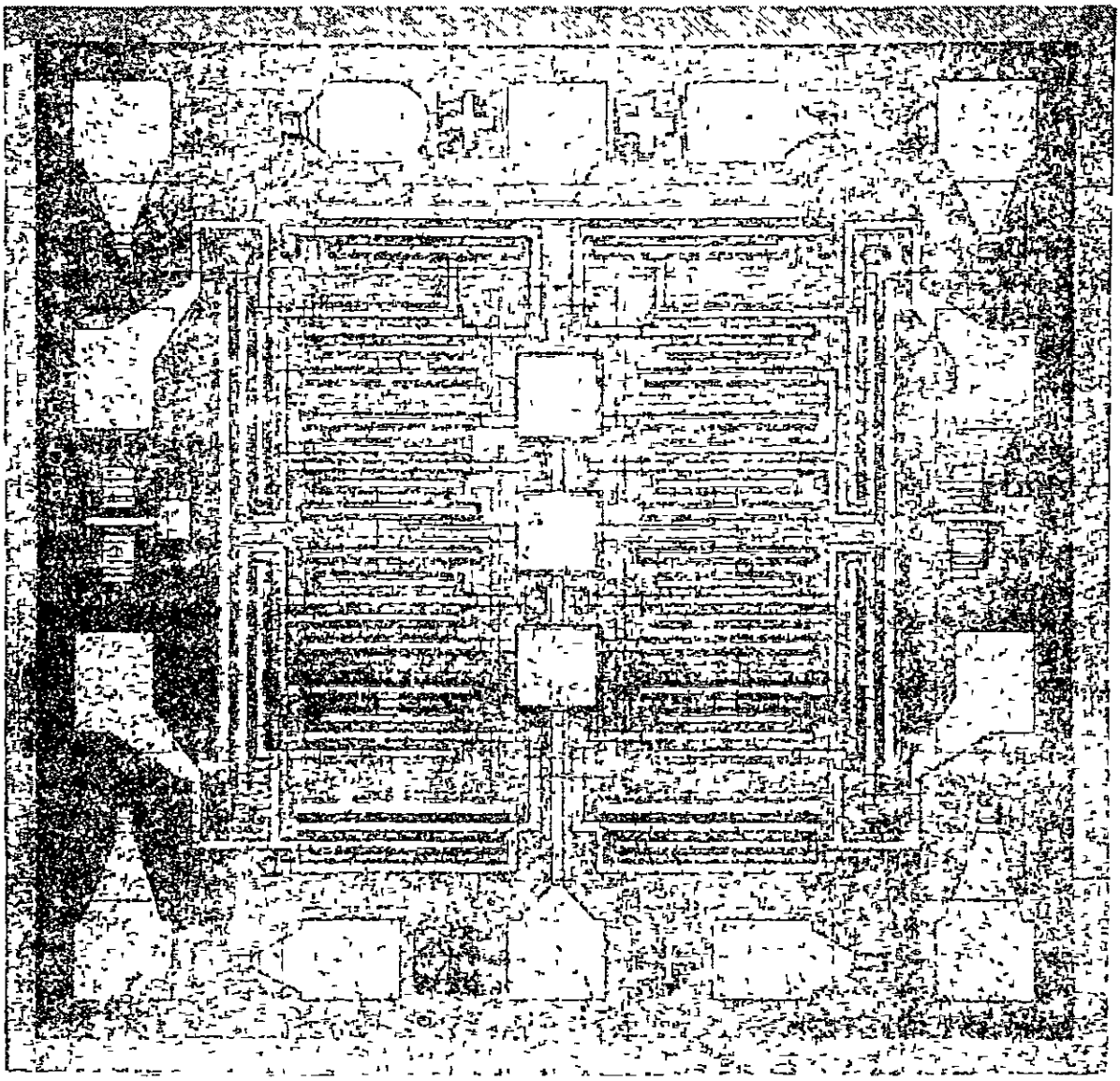


Fig. 2 - CD4011A microcircuit.

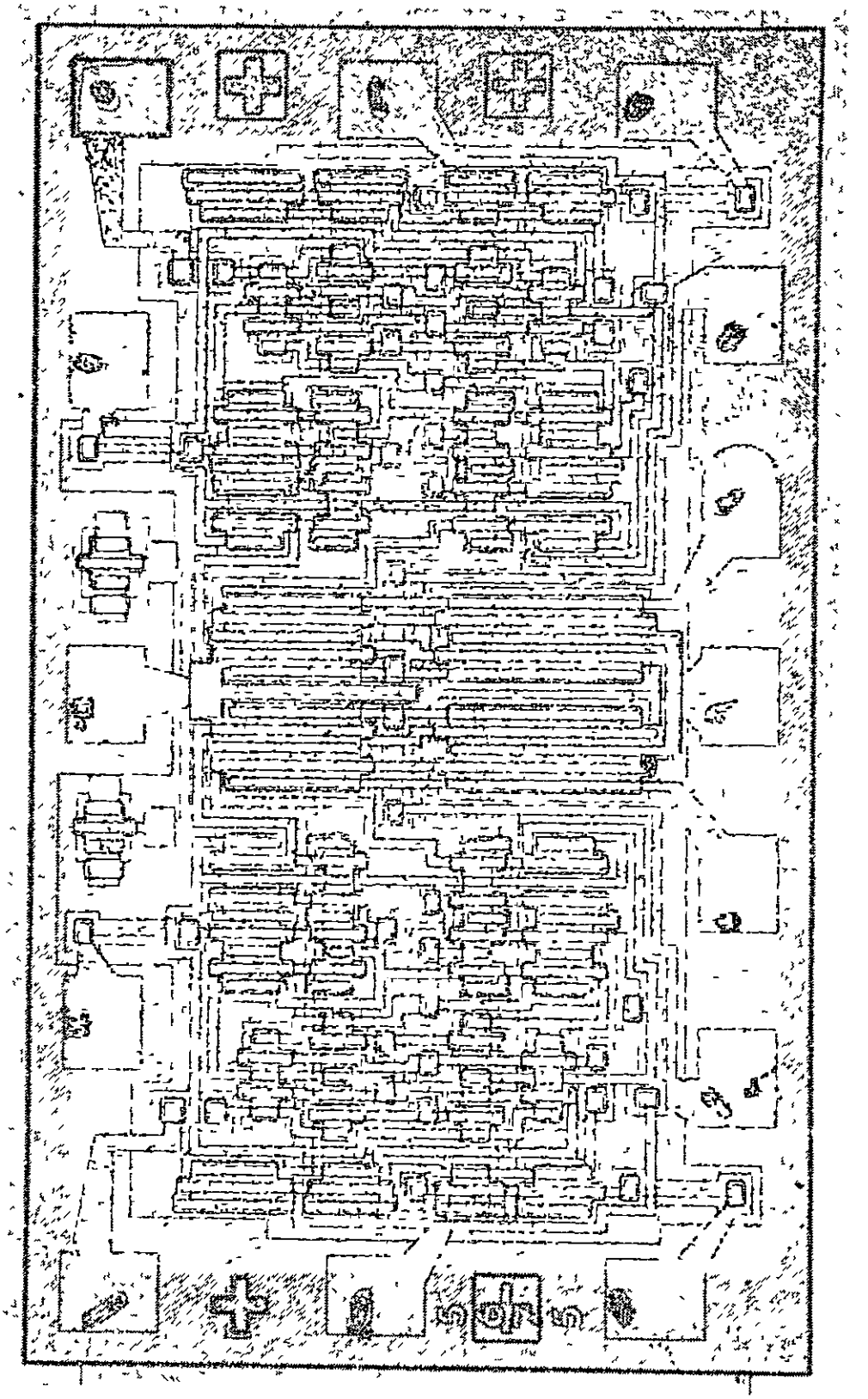


Fig. 3 - CD4013A microcircuit.

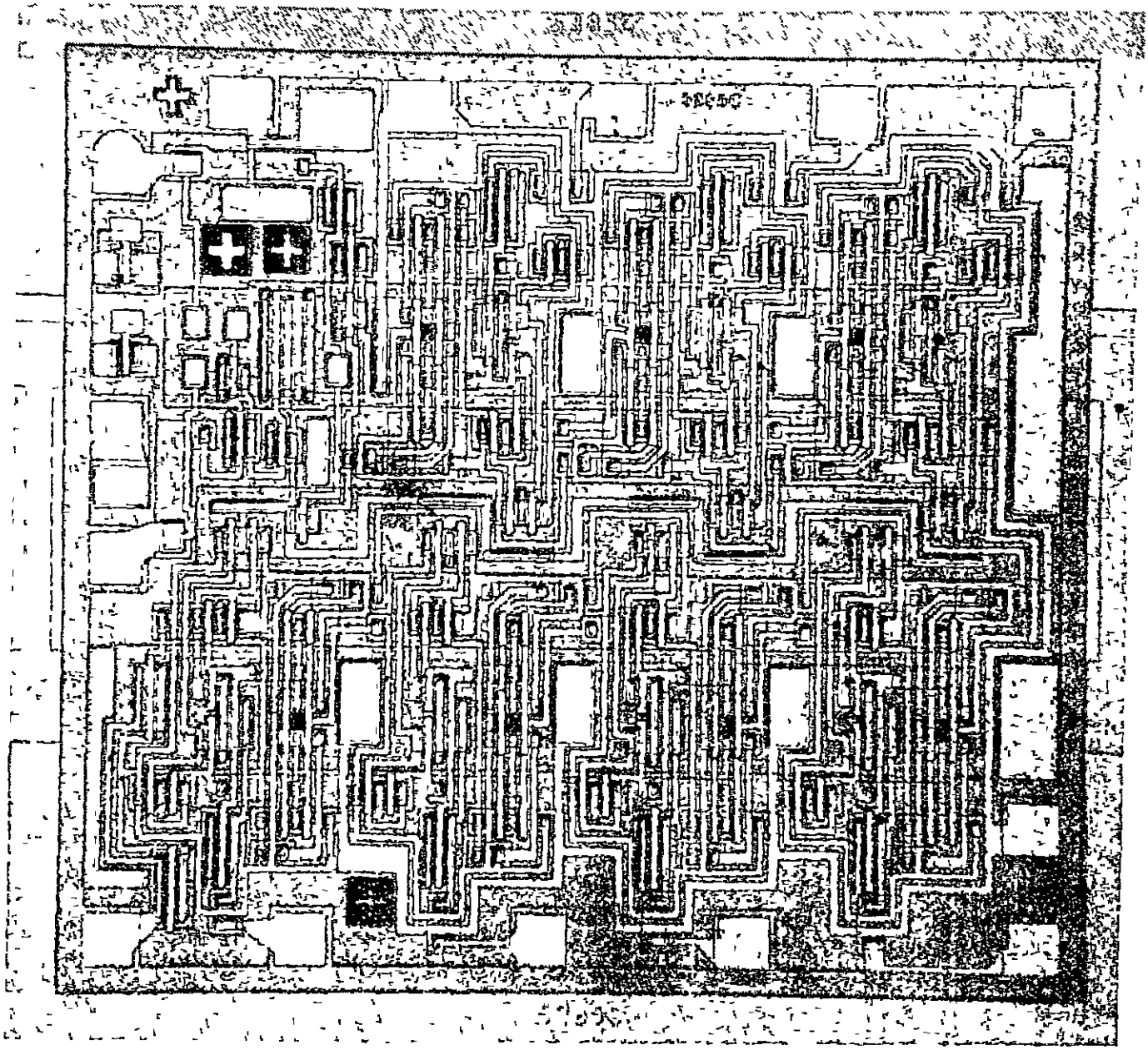
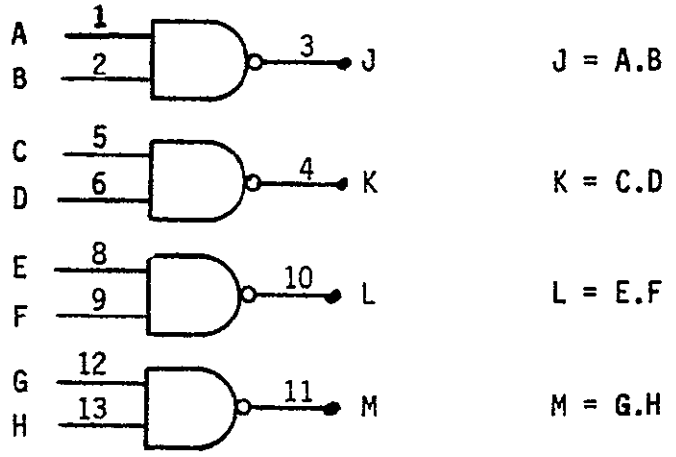


Fig. 4 - CD4024A microcircuit.



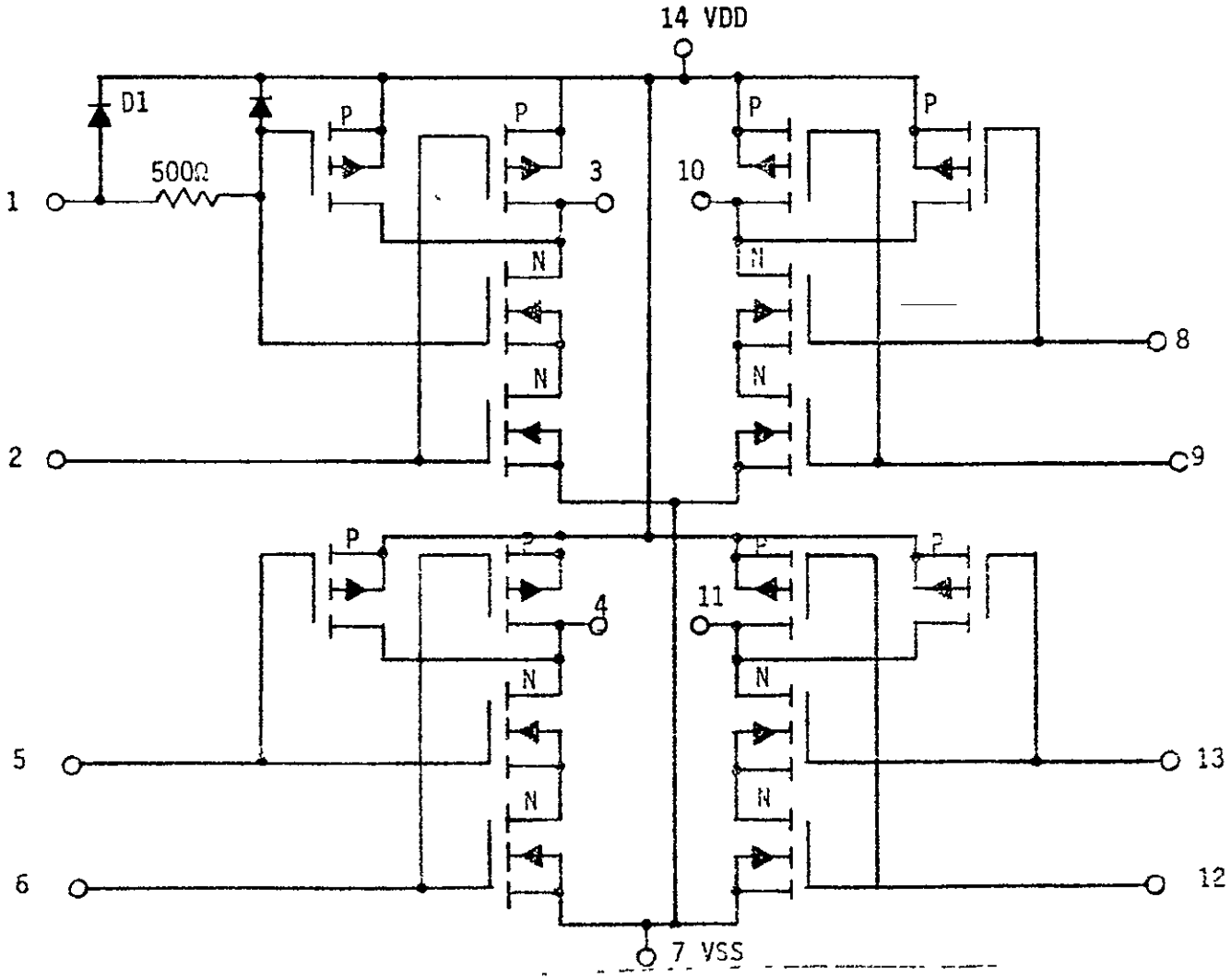


Fig. 5 - Logic and circuit diagrams for the CD4011A.

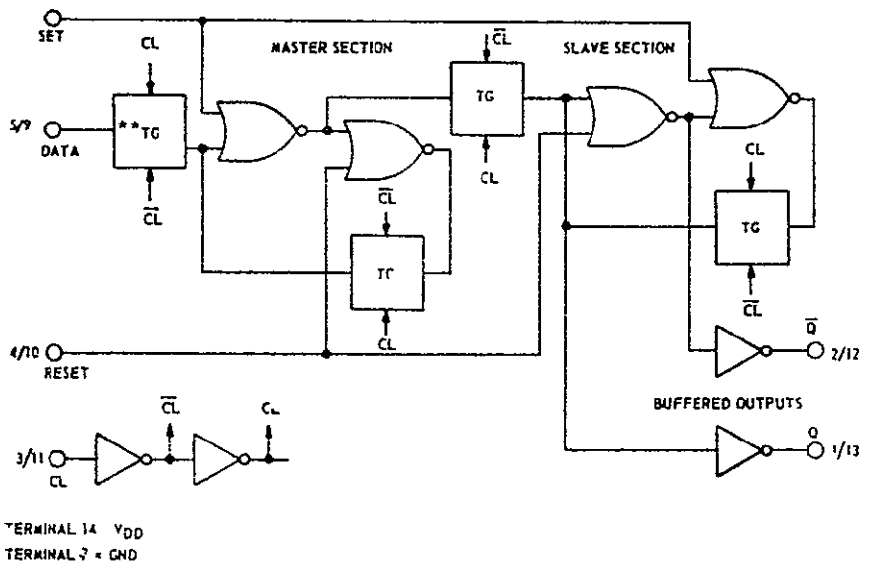


Fig. 6 - Logic and circuit diagrams for the CD4013A. (Page 1 of 2 pages.)

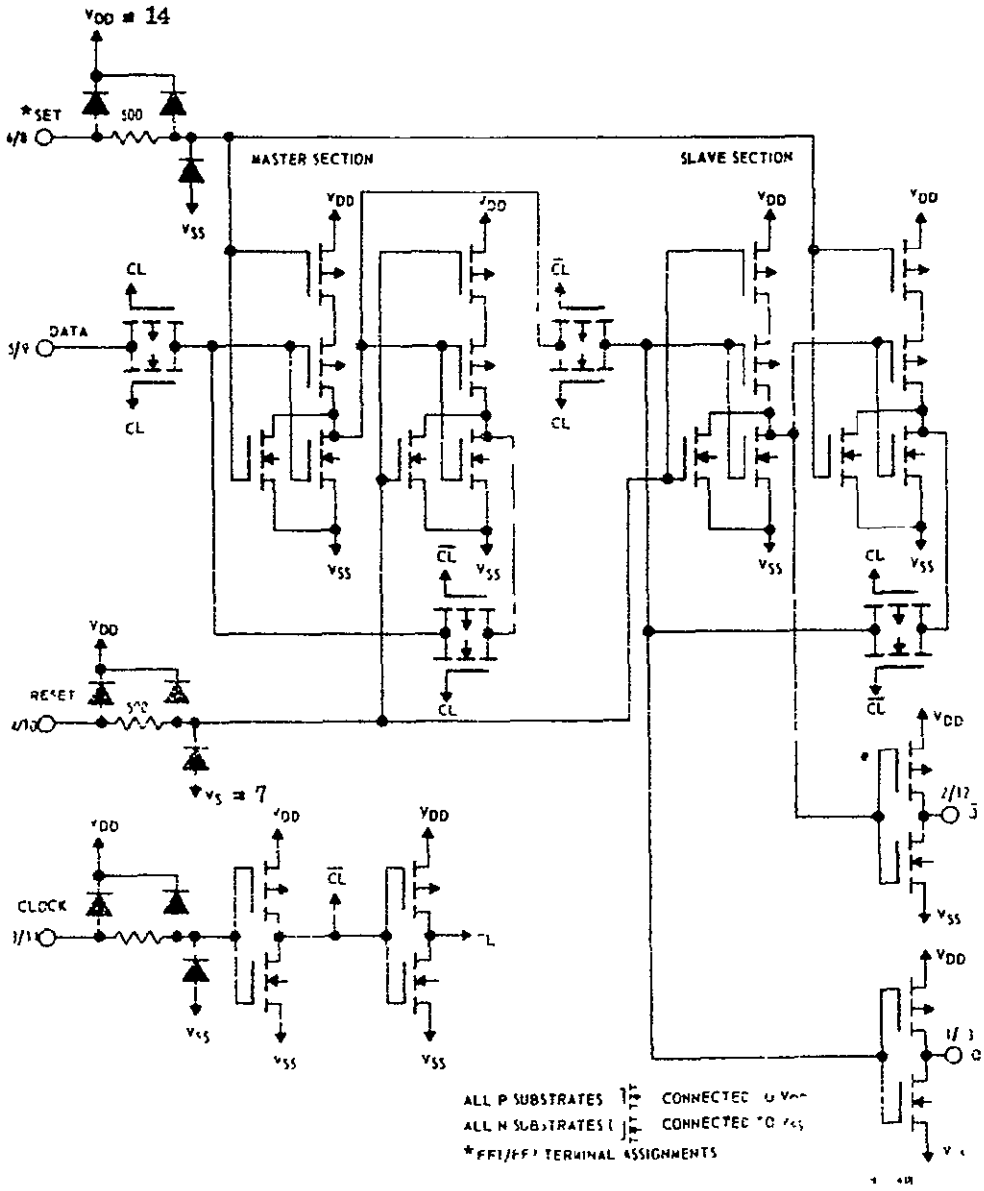


Fig. 6 - Logic and circuit diagrams for the CD4013A. (Page 2 of 2 pages.)

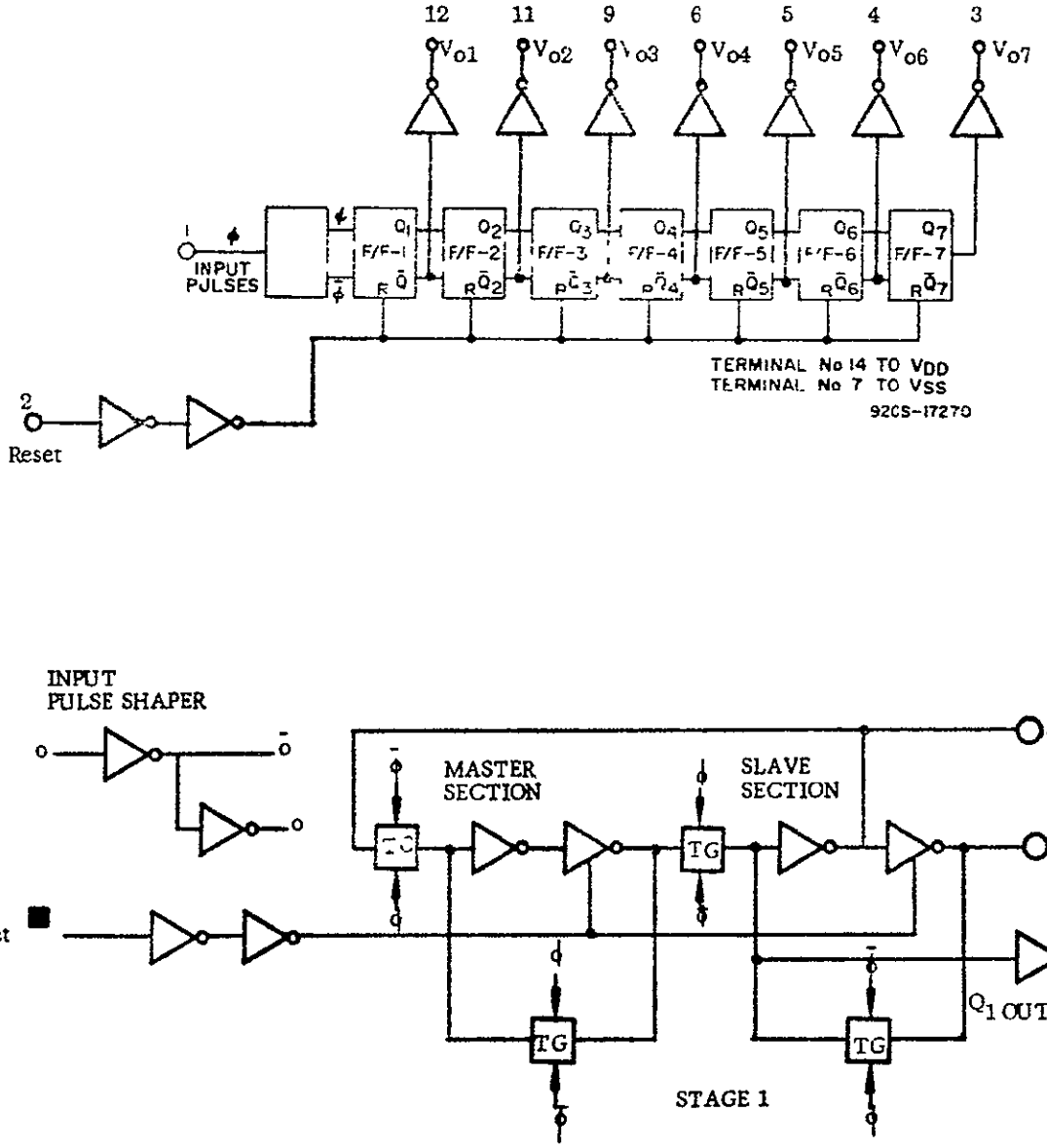
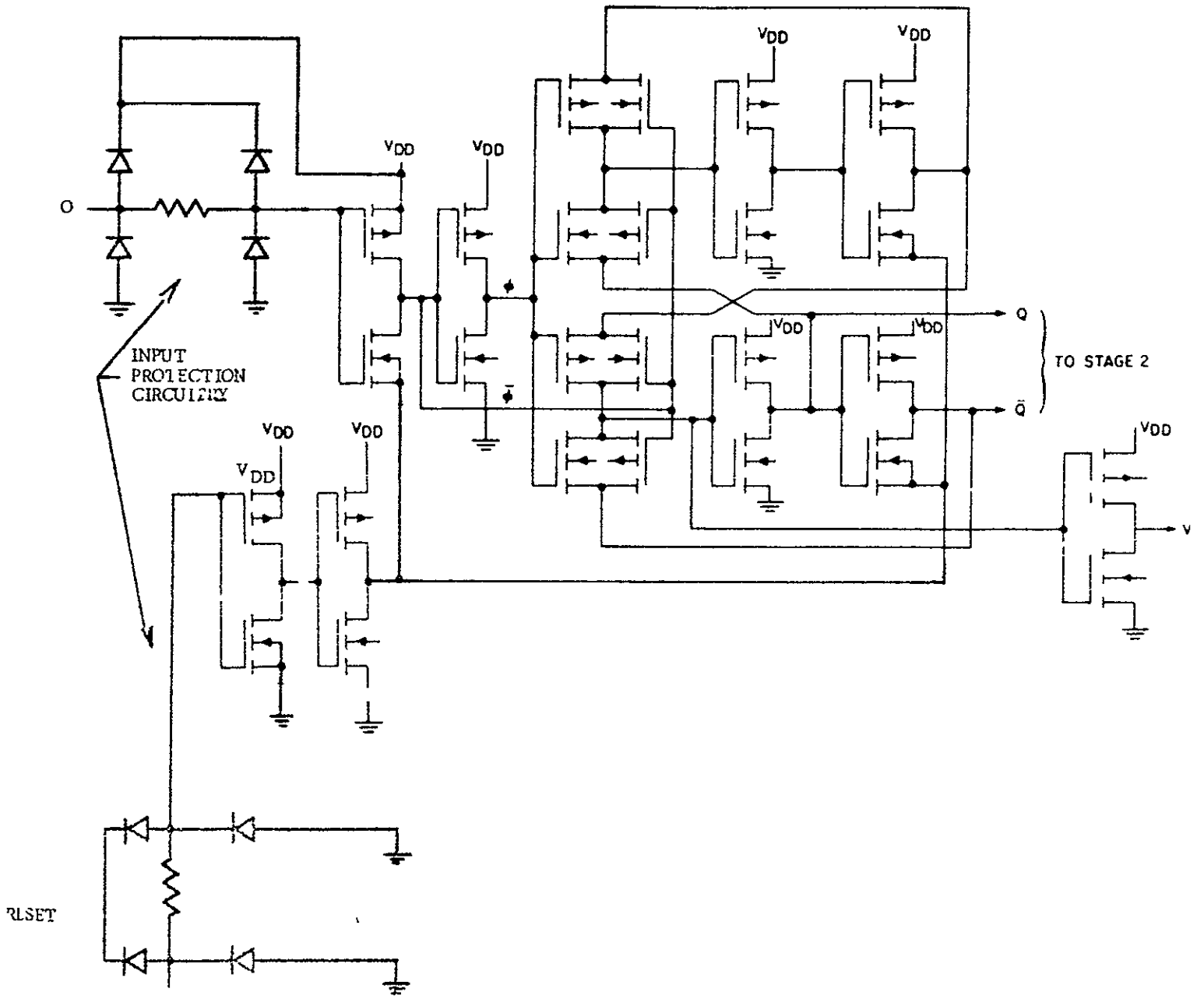


Fig. 7 - Logic and circuit diagrams for the CD4024A. (Page 1 of 2 pages.)



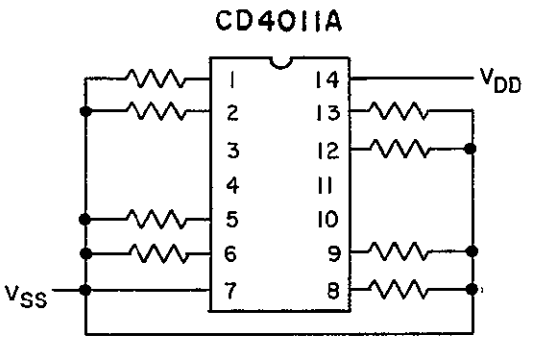
NOTE: SUBSTRATES FOR ALL "P" UNITS ARE CONNECTED TO V_{DD}
SUBSTRATES FOR ALL "N" UNITS, UNLESS OTHERWISE SHOWN, ARE CONNECTED TO GROUND.

Schematic diagram of Input Pulse Shaper and one of seven binary stages for CD4024A

Fig. 7 - Logic and circuit diagrams for the CD4024A. (Page 2 of 2 pages.)

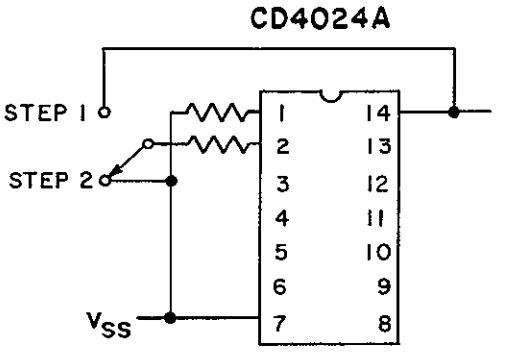
SECTION IV
TEST VOLTAGE AND BIAS

The choice of bias was dictated by the desire to further accelerate the life testing process by stressing the n-channel transistor to possibly the worst-case condition. The available evidence suggests that the n-channel transistor in CMOS microcircuits is the weak link when biased to the off condition (gate is low with respect to drain). The drain-to-source and drain-to-gate potentials set up under this bias accelerate movement of the positively charged (usually sodium) particles. These particles are thought to accumulate in the oxide, thereby neutralizing the effect of the negatively biased gate and setting up a mechanism for potential leakage. The biases used are shown in the pin connection diagrams of Fig. 8. The operating voltage was chosen as 12.5 volts dc to conform to the M-38510 specifications.



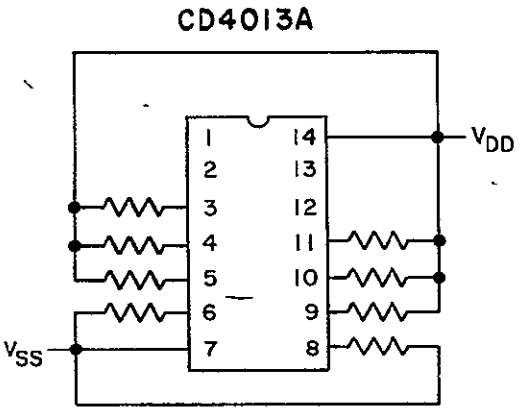
92CS-28638

ALL RESISTORS ARE 47KΩ



92CS-28637

ALL RESISTORS ARE 47KΩ



92CS-28636

ALL RESISTORS ARE 47KΩ

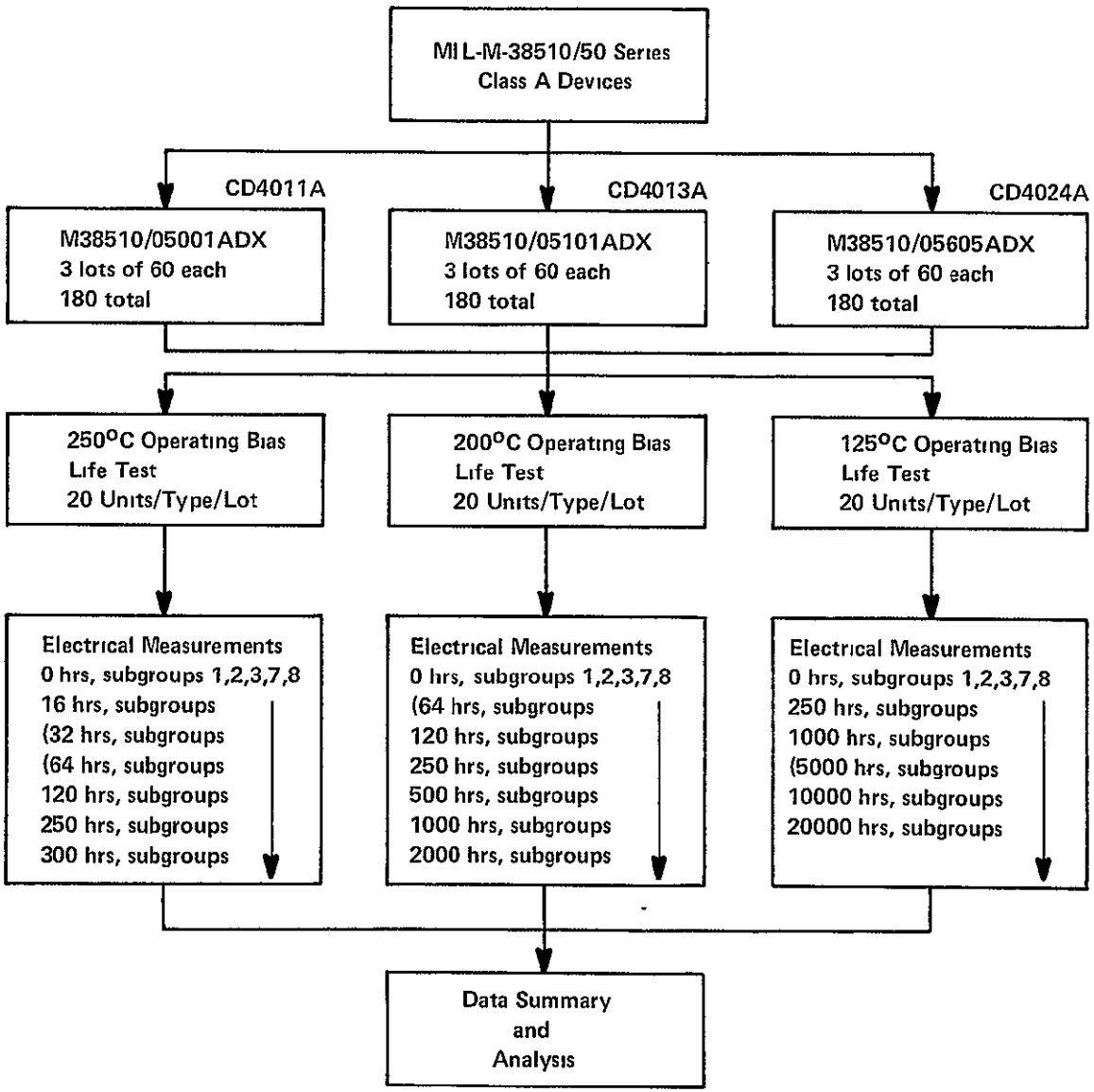
Fig. 8 - Bias connection diagrams.

SECTION V
THE TEST

The test matrix was developed and is shown in Table IV. Devices were selected from three lots in each type to represent broad process variations. The program encompasses 3 life-test temperatures. Each lot is represented by 20 test devices in each life test for a total of 60 test devices of each type. Each test sample of 20 test devices had, in addition, 5 control devices which were monitored at each measurement point together with the test devices, but were not life tested.

Prior to beginning of the contract, trial runs were started. Data from those runs prompted the introduction of more measurement points for the 250°C as well as the 200°C life test. The testing at each measurement point was broadened to include 125°C, and -55°C measurements.

Table IV – Test Matrix



SECTION VI
DATA PRESENTATION AND ANALYSIS

The test measurement results obtained in the course of this program were considered in three ways.

1. Data from the three life-test temperature cells (250°C, 200°C, and 125°C). This data includes failure attributes summary, parameter trend tables and curves, and failure rate versus time charts.
2. Results that require data from failure analysis. This report includes early failure analysis on some catastrophically failed devices.

Tables V, VI, and VII give the cumulative failures per type for each life-test temperature cell versus time. In an attempt to minimize the arbitrariness in the failure definition, the failure attributes data is presented in the following ways.

1. Column I. The failures are defined in accordance with the M38510/50 individual specifications limits as given in Table III of these specifications (Tables I, II, and III of this report). All failures are counted including the continuity failures. This data is not plotted.
2. Column II. Less continuity. The continuity failures are excluded from the count if the failure analysis reveals: (a) burned-out metallization indicating possibility of external influence, (b) automated testing problems steming from improper socket contact. The failure as in (b) is really a good device and is considered as such in subsequent measurement points.

TABLE V - SUMMARY OF FAILURE ATTRIBUTES

(CD4011A)

		I ALL FAILURES				II LESS CONTINUITY				III LESS MARGINAL LEAKAGE			
Temp.	Lot/Hrs	16	32	64	120	16	32	64	120	16	32	64	120
250°C	40	0/19	0/19	0/17	16/17	0/19	0/19	0/17	16/17	0/19	0/19	0/17	16/17
	50	2/20	6/20	8/20	16/20	2/20	6/20	8/20	15/19	0/20	1/20	2/20	15/19
	60	2/20	2/19	8/19	18/19	2/20	2/19	8/19	0/1	0/20	0/19	5/19	0/1
Total		4/59	8/58	16/56	50/56	4/59	8/58	16/56	31/37	0/59	1/58	7/56	31/37
%		7	14	29	89	7	14	29	84	0	2	13	84

Temp.	Lot/Hrs	64	120	250	500	1000	64	120	250	500	1000	64	120	250	500	1000
200°C	43	0/20	0/20				0/20	0/20				0/20	0/20			
	53	1/20	1/20	1/20			1/20	1/20	1/20			0/20	0/20	1/20		
	63	2/20	2/20	2/20			1/19	1/20	1/20			0/19	0/20	0/20		
Total		3/60	3/60	3/40			2/59	2/60	2/40			0/59	0/60	1/40		
%		5	5	7.5			3	3				0	0			

Temp.	Lot/Hrs	168	500	1000	168	500	1000	168	500	1000
125°C	40	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
	50	0/20	0/20	2/20	0/20	0/20	0/18	0/20	0/20	0/18
	60	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20
Total		0/60	0/60	2/60	0/20	0/20	0/58	0/60	0/60	0/58
%		0	0	3	0	0	0	0	0	0

TABLE VI - SUMMARY OF FAILURE ATTRIBUTES

(CD4013A)

		I ALL FAILURES				II LESS CONTINUITY				III LESS MARGINAL LEAKAGE			
Temp.	Lot/Hrs	16	32	64	120	16	32	64	120	16	32	64	120
250°C	41	2/20	10/20			2/20	8/18			0/20	1/18		
	81	5/20	7/20	15/15		5/20	6/19	15/15		5/20	5/19	15/15	
	21	2/20	12/20			1/19	11/19			0/19	6/19		
Total		9/60	29/60	15/15		8/59	25/56	15/15		5/59	12/56	15/15	
%		15	48	100		14	45	100		8	21	100	

Temp.	Lot/Hrs	64	120	250	500	1000	64	120	250	500	1000	64	120	250	500	1000
200°C	83	1/20	4/20	5/20	8/20		0/19	1/17	1/16	3/15		0/19	1/17	1/17	2/15	
	43	0/20	2/20	2/20	2/20		0/20	0/18	0/18	0/18		0/18	0/18	0/18	0/18	
Total		1/40	6/40	7/40	10/40		0/39	1/35	1/34	3/33		0/37	1/35	1/35	2/33	
%		5	15	18	25		0	3	3	9		0	3	3	6	

Temp.	Lot/Hrs	250	1000	250	1000	250	1000
125°C	42	0/20		0/20		0/20	
	82	0/20		0/20		0/20	
	22	0/20		0/20		0/20	
Total		0/60		0/60		0/60	
%		0		0		0	

TABLE VII - SUMMARY OF FAILURE ATTRIBUTES

(CD4024A)

		I ALL FAILURES				II LESS CONTINUITY				III LESS MARGINAL LEAKAGE			
Temp.	Lot/Hrs	16	32	64	120	16	32	64	120	16	32	64	120
250°C	51	2/20	13/19			2/20	12/18			1/20	11/18		
	61	8/20	15/20			6/18	13/18			4/18	13/18		
	32	7/19	10/18	18/18		7/19	10/18	18/18		7/19	9/18	18/18	
Total		17/59	38/57	18/18		15/57	35/54	18/18		12/57	33/54	18/18	
%		28	66	100		26	65	100		21	65	100	

Temp.	Lot/Hrs	64	120	250	500	1000	64	120	250	500	1000	64	120	250	500	1000
200°C	53	0/20	3/20	11/19			0/20	3/20	11/19			0/20	2/20	7/19		
	33	0/20	1/20	7/20			0/20	1/20	7/20			0/20	1/20	7/20		
	63	3/20	3/20	11/20			3/20	3/20	11/20			0/20	0/20	7/20		
Total		3/60	7/60	29/59			3/60	7/60	29/59			0/60	3/60	21/59		
%		5	12	49			5	12	49			0	5	36		

Temp.	Lot/Hrs	250	1000	250	1000	250	1000
125°C	52	0/20	3/20	0/20	3/20	0/20	0/20
	34	0/20	3/20	0/20	0/17	0/20	0/17
	62	3/20	3/20	3/20	3/20	0/20	0/20
Total		3/60	9/60	3/60	6/57	0/60	0/57
%		5	15	5	11	0	0

3. Column III. Less marginal leakage. The marginal leakage devices are subtracted from the count of Column II. The marginal leakage failures are those which have their measured leakages below the clamped values. The clamped values for each type are given in the table below; they are determined by the automated test set up.

	I_{SS}		I_{1H}/I_{1L}	
Type	25°C	125°C	25°C	125°C
CD4011A	159.8 nA	1598 nA	15.98 nA	159.8 nA
CD4013A	1598 nA	15.98 μA	15.98 nA	159.8 nA
CD4024A	1598 nA	15.98 μA	15.98 nA	159.8 nA

It is believed that in presenting the data this way, devices which indicate a higher probability of becoming non-functional in the application will be segregated from those devices which have leakage increases but that would not affect system functioning.

The data tabulated in Tables V, VI and VII, "Summary of Failure Attributes" has been plotted in Figs. 9 through 16. The graph paper used is log normal since this type of accelerated testing is expected to have a log-normal distribution. For the log-normal distribution, the failure rate at any given time can be calculated. The curve allows one to get a quick indication of whether the failure rate is increasing or decreasing. In addition, this type of plot provides the ability to determine the "freak" part, if it exists, and the main part of the distribution.

Figs. 9 and 10 indicate the failure rate at 250°C versus time. Some observations can be made at this point in regard to these results:

1. The percent of the CD4011A is significantly lower than those of the CD4013A or CD4024A.

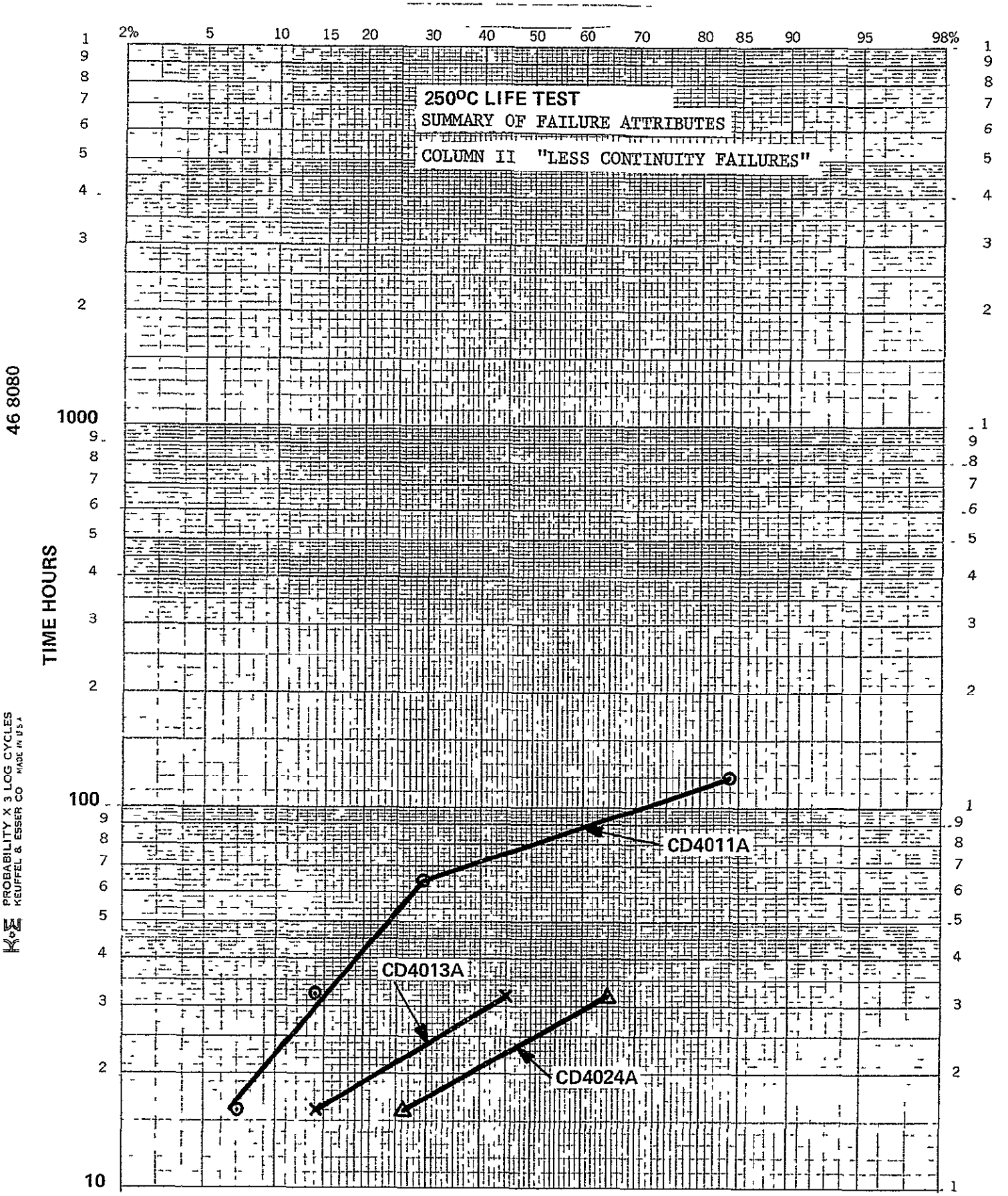

% CUMULATIVE FAILURES
2% 5 10 15 20 30 40 50 60 70 80 85 90 95 98%
250°C LIFE TEST
SUMMARY OF FAILURE ATTRIBUTES
COLUMN II "LESS CONTINUITY FAILURES"
TIME HOURS
1000
100
10
CD4011A
CD4013A
CD4024A
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 9

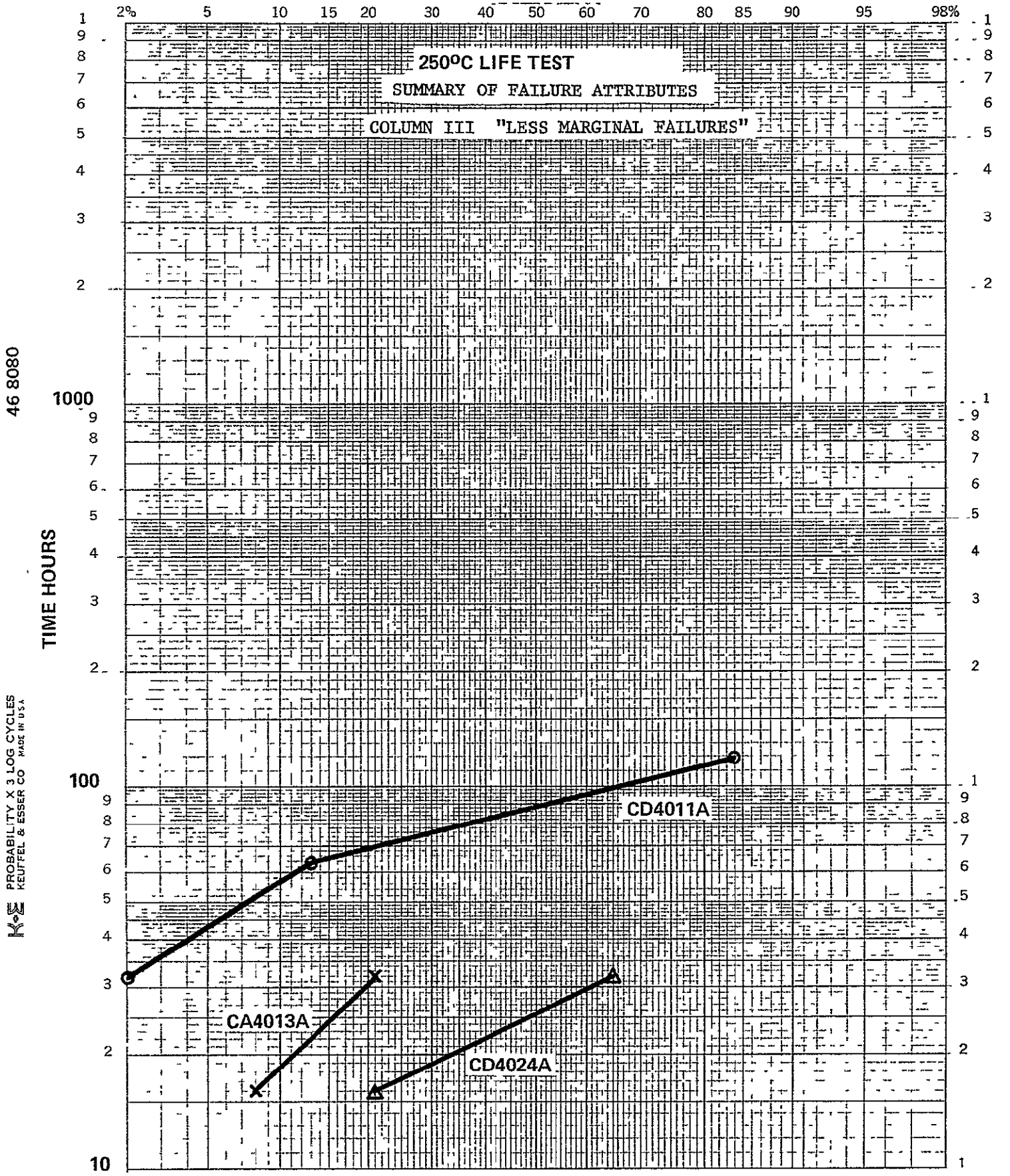

% CUMULATIVE FAILURES
2% 5 10 15 20 30 40 50 60 70 80 85 90 95 98%
250°C LIFE TEST
SUMMARY OF FAILURE ATTRIBUTES
COLUMN III "LESS MARGINAL FAILURES"
TIME HOURS
1000
100
10
CD4011A
CA4013A
CD4024A
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 10

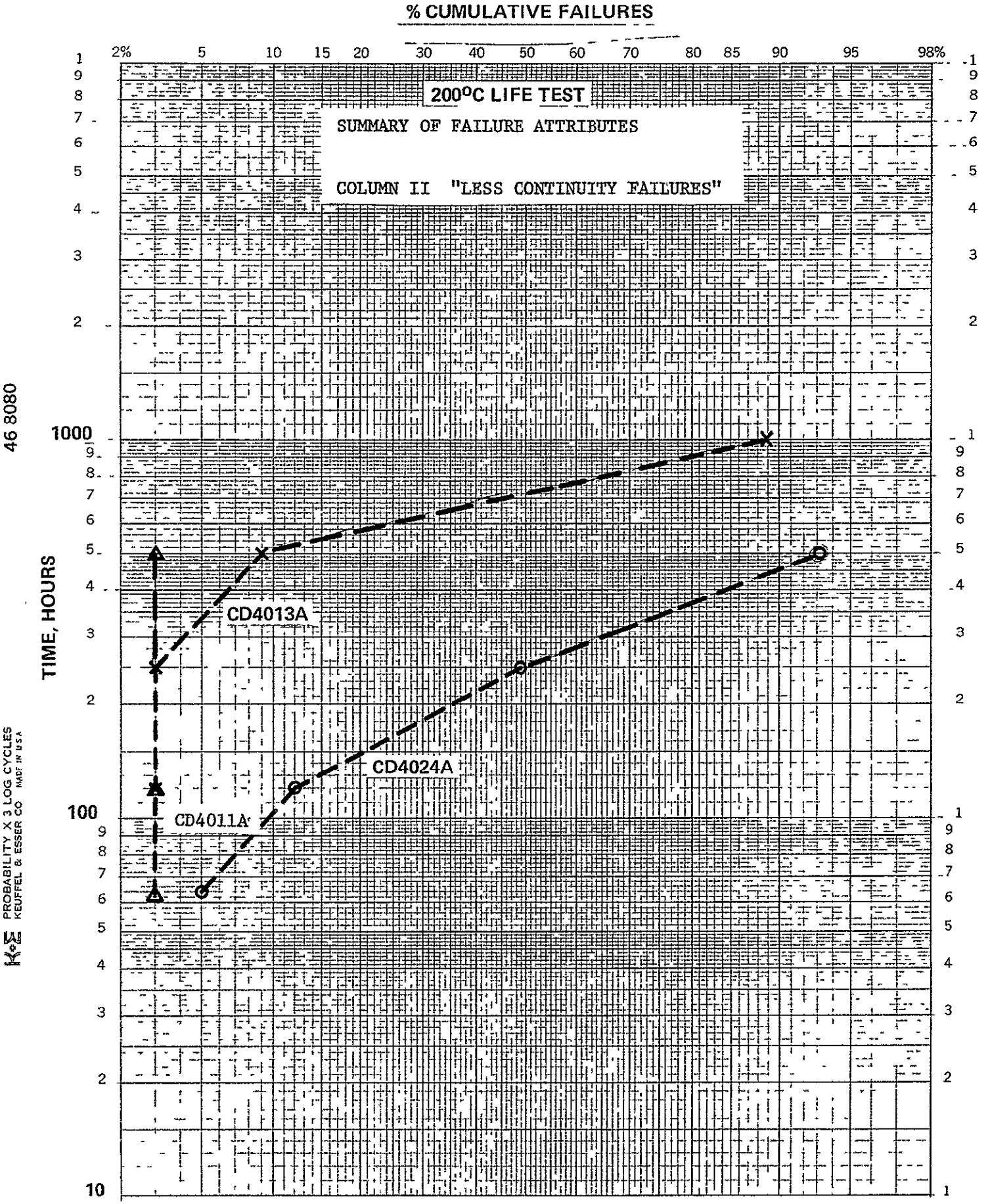

% CUMULATIVE FAILURES
2%
5
10
15
20
30
40
50
60
70
80
85
90
95
98%
200°C LIFE TEST
SUMMARY OF FAILURE ATTRIBUTES
COLUMN II "LESS CONTINUITY FAILURES"
TIME, HOURS
1000
100
10
CD4013A
CD4024A
CD4011A
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 11

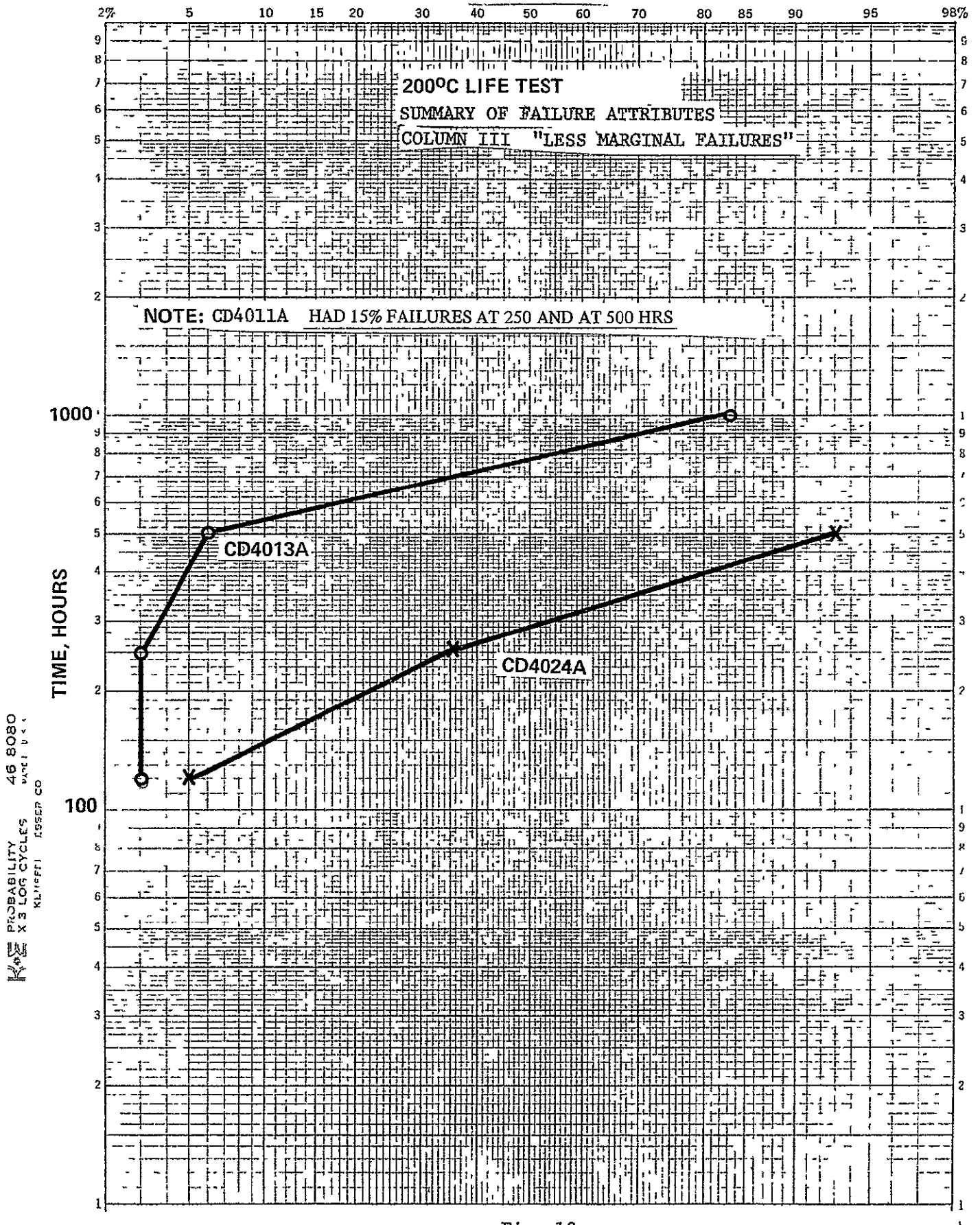

% CUMULATIVE FAILURES
2%
5
10
15
20
30
40
50
60
70
80
85
90
95
98%
200°C LIFE TEST
SUMMARY OF FAILURE ATTRIBUTES
COLUMN III "LESS MARGINAL FAILURES"
NOTE: CD4011A HAD 15% FAILURES AT 250 AND AT 500 HRS
CD4013A
CD4024A
TIME, HOURS
1000
100
PROBABILITY
X 3 LOG CYCLES
46 8080

Fig. 12

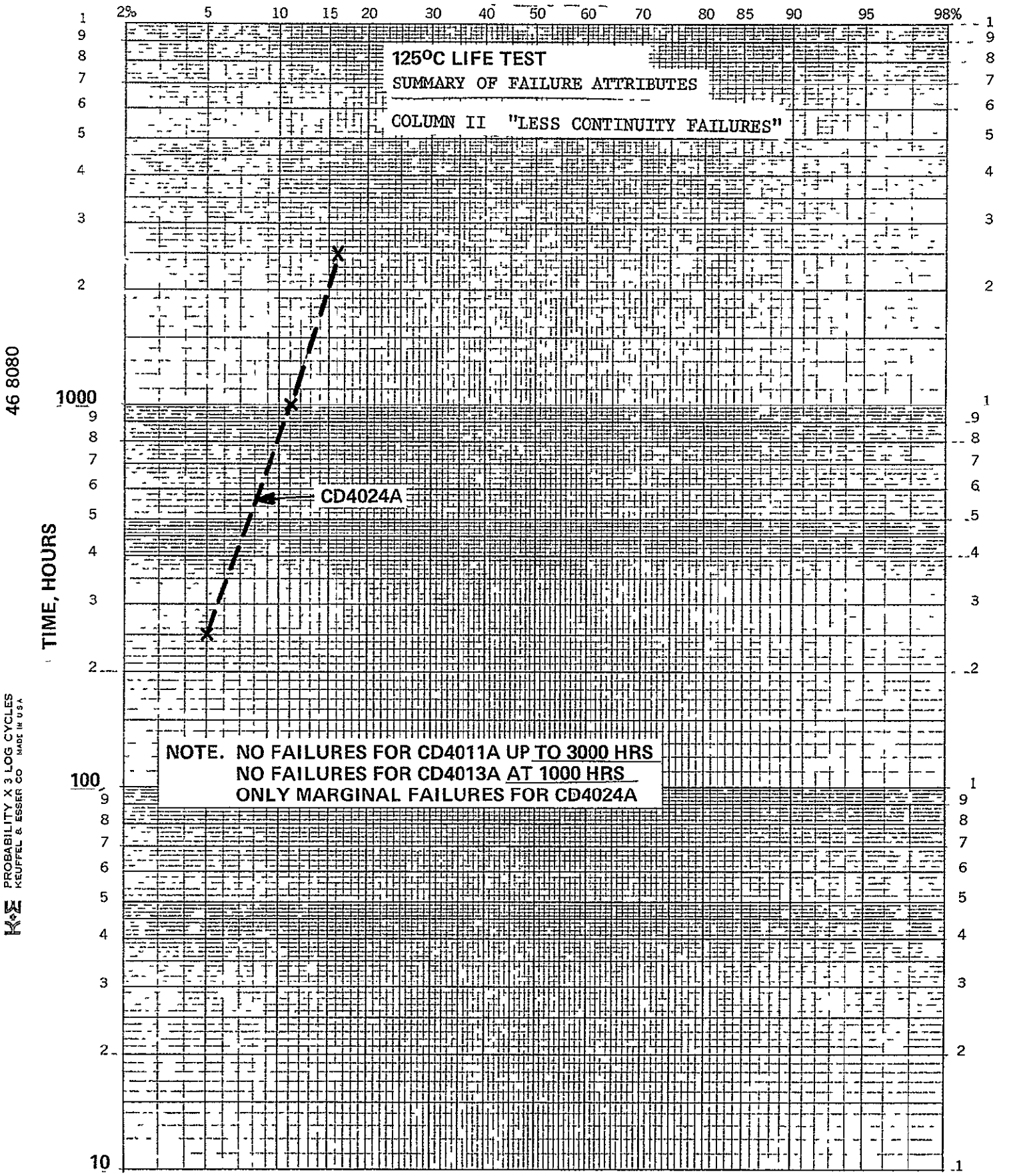

% CUMULATIVE FAILURES
2% 5 10 15 20 30 40 50 60 70 80 85 90 95 98%
125°C LIFE TEST
SUMMARY OF FAILURE ATTRIBUTES
COLUMN II "LESS CONTINUITY FAILURES"
CD4024A
NOTE. NO FAILURES FOR CD4011A UP TO 3000 HRS
NO FAILURES FOR CD4013A AT 1000 HRS
ONLY MARGINAL FAILURES FOR CD4024A
TIME, HOURS
1000
100
10
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 13

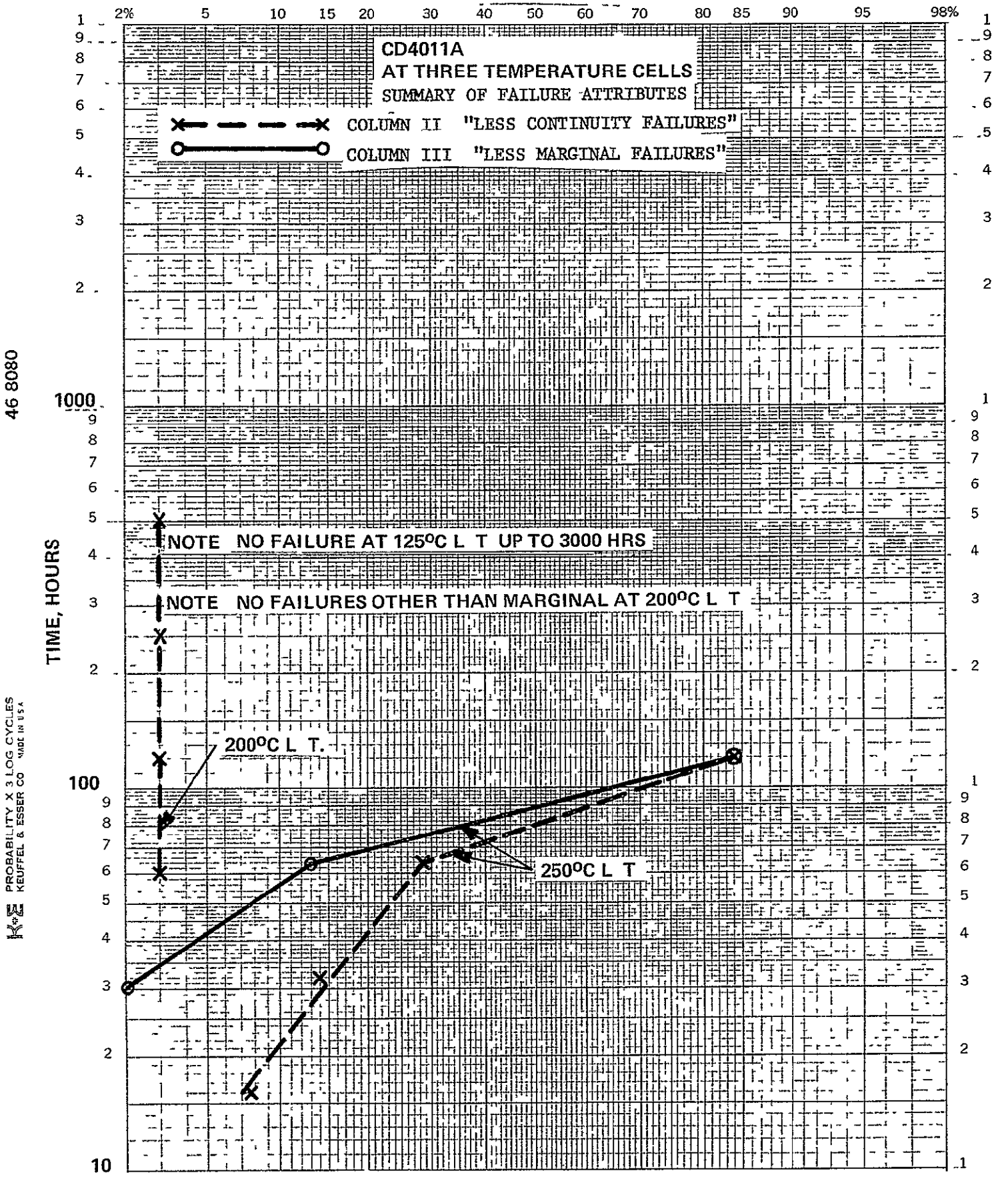

% CUMULATIVE FAILURES
2% 5 10 15 20 30 40 50 60 70 80 85 90 95 98%
CD4011A
AT THREE TEMPERATURE CELLS
SUMMARY OF FAILURE ATTRIBUTES
COLUMN II "LESS CONTINUITY FAILURES"
COLUMN III "LESS MARGINAL FAILURES"
NOTE NO FAILURE AT 125°C L T UP TO 3000 HRS
NOTE NO FAILURES OTHER THAN MARGINAL AT 200°C L T
200°C L T.
250°C L T
TIME, HOURS
1000
100
10
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 14

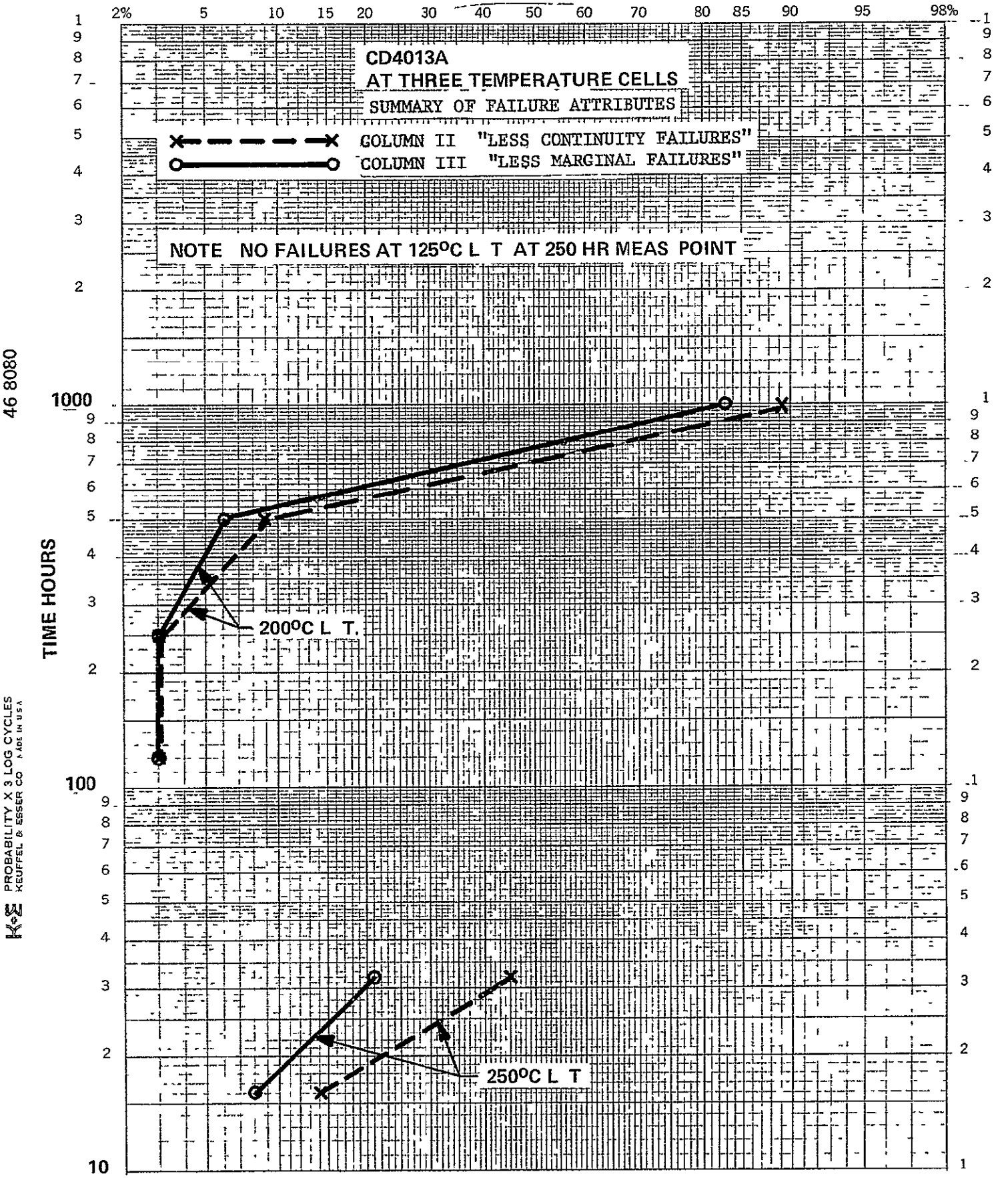

% CUMULATIVE FAILURES
2% 5 10 15 20 30 40 50 60 70 80 85 90 95 98%
CD4013A
AT THREE TEMPERATURE CELLS
SUMMARY OF FAILURE ATTRIBUTES
COLUMN II "LESS CONTINUITY FAILURES"
COLUMN III "LESS MARGINAL FAILURES"
NOTE NO FAILURES AT 125°C L T AT 250 HR MEAS POINT
TIME HOURS
1000
100
10
200°C L T.
250°C L T
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 15

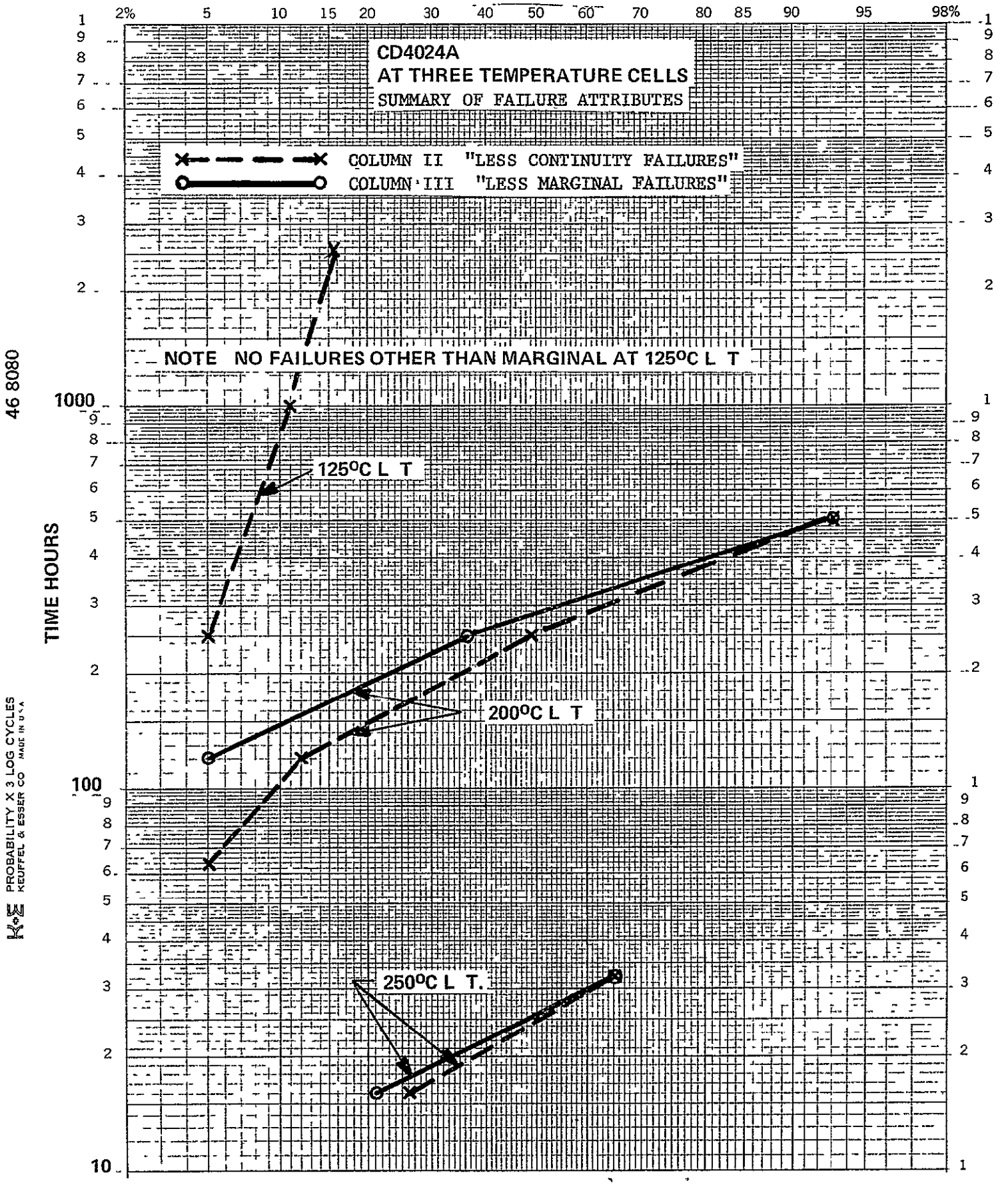

% CUMULATIVE FAILURES
2% 5 10 15 20 30 40 50 60 70 80 85 90 95 98%
CD4024A
AT THREE TEMPERATURE CELLS
SUMMARY OF FAILURE ATTRIBUTES
COLUMN II "LESS CONTINUITY FAILURES"
COLUMN III "LESS MARGINAL FAILURES"
NOTE NO FAILURES OTHER THAN MARGINAL AT 125°C L T
125°C L T
200°C L T
250°C L T.
TIME HOURS
1000
100
10
46 8080
PROBABILITY X 3 LOG CYCLES
KEUFFEL & ESSER CO MADE IN U.S.A.

Fig. 16

2. There is a noticeable increase of CD4011A failure rate and a change in distribution between the 64 hour and the 120 hour measurement points, indicating that perhaps some as yet unidentified threshold has been exceeded.
3. The difference in failure rates between CD4011A, CD4013A and CD4024A suggests a desirability to consider the chip size and/or the complexity of a microcircuit as a possible factor influencing failure rates. This observation supports a conclusion arrived at in another report prepared by RCA Solid State Division for the RADC, Contract #F30602-73-C-0282.
4. The high percentage of failures observed during the early measurement points (16 hours and 32 hours) as well as significant failure-rate changes between the 64 hour and the 120 hour measurement points suggest a desirability of even more frequent measurement points. This is especially applicable to the 250°C life test. Some improvement in that direction has been implemented, following consequent recommendation, by introducing the 32 hour and the 64 hour measurement points for the 250°C life test and the 64 hour measurement point for the 200°C life test.
5. For the present, we are inclined not to recommend the 250°C temperature for the accelerated life test for the following reasons:
   a. The three CMOS device types listed, CD4011A, CD4013A, and CD4024A did not meet the requirements for Class A conformance testing delineated in MIL Std 883A Method 5005.3, Table II(a), Subgroup 5; 250°C testing.
   b. There is strong evidence that a threshold may have been exceeded.
   c. Sample selection presents difficulty because solder-dipped leads, the standard finish for Class A devices, cannot be used at such high temperature.
   d. Presently available high-temperature carriers are too brittle and present considerable handling problems in the life test racks as well as the automated test equipment.

Figs 11 through 16 are included to give an insight into the failure rates at the 200°C life test and the 125°C life test. Although the early measurement points suggest lower failure rates, no definite statements to that effect can be made until data from more measurement points is available.

Tables VIII, IX, and X give for the 250°C test cell the means, the standard deviation, and the high value at each measurement point on the per lot basis for the surviving devices at two measurement temperatures, 25°C and 125°C. Figs. 17, 18, and 19 represent plots of mean averaged over three lots for each type and at two temperatures. The surviving units are defined as those the readings of which did not reach the clamped values. Clamped values are the upper limits of the instrument range to which the automated measurement system is set. The table on page 31 gives clamped values for I_{SS} for each type at 25°C and 125°C measurement temperatures.

There are three I_{SS} tests in the M58510/05001ADX (CD4011A) specifications The results of all three of these tests were used in the parameter trend tables and graphs. From the M38510/05101ADX (CD4013A) and M38510/05605ADX (CD4024A) test results, three I_{SS} tests for each type were selected to avoid presentation of repetitious data. The selected I_{SS} test data indicated the greatest parameter shift. The leakage versus time plot indicates a fair stability for the surviving CD4011A, but show considerable movement for the CD4013A and CD4024A. The 25°C measurements seems to track the 125°C measurements, indicating that for the purpose of observing leakage shift, both measurement temperatures are equally effective.

TABLE VIII – I_{SS} Trend with Time for the M38510/05001ADX (CD4011A)

Time			0 Hrs			16 Hrs			32 Hrs			64 Hrs			120 Hrs		
		Test #	50	51	52	50	51	52	50	51	52	50	51	52	50	51	52
	Lot #	Unit	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA
25°C Measurements	5361740	Mean	0 17	0 16	0 44	0 75	1 1	2 7	0 83	1 07	1 39	1	1 04	1 27	0 68	10 8	0 37
		S D	0 27	0 36	0 59	0 25	0 76	0 19	0 18	0 13	0 17	0 20	0 09	0 33	0 3	30 8	0 32
		H V	0 7	1	1 3	1 1	1 1	3	1 2	1 2	1 6	1 4	1 3	1 5	159 8	108 4	1 2
	6153050	Mean	0 65	1 01	1 37	2	1 32	3 4	3 73	3 22	5 55	3 55	3 48	5 21	2 2	1 76	0 70
		S D	0 4	0 1	0 16	2 2	0 44	0 56	6 31	1 28	7 87	2 3	0 91	3 8	2 89	1 19	0 14
		H V	1 2	1 2	1 7	3 1	3 1	5 6	30 4	8 2	38	11 8	6 3	19 7	10 8	3	0 9
	6153060	Mean	0 07	0 88	1 13	0 9	1 4	3 4	0 67	1 2	1 55	1 61	1 93	2 23			
		S D	0 09	0 1	0 12	1 2	1 1	2 3	0 35	0 32	0 34	0 78	0 54	0 75			
		H V	0 2	1	1 4	5 7	5 5	12 5	1 2	2	2 5	3 5	3 1	4 7			
125°C Measurements		Unit	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA
	5361740	Mean	100 2	67	74	125 7	100 3	72 1	131 7	96 9	73 4	134 6	89 8	72 8	301 4	457 5	115
		S D	19 6	39 7	16	26 4	19	14 6	28 4	20	15	33 4	23 5	15 6	361 1	415 1	24 4
		H V	136	109	98	172	132	97	188	137	103	193	133	104	1393	751	158
	6153050	Mean	143 7	64 1	126 2	175 1	103 8	130	180 1	97 1	125 2	196 1	89 1	230 8	259	395 2	103 6
		S D	53 3	36 6	31	47 7	26 2	36 5	53	17 6	39 7	60 4	22 8	295 2	137 1	509 2	30 8
		H V	222	103	197	265	124	197	284	125	200	292	117	1086	499	227	176
	6153060	Mean	63	79 6	51 3	76 7	79 3	48 5	77 1	78 6	49	45	42 8	27 7			
		S D	26	26 4	18 5	28	25 1	19 8	30 1	25 7	19 22	21	18 2	15 3			
		H V	138	140	91	134	136	84	132	136	83	86	80	55			

TABLE IX – I_{SS} Trend with Time for the M38510/05101ADX (CD4013A)

Time			0 Hrs			16 Hrs			32 Hrs			64 Hrs			120 Hrs
Lot #		Test # / Unit	50 nA	55 nA	60 nA	50 nA	55 nA	60 nA	50 nA	55 nA	60 nA	50 nA	55 nA	60 nA	
25°C Measurements	5393021	Mean	0 0	0 0	0 0	1 1	0 8	1 4	0 0	0 0	0 5				
		S D	0 0	0 0	0 0	4 6	0 8	1 0	0 0	0 0	1 0				
		H V	0 0	0 0	0 0	20 0	3 0	3 0	0 0	0 0	3 0				
	6123241	Mean	0 0	0 0	0 0	0 0	0 5	1 2	0 0	0 0	0 1				
		S D	0 0	0 0	0 0	0 0	0 8	1 1	0 0	0 0	0 2				
		H V	0 0	0 0	0 0	0 0	3 0	3 0	0 0	0 0	1 0				
	6153081	Mean	0 0	0 0	0 0	0 8	1 6	2 0	41 0	87 0	95 0	31 0	3 1 8	3 9 8	
		S D	0 0	0 0	0 0	2 4	2 6	2 6	140 0	360	390 0	89 0	1 1 7	1 3 7	
		H V	0 0	0 0	0 0	7 0	11 0	11 0	570 0	1500	1600	330	4 4-7	5 0-7	
125°C Measurements		Unit	µA	µA	µA	µA	µA	µA	µA	µA	µA	µA	µA	µA	
	5393021	Mean	0 093	0 07	0 092	0 27	0 12	0 19	0 67	2 5	2 4				
		S D	0 013	0 015	0 013	0 65	0 01	0 013	2 5	3 5	2 8				
		H V	0 12	0 12	0 12	3 0	0 13	0 14	11 0	13 0	8 2				
	6123241	Mean	0 11	0 12	0 12	0 28	0 19	0 21	0 08	11 0	0 13				
		S D	0 01	0 009	0 01	0 75	0 36	0 46	0 02	0 08	0 1				
		H V	0 13	0 13	0 13	3 5	1 7	2 2	0 13	0 42	0 52				
	6153081	Mean	0 072	0 074	0 074	0 24	0 57	0 64	0 84	0 5	0 53	0 58	0 28	0 35	
		S D	0 009	0 007	0 008	0 54	1 2	1 4	2 4	1 1	1 2	0 61	0 41	0 5	
		H V	0 09	0 09	0 09	2 3	4 5	5 4	9 1	3 5	3 8	1 6	1 1	1 3	

TABLE X – I_{SS} Trend with Time for the M38510/05605ADX (CD4024A)

Time			0 Hrs			16 Hrs			32 Hrs			64 Hrs			120 Hrs
		Test #	60	63	67	60	63	67	60	63	67	60	63	67	
Lot #		Unit	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	
25°C Measurements	6201051	Mean	45 81	53 35	55 8	33 4	35 7	34 2	41 7	103 7	82 3				
		S D	109 36	110 98	110 57	129	125 2	123	96 6	246 3	177 5				
		H V	418	417	418	565	564	555	578	580	565				
	6201061	Mean	1 11	3 35	2 88	0	9 6	8 75	11	12	12				
		S D	1 11	2 39	2 86	0	0 7	1 9	24	24	23				
		H V	4	11	13	0	11	16	114	113	112				
	6202232	Mean	2 31	4	2 25	1 42	10 85	8 4	20	20	17 2	782	779	761	
		S D	5	5 63	1 1	5 95	6	0 95	29	27 8	26 1	287	285	293	
		H V	23	27	4	26	37	9	99	103	101	1160	1153	1142	
125°C Measurements		Unit	µA	µA	µA	µA	µA	µA	µA	µA	µA	µA	µA	µA	
	6201051	Mean	0 42	0 54	0 54	0 70	0 77	0 73	1 2	1 2	1 9				
		S D	0 61	0 83	0 83	1 86	1 89	1 84	1 7	1 7	1 4				
		H V	2 34	2 96	2 95	8 4	8 41	8 41	6 03	5 76	5 24				
	6201061	Mean	0 18	0 21	0 21	0 17	0 19	0 18	3	3	3				
		S D	0 06	0 10	0 10	0 06	0 11	0 12	5	4	4				
		H V	0 37	0 55	0 56	0 29	0 28	0 28	0 5	0 49	0 50				
	6202232	Mean	0 12	0 12	0 12	0 24	0 22	0 22	0 45	0 44	0 43	7 58	All		
		S D	0 02	0 02	0 02	0 29	0 27	0 27	0 50	0 48	0 47	2 75	clamped		
		H V	0 2	0 21	0 21	1 4	1 35	1 32	1 7	1 7	1 6	9 39			

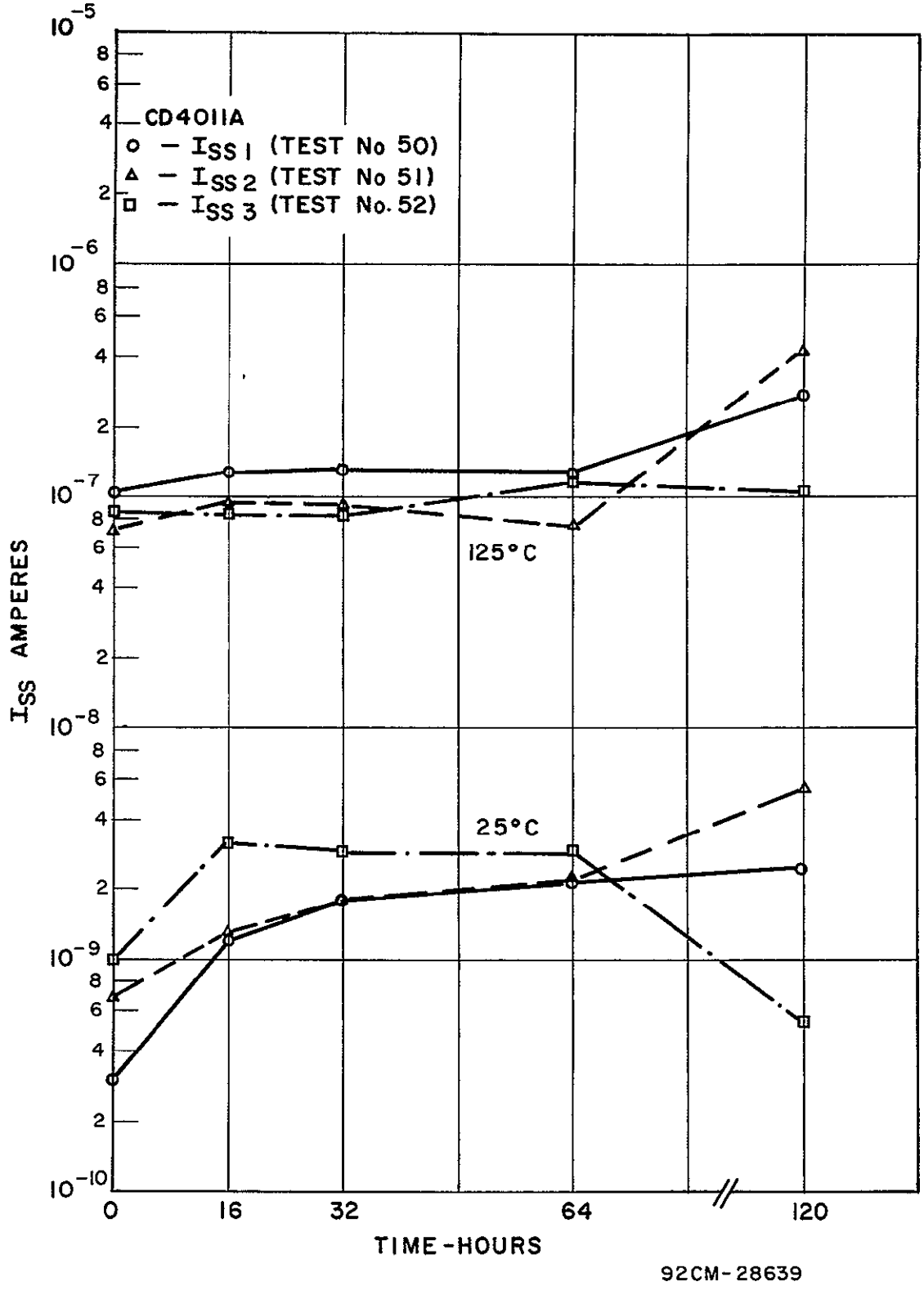


Fig. 17 - CD4011A; I_{SS} vs time; three-lot average of mean.

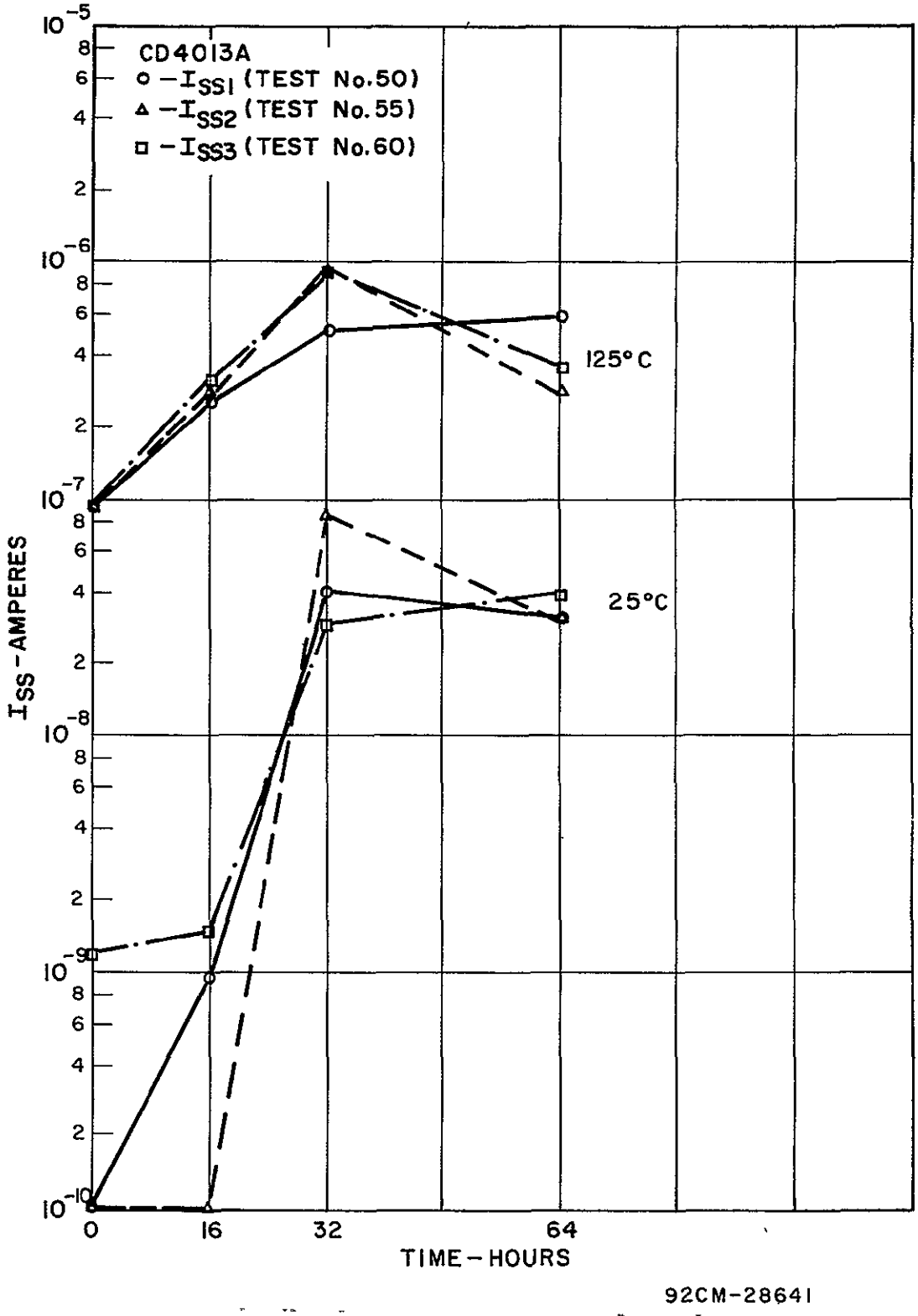


Fig. 18 - CD4013A; I_{SS} vs time; three-lot average of mean. Only one lot was kept on life test to 64 hours. Value of I_{SS} < 0.1 nA are plotted on the base line.

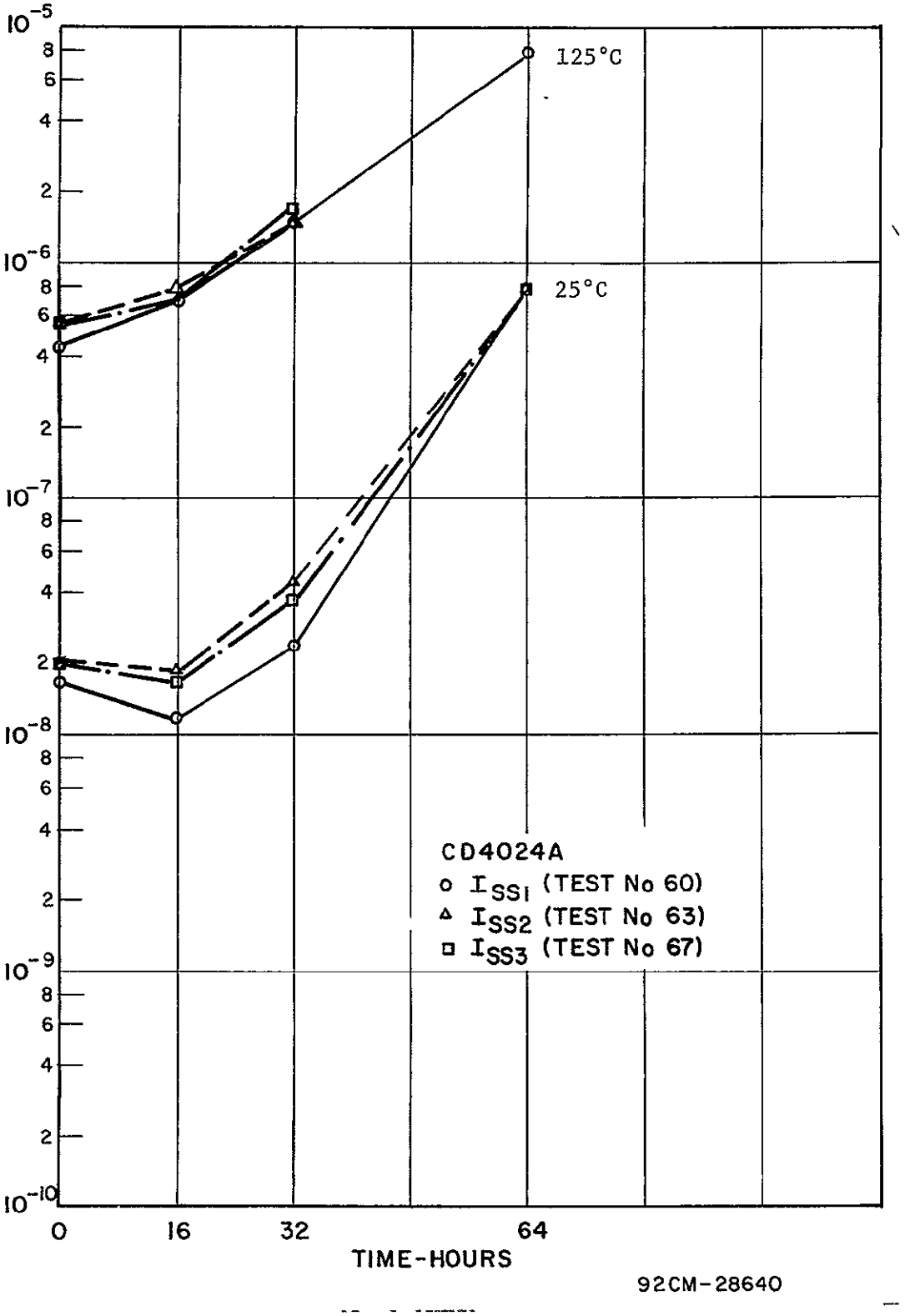


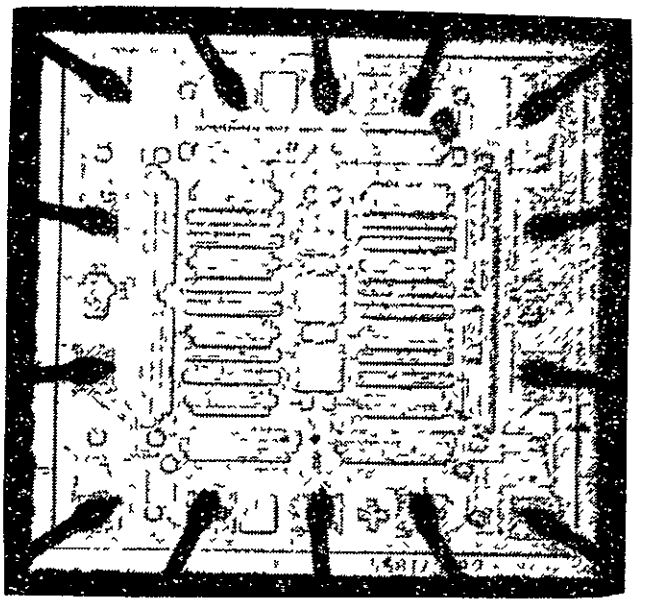
Fig. 19 - CD4024A; I_{SS} vs time; three-lot average of mean. Only one lot was kept on life test to 64 hours.

SECTION VII
PRELIMINARY FAILURE ANALYSIS

Two types of continuity failures were identified; socket problems and burned-out metallization. Test-socket problems are not considered as failures during accelerated testing.

Lot 6153060 (18/19) has failed continuity test at the 120-hour measurement point. Further tests confirmed open leads in 18 devices. External examination did not reveal lead oxidation sufficient to cause continuity problems. Consequently, two devices were opened and examined under a microscope. V_{SS} metal was found open in both devices. Fig. 20 shows photographs of one of the failed chips. No explanation for these failures will be offered at this point except to note that this type of failure is not likely to result from a gradual deterioration of the microcircuit. Further failure analysis of these devices is needed.

The predominant failure mode for all three device types is total leakage, I_{SS} and/or input leakage, I_{IL}, I_{IH}. To help determine the cause of the increase, leakage devices were baked at 200°C, no bias for 24 hours. These devices are being retested to determine whether the leakage levels have been reduced. Reduction in leakage after a high-temperature bake is generally considered as an indication of mobile ion presence.



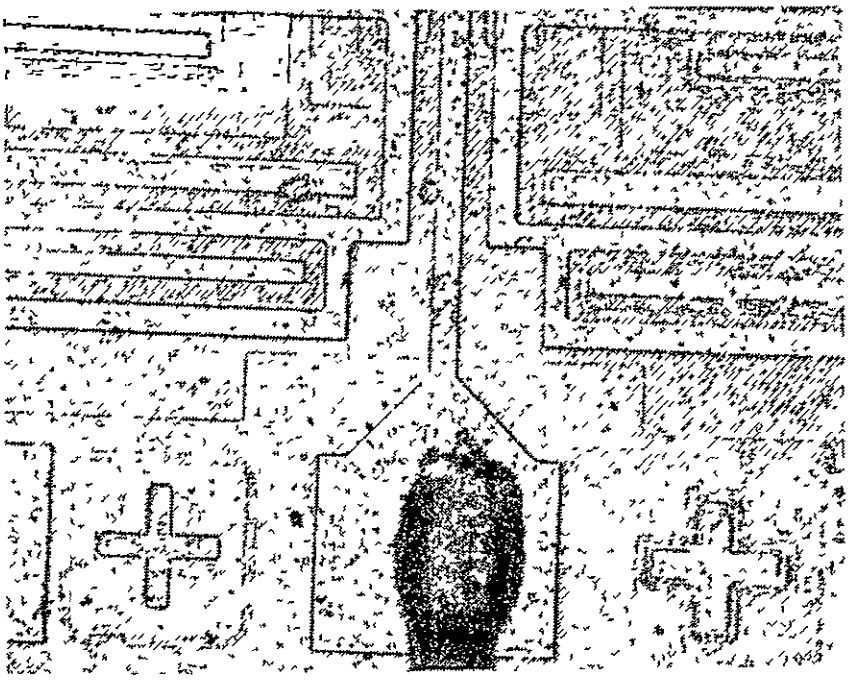


Fig. 20 - Photographs of failed CD4011 chips.

SECTION VIII
CONCLUSIONS

Recognizing that broad recommendations cannot be made until additional data is generated from Phases II and III, the following limited conclusions have been reached:

1. The three CMOS device types tested, CD4011A, CD4013A and CD4024A did not meet the requirements for Class A conformance testing delineated in MIL Std 883A Method 5005.3, Table II(a), subgroup 5; 250°C testing.

2. The utility of a 250°C accelerated life test as a predictor for CMOS long-term reliability at application temperatures has not been established.

SECTION IX
ACKNOWLEDGMENT

Acknowledgement is given Mr. E. Reiss for his guidance in this project, to Messrs. L. Campbell and F. Gusler for developing and implementing the computer test programs to Mr. H. Ahlers who had the difficult task of running an engineering program in a production environment, to Mr. C. Petrizzio and members of the Design Automation activity for their efforts in computer data analysis, and to Mr. S. Kukunaris for his help in statistical data analysis.