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# **HYBRID RECEIVER STUDY**

By

Marvin S. Stone  
Peter L. McAdam  
Oliver W. Saunders

April 1977

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Prepared under Contract No. NAS2-9367 by

TRW DEFENSE AND SPACE SYSTEMS  
Redondo Beach, California

for

AMES RESEARCH CENTER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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## ABSTRACT

This final report presents the results of a 4 month study to design a hybrid analog/digital receiver for outer planet mission probe communication links. The scope of this study includes functional design of the receiver; comparisons between analog and digital processing; hardware tradeoffs for key components including frequency generators, A/D converters, and digital processors; development and simulation of the processing algorithms for acquisition, tracking, and demodulation; and detailed design of the receiver in order to determine its size, weight, power, reliability, and radiation hardness. In addition, an evaluation was made of the receiver's capabilities to perform accurate measurement of signal strength and frequency for radio science missions.

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## 1. INTRODUCTION AND SUMMARY

This final report describes the work performed on NASA/Ames Contract No. NAS2-9367, Hybrid Receiver Study. The period of performance was 1 November 1976 to 1 March 1977. The contract monitor was Mr. Terry Grant of NASA/Ames.

The results of feasibility studies of missions to Jupiter, Saturn, and Uranus indicate the desirability of operating a flyby or orbiting spacecraft bus as a relay for the data acquired by the atmospheric probes. A hybrid receiver has been proposed as the vehicle for closing the probe-to-bus communication link in a way which allows maximum flexibility to mission planners, while minimizing development costs by using the same flight hardware for a variety of modulation types and data rates. A receiver which meets these requirements was analyzed and designed during the course of this study.

### 1.1 RECEIVER PERFORMANCE

The hybrid receiver has been designed to operate over a 20 MHz band centered about 1 GHz, with 20 channels spaced at 1 MHz intervals. A predominant characteristic of the probe communication link at this frequency is the magnitude of the doppler uncertainty over which the system must operate. The receiver has been designed to acquire, track, and demodulate over a total frequency uncertainty of  $\pm 80$  kHz (due to doppler spread and oscillator drift) and to track a doppler rate of  $\pm 50$  Hz/sec. The information bandwidth of the received signal ranges from 100 to 1000 Hz using either differential phase shift keyed (DPSK) or a continuous phase frequency shift keyed (CPFSK) modulation. The signal-to-noise ratios, defined in terms of the ratio of carrier power  $C$  to noise spectral density  $N_0$ , may be as low as 24.5 dB-Hz for 100 Hz, or 34.5 dB-Hz for 1000 Hz. These power levels correspond to an  $E_b/N_0$  of 4.5 dB at both the 100 and 1000 Hz information bandwidths.

The most important consideration in specifying the performance of the hybrid receiver is acquisition time. The active life of the nonrecoverable entry probe for Jupiter atmospheric tests has been estimated at 30 minutes. Of this time, 50 seconds has been allocated for receiver acquisition (minimum  $C/N_0$ , probability of acquisition greater than 0.995, and probability of false acquisition below  $10^{-4}$ ). One fundamental result of the tradeoff study was the determination that a conventional phase-locked receiver is unable to meet this acquisition time requirement by a wide margin. For this reason, a sequential acquisition procedure has been developed which not only achieves the required performance, but also avoids the complexity of performing parallel searches in frequency by means of multiple channels or FFT filtering.

When coarse frequency acquisition has occurred, the receiver is required to lock up and track a 50 Hz doppler rate with less than 1 Hz rms frequency error (1 second

average and strong  $C/N_0$ ). In order to accomplish this, a second order frequency-lock loop algorithm is incorporated. The receiver also performs bit synchronization with a transition tracking loop, and data demodulation for DPSK and CPFSK signals. Both the frequency and time tracking loops are optimum loops in the sense that the pre-detection signal-to-noise ratio is maximized by filtering to the data bandwidth, and the demodulation decisions are fed back to the tracking loops (data directed).

The results of extensive analysis and simulation of the hybrid receiver algorithms indicate that all performance specifications are met with margin. For initial acquisition, the probability of acquiring exceeds 0.995 at 45 seconds, while the false alarm rate is below  $10^{-6}$ . The frequency and time tracking loops are able to acquire and track at 24.5 dB  $C/N_0$  not only for 100 Hz of data but also at 1000 Hz. These tracking loops yield a frequency variance of 3 Hz and time jitter of less than 1% at minimum  $C/N_0$ . Simulation of the entire receiver demodulation sequence shows a performance which is within 0.5 dB of the theoretical performance of DPSK and CPFSK signaling. Table 1-1 lists the key performance specifications and capabilities for the hybrid receiver.

Table 1-1. Hybrid Receiver Performance

Performance Parameter	Specification	Capability
Frequency (selectable)	1000 $\pm$ 10 MHz	991, 992, ..., 1011 MHz
Doppler uncertainty	$\pm$ 80 kHz	$\pm$ 80 kHz
Maximum doppler rate	$\pm$ 50 Hz/sec	$\pm$ 50 Hz/sec
Minimum signal	-146 dBm	-146 dBm
Maximum signal	-116 dBm/Hz	-116 dBm
Maximum noise ( $N_0$ )	-166 dBm/Hz	-166 dBm/Hz
Minimum noise ( $N_0$ )	-170 dBm/Hz	-170.5 dBm/Hz
Minimum operating $C/N_0$	24 dB-Hz	24.5 dB-Hz
Minimum signal BW	100 Hz	100 Hz
Maximum signal BW	1000 Hz	1000 Hz
Acquisition time (24.5 dB-Hz)	50 sec	45 sec
Probability of acquisition	0.995	0.995
Probability of false acquisition	$10^{-4}$	$<10^{-4}$
Frequency track error*	1 Hz	0.2 Hz

\* $C/N_0$  = minimum plus 20 dB, maximum doppler rate

In addition to the demodulation functions, the hybrid receiver design lends itself to extremely accurate measurements of frequency and signal strength. Table 1-2 lists the capabilities of the hybrid receiver in estimating these parameters for the purposes of radio science missions. Because the entire receiver is coherently tied to a single frequency reference and all frequency tuning is done digitally (without voltage controlled oscillators), frequency resolution to 0.14 Hz

Table 1-2. Radio Science Performance

Performance Parameter	Statement of Work Specification	Receiver Capability
<u>Signal Power Measurement</u>		
Accuracy	±1 dB	±0.7 dB
Gain stability	±0.1 dB	±0.1 dB*
Averaging times	1 to 60 sec	1,2,4,8,16,32,64 sec
Estimate uncertainty (3σ)		
1 kbps, C = -116 dBm (high SNR)		
Single sample	—	±0.04 dB
0.1 sec (100 samples)	—	±4.3 x 10 <sup>-3</sup> dB
10 sec (1000 samples)	—	±4.3 x 10 <sup>-4</sup> dB
100 bps, C = -146 dBm (low SNR)		
Single sample	—	±3 dB
1 sec (100 samples)	—	±0.41 dB
60 sec (6000 samples)	—	±0.056 dB
<u>Frequency Measurement</u>		
Frequency Resolution	TBD	±0.114 Hz (24-bit command)
Averaging times	1 to 60 sec	1,2,4,8,16 sec
Frequency uncertainty (3σ)		
100 bps, D = 50 Hz/sec, C = -126 dBm		
Single sample	—	±3.78 Hz
1 sec (100 samples)	—	±0.378 Hz
5 sec (500 samples)	—	±0.169 Hz
10 sec (1000 samples)	—	±0.119 Hz
1 kbps, D = 50 Hz/sec, C = -136 dBm		
Single sample	—	±7.53 Hz
1 sec (1000 samples)	—	±0.24 Hz
5 sec (5000 samples)	—	±0.11 Hz
10 sec (10,000 samples)	—	±0.076 Hz

\* Assumes regulated power to front end

is possible and filtered doppler estimates can be made with uncertainties below 0.25 Hz. For measuring incoming signal strength, assuming accurate power regulation is provided for the front end RF/IF circuitry, the fixed gain front end (no AGC amplification) allows extremely accurate relative gain measurements. By averaging for periods up to 60 seconds, the estimates of signal strength can be made with relative uncertainties below 0.1 dB.

The accuracies of both the frequency and time estimates are felt to be difficult or impossible to achieve using conventional analog receiver techniques.

## 1.2 RECEIVER CHARACTERISTICS

The hybrid receiver has been designed to meet severe environmental and physical requirements. The tightest environmental restrictions placed on the system are in the areas of power dissipation, reliability, and radiation hardness. The hybrid receiver consumes a total of 12 watts of regulated power for a single unit, including all the RF-IF equipment, the A/D conversion, frequency generation, and digital signal processing. This unit is estimated to have a reliability over the 8 year lifetime of the mission of 0.941. Since the specification requires reliability greater than 0.98, two units are called for, one in a stand-by powered down mode. In this configuration, a 0.997 reliability is achieved and no single point failure exists.

The outer planet mission profiles indicate a probable radiation dose of up to 200K rad(Si). At these levels, severe performance degradations can occur in both digital and analog circuits. For this reason, the hybrid receiver was designed using only parts which are inherently radiation resistant, thereby eliminating the need for radiation shielding. The amplifier chain in the analog portions of the radio is constructed using parts which have been previously used on radiation resistant military spacecraft programs or have been radiation tested. In addition, only fixed gain amplifiers have been chosen, thereby eliminating any AGC circuits as sources of degradations. The sample and hold circuits are designed using J-FET's and radiation-hard operational amplifiers. The analog-to-digital converter is a monolithic device developed for the Air Force for radiation hardened applications. Frequency generation for receiver tuning is done in the digital domain, thereby eliminating any VCO problems. The entire digital processor is designed using only bipolar technology. Tradeoff studies dictated the use of bipolar instead of the slightly lower powered C-MOS family because the performance of C-MOS has been shown to degrade in a high radiation environment and C-MOS cannot meet the processing speed requirements.

Figure 1-1 illustrates the environmental and physical characteristics of the hybrid receiver, the packaging concept for the flight hardware, and the fundamental performance capabilities of the design.

### 1.3 RECEIVER DESCRIPTION

The hybrid receiver combines the positive attributes of analog and digital signal processing to achieve a design with maximum flexibility and minimum complexity. The design is based to a large extent on existing analog and digital subassemblies and circuits in order to minimize development cost and risk. The receiver incorporates several unique features which result in significant simplification and/or performance advantages relative to conventional analog receiver design. These features are:

- Fixed RF/IF gain — No AGC
- Digital frequency generation — No VCO
- IF sampling — No I-Q balance problems
- Sequential detection for rapid acquisition
- Digital signal processing for improved performance and flexibility.

These features are based on proven design principles and make maximum use of previously developed hardware to minimize development cost and risk. In arriving at the final design of hybrid receiver, the criteria used for making design selections were:

- Satisfying the stated performance specifications
- Minimizing the design complexity to reduce size, weight, and power, and to increase reliability.
- Maximize the flexibility of the design to accommodate varying mission requirements
- Utilize existing designs where feasible.

A functional diagram of the hybrid receiver is shown in Figure 1-2.

The design utilizes a triple conversion front end, the third step being an I-Q digital downconversion within the sample-and-hold and A/D converter. The received 1 GHz signal is first bandpass filtered to a 20 MHz bandwidth in a stripline filter, amplified in a two-stage preamplifier module, and amplified again in another two-stage amplifier. The filter bandwidth accommodates any input frequency in the 1000  $\pm$ 10 MHz range without redesign, as required. The noise figure for this front end is 3.2 dB and the amplifiers provide a self-limiting feature to protect against large input signals (up to -10 dBm). The design is an adaptation of a TRW L-band receiver used on a military satellite program.

The L-band signal is downconverted to a first IF of 31 MHz, where the signal is amplified again and bandpass filtered. The crystal filter at 31 MHz is a 4-pole amplitude equalized filter having a 3 dB bandwidth of 210 kHz, which accommodates the maximum frequency uncertainty of  $\pm$ 75 kHz due to doppler and any offsets due to oscillator drift. The design of this IF strip is taken directly from the TRW work for the

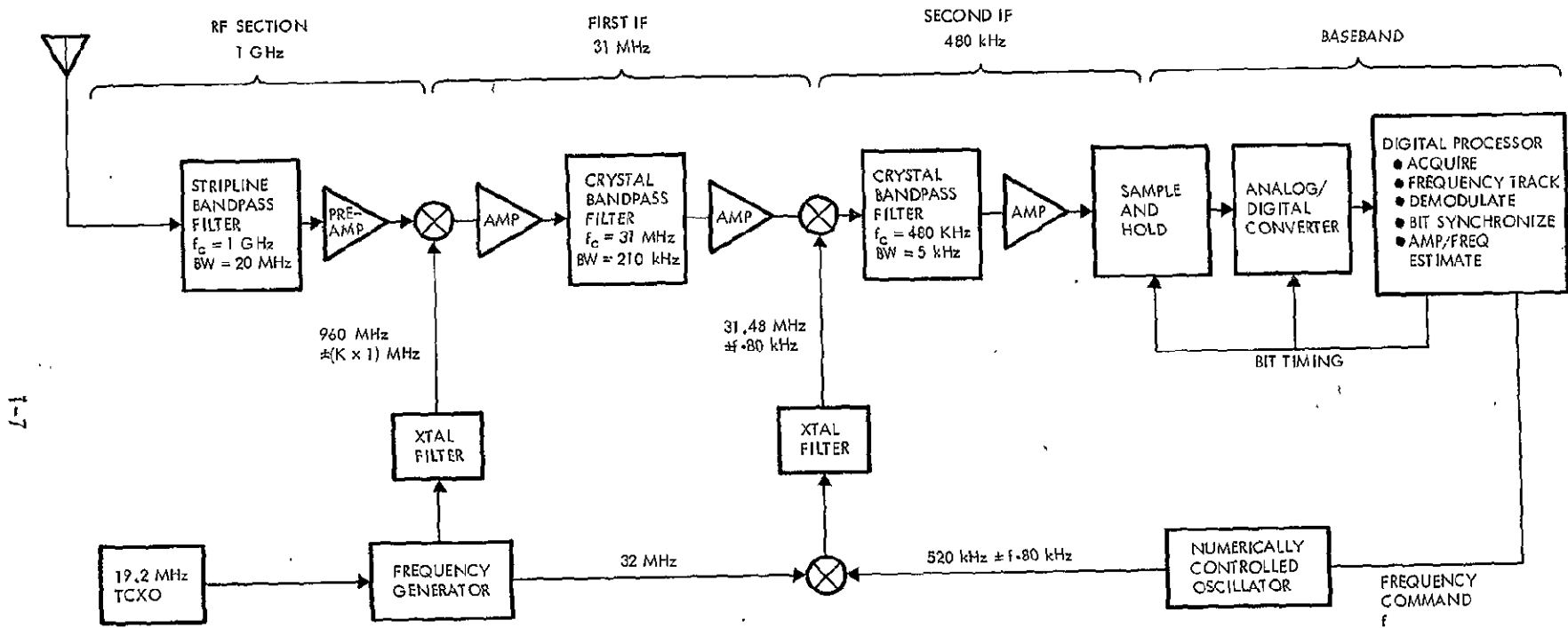


Figure 1-2. Hybrid Receiver Functional Diagram

Space Shuttle S-band communications program. The LO source for the 1st downconversion is obtained by selecting (via crystal filter) the desired mixing signal from a comb of frequencies spaced at 1 MHz intervals, thereby providing 20 separate channels in the interval from 991 to 1011 MHz. The comb of frequencies is generated by multiplying the 19.2 MHz reference to 192 MHz, and mixing with a comb of frequencies spaced at 200 kHz which in turn are also generated from the 19.2 MHz source. The resulting 192 MHz comb is filtered to acquire the desired spectral line, and multiplied times 5 to get to 960 MHz. Since all mixing operations are coherent with the 19.2 MHz precision reference, the resulting LO reflects the stability of the 19.2 MHz reference. Assuming a space qualified TCXO, the stability of this LO is  $5 \times 10^{-7}$  per year (long term) and  $1 \times 10^{-9}$  per second (short term). The short term variance at 1 GHz is 1 Hz/sec rms, which is sufficient to allow radio science frequency estimation for averaging times between 1 and 60 seconds.

A second downconversion accomplishes the tuning of the receiver across the 160 kHz doppler range, and yields a second IF signal at 480 kHz. This signal is filtered to a bandwidth of 5 kHz, amplified, and applied to the sample and hold circuit for digitizing. The frequency source for the second downconversion results from mixing a 32 MHz reference ( $19.2 \text{ MHz} \times 5 \div 3$ ) with a tuning signal which is generated digitally in a numerically controlled oscillator (NCO). The NCO operates by incrementing a phase accumulator  $3.84 \times 10^6$  times per second with an incremental phase generated by the digital processor. This incremental phase is a 24-bit binary word which constitutes the frequency tune command, and has a resolution of 1/4 Hz across the range from 440 to 600 kHz. The resulting phase ramp is mapped to an amplitude, converted to an analog voltage, and filtered to produce the offset tuning source.

The advantage of using a digital NCO for tuning lies in its inherent stability and simplicity. A conventional tunable VCO with a digital-to-analog interface to convert frequency commands to control voltages is replaced by a simple synthesizer with a direct digital interface to the processor. The result is a clean high reliability digital-to-frequency interface design which eliminates the necessity for the high resolution (19 bits for 0.25 Hz resolution) D/A converter needed to attain the specified tuning accuracy with a VCO. A D/A converter is used in the synthesizer, but it requires only 8 bits of resolution. In addition, the long term frequency accuracy reflects that of the 3.84 MHz clock. Since both the 32 MHz reference and the 3.84 MHz clock are derived from the 19.2 MHz oscillator, the overall receiver stability is locked to the precision reference.

The 480 kHz signal is sampled directly at the second IF by a sample and hold circuit and the samples are quantized to 8 bits in the A/D converter. The sample and hold has an aperture time of 100 psec, which introduces negligible degradation to the sampling process due to sampling time jitter. The 8-bit A/D converter is a monolithic chip of the successive approximation type which is radiation hardened and

designed for a maximum clock rate of 13 MHz. The A/D converter is a lower power version of a design developed for the Air Force Avionics Laboratory (AFAL).

The input signal to the sample and hold circuit is 5 kHz wide. Calculations show that in this bandwidth the total signal plus noise power varies 17.8 dB as the signal goes from -146 to -116 dBm. By selecting the nominal loading point of the A/D converter to be -4 dB (ratio of rms signal power to A/D input clipping level), the digitizing process introduces quantization noise which is at least 20 dB below the thermal noise over the entire 30 dB variation in signal power. In addition, with signal absent the noise alone loads the A/D to level 8 which allows sufficient quantization to accurately perform the coarse acquisition sequential detection algorithm. Thus the entire receiver front end can be operated with fixed gain, eliminating the need for AGC.

In addition to digitizing the signal, the sampling process accomplishes the final downconversion to baseband, and separates the signal into inphase and quadrature channels. This is accomplished by taking successive pairs of samples spaced by an odd number of quarter cycles at the frequency being converted to baseband. For truly narrowband signals of bandwidth less than the sampling rate, this process yields alternating inphase and quadrature samples from the A/D converter. The advantage of this approach lies in its simplicity. The complex and costly quadrature hybrids, mixers, amplifiers, filters, and redundant A/D converters classically used in an analog implementation of the interface with the digital processor are all replaced by a simple direct digital interface. The result is a simple, high reliability analog/digital interface design which eliminates the alignment and balancing procedures normally associated with analog I/Q circuitry.

The quantized baseband I-Q samples are transferred to a high speed digital signal processor (DSP) for acquisition and tracking as well as demodulation and symbol synchronization. It was determined that the coarse frequency acquisition requirement was the determining factor in the design of the DSP. A modified sequential detection algorithm was selected for the hybrid receiver because it does not require parallel operations on multiple frequencies, and therefore eliminates the need for high speed (and high power) FFT processing. This algorithm processes a single frequency hypothesis at a time, sweeping across the region of uncertainty in search of the additional energy represented by the signal over the thermal noise.

Once the presence of the signal within a given frequency hypothesis has been detected, the processor enters a pull-in mode to establish coarse frequency and symbol synchronization by performing high rate frequency discrimination and bit transition detection. When coarse sync has been established, the processor begins tracking with a decision directed second order frequency-lock loop and transition tracking loop. In addition, the processor demodulates either differentially coherent PSK or continuous phase FSK data. Section 1.4 discusses the operation of the processing algorithms in greater detail.



The digital signal processor is a simplification of a high speed microprocessor developed for the Joint Tactical Information Distribution System (JTIDS) program. The JTIDS microprocessor was chosen as the basis for the DSP because it is a proven parallel design with low power and sufficient speed to allow execution of the signal processing algorithms with the desired computational margin. The DSP consists of a central processor containing an arithmetic logic unit, a monolithic hardware multiplier, random access memory for computational storage, and permanent read only memory for parameters and constants. In addition, the processor contains control memory for program storage, control circuitry for execution and program control, and address distribution logic for data movement and control transfer (branching). Figure 1-3 shows a functional diagram of the microprocessor. The basic architecture of the DSP utilizes simultaneous 8-bit

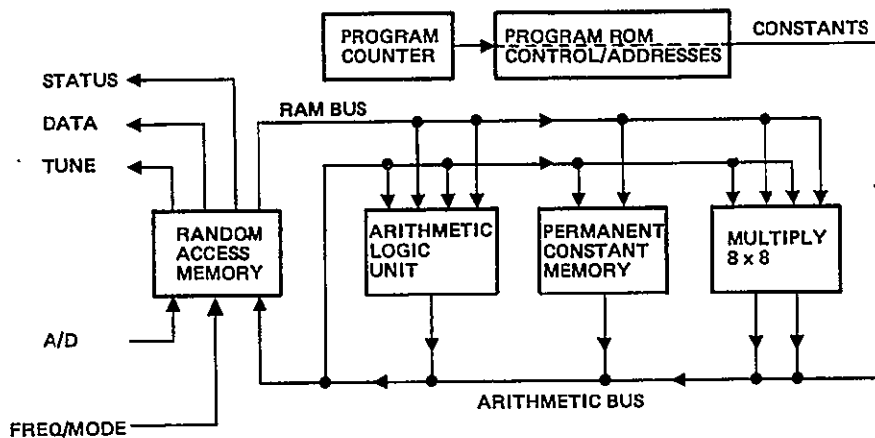


Figure 1-3. Digital Signal Processor Functional Diagram

parallel processing in the arithmetic unit and multiplier. The processor is configured to perform multiple precision arithmetic as needed for the signal processing algorithms. Most of the processing requires 16-bit precision, since the bulk of the algorithms call for multiplication of the 8-bit input samples with 8-bit constants as the initial step, yielding a 16-bit product. The advantage to building the processor as an 8-bit machine is in complexity and power. The total count for the DSP is 54 parts and the total power is just under 6.5 watts. Using the low power Schottky logic family in an 8-bit configuration takes advantage of a favorable speed-power product while trading higher speed for reduced parts count. The resulting design is well matched to the processing requirements of the hybrid receiver, using just under 50% of the processing speed for the worst case acquisition algorithms, and roughly 60% of the available program memory. Table 1-3 presents a summary of the processor utilization in both speed and memory as a function of the various algorithms.

Table 1-3. Processor Utilization

Function	Execution Rate		Program Size	
	Instruct/sec	%	Instruct	%
Coarse Acquisition	640k	32	80	15
Fine Acquisition	800k	40	55	10
Tracking/Demod.	200k	10	120	25
Overhead	200k	10	50	10
Maximum*/Total	1000k	50	305	60

\*Fine acquisition plus overhead represents maximum load

The digital signal processor provides for inputs from the A/D converter and an external 8-bit parallel entry port for mode control and frequency estimate inputs. Three 8-bit output ports are also available. The first port transfers the 24-bit frequency command to the NCO in three bytes. The second port is for demodulated data output. The third provides a programmable port for frequency estimates, signal power estimates, and receiver status. Figure 1-3 shows the digital signal processor interfaces as well as the functional diagram.

Table 1-4 is a summary of the design derivations for each of the major components of the hybrid receiver.

Table 1-4. Hybrid Receiver Component Derivation

<u>Component</u>	<u>Program Derivation</u>
1 GHz front end	Modification of an L-band receiver from military spacecraft program
31 MHz 1st IF	Direct application from Space Shuttle and L-band receiver
Frequency generator	Modification of FLTSATCOM frequency generator
19.2 MHz TCXO	Space qualified from FEI
A/D converter	Existing radiation hardened unit developed for AFAL
Numerically controlled oscillator	Existing design developed for a wideband frequency hopper
Digital signal processor	Simplification of the JTIDS microprocessor

## 1.4 RECEIVER OPERATION

The hybrid receiver has three modes of operation:

- Coarse frequency acquisition
- Coarse frequency tracking and bit timing (fine acquisition)
- Demodulation and decision directed tracking.

The signal acquisition sequence begins in the coarse frequency search algorithm. In this first processing stage, the  $\pm 80$  kHz frequency uncertainty is reduced to within the pull-in capability of the frequency-lock loop. This is accomplished by means of a sequential detection algorithm as shown in Figure 1-4. The basic idea of sequential detection is to step the receiver across the frequency uncertainty region until the signal is detected. Energy detection is used with post detection integration to improve the signal-to-noise ratio. The receiver tunes to a frequency hypothesis and integrates the incoming energy. If the accumulated energy rate falls below a pre determined threshold, the signal is assumed not to be at that frequency and the receiver is stepped to the next hypothesis. If the energy remains above the threshold for a preselected dwell time, a signal detection is declared and the coarse frequency tracking commences. If the full 160 kHz range is swept and no signal has been detected, the NCO is reset back to the starting frequency and the process repeated. The threshold, integrating filter bandwidth (selected to be 1000 Hz), and filter dwell time were chosen to minimize acquisition time.

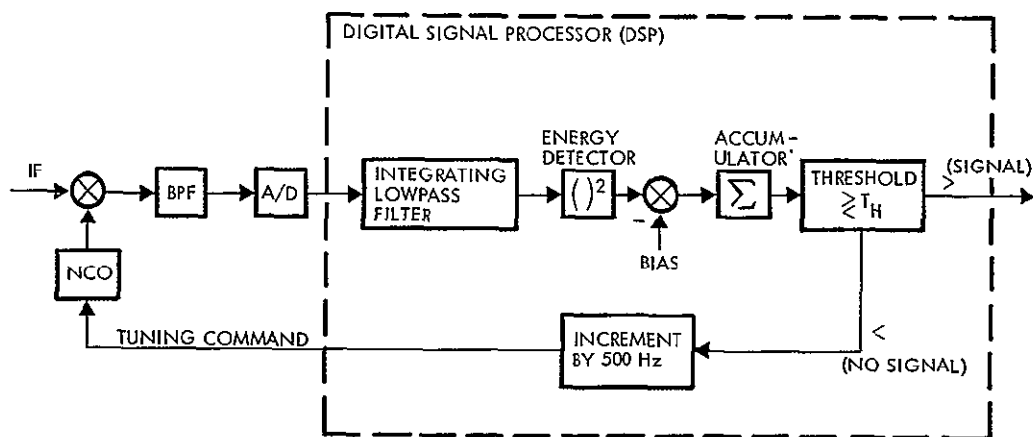


Figure 1-4. Coarse Frequency Acquisition

After the presence of a signal has been detected, the coarse frequency tracking and bit timing algorithms are executed to bring the receiver into lock in preparation for data demodulation. The coarse frequency tracking algorithm, shown in Figure 1-5, resolves the carrier frequency of the signal to less than 10% of the data rate. This is accomplished by a digital frequency discriminator followed by a second order low-pass filter. The average discriminator signal output is proportional to the

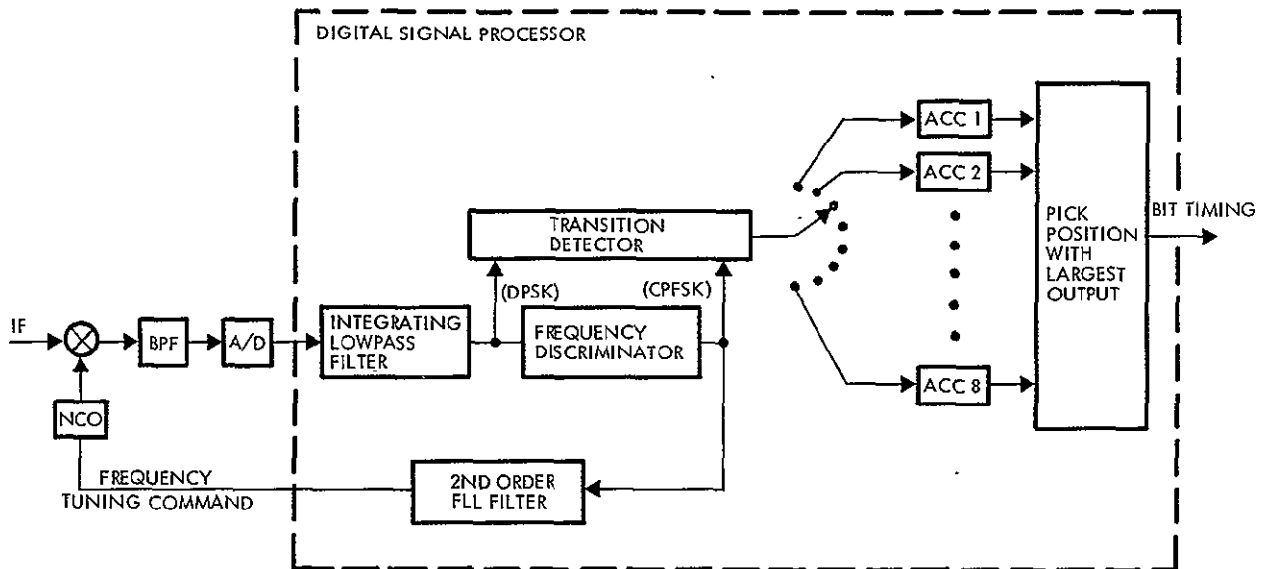


Figure 1-5. Coarse Frequency Tracking and Coarse Bit Timing

frequency of the input signal. For DPSK signals, the discriminator regenerates the suppressed carrier, for continuous phase FSK signals, the discriminator output corresponds to one of the two signal frequencies which are evenly spaced on either side of the carrier. By lowpass filtering the discriminator output, an estimate of the suppressed carrier frequency is obtained. A second order filter is used to track the signal with the doppler rate without introducing a frequency bias into the estimate. This loop filter output is then used to generate a frequency command to the NCO. As the estimate of the carrier frequency improves, the discriminator output goes to zero. The pull-in range of the frequency-lock loop is determined by the rate at which the frequency discrimination is performed. In the coarse frequency tracking processing, the discriminator is operated at a rate of 8 kHz corresponding to a pull-in range of  $\pm 4$  kHz. This allows the receiver to lock onto the main signal lobe even if the coarse acquisition algorithm happens to detect a signal sidelobe rather than the true carrier.

The second stage processing also includes a coarse bit timing estimator which resolves timing to within 1/16th of the bit duration (see Figure 1-5). This is accomplished by searching for phase transitions, in the case of DPSK, or frequency transitions, for CPFSK, which occur every  $T_B$  seconds ( $T_B$  is the data bit duration). A bank of eight integrators, spaced  $T_B/8$  seconds apart is used to average the transition detector output sampled at the data rate. At the end of fine frequency acquisition, the summer with the largest signal is taken to correspond to the first sample in the data bit thereby establishing time to within 1/16 of a bit. For DPSK data the phase transition detector takes its inputs directly from the pre-detection lowpass filter. For CPFSK data, the frequency transition detector derives its output signal from the discriminator.

Once frequency and coarse bit timing have been acquired, demodulation and decision directed tracking begins. The DPSK demodulation algorithm is shown in Figure 1-6. An integrating filter is used to filter the input down to the data bandwidth in order to maximize the predetection signal-to-noise ratio. This lowpass output is used as an input to a differential phase detector for data demodulation, an input to a data transition tracking loop (DTTL) for bit timing, and as an input to a frequency discriminator for frequency tracking. DPSK demodulation is accomplished by passing the output of the differential phase detector through a simple threshold device. The resulting demodulated data is then used to gate the bit synchronizer on at bit transitions when there is timing information, and off when there is no transition between consecutive data symbols. The demodulated data is also fed back to resolve the ambiguity in the sign of the discriminator output error signal. The CPFSK demodulation algorithm shown in Figure 1-7 is similar to the DPSK algorithm. The major difference is that the demodulated data is obtained by performing post detection integration on the output of the frequency discriminator. Since the frequency-lock loop tracks the carrier frequency, the integrator accumulates a positive frequency offset signal if the upper signal frequency is transmitted, and a negative offset signal for the lower signal frequency. Data can therefore be detected with a sign detector, as before. A detailed description of the acquisition, demodulation, and tracking algorithms is presented in section 3, and a summary of the acquisition and tracking performance is presented in Table 1-5.

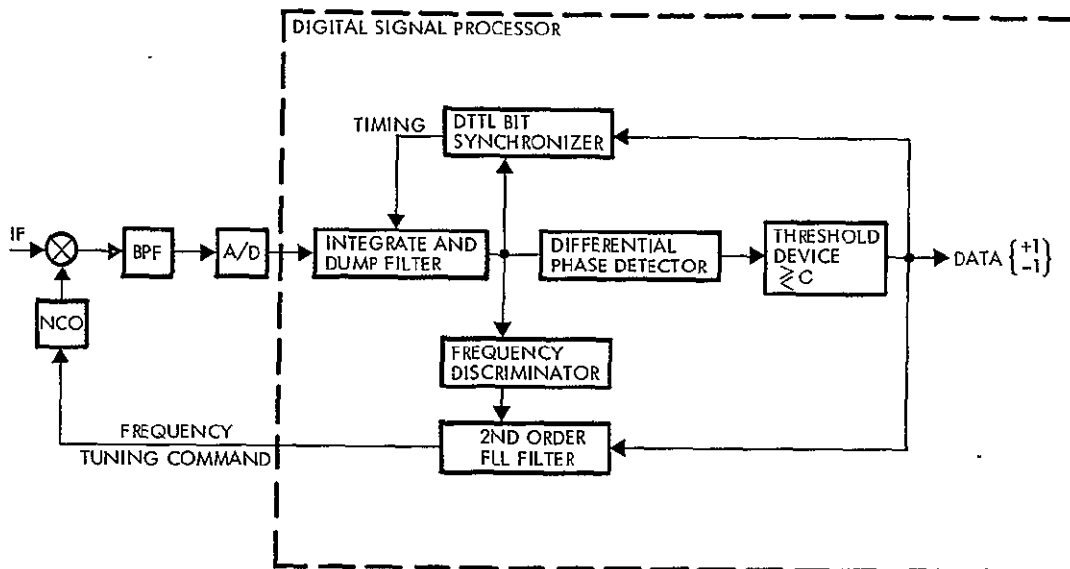


Figure 1-6. Demodulation of DPSK Data

Table 1-5. Acquisition and Tracking Performance

Operating Mode	Performance
<u>Coarse frequency acquisition</u>	
Probability of acquisition	0.995
Probability of false alarm	$<10^{-4}$
Acquisition time	45 sec
<u>Coarse frequency and bit sync tracking</u>	
Acquisition time (to 10% of data rate)	2 sec
RMS frequency jitter	$<10\%$ of data rate
Bit timing	1/16th of bit
<u>Demodulation and tracking</u>	
Bit error performance	$<0.5$ dB from theory
RMS frequency jitter	$<4.5$ Hz at low $C/N_0$
RMS frequency jitter	0.2 Hz at high $C/N_0$
RMS timing jitter	$<1\%$ of bit

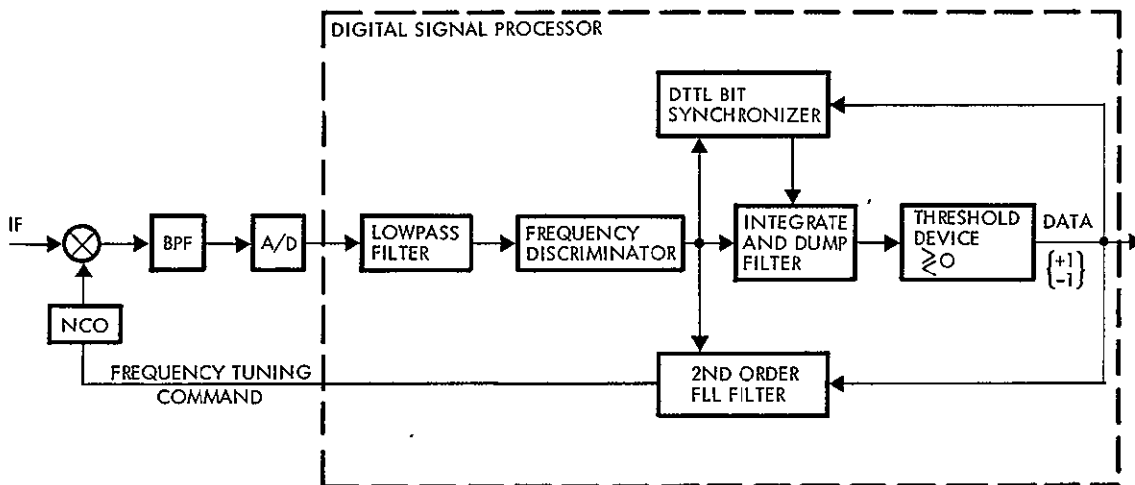


Figure 1-7. Demodulation of CPFSK Data

## 2. RECEIVER DESCRIPTION

This section presents detailed descriptions of the major subassemblies which comprise the hybrid receiver. These subassemblies are the analog processor, A/D converter and its associated sample and hold, and the digital processor.

### 2.1 ANALOG PROCESSOR

#### 2.1.1 RF/IF Subsystem

A simplified block diagram of the RF/IF and tuning portions of the hybrid receiver are shown in Figure 2-1. A substantial amount of the hardware used in this design is already proven and space-qualified. Some modifications to this hardware have been suggested to better match the receiver's operating frequency, tuning, and dynamic range requirements. Table 2-1 presents the key features of the RF/IF subsystem.

Table 2-1. RF/IF Subsystem Features

Operating frequencies	991, 992, 993, ..., 010, 1011 MHz
Noise figure	3.2 dB max
Gain	121 dB $\pm$ 1 ( $\pm$ 0.5 dB with temperature compensation)
IF bandwidths	
First IF	210 kHz centered at 31 MHz
Second IF	5 kHz centered at 480 kHz
Transmitter protection	20 MHz wide preselector centered at 1 GHz
Overload protection	Up to -10 dBm with no damage

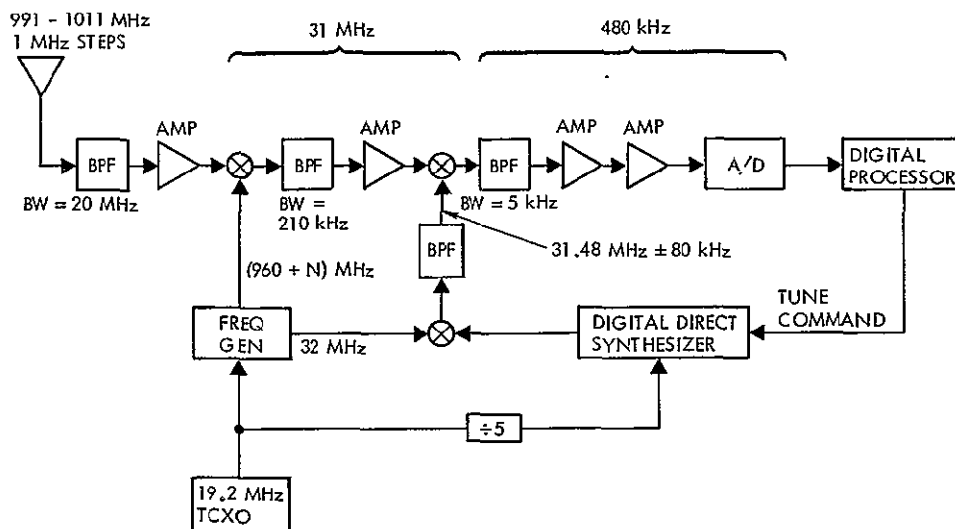


Figure 2-1. Hybrid Receiver Simplified Block Diagram

The 1 GHz input signal is filtered, amplified, and downconverted to the 31 MHz first IF frequency. The receiver's operating frequency can be set to any of the proposed mission frequencies 991 to 1011 MHz in 1 MHz steps by choosing the appropriate local oscillator frequency from the frequency generator. In the first IF, the input passband is filtered to a 210 kHz bandwidth and further amplified. A variable frequency second local oscillator then performs another downconversion to the final 480 kHz, second IF frequency where a 5 kHz filter establishes the final bandwidth. The signal is further amplified, then A/D converted and demodulated in the digital processor. Receiver fine tuning is also performed under the control of the digital processor.

The detailed front end block diagram is presented in Figure 2-2. Detailed noise figure calculations presented in Figure 2-3 show that the front end achieves a worst case noise figure of 3.2 dB. This excellent noise figure is primarily due to the pre-amplifier stages which provide sufficient low noise gain (20 dB) to make the noise contribution from the remainder of the front end negligible (0.03 dB).

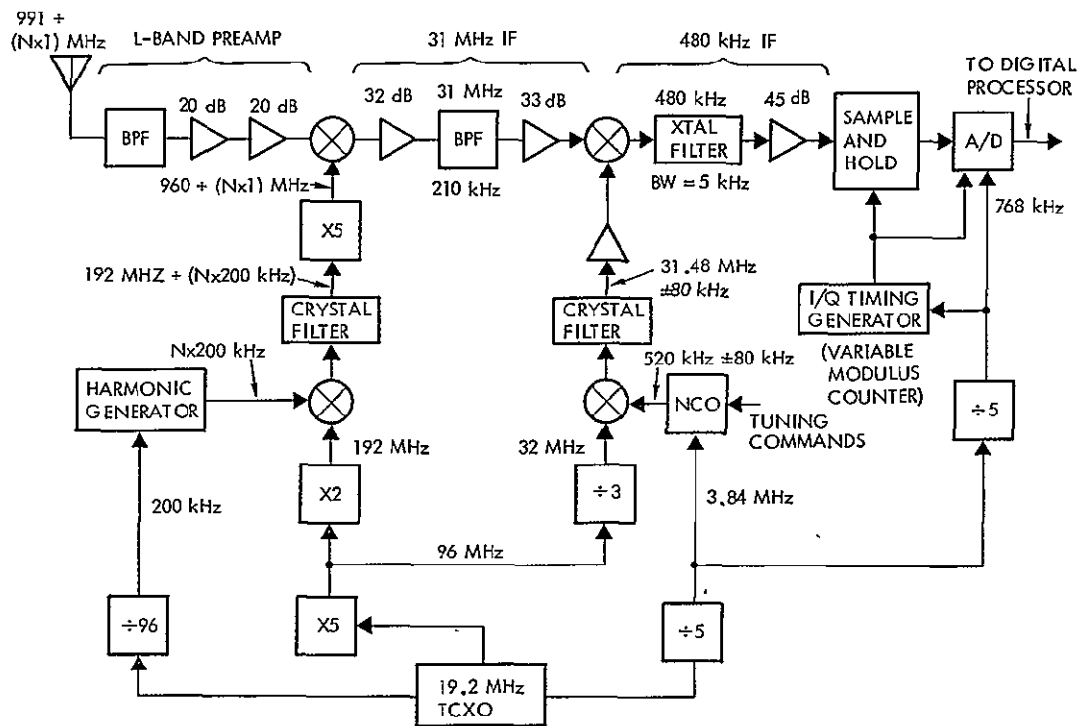


Figure 2-2. Hybrid Receiver Front End



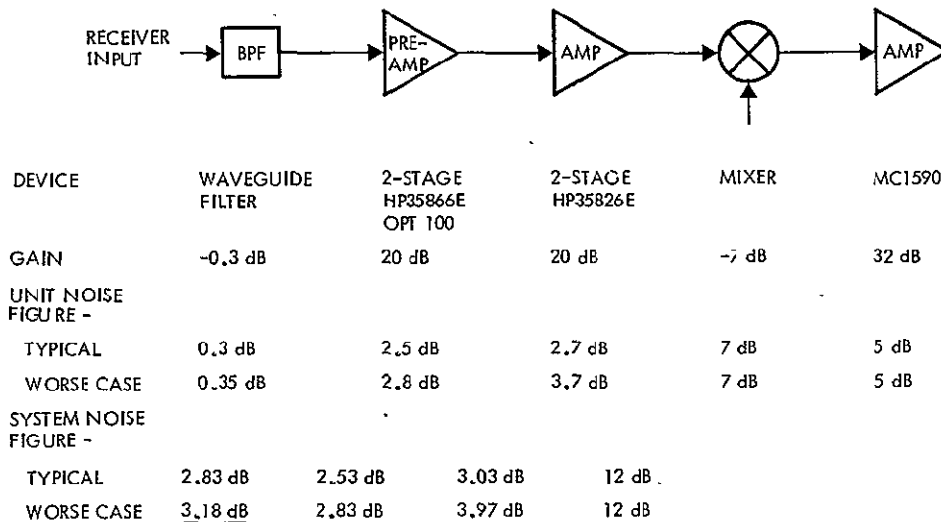


Figure 2-3. Noise Figure Calculation

The input bandpass filter has been placed in a somewhat unusual position between the antenna input and the first preamplifier stage. This placement carries with it a direct noise figure penalty of 0.3 dB maximum but protects the preamplifier against high level signals from the S and X-band transmitters commonly employed on deep space missions.

The first local oscillator is derived from the receiver reference oscillator through a series of frequency multipliers (X5, X2, X5). The reference oscillator is a space qualified 19.2 MHz TCX0. The multiplier circuits are derivatives of those used in the FLTSATCOM frequency generator. The frequency offsets which permit 1 MHz receive frequency spacings at 1 GHz are created by mixing harmonics of 200 kHz with the 192.0 MHz (= 19.2 (X2) (X5)) signal prior to the final X5 multiplier stage. A crystal filter then extracts the desired mixer output frequency (192 MHz + (N x 200 kHz)). The 200 kHz signal is produced by digitally dividing the 19.2 MHz receiver reference by 96. Additional digital logic circuits then produce the required harmonic spectrum.

The first real filtering takes place in the first IF. The bandwidth of the IF filter must be wide enough to pass the modulated signal plus any doppler uncertainty plus any frequency uncertainty due to oscillator drift. Therefore, it must be at least 160 kHz wide. This filter is the major source of amplitude ripple with changes in input frequency. The noise estimation process which supports the signal acquisition algorithm requires that this ripple be limited to  $\pm 0.1$  dB. Hence, an amplitude equalized version of the 210 kHz IF filter currently used on the Space Shuttle program was selected as the filter in the first IF. The 31 MHz IF amplifiers are direct adaptations of Space Shuttle/military L-band receiver IF amplifiers.

Conversion to the second IF is achieved by mixing the 31 MHz IF with a variable second local oscillator signal which tunes from 31.40 to 31.56 MHz in steps of 0.2288 Hz. This local oscillator is created by mixing a fixed 32 MHz signal with the variable output of a numerically controlled oscillator (NCO) and extracting the difference frequency with a crystal filter. The 32 MHz signal is obtained by taking 96 MHz (19.2 MHz x 5) from the first LO multiplier chain and digitally dividing by 3. Operation of the NCO is discussed in a subsequent section.

A 5 kHz crystal filter bandlimits the signal prior to the final amplification required to properly drive the A/D converter. The 5 kHz bandwidth was selected primarily to establish a noise bandwidth which sufficiently loads the A/D under noise-only conditions to permit accurate estimates of noise power density. This bandwidth also reduces by some 13 dB the dynamic range seen by the A/D in going from no signal to maximum operating signal level. The amplifiers used in the second IF are modifications of the same Space Shuttle/military L-band receiver amplifiers used in the first IF.

Table 2-2 shows the derivation of the major elements from programs such as FLTSATCOM and the Space Shuttle. The estimated power consumption of the RF/IF subsystem is 1.52 watts. Table 2-3 presents the basis for this estimate.

#### 2.1.2 Numerically Controlled Oscillator

The detailed tuning of the receiver under direct control of the digital processor is accomplished through the use of an NCO. This oscillator uses a synthesis technique which is known as digital phase accumulation. It involves four basic operations:

- Computation of the current signal phase
- Mapping of the phase into an amplitude value
- Digital to analog conversion
- Bandlimiting of the output.

Figure 2-4 presents a functional block diagram of the synthesis technique. A detailed block diagram of the receiver's NCO is presented in Figure 2-5.

A digital representation of phase (modulo  $2\pi$ ) is generated in the accumulator. The inputs to this accumulator are the current phase and the NCO command word. The NCO command word indicates the phase change per clock period and hence defines the NCO frequency, according to the relationship

$$f = \frac{Kf_c}{2^L}$$

Table 2-2. Receiver RF Component Derivation

<u>Unit</u>	<u>Source</u>
Receiver input bandpass filter	Wavecom standard line filter
1 GHz preamplifier	Modification of an L-band receiver amplifier from a military spacecraft program. Substitution of HP35866E OPT 100 transistor for HP35821E transistor
1 GHz amplifier	Modification of same L-band receiver amplifier. Substitution of HP35826E for HP35822E transistor
X5 and X2 multipliers	Derived from FLTSATCOM frequency generator
31 MHz amplifier	Direct adaptation from the L-band receiver and Space Shuttle IF amplifier
31 MHz BPF	Amplitude equalized filter similar to one used on Shuttle
480 kHz amplifier	Modification of 31 MHz amplifier
480 kHz BPF	Conventional crystal filter
19.2 MHz TCXO	Off-the-shelf FEI part, FE13-T02F
31.48 MHz BPF	Modification of Shuttle 31 MHz filter
192 MHz $\pm$ $\Delta$ BPF	Monolithic crystal filter
1st mixer	From S-band Shuttle (Anzac)
Other mixers	Used on Shuttle (WJ) M9BC

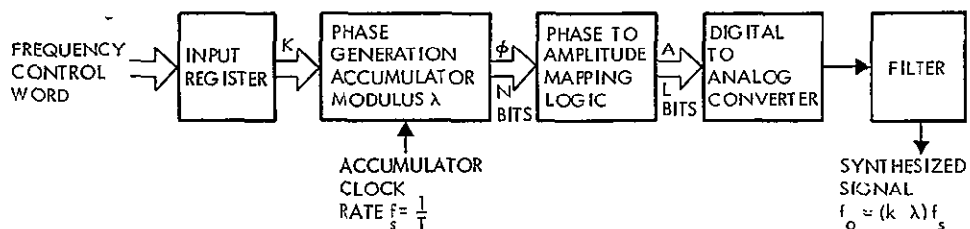


Figure 2-4. Digital Phase Accumulation

Table 2-3. Bias Current Estimation

$$V_{CC} = 12V$$

RF Amp	- 20 dB: Two-stage HP35866 OPT 100	16 mA
RF Amp	- 20 dB: Two-stage HP35826	16 mA
IF Amp	- 30 dB: Single-stage MC1590	15 mA
IF Amp	- 30 dB: Single-stage MC1590	15 mA
2nd IF Amp	- 44 dB: Single-stage MC1590 or MC1520	15 mA
X5 Multiplier:	Single-stage MS175JE	10 mA
X2 Multiplier:	Single-stage MS175JE	10 mA
X5 Multiplier:	Two-stage HP 21	10 mA
Buffer Amp:	Single-stage MC1590	10 mA
TCXO		<u>10</u> mA
	Total current	127 mA
	Total power	1.52 watts
	Total principal parts	10

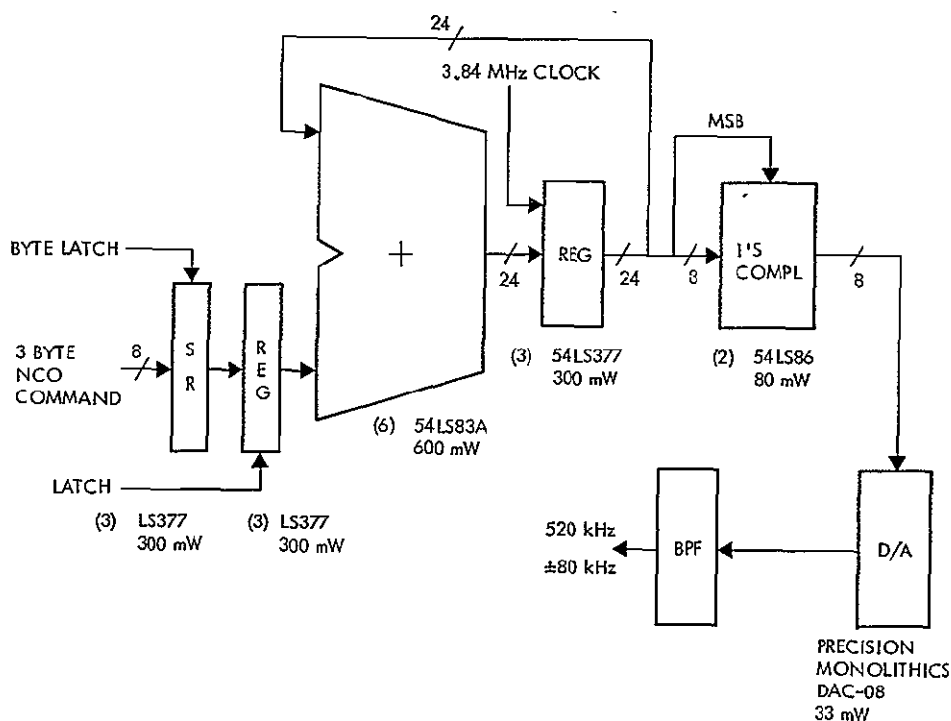


Figure 2-5. NCO Design

where

$f$  = NCO frequency

$K$  = NCO command word

$f_c$  = accumulator clock frequency = 3.84 MHz = 19.2 MHz/5

$L$  = accumulator length = 24 bits

The minimum frequency step size is given by  $1 \times 3.84 \times 10^6 / 2^{24} = 0.2288$  Hz.

The sawtooth of phase generated by this accumulation process is mapped into an 8-bit triangular representation of amplitude by using the accumulator's MSB to invert the lower order bits. This 8-bit amplitude word is converted to an analog signal by a monolithic D/A converter. A bandpass filter then extracts the triangle wave's fundamental frequency. Figure 2-6 shows the relationship between the various waveforms.

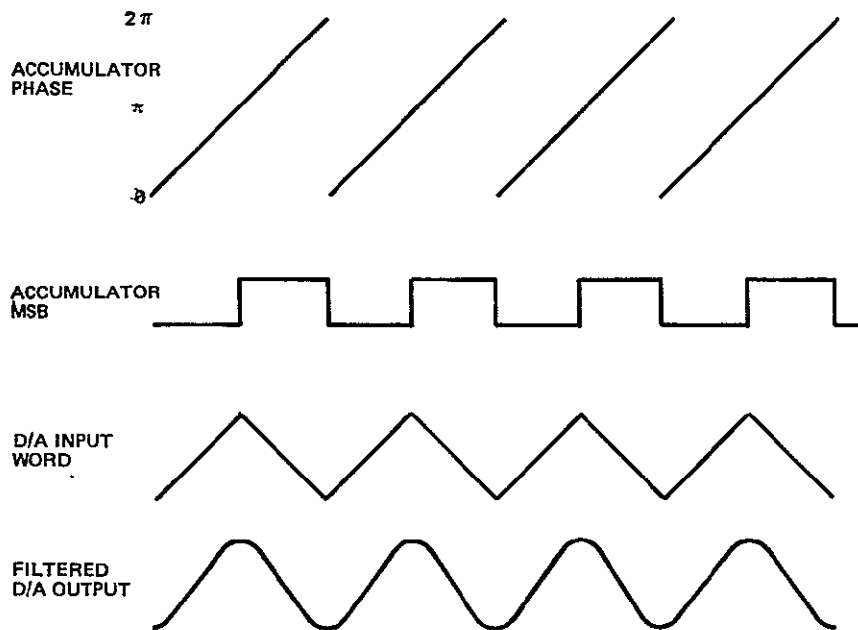


Figure 2-6. NCO Waveforms

In many applications, a ROM is used to map phase directly into a sinusoid. A power savings of 0.35 watt is obtained in this instance, however, by mapping to a triangle wave and then filtering.

The spectral purity of the NCO is degraded by such factors as phase truncation, aliasing of harmonics, and imperfections in the D/A such as nonlinearity and glitches. The triangle wave contains only odd harmonics whose amplitude falls off as  $1/N^2$  where  $N$  is the harmonic number. Since the NCO is a sampled data device, these harmonics alias about the sample clock frequency and can appear as discrete spurious signals in the band of desired output frequencies. The combination of sampling clock frequency

and tuning range is such that the major discrete spurious output is an aliased 7th harmonic some 33 dB below the desired NCO output. At this low spurious level, no difficulties are foreseen. If required, however, discrete spurious signals can be held to more than 50 dB below the desired NCO output by using a 256 x 8 ROM as the phase-to-amplitude mapping element. An additional 450 mW of power would be required for this approach.

With regard to short term stability, the phase noise density other than line spectra will be sum of the effects of logic jitter and the clock signal's noise spectral density modified by  $20 \log (f_{out}/f_{clock})$  dB. Breadboard tests performed on a similar synthesizer obtained the phase noise density curve presented in Figure 2-7.

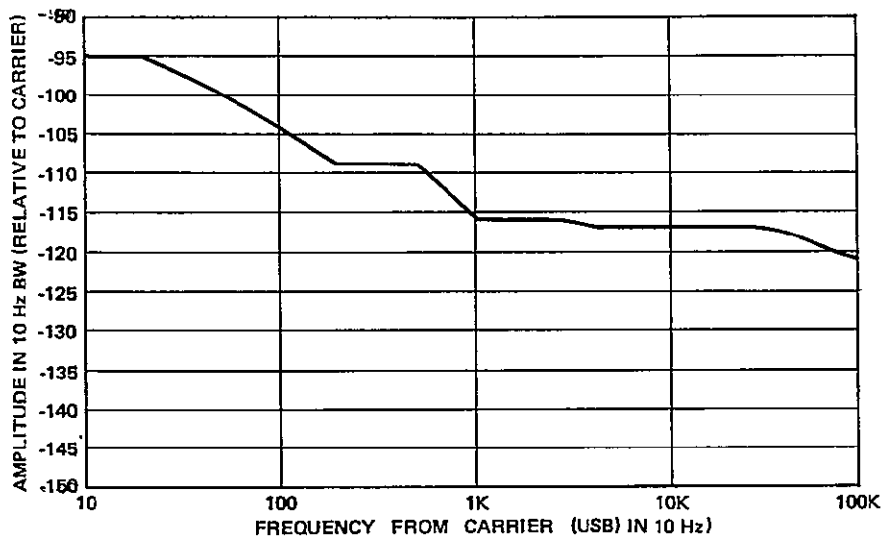


Figure 2-7. Phase Noise Test. Integrated Phase Noise: -67 dB (0.03° RMS Phase Jitter)

## 2.2 A/D AND SAMPLE AND HOLD

The A/D converter and its associated sample and hold amplifier form the interface between the RF front end and the digital processor. In addition to its normal function of quantizing the analog signal, the A/D is used as a quadrature mixer converting the 480 kHz IF passband into inphase and quadrature (I/Q) baseband components. This is accomplished by means of a sampling technique which is explained in detail in Section 2.2.1. Figures 2-8 and 2-9 are simplified block diagrams of the selected interface configuration and a functionally equivalent, conventional implementation.

A modification of the existing TRW ADC-4, 8-bit A/D converter was selected for use in this application. Its major features are:

- High reliability, monolithic construction (this A/D was designed expressly for spacecraft application for AFAL)

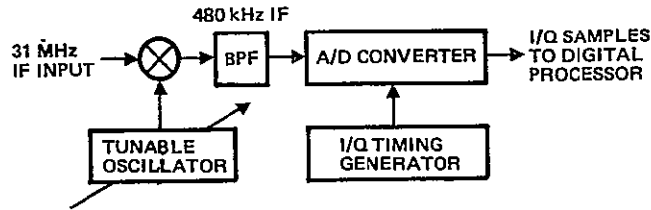


Figure 2-8. RF/A-to-D Interface

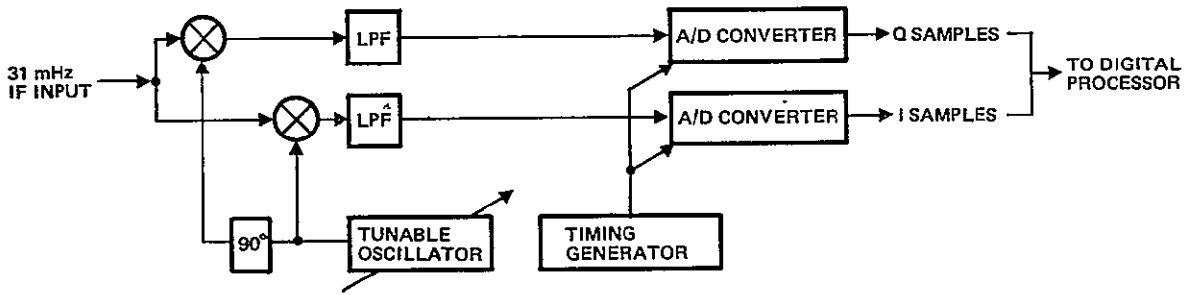


Figure 2-9. RF/A-to-D Interface Functional Equivalent

- Low power consumption (a reduction from 800 mW to 200 mW can be obtained by raising sheet resistivity during fabrication)
- Radiation hardness ( $>10^6$  rad(Si)) without materially altering performance.

The use of an 8-bit A/D simplifies the RF design as it eliminates the need for AGC. By proper selection of the IF bandwidth and gain (which defines the A/D loading), quantization noise can be made negligible (i.e.,  $>20$  dB below thermal noise) over the specified range of input levels without resorting to AGC.

The major interconnections between the A/D, sample and hold amplifier, clock, and data buffers, etc., are shown in Figure 2-10. The ADC-4 quantizes voltages in the 0 to  $-1.32$  V range only. Thus, to obtain symmetric operation, the input signal must be superimposed upon an offset voltage of  $-0.66$  V. This is accomplished by the offset circuit shown in the diagram which derives the bias voltage from a precision reference within the ADC-4. A detailed schematic diagram of the A/D interface is shown in Figure 2-11.

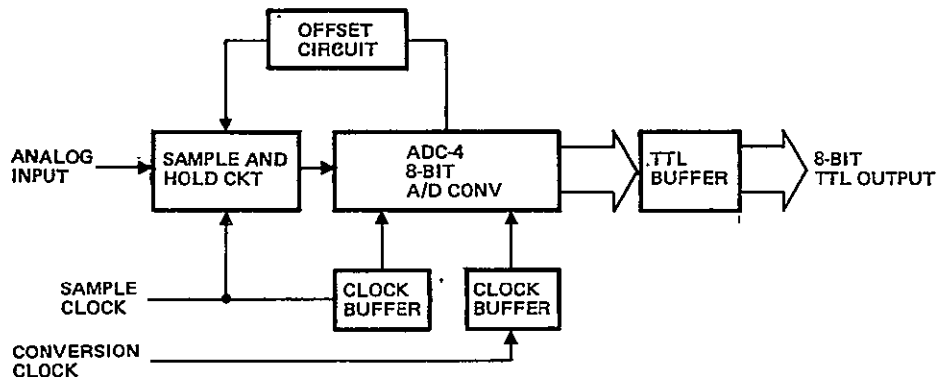


Figure 2-10. Interface Block Diagram

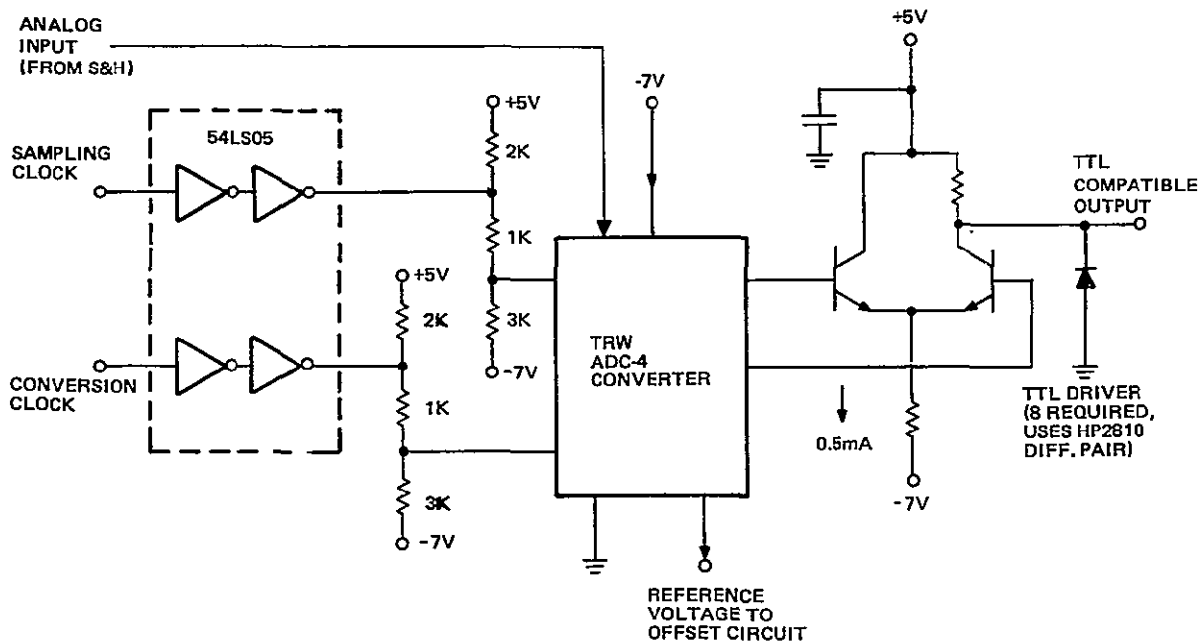


Figure 2-11. A/D and Support Circuitry

### 2.2.1 I/Q Downconversion by IF Sampling

I/Q sampling of an IF signal can be achieved by a single A/D converter if major conditions are met, namely:

- The IF process must be truly narrowband (i.e.,  $BW \ll f_{if}$ )
- The time interval between successive samples (i.e., I and Q) must correspond exactly to an odd number of quarter cycles at the frequency (e.g.,  $f_{if}$ ) which is to be translated to zero frequency (i.e., baseband)
- The I/Q sampling rate (as defined by the interval between successive I samples) is an integer submultiple of  $f_{if}$  and is consistent with the bandwidth of the process being converted (i.e., the Nyquist criterion is satisfied)

The mathematical basis for this form of sampling is as follows. Let  $Z(t)$  be the sampled waveform which can be expressed as

$$Z(t) = x(t) s(t)$$

where  $x(t)$  = the input bandpass waveform and  $s(t)$  = the sampling waveform. The sampling waveform consists of groups of two unit impulses in which the second impulse is delayed from the first by an odd number of quarter cycles at the frequency to be translated to zero frequency. The groups of impulses are repeated at time intervals  $T_s$  ( $= 1/f_s$ ). Thus  $s(t)$  may be written as



$$s(t) = \sum_{m=-\infty}^{\infty} \left[ \delta(t - m T_s) + \delta\left(t - m T_s - \frac{k}{4f_{if}}\right) \right]$$

where

$f_{if}$  = center frequency of bandpass waveform

$T_s = 1/f_s$  = reciprocal of the I/Q sample rate

$k$  = an odd integer

Since  $s(t)$  is periodic, it can be written as a Fourier series

$$s(t) = \sum_{n=-\infty}^{\infty} s_n e^{j2\pi n f_s t}$$

Solving for  $s_n$  we get

$$s_n = \frac{1}{T_s} \int_{-T_s/2}^{T_s/2} s(t) e^{-j2\pi n f_s t} dt$$

$$s_n = \frac{1}{T_s} + \frac{1}{T_s} e^{-j2\pi n k f_s / 4f_{if}}$$

Therefore

$$s(t) = \sum_{n=-\infty}^{\infty} \left[ f_s e^{j2\pi n f_s t} + f_s e^{-j2\pi n k f_s / 4f_{if}} e^{j2\pi n f_s t} \right]$$

The Fourier transform of  $Z(t)$  is then given by

$$Z(\omega) = f_s \sum_{n=-\infty}^{\infty} \left[ X(\omega - 2\pi n f_s) + e^{-j\pi n k f_s / 2f_{if}} X(\omega - 2\pi n f_s) \right]$$

where

$X(\omega)$  = Fourier transform of  $X(t)$

For a properly chosen value of  $f_s (= f_{if}/n$  where  $n$  is any positive integer), a portion of  $X(\omega)$  is translated to baseband. In addition, under this condition (i.e.,  $f_{if} = f_s/n$ )

$$e^{-j\pi n k f_s / 2 f_{if}} = e^{-k\pi/2}$$

Remembering that  $k$  was required to be an odd integer, we see that the portion of  $X(\omega)$  which was translated to baseband consists of two parts, one being a  $\pm 90^\circ$  shifted version of the other. Thus, a quadrature downconversion has been achieved by taking sample pairs at an appropriate spacing and pair rate.

In order to simplify generation of the timing signals necessary to achieve the sampling relationships defined above, the receiver's second IF frequency and the I/Q pair sample rate (i.e.,  $f_s$ ) are expressed as integer submultiples of the receiver reference source frequency (19.2 MHz). That is

$$f_{if} = 480 \text{ kHz} = \frac{f_{ref}}{40}$$

$$f_s = 32 \text{ kHz} = \frac{f_{ref}}{600} = \frac{f_{if}}{15}$$

Hence, exactly 15 cycles at the IF center frequency occur between successive I samples (and similarly between successive Q samples). A 32 kHz sampling rate is maintained at the A/D converter although the digital processor will operate at an 8 kHz rate by only using every fourth I/Q pair. This effectively allows the digital processor to jog its sample timing by 1/4 of a sample period for fine resolution bit timing.

In addition to a pulse to tell it when to sample the input process, the ADC-4 also requires a conversion clock which consists of at least 9 clock pulses between sample pulses. (Clock pulses in excess of 9 are ignored.)

The timing generation scheme shown in Figure 2-12 satisfies all requirements imposed by the sampling technique and the needs of the ADC-4. The conversion clock (768 kHz) is obtained by dividing the receiver reference frequency by 25 ( $= f_{ref}/25$ ) and is fed directly to the ADC-4. The conversion clock also feeds a variable modulus divider which generates sampling pulses in the required time relationship by alternately dividing by 10 and then by 14.

Figure 2-13 demonstrates that all the necessary timing relationships are achieved by the use of the 768 kHz clock and variable modulus divider. The Q sample is taken precisely 6-1/4 cycles after the I sample and the succeeding I sample is taken 8-3/4 after the last Q. Ten conversion clock counts occur between I and Q sample while 14

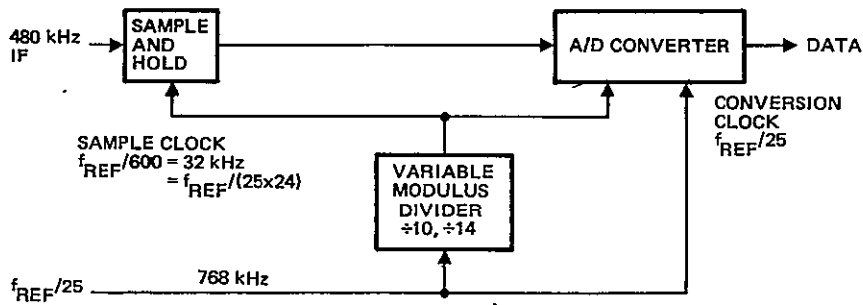


Figure 2-12. I/Q Sampling Generation

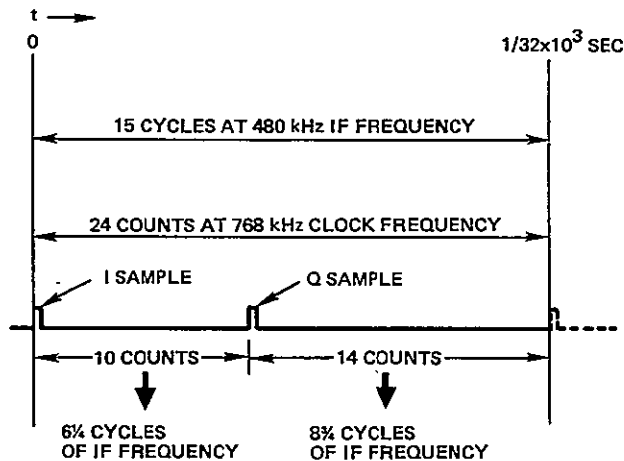


Figure 2-13. Hybrid Receiver I/Q Sampling Scheme

occur between Q and I samples. This meets the ADC's minimum of nine requirements and establishes an I/Q sample rate of 32 kHz as desired. Figure 2-14 presents the details of the variable modulus divider.

### 2.2.2 A/D Loading and Dynamic Range

The process of quantizing an analog signal produces distortion or quantization noise which is readily treated as additive noise. If the quantization noise is allowed to be of the same order as the thermal noise generated in the RF front end circuits (assuming external noise is negligible), the effective carrier-to-noise ratio ( $C/N_0$ ) is reduced. Thus, in order to achieve maximum receiver sensitivity, the parameters associated with the RF front end/A/D interface must be selected so as to place quantization noise well below the other noise sources.

The major factors which influence system  $C/N_0$  are the front end gain, noise figure, and pre-A/D bandwidth, and the A/D's quantum step size, number of bits, and input impedance.

It was desired to operate the A/D converter such that the noise introduced by quantization would be at least 20 dB below the minimum thermal noise. In addition, it

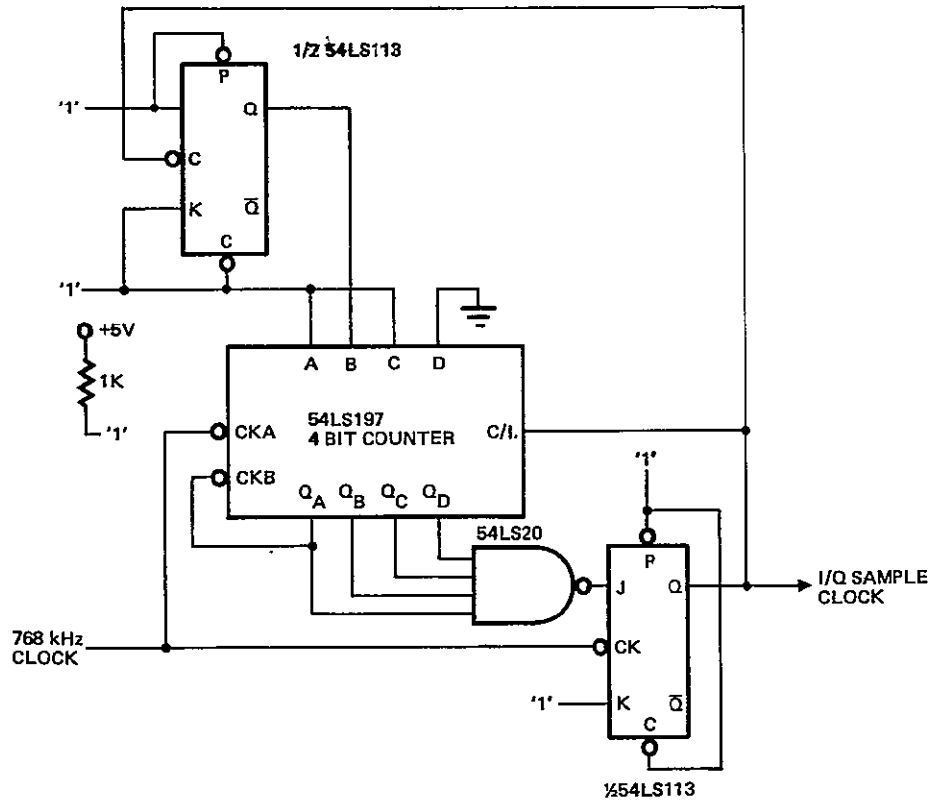


Figure 2-14. Variable Modulus Divider

was necessary that the minimum rms thermal noise power at the input to the A/D represent a sufficiently large number of bits to permit accurate derivation of the bias value required for the sequential detection process.

The relationship for determining quantization noise power density is given by

$$N_Q = \frac{\delta \left[ (2^{N-1} - 1) Q \right]^2}{R \text{ NPR}_R(\delta) \frac{f_s}{2} G} \quad (2.1)$$

where

$N_Q$  = quantization noise power density (W/Hz)

$\delta$  = loading factor =  $P_{\text{rms}}/P_{\text{peak}}$  = average signal power/A/D peak-clipping power level

$N$  = number of bits in A/D output word

$Q$  = quantization step size (V)

$R$  = A/D input resistance (ohms)

$\text{NPR}_R(\delta)$  = noise power ratio (NPR) as a function of  $\delta$  in bandwidth  $f_s/2$

$f_s$  = A/D sample rate (Hz)

G = RF front end gain

Noise power ratio represents the signal-to-quantization noise ratio which is a function of the probability distribution function of the input signal and  $\delta$ , the loading factor. Figure 2-15 presents curves of  $NPR(\delta)$  plotted against  $\delta$ . At low values of  $\delta$ , NPR decreases because the A/D is underloaded. That is, the full dynamic range of the A/D is not being used while the quantization noise level remains constant. At high values of  $\delta$ , NPR also decreases because the signal is clipped, resulting in significant signal distortion. As expected, NPR increases as the number of quantum levels is increased because the quantum step size (and hence, quantization noise) decreases. NPR curves are shown for two types of inputs, Gaussian noise and a CW input. The differences at higher values are due to the differences in pdf which determine at what loading clipping distortion becomes appreciable.

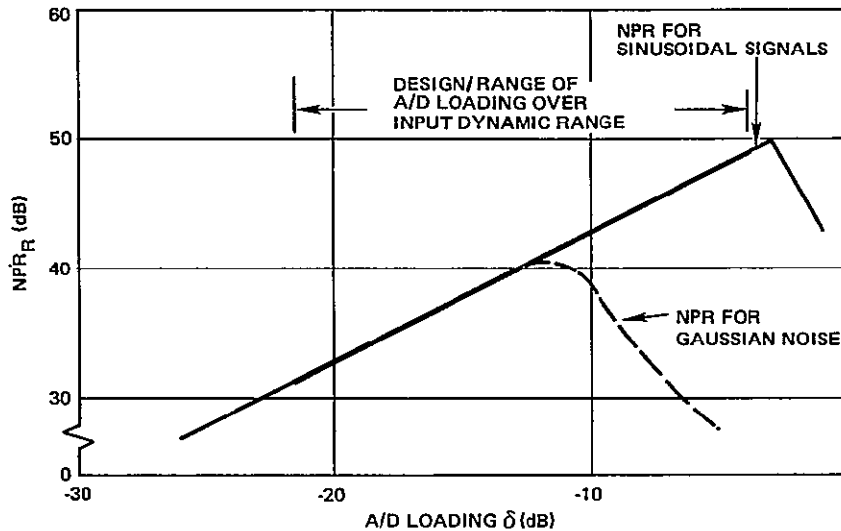


Figure 2-15. A/D Loading and NPR Performance

Through a tradeoff process, an IF bandwidth of 5 kHz and a front end gain of 121 dB were selected. The choice of 5 kHz is significant as it materially reduces the dynamic range which the A/D converter will see as the signal level is varied over its specified range. Table 2-4 presents the calculations which show that the dynamic range is compressed from 30 to 17.8 dB.

The nature of the process which the A/D converter sees varies from essentially Gaussian at low input levels to essentially sinusoidal at the high input levels. The sinusoidal character at high SNR allows heavier A/D loading (following the CW NPR curve) and hence higher front end gain may be employed.

Table 2-4. Dynamic Range Calculations

Noise power in 5 kHz IF bandwidth	
Minimum Power	Maximum Power
-174.0 dBm/Hz	-166.0 dBm/Hz
3.2 dB NF	
<u>37.0 dB-Hz (5 kHz)</u>	<u>37.0 dB-Hz (5 kHz)</u>
-133.8 dBm	-129.0 dBm
Minimum noise plus minimum signal	
	$4.17 \times 10^{-17}$ W (-133.8 dBm)
	<u><math>.25 \times 10^{-17}</math> W (-146.0 dBm)</u>
	$4.42 \times 10^{-17}$ W = -133.55 dBm
Maximum noise plus maximum signal	
	$1.26 \times 10^{-16}$ W (-129.0 dBm)
	<u><math>2.51 \times 10^{-15}</math> W (-116.0 dBm)</u>
	$2.64 \times 10^{-15}$ W = -115.78 dBm
Dynamic range	
	= -115.78 - (-133.55) = 17.77 dB

The limited dynamic range which the A/D converter will see and the transition from an essentially Gaussian to an essentially sinusoidal process allows a maximum signal loading point to be chosen which will allow a linear variation of NPR with  $\delta$ . Thus,  $N_Q$  variation with  $\delta$  can be eliminated and  $C/N_0$  improves linearly with C. Under these conditions, (2.1) may be rewritten as

$$N_Q = \frac{[(2^{N-1} - 1) Q]^2}{R \text{ NPR}_R G \frac{f}{2}} \quad (2.2)$$

The parameters associated with the ADC-4 are

$$N = 8 \text{ bits}$$

$$Q = 5.16 \times 10^{-3} \text{ (V)}$$

$$\text{NPR}_R = 1 \times 10^5 \text{ (including all degradation sources)}$$

$$R = 50 \text{ (ohms) (achieved by externally padding the input)}$$

At a front end gain of 121 dB, the loading at maximum input signal level is -4 dB (which utilizes the CW portion of the NPR curves) and at minimum signal level is -21.6 dB.

This gain, combined with an effective sampling rate of 8 kHz, produces a constant noise power density of -200.7 dBm/Hz which is 30 dB below the thermal noise. Additionally, the combination of front end gain and bandwidth allows the rms noise power in 1 kHz to be represented by eight quantum steps, a value which permits the required accuracy in estimation of the sequential detector's bias level.

### 2.2.3 Sample and Hold Circuit

Although the ADC-4 is capable of performing conversions in less than 80  $\mu$ sec, this time period represents greater than  $12^0$  at the 480 kHz IF frequency. Therefore, the use of a sample and hold circuit is required.

In the realm of ready-built devices, alternatives ranged from commercially produced modules to TRW's own hybrid IC's. All, however, had problems with high power consumption or unknown radiation, and/or reliability characteristics. Therefore, it was decided to design a S&H circuit with performance adequate for this application from low power components of established reliability and radiation performance.

Figure 2-16 presents a schematic of the circuit which incorporates the voltage offset feature necessary for operation with the ADC-4. The major components of this circuit, i.e., the gating FET and operational amplifiers, are types of known reliability and radiation characteristics.

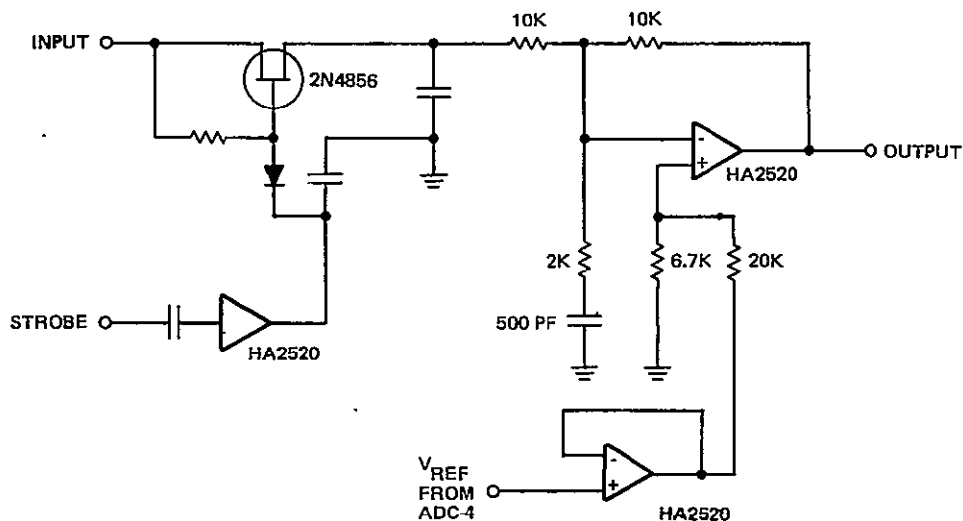


Figure 2-16. Sample and Hold Circuit

## 2.3 DIGITAL PROCESSOR DESCRIPTION

### 2.3.1 Digital Signal Processor Characteristics

A microprocessor or "microprogrammed processor" is a very small computer-like module which controls all basic computer functions by a sequence of instructions stored in a read only memory. These processors have great inherent flexibility since the ROM stored instructions or "firmware" controls all data bus interconnects, data storage, arithmetic operations, and input/output transfers. The basic design philosophy of the hybrid receiver digital signal processor (DSP) has been to use microprogrammed control for flexibility, and simple orderly control logic and to use simultaneous parallel instruction execution for maximum throughput and resource utilization.

As illustrated in Figure 2-17, the DSP microprocessor implementation has two major parts, the central processor and microprogrammed control.

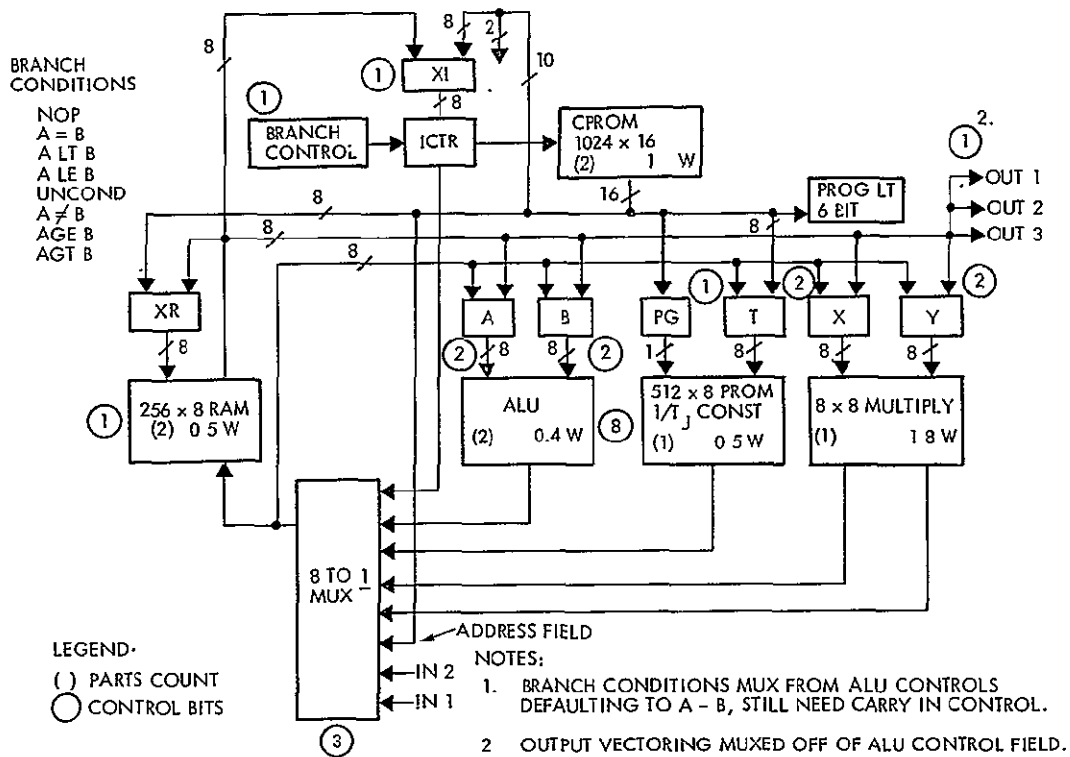


Figure 2-17. Digital Signal Processor (DSP) Block Diagram

The basic functions of the central processor are data storage (RAM), arithmetic and logic operations (ALU), 2's complement multiplication (MPY), and constant or reciprocal storage (PROM). Operands for each central processor element may be selected from the RAM or a common output bus. The ALU and multiplier are configured to allow multiple precision arithmetic on the basic 8-bit data word.



The basic functions of the microprogrammed controller are program storage (CPROM), program addressing and branch control (ICTR), and memory addressing (XR,XT). Memory addresses are derived from the CPROM address or indirectly from the data RAM. The CPROM is organized as a 1024 x 16 memory and is accessed twice per instruction for a basic control word length of 32 bits and 512 instructions.

Input/output control assumes a single 8-bit parallel transfer across a request/acknowledge interface. Each side (input/output) has three ports and transfers one 8-bit byte per request.

The basic DSP machine cycle is 500 nsec for a full 32-bit instruction (two CPROM accesses required). The technology used is standard off-the-shelf bipolar LSI such as RAM's, ROM's, and ALU's and is implemented with the low power Schottky TTL logic family throughout. The parts count is 54 integrated circuits with a power dissipation of 6.5 watts. A summary of DSP characteristics is shown in Table 2-5.

#### Central Processor

The central processor incorporates all arithmetic and logic functions, data storage, table lookup, and a 2's complement multiplier. All these elements are controlled and operated in parallel. This feature provides maximum hardware resource utilization and a high instruction execution rate (up to  $2 \times 10^6$  instructions/sec). Section 2.3.3 demonstrates that this concept results in a maximum machine loading of 50% of full capacity.

Selection of the DSP microprocessor concept is based on a very low power dissipation requirement and a proportionately high data throughput requirement. Low power dissipation implies a small data word (8 bits). The basic signal processing algorithms require 24-bit arithmetic at the 8 kHz sampling rate. The architecture selected to resolve these conflicting requirements consists of using a small data word with parallel multiprecision arithmetic to accommodate the throughput requirements.

The DSP central processor is organized around a single RAM and an output bus. Operands for all arithmetic operations are selected from these two sources. Two registers in front of the ALU and multiplier save operands from cycle to cycle. Hence, a single microinstruction can set one memory address and load two operands from separate sources. The objective of this parallelism is to increase data throughput and maximize the utilization of hardware resources.

The arithmetic logic unit (ALU) provides add and subtract operations and various logic functions including a shift matrix. Carry storage and control is provided for multiple precision arithmetic. For data accumulation, ALU results are transferred back to input storage registers via the output bus. Status or flag data (such as overflow, less than, or carryout) is transferred directly to the branch control in the microprogrammed controller.

Table 2-5. DSP Microprocessor Summary

Digital signal processor
Microprogrammed parallel architecture
Basic instruction cycle time — 500 nsec
Word length — 8 bits
Multiple precision arithmetic
8 x 8 hardware multiply — 1 instruction cycle
ALU implements shift matrix
Request/acknowledge I/O interface — TTL compatible
Vectored interrupt structure
Capacity
RAM capacity 256 x 8
PROM capacity 512 x 8
CROM capacity 1024 x 16 — 512 instructions
Basic logic technology — Low power Schottky TTL
Standard off-the-shelf bipolar LSI
Physical
54 integrated circuits
6.5 watts power dissipation

The multiplier (MPY) is an 8 x 8 2's complement multiplier with input and output storage. The multiplier result is a 16-bit product but only the upper or lower half may be accessed in a single instruction. Output data may be transferred back to the multiplier, to the ALU, or saved in the RAM via the output bus.

The read only memory (PROM) shown is a 512 word by 8 bits per word nonvolatile memory. All algorithm constants and coefficients including a table of reciprocals are stored in the ROM. The ROM can interface with any of the other computational elements via the output bus.

## Microprogrammed Control

The microprogrammed control (MPC) provides all the direct address, control, and clock signals to the central processor. This includes any multiplexer selects and I/O load strobes. The control addresses data or microprograms are stored in the control read only memory (C-ROM) which in most implementations would be a programmable ROM (PROM). Each microprogram consists of microinstructions which have fields dedicated or sectored for each central processor function in addition to the direct address fields. Each field thereby contains the microcode which would be decoded and distributed for data transfers and other operations.

Microprogramming techniques are used because of the efficiencies and economics of handling microinstructions in firmware as opposed to the conventional random logic approach. The control section of a nonmicroprogrammed processor tends to be complex, containing numerous gates, multiplexers, storage elements, and decoding networks for each instruction that is executed. Using microinstructions stored in a semiconductor ROM, the control can be greatly simplified. Randomness remains, but only stored as random data in the memory — not as an unstructured design of logic networks. In essence, a more structured organization of hardware logic results.

The control memory outputs, which are groups of synchronous word-parallel data streams, are used to set flip-flops, select multiplexer inputs, load/increment, or select ALU functions or any other control function associated with hardware operation. When the control memory outputs perform a single unique control function, this is labeled horizontal microprogramming or minimally encoded. This approach is used in the microprocessor primarily for higher operational speed and multi-instruction executions. This horizontal approach requires a wide (bits per word) control word and availability of all functions with each word.

Alternatively, vertical programming uses microinstructions that are partially or fully encoded, such as how memory addresses are used in RAM's. The penalty is that some flexibility is lost and speed of rotation is reduced. The latter results from multiple steps being required for a single operation. However, encoding the microinstructions does tend to reduce the control memory storage capability requirements. Typically, the encoding is done within a single 8 to 16-bit word or byte.

The data flow for a microinstruction starts with either a direct address selected by the P-multiplexer, by presetting the ROM P-CTR (program counter), or by the P-CTR being incremented by 1. The instruction fields, or the bit allocations within the instruction, are transferred to the central processor or used as part of the microprogrammed control functions. Control signals and memory direct address are shifted word parallel to the instruction register (storage for the control signal decoding) and the memory address counters, respectively. The jump instruction (JMP), both conditional and unconditional, requires use of the address or pointer in the control ROM format.

All of the above resources are under the control of the P-CTR. All control signals and required timing signals are referenced to the P-CTR and the clock generator. All timing and operations are fully synchronous with the clock generator.

Typically, a logic system performs an operation either in response to a change in state of its inputs or as a function of time, such as an internal timer. For the microprogrammed control, there are two ways of initiating a response — polling or interrupts. Polling uses a sample that sequentially senses the state of each input line and, based on input logic states, either jumps to the appropriate ROM program directly or continues polling. The interrupt method generates a unique ROM address for each input line. This address may be either the beginning of a microprogram or the address of a jump microinstruction which in turn contains the starting address. The latter is a form of indirect addressing. In either case, the interrupting program is executed immediately.

Polling provides the slower microprocessor response since each input must be scanned individually and each must wait their turn to be recognized. This is somewhat less complex than the interrupts and sequentially handles simultaneous inputs. Interrupts, especially priority interrupts, require additional logic for address generation and the priority strategy. The technique does offer the fastest response time, which is almost negligible if the highest priority is requested. Hence, an interrupt structure was selected for the DSP.

#### Instruction Set

The microprocessor has four basic instructions: arithmetic, shift, branch, and transfer. These four operation codes essentially specify four different interpretations of the ALU control field. None of the other control fields are subject to multiple interpretations. The basic instruction set is two-address (source and destination) and register-transfer oriented. Table 2-6 defines mnemonics for various machine storage elements (refer to Figure 2-17) and Table 2-7 enumerates a basic set of operations which may be performed on the various storage elements.

#### Control ROM (CROM)

The control ROM program formats illustrated in Figure 2-18 require a 32-bit ROM word. Each control field has a direct relationship to central processor resources. The 8-bit ALU control field is multiplexed by a 2-bit opcode field (OP) giving four different instruction types (AR, SH, IO, and BR). Usage of the remaining 22 control bits is fixed for all instruction types. The ADDRESS field contains an 8-bit direct address which may be loaded to any memory address latch. The field labeled XC is the memory address latch destination control and directs ADDRESS field data to a specific memory address latch. The OBUS field selects one of eight possible outputs for direction to the output bus. The field labeled RW is the RAM write enable. The remaining

Table 2-6. Storage Element Mnemonics

A	Left side ALU input
B	Right side ALU input
X	Left side MPY input
Y	Right side MPY input
AD	CROM address field
RM	RAM output
TB	PROM output
AL	ALU output
MP.L	Lower half of product
MP.U	Upper half of product
XR	RAM address
XT1	PROM address
XT2	PROM page bit
CY	Carry flip-flop
A OP B	Result of ALU OP on A and B

Table 2-7. Basic Instruction Set

A < RM	XR < AD
A < OB	XR < OB
B < RM	XT1 < AD
B < OB	XT1 < OB
X < RM	XT2 < AD
X < OB	XT2 < OB
Y < RM	
Y < OB	
BR.OP.AD (Conditional Branch)	OB = Output bus

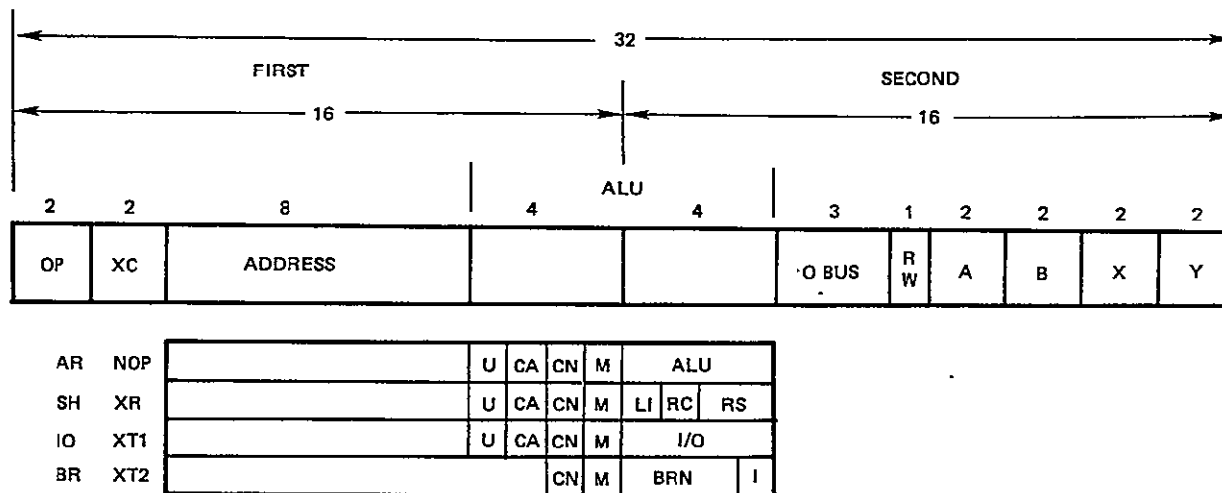


Figure 2-18. Control ROM Format

fields labeled A, B, S, and Y control the four input storage latches in front of the ALU and multiplier.

The ARITHMETIC (AR) microinstruction contains all controls needed to use the ALU in arithmetic and logic mode. The U field is the carry flip-flop update control. The CA and CN fields are carry-in select controls for multiple precision arithmetic. The M field is the ALU mode control (logic or arithmetic). The ALU field is the instruction code input to the ALU.

The SHIFT (SH) instruction controls the ALU in shift mode. The LI field is the left input for right shifts. The CA and CN fields select the carry in which is used as a right input for left shifts. The RC and RS fields control the shift mode (left, right, sign extend, etc.) of the internal ALU shift register.

The INPUT/OUTPUT (IO) instruction reserves 4 bits of ALU control for I/O vectoring. The BRANCH (BR) instruction expands the address field to 10 bits for full program addressing capability and reserves the other four ALU control bits for branch condition selects.

The instruction set of Tables 2-6 and 2-7 is translated to the specific control field value of Figure 2-18 by an assembler.

### Fetch/Execute Sequence

The complete DSP instruction cycle consists of a fetch cycle and an execute cycle. The fetch cycle reads the current microinstruction from the control ROM and the execute cycle performs the specified operation. The entire cycle repeats every 500 nsec. for a basic execution rate of  $2.0 \times 10^6$  instructions/sec.

The actual implementation of the control ROM breaks the 32-bit word into two 16-bit slices. This technique required two control ROM accesses per instruction. Figure 2-19 shows the DSP fetch/execute timeline for a typical instruction. ("P" in Figure 2-19 is time required for the ROM to respond to a new control address.) Note that the fetch of the second 16-bit slice is overlapped with the execute of the first 16-bit slice. The first 16-bit slice contains address control and the second contains central processor control.

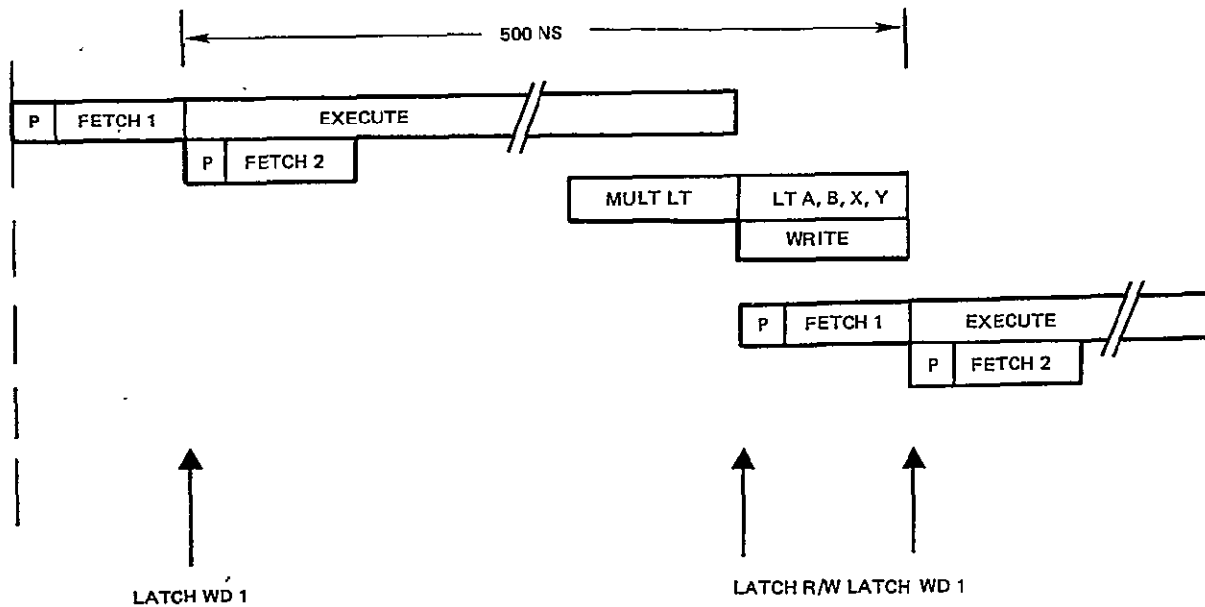


Figure 2-19. DSP Fetch Sequence

### 2.3.2 I/O Interfaces

The basic DSP I/O interface is a single byte oriented request/acknowledge or "handshaking" interface. The input side has two 8-bit parallel ports and the output side has three 8-bit parallel ports and associated control lines for each port. Table 2-8 lists input and output to/from each port.

Table 2-8. Input/Output Ports

<u>Input</u>	<u>Output</u>
1 A/D	Demod data
2 External	Phase accumulator (NCO)
3	External

The A/D port receives 8-bit samples (I, Q channels) at a maximum rate of 8000/sec. The EXTERNAL port receives inputs from peripheral devices such as the spacecraft remote data terminal (RTU), test equipment, etc.

Output of the DEMOD DATA port consists of single bits at a maximum rate of 1000/sec. Output at the NCO port is a 24-bit frequency increment ( $\Delta f$ ) and occurs at a maximum rate of 1000/sec. Output at the EXTERNAL port consists of data sent to peripheral devices such as test equipment, RTU, etc.

Figure 2-20 shows a block diagram of the interface and control waveforms for a typical transfer. REQUEST is implemented as a vectored interrupt in the processor and immediately drives program control to the appropriate interrupt service routine. The interrupt service routine acknowledges receipt of the request via the ACK control line. If the requesting port is input, the service routine waits on the I/O complete signal to guarantee that incoming data is at the port and stable. If the requesting port is output, the service routine sends the requested data followed by the I/O complete signal.

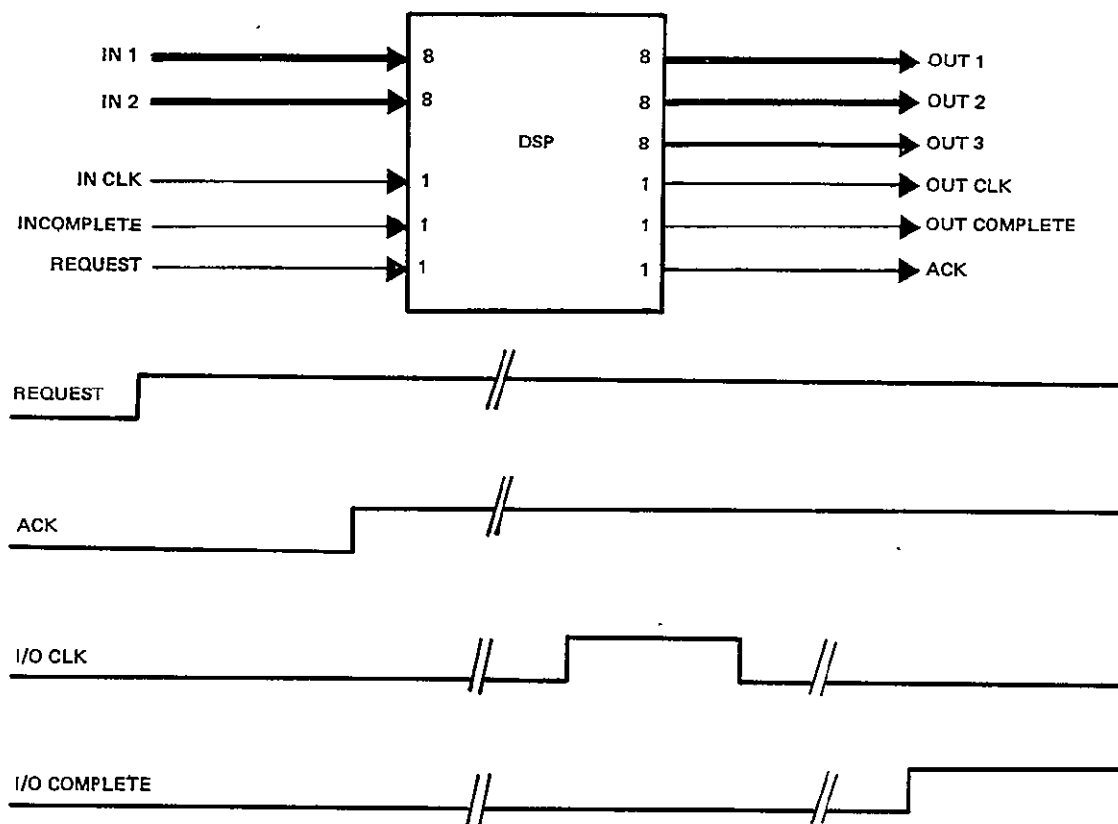


Figure 2-20. Hybrid Receiver Interface



### 2.3.3 Processing Capabilities

The signal processing algorithms uniformly require multi-precision arithmetic. For example, the second order loop filter shown in Figure 2-21 requires 24-bit accumulation and several 8 x 24 multiplies. The coarse acquisition algorithm of Figure 2-22 requires 24-bit addition and subtraction. Computation of  $I^2 + Q^2$  requires two 8 x 8 multiplies and a 16-bit addition.

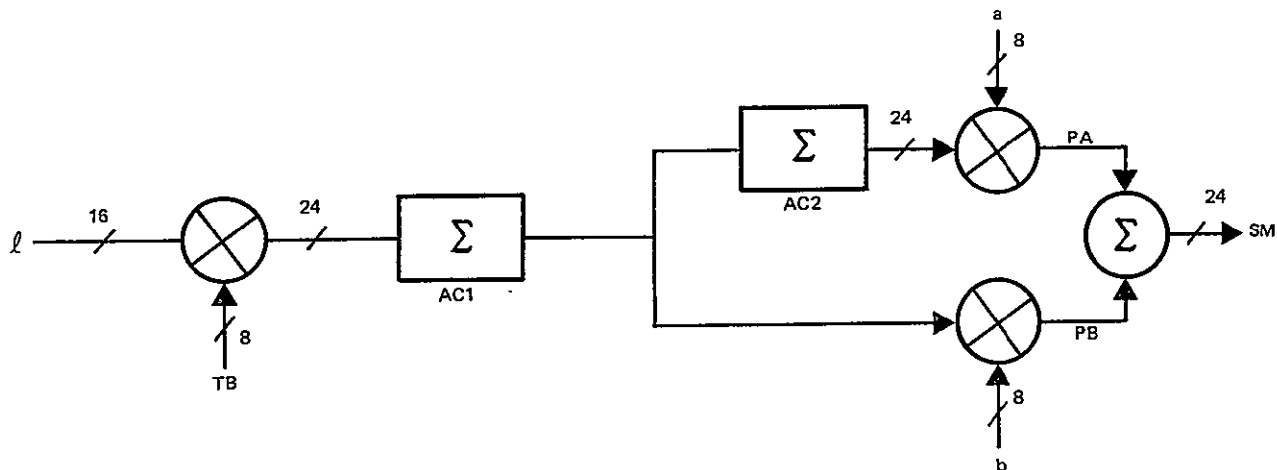


Figure 2-21. Basic Second Order Filter

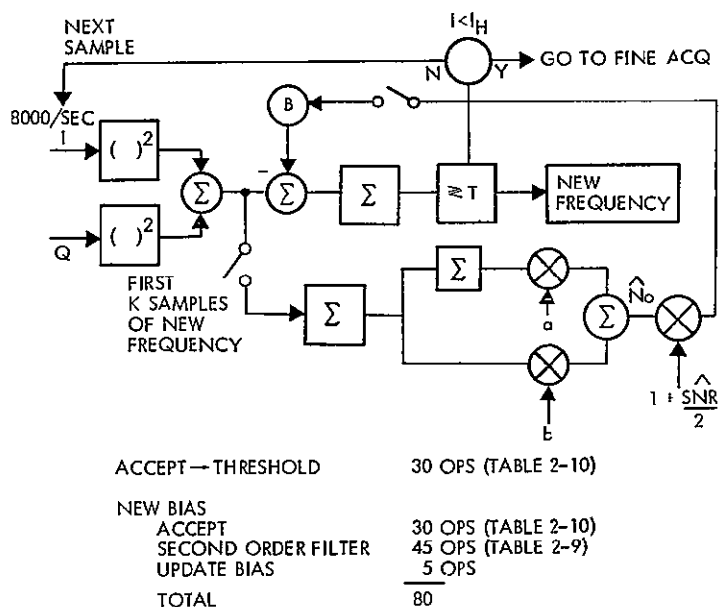


Figure 2-22. Coarse Acquisition Algorithm

To obtain an estimate of overall processor loading for signal processing, several of the high rate processes are programmed and sized in detail. Lower rate processes are sized using conservative estimates derived from the detailed sizings. For example, sizing for a 24-bit accumulate can be derived from the detailed sizing of the second order filter of Figure 2-21, since there are several 24-bit accumulates in the filter. Table 2-9 presents a complete program for implementing the second order loop filter. Table 2-10 presents a complete program for implementing the coarse acquisition algorithm.

Figures 2-23 through 2-27 show block diagrams of each phase of the signal processing algorithms. The precision of each operation is defined in the block diagram and the operation count for the algorithm is derived from counts defined in Tables 2-9 and 2-10.

Table 2-11 presents a summary of processor loading estimates for each algorithm. This summary shows that maximum overall processor load is 40% of full capacity. The estimates in Table 2-11 do not account for any realtime executive or mode control overhead. This overhead is estimated to be approximately 10% of processing capacity (25 instructions per input sample) which yields an overall load figure of 50% of full capacity.

Table 2-12 presents a summary of estimated program memory usage. This estimate assumes linear code (no subroutines) except for the case of the second order loop filter. There is only one filter in each of three processes (coarse acquisition, fine acquisition, and tracking) which are mutually exclusive in time. This fact implies that program memory for the second order loop filter may be shared between the three

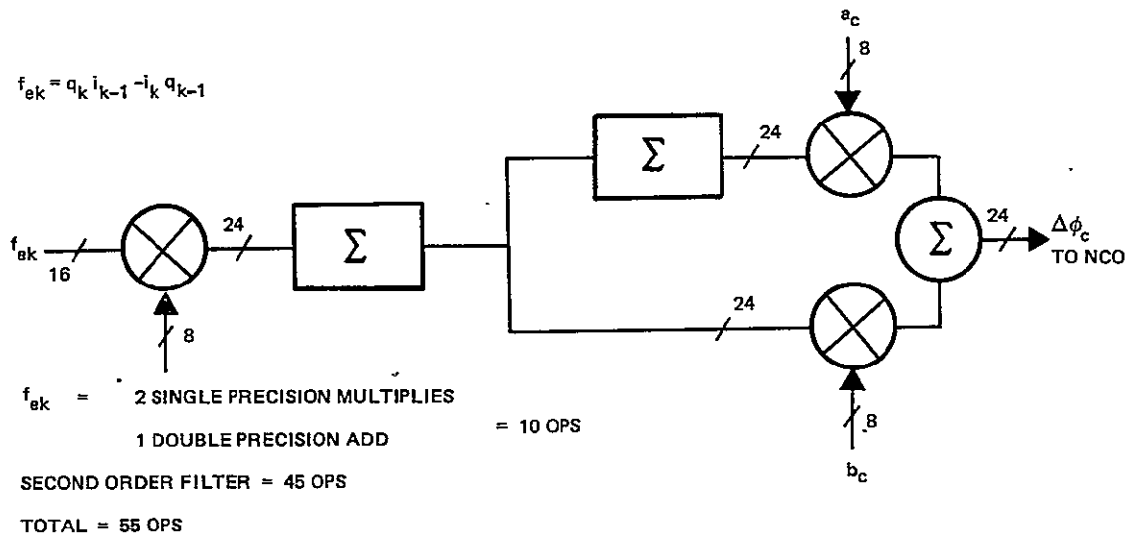


Figure 2-23. Frequency Lock Loop Filter

Table 2-9. Second Order Filter Program

<u>Instruction</u>	<u>Code</u>
1	XR < e.L , X < (e.L), Y < TB
2	XR < AC1.L, B < (AC1.L), A < MP.L
3	RM < A + B = AC1.L
4	XR < e.U , X < (e.U), A < MP.U
5	B < MP.L
6	XR < AC1.M, B < (AC1.M), A < A + B + C
7	RM < A + B
8	XR < AC1.U, A < (AC1.U), B < MP.U
9	XT < b , RM < A + B
10	XR < AC1.L, X < (AC1.L), A < (AC1.L), Y < b
11	XR < AC2.L, B < (AC2.L)
12	AC2.L < A + B
13	24 BIT ADD XR < AC1.M, A < (AC1.M)
14	9 OPS XR < AC2.M, B < (AC2.M)
15	, AC2.M < A + B + C
16	XR < AC1.U, A < (AC1.U)
17	XR < AC2.U, B < (AC2.U)
18	, AC2.U < A + B + C
19	XR < PB.L., PB.L < MP.L
20	XR < AC1.M, X < (AC1.M), A < MP,U
21	B < MP.L
22	XR < PB.M , PB.M < A + B
23	XR < AC1.U, X < (AC1.U), A < MP,U
24	XT < a , B < MP.L
25	XR < PB.U , PB.U < A + B + C

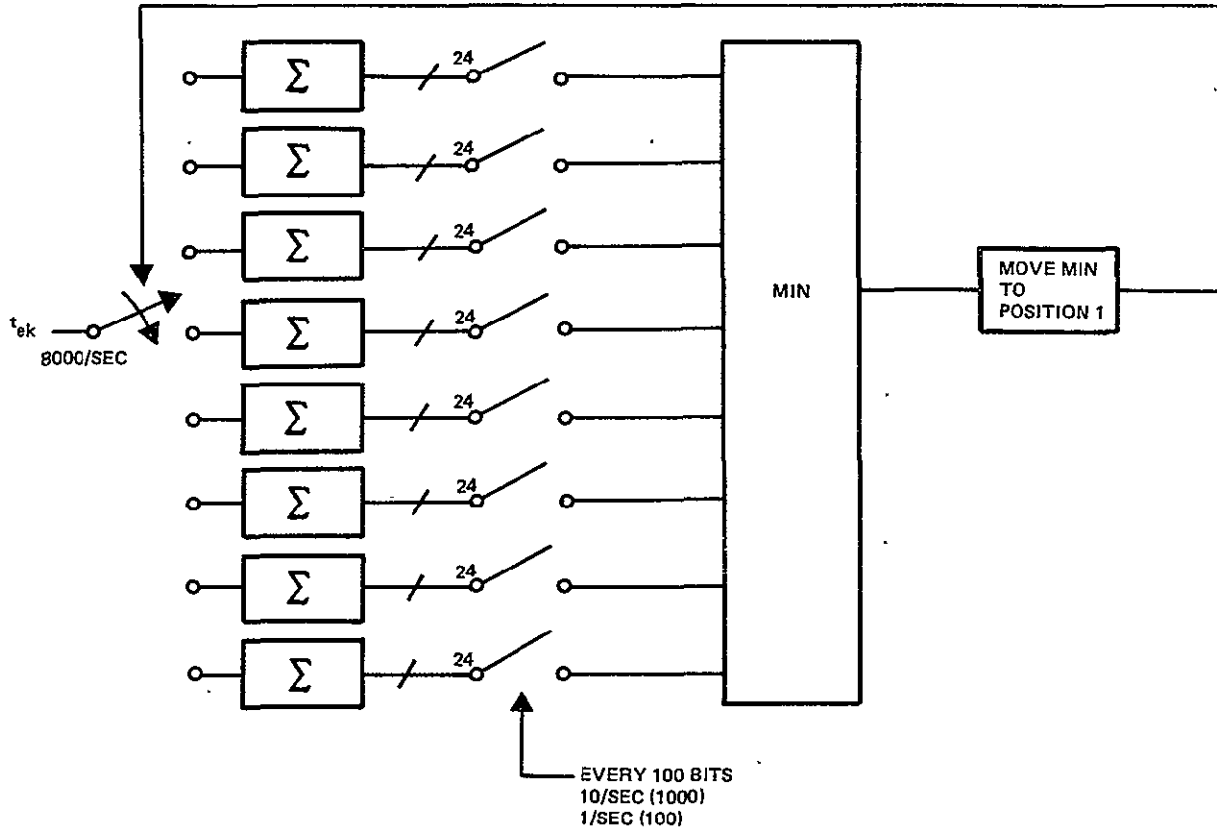
Table 2-9. Second Order Filter Program (Continued)

<u>Instruction</u>	<u>Code</u>
26	XR < AC2.L, X < (AC2.L), Y < a
27	XR < PA.L , PA.L < MP.L
28	XR < AC2.M, X < (AC2.M), A < MP.U
29	multiply B < MP.L
30	9 OPS XR < PA.M , PA.M < A + B
31	XR < AC2.U, X < (AC2.U), A < MP.U
32	B < MP.L
33	XR < PA.U , PA.U < A + B + C
34	XR < PA.L , A < (PA.L)
35	XR < PB.L , B < (PB.L)
36	XR < SM.L , SM.L < A + B
37	XR < PA.M , A < (PA.M)
38	XR < PB.M , B < (PB.M)
39	XR < SM.M , SM.M < A + B + C
40	XR < PA.U , A < (PA.U)
41	XR < PB.U , B < (PB.U)
42	XR < SM.U , SM.U < A + B + C
<u>43</u>	BR,UN.(START)
43	TOTAL OPS FOR = 43 → 45 SECOND ORDER LOOP

Table 2-10. Coarse Acquisition Program

Instruction	Code
1	SEND ACK
2	WAIT COMPLETE
3	XR < IK , A < (IK), X < $i_k$ , Y < $i_k$
4	XR < IK-1 , IK-1 < A
5	XR < IK , IK < $i_k$
6	XR < IK2.U, IK2.U < MP.U
7	XR < QK , A < MP.L
8	B < (QK), X < $q_k$ , Y < $q_k$
9	XR < QK-1 , QK-1 < B
10	XR < QK , QK < $q_k$
11	XR < QK2.U, QK2.U < MP.U
12	B < MP.L
13	BR.UN.(START)
14	START XR < IPQ.L, IPQ.L < A + B
15	XR < IK2.U, A < IK2.U
16	XR < QK2.U, B < QK2.U
17	XR < IPQ.U, IPQ.U < A + B + C
18	XR < IPQ.L, A < (IPQ.L)
19	XR < BS.L , B < (BS.L)
20	XR < IMB.L, IMB.L < A - B
21	XR < IPQ.U, A < IPQ.U
22	XR < BS.U , B < BS.U
23	XR < IMB.U, IMB.U < A - B - C
24	XR < AC.L , A < (AC.L)
25	16 BIT ADD XR < IMB.L, B < (IMB.L)
26	6 OPS XR < AC.L , AC.L < A + B
27	XR < AC.U , A < (AC.U)
28	XR < IMB.U, B < (IMB.U)
29	XR < AC.U , AC.U < A + B + C
30	ACCEPT INPUT REQUEST TO BRANCH ON THRESHOLD = 30 OPS ADD 45 FOR FILTER = 75 OPS FOR COARSE ACQUISITION

$$t_{ek} = i_k i_{k-1} + q_k q_{k-1} \text{ (8000/SEC MAX)}$$

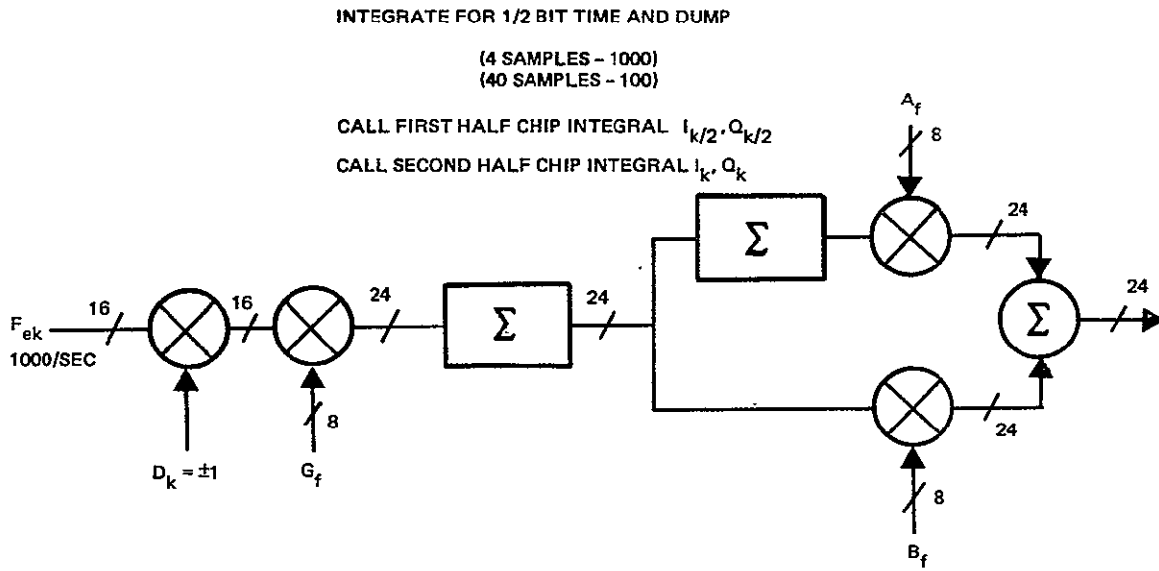


$t_{ek}$	2 SINGLE PRECISION MULTIPLIES	4
	1 DOUBLE PRECISION ADD	6
COMMUTATOR	1 ADDRESS MODULO 8	26
	1 TRIPLE PRECISION ACCUMULATE	9
	TOTAL	<u>45</u>

Figure 2-24. Coarse Bit Timing Algorithm

Table 2-11. Summary of Processor Speed Loading

Function		Maximum Ops/Function	Load
Coarse acquisition (8000/sec)			
Accept → threshold	35		
Second order filter	$\frac{45}{80}$	250	30%
Fine acquisition (8000/sec) (Coarse tracking)			
Frequency			
$f_{e_k}$	10		
Second order filter	45		
Time			
$t_{e_k}$	10		
Commutator	$\frac{35}{100}$	250	40%
Tracking (1000/sec)			
Integral truncation	40		
Frequency			
$F_{e_k}$	20		
Second order filter	45		
Time			
$T_{e_k}$	20		
$T_e$	20		
Data demod			
$D_k$	$\frac{20}{165}$	2000	9%
Maximum = 40% + 10% overhead =			50%



$$F_{ek} = (I_{k-1} + I_{k-1/2})(Q_k + Q_{k/2}) - (I_k + I_{k/2})(Q_{k-1} + Q_{k-1/2})$$

RATE	OPERATION	COUNT
1000	TRUNCATE HALF CHIP INTEGRALS (8 BITS)	40
1000	COMPUTE $F_{ek}$ FROM INTEGRALS	20
1000	SECOND ORDER FILTER	45
	TOTAL	105

Figure 2-25. Frequency Tracking Loop

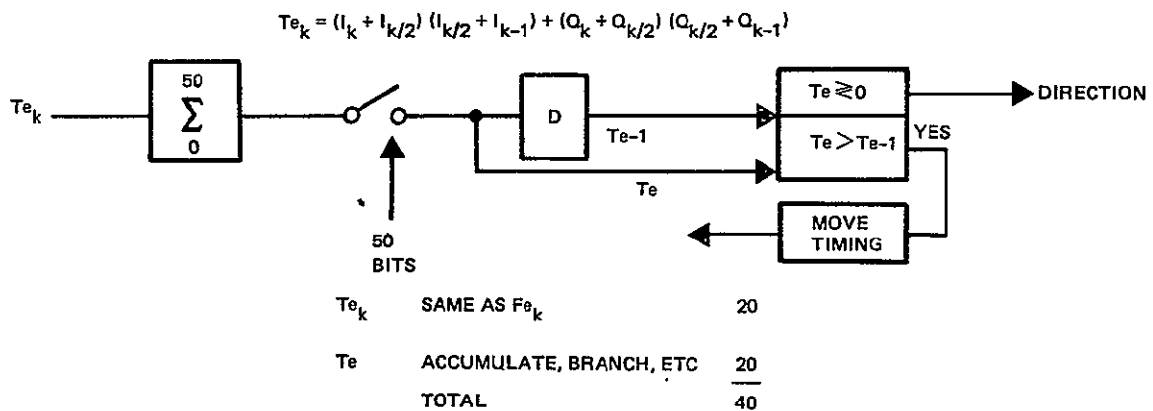


Figure 2-26. Fine Bit Timing



$$D_k = (I_k + I_{k/2}) (I_{k-1} + I_{k-1/2}) + (Q_k + Q_{k/2}) (Q_{k-1} + Q_{k-1/2})$$



$D_k$  SAME AS  $F_{e_k} = 20$   
 $SIGN(D_k) = 2$   
 TOTAL = 22

Figure 2-27. Data Demodulation

processes provided that accumulators and constants are reinitialized whenever the processing mode of the receiver changes. Given these assumptions, the program memory estimate of Table 2-12 has the same itemization as the loading estimate of Table 2-11 except for subtraction of memory for the second order filter in fine acquisition and tracking. Table 2-12 shows that 305 memory cells or 60% of the total capacity of 512 are used.

Table 2-12. Program Memory Usage Estimate

Coarse acquisition		
Accept → threshold		35
Second order filter		45
Fine acquisition (coarse tracking)		
Frequency	$f_{e_k}$	10
Time	$t_{e_k}$	10
	Commutator	35
Tracking		
Integral truncation		40
Frequency	$F_{e_k}$	20
Time	$T_{e_k}$	20
	$T_e$	20
Data demod		
Data	$D_k$	<u>20</u>
Total		255
Overhead		<u>50</u>
		305
	305/512	60% Capacity

It is also estimated that approximately 50% of the total data memory capacity is used. Hence, no more than 60% of any processor resource is used in implementing the hybrid receiver signal processing algorithms.

#### 2.3.4 Algorithm Development Procedure

The basic hybrid receiver signal processing algorithms have been simulated extensively in FORTRAN and meet specification requirements. Hence, the development process referred to in this section consists of translating these algorithms from their current block diagram form to "firmware" which is acceptable to the digital signal processor (DSP) and designing the overhead firmware. A number of filter multipliers and gain constants must also be determined during this development phase, since the DSP does no fractional or floating point arithmetic.

A basic requirement of this development phase is an assembler which translates the language specified in Section 2.3.3 to the DSP control word format. This assembler should probably be written in FORTRAN and be designed to be as machine independent as possible. It would generate hard copy binary output, such as paper tape, for control memory contents and a listing of the source language input for reference purposes.

The development phase also requires a breadboard which has a read/write program memory instead of the normal read-only program memory and test equipment to monitor and display performance parameters, demodulated data, etc. The read/write program memory requires additional test equipment to load, display, and edit the program memory during development.

The basic algorithm development procedure consists of the following five steps:

- Transform "block diagram" algorithms to firmware algorithms
- Design I/O real time control algorithms
- Debug and verify firmware algorithms using breadboard and test equipment
- Determine gain constants, filter multipliers, etc. to satisfy performance requirements
- Program read/only memories and convert RAM breadboard to PROM breadboard.

An optional requirement is to have a software simulation of the DSP. A register transfer level processor simulation is a very useful tool in firmware development. Although not required, this tool provides an accessible machine model and can be used as a firmware debugging aid before any hardware is available.

### 3. SYSTEM ANALYSIS AND ALGORITHM DESIGN

This section summarizes the analysis and design of the processing algorithms within the digital signal processor. The processing is made of up:

- The coarse frequency acquisition, which determines the center frequency of the received signal to within an accuracy of  $\pm 1$  kHz
- The coarse frequency tracking algorithms, which further resolve the signal carrier frequency to within 10% of the data rate
- Coarse bit timing algorithms, which estimate bit timing to within 1/16th of a data bit duration
- The demodulation and decision directed tracking algorithms for both continuous phase frequency shift keying (CPFSK) and differential phase shift keying (DPSK).

The selected algorithms were chosen to minimize overall processor complexity and still meet the design specifications. To accurately assess the performance of the receiver and help select the design parameters, simulation programs were developed. The description of the simulations and the measurement results are included in this section.

#### 3.1 COARSE FREQUENCY ACQUISITION

Coarse frequency acquisition is defined as the process of reducing the received signal frequency uncertainty to a value within the pull-in capability of the frequency tracking loop. The design of the acquisition algorithm is particularly important because of its impact on mission objectives and on the complexity of the signal processor. Therefore, considerable effort was expended in designing an algorithm which best satisfies the performance objectives with minimum processing complexity. This section describes the selected algorithm and its projected performance based on analysis and simulation.

##### 3.1.1 Acquisition Performance Objectives

The significant measure of performance for the hybrid receiver application is acquisition time, which is defined as the time between initiation of the frequency search algorithm and correct detection of the signal to an accuracy within the pull-in range of the frequency tracking loop. The desired acquisition time is 50 sec. under the situations given in Table 3-1. The frequency uncertainty is  $\pm 80$  kHz, which includes an offset of  $\pm 75$  kHz due to doppler shift and an additional offset of  $\pm 5$  kHz to allow for inaccuracies between the local oscillator frequencies of the transmitter and receiver. The frequency uncertainty range determines the extent of the search pattern and, therefore, is directly related to acquisition time. Information which reduces this uncertainty or which indicates which regions are more likely to contain the signal can reduce the acquisition time. The doppler rate is  $\pm 50$  Hz/sec. It is assumed that the doppler rate can be sustained as long as the doppler shift is less than  $\pm 75$  kHz.

Table 3-1. Frequency Acquisition Performance Parameters

Frequency uncertainty	±80 kHz
Doppler rate	±50 Hz/sec
Probability of detection	0.995
Probability of false alarm	$10^{-4}$
C/N <sub>0</sub>	24.5 dB-Hz at 100 bps 34.5 dB-Hz at 1000 bps

The desired probability of detection is 0.995 with a probability of false alarm less than  $10^{-4}$ . The effective carrier-to-noise density ratio at which this level of performance is to be achieved is 24.5 dB-Hz for a data rate of 100 bps, increasing proportionally to 34.5 dB-Hz for a data rate of 1000 bps. These levels are 0.5 dB higher than those given in the statement of work and are based on an evaluation of the receiver worst case noise figure and degradation sources in the implementation of the receiver. This is discussed further in Section 3.1.3.

### 3.1.2 Sequential Detection Algorithm Description

The sequential detection algorithm was selected from a number of candidates as the acquisition algorithm for the hybrid receiver based on its performance and relative ease of implementation. The basic idea of sequential detection is to perform a continuous test of the decision variable (detector output) against a threshold rather than take a fixed sample size for each frequency hypothesis. The test duration is thus a random variable rather than a constant. If the test is properly designed, however, the mean time to acquire the signal can be significantly reduced from that of a fixed sample size test. The heuristic explanation for this is that frequency cells containing noise only can be dismissed quickly, as soon as the test statistic indicates a high probability of no signal, rather than after a full period integration. Therefore, in situations where a large number of empty cells must be searched, as is true in this application, the time required to search these cells can be considerably reduced.

Figure 3-1 is a functional flow diagram of the sequential detection algorithm. For a given frequency hypothesis, the input inphase and quadrature components are filtered, sampled, squared, and summed. This produces a measurement which essentially reflects the energy in the signal. A bias is then subtracted. The bias is selected such that with a noise-only input, the accumulated envelope detector output minus the bias decreases with integration, while for inputs consisting of signal-plus-noise, the accumulated detector output minus the bias increases with integration. The optimum choice for the bias is the midpoint between the mean detector output for signal-plus-noise and noise-only.

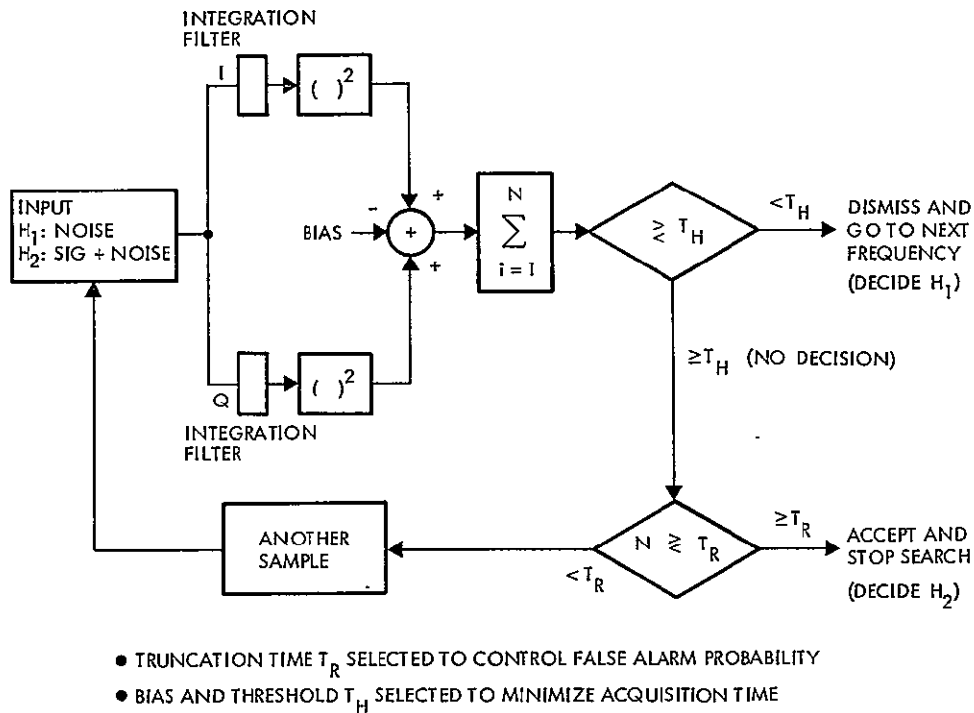


Figure 3-1. Sequential Detection Algorithms

As each new signal sample is taken, the bias is subtracted and the result is added to a running sum. The sum is compared to a (negative) threshold  $T_H$  after each new sample is added. If the sum falls below the threshold, the signal is presumed not to be present in that frequency cell and the hypothesis is dismissed, the sum reset, and the receiver stepped to the next frequency hypothesis. If the sum is above the threshold  $T_H$ , another sample is taken and the process is repeated. If however, the number of samples taken is greater than the threshold  $T_R$  (referred to as the truncation time), then the signal is declared present.

The bias and the threshold  $T_H$  are selected to minimize the acquisition time. As the bias is increased, the integrated output has a stronger negative bias and therefore a frequency bin containing noise-only is dismissed faster. But if the bin contains a signal, there is a greater likelihood that the bin will be incorrectly declared as having no signal, thereby necessitating an increased number of passes through the uncertainty region in order to detect the signal. Thus, although the dismissal time is decreased for increased bias, the acquisition time may increase due to the greater number of passes required to detect the signal. Conversely, as the bias is decreased, the dismissal time increases, but the probability of detection per pass increases. Therefore, although the search time per pass is increased, the number of passes is decreased. It should be apparent that there is an optimum choice for the bias. Analysis shows that the bias should be selected equal to the midpoint of the detector output for signal-plus-noise and noise-only.

A similar phenomenon occurs with variations in the threshold  $T_H$ . As  $T_H$  is increased (made more positive), the dismissal time per cell is decreased but the probability of false dismissal is also increased. As  $T_H$  is decreased, the dismissal time increases but the probability of detection increases also. Therefore, an optimum choice exists for  $T_H$ .

The truncation time  $T_R$  primarily controls the false alarm probability. It has some effect on the probability of detection, but analysis and simulation show this effect to be small and negligible for reasonably large values of  $T_R$ . As  $T_R$  is increased beyond a certain point, the probability of detection remains almost constant. The probability of false alarm, however, decreases rapidly as  $T_R$  is increased so that appropriate selection of  $T_R$  sets the false alarm probability at the desired level.  $T_R$  has a very small effect on the acquisition time since the test duration is  $T_R$  only for the frequency bin in which there is a signal. The prime determinant of acquisition time is the time required to dismiss a bin containing noise alone because of the large number of such bins which must be searched.

Another important algorithm parameter is the bandwidth of the integration filter. As the bandwidth is made wider, the number of bins into which the frequency uncertainty is divided is reduced, but the signal-to-noise ratio is also reduced. As the bandwidth is narrowed, the signal-to-noise ratio increases (provided the data bandwidth is less than the filter bandwidth) but the number of bins also increases and, in addition, the filter response time grows and becomes a significant fraction of the dwell time at each frequency. An optimum choice for the integration filter bandwidth therefore exists.

The sequential algorithm also requires knowledge of the receiver noise level in order to set the bias and threshold. Since this parameter is not known a priori, it is estimated by measuring the average power of the input signal as the search progresses. A relatively long integration time is used to smooth over variations in the noise samples. The integration filter memory extends over many frequency bins so as to allow discrimination of the presence of a signal in one of the bins.

A pictorial showing a sequential detection example is given in Figure 3-2. The upper path shows a typical sample for the accumulated detector output for signal-plus-noise. It remains above the threshold  $T_H$  until the truncation time  $T_R$  is reached, whereupon a detection is declared. The lowest path shows a typical sample of noise only. It crosses the negative threshold  $T_H$  early, allowing the empty bin to be dismissed quickly. This is the advantage of the sequential detection algorithm over the fixed sample size algorithm. By allowing quick dismissal of a frequency bin based on a continuous estimate of the likelihood of that bin containing a signal, a large number of bins can be searched in a relatively short period of time.

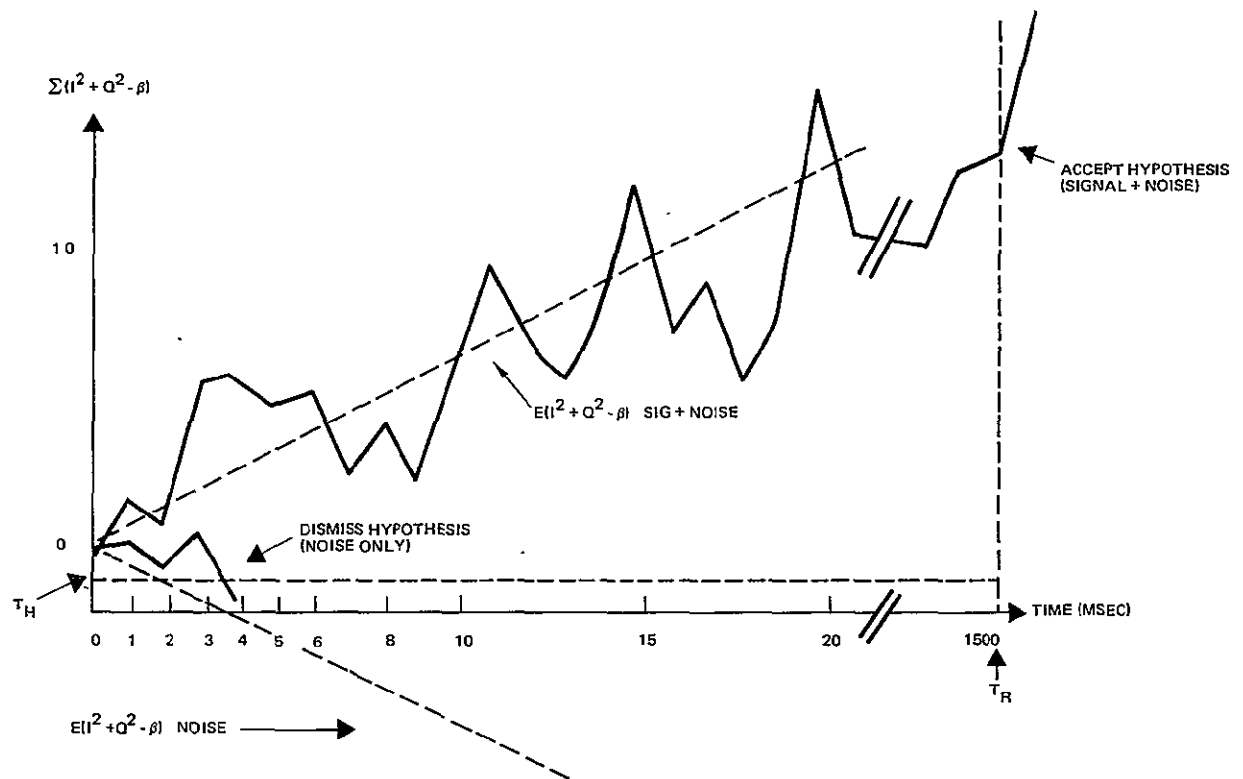


Figure 3-2. Sequential Detection Example

### 3.1.3 Sequential Detection Algorithm Performance Analysis

Evaluation of the sequential detection algorithm was performed via a combination of analysis and simulation. Particular attention was given to including all identifiable loss factors. Therefore, it is felt that the acquisition time results presented here are an accurate estimate of the acquisition time to be achieved in an actual implementation of this algorithm.

#### Loss Budget

To perform an accurate assessment of the acquisition algorithm performance, loss factors were identified and a loss budget was set up as shown in Table 3-2. The minimum carrier power was specified in the statement of work as -146 dBm. The noise spectral density represents thermal noise present in an ideal receiver front end at standard temperature (290<sup>0</sup>K). The receiver noise figure of 3.2 dB is a worst case estimate based on the proposed implementation of the receiver front-end. The available RF carrier-to-noise density ratio is therefore 24.8 dB-Hz for a data rate of 100 bps. At higher data rates, the carrier power increases proportionally, so that at 1000 bps the available C/N<sub>0</sub> is 34.8 dB-Hz.

The quantization noise due to digitization of the input signal to 8 bits was evaluated as being negligible. As was shown in Section 2, the worst case noise power density due to quantization is 27 dB below thermal noise so that the quantization noise is negligible.

Table 3-2. Frequency Acquisition Loss Budget

	100 bits/second	1000 bits/second
Minimum carrier power	-146 dBm	-136
Noise spectral density	-174 dBm/Hz	-174
Maximum receiver noise figure	3.2 dB	3.2
Available RF $C/N_0$	24.8 dB-Hz	34.8
Maximum IF filter loss	0.1 dB	0.1
A/D quantization noise (-30 dB down)	-0-	-0-
Aliasing noise (-40 dB down)	-0-	-0-
Processor quantization loss	-0-	-0-
Frequency offset	Included in sim	Included in sim
Timing offset	Included in sim	Included in sim
Noise power estimate error	Included in sim	Included in sim
Available $C/N_0$	24. dB	34.7 dB
$C/N_0$ input to simulator	24.5 dB	34.5 dB
Margin	0.2 dB	0.2 dB

The loss due to the IF filter which precedes the A/D converter was evaluated for various filter shapes. Figure 3-3 shows the IF filtering considerations. The filter bandwidth was selected to minimize signal degradation and dynamic range at the A/D input (see Section 2.2.2). As the bandwidth is made narrower, signal degradation increases due to distortion of the signal itself. The amount of degradation was evaluated through simulation, which included the effects of intersymbol interference and pulse shape distortion. In addition, pre-A/D dynamic range increases, which degrades the NPR. As the bandwidth is increased, the signal degradation decreases and dynamic range decreases because the filter output becomes noise dominated. However, it is necessary that the filter response roll off quickly to eliminate the possibility of false sync due to the aliased signal resulting from sampling. As the figure shows, it is desirable that the filter response be at least 40 dB down at the aliased signal location, which becomes significant 7 kHz away for an 8 kHz sampling rate. This guarantees that a large signal 8 kHz away, which can be 30 dB larger than the smallest expected signal (since the specified signal dynamic range is 30 dB) will not create a false response, since the amplitude due to such an offset signal will be at least 10 dB below the smallest expected signal. Therefore, the wider the filter bandwidth, the more complex the filter since more poles are required to obtain the desired rolloff.



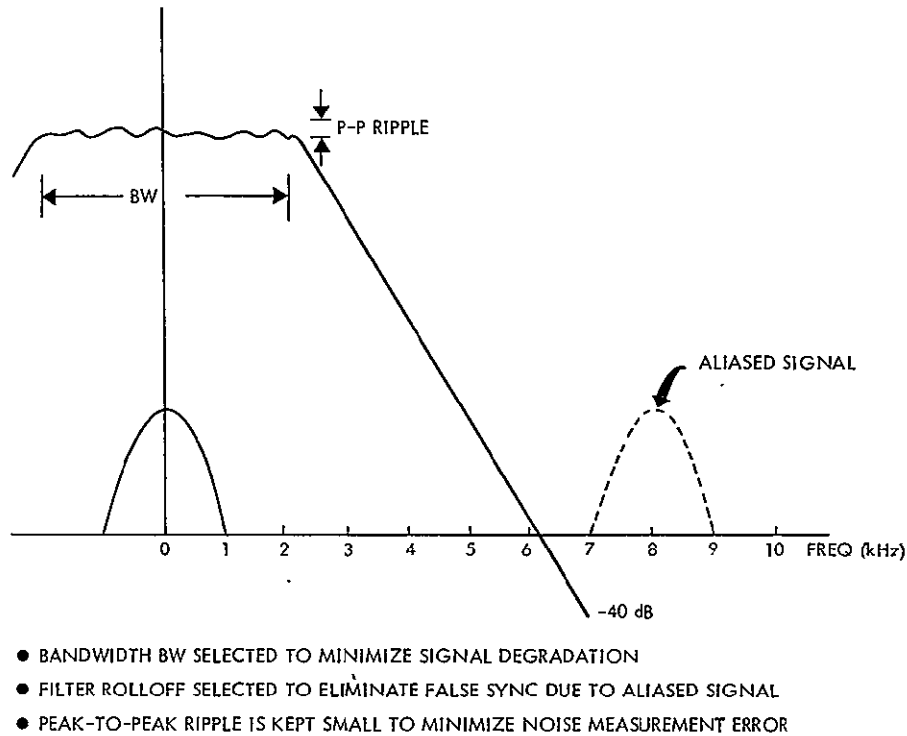


Figure 3-3. IF Filtering Considerations

Table 3-3 is a listing of the different types of filters considered, with the peak-to-peak ripple, the rejection at 7 kHz, and the degradation in signal-to-noise ratio caused by the filter. The in-band ripple is of interest because it affects the accuracy with which noise estimates can be made for setting the bias and threshold in the sequential detection algorithm. As shown, the Chebyshev filter of 3 dB bandwidth, 4.84 kHz, and peak-to-peak ripple 0.1 dB is the proposed filter. It has the advantages of simplicity (a 4-pole filter is sufficient), small in-band ripple (0.1 dB), good rejection of the aliased signal (-46 dB), and small signal-to-noise ratio degradation (less than 0.1 dB). In addition, the bandwidth is sufficiently large such that the A/D converter NPR is only minimally degraded over the full signal dynamic range with no AGC. The other filters are either more complex, have greater ripple, or more degradation.

The acquisition algorithm was evaluated using a simulation program designed specifically to determine the effects of finite word size arithmetic on the performance of signal processing algorithms. Figure 3-4 shows a block diagram of the simulation. The input signal is offset in frequency to simulate the effect of doppler, and white Gaussian noise is added. The signal is then filtered and quantized by an 8-bit A/D converter. The rest of the processing is exactly as it would be performed in the microprocessor. The selected word size was 16 bits, as it would be in the proposed implementation. The results of this simulation indicate that the degradation in performance due to the 8-bit A/D conversion and the 16-bit arithmetic in the subsequent processing is negligible.

Table 3-3. IF Filtering Losses

Filter Type	P-P Ripple ±2 kHz	Rejection at 7 kHz	Signal-to-Noise Ratio Degradation
Butterworth 6 poles, BW (3 dB) = 6 kHz	0.03	44	0.02
Butterworth 5 poles, BW (3 dB) = 5.72 kHz	0.1	39	0.01
Butterworth 4 poles, BW (3 dB) = 4 kHz	3	44	0.08
Butterworth 3 poles, BW (3 dB) = 3 kHz	8	40	0.14
Chebyshev 5 poles, BW (3 dB) = 4.52 kHz	0.1	61	0.12
Chebyshev* 4 poles, BW (3 dB) = 4.84 kHz	0.1	46	0.07
Chebyshev 4 poles, BW (3 dB) = 4.52 kHz	0.3	50	0.10
Chebyshev 4 poles, BW (3 dB) = 4.36 kHz	0.5	53	0.12

\*Proposed filter

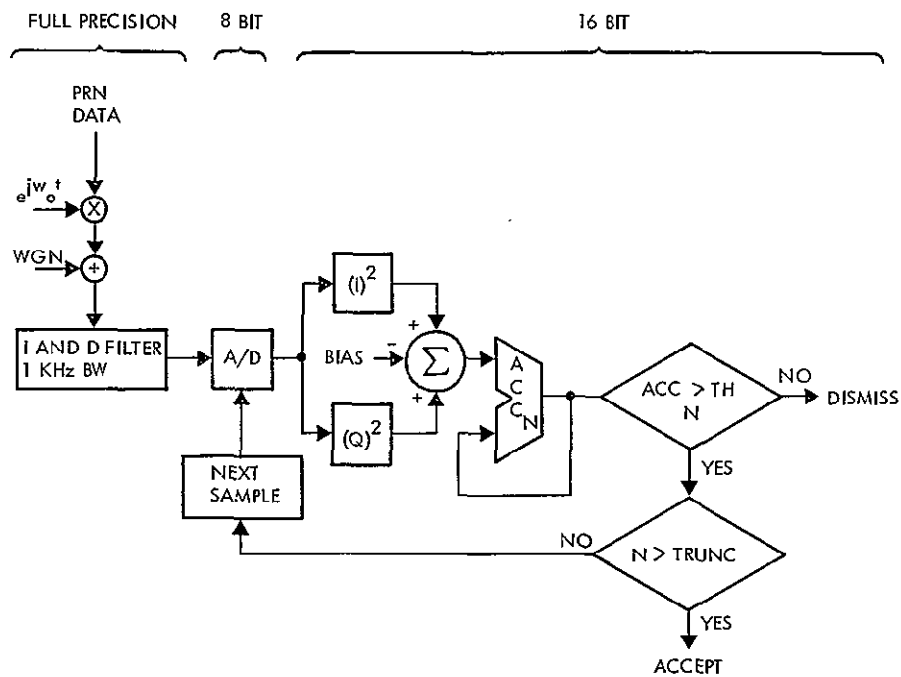


Figure 3-4. Finite Word Size Simulation

Because of the complexity and large amounts of computer time required to run the simulation described above, it was not used in optimizing the acquisition algorithms. It was used to obtain performance estimates in selected cases only. Instead, a simplified simulation program was written to simplify the optimization process. As a part of this simulation program, the effects of frequency offset was included. Since the frequency uncertainty region is searched in discrete frequency steps, the actual received frequency may differ from the center frequency of the frequency cells. As a result, the effective signal-to-noise ratio in that cell is reduced. It can be shown analytically that the loss, L, for a matched filter which is offset in frequency is given by

$$L(\text{dB}) = 20 \log \frac{\sin \pi \Delta f T}{\pi \Delta f T}$$

where  $\Delta f$  = the frequency offset in Hz and  $T$  = the matched filter integration time. Figure 3-5 shows a plot of this loss as a function of  $\Delta f T$ . As the spacing between frequency cells increases,  $\Delta f$  decreases so that the frequency offset loss decreases, but there are more cells to search. There is an optimum choice for frequency cell spacing for minimum acquisition time. In the simulation, the loss in SNR due to frequency offset was calculated from the above formula for the randomly chosen signal frequency.

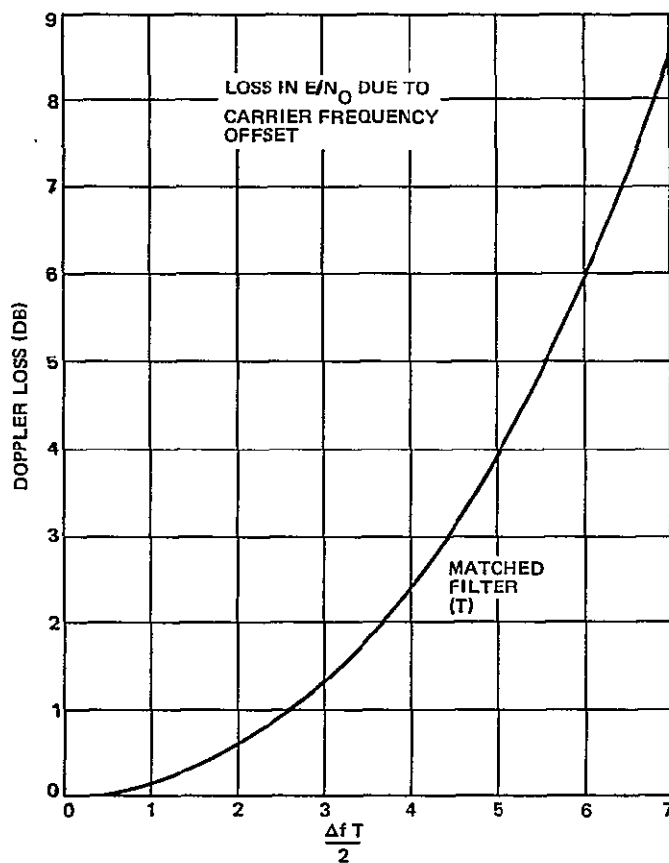


Figure 3-5. Loss in  $E/N_0$  Due to Carrier Frequency Offset

Another factor in the acquisition loss budget is the loss in SNR due to sample time offset. The effect is seen in Figure 3-6, where the envelope response of two filters is shown, one having impulse response duration  $T$  which is matched to the pulse-width and the other having impulse response duration  $T/2$ . For the matched filter, note that the output envelope ( $\sqrt{I^2 + Q^2}$ ) decreases to zero for each transition in the data. This implies that during the acquisition phase, many of the matched filter output samples could fall within these "dips" since data transition times are not known.

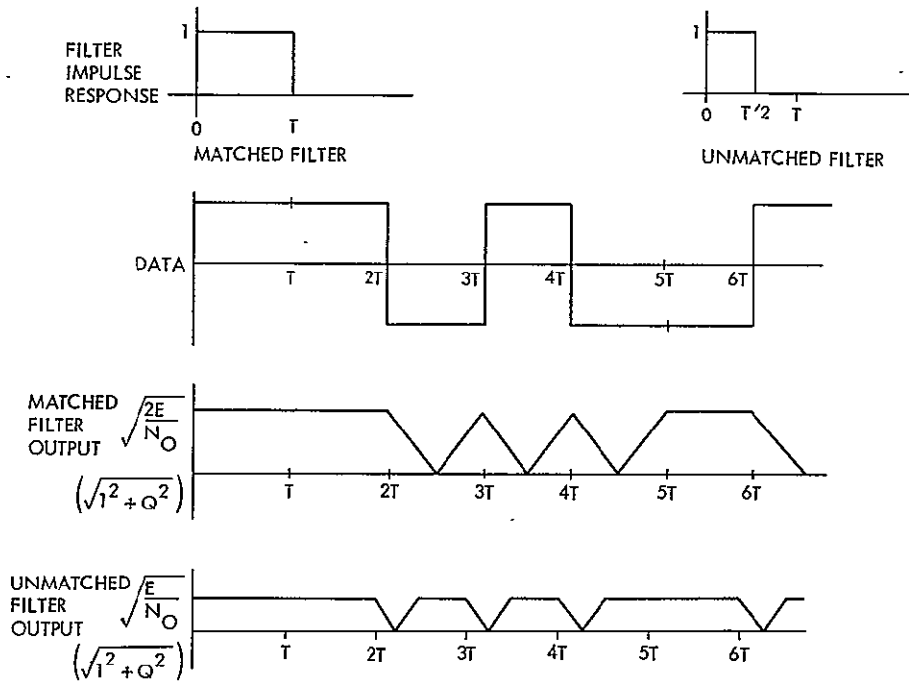


Figure 3-6. Loss in  $E/N_0$  due to Sample Time Offset

Figure 3-6 also shows the output of an unmatched filter (one having impulse response duration  $T/2$ ) to the same data pattern. As before, there are dips in the envelope corresponding to transitions in the data, but the dips occupy a smaller fraction of the time. However, the peak SNR is 3 dB lower than the peak SNR in the matched filter case.

In the simulation, the loss due to sampling time offset was computed for a randomly selected sample time relative to the data transitions. The specific loss function is, as shown above, a function of data rate and integration time.

The recommended sequential detection algorithm requires knowledge of the magnitude of the noise power spectral density in order to set the bias and threshold values appropriately. As indicated earlier, the optimum bias value is equal to the midpoint between signal and signal-plus-noise. In the actual implementation of the algorithm, the noise amplitude is unknown. Therefore, an estimate of its value is made by computing the mean square value of the filter output as the frequency uncertainty region is searched. This mean square value is then used to estimate the noise. It is

continually updated as the search algorithm progresses. The simulation reflects the implementation of this technique and, therefore, accurately evaluates the effects of error in the noise estimate.

### Acquisition Algorithm Simulation Description

To accurately assess the performance of the sequential detection algorithm, a simulation program was developed. The program accurately simulates the effects of frequency offset, time offset, and noise measurement inaccuracy as described previously, and enables the designer to select parameters, such as bias and thresholds, and to evaluate performance.

Figure 3-7 shows a block diagram of the simulation. It replicates the implementation of the sequential algorithm in the microprocessor. To evaluate the acquisition time, it is necessary to evaluate two quantities. These are the time required to dismiss a frequency cell which contains noise-only and the probability of detecting the presence of a signal if one is present. The simulation program is a Monte Carlo type which produces the probability distribution function of the dismissal time and computes the probability of detection.

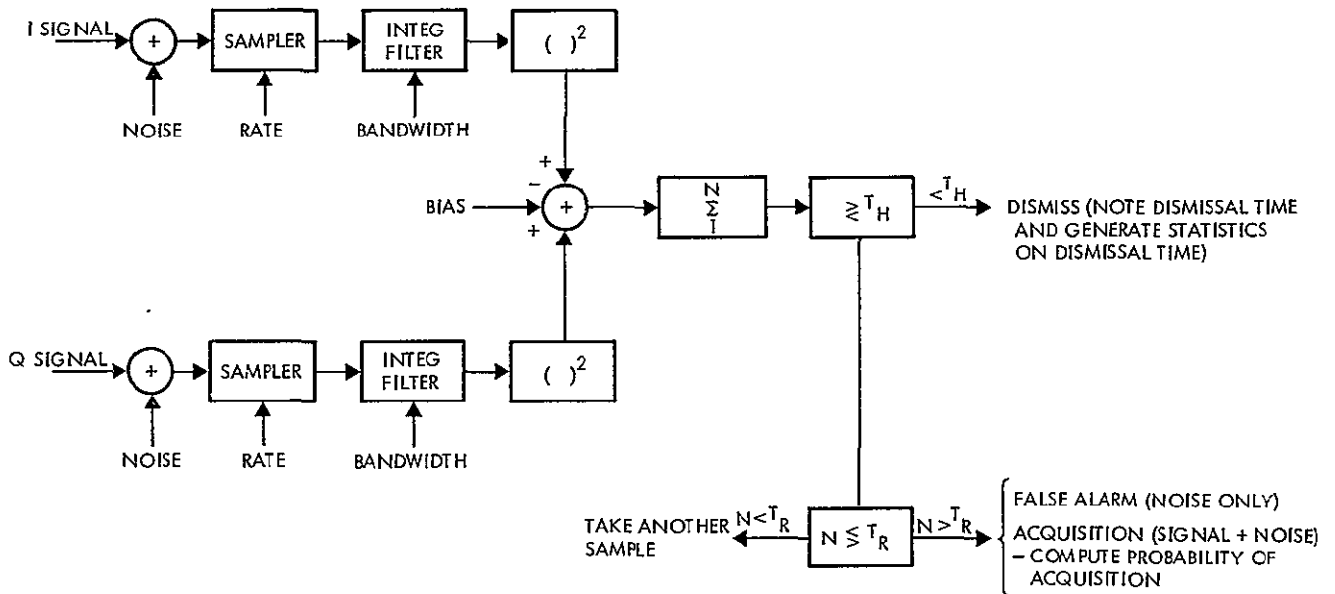


Figure 3-7. Sequential Detection Algorithm Simulation Block Diagram

To evaluate the dismissal time, noise-only is input to the simulation. The noise samples are integrated as they would be in a moving window filter and the filter output envelope ( $\sqrt{I^2 + Q^2}$ ) is computed. The bias is then subtracted and the result is accumulated. The accumulated sum is compared to a threshold  $T_H$  after each sample is added. The number of samples required before the threshold  $T_H$  is crossed is determined and statistics of this random variable are computed over a large number of trials. The

simulation results in the distribution function of the threshold crossing time. A sample of this is shown in Figure 3-8, which shows the probability that the threshold has not been crossed at time  $t$  as a function of  $t$ . The simulation also computes the average dismissal time, which is used as explained below in optimizing the algorithm parameters.

The simulation program is also used to estimate the probability of detection. For each acquisition trial, a random sampling time relative to the bit transitions is selected and the loss due to sampling time offset is computed as previously described. In addition, a random frequency offset is selected and the loss due to this offset is calculated for each frequency cell for which the signal is within the null-to-null bandwidth of the moving window filter. The simulation is then run for each of these frequency cells and statistics equivalent to those produced in the noise only case are computed. That is, the probability that the threshold is not crossed before time,  $t$ . Note that in this case, the probability of detection is given by the probability that the threshold is not crossed before  $T_R$ , the truncation time. Figure 3-8 shows a sample result of the simulation for signal-plus-noise input.

The two results from the simulation program, namely the average time to dismiss an empty frequency cell,  $\overline{TDIS}$ , and the probability of detection, PDET, can be used to calculate the mean time to acquire  $\overline{TACQ}$  as follows

$$TACQ = \sum_{i=1}^N (TDIS(i) + TI) + T_R$$

where

$TDIS(i)$  = the time to dismiss cell  $i$

$N$  = the number of cells searched before the signal is detected

$TI$  = filter settling time

$T_R$  = the test truncation time

Then

$$\overline{TACQ} = \overline{N} (\overline{TDIS} + TI) + T_R$$

where

$$\overline{N} = E(N) = 1/2 N_u PDET + 3/2 N_u (1-PDET)PDET + 5/2 N_u (1-PDET)^2 PDET + \dots$$

$N_u$  = number of frequency cells in uncertainty region

Therefore

$$\overline{N} = N_u PDET \left( \frac{1}{PDET} \right)^2 - 1/2 N_u = \frac{N_u}{PDET} - 1/2 N_u$$

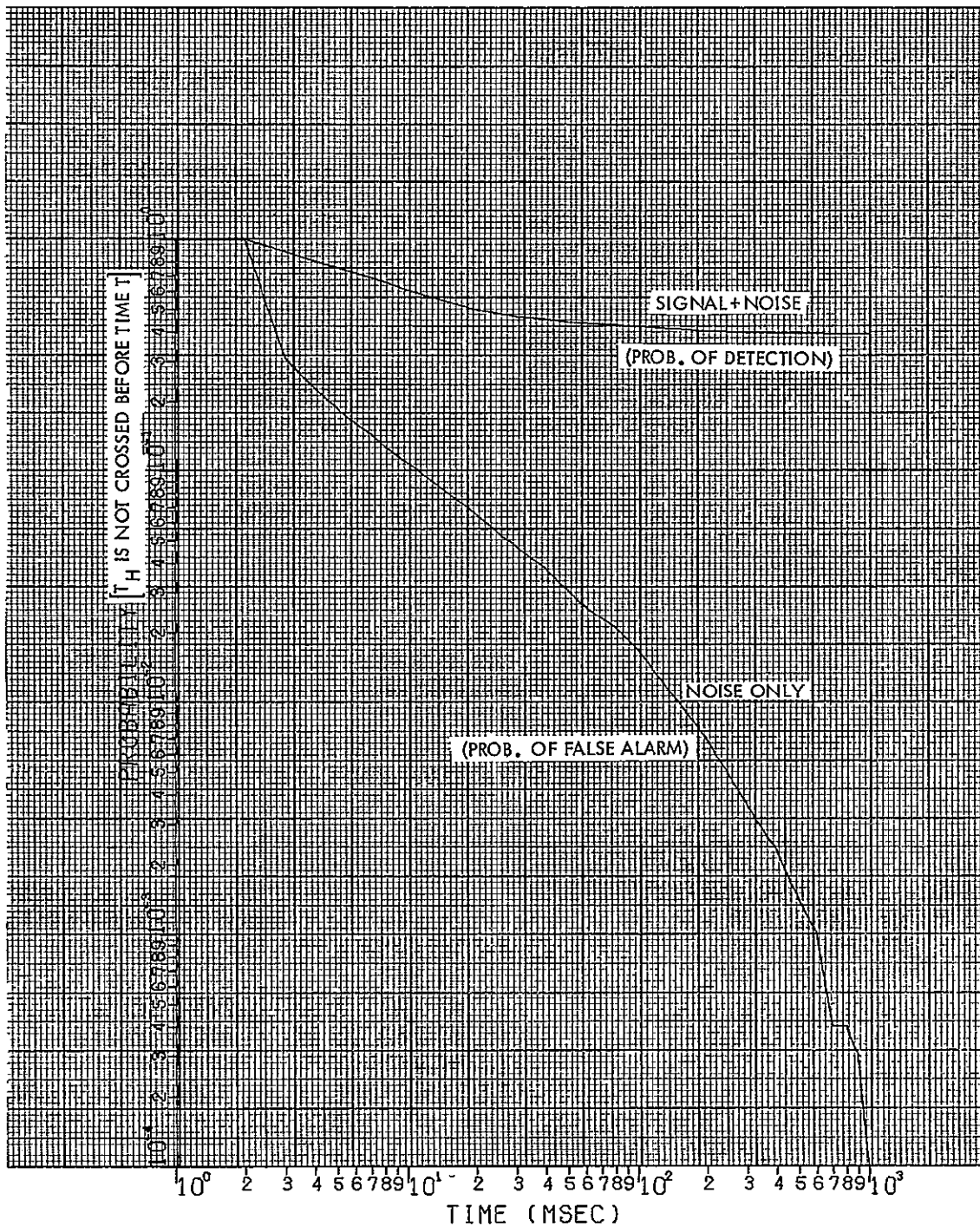


Figure 3-8. Probability Distribution of Threshold Crossing Time

The mean time to acquire is then given by

$$\overline{TACQ} = \left( \frac{N_u}{P_{DET}} - 1/2 N_u \right) (\overline{TDIS} + T_I) + T_R$$

and

$$N_u = F_u / \Delta F$$

$F_u$  = frequency uncertainty = 160 kHz

$\Delta F$  = frequency step size for search algorithm

Using  $\overline{TACQ}$  as the criterion of performance (that is, minimizing the mean time to acquire) the simulation program was exercised to give  $\overline{TDIS}$  and PDET for various values of  $\Delta F$ , TI, input bit rate, sample rate, bias, and threshold. The values of  $\Delta F$ , which is the spacing between frequency steps, TI, the inverse of the integration filter bandwidth, bias, and threshold were optimized to give minimum  $\overline{TACQ}$ . The results are summarized in the next section.

The analysis given above neglects the effects of false alarms. This is reasonable in this case since the false alarm rate was set to be very low through choice of the truncation time,  $T_R$ . The effect of  $T_R$  on the probability of false alarm and probability of detection can be seen in the example of Figure 3-8. Note that as  $T_R$  increases, the probability of false alarm decreases very rapidly, but the probability of detection remains relatively constant beyond a certain point. Therefore,  $T_R$  can be selected to achieve any false alarm probability desired without significantly affecting the acquisition time since PDET is not affected and  $T_R$  is normally a small component of  $\overline{TACQ}$ .

The calculation of the mean time to acquire a signal can be extended to yield an estimate of the time to acquire with probability equal to an arbitrary value P as follows. We first make the assumption that the signal detection events are independent from one pass through the uncertainty region to the next. Then, the probability of detecting the signal in N passes or less is given by

$$P(N) = 1 - (1 - PDET)^N$$

where PDET = probability of detection in one pass. By setting a value for P(N) say 0.995, the number of passes, N, required to achieve this can be found and the acquisition time can be estimated by using this value of N in conjunction with the dismissal time per cell,  $\overline{TDIS}$ , and the number of cells to be searched  $N_0$ , as follows

$$TACQ \approx (NN_u - N_u/2) (\overline{TDIS} + TI) + T_R$$

This is an estimate of the acquisition time, assuming that the sum of the dismissal times over a large number of trials is equal to the number of trials times the average dismissal time.

#### Acquisition Algorithm Simulation Results

The simulation program described in the previous section was run for a large variety of cases. The variable parameters were input signal bit rate, sampling rate, integration filter bandwidth, frequency step size, carrier-to-noise density ratio, bias, threshold, truncation time, and number of trials. The objective of this effort was to optimize the choice of integration filter bandwidth, step size, bias, threshold, and truncation time and to estimate the acquisition time for these optimized parameters.



One parameter whose value could be set independently of others was the truncation time for the sequential test. As discussed earlier, the truncation time is selected primarily to control the false alarm rate. Based on early simulation results, it was determined that a truncation time of 1.5 sec. was sufficiently long to produce a negligibly low false alarm rate. In simulation runs involving 100,000 trials, no false alarms were observed and it is estimated that the probability of false alarm per trial is less than  $10^{-6}$ .

The simulation results also indicated that a reasonable choice for the frequency step size is one-half the bandwidth of the integration filter. A smaller value for the step size results in an increased number of search cells without a commensurate decrease in frequency offset loss. Consequently, the acquisition time is increased. A large value for the step size reduces the number of search cells, but the worst case frequency offset loss becomes significantly larger, resulting in reduced SNR and increased acquisition time. This effect can be seen by noting that the worst case frequency offset loss, (one-half the spacing) is 0.25 dB for a step size of one quarter the bandwidth, 0.9 dB for a step size of one-half the bandwidth, and 4 dB for a step size equal to the bandwidth (Figure 3-5).

A third constraint placed on the parameter set was that the threshold,  $T_H$ , was always related to the bias B by

$$T_H = -2(B-1)$$

This choice is based on simulation results which show this to be a reasonable choice in terms of optimizing performance for a range of biases.

The remaining parameters of bias and integration filter bandwidth were varied independently to minimize the acquisition time. The low data rate case (100 bps) is the worst case situation since it corresponds to the lowest available signal to noise ratio ( $C/N_0 = 24.5$  dB-Hz). As the data rate increases, the available SNR is also assumed to increase in proportion, thereby alleviating the detection problem. Consequently, greater effort was concentrated on the low data rate case.

Figure 3-9 shows the simulation results for the case where the input bit rate is 100 bps, the sampling rate is 2000 samples/sec., the integration filter bandwidth is 1000 Hz, the frequency step size is 500 Hz, the  $C/N_0$  is 24.5 dB-Hz, and the truncation time is 1.5 sec. The results are plotted in terms of the probability that the threshold is not crossed before time  $t$  vs  $t$ . Two cases are shown, one where noise-only is present. In each case, the bias is varied to show its effect. It is clear from the curves that for the noise-only case, the probability that the threshold is not crossed at crossing time and is a strong function of  $t$ , decreasing quickly as  $t$  is increased. For the signal case, however, the probability of threshold crossing is a relatively weak function of  $t$  beyond a certain point, remaining almost constant as  $t$

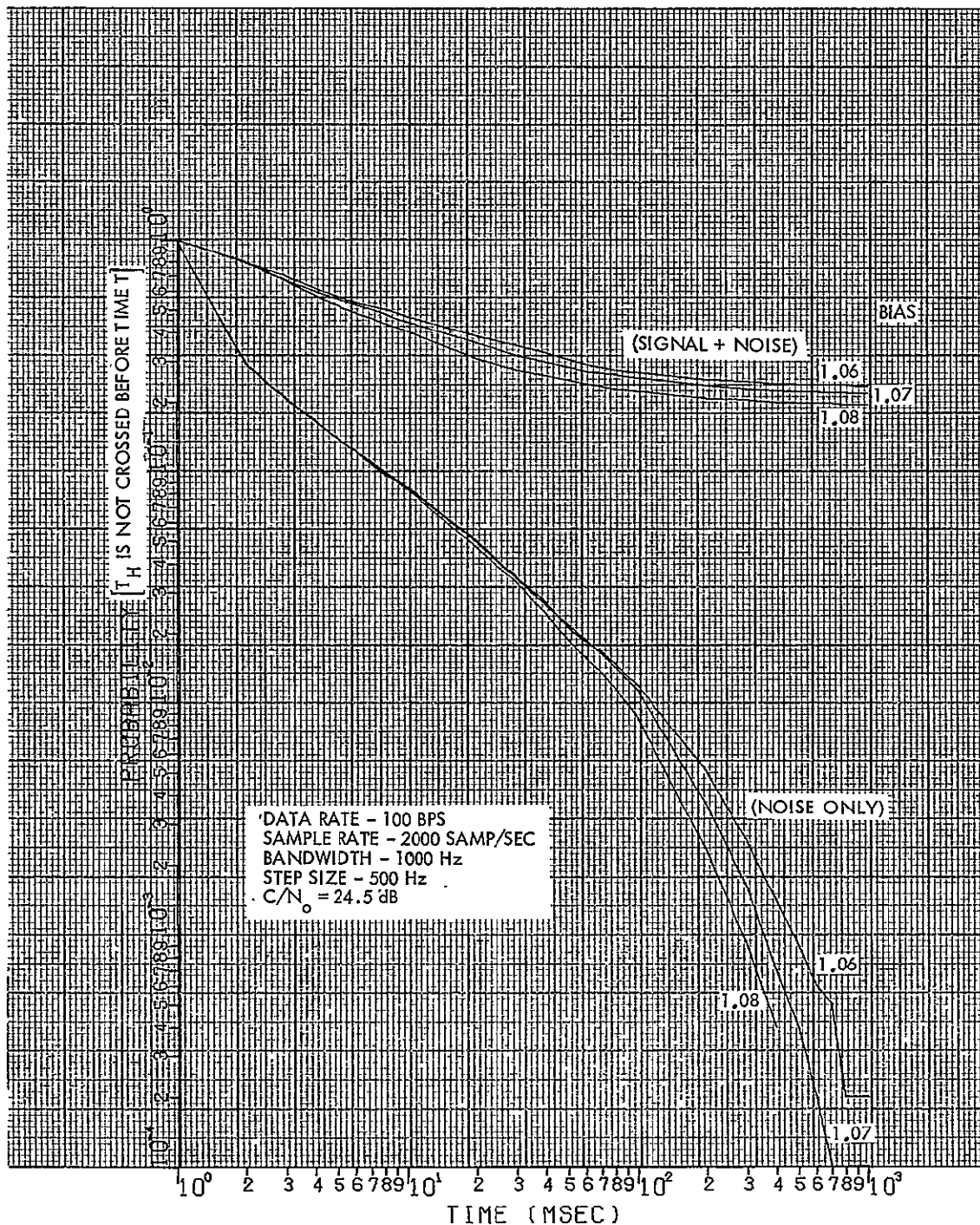


Figure 3-9. Probability Distribution of Threshold Crossing Time as a Function of Bias

is increased. This result enables the selection of the truncation time long enough to reduce the false alarm rate to the desired level without materially affecting the probability of detection.

It also appears from the curves that the algorithm performance is not sensitive to small changes in the bias. Changes of a percentage point result in small though discernible changes in the probability of detection and the distribution of dismissal times. The effect of changes in the bias can more readily be evaluated if the data is presented in another form. Using the method described in the previous section, the time required to acquire the signal with a given probability was computed. Three

probability values were selected, 0.5, 0.9, and 0.995. The results are plotted in Figure 3-10 as a function of bias. The results show nearly identical performance for bias levels ranging from 1.06 and 1.09. The acquisition time is approximately 45 sec. for a probability of detection of 0.995. This is within the 50 sec. requirement at the lowest SNR. As the bias is increased above 1.1, the acquisition time increases.

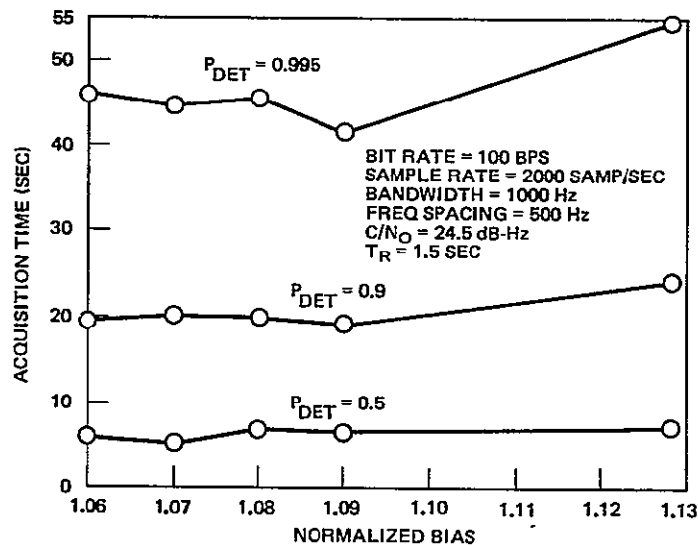


Figure 3-10. Acquisition Time vs Bias

Figures 3-11 and 3-12 show the equivalent simulation results to those shown in Figures 3-9 and 3-10 except that the integration filter bandwidth has been reduced to 800 Hz and the frequency step is 400 Hz.

Several other values for integration bandwidth were used in the simulation to evaluate their effect. Figure 3-13 shows a plot of the acquisition time, as a function of integration filter bandwidth for various values of probability of detection. In each case, the optimum bias setting is assumed. As can be seen, the optimum choice of bandwidth is 800-1000 Hz. As the bandwidth is increased, the number of cells to be searched decreases but the SNR in the integration filter bandwidth also decreases and the net effect is a longer acquisition time. Conversely, as the integration filter is narrowed, the SNR and the number of cells increases, but two effects result in a longer acquisition time. First, the number of cells to be searched increases directly, and second, the filter transient response time becomes important. That is, as the filter bandwidth is made narrower, the response time of the filter becomes a significant fraction of the time required to dismiss an empty frequency cell, thus resulting in a longer acquisition time.

Simulation results were also obtained for the case where the input bit rate is 1000 bps. At a  $C/N_0$  of 34.5 dB, simulation results show an acquisition time of 3.23 seconds for a probability of detection of 0.995. This is considerably less than the specification requirement.

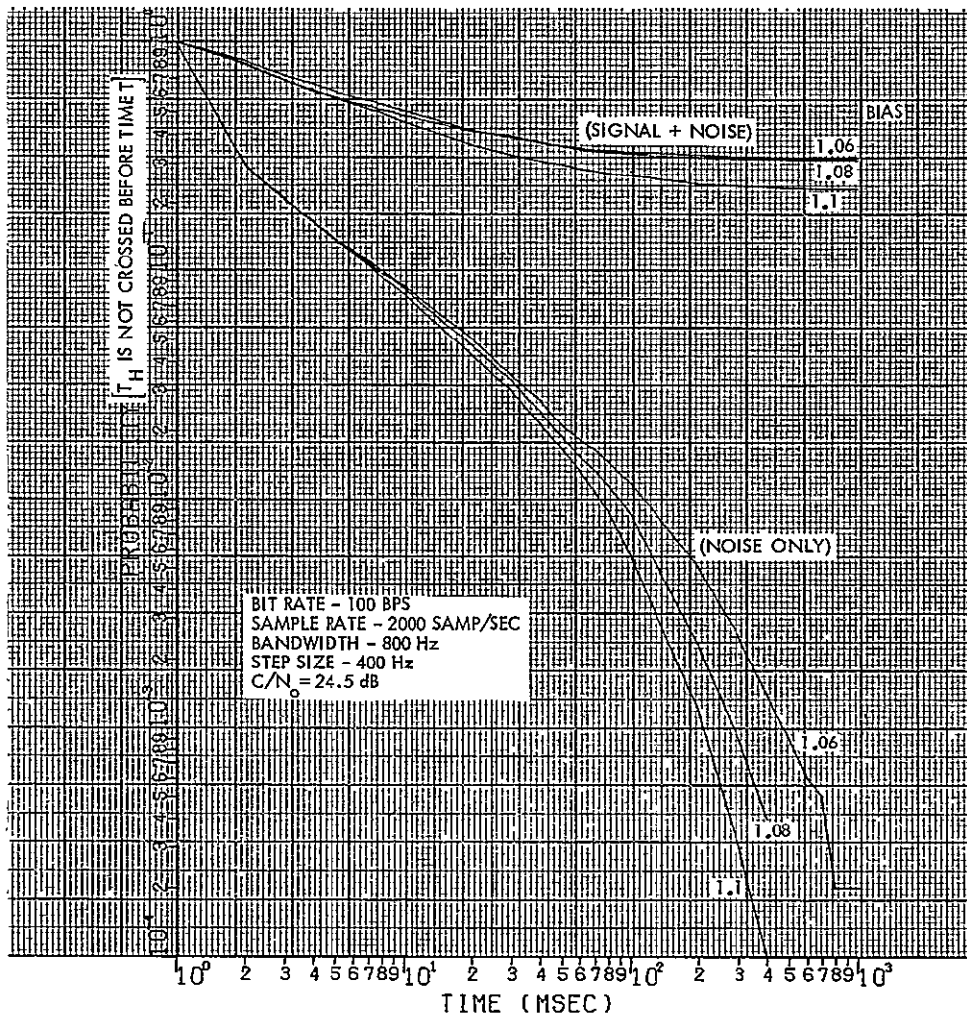


Figure 3-11. Probability Distribution of Threshold Crossing Time for Integration Bandwidth of 800 Hz

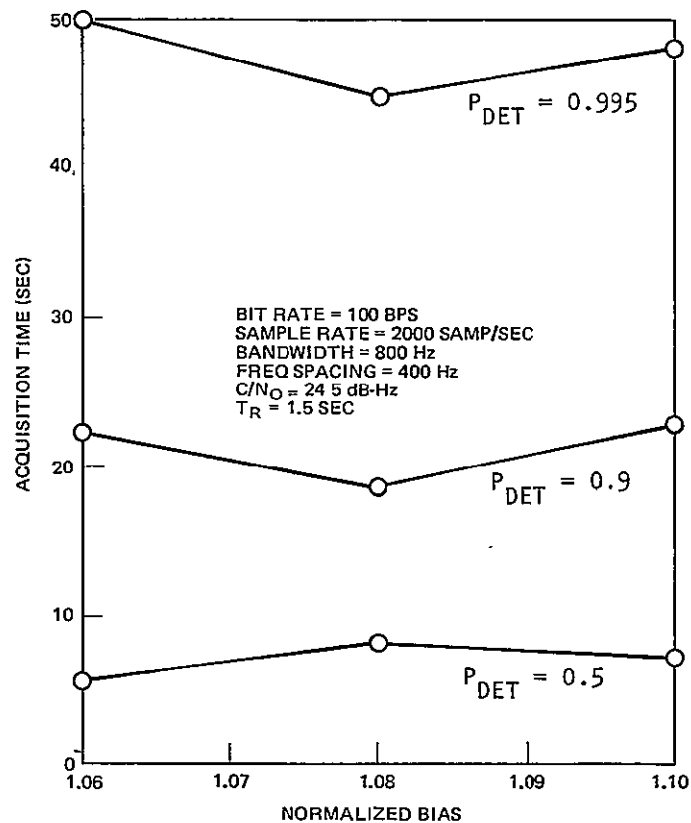


Figure 3-12. Acquisition Time vs Bias

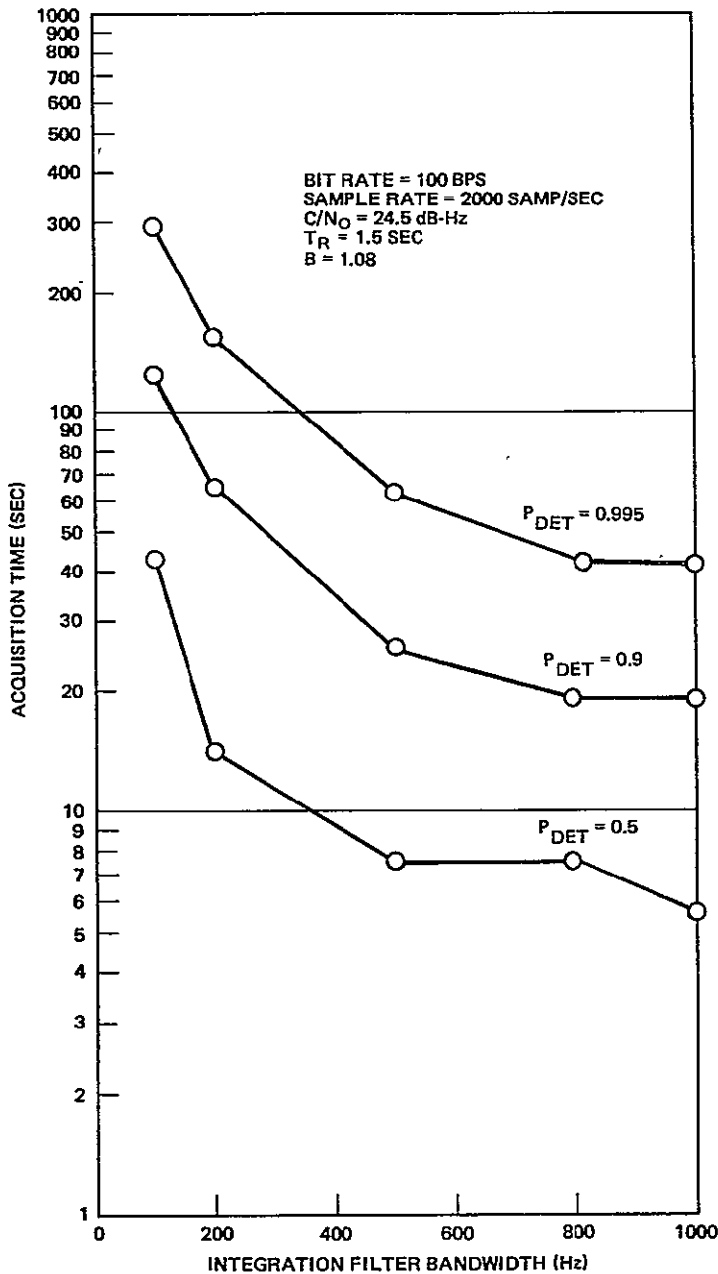


Figure 3-13. Acquisition Time vs Bandwidth

Full Scale Monte Carlo Simulation

A third simulation program was written to perform a full scale Monte Carlo simulation of the acquisition algorithm. As described previously, the results of the second simulation program derived from a combination of analysis and simulation. The third simulation program is a more complete simulation. In it, the search algorithm is implemented in detail, covering the full uncertainty region of 160 kHz in steps. The signal is located randomly in the uncertainty region and statistics are kept on the time of detection over many trials. Because of the large amounts of computer time required to run this program, the simplified program described earlier was used to

optimize the algorithm parameters. To validate the results further, however, the full scale simulation was run with the optimum set of parameters. Figure 3-14 shows a plot of the probability of detection as a function of time for the case in which the input bit rate is 100 bps, the sampling rate is 2000 samples/sec., the integration filter bandwidth is 1000 Hz, the frequency step size is 500 Hz, the  $C/N_0$  is 24.5 dB, and the bias is 1.08. As can be seen, the acquisition time for a 0.995 probability of detection is approximately 40 sec. This coincides quite well with the results shown in Figure 3-10 which show an acquisition time of approximately 46 sec. for the same choice of parameters. The median acquisition time is approximately 6.5 sec. which again coincides well with the median value shown in Figure 3-10 of 7 sec. Based on these results, an integration bandwidth of 1000 Hz is recommended for all data rates from 100 bps up to 1000 bps. The performance is near optimum and the fixed bandwidth simplifies the firmware.

### 3.2 TRACKING ALGORITHMS FOR DPSK AND FSK

As shown in the last section, the sequential acquisition algorithm determines the center frequency of the received signal to within the  $\pm 1$  kHz of the true signal frequency. Before the data can be demodulated with any confidence, however, bit synchronization (symbol sync) and frequency tracking must be obtained. There are basically two schools of thought on data-derived symbol synchronization and frequency tracking. One school seeks to obtain time synchronization and tracking independently of the data symbol sequence. The other uses the demodulated data to aid in the tracking. Approaches belonging to the latter, known as decision directed (feedback) techniques, generally outperform unaided tracking techniques provided that the data demodulation can be performed with less than approximately a 10% error rate.

The approach taken in the hybrid receiver program is to initially track frequency and bit timing independently of data feedback until frequency and timing errors are within the pull-in range of the decision directed FLL and bit synchronizer loops, that is, until the errors are small enough so that demodulation can take place reliably. In the following sections, the coarse frequency tracking and coarse timing algorithms are described for both DPSK and FSK data. Section 3.3 discusses the associated demodulation algorithms and the decision directed tracking loops.

#### 3.2.1 Coarse Frequency Tracking Algorithms

Without bit timing and decision feedback, it is not possible to filter the input signal down to the data bandwidth to maximize the SNR into the frequency discriminator without distorting the input signal.

The predetection lowpass filter must therefore be widened to encompass the frequency uncertainty in the signal. At low signal levels, the additional noise forces operation in the nonlinear range of the discriminator characteristic, where the click noise phenomenon is a factor. The approach taken in the hybrid receiver is to operate

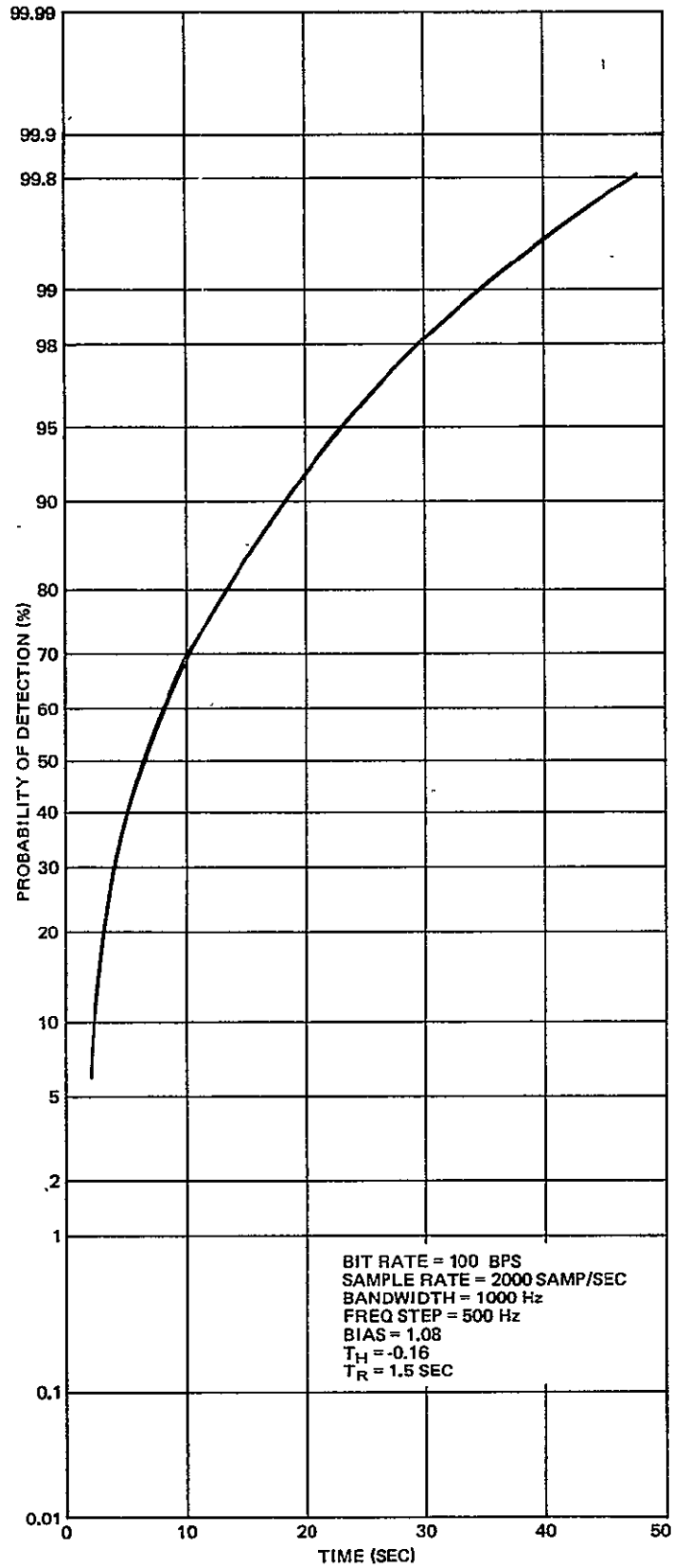


Figure 3-14. Probability of Detection vs Time

the frequency discriminator at a high rate and utilize post-detection integration to reduce the variance in the frequency estimate.

### Coarse Frequency Tracking for DPSK

The coarse frequency tracking loop features a digital discriminator based on the following algorithm.

$$\begin{aligned}
 F_K &= Q_K I_{K-1} - I_K Q_{K-1} = A_K A_{K-1} \left[ \sin \theta_K \cos \theta_{K-1} - \cos \theta_K \sin \theta_{K-1} \right] \\
 &= A_K A_{K-1} \sin(\theta_K - \theta_{K-1}) \\
 &= A_K A_{K-1} \sin(\Delta \theta_K)
 \end{aligned}$$

where

- $I_K$  =  $K^{\text{th}}$  sample of the inphase lowpass component of the signal
- $Q_K$  =  $K^{\text{th}}$  sample of the quadrature lowpass component of the signal
- $A_K$  = amplitude of signal component for the  $K^{\text{th}}$  sample
- $\theta_K$  = signal phase

If the sampling rate is large enough that the change in phase  $\theta_K$  is small ( $\Delta \theta_K < 0.4$  radians), then  $\sin(\Delta \theta_K) \approx \Delta \theta_K \approx \dot{\theta}_K$ .

With this algorithm, the true derivative of  $\theta(t)$  is approximated by the sin of a first difference. This  $\sin(x)$  discriminator characteristic is shown in Figure 3-15. The frequency pull-in range is  $\pm f_s/2$  Hz, where  $f_s$  is the sampling rate. From the

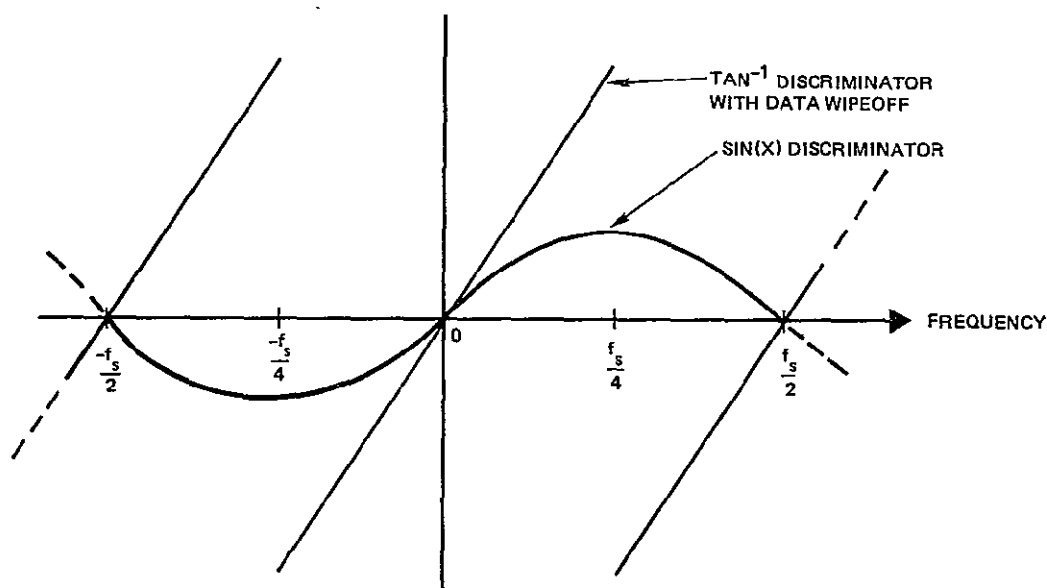


Figure 3-15.  $\sin(x)$  and  $\tan^{-1}$  Discriminator Characteristics with Data Wipeoff



sampling theorem, the discriminator characteristic will be periodic in  $f_s$  Hz intervals and therefore the discriminator must be operated at a sample rate at least twice the largest (possible) frequency offset.

For DPSK data, the  $\sin(x)$  discriminator automatically wipes off the biphase modulation, regenerating the suppressed carrier for tracking. This is true for all samples except those at data bit transitions. At a bit transition,  $\theta_K = \theta_{K-1} + \omega_0 T_s + \pi$  where  $\omega_0$  is the radian carrier frequency and  $T_s$  the sampling interval. Therefore

$$\begin{aligned} Q_K I_{K-1} - I_K Q_{K-1} &= A_K A_{K-1} \sin(\theta_K - \theta_{K-1}) \\ &= A_K A_{K-1} \sin(\omega_0 T_s + \pi) \\ &= -A_K A_{K-1} \sin(\omega_0 T_s) \\ &\approx -A_K A_{K-1} \omega_0 T_s \end{aligned}$$

Elsewhere,  $\theta_K = \theta_{K-1} + \omega_0 T_s$  and so

$$\begin{aligned} Q_K I_{K-1} - I_K Q_{K-1} &= A_K A_{K-1} \sin(\omega_0 T_s) \\ &\approx A_K A_{K-1} \omega_0 T_s \end{aligned} \tag{3.1}$$

The  $\sin(x)$  discriminator produces a signal proportional to the frequency offset  $\omega_0$  (for small offsets) except for samples occurring at the data bit transitions, where the sign of the error signal is reversed. However, since the discriminator is operated at several times the data rate (typically at 8 kHz), the relative frequency of occurrence of this sign reversal is small (one out of 16 on the average at 1000 bits/sec data rate) and it therefore has minimal effect on the coarse frequency tracking algorithm.

An alternative discriminator implementation makes use of the arctangent operation and results in a linear error characteristic (see Figure 3-15).

$$\begin{aligned} 2\dot{\theta}_K \approx 2(\theta_K - \theta_{K-1}) &= \left[ 2 \left( \tan^{-1} \left[ \frac{Q_K}{I_K} \right] - \tan^{-1} \left[ \frac{Q_{K-1}}{I_{K-1}} \right] \right) \right]_{\text{MOD } 2\pi} \\ &= 2 \omega_0 T_s \end{aligned}$$

The factor of 2 in the equation above wipes off the biphase modulation. It also, however, has the disadvantage of reducing the pull-in range by a factor of 2. If both the  $\sin(x)$  and  $\tan^{-1}$  discriminator are operated at the same rate, their closed loop performance are nearly the same (except for pull-in range). The  $\sin(x)$  discriminator was chosen for the

hybrid receiver program since it is more computationally efficient, eliminating the need for a division ( $Q_K/I_K$ ) and the requirement to resolve a  $2\pi$  ambiguity in the change in phase ( $\tan^{-1} [Q_K/I_K] - \tan^{-1} [Q_{K-1}/I_{K-1}]$ ). In addition, its wider pull-in range minimizes the possibility of locking onto a signal sidelobe rather than the main lobe.

The output of the  $\sin(x)$  discriminator is averaged in a lowpass filter and the result used to generate a tuning command to a numerically controlled oscillator (NCO). The frequency tracking loop analytical model is shown in Figure 3-16, and its equivalent loop (baseband) model in Figure 3-17. In order to track a frequency ramp with zero steady state error, the loop filter  $F(s)$  must be at least second order, for example, of the form

$$F(s) = \frac{a}{s} + \frac{b}{s^2}$$

where  $s$  is the Laplacian operator. The equivalent digital loop filter is obtained by performing the transformation  $\frac{1}{s} \rightarrow \frac{1}{1-Z^{-1}}$ , where a pure integrator is replaced by a running sum ( $Z$  is the  $Z$ -transform operator)

$$F(Z) = \frac{1}{1-Z^{-1}} \left( a + \frac{b}{1-Z^{-1}} \right)$$

The block diagram of the digital FLL for the coarse frequency tracking of DPSK data is shown in Figure 3-18.

#### Coarse Frequency Tracking for FSK

Frequency tracking for continuous phase frequency shift keying (CPFSK) is identical to that used for DPSK. CPFSK refers to an FSK modulation scheme in which the phase is constrained to be continuous during a bit transition. The signal is constructed such that the two signal frequencies are located  $\omega_s/2\pi$  Hz away from the carrier,

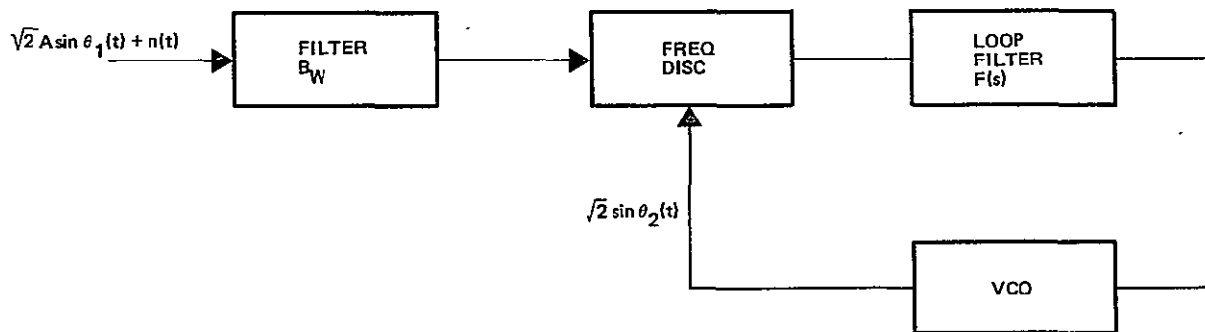
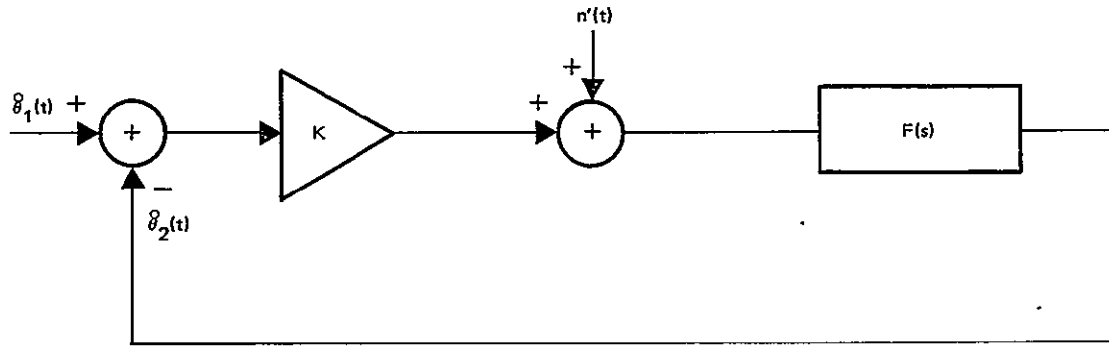


Figure 3-16. Frequency Tracking Loop Analytical Model



LOOP EQUATION:  $\frac{d\psi}{dt} = \frac{d\theta_1}{dt} - \frac{d\theta_2}{dt} = \frac{d\theta_1}{dt} - \int_0^t f(t-u) [K \frac{d\psi(u)}{du} + n'(u)] du$

Figure 3-17. Frequency Tracking Equivalent Loop Model

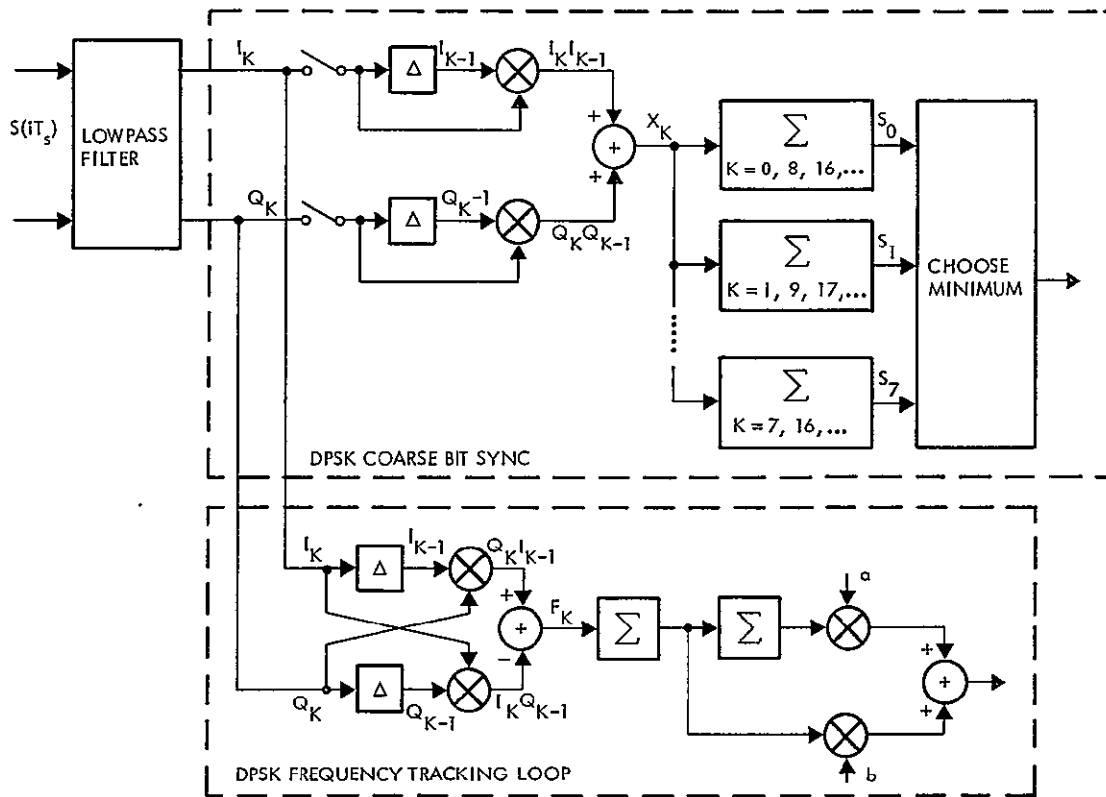


Figure 3-18. Coarse Bit Sync and Coarse Frequency Tracking for DPSK Data

where  $\omega_s = h/\pi T_B$ ;  $h$  is the deviation ratio, and  $T_B$  the data bit duration. In particular, the lowpass inphase and quadrature components of the CPFSK signal are given by

$$I_k = A_k \cos(\phi_k)$$

$$Q_k = A_k \sin(\phi_k)$$

where the signal phase  $\phi_k$  is defined by the recursive definition

$$\phi_k = \phi_{k-1} + (d_k \omega_s + \omega_0) T_s \quad (3.2)$$

for

$\omega_0$  = carrier radian frequency offset

$\omega_s$  = radian frequency separation between signal frequencies and carrier

$d_k$  = information data bit ( $\pm 1$ )

$T_s$  = sampling interval

$A_k$  = signal amplitude

The  $\sin(x)$  discriminator output for a CPFSK signal is therefore given by

$$\begin{aligned} F_k &= Q_k I_{k-1} - I_k Q_{k-1} \\ &= A_k A_{k-1} \sin[(d_k \omega_s + \omega_0) T_s] \end{aligned} \quad (3.3)$$

For small carrier offsets  $\cos(\omega_0 T_s) \approx 1$  and  $\sin(\omega_0 T_s) \approx \omega_0 T_s$ , and therefore

$$\begin{aligned} F_k &= A_k A_{k-1} [\sin(d_k \omega_s T_s) \cos(\omega_0 T_s) + \cos(d_k \omega_s T_s) \sin(\omega_0 T_s)] \\ &\approx A_k A_{k-1} d_k \sin(\omega_s T_s) + [A_k A_{k-1} \cos(\omega_s T_s)] \omega_0 T_s \end{aligned}$$

Since  $F_k$  is averaged through the lowpass FLL filter, for random data (probability of  $d_k = 1$  equals probability of  $d_k = -1$ ) the first term in the equation above goes to zero. The closed frequency tracking loop therefore will track the average value of  $F_k$ , the suppressed carrier midway between the two FSK signal frequencies

$$\langle F_k \rangle \approx [A_k A_{k-1} \cos(\omega_s T_s)] \omega_0 T_s$$

A block diagram of the FSK tracking loop for coarse frequency tracking is shown in Figure 3-19.

### 3.2.2 Coarse Bit Timing Algorithms

Coarse bit timing is obtained independently of the data symbol sequence (that is, no data feedback is used). However, since sync is derived from the transmitted data, some minimum number of transitions in the data sequence is necessary before sync can be obtained successfully. This is because sync information is derived from changes in phase (for DPSK) or frequency (in FSK) which occur only at bit transitions. Again, the approach taken in the hybrid receiver was to incorporate similar algorithms for the different signal modulation formats for computational efficiency.

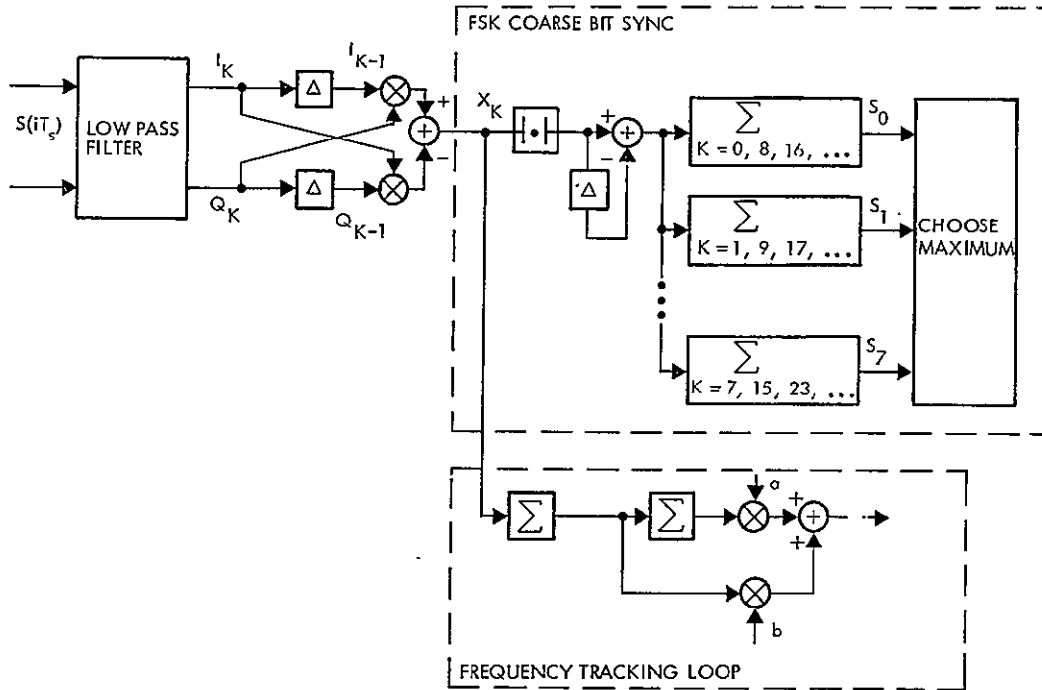


Figure 3-19. Coarse Bit Sync and Coarse Frequency Tracking for FSK Data

#### Coarse Bit Timing for DPSK

In differential encoding, information to be transmitted is represented in terms of changes between successive data symbols rather than the symbols itself. Let  $s_i(t) = A \sin(\omega_0 t + \phi_i)$  represent the signal transmitted in the  $i^{\text{th}}$  transmission interval  $(i-1)T_B \leq t \leq iT_B$ . For DPSK, the signal phase in the  $i^{\text{th}}$  interval is related to the phase in the previous interval by  $\phi_i = \phi_{i-1}$  or  $\phi_i = \phi_{i-1} + \pi$  depending on whether there is a data bit transition.

The received inphase and quadrature lowpass sampled signals are given by

$$\begin{aligned}
 I_K &= A_K \cos(\omega_0 K T_s + \phi_K) \\
 Q_K &= A_K \sin(\omega_0 K T_s + \phi_K)
 \end{aligned}
 \tag{3.4}$$

where

- $\phi_K$  = signal phase
- $\omega_0$  = signal frequency offset
- $A_K$  = signal amplitude
- $T_s$  = sampling interval

Suppose the computation  $X_K = I_K I_{K-1} + Q_K Q_{K-1}$  is performed. Then from (3.4)

$$X_K = A_K A_{K-1} \cos(\omega_0 K T_s + \phi_K) \cos(\omega_0 (K-1) T_s + \phi_{K-1}) \\ + A_K A_{K-1} \sin(\omega_0 K T_s + \phi_K) \sin(\omega_0 (K-1) T_s + \phi_{K-1})$$

$$X_K = A_K A_{K-1} \cos(\omega_0 T + \phi_K - \phi_{K-1}) \quad (3.5)$$

Since the data has been differentially phase encoded,  $\phi_K \neq \phi_{K-1}$  only when samples  $K$  and  $K-1$  straddle a bit transition. This is shown in Figure 3-20 (for  $\omega_0 = 0$ ). If the amplitude of the received signal is slowly varying ( $A_K = A_{K-1} = A$ ) then the average signal component of  $X_K$  will be given by

$$\langle X_K \rangle = \begin{cases} -A^2 \cos(\omega_0 T_s) & \text{At bit transitions} \\ A^2 \cos(\omega_0 T_s) & \text{Elsewhere} \end{cases}$$

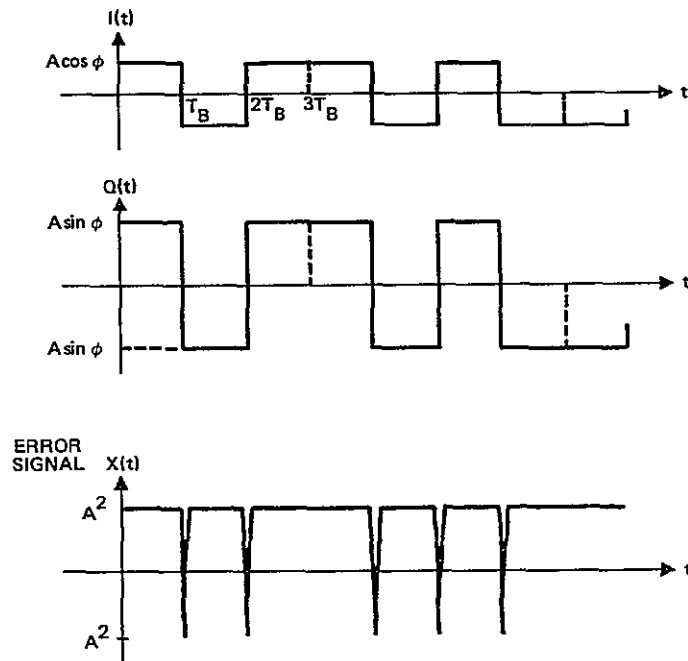


Figure 3-20. Coarse Bit Timing Example for DPSK Data

Where  $\langle \cdot \rangle$  is the expectation operator. For small frequency tracking errors,  $\cos(\omega_0 T) \approx 1$  and coarse bit timing can therefore be obtained by averaging corresponding values of  $X_k$  sampled at multiples of the bit rate. A block diagram of the coarse sync algorithm for DPSK is shown in Figure 3-18. For coarse timing accurate to 1/16th the bit interval  $T_B$  (degradation of  $\approx 0.6$  dB), eight summers are used, where the sampling interval  $T = T_B/8$ . For example, at the 1000 bps data rate ( $T_B = 1$  msec),  $X_k$  (and therefore  $I_k$  and  $Q_k$ ) should be sampled at an 8 kHz rate. The register with the smallest output corresponds to the sample time closest to a bit transition. Note that since, on average, half as many 0's as 1's are transmitted, then

$$\langle S_k \rangle = \begin{cases} 0 & \text{At bit transitions} \\ A^2 N \cos(\omega_0 T_s) & \text{Elsewhere} \end{cases}$$

where  $N$  is the number of bit intervals over which the sums  $S_k$  are computed.  $N$  should therefore be chosen such that the sum  $S_k$  corresponding to the true sync position (that is, that  $S_k = \min S_0, S_1, \dots, S_7$ ) is chosen with high probability. An approximate formula for the probability of selecting the true coarse sync position is given by

$$P_{\text{sync}} \approx \left[ 1 - \text{ERFC} \left( \frac{C}{N_0} \frac{\sqrt{N/2} \cos(\omega_0 T_s)}{2T_B \sqrt{1 + \frac{C}{N_0 T_B}}} \right) \right]^7$$

where

$C/N_0$  = carrier-to-noise density

$N$  = number of bits

$T_B$  = bit time interval

$T_s$  = sampling interval ( $= T_b/8$ )

$\omega_0$  = FLL tracking error

and  $\text{ERFC}(x)$ , the complementary error function is given by

$$\text{ERFC}(x) = \int_x^{\infty} \frac{1}{\sqrt{2\pi}} \exp(-y^2/2) dy$$

$P_{\text{sync}}$  is plotted in Figure 3-21 for a carrier-to-noise density ratio of 24.5 dB at the 100 bps data rate (or proportionately larger at the higher data rates) for static frequency tracking errors equal to 0 Hz, half the data rate ( $\omega_0 T_B = \pi$ ), and the data rate ( $\omega_0 T_B = 2\pi$ ). A suitable value for  $N$  is 50 bits. Simulation results have indicated that coarse timing sync will typically be obtained before fine frequency acquisition.

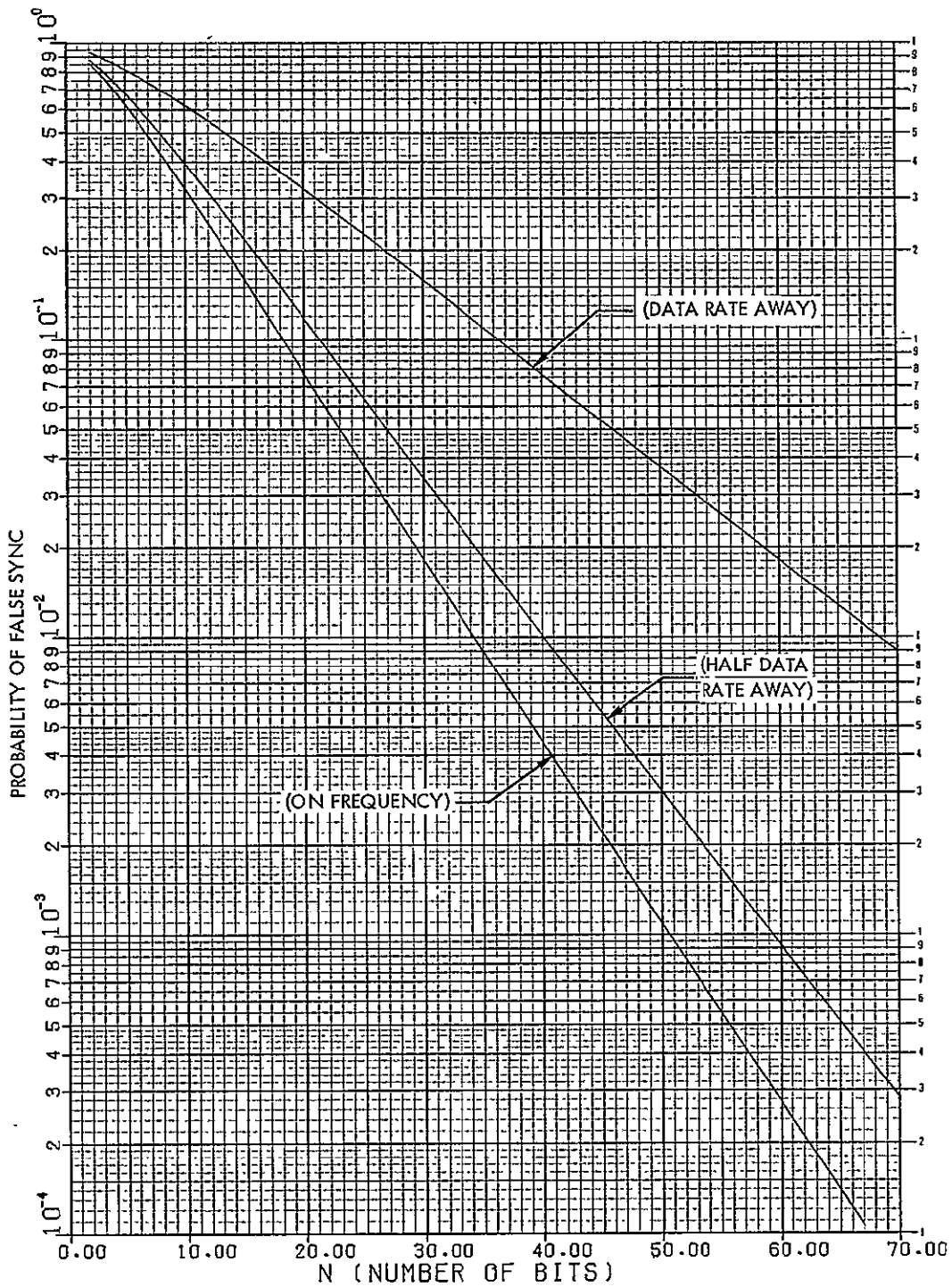


Figure 3-21. Probability of False Sync as a Function of Carrier Frequency Offset

#### Coarse Bit Timing for FSK

The coarse bit timing algorithm is similar to that for DPSK except that timing is derived from the discriminator output. Again assuming that the modulation is CPFSK, from (3.3), the discriminator output is

$$F_k = A_k A_{k-1} \sin [(d_k \omega_s + \omega_0) T_s]$$



Since  $F_k$  is an NRZ signal, coarse bit timing can be obtained by differentiating  $F_k$ . Approximating the ideal differentiator by a first difference

$$X_k = F_k - F_{k-1}$$

$$X_k = \begin{cases} 0 & \text{No transition} \\ A_k A_{k-1} d_k ([\sin(-\omega_s + \omega_0)]T_s - \sin[(\omega_s + \omega_0)T_s]) & \text{Bit transition} \end{cases}$$

$d_k = d_{k-1}$   
 $d_k = d_{k-1}$

$X_k$  is nonzero only at bit transitions. Therefore, bit timing is obtained by averaging corresponding values of  $X_k$  sampled at the data rate. This coarse timing algorithm is shown in Figure 3-19. The coarse sync algorithm consists of forming  $L$  running sums each offset by a sample time  $T_s$  from the previous

$$S_\ell = \sum_{n=0}^{N-1} |X(\ell T_s + nT_B)| \quad \text{for } \ell = 0, 1, \dots, L$$

where  $L$  equals the number of samples in a data bit duration  $T_B$ , and  $N$  the number of bit intervals in the running sums. A suitable value for  $N$  is 50 bits, which corresponds to 0.5 sec for the 100 bps data rate. Unlike the DPSK algorithm, the correct coarse sync position is taken to be that which corresponds to the largest sum  $S_\ell$  rather than the smallest.

### 3.3 DEMODULATION ALGORITHMS

Once coarse frequency and bit timing have been acquired, data demodulation can take place. The selected demodulation algorithms were chosen to minimize processing complexity. Once demodulation begins, the detected data is used to improve frequency tracking and bit timing performance. Those decision directed algorithms are also described in this section.

#### 3.3.1 DPSK Demodulation and Decision Directed Tracking

The DPSK demodulation algorithm is shown in Figure 3-22. The filtered inphase and quadrature inputs are integrated for a bit time and the differential phase between successive bit samples obtained by performing the operation

$$X(KT_B) = I(KT_B)I((K-1)T_B) + Q(KT_B)Q((K-1)T_B)$$

where

$I(KT_B)$  = inphase lowpass component of the signal at time  $kT_B$

$Q(KT_B)$  = quadrature lowpass component of the signal at time  $kT_B$

$T_B$  = data bit duration

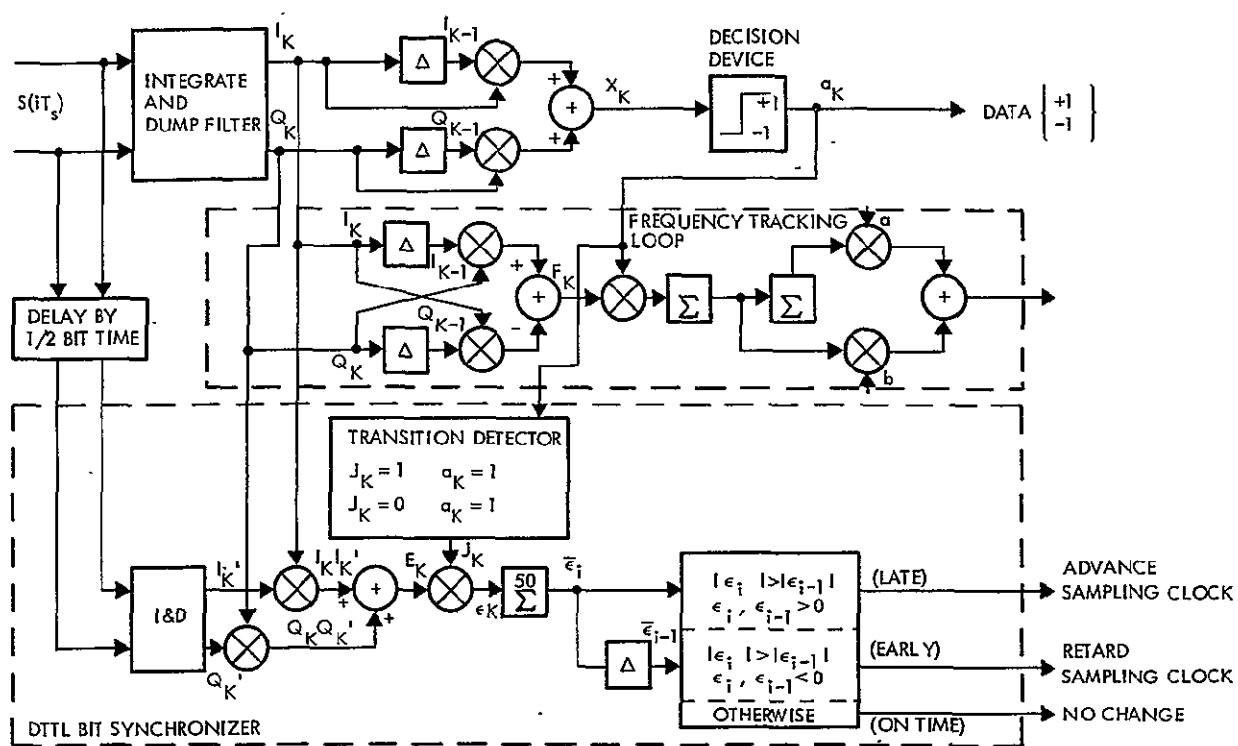


Figure 3-22. Decision Directed Tracking and Demodulation of DPSK Data

Substituting  $I(KT_B) = A_K \cos(\omega_0 KT_B + d_K)$  and  $Q_K = A_K \sin(\omega_0 KT_B + d_K)$

$$X(KT_B) = A_K A_{K-1} \cos[(d_K - d_{K-1}) + \omega_0 T_B]$$

where  $A_K$  and  $d_K$  are the signal amplitude and phase for the  $K^{\text{th}}$  data bit respectively, and  $\omega_0$  the frequency tracking error (assumed to be static across a bit time). For small tracking errors ( $\omega_0 T_B \approx 0$ )

$$X_K = \begin{cases} A_K A_{K-1} & \text{for } d_K = d_{K-1} \\ -A_K A_{K-1} & \text{for } d_K = d_{K-1} + \pi \end{cases}$$

The differential phase between successive bit samples is obtained by passing  $X_K$  through a threshold device (a sign detector).

An AFC correction signal is derived by performing the computation

$$\begin{aligned} F_K &= Q(KT_B)I((K-1)T_B) - I(KT_B)Q((K-1)T_B) \\ &= A_K A_{K-1} \sin[(d_K - d_{K-1}) + \omega_0 T_B] \\ &\approx A_K A_{K-1} \sin(\omega_0 T_B) \quad \text{for } d_K = d_{K-1} \\ &\approx -A_K A_{K-1} \sin(\omega_0 T_B) \quad \text{for } d_K = d_{K-1} + \pi \end{aligned}$$

For small frequency errors,  $\sin(\omega_0 T_B) \approx \omega_0 T_B$ , the correction signal  $F_K$  is proportional to the carrier frequency offset. The sign of  $F_K$ , however, is dependent on the differential phase  $\phi_K = d_K - d_{K-1}$ . For proper loop operation,  $F_K$  is inverted if  $X_K < 0$ ; that is, when a bit transition is detected (see Figure 3-22). The resulting error signal is then lowpass filtered as before, and the output used to tune the NCO. Unlike the coarse frequency tracking algorithm described in Section 3.2.1 for which the uncertainty range in the carrier frequency was large, once decision directed tracking and demodulation take place reliably, the NCO command word need only be updated at the data rate (every  $T_B$  sec).

In a similar manner, it is possible to incorporate data feedback to further resolve bit timing to drive the steady state timing error to zero. This is the subject of the next section.

#### Data Transition Tracking Loop (DTTL) Bit Synchronizer for DPSK

The fine bit timing algorithm used in the hybrid receiver is a DTTL bit synchronizer shown in Figure 3-22. The input signal is processed through inphase and quadrature integrate and dump filters as before except that lowpass outputs sampled at mid-bit are also needed. A timing error signal,  $E_K$ , is derived by performing

$$E_K = I(KT_B)I(KT_B - T_B/2) + Q(KT_B)Q(KT_B - T_B/2)$$

where  $I(KT_B)$  and  $I(KT_B - T_B/2)$  are the inphase lowpass outputs sampled at the bit time and previous mid-bit, respectively.\* Then assuming that the tracking error is small, for small timing errors, the error signal can be shown to be given by

$$E_K = \begin{cases} A^2 & \text{for } d_K = d_{K-1} & \text{No bit transition} \\ 2A^2 \frac{\tau}{T_B} & \text{for } d_K = d_{K-1} + \pi & \text{Bit transition} \end{cases}$$

where  $A$  is the amplitude of the input signal and  $\tau$  the sync timing error ( $|\tau| \ll T_B$ ). At data bit transitions, an error signal is produced with amplitude proportional to the timing offset. For an early sync condition,  $\tau > 0$  and therefore  $E_K > 0$ . For late conditions,  $\tau < 0$  and  $E_K < 0$ . For proper loop operation, the timing error signal  $E_K$  is gated on only at bit transitions ( $X_K < 0$ ) and off when no transitions are detected. The resulting error signal  $\epsilon_K \triangleq E_K J_K$  ( $J_K = 1$  for  $X_K > 0$ ;  $J_K = 0$  for  $X_K < 0$ ) is digitally filtered with the resulting output used to advance (early) or retard (late) the A/D sampling clock by one sample time. A convenient digital filter which is

---

\*Computationally  $I(KT_B)$  and  $I(KT_B - T_B/2)$  can be obtained from an integrating filter with dump rate at twice the bit rate. The appropriate integrator outputs are then combined.

relatively insensitive to variations in the input amplitude signal is shown in Figure 3-22.  $\epsilon_K$  is averaged over 50 bit transitions and compared to the previous average. The A/D sampling clock is changed only if the average timing sync error is increasing. Examples of the appropriate waveforms in the loop for a typical input sequence under early and late conditions are shown in Figures 3-23 and 3-24.

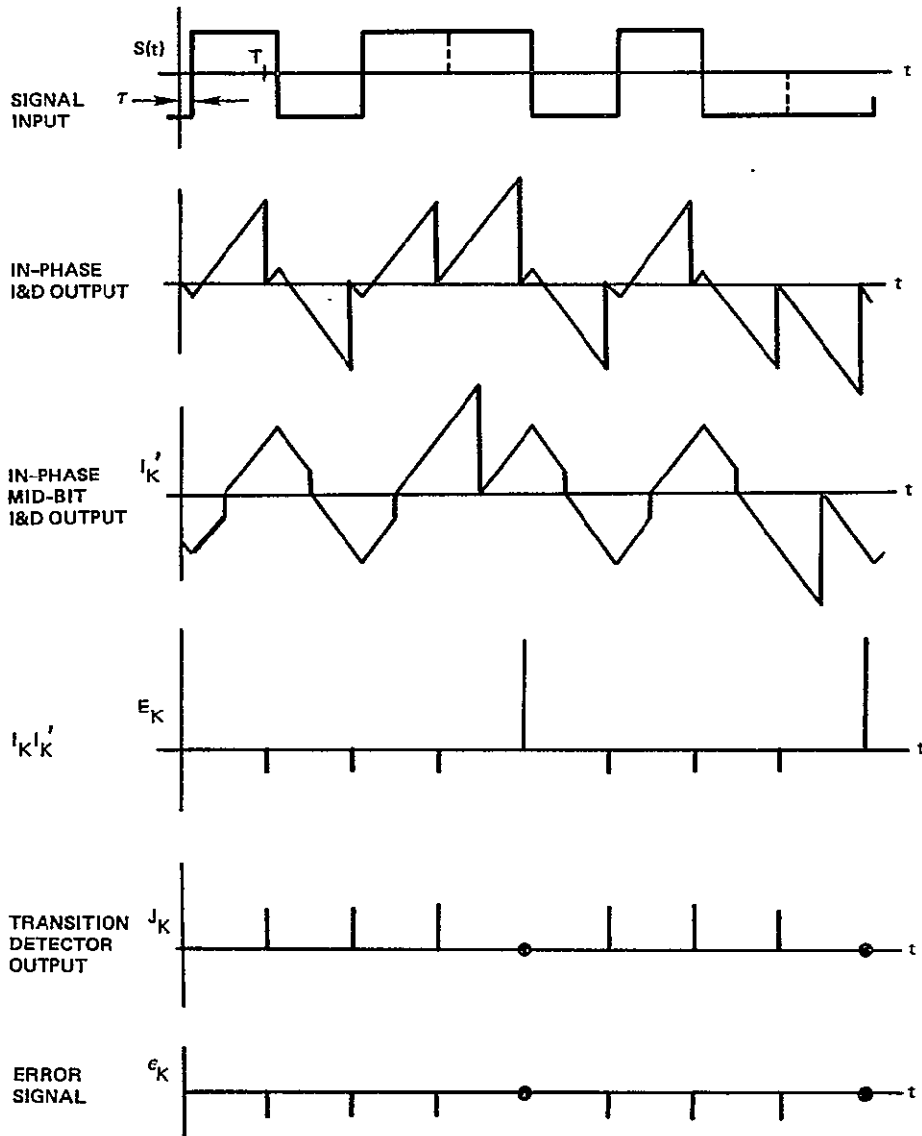


Figure 3-23. DTTL Bit Synchronization for DPSK Data. Early by  $\tau$  Seconds — Data in I-Channel

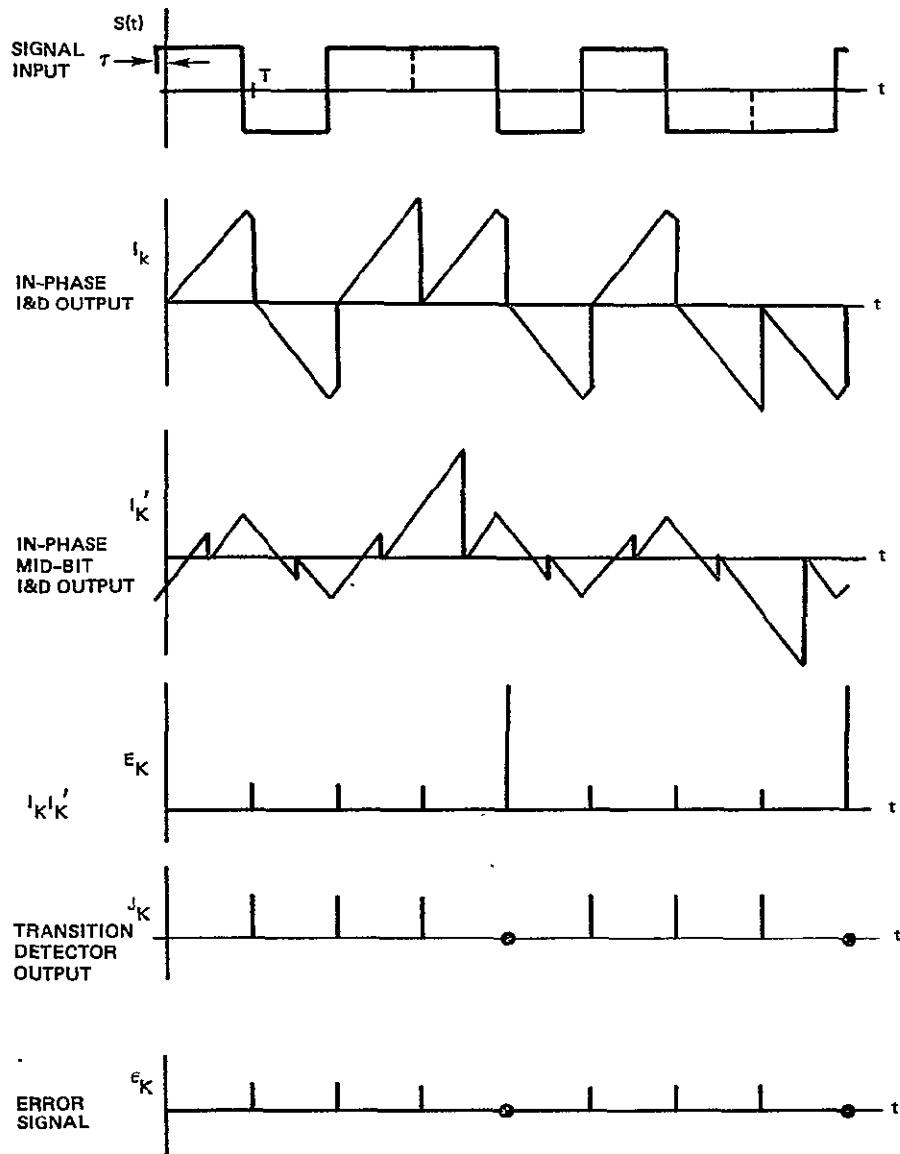


Figure 3-24. DTTL Bit Synchronization for DPSK Data.  
Late by  $\tau$  Seconds — Data in I-Channel

### 3.3.2 FSK Demodulation and Decision Directed Tracking

The demodulation algorithm of CPFSK data is shown in Figure 3-25. The signal is processed through lowpass filters wide enough to pass the signal frequencies, and frequency discriminated at the 8 kHz sampling rate. From (3.3), the discriminator output of the signal component is given by

$$\begin{aligned}
 X(kT_s) &= Q(kT_s) I((k-1)T_s) - I(kT_s) Q((k-1)T_s) \\
 &= A_k A_{k-1} \sin[(d_k \omega_s + \omega_0) T_s]
 \end{aligned}
 \tag{3.6}$$

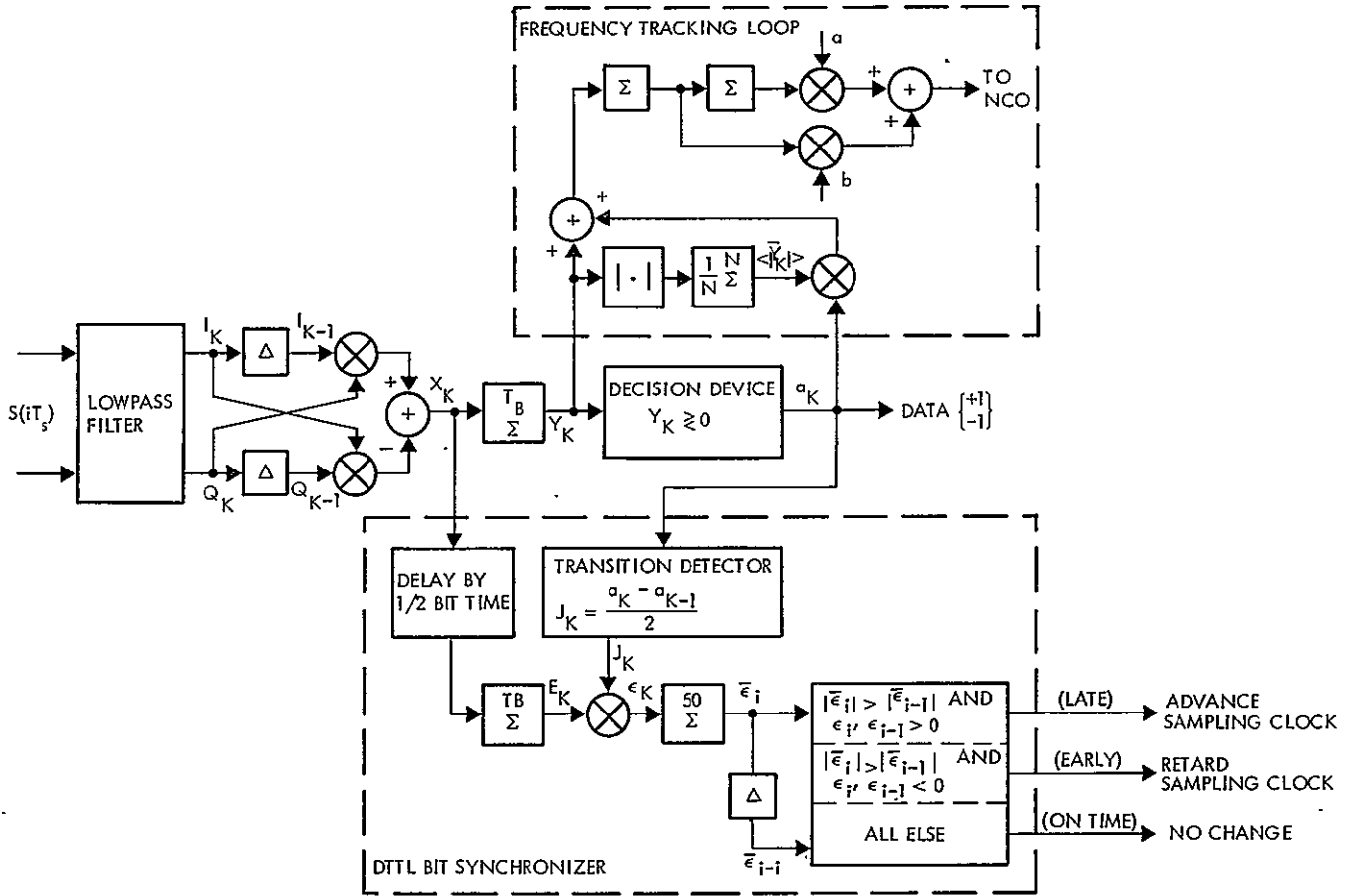


Figure 3-25. Decision Directed Tracking and Demodulation of FSK Data

For small carrier frequency offsets  $\omega_0$  with respect to the signal frequency deviations  $\omega_s$

$$X(kT_s) \approx d_k A_k A_{k-1} \sin(\omega_s T_s)$$

The information data bit  $d_k$  is detected by integrating  $X(kT_s)$  over a bit duration  $T_B$  and passing this sum  $|Y_k|$  through a threshold device (sign detector). The number of samples in the sum is given by  $T_B/T_s$ , the ratio of the bit duration to sampling interval.

An AFC signal is obtained by subtracting a bias signal from  $Y_k$  corresponding to the expected value of  $Y_k$  when the carrier offset  $\omega_0$  is zero. The appropriate frequency error signal  $F_k$  is given by

$$\begin{aligned}
F_k &= Y_k - d_k \langle |Y_k| \rangle \\
&= \left( \frac{T_B}{T_S} A_k A_{k-1} \sin[(d_k \omega_s + \omega_0) T_S] \right) - d_k \left( \frac{T_B}{T_S} A_k A_{k-1} \sin(\omega_s T_S) \right) \\
&= \frac{T_B}{T_S} A_k A_{k-1} [d_k (\sin(\omega_s T_S) \cos(\omega_0 T_S) - \sin(\omega_s T_S)) + \cos(\omega_s T_S) \sin(\omega_0 T_S)]
\end{aligned}$$

Assuming that the data bit  $d_k (\pm 1)$  is correctly demodulated and that  $\omega_0 T_S$  is small enough such that  $\cos(\omega_0 T_S) \approx 1$  and  $\sin(\omega_0 T_S) \approx \omega_0 T_S$ , then the correction signal  $F_k$  is proportional to the frequency offset  $\omega_0$ . As before,  $F_k$  is lowpass filtered and the loop filter output used to generate an NCO tuning command. In practice the signal amplitude  $A_k$  and therefore the bias signal is not known a priori. An estimate of the magnitude of the required bias can be obtained, however, by averaging  $|Y_k|$  across a number of previous bits. This is shown in Figure 3-25. The proper sign of the bias signal is obtained by feeding back the detected data symbol.

A DTTL bit synchronization algorithm is used to resolve bit timing to less than 1/16th of a bit duration. If the inphase and quadrature noise components are independent and zero mean, then from (3.6), the noise component out of the frequency discriminator will also be zero mean. Fine bit timing can be obtained by integrating the discriminator output  $X_k$  for a bit duration across bit transitions. This error signal is given by

$$\begin{aligned}
E_k &= \left( \frac{T_B}{2T_S} + \tau \right) d_{k-1} A^2 \sin(\omega_s T_S) + \left( \frac{T_B}{2T_S} - \tau \right) d_k A^2 \sin(\omega_s T_S) \\
&= \left[ \frac{T_B}{2T_S} A^2 \sin(\omega_s T_S) (d_k + d_{k-1}) \right] + \tau \left[ A^2 \sin(\omega_s T_S) (d_k - d_{k-1}) \right]
\end{aligned}$$

where

$A$  = signal amplitude (assumed to be constant)

$d_k$  = the  $k^{\text{th}}$  data information bit

$T_B$  = data bit duration

$T_S$  = sampling interval

$\omega_s$  = signal radian frequency deviation

$\tau$  = sync timing error

When the integration is performed across a bit transition ( $d_k = -d_{k-1}$ ), the first term in the equation above goes to zero, and the error signal becomes

$$E_k = \tau d_k [2A^2 \sin(\omega_s T_S)]$$

$E_k$  is proportional to the timing error  $\tau$ . For proper loop operation, the appropriate timing error signal  $\epsilon_k$  is obtained by multiplying  $E_k$  by a transition detector signal  $J_k = (a_k - a_{k-1})/2$ , where  $a_k$  is the  $k^{\text{th}}$  detected data bit. This operation ignores  $E_k$  when there is no data bit transition and determines proper sign of the error when there is a transition. Therefore, when the data bits are correctly demodulated ( $d_k = a_k, d_{k-1} = a_{k-1}$ )

$$\epsilon_k \triangleq J_k E_k = \begin{cases} 0 & \text{No transition} \\ & d_k = d_{k-1} \\ \tau[A^2 \sin(\omega_s T_s)] & \text{Bit transition} \\ & d_k = -d_{k-1} \end{cases}$$

As in the DPSK algorithm,  $\epsilon_k$  is digitally filtered with the output of the filter used to advance ( $\tau < 0$ ) or retard ( $\tau > 0$ ) the A/D sampling clock (see Figure 3-25).

#### 3.4 SIMULATION RESULTS FOR DPSK AND FSK DEMODULATION

The DPSK and FSK demodulation and tracking algorithms shown in Figures 3-22 and 3-25 were simulated on a digital computer. A 5-pole Chebyshev digital filter was designed to approximate the required analog IF filter. A typical frequency tracking response is shown in Figure 3-26 for 100 bps DPSK data with  $C/N_0$  equal to 24.5 dB-Hz and worst case doppler of 50 Hz/sec. The one-sided loop bandwidth of the FLL (3 Hz) was selected to accommodate both dynamic tracking and rms frequency errors. In Figure 3-27, a fine frequency acquisition and tracking response is shown for 1000 bps DPSK data where an initial 200 Hz carrier offset has been assumed. For this simulation, demodulation was started after 3 seconds of coarse frequency tracking, Figure 3-28 shows the response for 100 bps DPSK where an initial offset of 1000 Hz and a doppler rate of 40 Hz/sec have been assumed. Here demodulation was started after 2 seconds of coarse frequency tracking. Note that once bit timing is obtained and data directed frequency tracking starts up, the rms frequency jitter decreases substantially. A summary of the frequency tracking simulation is given in Table 3-4.

The bit error probability ( $P_e$ ) performance for ideal differentially coherent detection of differentially encoded PSK is given by

$$P_e(\text{DPSK}) = 0.5 \exp(-E_b/N_0)$$

where  $E_b/N_0$  is the energy per bit to noise density ratio. This equation is plotted in Figure 3-29. A summary of the simulation results are given in Tables 3-5 and 3-6 for 100 and 1000 bps DPSK demodulation.



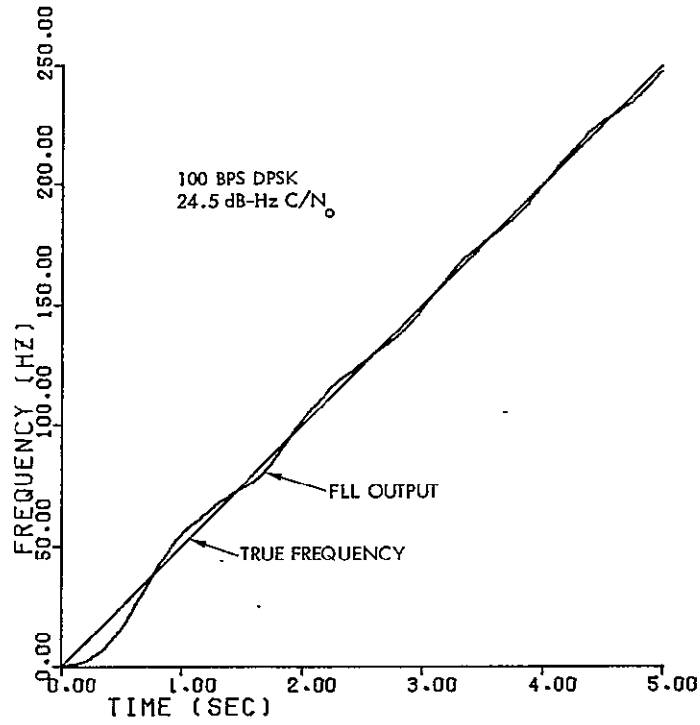


Figure 3-26. Decision Directed Frequency Tracking

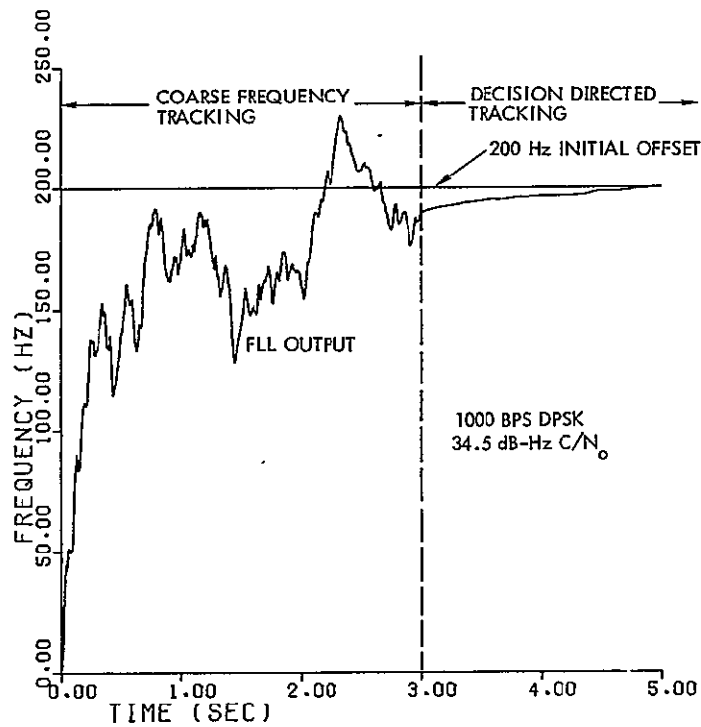


Figure 3-27. Coarse Frequency Tracking Followed by Decision Directed Tracking - 1000 bps

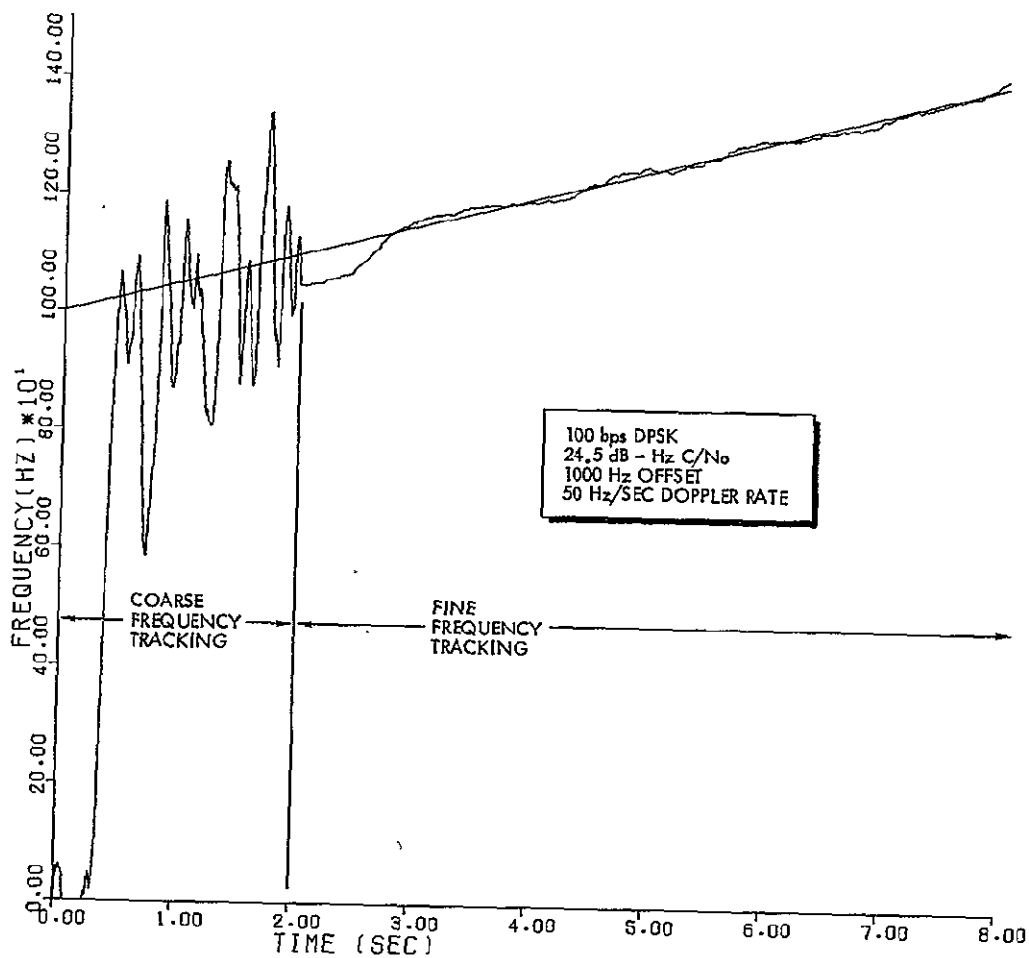


Figure 3-28. Coarse Frequency Tracking Followed by Decision Directed Tracking - 100 bps

Table 3-4. Summary of Frequency Tracking Simulation

Parameter	Data Rate	
	100 Hz	1000 Hz
$C/N_0$ operating point (dB)	24.5	34.5
One sided loop bandwidth (Hz)	3	3
RMS frequency error (Hz) at $C/N_0$ operating point	3.5	4.5
RMS frequency error (Hz) at 20 dB above $C/N_0$ operating point	0.2	0.2

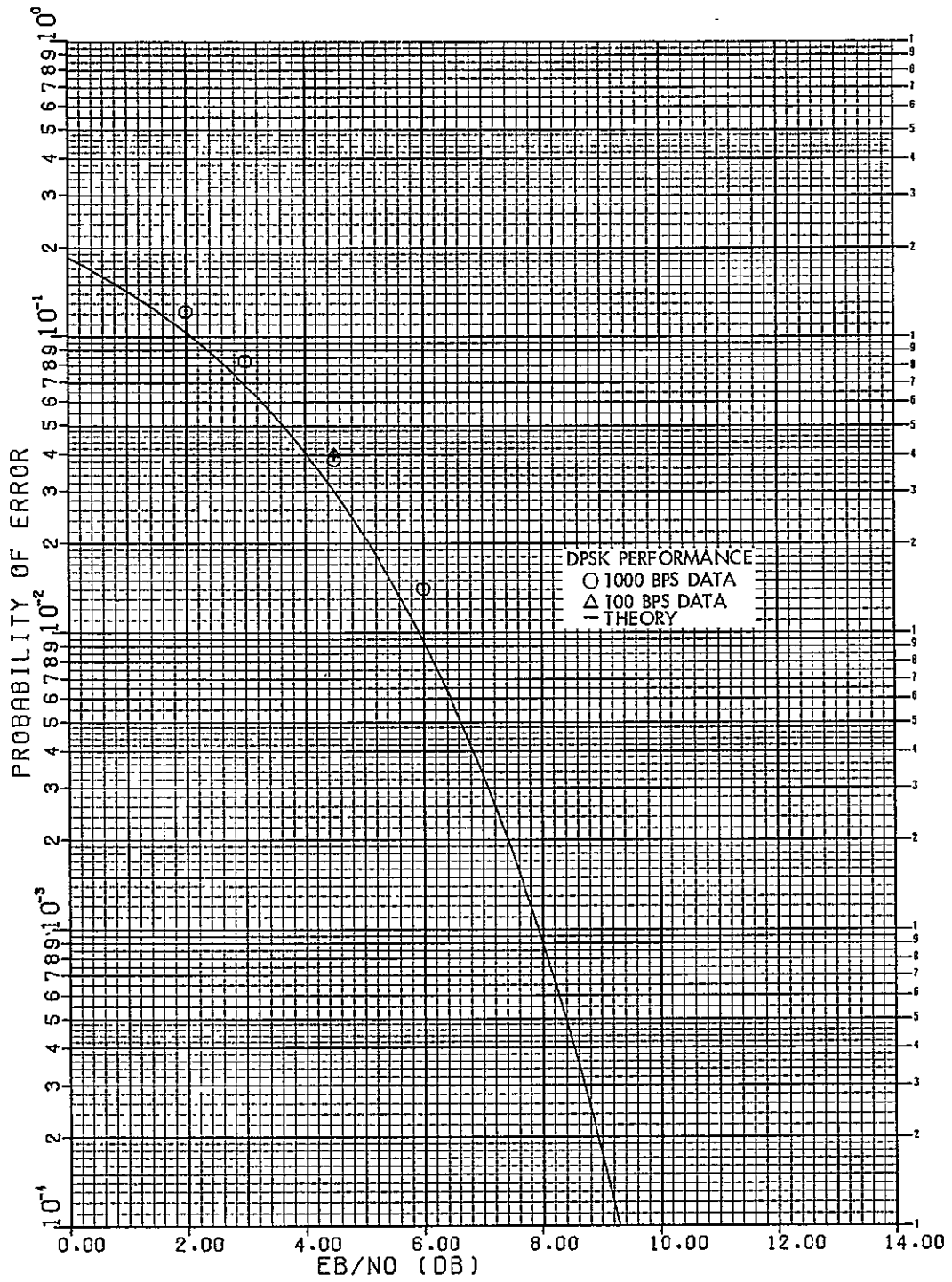


Figure 3-29. DPSK Bit Error Probability Performance

Table 3-5. 1000 BPS DPSK 50 Hz/sec Doppler

C/N <sub>0</sub>	E <sub>b</sub> /N <sub>0</sub>	P <sub>E</sub>	
		Theory	Measured (500 bit samples)
32.0 dB	2.0 dB	0.102	0.121
33.0	3.0	0.0680	0.082
34.5	4.5	0.0299	0.038
36.0	6.0	0.0093	0.014

Table 3-6. 100 BPS DPSK 50 Hz/sec Doppler

C/N <sub>0</sub>	E <sub>b</sub> /N <sub>0</sub>	P <sub>E</sub>	
		Theory	Measured (500 bit samples)
24.5	4.5	0.0299	0.040
26.0	6.0	0.0093	0.004

The DPSK demodulation results under a worst case 50 Hz/sec doppler rate are less than 0.5 dB from theory.

The bit error probability performance of discriminator detection of continuous phase FSK is a function of  $BT_B$ , the product of the predetection bandwidth B and the bit duration  $T_B$ , and the peak-to-peak frequency deviation ( $hT_B$ ). Experimental measurements\* of the probability of error for  $BT_B = 1$  and deviation  $h = 0.71$  are shown in Figure 3-30. At these parameters performance for discriminator detection falls between the noncoherent and coherent detection of FSK. The FSK demodulation algorithm shown in Figure 3-25 was simulated on a digital computer. The simulation results are summarized in Table 3-7 for the 1000 bps case. The deviation ratio (h) was taken to be 0.71. The simulated results are approximately 0.5 dB from that which was predicted.

\*P.D. Shaft, "Error Rate of PCM-FM Using Discriminator Detection," IEEE Trans on Space Electronics and Telemetry, December 1963, pp. 131-137.

Table 3-7. 1000 bps FSK 50 Hz/sec Doppler

$C/N_0$	$E_b/N_0$	$P_E$
33.0 dB	3.0 dB	0.183
34.5	4.5	0.126
36.0	6.0	0.075
40.0	10.0	0.005

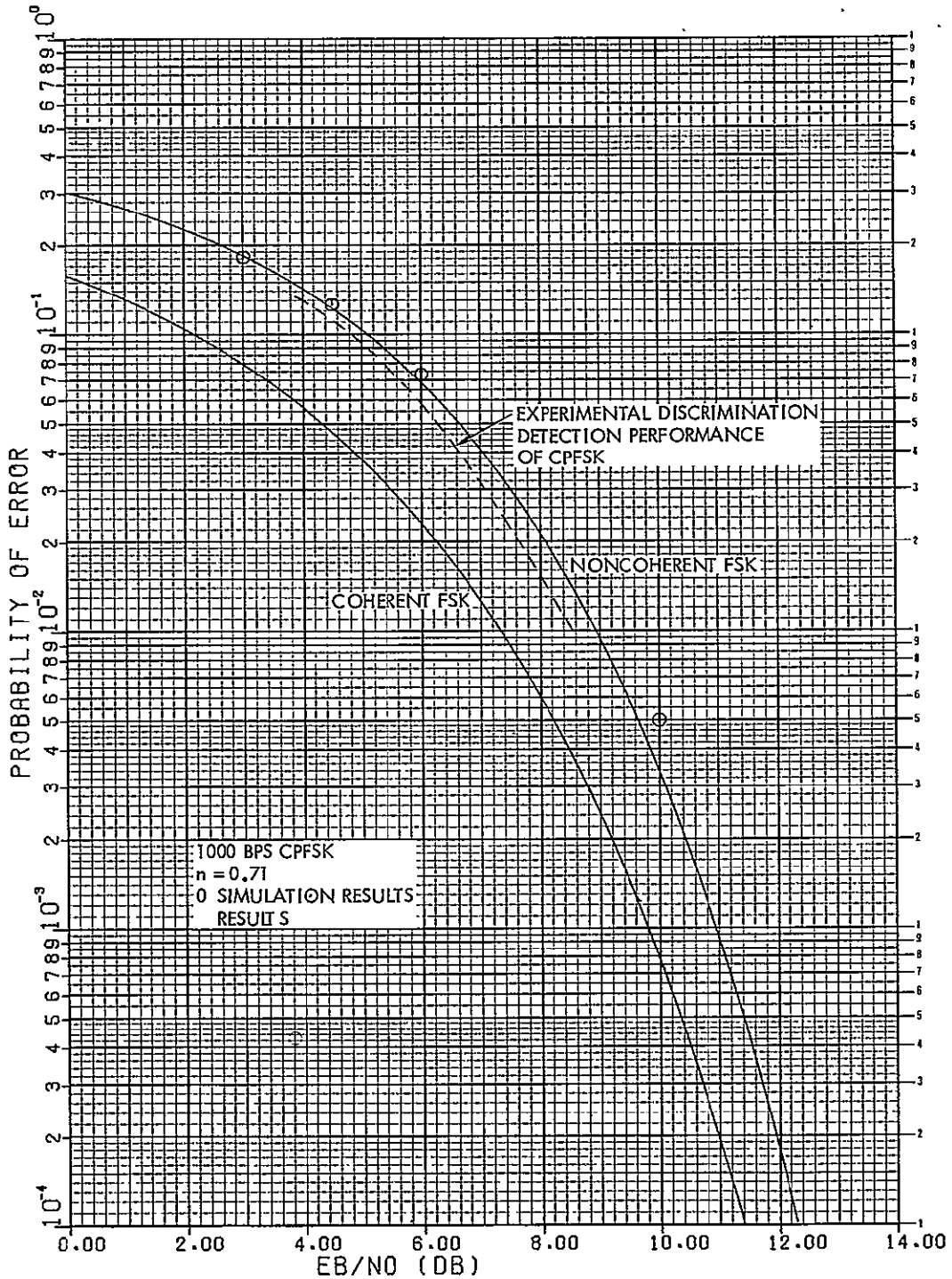


Figure 3-30. Performance of Discriminator Detection of CPFSK

## 4. RECEIVER CHARACTERISTICS

This section presents the mechanical configuration selected for the receiver and a preliminary set of interfaces for its operation and control. The reliability analysis has been completed and a method suggested for meeting the mission requirements. The receiver's reliability, radiation, and power consumption requirements greatly influenced the choice of components.

### 4.1 MECHANICAL LAYOUT

Figure 4-1 presents the mechanical layout suggested for the receiver and summarizes the receiver's other features. The layout is based on TRW's "standard slice" concept for high reliability spacecraft applications and combines two totally independent receivers into a single package. This fully redundant approach provides the simplest method of meeting the mission reliability requirements. Each individual receiver consists of three slices, one carrying RF/IF components, one carrying the microprocessor, and one for the A/D, sample and hold, NCO, and timing.

By grouping functions into slices, the process of detailed layout, assembly, and test is substantially simplified. Since each slice tends to contain a specific type of circuitry, measures to provide shielding and isolation, to protect against shock, vibration, EMI/EMC, etc., can be effectively tailored to that particular slice's needs.

The layout of the RF/IF slice is presented in Figure 4-2. This reflects the specialized needs of high frequency analog circuits as it consists of a number of individual cavities into which previously developed and tested assemblies are mounted. The cavities provide isolation between stages to reduce the possibility of instability and spurious response. Provisions have also been made for the mounting of EMI/EMC filters on the input power and output status lines.

An additional advantage which should not be overlooked is that new technology which would improve the receiver's performance can be incorporated into the receiver at the slice level.

### 4.2 RELIABILITY

A reliability analysis of the receiver design was performed based on the assumption that a typical mission would consist of 7-1/2 years in an unpowered state, followed by 6 months of operation at an effective operating temperature of 30<sup>0</sup> ambient. Failure rates were taken from MIL-HDBK-217B with rates for TRW LSI taken from TRW history and test data or from projections based upon similar parts previously produced.

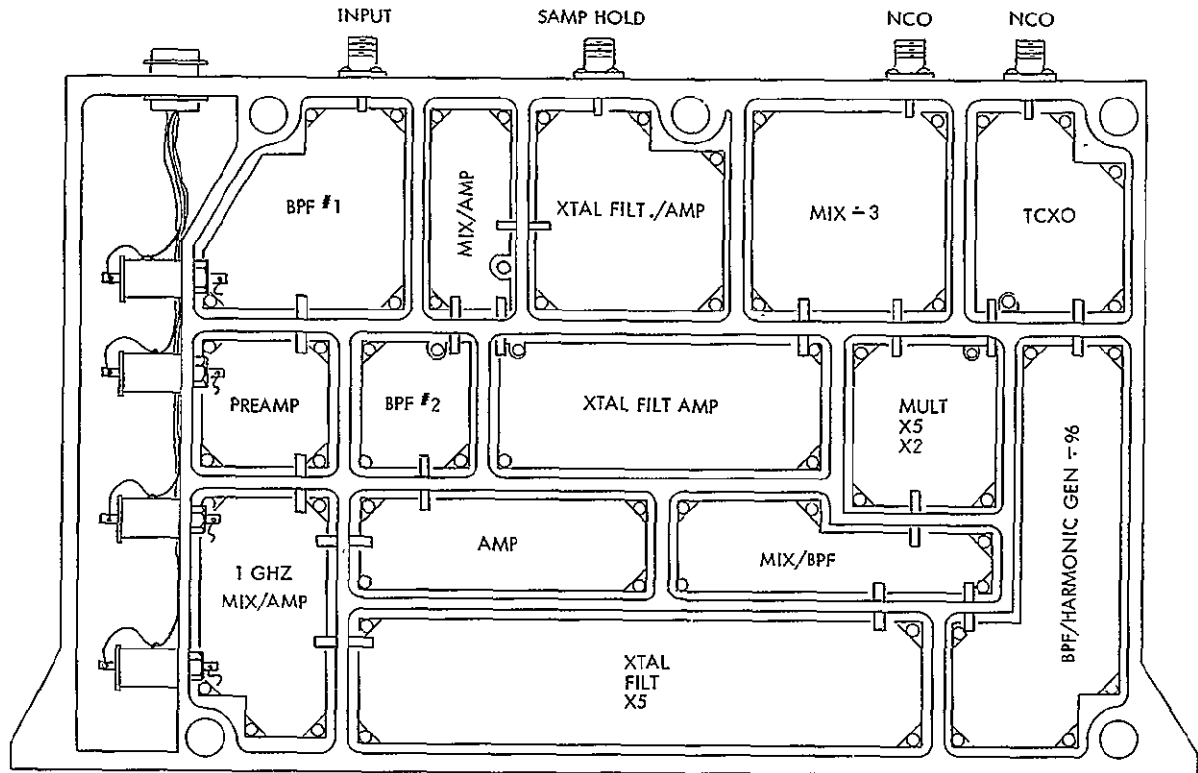


Figure 4-2. RF/IF Slice

The analysis used the following part reliability levels:

- Passive parts - ERMIL level P minimum  
level R or S for most parts
- Transistors and diodes - JANTXV
- SSI/MSI/memories - MIL-M-38510/MIL-STD-883 Class A where available,  
otherwise Class B
- TRW LSI - Full TRW reliability controls (Class B+)

For purposes of simplifying the analysis, the receiver was subdivided into three major portions: the front end, the digital system, and the frequency generator. A failure rate was then computed for each portion. These were then summed and an overall probability of mission success computed. Figures 4-3, 4-4, and 4-5 show the functions association with each portion while Tables 4-1, 4-2, and 4-3 present the corresponding failure rate calculations. In Table 4-2, the failure rates for the harmonic generator and 1st LO chain crystal filter was based on a simplification of the harmonic generator used on the FLTSATCOM spacecraft and the use of a plug-in board assembly which would contain a bandpass filter to limit the number of harmonics reaching the mixer. P7 in Tables 4-1 and 4-2 denotes a classified program.

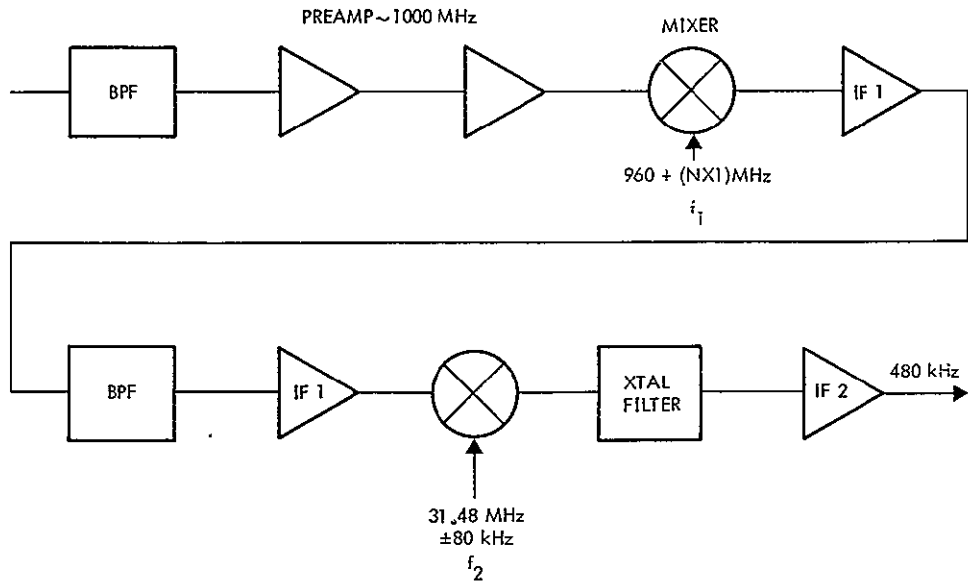


Figure 4-3. RF Section

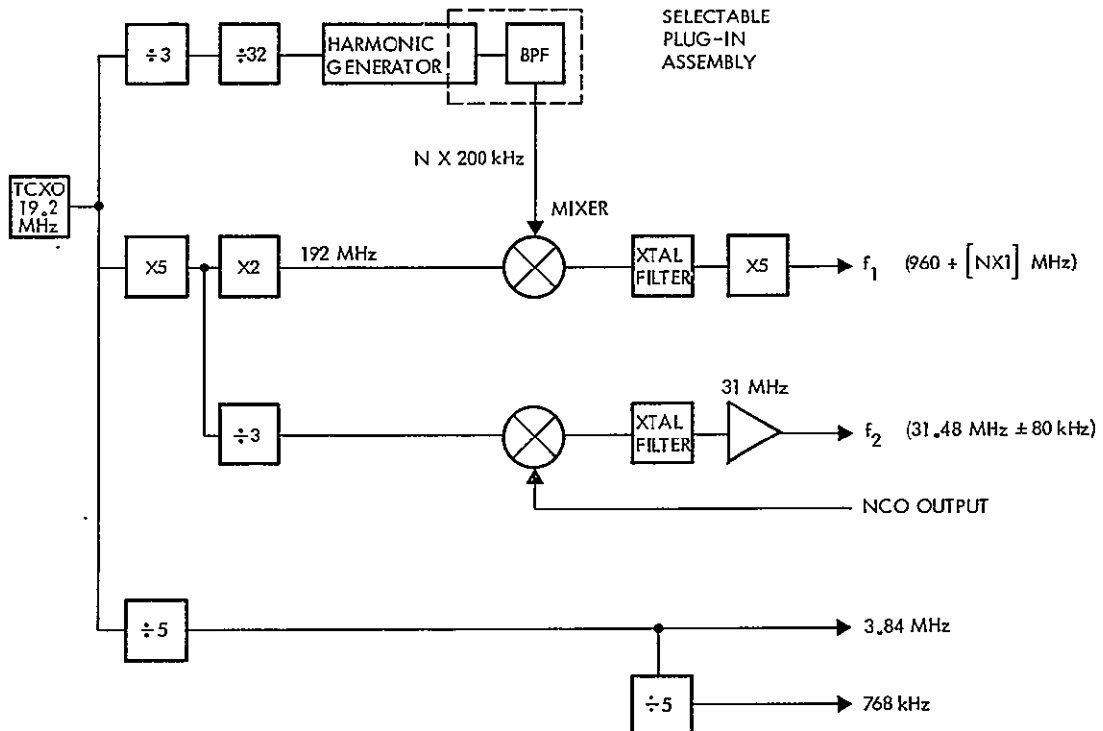


Figure 4-4. Frequency Generator



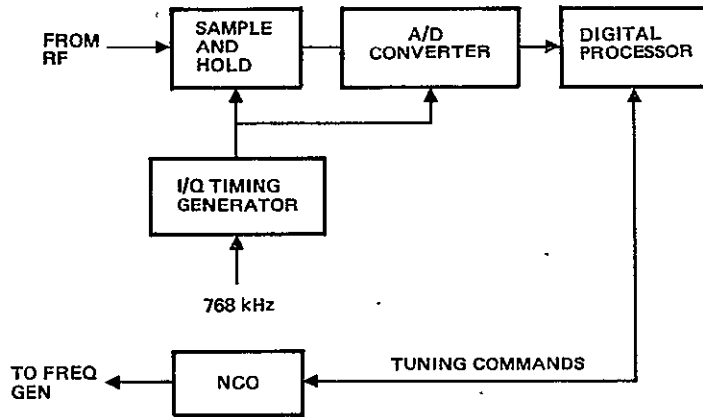


Figure 4-5. Digital System

Table 4-1. A RF Section Failure Rate Summary

Assembly	Reliability Data Source	Failure Rate $\lambda$ per $10^6$ hrs	Qty n	$\lambda N$
Input bandpass filter	Wavecom	0.025	1	0.0250
Preamplifier	P7	0.0494	2	0.0988
Mixer	P7, Space shuttle	0.084	2	0.1680
IF amplifier	P7, Space shuttle	0.0151	3	0.0453
1st IF BPF	P7	0.100	1	0.1000
2nd IF Xtal filter	Space shuttle	0.150	1	0.1500
				<u>0.5871 total</u>

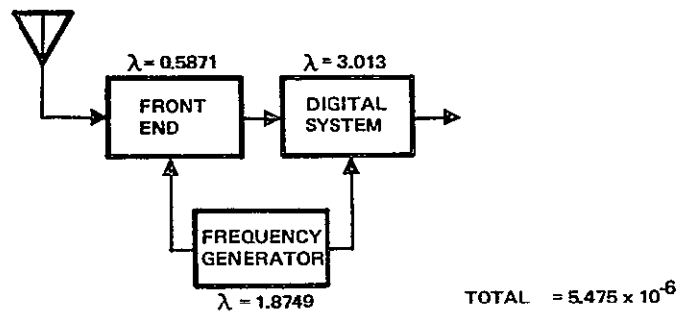
Table 4-2. Frequency Generator Failure Rate Summary

Assembly	Reliability Data Source	Failure Rate $\lambda$ per $10^6$ hrs	Qty N	$\lambda N$
TCXO	Space Shuttle	0.0826	1	0.0826
Multipliers/dividers (x5, ÷3, ÷5, ÷32)	FLTSATCOM	0.1058	7	0.7386
X2 multiplier	FLTSATCOM	0.1338	1	0.1338
Harmonic generator	FLTSATCOM adapt	0.251	1	0.251
Plug-in BPF board	FLTSATCOM adapt	0.1858	1	0.1858
Mixer	Space Shuttle	0.084	2	0.1680
Xtal filter	Space Shuttle	0.150	2	0.3000
31 MHz amplifier	P7	0.0151	1	<u>0.0151</u>
				1.8749 total

Table 4-3. Digital System Failure Rate Summary

Assembly	Component	Qty N	Failure Rate $\lambda N$
Sample and hold	Linear amplifiers	3	0.062
	Discretes	13	<u>0.086</u>
			0.148
A/D and Interfaces	A/D converter (TRW ADC-4)	1	0.500
	SSI and discretes	9	<u>0.021</u>
			0.521
NCO	SSI/MSI	17	0.205
	D/A converter (DAC-08)	1	<u>0.160</u>
			0.365
Digital processor	LSI (TRW MPY-8A)	1	0.500
	RAM's	2	0.038
	PROM's	3	1.005
	SSI/MSI	49	<u>0.436</u>
			0.979
			3.013 total

Figure 4-6 presents the configuration of a single receiver. The reliability calculations shown project a reliability figure of 0.941 which is below the required 0.98. The simplest redundant configuration was then analyzed. Figure 4-7 presents the proposed redundant configuration and the reliability calculations which established a reliability figure of 0.997. On the basis of this figure, a physical package consisting of two independent receivers was developed.



ACTIVE OPERATION (6 MONTHS = 4380 HOURS)

$$R_A = \exp[-4380 \times 5.475 \times 10^{-6}]$$

$$R_A = 0.974$$

STANDBY (7 1/2 YEARS = 65,700 HOURS)

$$R_S = \exp[-65,700 \times 5.475 \times 10^{-7}]$$

$$R_S = 0.965$$

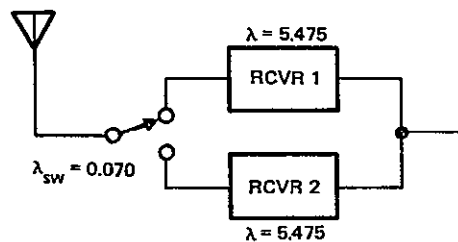
OVERALL RELIABILITY

$$R_{\text{MISSION}} = R_A R_S$$

$$= (0.974)(0.965)$$

$$= 0.941$$

Figure 4-6. Receiver Reliability Calculations



● DUTY CYCLE

$$d = 0.5/8 = 0.0625$$

● ACTIVE FAILURE RATE

$$\lambda_a = 5.475 \times 10^{-6}$$

● STANDBY FAILURE RATE

$$\lambda_s = 5.475 \times 10^{-7}$$

● EFFECTIVE FAILURE RATE

$$\lambda_e = \lambda_a(d) + \lambda_s(1-d)$$

$$\lambda_e = 0.859 \times 10^{-6}$$

● OVERALL RELIABILITY

$$R_{\text{MISSION}} = [\exp(-\lambda_e T)] \left[ 1 + \frac{\lambda_a}{\lambda_s + \lambda_{sw}} [1 - \exp(-\lambda_s T - \lambda_{sw} T)] \right]$$

$$T = 8 \text{ YEARS} = 70,800 \text{ HRS}$$

$$R_{\text{MISSION}} = (0.941) \{ 1 + (1.386)(0.043) \}$$

$$= 0.997$$

Figure 4-7. Redundant Receiver Reliability Calculations

### 4.3 INTERFACES

A preliminary list of the receiver's interfaces has been compiled and is presented in Table 4-4. Table 4-5 presents the list of commands envisioned for operational control of the receiver. Note that this command list allows the acquisition search to be restricted to as little as 20 kHz. Thus, if sufficient forehand knowledge of the doppler offset is available, it may be used to significantly reduce acquisition time. These tables should be considered typical but not performance limiting.

Table 4-4. Hybrid Receiver Interfaces

<u>INPUTS</u>		
Name	Form	Comments
RF Input	Analog	50 $\Omega$ input impedance, 1.5:1 Max VSWR at operating frequency $\pm 80$ kHz, -10 dBm max input level without receiver damage
DC power	Analog	12 V at 172 mA, 5 V at 1845 mA, -7 V at 41 mA, -12 V at 15 mA, -5 V at 5 mA
On/off control	Digital, 1-bit TTL compatible	Commands the receiver on and off
Operational	Digital, 8-bit Parallel format TTL compatible	Selects modulation type and bit rate, controls operational mode (acquisition/track), defines acquisition search range and radio science parameters
<u>OUTPUTS</u>		
Demodulated data	Digital, 8-bit Parallel format TTL compatible	One data bit per byte, 8-bit format allows for soft decision detection if desired later
Receiver status	Digital, 8-bit parallel format TTL compatible	Indicates receiver mode: standby, acquiring, pull-in, locked. Uses same output port as radio science data
Buffered TCXO	TBD	19.2 MHz signal from rcvr TCXO
Temperature TLM	Analog	TLM voltage derived for rcvr internal temperature, exact format is TBD
Current TLM	Analog	One output for each input voltage is supplied, exact format is TBD
Radio science data	Digital, 8-bit parallel format TTL compatible	Serial byte format. First byte indicates type of measurement, integration time, and number of data bytes to follow (32 max). Data bytes are transmitted in order beginning with the MSB.

Table 4-5. Operational Control Commands

Function	Representation 3-3-2 Bits	Comments
No-op	0 0 0	
Standby	7 0 0	Places receiver in idle condition
Initiate coarse acquisition (wide sweep range)	1 0 A	Field "A" selects sweep range  A = 0 indicates $\pm 80$ kHz sweep = 1 indicates 0 to +80 kHz = 2 indicates 0 to -80 kHz = 3 indicates -40 to +40 kHz
Initiate coarse acquisition (fine sweep range)	1 B 0	Field "B" selects sweep range  B = 0 indicates $\pm 80$ kHz sweep = 1 indicates -20 to +20 kHz = 2 indicates 0 to -20 kHz = 3 indicates 0 to +20 kHz = 4 indicates 0 to -40 kHz = 5 indicates 0 to +40 kHz = 6 indicates -80 to -40 kHz = 7 indicates +40 to +80 kHz
Initiate fine acquisition (pull-in)	3 0 0	Optional - backup command
Demodulate and track	5 0 0	Optional - backup command
Set demodulator type and bit rate	2 A B	Field "A" selects data rate  A = 0 indicates 100 bps = 1 indicates 200 bps = 2 indicates 400 bps = 3 indicates 1000 bps  Field "B" selects demodulator type  B = 0 indicates type 1 = 3 indicates type 2
Initiate radio science measurements	4 A B	Field "A" selects integration time  A = 0 indicates 1 sec = 1 indicates 2 sec = 2 indicates 4 sec = 3 indicates 8 sec = 4 indicates 16 sec = 5 indicates 32 sec = 6 indicates 64 sec  Field "B" selects measurement type  B = 0 indicates pwr measurement = 3 indicates freq measurement = 1 or 2 indicates both

#### 4.4 COMPONENT SELECTION

The selection process for the major receiver components was based on criteria:

- Reliability
- Performance
- Power consumption
- Radiation hardness.

Of these, reliability had to be the dominant consideration if the mission reliability requirement was to be met without excessive redundancy. Section 4.2 presented, the minimum reliability levels required for passive and active components in this application. It is noteworthy that the reliability analysis which assumed the use of high-reliability parts throughout concluded that two receivers are necessary to meet the mission requirement.

The remaining three factors must be traded off to determine if a component (or family of components) is to be preferred over another. The tradeoffs associated with the major component groups (LSI/MSI, A/D and D/A converters, active RF components, operational amplifiers, and analog switches) are discussed in the following sections. Table 4-6 presents a complete list of all active components used in the receiver.

##### 4.4.1 Digital LSI/MSI

Investigations of the various logic families which might be used to construct the digital processor, NCO, variable modulus divider, and timing circuits determined that the low power Schottky TTL and radiation hardened CMOS families were the most attractive. Low power Schottky TTL was the final choice. The selection process specifically concentrated on "families" rather than individual devices except in the most specialized of applications. This was done to assure uniformity in such practical considerations as supply voltages and logic levels.

Low power consumption was the primary reason for considering CMOS logic. A fairly extensive family of devices (the 4000 series) capable of operating over the military temperature range is available. Many of these are qualified to MIL-STD-883. Standard CMOS devices, however, are very susceptible to radiation damage and thus extensive radiation shield would be required.

RCA, one of the major manufactures of CMOS, was contacted to determine the current and projected status of CMOS relative to radiation. RCA is currently producing CMOS which is guaranteed to 100K rad (Si). A very limited group of devices tested on a wafer basis to 150K rad (Si) is also being supplied to JPL. RCA projects that a large number of the 4000 series devices guaranteed to 500K rad (Si) will be available within the next 2 years.

Table 4-6. Active Parts List

Part Designator	Power Unit	Number	Total Power	MIL 38510	MIL 883	Comments
● <u>Sample &amp; hold with offset circuit</u>						
HA2520	120 mW	3	360		✓	JANTXV
2N4856	360 mW	1	360			
		<u>4</u>	<u>720 mW</u>			
● <u>Numerically controlled oscillator</u>						
54LS377	100 mW	9	900		✓	
54LS83A	100 mW	6	600	✓	✓	
54LS86	40 mW	2	80	✓		
DAC-08	33	1	33		✓	
		<u>18</u>	<u>1.613 W</u>			
● <u>A/D converter &amp; interface</u>						
TRW ADC-4(MOD)	200 mW	1	200	—	—	TRW reliability controls
54LS05	8 mW	1	8	✓		
HP2810	6 mW	8	48 mW		✓	
Bias network	24 mW	2	48 mW	N/A	N/A	
		<u>12</u>	<u>304 mW</u>			

Table 4-6. (Continued)

Part Designator	Power Unit	Number	Total Power	MIL 38510	MIL 883	Comments
● <u>RF front end</u>						
HP35866 OPT 100	96 mW	2	192		✓	
HP35826	96 mW	2	192		✓	
HP21	60 mW	2	120		✓	
MC1590	180 mW	3	540		✓	
MC1590	120 mW	1	120		✓	Different biasing
MS175JE	120	2	240		✓	
FEI TCXO	120 mW	1	120	N/A	N/A	Nasa reliability specs
		<u>13</u>	<u>1.524W</u>			
● <u>Frequency generator and variable modulus divider</u>						
54LS196	60	2	120	✓		
54LS30	3	1	3	✓		
54LS197	60	2	120	✓		
54LS113	20	3	60	✓		
54LS20	4	1	4	✓		
54S140	44	1	44	✓		
MC10535	270	1	270		✓	
54S00	75	1	75	✓		
54LS163	130	1	130	✓		
		<u>13</u>	<u>826</u>			
● <u>Micro processor</u>						
25LS281	150 mW	2	300		✓	
82S181	400	3	1200		✓	
TRW MPY-8A	1800	1	1800	—	—	TRW reliability controls
93L422	300	2	600		✓	
54LS298	100	14	1400		✓	
54LS163	100	4	400	✓		
54LS151	40	8	320	✓		
54LS174	100	1	100	✓		
54LS00	8	4	32	✓		
54LS02	11	2	22	✓		
54LS04	12	4	48	✓		
54LS08	17	2	34	✓		
54LS10	8	2	16	✓		
54LS86	32.5	2	65	✓		
54LS74	40	4	160	✓		
		<u>54</u>	<u>6.497W</u>			
			<u>11.484 receiver total</u>			



CMOS logic was determined to be too slow for use in the NCO design with its 3.84 MHz clock rate. For instance, a 24-bit addition must be performed in less than 260 nsec. A 16-bit addition using CMOS requires more than 500 nsec even when the logic is operated at a +10 V supply level. Similar problems were encountered when application of CMOS to the microprocessor architecture was investigated. Thus the ideas of using CMOS digital logic was abandoned.

Conversely, low power Schottky (LS) TTL has more than adequate speed for all the receiver's digital applications except the 96 MHz divide-by-3 process which required a ECL device. LS TTL devices also exhibit excellent immunity to radiation at the specified exposure levels.

The devices selected for use are primarily from the 54LSXXX family. All are qualified to the full military temperature range and virtually all are available with MIL-M-38510 certification. A number of specialized devices not found in the 54LSXXX family are required to complete the microprocessor design. These are off the shelf items available from a number of manufacturers including TRW, AMD, Signetics, and Fairchild. All are radiation hard, meet the military temperature range, and are available in high reliability versions.

Because of the extensive variety of devices in the 54LSXXX series and the availability of specialized devices to fill other key roles, it was possible to achieve a very efficient design whose overall power requirement was acceptable.

#### 4.4.2 A/D and D/A Converters

Power consumption and radiation hardness were the primary factors in the selection of the A/D converter. The combination of word size and sampling rate are sufficiently modest that any one of a number of hi-rel devices is capable of meeting these requirements.

The TRW ADC-4 was selected over the others, however, because it is a radiation hardened, monolithic device specifically designed for spacecraft applications. In its original form, the ADC-4 requires 800 mW of power which is slightly higher than some of the commercial monolithics. Through discussions with the TRW LSI designers, it was learned that this power figure could easily be reduced to under 200 mW by merely changing sheet resistivity during chip fabrication. This change would have no adverse effect upon the A/D's radiation hardness and performance when operating at these rates.

The Precision Monolithics Model DAC-08 D/A converter was selected for use in the NCO because it is a proven component which represents the best combination of performance and power consumption presently available. The NCO design requires a D/A with a settling time much faster than its 260 nsec clock time. The DAC-08's guaranteed performance is 135 nsec at a power consumption of only 33 mW. For this reason, the

DAC-08 is widely used in TRW's NCO designs and other D/A applications. Versions are available qualified to MIL-STD-883 and the full military temperature range.

#### 4.4.3 Active RF Components

With the exception of the L-band transistors, complete RF assemblies were selected rather than individual RF components. In keeping with the requirements of the Statement of Work, emphasis during design of the front end was placed upon making use of proven, space qualified designs.

The only changes of active components for those originally used were in the 1 GHz preamplifier and amplifier assemblies. Here a HP35866 option 100 is substituted for the existing HP35821 and a HP35826 is substituted for the HP35822. The impact of these changes is to provide better noise figure performance. Reliability and radiation performance are unaffected as these are space qualified devices which use the same bipolar fabrication techniques as the transistors they replaced.

#### 4.4.4 Operational Amplifiers and Analog Switches

The design of the hybrid receiver has been especially tailored to make minimal use of operational amplifiers and analog switches because of their notorious difficulties with radiation. Only the sample and hold circuit uses these devices. The numbers involved (3 op amps, 1 JFET switch) were so small that it was decided to use the most radiation resistant devices available which were compatible with performance requirements. On this basis, the Harris HA2520 operational amplifier and the 2N4856 JFET were selected. Both have acceptable radiation resistance and are rated for the military temperature range. High reliability versions of both devices are available and the power requirements for their use are acceptable.

## 5. RADIO SCIENCE MISSION

A secondary function which the hybrid receiver is well suited to perform is that of making precision signal power and doppler frequency measurements for radio science purposes. The parameters to be measured (i.e., signal amplitude and frequency) are already in digital form within the receiver's processor. Therefore, the process of integration (smoothing) required to reduce the uncertainty of estimates due to noise reduces directly to a straightforward mathematical operation. Only a fraction of the processor's unused memory and excess processing speed is taken up by this operation. Additionally, the smoothed estimates are in a form directly compatible with a digital telemetry interface.

The desired levels of performance presented as design guidelines for the radio science measurements and the estimated receiver capabilities are presented in Table 5-1.

### 5.1 . SIGNAL POWER MEASUREMENT

The impact of the signal power measurement requirements upon the receiver design is minimal. This is because the sequential detection algorithm used during signal acquisition already demands high resolution noise power estimates. A high measure of gain stability has also been incorporated into the front end to minimize noise figure variations. Thus, many of the features which contribute to accurate signal power estimates already are found in the basic receiver design. The factors which limit signal power measurement accuracy are:

- Front end gain variation (assuming constant temperature) with:
  - Input frequency
  - Supply voltage
- Quantization noise
- Thermal noise.

Of these factors, the effect of quantization noise is negligible. Referring back to Section 2.2, the design of the interface between the RF front end and the A/D converter placed quantization noise more than 20 dB below the thermal noise for all input signal levels.

Variations in front end gain with input frequency are caused by amplitude ripple in the passband of the first IF filter. For noise estimation purposes, this ripple has already been limited to less than  $\pm 0.1$  dB, which is adequate for signal estimation.

At a constant temperature ( $\pm 1^{\circ}\text{C}$ ), other gain variations are solely a function of the regulation on voltages supplied to the front end amplifiers. The various mixers are operated in sufficiently LO saturated mode that their output levels are virtually unaffected by small variations in LO drive level. A number of tests were performed on

Table 5-1. Radio Science Performance

Performance Parameter	SOW Specification	Receiver Capability
<u>Signal Power Measurement</u>		
Accuracy	±1 dB	±0.7 dB
Gain stability	±0.1 dB	±0.1 dB*
Averaging times	1 to 60 sec	1,2,4,8,16,32,64 sec
Estimate uncertainty (3σ)	-	-
● 1 kbps, C = -116 dBm (high SNR)		
Single sample	-	±0.04 dB
0.1 sec (100 samples)	-	±4.3 x 10 <sup>-3</sup> dB
10 sec (1000 samples)	-	±4.3 x 10 <sup>-4</sup> dB
● 100 bps, C = -146 dBm (low SNR)		
Single sample	-	±3 dB
1 sec (100 samples)	-	±0.41 dB
60 sec (6000 samples)	-	±0.056 dB
*Assumes regulated power to front end		
<u>Frequency Measurement</u>		
Frequency resolution	TBD	±0.114 Hz (24-bit command)
Averaging times	1 to 60 sec	1,2,4,8,16 sec
Frequency uncertainty (3σ)		
● 100 bps, D = 50 Hz/sec, C = -126 dBm		
Single sample	-	±3.78 Hz
1 sec (100 samples)	-	±0.377 Hz
5 sec (500 samples)	-	±0.169 Hz
10 sec (1000 samples)	-	±0.119 Hz
● 1 kbps, D = 50 Hz/sec C = -136 dBm		
Single sample	-	±7.53 Hz
1 sec (1000 samples)	-	±0.24 Hz
5 sec (5000 samples)	-	±0.11 Hz
10 sec (10,000 samples)	-	±0.076 Hz

gain stages typical of those proposed for use in the front end to determine their sensitivity to changes in supply voltage. These tests indicated that voltages regulated to 0.5% must be provided if the stability specification is to be met. Approximately 0.93 watts of regulated power (12 V at 77 mA) are required.

The A/D converter has its own internal voltage reference and hence is less sensitive to supply voltage fluctuations. However, the A/D's power consumption is so low (200 mw = -7 V at 29 mA) that the effect of adding it to the circuits receiving regulated power would be minimal.

It is estimated that with regulated power and additional temperature compensation, the total front end gain will not vary more than ±0.5 dB with age, radiation, and temperature. Table 5-2 presents the overall error figures associated with front end gain. These figures indicate that an on-board amplitude calibrator would not be required to meet the accuracy specification.

Table 5-2. Gain Errors

Age, Temperature, Radiation	Power Supply Fluctuation	Filter Ripple	Worst Case Error	RSS Error
±0.5 dB	±0.1 dB	±0.1 dB	±0.7 dB	±0.52 dB

The effect of thermal noise on the signal power estimate is reduced by a process of integration (averaging) which is implemented in the digital processor as

$$(N)(\hat{P}) = \sum_{i=1}^N (I_i^2 + Q_i^2) \quad (5.1)$$

where

$\hat{P}$  = the power estimate

N = the number of samples to be averaged

$I_i, Q_i$  = the  $i^{\text{th}}$  inphase and quadrature component of the filtered bandpass process

The output of the microprocessor to telemetry consists of two portions: the accumulator value ( $\sum (I_i^2 + Q_i^2)$ ) and the sample count (N). On the ground,  $\hat{P}$  is then calculated to the desired accuracy.  $I_i^2$  and  $Q_i^2$  are 16-bit numbers which provide for better resolution than the required ±0.1 dB. The processor is capable of multiple precision accumulation so that the accumulator value can be transmitted without truncation or rounding errors.

The "weak law of large numbers" indicates that the variance of the estimate can be reduced by appropriate selection of the number (N) of independent I/Q sample pairs used in the integration process. This assumes, of course, that the signal amplitude (without noise) is constant during the integration period. The number of independent samples per second is a function of input bandwidth (bit rate) and thus, similarly to analog systems, improvement is a function both of input bandwidth and integration time. The worst case processor load imposed by the accumulation process (assuming one sample per data bit) is less than 1%.

Table 5-3 presents calculations of signal measurement errors due to noise for several combinations of signal level and data rates.

Table 5-3. Signal Power Measurement Error

<p><u>Case I - High SNR (1 kbps, C = -116 dBm)</u></p> <p><u>Single sample</u></p> <p>Noise power (<math>3\sigma</math>) = 20.0 dB relative to signal power</p> <p>Quantization noise power = -40.0 dB relative to signal power</p> <p>Total (<math>3\sigma</math>) error = -20 dB relative to signal power</p> <p><u>Improvement with averaging</u></p> <p>0.1 sec (100 samples): Total error = -30 dB relative to signal power</p> <p>10 sec (10,000 samples): Total error = -40 dB relative to signal power</p> <p><u>Case II - Low SNR (100 bps, C = -146 dBm)</u></p> <p><u>Single sample</u></p> <p>Noise power (<math>3\sigma</math>) = 0 dB relative to signal power</p> <p>Quantization noise power = -20 dB relative to signal power</p> <p>Total (<math>3\sigma</math>) error = 0 dB relative to signal power</p> <p><u>Improvement with averaging</u></p> <p>1 sec (100 samples): Total error = -10 dB relative to signal power</p> <p>60 sec (6000 samples): Total error = -18.9 dB relative to signal power</p>
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## 5.2 FREQUENCY MEASUREMENT

The tuned frequency of the receiver is controlled by the NCO command word which is generated by the microprocessor. When a signal has been acquired and is being tracked, its frequency may be derived from the NCO command word and the frequency of the receiver's reference source(s). The doppler offset is then the difference between the measured frequency and the "at rest" frequency.

A single 19.2 MHz TCXO of proven reliability in spacecraft applications has been established as the receiver's sole frequency reference. All the receiver's internal frequencies (LO's, A/D timing, etc.) are derived from this reference. Thus, the accuracy and stability of any frequency measurements made by the receiver are influenced directly by the TCXO's performance. The relationship between the signal frequency, reference frequency, and NCO command word is given by

$$f_{\text{sig}} = f_{\text{ref}} \left( 50 + \frac{5M}{96} + \frac{5}{3} - \frac{1}{40} - \frac{N}{5 \times 2^{24}} \right) \quad (5.2)$$

where

$f_{\text{sig}}$  = signal frequency

$f_{\text{ref}}$  = reference source frequency

N = NCO command word

M = a positive integer (0, 1, 2, ...) which is set when the receiver's center frequency is established

Figure 5-1 provides the basis for this derivation.

Two types of errors are associated with the frequency measurement process. Bias errors are essentially constant over the measurement interval and are independent of averaging time. Thus, they cannot be reduced by extending the averaging time. Random errors have instantaneous values which fluctuate over the averaging time. Since they behave as random variables, their effect on measurement accuracy can be reduced by extending the averaging time. The major sources of bias and random errors are presented in Table 5-4.

The worst case error values attributable to the TCXO reference oscillator are:

Accuracy	$\pm 5 \times 10^{-7}$ per year ( $\approx \pm 500$ Hz/year at 1 GHz)
Stability	$\pm 1 \times 10^{-9}$ per sec ( $\approx \pm 1$ Hz/sec at 1 GHz)
Radiation effects	$\pm 1 \times 10^{-12}$ per rad ( $\approx 200$ Hz at 1 GHz after 200K rad)

$$f_{SIG} = f_{1LO} + f_{1IF}$$

$$f_{1LO} = (10 + \frac{M}{96}) 5 f_{REF} \text{ (where M is the harmonic selected from the comb generator)}$$

$$f_{1IF} = 31 \text{ MHz} = f_{2LO} - f_{2IF}$$

$$f_{2IF} = \frac{f_{REF}}{40} \text{ (a fixed relationship necessitated by the I/Q sampling scheme)}$$

$$f_{2LO} = \frac{5}{3} f_{REF} - f_{NCO}$$

$$f_{NCO} = \frac{N f_{REF}}{5 \times 2^{24}} \text{ (where N is the NCO command word)}$$

Therefore

$$f_{SIG} = f_{REF} (50 + \frac{5M}{96} + \frac{5}{3} - \frac{1}{40} - \frac{N}{5 \times 2^{24}})$$

Figure 5-1. Relationship Between Receiver Tuned Frequency, NCO Command Word and Reference Source Frequency

Table 5-4. Frequency Measurement Error Sources

Bias Error Sources

Reference oscillator accuracy (long term drift)

Radiation effects on the reference oscillator

Random Error Sources

NCO quantization noise

Tracking loop jitter

Reference oscillator stability (short term drift)



The accuracy and stability figures are taken directly from the manufacturer's guaranteed performance specifications over temperature and hence may be pessimistic by a factor of 2 or 3. The radiation effects figure is the one commonly employed by TRW's vulnerability and hardness group in their analyses. This again is a somewhat pessimistic value as JPL measured  $\approx 1.8 \times 10^{-11}$  per rad in their testing of the Jupiter Orbiter's ultra stable oscillator.

The peak error due to quantization of the NCO command word is  $\pm(\frac{1}{2})$   
 $(\frac{19.2 \times 10^6}{5 \times 2^{24}}) = \pm 0.114$  Hz. Assuming a uniform distribution of error, the rms error associated with the NCO command word is then 0.0661 Hz which should be negligible. The tracking loop performance was discussed in detail in Section 3.

As with amplitude measurements, the effect of random errors on the estimate can be reduced by a process of integration which is implemented in the digital processor as

$$(K) (\hat{N}) = \sum_{i=1}^K N_i \quad (5.3)$$

where

$\hat{N}$  = the NCO command word corresponding to the estimated frequency

$N_i$  = the  $i^{\text{th}}$  NCO command word

$K$  = the number of samples to be integrated

The output of the microprocessor to the telemetry consists of two portions: the accumulator value ( $\sum N_i$ ) and the sample count ( $K$ ). On the ground,  $\hat{N}$  is calculated and the frequency estimate is obtained by using equation (5.2).

The NCO command word utilizes 22 bits of a 24-bit (3 byte) format and thus the accumulation process might appear somewhat awkward. The processor, however, is readily capable of multiple precision accumulation and the NCO word update rate is sufficiently slow that worst case processor load is under 1%. Table 5-5 presents worst case frequency measurement errors.

For those missions which cannot tolerate the levels of error introduced by the TCXO, a number of alternatives are available. These include:

- Provide radiation shielding for the receive reference oscillator (bias error reduction only)
- Provide a frequency calibrator to measure the TCXO output frequency (bias error reduction only)
- Use the spacecraft on-board reference oscillator as the receiver reference oscillator.

Table 5-5. Frequency Measurement Error

Bias error ( $f_{ref} = 19.2$  MHz,  $f_{sig} = 991.0$  MHz)

Accuracy Error	Radiation Error	Worst Case Error	RSS Error
±499.5 Hz	±198.2 Hz	±697.7 Hz	±537.4 Hz

Random error

High SNR (Loop BW = 3 Hz, data rate = 100 bps, doppler = 50 Hz/sec)

Single sample

3 $\sigma$ Stability Error	3 $\sigma$ Loop Jitter Error	Peak NCO Quant Noise	Worst Case Error
±2.973 Hz	±0.69 Hz	±0.114 Hz	±3.777 Hz

Multiple samples

3 $\sigma$ Error After 100 Samples (1 sec)	3 $\sigma$ Error After 500 Samples (5 sec)	3 $\sigma$ Error After 1000 Samples (10 sec)
±0.377	±0.169 Hz	±0.119 Hz

Low SNR (loop BW = 3 Hz, data rate = 1 kbps, doppler = 50 Hz/sec)

Single sample

3 $\sigma$ Stability Error	3 $\sigma$ Loop Jitter Error	Peak NCO Quant Noise	Worst Case Error
±2.973 Hz	±4.5 Hz	±0.114 Hz	±7.59 Hz

Multiple samples

3 $\sigma$ Error After 1000 Samples (1 sec)	3 $\sigma$ Error After 5000 Samples (5 sec)	3 $\sigma$ Error After 10000 Samples (10 sec)
±0.24 Hz	±0.11 Hz	±0.076 Hz

Radiation induced errors can be reduced by shielding the receiver's reference oscillator. A special removable shield could be configured and then utilized only on those missions which demonstrated a favorable tradeoff of additional weight vs reduced bias error.

A frequency calibrator would require an on-board reference source whose accuracy is substantially better than that of the TCXO. It is estimated that a calibrator capable of measuring the TCXO to an accuracy of  $\pm 1 \times 10^{-8}$  (plus the on-board reference uncertainty) would require approximately 1.5 watts. Since the calibrator could reduce only long term errors, it would not have to operate constantly and therefore its average power consumption would be substantially less than 1.5 watts. The worst case bias error remaining after use of the calibrator would be  $\pm 10$  Hz. As with shielding, the additional weight and power consumption attributable to the use of the calibrator could be traded off against the reduction in bias error to determine if its use was justified.

Missions which utilize the DSN standard transponder are equipped with a JPL ultra stable oscillator (USO) whose output frequency is in the range of 19.08 to 19.17 MHz. The exact frequency is determined by the S-band transmission frequency assigned for the transponder's one-way TLM operating mode. The ultra stable oscillator has substantially better stability and accuracy than a TCXO. Nominal performance values are:

Accuracy  $\pm 1 \times 10^{-7}/3$  years ( $\approx \pm 100$  Hz/3 years at 1 GHz)

Stability  $\pm 1 \times 10^{-12}/\text{second}$  ( $\approx \pm 0.001$  Hz/second at 1 GHz)

Accuracy can be improved to approximately  $1 \times 10^{-10}$  by earth measurement of the one-way TLM frequency.

The output frequency range is sufficiently close to the TCXO's that it could be used as the receiver's reference oscillator if certain modifications are made to the front end. Table 5-6 presents the worst case frequency measurement errors when the USO is used as the reference oscillator.

The second IF frequency, the center frequency of the second local oscillator, and the NCO tuning range are influenced by the reference oscillator frequency. The frequencies which result from use of the USO are shown in Table 5-7. The major impact of these changes in frequency is to require substantially better shape factor performance from the crystal filter which extracts the desired LO frequencies ( $f_{\text{mix}} - f_{\text{NCO}}$ ). This is because, in the worst case, the  $f_{\text{mix}}$  feedthrough signal is moved some 200 kHz closer to the desired passband and the ( $f_{\text{mix}} + f_{\text{NCO}}$ ) product is moved 385 kHz closer. It is very doubtful that a single filter could provide the required combination of percentage passband and shape factor. Thus, at least one additional filter and buffer stage would be required to achieve the same suppression that a single filter gives when used with the TCXO.

Table 5-6. Frequency Measurement Error  
(Ultra Stable Oscillator)

Bias Error ( $f_{ref} = 19.17$  MHz,  $f_{sig} = 989.3$  MHz)

	Accuracy Error	Radiation Error	Worst Case Error	RSS Error
No calibration	$\pm 32.98$ Hz	$\pm 197.9$ Hz	$\pm 230.8$ Hz	$\pm 200.6$ Hz
Earth calibration	N/A	N/A	$\pm 0.21$ Hz	$\pm 0.15$ Hz

Random error

High SNR (loop BW = 3 Hz, data rate = 100 bps, doppler = 50 Hz/sec)

Single sample

$3\sigma$ Stability Error	$3\sigma$ Loop Jitter Error	Peak NCO Quant Noise	Worst Case Error
$\pm 3 \times 10^{-3}$ Hz	$\pm 0.69$ Hz	$\pm 0.1144$ Hz	$\pm 0.81$ Hz

Multiple samples

$3\sigma$ Error After 100 Samples (1 sec)	$3\sigma$ Error After 500 Samples (5 sec)	$3\sigma$ Error After 1000 Samples (10 sec)
$\pm 0.081$ Hz	$\pm 0.036$ Hz	$\pm 0.026$ Hz

Low SNR (loop BW = 3 Hz, data rate = 1000 bps, doppler = 50 Hz/sec)

Single sample

$3\sigma$ Stability Error	$3\sigma$ Loop Jitter Error	Peak NCO Quant Noise	Worst Case Error
$\pm 3 \times 10^{-3}$ Hz	$\pm 4.5$ Hz	$\pm 0.1144$ Hz	$\pm 4.62$ Hz

Multiple samples

$3\sigma$ Error After 1000 Samples (1 sec)	$3\sigma$ Error After 5000 Samples (5 sec)	$3\sigma$ Error After 10,000 Samples (10 sec)
$\pm 0.146$ Hz	$\pm 0.065$ Hz	$\pm 0.046$ Hz

APPENDIX A  
COMPONENTS SURVEY

This appendix presents a list of components whose performance, reliability, power consumption, and radiation hardness characteristics make them potentially applicable to the hybrid receive design concept. To be included; a component had to meet the following minimum requirements:

- Reliability — Qualification to MIL-STD-883 Class A or B  
or MIL-M-38510 Class A or B
- Temperature — Qualified over the range -20°C to +60°C
- Radiation — Capable of withstanding 200 K rad (Si) with reasonable shielding.

No claim is made as to the exhaustiveness of this list as it is intended only to present starting points for alternate hardware designs.

Digital Logic

- 54 LSXXX family (Low power Schottky)
- Am 25LSXXX family (Low power Schottky)
- Am 27LSXXX family (Low power Schottky)
- RCA CD4XXX family (C-MOS with option "Z" processing)  
(see RCA publication SSD-230 "High Reliability Devices")

Binary Multipliers

- TRW MPY-8A (8 x 8, 2's complement)
- AMD Am 25L05 (4 x 2, 2's complement)
- TI 54LS261 (4 x 2, 2's complement)

Analog-to-Digital Converters

- TRW ADC-04
- Precision Monolithics AD-02
- Micro Networks MN333 (0° to 70°C only)

Digital-to-Analog Converters

- Precision Monolithics DAC-08
- Precision Monolithics DAC-100
- Micro Networks MN333 (0° to 70°C only)

### Operational Amplifiers

- Harris HA2520
- RCA CA108A
- National Semiconductor LM108A

### Analog Switches

- 2N4856
- 2N4859
- 2N3970
- 2N4091

# HYBRID RECEIVER-PHYSICAL AND OPERATIONAL CHARACTERISTICS

## PHYSICAL CHARACTERISTICS

- SIZE 15.24 x 22.86 x 17.77 cm\*  
(6 x 9 x 7 in)
- WEIGHT 4.31 kg\* (9.5 lbs)
- PWR CONSUMPTION 12 WATTS
- RELIABILITY 0.941/UNIT  
0.997/PAIR

\* DUAL RECEIVER CONFIGURATION

## ENVIRONMENTAL CHARACTERISTICS

- TEMPERATURE -20°C/+60°C
- VIBRATION AND SHOCK SHUTTLE LAUNCH ENVIRON.
- HUMIDITY 0 TO 85%
- PRESSURE SEA LEVEL/10<sup>-8</sup> torr
- MAGNETIC CLEANLINESS 10mT/0.5m
- RADIATION 200KRAD (SI)

## INTERFACES

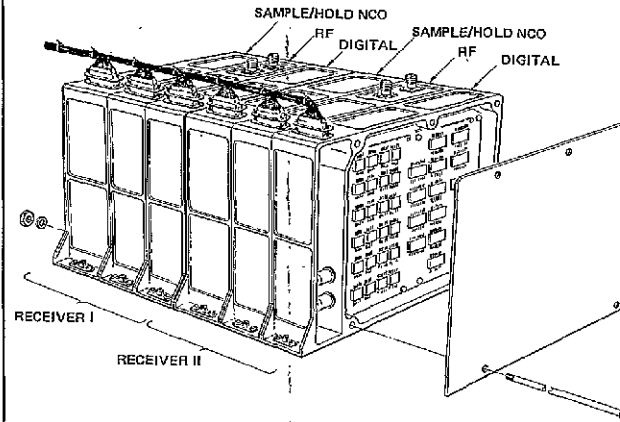
### ● INPUTS

RF SIGNAL  
DC POWER  
ON/OFF CONTROL  
OPERATIONAL CONTROL  
DEMODULATED DATA  
STATUS INFORMATION  
RADIO SCIENCE DATA  
TEMPERATURE AND CURRENT TLM  
BUFFERED TCXO

### ● OUTPUTS

## FEATURES

- FIXED RF/IF GAIN -- NO AGC
- DIGITAL FREQUENCY GENERATION -- NO VCO
- IF SAMPLING -- NO IQ BALANCE PROBLEMS
- SEQUENTIAL DETECTION FOR RAPID ACQUISITION
- DIGITAL SIGNAL PROCESSING FOR IMPROVED PERFORMANCE



## SIGNAL CHARACTERISTICS

- FREQUENCY 991 TO 1011 MHz, 1 MHz INCREMENTS
- MAXIMUM FREQ UNCERTAINTY ±80 kHz
- MAXIMUM DOPPLER RATE ±50 Hz/SEC
- MINIMUM SIGNAL -146 dBm
- MAXIMUM SIGNAL (OPERATING) -115 dBm
- MAXIMUM SIGNAL (NO DAMAGE) -10 dBm

## ACQUISITION CAPABILITIES

- PROBABILITY OF ACQUISITION AT 4.5 dB E<sub>b</sub>/N<sub>0</sub> 0.995 IN LESS THAN 50 SEC
- PROB OF FALSE ACQUISITION 1 x 10<sup>-4</sup>

## DEMODULATION AND TRACKING CAPABILITIES

- MODULATION TYPES DPSK, CPFSK (SELECTABLE)
- BIT RATES 100, 200, 400, 1000 BPS (SELECTABLE)
- DEMODULATION PERFORMANCE WITHIN 1 dB OF THEORETICAL FOR P<sub>b</sub> BETWEEN 0.1 AND 1 x 10<sup>-6</sup>
- NON-COHERENT TRACKING <1 Hz RMS ERROR FOR 1 SECOND INTEGRATION TIME (STRONG SIGNAL)

## RADIO SCIENCE CAPABILITY

- SIGNAL POWER MEASUREMENT BETTER THAN 0.1 dB RESOLUTION
- FREQUENCY MEASUREMENT BETTER THAN 0.25 Hz RESOLUTION

FOLDOUT FRAME 1

FOLDOUT FRAME 2

Figure 1-1. Hybrid Receiver Physical and Operational Characteristics

# HYBRID RECEIVER-PHYSICAL AND OPERATIONAL CHARACTERISTICS

## PHYSICAL CHARACTERISTICS

- SIZE 15.24 x 22.86 x 17.77 cm\*  
(6 x 9 x 7 in)
- WEIGHT 4.31 kg\* (9.5 lbs)
- PWR CONSUMPTION 12 WATTS
- RELIABILITY 0.941/UNIT  
0.997/PAIR

\* DUAL RECEIVER CONFIGURATION

## ENVIRONMENTAL CHARACTERISTICS

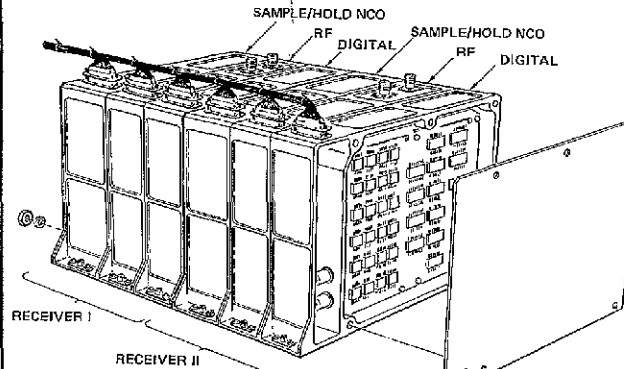
- TEMPERATURE -20° C/+60° C
- VIBRATION AND SHOCK SHUTTLE LAUNCH ENVIRON.
- HUMIDITY 0 TO 85%
- PRESSURE SEA LEVEL/10<sup>-6</sup> torr
- MAGNETIC CLEANLINESS 10nT/0.5m
- RADIATION 200KRAD (Si)

## INTERFACES

- INPUTS RF SIGNAL  
DC POWER  
ON/OFF CONTROL  
OPERATIONAL CONTROL
- OUTPUTS DEMODULATED DATA  
STATUS INFORMATION  
RADIO SCIENCE DATA  
TEMPERATURE AND CURRENT TLM  
BUFFERED TCXO

## FEATURES

- FIXED RF/IF GAIN - NO AGC
- DIGITAL FREQUENCY GENERATION - NO VCO
- IF SAMPLING - NO IQ BALANCE PROBLEMS
- SEQUENTIAL DETECTION FOR RAPID ACQUISITION
- DIGITAL SIGNAL PROCESSING FOR IMPROVED PERFORMANCE



## SIGNAL CHARACTERISTICS

- FREQUENCY 991 TO 1011 MHz, 1 MHz INCREMENTS
- MAXIMUM FREQ UNCERTAINTY ±50 kHz
- MAXIMUM DOPPLER RATE ±50 Hz/SEC
- MINIMUM SIGNAL -146 dBm
- MAXIMUM SIGNAL (OPERATING) -116 dBm
- MAXIMUM SIGNAL (NO DAMAGE) -10 dBm

## ACQUISITION CAPABILITIES

- PROBABILITY OF ACQUISITION AT 4.5 dB E<sub>s</sub>/N<sub>0</sub> 0.995 IN LESS THAN 50 SEC
- PROB OF FALSE ACQUISITION 1 x 10<sup>-4</sup>

## DEMODULATION AND TRACKING CAPABILITIES

- MODULATION TYPES DPSK, CPFSK (SELECTABLE)
- BIT RATES 100, 200, 400, 1000 BPS (SELECTABLE)
- DEMODULATION PERFORMANCE WITHIN 1 dB OF THEORETICAL FOR P<sub>b</sub> BETWEEN 0.1 AND 1 x 10<sup>-5</sup>
- NON-COHERENT TRACKING < 1 Hz RMS ERROR FOR 1 SECOND INTEGRATION TIME (STRONG SIGNAL)

## RADIO SCIENCE CAPABILITY

- SIGNAL POWER MEASUREMENT BETTER THAN 0.1 dB RESOLUTION
- FREQUENCY MEASUREMENT BETTER THAN 0.25 Hz RESOLUTION

Figure 4-1. Hybrid Receiver Physical and Operational Characteristics