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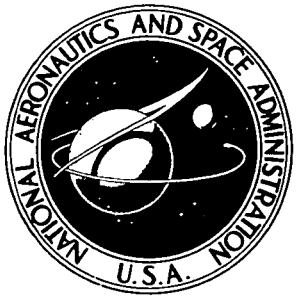

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INTEGRALLY REGULATED SOLAR ARRAY DEMONSTRATION USING AN INTEL 8080 MICROPROCESSOR

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON D. C. • JULY 1977

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA TM X-3566		

4. Title and Subtitle	5. Report Date
INTEGRALLY REGULATED SOLAR ARRAY DEMONSTRATION USING AN INTEL 8080 MICROPROCESSOR	July 1977
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
Edward J. Petrik	E-9144
	10. Work Unit No.
9. Performing Organization Name and Address	506-23
National Aeronautics and Space Administration Lewis Research Center Cleveland, Ohio 44135	11. Contract or Grant No.
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Technical Memorandum
National Aeronautics and Space Administration Washington, D.C. 20546	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

A concept for regulating the voltage of a solar array by using a microprocessor to effect discrete voltage changes was demonstrated. Eight shorting switches were employed to regulate a simulated array at set-point voltages between 10 000 and 15 000 volts. The demonstration showed that the microprocessor easily regulated the solar array output voltage independently of whether or not the switched cell groups were binary sized in voltage. In addition, the microprocessor provided logic memory capability to perform additional tasks such as locating and insolating a faulty switch.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Microprocessor; Digital control; Solar array; Power supplies; Switching circuits	Unclassified - unlimited STAR Category 20

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	16	A02

* For sale by the National Technical Information Service, Springfield, Virginia 22161

INTEGRALLY REGULATED SOLAR ARRAY DEMONSTRATION USING AN INTEL 8080 MICROPROCESSOR

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SUMMARY

A concept for regulating the output voltage of an integrally regulated solar array (IRSA) by using a microprocessor to effect discrete or incremental voltage changes was demonstrated. For this demonstration a conceptual solar array was simulated on an EAI PC-12 analog computer. The microprocessor was an Intel 8080.

For this demonstration the operating point of the simulated solar array was varied from 0 to 1 ampere at set-point voltages between 10 000 and 15 000 volts. A variable voltage from 0 to 5000 volts in approximately 20-volt increments is obtained with eight switches coded in a binary configuration and used to regulate the output voltage.

From the investigation it was determined (1) that the voltage regulation was maintained whether or not the switchable sections were binary sized in voltage, (2) that regulation was provided over the full current capability of the simulated solar array, and (3) that the major effort was defining the regulation algorithm in a way that efficiently utilized the capability of the microprocessor.

INTRODUCTION

Solar arrays made of silicon solar cells are the main source of electrical power for Earth satellites. The silicon cells used on these arrays are low-powered, low-voltage devices. Advanced satellites incorporating ion thrusters and high-frequency electron tubes have created a need for multikilowatt dc power supplies with 1000- to 16 000-volt outputs.

To meet these large power requirements, blocks of solar cells are connected in series and/or parallel to form manageable subunits of the total array. The specific design of the blocks depends on the load specifications, the extent of radiation degradation, the intensity of solar illumination, and the solar cell temperature. References 1 to 3 discuss the system configuration.

To provide fine control and regulation, these blocks of solar cells must be adjustable in their output, with sufficient resolution to satisfy the regulation accuracy requirements. This can best be achieved by varying the voltage-current (V-I) characteristics of given power blocks by control techniques that short out solar cell groups within the blocks. With these techniques the array output voltage is reduced by the voltage of the shorted group. By using a number of these shorting switches, each operating on a different block of solar cells, it is possible to regulate the array output voltage. Since each switch is either fully on or fully off, some form of digital control can be used to regulate the array power. Reference 4 describes some operational results obtained with a prototype solar array using this approach. Reference 5 describes a 40-watt experimental solar array that was regulated by shorting out combinations of series and parallel segments of the solar array.

The work described in this report was done to demonstrate that a solar array can be regulated by using a microprocessor to effect discrete voltage changes. Thus, the output voltage can be changed by a predetermined amount, rather than in incremental steps, equal to the operating voltage of the smallest block of cells. In addition, the microprocessor has the capability to make decisions and to store information. These features were demonstrated by means of a calibration algorithm and a faulty switch detection algorithm.

SYSTEM DESCRIPTION

A simplified diagram of an integrally regulated solar array is shown in figure 1. A voltage that is proportional to the solar array voltage is sensed by an analog-to-digital converter and fed to a microprocessor. The microprocessor determines if switching is necessary to maintain the desired voltage. Knowledge of the existing switch states is required and kept by the microprocessor.

IRSA Simulation

A solar array was not available for the IRSA demonstration. Therefore, the electrical characteristics of a solar array were simulated on an EAI PC-12 analog computer. The solar array described in this section should not be considered as a design configuration. Rather, it is only one of many possible conceptual configurations capable of delivering power to a load. A high-voltage solar array was assumed for this investigation. The unswitched section represented two-thirds of the array with an output power of 10 000 volts at zero current. The switchable array sections were divided into eight sections or blocks with a total output of 5000 volts at zero current. These eight blocks

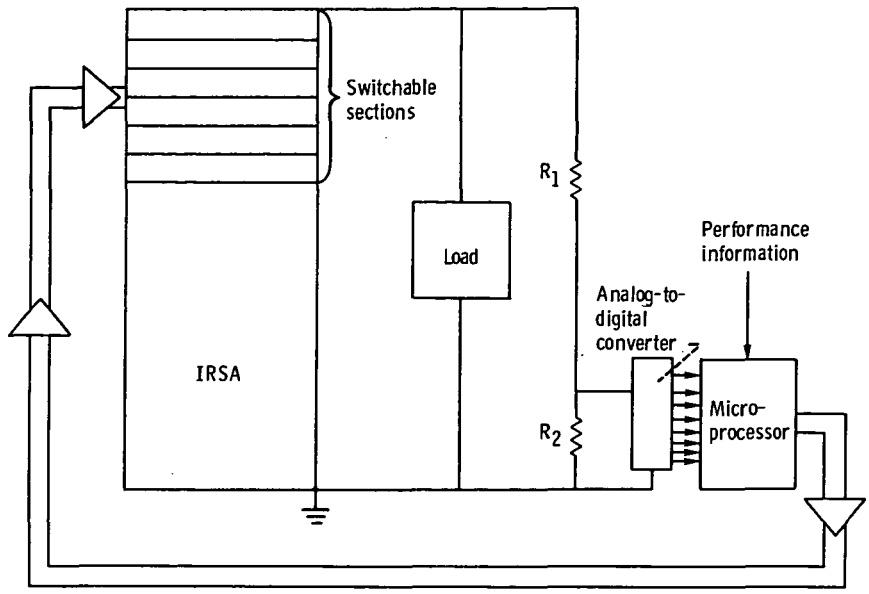

Figure 1. - Schematic diagram of conceptual integrally regulated solar array (IRSA).

were configured in two ways. For voltage regulation the eight switches were coded in a binary manner. The voltage blocks were grouped into voltage increments that corresponded to the weighted binary system, that is, 20, 21, ..., 27. With eight blocks, the smallest voltage increment was approximately 20 volts. For redundant switch testing, five switches were used to select the voltage blocks needed for voltage regulation. The smallest block voltage was approximately 160 volts. The remaining switches were used for redundant testing.

The shorting switches used for the simulation were hermetically sealed relays with mercury-wetted contacts. The contacts were the make-before-break type. High-voltage isolation was not needed for this investigation since the solar array was simulated. Figure 2 shows the V-I characteristic of the conceptual high-voltage solar array. The figure shows how the V-I curves are generated as additional series sections are added. By selecting the appropriate V-I curve, the voltage is regulated regardless of the load current.

To simulate the solar array V-I characteristics, a straight-line approximation was used. This is shown in figure 3. At the maximum-power point, the block can deliver 1 ampere of simulated current. Each switchable section and the unswitched section (fig. 1) are represented by a V-I curve that is written as

$$v = V - 0.2\,Vi$$

The analog diagram of the high-voltage solar array simulation is shown in figure 4.

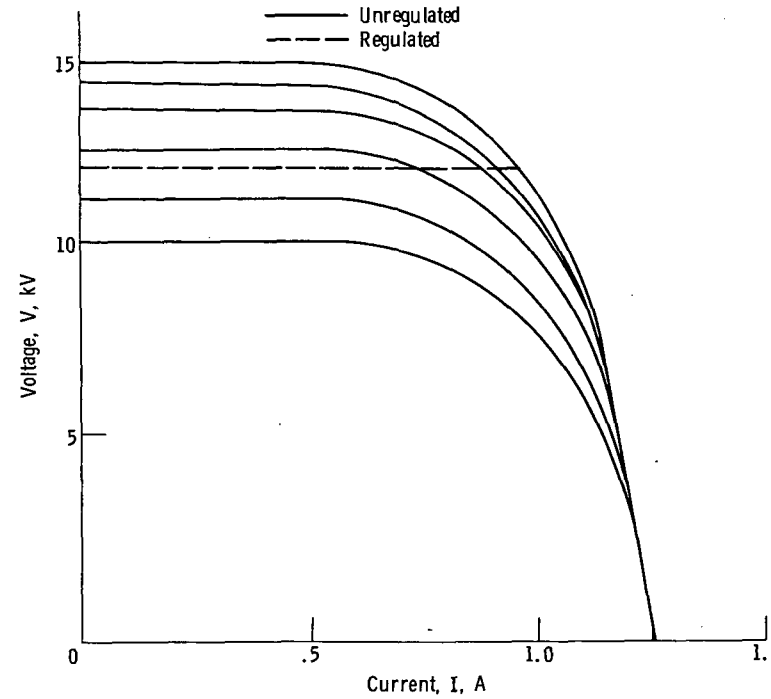

Figure 2. - Voltage-current characteristic of conceptual integrally regulated solar array.

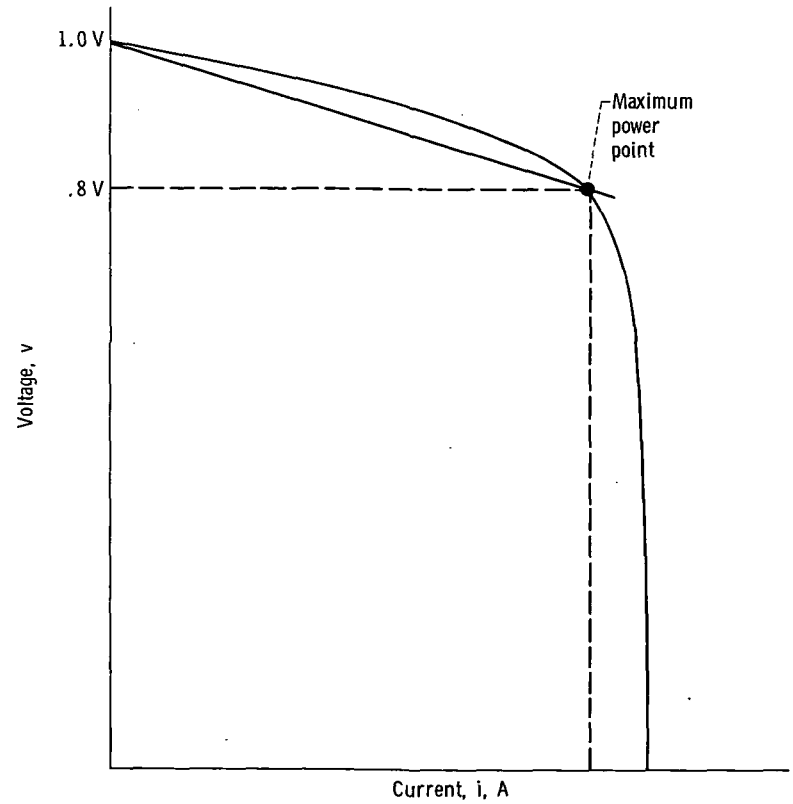

Figure 3. - Voltage-current characteristic of any switchable block of solar cells.

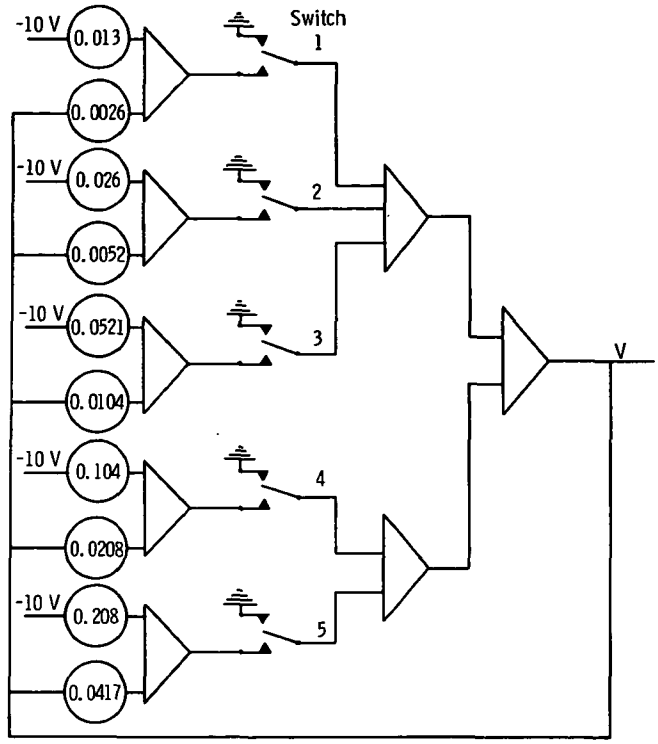

Figure 4. - Analog computer diagram for five switchable sections.

Microprocessor

The microprocessor used for this investigation was an Intel 8080. The Intel 8080 is an 8-bit microprocessor capable of directly addressing 64 000 bytes of semiconductor memory. The 8080 can be interfaced with as many as 256 input and 256 output devices and offers a 2-microsecond instruction cycle. Six, 8-bit data registers, an 8-bit accumulator, four temporary registers, and four testable flags are contained on the chip. The 8080 has a stack arrangement wherein any portion of external memory can be used as a last-in/first-out stack to store or retrieve the contents of the accumulator, the flags, or any data register. This permits virtually unlimited subroutine nesting and interrupt levels. Communication to and from the device is accomplished through a 16-bit address bus, an 8-bit bidirectional data bus, and various control lines. Microprocessor software consists of a total complement of 78 instructions.

As a part of the basic subsystem, a system clock was included. The system clock can give time-delay information from approximately 0.1 to 16 seconds. Using this clock makes possible automatic testing or control, where inputs and outputs must be timed at regular clock intervals. The desired time interval is entered into the clock's register by a computer output instruction. The clock will interrupt operation of the central

processing unit (CPU) when the programmed time interval has elapsed. A detailed description of the Intel 8080 microprocessor and its supporting equipment is given in the appendix.

Analog-to-Digital Converter

To provide versatility, a 16-input-line multiplexer with a high-performance, 12-bit, successive-approximation, analog-to-digital (A/D) converter was included in the microprocessor equipment. Each analog channel can accept an analog signal that varies from 0 to 5 volts. By using an analog multiplexer, the computer can select any of the 16 channels. The analog signal is then converted to digital form by using a 12-bit A/D converter and truncating the least significant four bits. The integrally regulated solar array demonstration uses only one analog channel.

ALGORITHMS

Algorithms are used by the microprocessor for assessing voltage regulation, calibration, and redundancy (locate and isolate switch failure). The power requirements of an integrally regulated solar array are determined by a specific mission. The simulated array is composed of nine blocks, eight of which can be shorted to obtain a desired regulated output voltage. The switchable sections can be configured to represent any number of voltage-weighting schemes, including a binary-weighted system. In addition, redundant sections can also be used in the simulation. The simulation is capable to operating at 0 to 15 000 volts.

Voltage Regulation

The initial investigation uses a very simple voltage regulation algorithm, represented by

$$N(k + 1) = N(k) + K^{*}\left[V_{ref} - V_{o}(k)\right] = N(k) + K^{*}E(k)$$

where

N 8-bit control word used to switch sections contributing to output voltage

k time step

K gain constant

V_{ref} reference voltage

V_o solar array output voltage

E error voltage

To implement this algorithm, it is assumed that the microprocessor has available (in memory) calibration data that are proportional to the voltage of each switchable segment. The algorithm requires that the data be stored in order of decreasing magnitude.

Using this control algorithm, as well as reference data that have been entered by the operator, the microprocessor computes an error signal that it then uses to update the last control word. In this manner, each iteration of the computer results in a new control input to the array switches. After some fixed time delay, during which the microprocessor is available for other tasks, the results of the iteration are available to the microprocessor for further evaluation and control.

Calibration

The calibration algorithm is used to measure the voltage of each of the switchable sections of the simulated array. The algorithm first measures the voltage of the unswitched section and then alternately switches in one section at a time. The voltage difference is computed by the microprocessor and stored in memory in order of decreasing magnitude.

Redundancy

Essential to the operation of an integrally regulated solar array are reliable dc switches. The effect of a shorting switch failure is either loss of voltage and power from that switchable section or loss of control of that section. In practice, the shunt switches will be power transistors. The worst transistor failure modes from a performance standpoint are open and short circuits. The most prevalent failure in a transistor is excessive leakage in the OFF mode. This effectively shunts the switchable section.

For this demonstration, it is assumed that a switch failure results in a complete loss of power in the section controlled by that switch. Redundant sections are added to the solar array to improve reliability. To demonstrate the effect of using redundant sections, redundancy was also added to the simulation.

When a switch fails in the shorted mode, regulation may be lost. This may cause the output voltage to oscillate. There are several algorithms that can locate and isolate a faulty switch.

The simplest algorithm is to remove the load from the solar array and recalibrate. This approach would locate and isolate the faulty switch. If there was a redundant section for the shunted faulty section, it would be used to continue regulation. If there was no redundant section, regulation would continue but at a loss of accuracy.

Another algorithm is to detect loss of regulation and then switch to a complete set of the redundant switchable sections for further regulation. This approach would not immediately isolate the faulty switch, but regulation would only be lost for the time that it takes the microprocessor to decide that regulation is lost. Later, at a more convenient time, the load could be removed, the switchable sections calibrated, and the faulty switch isolated.

In the particular algorithm demonstrated, the microprocessor detects the loss of regulation and immediately determines if the faulty switch has a redundant section available. If a redundant section is available, the faulty switch is not used again for regulation. This algorithm requires knowledge of the present switch setting and knowledge of the redundant sections that are available for regulation. With this information stored in memory, the microprocessor selectively switches out the primary sections and switches in the redundant sections. A change in voltage equal to the section voltage under test identifies the faulty switch. For this demonstration, three redundant sections were used.

RESULTS

The results of operating the simulated solar array under the control of a microprocessor show that regulating the output voltage was easily accomplished by the microprocessor using the simple algorithm discussed in the preceding section. Figure 5 shows the

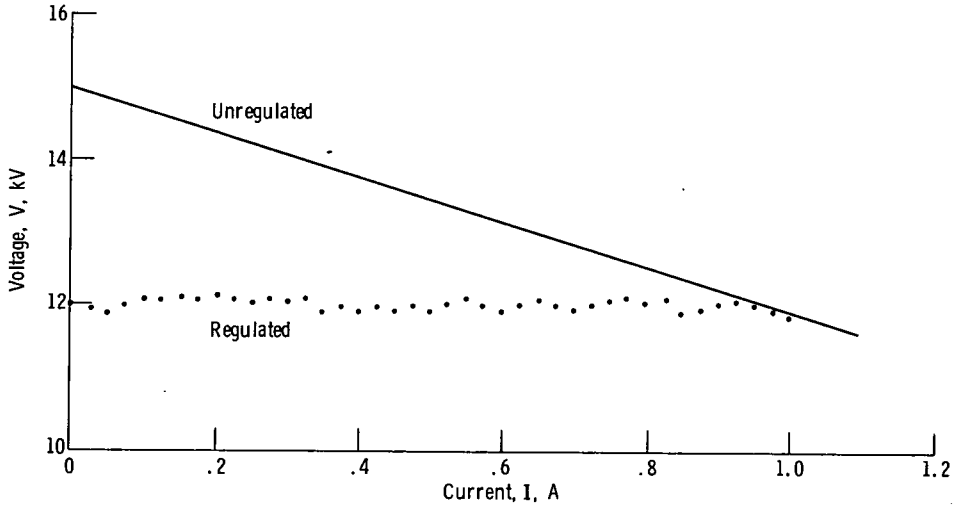

Figure 5. - Regulation characteristics obtained by microprocessor control.

regulation characteristics of the system at 12 000 volts. This figure was obtained by using the microprocessor and five shorting switches to regulate the output voltage. The voltage variations appearing in the figure are caused by discrete voltage changes as the state of the switches changes. With five switches, the smallest block voltage is approximately 160 volts. Therefore, the voltage variations are ±160 volts. To minimize this condition, either more voltage blocks with smaller voltages are needed or a proportional-plus-integral control law can be used.

One significant feature of this regulation algorithm is that the algorithm is independent of the size (V-I characteristic) of each switchable section. The algorithm determines which switches should be activated on the basis of the error that exists between the sensed output level and the desired output level. Since each switchable section is proportional to its actual voltage and since the microprocessor already knows which sections are being used, any existing error is corrected by appropriately adding the section that will reduce the error to zero. This means that switchable sections of the solar array can be set up in any coded manner such as a single, binary, trinary, or fully redundant weighted system.

Furthermore, the calibration algorithm and the redundant switch algorithm demonstrate the flexibility of using a microprocessor for regulating the output voltage of an integrally regulated solar array.

SUMMARY OF RESULTS

An integrally regulated solar array regulation concept that uses an Intel 8080 microprocessor to provide the logic necessary to activate the desired solar array sections was demonstrated. The solar array was simulated on an EAI PC-12 analog computer. The demonstration showed the following:

1. The voltage regulation was obtained independently of the relative size of the switchable sections. That is, voltage regulation was maintained whether or not the switchable sections were binary sized in voltage.

2. Regulation was provided over the full current capability of the simulated solar array.

3. A major effort was required to define the potential operational problem areas in such a way that they could be incorporated into the regulation algorithms - for example, locating and isolating a faulty shorting switch.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, May 3, 1977,
506-23.

APPENDIX - DESCRIPTION OF INTEL 8080 MICROPROCESSOR AND SUPPORTING EQUIPMENT

The Intel 8080 microprocessor requires controlling support, timing clock, memory, and input/output capabilities.

System Clock

To operate, the Intel 8080 requires a two-phase clock with high-level outputs. Voltage swing is from 0 to 12 volts with each clock phase held to nominal tolerances. Hardware to execute this timing consists of a crystal oscillator and a binary counter. The crystal frequency is eight times the desired CPU clocking frequency. Combinational logic in conjunction with the counter produces the pulse widths of the two clocking signals. A level shifter provides high-level clocking signals to the CPU. In addition to driving the level shifter, the two clocking phases that have been generated are used for timing other systems of the computer.

At the beginning of each machine cycle an 8-bit status word is strobed out of the CPU. By using the CPU synchronous pulse and phase 1 of the clock, this 8-bit word is captured by a latch. Information in the latch will remain for the duration of the machine cycle and alert supporting hardware as to the CPU's current intentions (input, output, memory read, interrupt acknowledge, etc.).

System Memory

Although this system is capable of addressing 64 000 bytes of memory, only a small amount of memory was purchased for this experimental system. The first 2048 locations are allocated to random access memory (RAM). Random access memory was implemented by using 16 chips, each of which is a 1024-by-1 bit of RAM. Eight chips were connected in parallel to provide a full 8-bit word. Control signals to the chips include a chip select and a read/write strobe. All memory is contained on separate plugable modules so that expansion or organizational changes of the system memory can be easily made. Programmable read-only memories (PROM's) of the 256- by- 8-bit type were purchased for the computer after prototyping was complete.

8212 Interface Ports

The 8212 is multimode in nature. It can be used to implement latches, gated buffers, or multiplexers. Thus, all of the principal peripheral and input/output functions of the microcomputer system are implemented with the 8212.

The 8212 input/output port consists of an 8-bit latch with tristate output buffers and and control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Input and Output Channels

The inputs and outputs of the computer consist of the following:

(1) Two 8-bit parallel input channels where the state of the input is determined by manually setting microswitches located on the real-time clock circuit card: The switches are directly coupled to 8212 interface ports. These inputs are used as testable sense switches or to change data.

(2) A system clock that will give time-delay information from approximately 0. 1 to 16 seconds: Use of this clock makes possible automatic testing or control, where inputs and outputs must be timed at regular clock intervals. The desired time interval is entered into the clock's register by a computer output instruction. The clock will interrupt the operation of the CPU when the programmed time interval has elapsed.

(3) Two 8-bit parallel outputs. These are merely outputs of two 8212 interface ports that can be addressed by the CPU.

(4) Two registers that display the two 8-bit parallel outputs by means of light-emitting diodes (LED's).

(5) Sixteen analog channels: Each analog channel can accept an analog signal that varies from 0 to 5 volts. The computer can select any of the 16 channels by using an analog multiplexer. The analog signal is then converted to digital form by using a 12-bit A/D converter and truncating the least significant 4 bits. The IRSA experiment used only one analog channel.

(6) A teletype input-output interface: The teletype can be used to load a program directly into memory or as an input-output device under computer control. When using the teletype to directly load or dump memory, it becomes necessary to generate a sequence of timing pulses that are used for loading, unloading, and incrementing address locations. These timing signals are generated with a one-shot integrated circuit. The following codes have been assigned to the various input and output channels:

1H	time-delay clock	5H	8-bit output channel 2
2H	8-bit switch input channel 1	6H	A/D input and output
3H	8-bit switch input channel 2	7H	interrupt priority mask
4H	8-bit output channel 1	8H	teletype input and output

Interrupt

The Intel 8080 has the built-in capacity to handle external interrupt requests. A peripheral device can initiate an interrupt simply by driving the processor's interrupt line high. The 8080 microprocessor honors interrupts on a priority basis. These priority and interrupt assignments are as follows:

Priority	Interrupt	Assignment
1	0	Control panel RESET
2	1	Time-delay clock
3	2	Teletype
4	3	A/D converter
5	4	Not used
6	5	Not used
7	6	Not used
8	7	Channel 1 and 2 output ready

In addition to vectored priority interrupt capability, a programmable interrupt mask has been implemented. Setting the mask allows the control program to determine the order in which multiple interrupts will be handled. If it is desirable to recognize another interrupt before service of the first is complete, the interrupt mask can be cleared.

System Control

The most complex subsystem of the computer is the processor control panel. The following functions were implemented in the design:

(1) Sixteen-bit address register capable of monitoring the address bus during the program execution or single-step mode

(2) Eight-bit data register capable of monitoring the data bus during the program execution or single-step mode

(3) Memory access mode, address, and data registers loaded by front panel switches so that the contents of the memory can be changed directly

(4) Contents of any memory location able to be examined with address and data registers

(5) Automatic increment of address register before a store or fetch operation

(6) Capability to disable the increment mode

(7) Three modes of operation: memory access, single step, and run

(8) CLEAR function for address and data registers

(9) Display of status latch contents

(10) Display of various CPU control lines

There are basically four major subdivisions of this control panel. They are visual display, address register, data register, and CPU timing control.

Visual display is accomplished by using LED's. The contents of the control panel address and data registers, as well as important computer control lines, are also displayed by means of LED's.

The address register function is accomplished by using D-type flip-flops. This permits the most efficient use of hardware and significantly reduces the number of gates needed to interface. Loading of the flip-flop by the front panel controls is accomplished by using the preset inputs. This method eliminates the need to use switch debouncers on all pushbuttons. The 16-bit address stored in the flip-flops is fed to a full adder, which produces the next incremented address values. When in the memory access mode, the flip-flop input is switched to this incremented value and updated when the INCRADD signal goes low. While in the run or step mode, the address bus data are latched at the beginning of each clock cycle. Only during the memory access mode does this entire register gain control of the address bus when the CPU is disabled.

The control panel data register is very similar to the address register. Preset inputs are used for front panel inputs. The data bus is monitored by control panel data register flip-flops. When in the memory access and store modes, the outputs of the register are channeled to the data bus so that the contents can be transferred to memory. When in the fetch mode, a high-to-low transition of LDOPFF will latch contents of the data bus.

Control panel timing and mode control are important for proper operation of the computer. To enter the memory access mode, a three-position toggle switch is positioned to memory access and a hold is issued to the CPU. Half a cycle after the CPU has honored the hold, the control panel will enter the memory access mode. When in the step mode, the hold signal is released, and the control panel gains control of the CPU ready line. Proper control of this ready line makes it possible to single step a program one machine cycle at a time. When in the run mode, both the hold and ready lines are released so that normal program execution can occur. During a control-panel store or fetch, a number of operations must sequence through at proper times. Located on the teletype interface are two one-shot pulse circuits. These circuits provide the timing re-

quired to read or write memory from the control-panel console. The fetch and store operations proceed as follows:

Fetch mode:

(1) The contents of the address register are incremented if the increment switch is on.

(2) Approximately 1 microsecond later, data from memory are latched into the control-panel data register.

Store mode:

(1) The contents of the address register are incremented if the increment switch is on.

(2) Approximately 1 microsecond later, the contents of the data register are transferred to memory.

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