ERDA/JPL-954405-77/6
Distribution Category UC-63

AUTOMATED ARRAY ASSEMBLY TASK
PHASE I

Texas Instruments Report No. 03-77-31

Quarterly Report

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July 1977

JPL Contract No. 954405

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the U. S. Energy Research and Development Administration, Division of Solar Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

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SECTION I
INTRODUCTION

The overall goal of the Array Automated Assembly Task, Phase I, of the Low-Cost Silicon Solar Array Project is a comprehensive assessment of the processes, conceptual designs, and new technologies required to achieve, by 1985, annual solar cell array production capability greater than 500 megawatts per year at a cost less than $500 per kilowatt. This goal is being approached from two directions. The first is to build a model or models of the costs involved in the various steps used to fabricate solar cell modules. These costs are being analyzed in terms of present-day capabilities and projected capabilities. Also, new technologies will be fitted to these models to determine the cost ranges for solar cell processing using new or emerging technologies. The second approach is to determine the cost goals for each of the processing steps. The program will then undertake a series of studies that are intended to point the way from existing and projected costs to the cost goals. The design-to-cost concept will establish allowable costs for each cell manufacture/array assembly step consistent with the 1985 cost goals.

During this quarter, effort was concentrated on various aspects of a sensitivity analysis, in particular, on the impact of variations in metal sheet resistivity, metal line width, diffused layer sheet resistance, junction depth, base layer lifetime, optical coating thickness and optical coating refractive index and on process reproducibility for As diffusion from a polymer dopant source and on module fabrication. Model calculations show that acceptable process windows exist for each of these parameters. A follow-on program to define a 1982 factory will be initiated in the next quarter.

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SECTION II
TECHNICAL DISCUSSION

A. SENSITIVITY ANALYSIS

1. Approach

The objective of the sensitivity analysis is to determine the effects of process variables on the performance of the cell. The basis for judging cell performance is the power output of the cell in a standard array. The sequence of models which relate array parameters to process parameters is shown in Figure 1. Computer-aided process models are available[1] for determining impurity profiles as a function of times and temperatures. There are other process models, less clearly defined, for lifetime and diffusion length as a function of impurity gradients and processing temperature cycles.

Device models relate cell parameters to the physcical structure. The cell parameters of interest are the short-circuit current, I_{SC}, the open-circuit voltage, V_{OC}, and the series resistance, R_S. These are directly related to the elements of the equivalent circuit shown in Figure 2. The cell equivalent circuit is the basis for computing the output of an array of cells using circuit models such as SPICE.

In this task, we will use various computer programs to calculate cell parameters in terms of physical parameters. The efficiency components of Table I are an interim step in calculating the cell parameters.

Test patterns have been designed which will be fabricated as an integral part of the cell; physical parameters can be determined from measurements of these devices. Runs will be made in which the physical parameters are intentionally varied. Cell parameters will be measured to verify and refine the device models. Finally, the impact of practical process variations on the output of a cell in a system will be computed and experimentally measured.

2. Cell Design

A new cell pattern, shown in Figure 3, will be used for the sensitivity experiment. The metallization pattern for this cell was designed for the array assembly technique described previously, i.e., a triangular shaped bar, 0.3 cm on a side, is connected across a minor diagonal of

1. Shah, P., "Computer-Aided Process Design and Optimization for Semiconductor Device Fabrication," *Proceedings of the Third International Symposium on Silicon Materials Sciences and Technology, Semiconductor Silicon 1977*, 923-931.

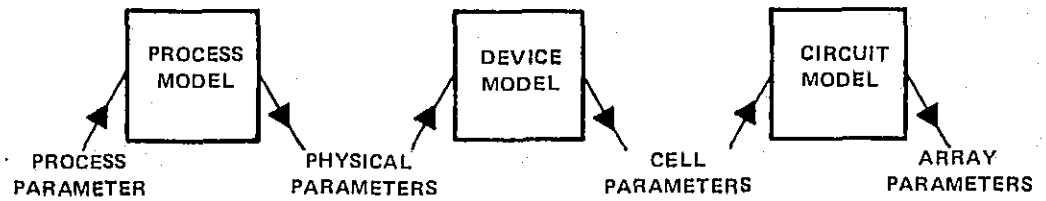

Figure 1. System of Models

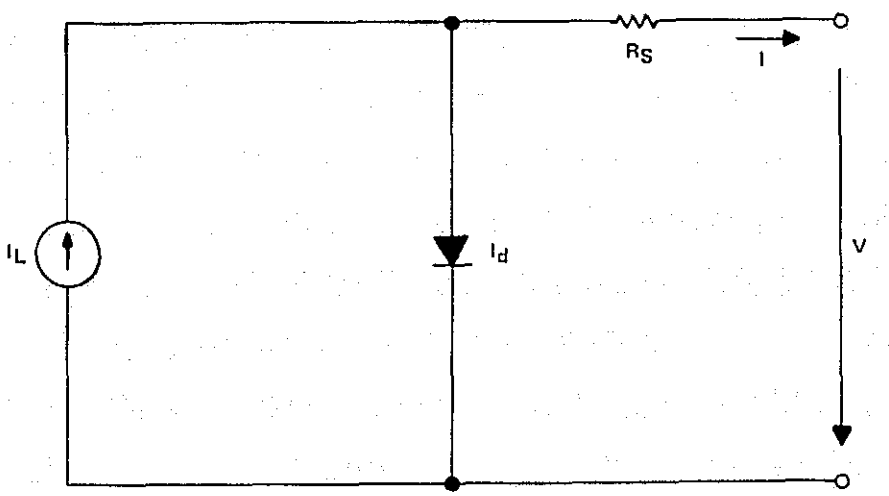

Figure 2. Basic Equivalent Circuit for Solar Cell

Table I. Dependence of Cell Parameters on Physical Parameters

Physical Parameter	Efficiency Component						
	Reflection	Metal Coverage	Collection-Diffused Region	Collection-Base Region	Voltage Factor	Fill Factor	Series Resistance
Insulator Thickness	X						
Refractive Index	X						
Finger Width		X					X
Metal Sheet Resistance							X
Metal Contact Resistance							X
Diffused Region Sheet Resistance							X
Junction Depth			X				
Base Resistivity					X		
Base Lifetime				X		X	

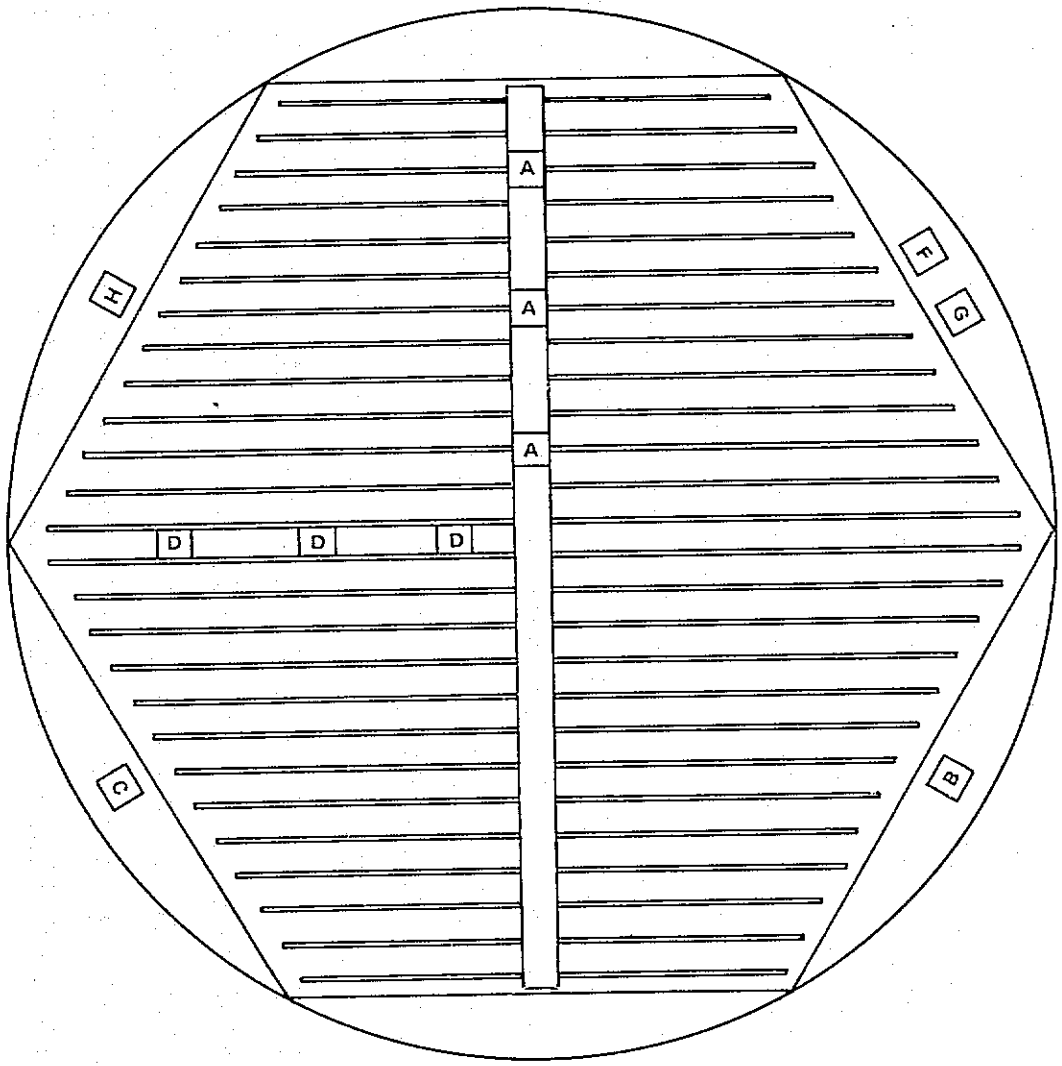

Figure 3. Layout of Cell and Test Devices

the 7.6-cm hexagon. A center trunk line is provided for connection to the bus bar and a fishbone array of fingers, 127-μm wide, feeds into this trunk line. Spacing between fingers varies slightly with distance from the center as required to minimize the sum of resistance and shadowing losses.

Test devices for measurement of physical parameters are fabricated within the cell. Locations of these devices are shown by letters on the cell pattern of Figure 3. The test devices are:

(A) Concentric pattern contacted to the diffused region (3 each)

(B) Parallel stripes contacted to the diffused region

(C) Metal pattern on top of oxide

(D) Diode (3 each)

(E) Spreading resistance contact to base region on back side (2 each)

(F) Small area solar cell with AR coating

(G) Small area solar cell with no AR coating

(H) MOS capacitor (2 each)

A picture of each test device (not to the same scale) is shown in Figure 4.

The purpose of devices (A) and (B) above is to measure the diffused region sheet resistance and contact resistance of the top side metallization. Device (B) has been used previously; diffused region resistance and contact resistance are easily separated since width of the stripes is small compared to spacing between stripes. However, this pattern cannot be used universally; e.g., in planar N on P cells, a P^+ guard ring would be required to prevent inversion of the P-type base material. Such a guard ring is not compatible with cell processing. The concentric ring pattern is more difficult to interpret because the transverse resistance under the metal contacts is significant. In theory, both diffused sheet resistance and contact resistance can be extracted from measurements between the four ring contacts. The parallel stripe pattern will be used to verify and calibrate parameters determined from the ring pattern. Three ring patterns allow measurement of resistance as a function of distance from center of the cell.

Two types of patterns are included for measurement of metal sheet resistance. One of the metal fingers of the main cell has four pads defined to denote 4-point probe locations for resistivity measurements. This is the preferred test pattern since essentially no space is lost from the cell. However, shunting by the diffused region will cause some inaccuracy. A second 4-point probe pattern (C) is included in one of the peripheral segments. This metal pattern is deposited over the oxide so that the diffused region does not shunt the current path. The latter pattern will be used to check accuracy of sheet resistance readings as measured on the metal finger patterns.

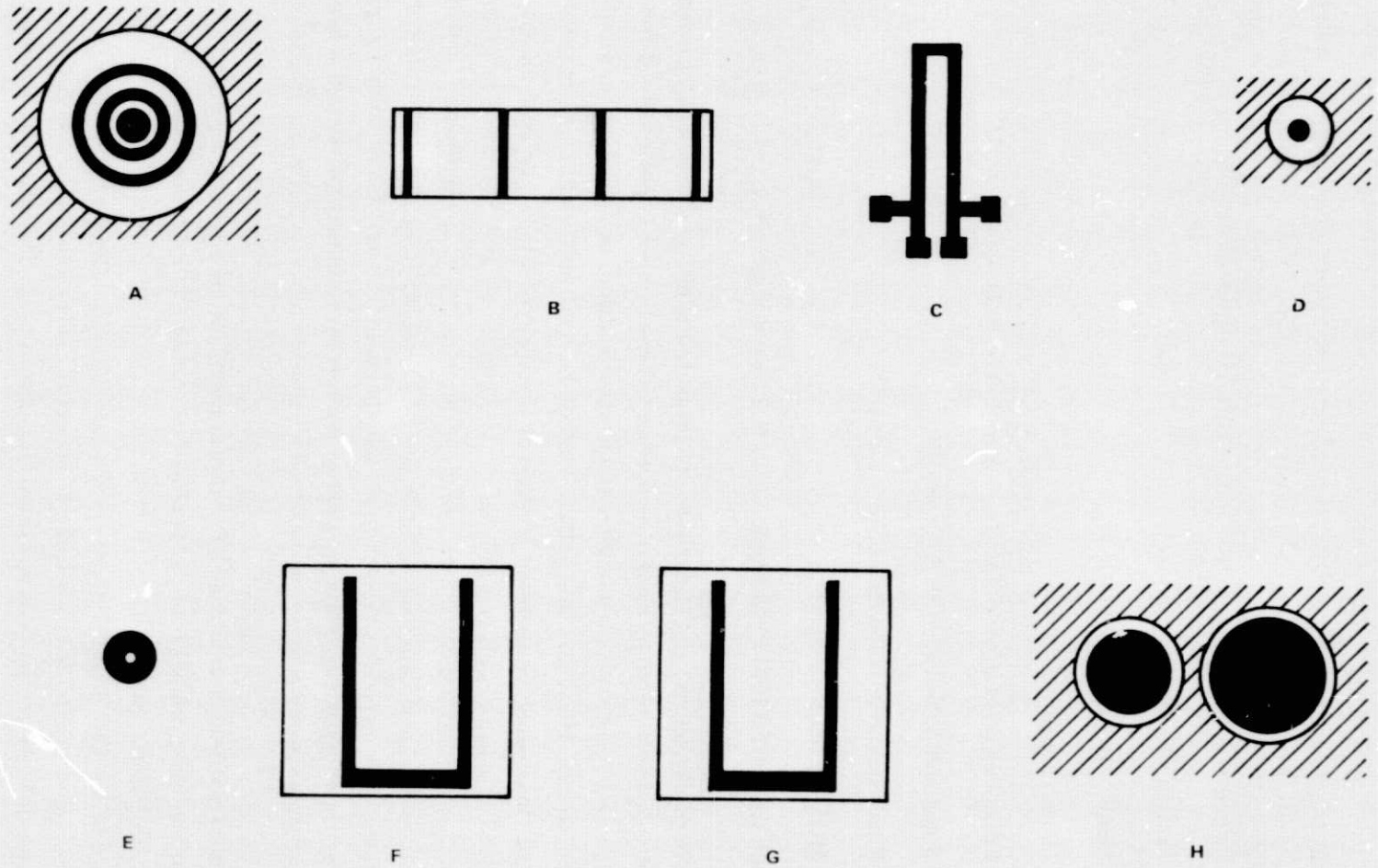

Figure 4. Test Devices

Small area diodes (device D) are included in the active portion of the cell to give convenient measurement of cell parameters, such as recovery time and dark IV characteristics. The diode area is 10^{-3} cm^2 for ease of calculating current densities. There are three diodes at varying distances from the center of the cell.

Spreading resistance contacts (device E) are patterned in the back side metallization. After back side metal and before sintering, a concentric circular section is etched away to leave a 0.005-cm diameter contact. Sintering provides ohmic contact for the measurement of spreading resistance R_{SP}. Then base resistivity can be calculated from the expression

$$R_{SP} = \rho_B \frac{1}{2d}$$

where d is the diameter of the contact; i.e.,

$$\rho_B = 0.01\ R_{SP}$$

Two small area solar cells are located in a peripheral segment. The area of each cell is 10^{-2} cm^2. One of the cells, device F, has the same AR coating as the large cell. Open-circuit voltage, short-circuit current density, and fill factor for this small area cell should approach those of an ideal cell. The second cell (device G) is identical except that there is no AR coating. Short-circuit current density for an optimized cell can be projected from measurements of this cell. Comparison with the AR cell gives an evaluation of the AR coating effectiveness.

Two MOS capacitors (pattern H) are included in another peripheral segment of the cell. Areas are 10^{-1} and 2×10^{-1} cm^2. For the planar cells, measurements of surface states may give useful information on excess diode currents or surface recombination velocity.

Seven mask levels have been designed for versatility of processing. The levels required for the different patterns and for various process alternatives are shown in Table II. Level three is for back side patterning; all other levels are for the front side.

Both N on P and P on N cells can be processed with either planar or mesa junctions. Level one defines the diffusion area for planar cells; level seven protects the cell when a mesa junction is etched. For planar P on N cells, level two protects the oxide over the junction during boron deglaze. Level four is for cutting contacts when the AR coating is applied before metallization. Level five is

Table II. Mask Level/Test Pattern Matrix

Mask	Level	7.6 cm Hex	N on P	P on N	Planar								Mesa							
					A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H
$N^+(P^+)$ Diffusion	1	X	X	X		X		X		X	X									
Deglaze OR	2	X				X		X		X	X									
Al Etch	3	X	X	X					X								X			
Contact OR	4	X	X	X	X	X		X		X	X		X	X		X		X	X	
Metal Definition	5	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X
Overcoat OR	6	X	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X
Mesa Etch	7	X	X	X										X		X		X	X	

Concentric Ring
Contact Stripes
4 PT – Metal
Diode
Spreading Resistance
Small Cell AR
Small Cell W/O AR
MOS Capacitor

Concentric Ring
Contact Stripes
4 – PT Metal
Diode
Spreading Resistance
Small Cell AR
Small Cell W/O AR
MOS Capacitor

used for metal definition in all process variations. For the case where AR coating is applied after metal, level six is used to expose metal pads; however, level six is needed in all cases to remove AR coating from one of the small test cells (device G).

Cells have been processed as 7.6-cm circular slices. Initial cell testing is in progress.

3. Metallization and Sheet Resistance Losses

Earlier in this contract, a computer program was developed to optimize the spacing between metal fingers and calculate the losses due to the metallization pattern. A similar analysis will be used here to calculate variation of shadowing and series resistance loss components with changes in processing parameters.

The metallization fingers are in a "fishbone" pattern as shown in Figure 3. Dimensions for a representative segment of the cell are shown in Figure 5. The width, T, of the fingers is constant; finger length, L, varies with distance of the finger from the center axis of the cell. The spacing, S, is optimized for each finger length to minimize the sum of resistive and shadowing losses.

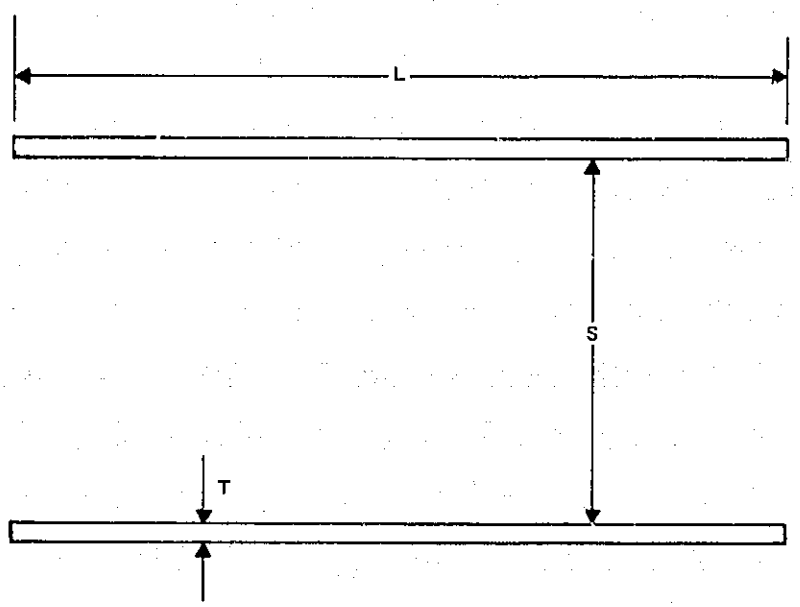

Figure 5. Representative Segment of Solar Cell

For this analysis it is assumed that the cell can be represented by a simple lumped model like that of Figure 2. In terms of this model, the power loss due to shadowing results form an increment, I_Δ, in the light-generated current I_L. Resistive loss is represented by an effective series resistance, R_S, defined by the relationship

$$R_S = \frac{P_R}{I^2} \tag{1}$$

where

P_R = the resistive power loss

I = the output current

For a single segment (Figure 5), the resistive losses in the diffused layer, P_D, and in the fingers, P_F, are

$$P_D = \frac{1}{12} J^2 r L S^3 \tag{2}$$

$$P_F = \frac{1}{3} J^2 \frac{M}{T} L^3 S^2 \tag{3}$$

where

r = sheet resistance of the diffused layer

M = metal sheet resistance

The output current per unit area is

$$J = I/A_T \tag{4}$$

Where A_T, the total cell area is

$$A_T = \sum_{j=1}^{n} Lj\,(T + Sj) \tag{5}$$

The total series resistance loss is calculated by summing loss components for all segments, i.e.,

$$P_R = S_D + S_F \tag{6}$$

where

$$S_D = \Sigma P_D \tag{7}$$

and

$$S_F = \Sigma P_F \tag{8}$$

From equations (1) through (8) the series resistance is

$$R_S = K_D\, r + K_F \frac{M}{T} \tag{9}$$

where

$$K_D = \left(\sum_{j=1}^{n} \frac{1}{12} L_j\, S_j^3\right) / \left(\sum_{j=1}^{n} L_j\, [S_j+T]\right)^2 \tag{10}$$

and

$$K_F = \left(\sum_{j=1}^{n} \frac{1}{3} L_j^3\, S_j^2\right) / \left(\sum_{j=1}^{n} L_j\, [S_j+T]\right)^2 \tag{11}$$

From a similar analysis, the increment, I_Δ, in light-generated current, I_L, due to coverage by the metal fingers is

$$I_\Delta = (I_L)\,(T)\,K_C \tag{12}$$

where

$$K_C = \sum_{j=1}^{n} L_j \Big/ \sum_{j=1}^{n} (L_j)\,(S_j+T) \tag{13}$$

The constants, K_D, K_F, K_C, determined from geometrical calculations for the pattern of Figure 3 are

$$K_D = 0.0001017$$

$$K_F = 0.01585 \text{ cm}$$

$$K_C = 4.23 \text{ cm}^{-1}$$

In Figures 6, 7, and 8, variations of series resistance and I_Δ, an increment of the light-generated current lost due to shadowing, are plotted as a function of process variables. I_Δ is used since this is a more sensitive measure of loss in the light-generated current. The process variables in Figures 6, 7, and 8 are diffused sheet resistance, metal sheet resistance, and finger width, respectively. Only one parameter is varied in each case. Variations of series resistance and light-generated current are normalized with respect to their values for the design value of the process parameters, i.e.,

$$r = 80 \text{ ohms/square}$$

$$M = 0.0033 \text{ ohms/square}$$

$$T = 0.0127 \text{ cm}$$

From inspection of Figure 6, it is evident that diffused sheet resistance has no effect on light-generated current—ignoring effects of lower lifetime in the diffused region—and exerts a direct linear impact on series resistance. A change of 20%, 16 Ω/□, in the diffused sheet resistance causes a change of 12%, 1.4×10^{-3} Ω, in the series resistance. This magnitude change in the series resistance, R_S causes a negligible change in cell performance. Therefore, control of diffused sheet resistance within ±20% of the nominal value is more than adequate for solar cell process control.

From inspection of Figure 7, it is evident that metal sheet resistance has no effect on light-generated current as expected. Series resistance is directly related to metal sheet resistance. An increase of 50% in metal sheet resistance causes an increase of 17%, 2×10^{-3} Ω, in series resistance, R_S, resulting in a negligible change in cell performance. Therefore, control of diffused sheet resistance within ±25 to 50% of the nominal value is more than adequate for solar cell process control.

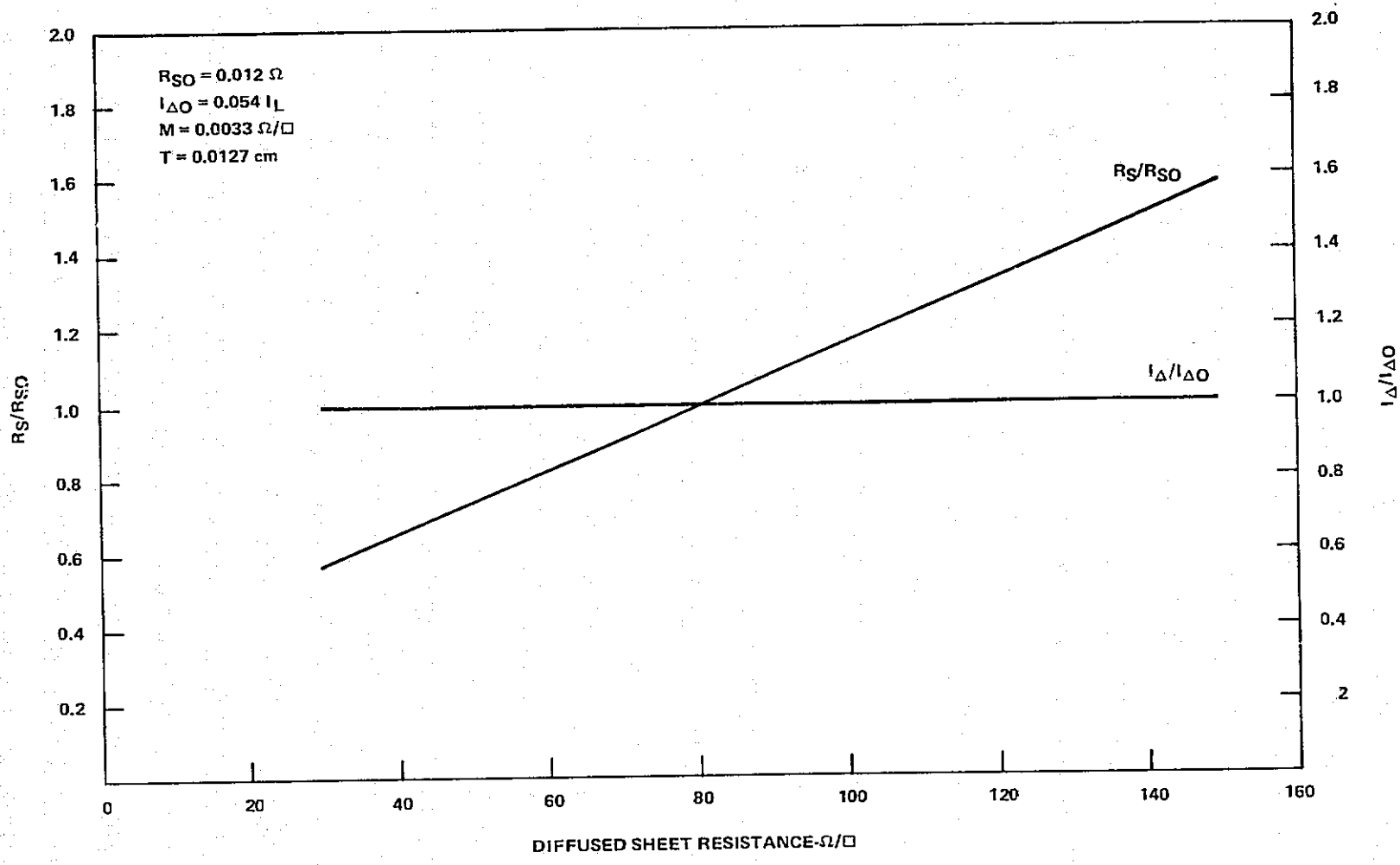

Figure 6. Variation of Series Resistance and Light-Generated Current with Diffused Sheet Resistance for Constant Metal Sheet Resistance and Finger Width

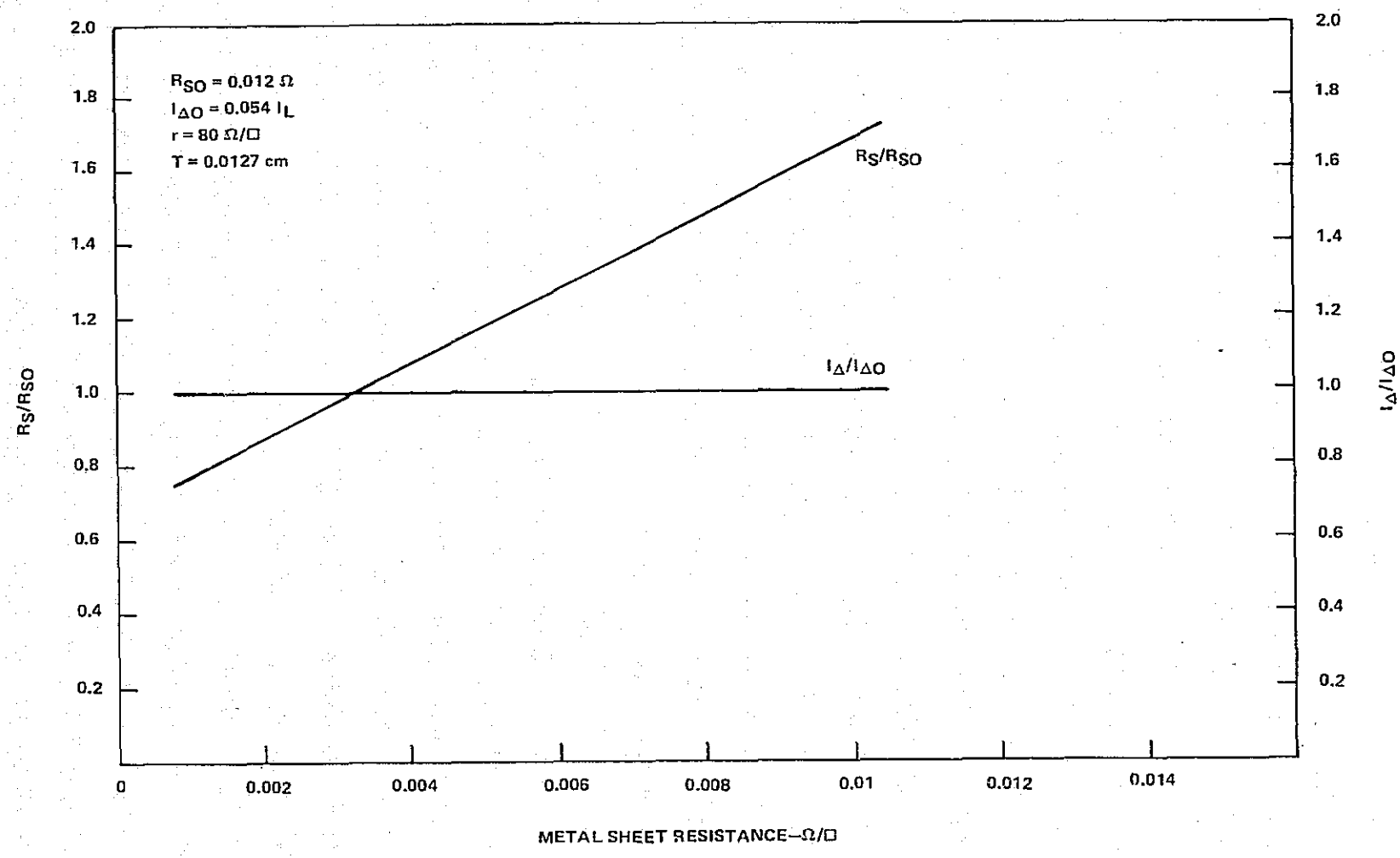

Figure 7. Variation of Series Resistance and Light-Generated Current with Metal Sheet Resistance for Constant Diffused Sheet Resistance and Finger Width

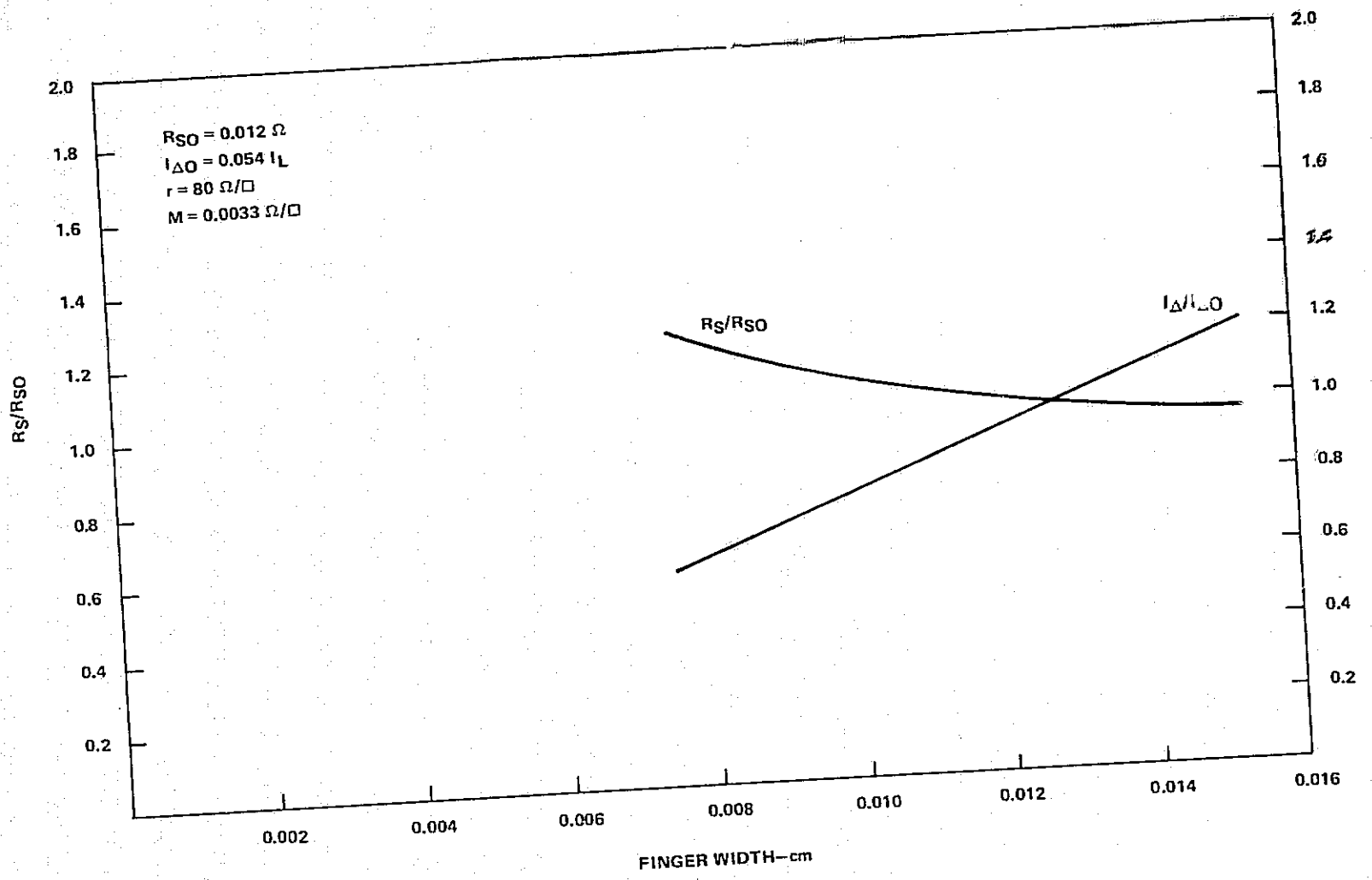

Figure 8. Variation of Series Resistance and Light-Generated Current with Finger Width for Constant Diffused Sheet Resistance and Metal Sheet Resistance

From inspection of Figure 8, it is evident that both I_Δ and R_S/R_{SO} change with changes in metal finger width. The changes in I_Δ and R_S/R_{SO} are of opposite sign and tend to compensate one another. For a decrease of 25 μm in finger width, I_Δ decreases 20% ($I_{SC} = I_L - I_\Delta$, I_{SC} increases $\approx$ 1%) and R_S/R_{SO} increases $\approx$8%, 1×10^{-3} Ω. These compensating changes result in negligible change in cell performance. Therefore, control of metal finger width within $\pm$25 μm at a nominal width of 127 μm is more than adequate for solar cell process control.

In summary, diffused sheet resistance, metal finger resistance and metal finger width are not sensitive variables in the control of a silicon solar cell process. The control evaluation should demonstrate whether specific process controls are required.

4. Carrier Generation

In order to examine the sensitivity of photogenerated carrier generation to processing variables in a solar cell process, a computer program has been written to determine generation rate and number of carriers at a given depth within a silicon solar cell when the characteristics of the silicon and the antireflection (AR) coating are changed. From Lambert's Law, the number of absorbed photons with wavelength between λ and $\lambda + d\lambda$ in a layer of thickness dx is

$$U(\lambda) = \alpha(\lambda)\, N(\lambda) \exp[-\alpha(\lambda)\, x]\, dx, \tag{14}$$

where

$\alpha(\lambda)$ = absorption coefficient

$N(\lambda)$ = number of incident photons at wavelength λ

The total number of carriers generated as a function of depth is given by

$$N(t) = \int_0^t \int_{\lambda_1}^{\lambda_2} \alpha(\lambda)\, N(\lambda) \exp[-\alpha(\lambda)\, x]\, d\lambda dx \tag{15}$$

where

t = depth into the silicon

The number of incident photons on the surface of the silicon is modified by the presence of an AR coating.

Since the coating is ≈0.1 micrometer, absorption of the film is negligible. The transmissivity, T, of the AR coating is given by

$$T = 1 - \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos 2\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos 2\theta} \qquad (16)$$

where

$r_1 = 1 - n_1 / 1 + n_1$

$r_2 = n_1 - n_2 / n_1 + n_2$

$\theta = 2\pi t n_2 / \lambda$

n_1 = refractive index of the AR coating

n_2 = refractive index of silicon

θ = phase thickness of coating

t = thickness of coating

λ = wavelength of incident radiation

Initial calculations have been made with SiO as the AR coating. The variation of the refractive index of SiO is given in reference 2.

The computer program has been run to calculate carrier generation as a function of distance from the silicon solar cell surface for a range of SiO antireflection coatings ranging from 0 to 0.150 μm in thickness for 250-μm thick solar cells under AM0 conditions. The carrier generation is reported as a generated current density (J_G), that is the current density assuming no losses in the cell, 100% collection efficiency. Selected data is shown in Table III and each decade of distance is plotted as J_G versus SiO thickness in Figure 9. The absolute value of these numbers is no better than the accuracy of the solar flux and refractive index as a function of wavelength data. However the relative values are very good. These data, for AM0, are used to determine limits for junction depth and AR coating.

5. Junction Depth

The calculated J_G values in Table III assume ideal conditions in which all generated carriers can be collected. In practice, carriers generated in the diffusion layer have a lower probability of being collected than carriers generated in the base layer due to trapping, surface recombination and other loss mechanisms. Therefore it is useful to know how much of the generated current is in the diffused layer and how much is in the base region.

2. Hass, G. and Salzberg, C. D., *J. Opt. Soc, Am.* 44 (1954), 181.

Table III. Current Density Generation as a Function of Depth with SiO Optical Coating Thickness as a Parameter at AM0

t (μm)	100% Abs.	0	0.020	0.030	0.040	0.050	0.060	0.070	0.075	0.080	0.090	0.10	0.11	0.12	0.14	0.15
0.001	0.145	0.063	0.100	0.119	0.124	0.111	0.082	0.090	0.091	0.093	0.099	0.106	0.109	0.091	0.098	0.098
0.002	0.278	0.129	0.194	0.230	0.242	0.217	0.168	0.175	0.177	0.180	0.191	0.206	0.212	0.183	0.190	0.189
0.005	0.629	0.321	0.444	0.529	0.560	0.507	0.414	0.408	0.408	0.412	0.436	0.472	0.491	0.448	0.437	0.434
0.010	1.11	0.593	0.787	0.944	1.01	0.920	0.774	0.735	0.728	0.731	0.770	0.838	0.880	0.827	0.779	0.772
0.020	1.88	1.02	1.32	1.59	1.72	1.58	1.36	1.26	1.23	1.23	1.28	1.40	1.48	1.43	1.32	1.31
0.050	3.47	1.88	2.38	2.88	3.18	3.01	2.63	2.39	2.32	2.28	2.32	2.50	2.67	2.65	2.48	2.44
0.10	5.23	2.85	3.53	4.25	4.75	4.63	4.15	3.76	3.62	3.52	3.50	3.67	3.91	3.94	3.80	3.76
0.20	7.62	4.22	5.08	6.05	6.83	6.85	6.33	5.78	5.55	5.36	5.19	5.29	5.52	5.61	5.62	5.61
0.50	12.01	6.83	7.97	9.30	10.51	10.88	10.46	9.77	9.40	9.07	8.61	8.47	8.56	8.62	8.82	8.97
1.0	16.35	9.52	10.88	12.47	14.04	14.77	14.56	13.88	13.45	13.02	12.32	11.93	11.81	11.73	11.89	12.13
2.0	21.85	13.00	14.59	16.47	18.42	19.55	19.66	19.11	18.66	18.18	17.26	16.61	16.21	15.89	15.82	16.06
5.0	29.81	18.27	20.11	22.30	24.67	26.29	26.88	26.66	26.32	25.87	24.88	23.99	23.26	22.58	21.90	21.95
10.0	35.79	22.31	24.30	26.67	29.89	31.22	32.12	32.19	31.96	31.60	30.69	29.76	28.89	28.01	26.84	26.67
20.0	40.80	25.75	27.84	30.34	33.13	35.26	36.39	36.70	36.57	36.31	35.54	34.66	33.77	32.79	31.28	30.92
50.0	45.34	28.87	31.03	33.62	36.54	38.83	40.14	40.63	40.60	40.43	39.83	39.07	38.24	37.26	35.56	35.05
100.	47.61	30.43	32.62	35.24	38.22	40.57	41.96	42.54	42.55	42.43	41.91	41.24	40.46	39.51	37.78	37.22
200.	49.26	31.56	33.77	36.42	39.43	41.83	43.27	43.91	43.96	43.86	43.41	42.79	42.07	41.14	39.42	38.83
250.	49.69	31.85	34.07	36.73	39.74	42.15	43.61	44.27	44.32	44.24	43.80	43.20	42.48	41.57	39.85	39.25
J_G/J_{G0}	1.000	0.641	0.686	0.739	0.800	0.848	0.878	0.891	0.892	0.890	0.881	0.869	0.855	0.837	0.802	0.790
$J_G/J_{G\ 0.075}$		0.719	0.769	0.829	0.897	0.951	0.984	0.999	1.000	0.998	0.988	0.975	0.958	0.938	0.899	0.886
0.28	9.06	5.06	6.02	7.12	8.05	8.18	7.67	7.06	6.77	6.53	6.27	6.30	6.49	6.59	6.69	6.73
0.30	9.38	5.25	6.23	7.36	8.32	8.47	7.97	7.34	7.05	6.80	6.51	6.52	6.71	6.81	6.92	6.97
0.32	9.68	5.43	6.44	7.58	8.58	8.76	8.26	7.62	7.32	7.06	6.75	6.74	6.92	7.02	7.15	7.21

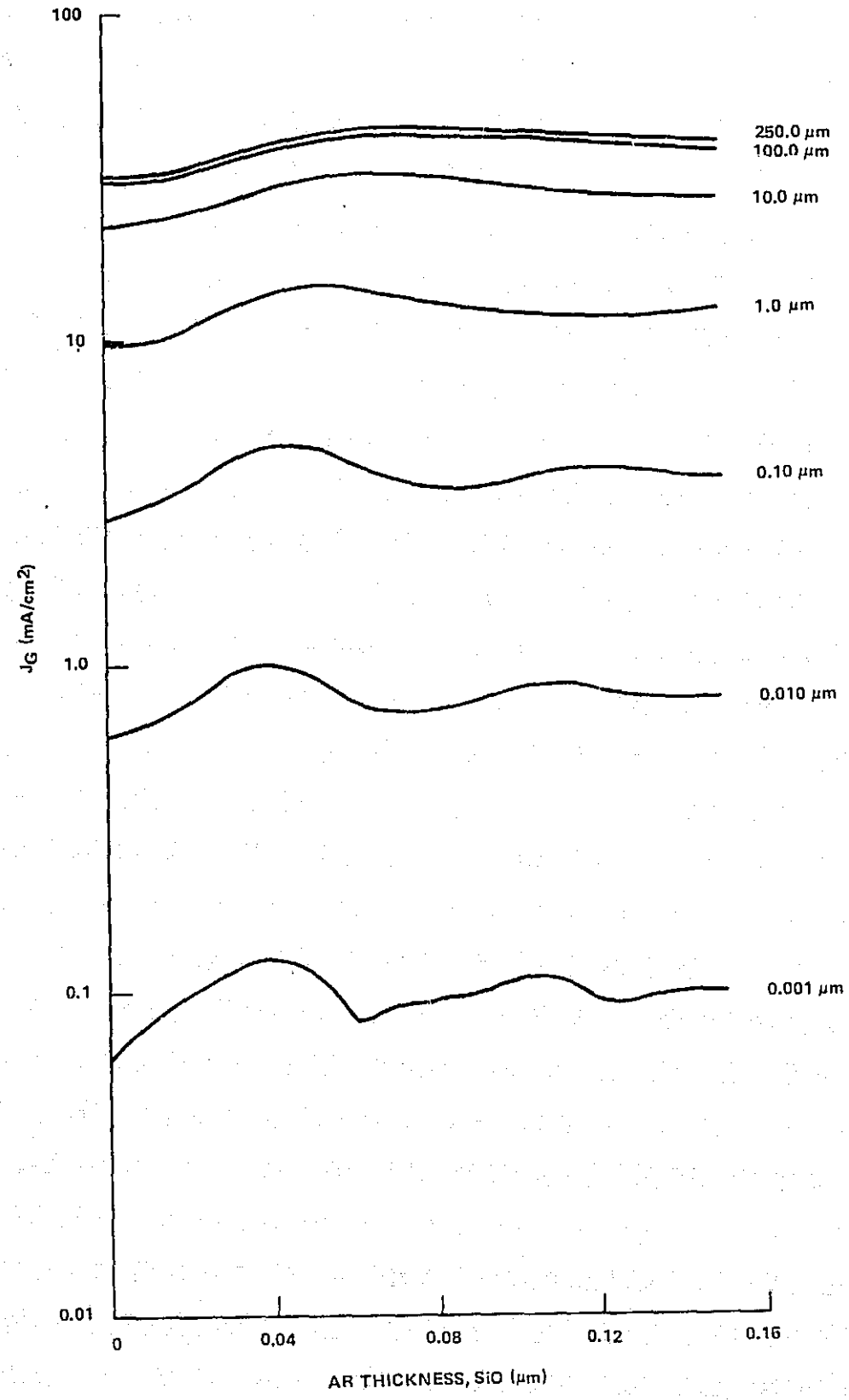

Figure 9. Sensitivity of J_G versus SiO thickness as a Function of Distance from the Surface under AM0 Illumination

From Table III, it can be seen that 15.9% of the total current density is generated in the top 0.30 μm, 12.5% in the top 0.20 μm and 8.2% in the top 0.10 μm of a cell that has a 0.075 μm SiO AR coating. This demonstrates the value of a very shallow front junction on a solar cell. The current generated in the diffused region does not represent a total loss but it does represent a low collection efficiency region.

The desire to work with the thinnest possible diffused layer must be balanced against the impact of higher diffused sheet resistance and metal contact alloy penetration. Optimum results appear to be achieved at junction depths in the region of 0.30 μm. At this junction depth, variations of $\pm$0.02 μm increase or decrease the current generated in the diffused layer by $\pm$0.6% for the 0.075 μm AR coating case. Junction depth control of 0.30 $\pm$ 0.02 μm is well within the control region for diffusion technology. Therefore diffusion depth does not appear to be a sensitive parameter. Normal sample testing of diffused sheet resistivity should be adequate to monitor junction depth.

6. Base Layer Lifetime

Base layer lifetime in the finished solar cell can be related to minority carrier diffusion length. Diffusion length must be sufficient to allow all carriers generated in the base material to be collected at the collecting junction. From Table III it is evident that carriers are generated at all depths in the solar cell, therefore effective collection length should be equal to or greater than the cell thickness. Collection lengths less than the cell thickness will result in significant loss of generated current, J_G to recombination. According to Fossum[3], typical resistivities employed in solar cell manufacture, 0.5 to 10 Ω-cm, exhibit diffusion lengths greater than or equal to cell thickness.

Control of the base layer lifetime is very complex. Many factors are involved including impurity levels in the silicon sheet material, particularly heavy metals, thermal history and defects. Relationships between these factors and base layer lifetime are not quantitatively understood. Therefore quantitative sensitivity correlations are not possible.

The impact of low base lifetime is very easy to observe however. As base lifetime falls below a critical level, J_{SC} degrades. The cause of this lowering of J_{SC} is the loss of carriers generated deep in the base of the solar cell.

Base lifetime can be monitored using the surface photo voltage technique or diode recovery techniques. For a fixed, controlled fabrication process, base lifetime should remain relatively constant. Therefore measurement of base lifetime at the end of the solar cell fabrication process should afford sufficient process control.

3. Fossum, J. G., *Solid State Electronics*, Vol. 19 (1976), 269.

7. Optical Coating

The sensitivity of generated current density, J_G, to optical coating thickness is a function of the optical parameters of the coating (absorption and refractive index as a function of wavelength), the thickness of the coating and the incident solar spectrum. Table III is a compilation of J_G as a function of thickness for SiO in an AM0 spectrum. The data is plotted in Figure 9.

The optimum optical coating thickness is 0.075 μm. At this thickness, J_G is 44.32 mA/cm^2 for a 250-μm thick solar cell. Variations of $\pm$0.015 μm in coating thickness cause J_G variations of $\approx$0.6 mA/cm^2. The region of maximum J_G is relatively broad and normal process control should provide reproducible results. From Figure 9 or Table III, variations toward thicker films cause less degradation in J_G than variations toward thinner films.

The same calculations will be run for the AM1 spectrum in the near future. Only minor differences are expected. Similar calculations could be made for other potential optical coatings if the relevant optical parameters are available.

Since refractive index of optical materials varies with the wavelength in question, a simple correlation between refractive index and cell output is not possible. Qualitative treatment shows that high index ($\approx$2) materials are better than low index ($\approx$1.4) materials.

Since the control limits on the optical coating are reasonably broad, a simple color comparison can be used to monitor coating thickness. Either mechanical or visual monitoring is acceptable. Special in-line testing is not required.

8. Other Observations

The above treatment assumes a relatively flat surface on the solar cell. In practice, high-efficiency solar cells will probably use textured surfaces to further reduce reflection losses. Quantitative treatment of the textured surface case is beyond the scope of this study but qualitative assessments are possible. All calculations involving depth into the cell are relative to a flat surface with normal incident solar flux. The case for a textured surface would treat the path of the absorbed light ray as the depth so that textured surface solar cells behave as though they are thicker than planar surface cells. Any nonabsorbed radiation that strikes the back of the cell can be reflected back through the cell giving a fractional increase in J_G.

Front surface recombination does not appear to be a significant factor since only $\approx$2% of J_G is generated in the first 10 nm. Less than 1% of the J_G is generated in the last 1 μm of a 250-μm cell so back surface recombination is even less of a factor.

B. PROCESS CONTROL EXPERIMENTS

1. Diffusion

An As polymer dopant reproducibility test was conducted for a 5-day period. Six 5.0-cm wafers were run in one lot each day. At least five points on each wafer were measured with a 4-point probe. All diffusions were run at 1000°C for 90 minutes to produce a target diffused sheet resistance of 60 Ω/□. The same lot of polymer dopant was used for the entire test. The results of this test are summarized below:

Test Day No.	Lot Resistivity (Ω/□)
1	59.9
2	60.6
3	64.9
4	65.2
5	61.8
Avg.	62.5

The day-to-day variation is <10% deviation from the nominal target diffused sheet resistance of 60 Ω/□ and within ±5% of the average for the 5-day test.

Within a given day, the six wafers also showed good uniformity and reproducibility. Typical data for the individual wafer run on day two are given in Table IV. Variance and standard deviation are calculated using N-1 weighing. The diffused sheet resistivity across a typical wafer and from wafer to wafer within a run is well under ±10%.

This level of process reproducibility coupled with the low sensitivity of light-generated current and series resistance to diffused layer resistivity makes this process one that does not require stringent testing for process control. Spot testing on a sample basis should be used as a process monitor but regular in-line testing does not appear to be justified or cost effective.

C. MODULE FABRICATION

The porcelain enameled steel substrate and locking frame are the unique and key elements of the 20-year lifetime LSSA modules designed under this contract. The basic work during this reporting period has been to identify the critical material and process parameters which will influence the manufacturability, cost, and durability of the porcelain enameled components.

Table IV. Arsenic Reproducibility Test – 2nd Day
(Resistivity in Ω/□)

	Slice 1	Slice 2	Slice 3	Slice 4	Slice 5	Slice 6	Av. Ω/□
	60.7	60.6	60.7	60.7	60.5	60.4	60.6
	60.0	59.3	62.3	60.0	60.2	62.6	60.7
	61.7	60.7	59.7	60.8	60.0	61.5	60.7
	62.3	59.3	60.7	60.0	60.5	59.7	60.4
	61.4	59.6	60.5	59.6	59.8	59.0	60.0
Average	61.22	59.9	60.78	60.22	60.2	60.64	60.6
Range	60-62.3	59.3-60.7	59.7-62.3	59.6-60.8	59.8-60.5	59.0-62.6	
Spread	2.3 Ω/□	1.4 Ω/□	2.6 Ω/□	1.2 Ω/□	0.7 Ω/□	3.6 Ω/□	
Variance	0.797	0.486	0.892	0.262	0.095	2.053	
Std Dev	0.892	0.696	0.944	0.511	0.308	1.432	

Three vendors of porcelain enameled steel: Challenger Stamping and Porcelain Co., Grand Haven, Michigan; Vitreous Steel Product Works, Cleveland, Ohio; and The Jones Metal Products Co., West Lafayette, Ohio have been contacted to obtain design information and to do sample porcelain enameling. Also data has been obtained from the Porcelain Enamel Institute and discussions have been held with TI personnel with background in ceramics and enameling to collect pertinent information.

Porcelain enamel is fused to the metal substrates at temperatures ranging from 900°F to 1800°F, with 1400°F-1600°F being the most common range. These relatively high temperatures impart unique effects upon the materials used, one of the most important criteria for proper design of parts to be porcelain enameled is an understanding of the materials and their reactions in the high-temperature areas of processing. Three common grades of steel sheets used for enameling are enameling iron, cold-rolled and decarburized steel. Strict adherence to material thickness and design factors such as corner radiuses, holes, symmetry of design, accessibility to apply the frit, etc., is necessary for a suitable finished porcelain coating.

To gain design information, soft tooling and normal sheet metal bending practices were used to manufacture several 28 X 33 cm substrates and corresponding lock frames. Two of these formed substrates which are similar to Design III have been provided to each of the three vendors for their evaluation. These vendors will evaluate the design for suitability for large-scale manufacturing, its ability to accept and retain the porcelain. The samples will be evaluated for dimensional changes in enameling and for the dielectric characteristics of the coating. The information will be used to optimize the design of the components.

Connector designs suitable for outside environment have been evaluated and Sure Seam^{TM} Connectors developed by ITT Cannon have been ordered and will be used initially for module-to-module interconnection. This manufacturer claims that these sealed connectors satisfy all of the parameters defined by automotive/industrial standards including vibration, shock, temperature cycling, salt water spray and immersion, petroleum derivations and industrial gas. Connectors will be assessed for their ability to meet the 1985 cost goals.

Bus bars for cell interconnections are presently being fabricated from copper clad Invar. Strips with a square cross section have been split from a sheet of Invar and subsequently drawn into wire form through a series of dies. The Invar wire will then be electrodeposited with copper to a 25/75 ratio. Forming of the triangular cross section to the finished gage will be the final step.

Information has been gathered and vendors of condensation and IR soldering equipment have been contacted. The first of these two processes seems to be uniquely suited to solder relatively large size but delicate cell rows. "Condensation/vapor-phase reflow soldering is a unique process which uses the latent heat of a hot condensing saturated vapor on an assembly to provide precise temperature control and high heat transfer rates for soldering assemblies." Condensation soldering offers many advantages over other forms of soldering such as (1) rapid heating with the precise temperature control that protects heat sensitive components from thermal damage, (2) even heating of the entire assembly surface regardless of parts geometry, and (3) an inherently clean operation since only continuously distilled vapor contacts the assembly.

All testing equipment for monitoring environmental data has been identified and obtained. Some of the equipment is in need of repair and actions have been initiated to complete this task.

SECTION III
CONCLUSIONS AND RECOMMENDATIONS

Sensitivity analyses show that diffused sheet resistivity, metal line width, and metal sheet resistivity do not strongly affect I_{SC} or R_S.

Calculation of generation rate and generated current density, J_G, for SiO under AM0 illumination show that an optical coating of 0.075 μm ±0.015 μm is optimum. Current generation at either the front or back surfaces is <2% of J_G. Variations of ±0.02 μm at a junction depth of 0.3 μm has a very slight impact on J_{SC}.

Control experiments on diffused sheet resistivity control for polymer dopant As sources indicate excellent reproducibility.

A solar cell design incorporating a number of in-process test sites has been designed and cells fabricated.

SECTION IV
NEW TECHNOLOGY

No new technology was discovered or employed during this quarter.

SECTION V
PROGRESS SUMMARY

Figure 10 shows the current work plan status. All major activities are in progress. No major problems are apparent at present to prevent attaining the indicated milestones.

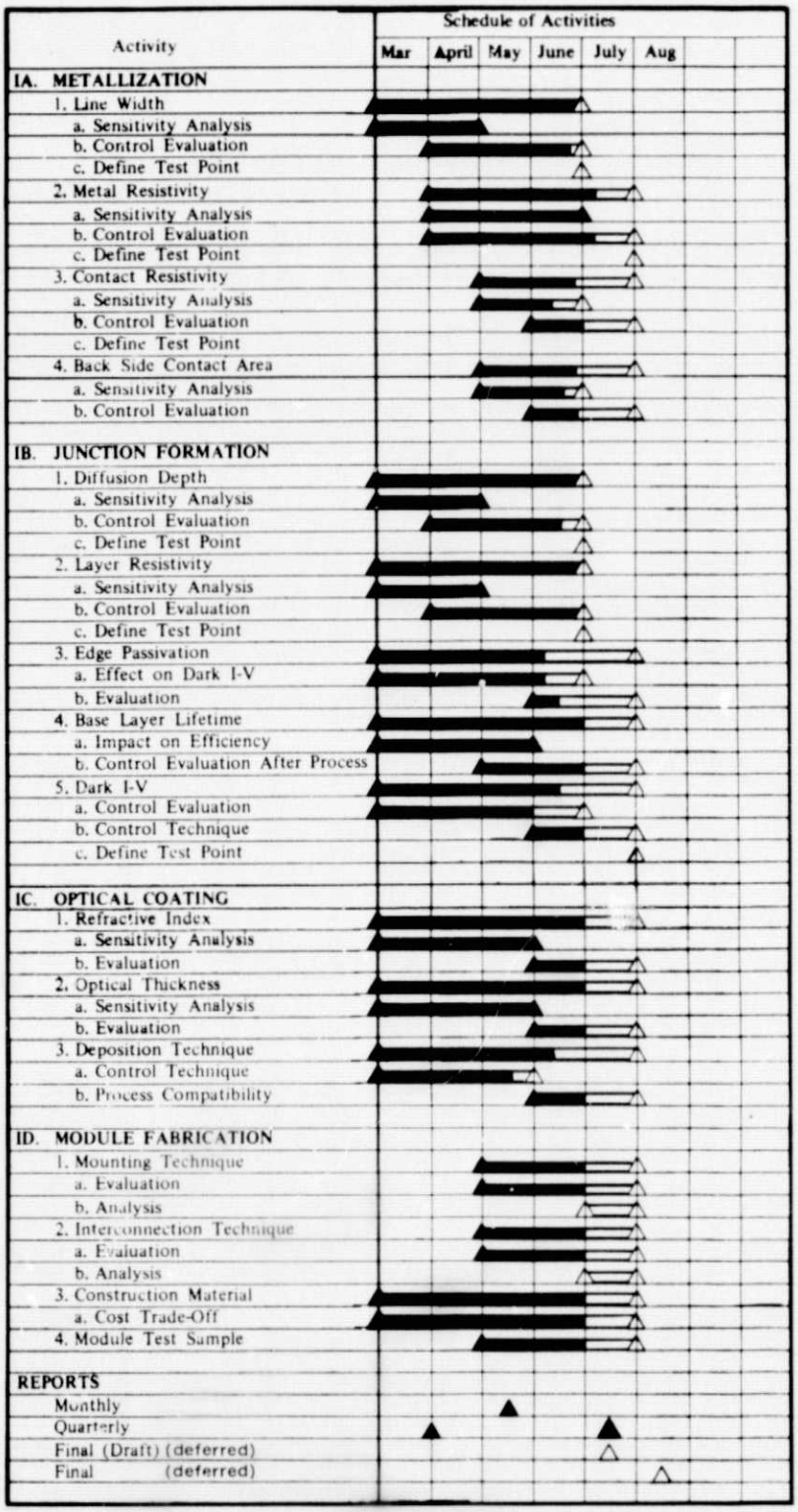

Figure 10. Work Plan Status