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Power Supply Sharing in the Apollo Telescope Mount Electrical Power System

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Power Supply Sharing in the Apollo Telescope Mount Electrical Power System

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TECHNICAL MEMORANDUM 78120

POWER SUPPLY SHARING IN THE APOLLO TELESCOPE MOUNT ELECTRICAL POWER SYSTEM

INTRODUCTION

This report addresses the technique used in solution of a problem that arose during the design of the Apollo Telescope Mount (ATM) electrical power system for the Skylab Mission. The problem was related to parallel operation of the modular power supplies, called charger-battery-regulator modules (CBRM's), used on the ATM (Fig. 1). The problem, a common one in paralleling dc power modules, was unequal load or power sharing. The result of the unequal load on the power supplies was unequal component stresses and, with limited power modular sources as the ATM had, loss of system output capability. Early in the program a study showed that a potential loss of 25 percent of the ATM power system capability existed even though care had been taken to provide precise output voltage regulation and programmed regulator impedance. Figure 2 depicts the magnitude of this problem on the ATM. Obviously, this was not acceptable and a solution was sought.

POWER SHARING DEVELOPMENT APPROACH

Existing methods widely used to obtain power sharing between power modules are shown in Figure 3. The advantages and disadvantages are relative to an ATM type application. Note that none of these methods provided a satisfactory solution for the ATM. Since none of the typical methods provided a satisfactory solution, a different technique had to be developed.

The goal for the new system was to reduce the maximum bus power loss from 25 percent to 3 percent or approximately 120 W. Achieving this goal required satisfying two basic considerations: (1) utilize maximum possible solar cell panel power and (2) discharge the batteries to equal depths of discharge to assure they were not depleted during orbital "night" and to maximize battery life. Both of these considerations were satisfied if all 18 CBRM regulators always delivered the same amount of power. Therefore, a system which provided the advantages of the master-slave system without its disadvantage of a single system critical CBRM was sought.

An analysis of a modular power system shows that the reasons for the variation in output power are twofold: (1) the output voltage levels of the modules are different and (2) the output impedances of the modules are different. The mismatch problem may be solved by minimizing or eliminating these variables.

A simplified schematic of the technique chosen to provide the necessary sharing is shown in Figure 4. In this closed-loop system, the bus voltage was sensed and compared to a reference. The resulting error signal was then used to determine the regulator output current. The system worked as follows: The heart of the system was a master reference containing a reference voltage, an amplifier, and an isolation network to prevent external faults from causing a circuit failure. The circuit sensed both ATM main bus voltages and selected the lower of the two voltages. The sensed bus voltage, V_B, was compared with a master reference, V_{R1}, and the difference or error between the two was operated on and distributed to each CBRM as a signal that was proportional to the desired CBRM regulator current required for the bus voltage. Inside the CBRM a signal, I_R, equivalent to the actual regulator output current was compared with the desired current signal, I_P, from the master reference. The error between these two current signals was operated on to provide a correction voltage signal to be added to the internal CBRM regulator reference voltage, V_{R2}, to give the regulator output voltage, V_o, necessary to supply the required current. When all CBRM's had the same output current, the output powers were different by only the difference in distribution line losses which were small on the ATM. Proper selection of system gains minimized this difference. The equation describing the loop is:

$$V_B = \left(\frac{1}{1 + A_1A_2}\right) V_{R2} + \left(\frac{1}{1 + A_1A_2}\right) V_{R1} - \left(\frac{A_2 + Z_L}{1 + A_1A_2}\right) I_R \quad , \quad (1)$$

where

V_B = lowest ATM bus voltage

V_{R1} = master reference voltage

V_{R2} = CBRM reference voltage

A_1 = master reference gain that determines the programmed impedance

A_2 = CBRM gain with which the regulator responds to the programmed current error

I_R = signal equivalent to CBRM output current

I_P = signal equivalent to the desired output current

V_o = CBRM regulator output voltage

Z_L = impedance of distribution line.

If the circuit gains, A_1 and A_2, are selected properly, the equation may be approximated as shown in Figure 5. The original equation may be simplified as follows:

$$V_B = \frac{1}{A_1 A_2} V_{R2} + V_{R1} - \frac{1}{A_1} I_R \quad . \tag{2}$$

Note that in equation (2) the reference voltage, V_{R1}, is in the master reference and is common to all regulators. Therefore, variation of this parameter only results in similar variations in bus voltage and do not affect the power sharing among the CBRM's. The dependence of regulator output current on bus voltage generates a resistance characteristic described by the term $(A_2 + Z_L/1 + A_1 A_2)$. If the gains are chosen properly, variations of the line impedances, Z_L, have negligible effect on the net impedance. On the ATM, maximum variations of line impedance resulted in less than 1 percent change in the net impedance. The effects of regulator voltage reference variations have been reduced by the factor $(1/A_1 A_2)$. Again, if the gains were chosen properly, variations of the regulator voltage references, V_{R2}, had negligible effect on the output voltage. On the ATM, maximum variations of CBRM reference voltage resulted in less than 0.1 percent change in output voltages. The result was negligible effect of individual CBRM parameters on the power sharing among the CBRM's.

POWER SHARING IMPLEMENTATION

A circuit was designed to implement the technique discussed. The sensing circuit, reference supply, comparator, and amplifier were designed with redundancy so that no single component failure would cause a loss of output. This redundant circuitry was packaged on one 7.8 by 11.4 cm printed circuit board. The isolation network for the 18 outputs were packaged on a second board. Since the redundancy technique used precluded the elimination of failures that would cause the circuit output to demand a current higher than required, (I_P signal high) a second redundant power sharing unit was also used on the ATM. The relays for switching the desired unit were located on the board with the isolation network.

The resulting circuit, except for the relays, lends itself well to microcircuit techniques. The entire circuit, including the isolation network components, could be packaged in one microcircuit, should the need arise.

CONCLUSION

The goal of introducing a power sharing scheme into the ATM electrical power system was to increase the system power capability as stated. An additional advantage of improved bus regulation also resulted. The improved bus regulation is shown in Figure 6. Theoretically, the regulation may be further improved by increasing the gain A_1 as noted in Figure 5. However, the practical aspects of line impedance, regulator output voltage, and system stability led to the particular voltage characteristic shown for the ATM.

The effect of incorporating the power sharing technique discussed on the ATM power system output is readily apparent by comparing Figure 7 and Figure 2. Note that the dispersion between the highest output CBRM regulator and an average output regulator is now less than 5 W. Before adding the power sharing circuitry this dispersion could be almost 60 W. The net system power loss with sharing was less than 100 W compared to approximately 1000 W before this circuit was added. The operation of the system with the power sharing circuit was demonstrated on the Skylab power breadboard and on the ATM. No problems resulted from implementing the sharing technique, and the predicted advantages were realized. Thus, all goals were reached, the development successfully completed, and a new approach to power sharing between dc modules was demonstrated.

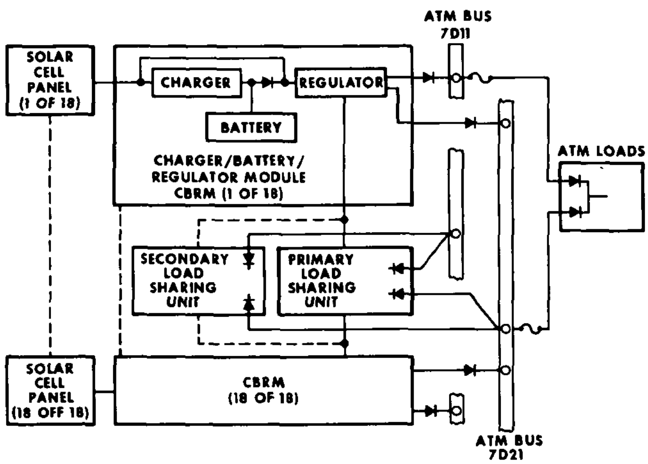


Figure 1. ATM electrical power system.

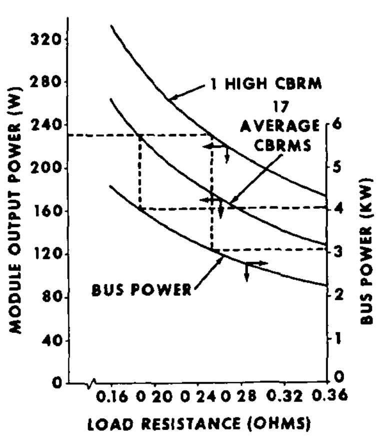
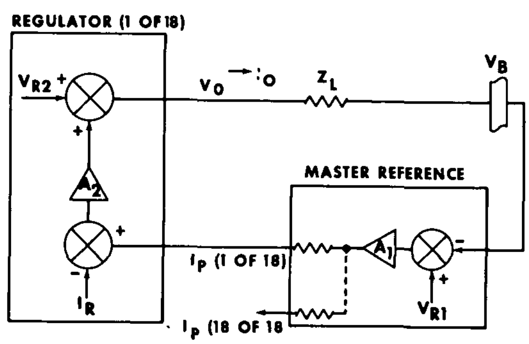


Figure 2. ATM EPS characteristics without power sharing.

METHOD	ADVANTAGES	DISADVANTAGES
EQUALIZE LINES	• SIMPLE	• ADDED WEIGHT • ADDED POWER LOSS • INADEQUATE SHARING • POOR BUS REGULATION
PROGRAM REG IMPEDANCE	• EFFICIENT	• INADEQUATE SHARING • POOR BUS REGULATION
MASTER-SLAVE SYSTEM	• EFFICIENT • GOOD BUS REGULATION • GOOD POWER SHARING	• MASTER MODULE IS SINGLE POINT FAILURE
CURRENT LIMITED REGS	• EFFICIENT • GOOD BUS REGULATION	• INADEQUATE SHARING

Figure 3. Typical power sharing methods.



$$V_B = \left(\frac{1}{1+A_1A_2}\right) V_{R2} + \left(\frac{A_1A_2}{1+A_1A_2}\right) V_{R1} - \left(\frac{A_2+Z_L}{1+A_1A_2}\right) I_R$$

Figure 4. Simplified feedback diagram for remote sensing and programmed impedance.

$$V_B = \left(\frac{1}{1+A_1A_2}\right)V_{R2} + \left(\frac{A_1A_2}{1+A_1A_2}\right)V_{R1} - \left(\frac{A_2+Z_L}{1+A_1A_2}\right)I_R \qquad (1)$$

MINIMIZE EFFECTS OF VARIATIONS IN LINE RESISTANCE (R_L) $\Rightarrow A_2 \gg Z_L$

MINIMIZE EFFECTS OF VARIATIONS IN A_2 ITSELF $\Rightarrow A_2 > 1$

PROGRAM IMPEDANCE FOR "HARD" BUS $\Rightarrow A_1 \gg 1$

THEREFORE: $\frac{1}{1+A_1A_2} \ll 1; \quad \frac{A_1\,A_2}{1+A_1A_2} \cong 1; \quad \frac{A_2+Z_L}{1+A_1A_2} \cong \frac{1}{A_1}$

THEREFORE: $V_B \cong \frac{1}{A_1A_2} V_{R2} + V_{R1} - \frac{1}{A_1} I_R \qquad (2)$

Figure 5. Reduction of feedback equation.

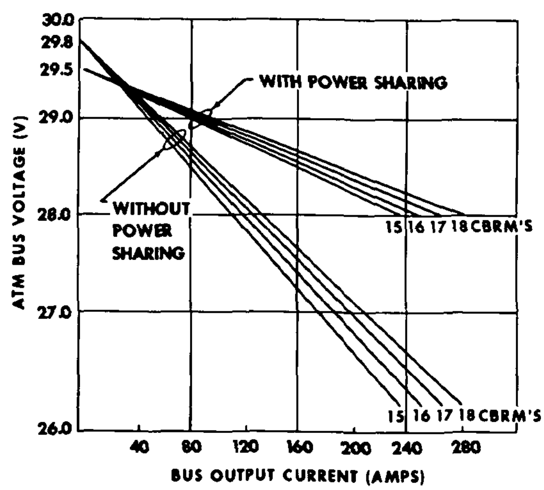


Figure 6. ATM bus voltage regulation.

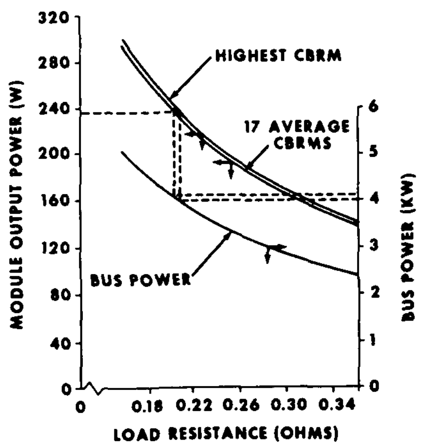


Figure 7. ATM EPS characteristics with power sharing.

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16. ABSTRACT

This report presents a new type of modular dc power supply power sharing technique that was developed for the Apollo Telescope Mount (ATM) electrical power system on the Skylab. The advantages and disadvantages of various techniques used in the past are reviewed and compared to the new method. The new technique design is discussed, and results of its implementation in the ATM power system are reviewed.

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