Effect of Interference on Delta Modulator Encoded Video Signals

Final Report

October 1, 1976 - September 30, 1977

Goddard Space Flight Center

Greenbelt, Maryland

under

NASA GRANT NSG - 5013

Donald L. Schilling

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DEPARTMENT OF ELECTRICAL ENGINEERING

THE CITY COLLEGE OF
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Introduction

This final report summarizes several aspects of the research sponsored by the National Aeronautics and Space Administration under NASA Grant NSG - 5013 for the period October 1, 1976 - September 30 1977

During this period of time the effect of interference on delta modulator encoded video signals was studied This study consists of two facets The first part concerned with selecting algorithms that could be implemented to operate in real time, the second concerned with comparing the resulting pictures when interference is present.

The first part of the study has now been completed One and two dimensional encoding algorithms have been developed and adaptive deltamodulators constructed A DPCM system has also been designed and built for the purpose of comparison

During the 1977-1978 Grant period we shall be considering the effects of interference on these systems Following the history of cooperation that has existed between Dr Schilling and NASA since 1964, the Communications Systems Laboratory has given NASA a video deltamodulation system NASA will be experimenting with this unit and we are hopeful that these experiments will enhance our knowledge of the effect of real interferers on deltamodulation systems

I. An All Digital Adaptive Delta Modulator

Introduction

The development of an adaptive delta modulator capable of encoding a television picture has been completed The delta modulator encoder accepts a 4MHz black and white composite television signal, or NASA's field sequential color television signal. and encodes it into a binary signal at a rate of up to 20 Mb/s The output bit rate is determined by the user Useable pictures can be obtained with bit rates between 8 and 20 Mb/s The higher the rate the better the picture quality

The digital signal is converted back into analog form by a delta modulator receiver The receiver requires a bit synchronizer to provide "bit timing" "Word timing" as used in PCM is not necessary with the adaptive delta modulator

No special circuits are required to provide for horizontal and vertical syncronization of the TV monitor at the receiver The composite video signal that entered the delta modulator encoder will emerge from the delta modulator receiver with its horizontal and vertical sync pulses intact Thus the TV monitor will obtain its syncronization from the composite video signal emerging from the delta modulator decoder.

Theory of Operation

The delta modulator used to digitize the television pictures is shown in block diagram form in Fig 1. The following is an explanation of the delta modulator algorithm First, the video signal, S(k) , is compared to X_k This yields the output of the encoder, E_k, where

$$E_{k+1} = \text{sgn}\ (-S_k - Y_k) \qquad (1)$$

X_k, is the transmitter estimage, and is obtained using the recursive equation

$$X_k = 98\, X_{k-1} + Y_k \qquad (2$$

Y_k, is the step size and is generated using the algorithm

$$Y_k = \begin{cases} Y_{k-1} \; ; & |Y_{k-1}| \geq 2\, Y_{min} \\ (E_k + 5\, E_{k-1}) \; ; & |Y_{k-1}| < 2\, Y_{min} \\ 2\, Y_{min}\, E_k \; ; & \\ Y_{max} \; ; & |Y_k| > Y_{max} \end{cases} \qquad (3)$$

where Y_{min} is 1/128 of the peak-to-peak video signal and Y_{max} is 1/8 of the peak-to-peak video signal.

The delta modulator decoder is just the feedback loop of the encoder The decoder reconstructs the estimate, X_k, from the E_k pulse train and converts X_k to an analog signal $\hat{S}(t)$ The quality of the received picture as compared to that of the transmitted picture depends upon how closely $\hat{S}(t)$ approximates the original signal, S (t)

Implementation of the Delta Modulator

The implementation block diagram is shown in Fig 2 The two flip-flops on the top of the diagram store E_k and E_{k-1} The upper adder/subracter register, multiplexer and "OR" gates implement Eq 3, the step size equation The other adder/subtracters and registers are used to generate Eq 2 and the D/A converter and comparator implement Eq 1 The complete circuit schematic for the delta modulator is shown in Fig. 3. It was constructed employing ECL integrated circuits one D/A converter and a high speed comparator. It was built on a single board 8" by 6" and dissipates 7 watts of power.

Instructions for Using the Delta Modulator

A typical test set-up using the delta modulator encoder and decoder is shown in Fig 5.

The Encoder has four BNC connectors on its front panel The function and electrical characteristics of each connector is listed below:

(1) Digital Output
   a ECL compatible voltage levels
   b Designed to drive 50 Ω tied to -1 3V
(2) Clock Input
   a 8 to 19 MHz
   b ECL compatible voltage levels (-0 9V to -1. 7V).
   c The input impedance is 50 Ω tied to -1 3V.
(3) Analog Video Input
   a 1 volt peak-to-peak composite video from TV camera
   b 75 Ω input impedance tield to ground.
(4) Analog Video Output
   a 1 volt peak-to-peak composite video from the feedback loop of the encoder It is used to monitor the operation of the encoder

The decoder has three BNC connectors on its front panel. The function and electrical characteristics of each connector is listed below·

(1) Digital Input
   a ECL compatible voltage levels
   b. The input impedance is 50 Ω tied to -1 3V.
(2) Clock Input
   a 12 to 20 MHz phase locked to incoming digital data
   b ECL compatible voltage levels (-. 9V to -1 7V)
   c. The input impedance is 50 Ω tied to -1 3V.
(3) Analog Video Output
   a. 1 volt peak-to-peak composite video signal
   b Bandlimited to 4MHz by a four pole Butterworth filter
   c. Must be terminated to 75 Ω to ground.

II Real Time Two-Dimensional Intraframe Delta Modulator

A two-dimensional intraframe delta modulator which operates in real time has been built The algorithm is described in great detail in the last semi-annual report and will be appearing in the November issue of the "IEEE Transactions on Communications" in a paper entitled "Adaptive Delta Modulation Systems for Video Encoding"

The two-dimensional delta modulator consists of two delta modulators: one that encodes vertically and one that encodes horizontally At each pixel, decision circuitry compares the estimate from the horizontal and vertical encoders with the value of the pixel to be encoded The estimate from the horizontal encoder is one pixel to the right of the pixel to be encoded while the vertical estimate is one pixel above the estimate to be encoded If the vertical estimate is closer in value to the pixel to be encoded, than the horizontal estimate, then the pixel will be encoded from the vertical delta modulator. If the reverse were true then the horizontal delta modulator would be used to encode the pixel.

This encoder requires 2 bits to be transmitted each time the input signal is sampled and therefore operates at the rate of 2 bits/pixel. The second bit is used to signal the receiver as to whether to encode in the horizontal direction or in the vertical direction

The hardware implementation of the delta modulator required about 60 IC's. Twelve of the IC's were required to store a line of video while the rest comprised the horizontal and vertical delta modulators and the decision circuitry. The circuit schematic, (not including the memory) is shown in Fig. 6. This device is three times as complex as the one dimensional delta modulator.

Even though the two dimensional delta modulator is far more complex than the one dimensional delta modulator we have found both delta modulators to be subjectively equivalent in picture quality at 16 Mb/s This result contradicts our earlier computer simulations which were presented in the paper "Adaptive Delta Modulation Systems for Video Encoding" The computer simulations suggested that the two dimensional delta modulator would be much better than the one dimensional delta modulator because it lacked edge "busyness" The two-dimensional delta modulator, however, had edge busyness in the temporal domain A single frame "looked good" but each frame, even from a scene that was not changing,was encoded slightly differently. As each frame was flashed on the screen at a rate of 30 times per second the differences between frames appeared as edge busyness The busyness was most pronounced on diagonal lines

A somewhat simplified implementation of the delta modulator is shown in Fig 7. We think that this delta modulator may find application in slow-scan TV where only a single frame of video is transmitted Since only one frame is sent the temporal edge busyness will disappear. This delta modulator is currently under construction Its circuit schematics are shown in Fig 7.

III. Papers Published

"Adaptive Delta Modulation Systems for Video Encoding", IEEE Trans. on Comm., November 1977, pp. 1302-1314

"Techniques for Correcting Transmission Errors in Video Adaptive Delta Modulation Channels, IEEE Trans on Comm, Sept. 1976, pp. 1064-1070

IV. Papers Presented

"An All Digital Technique for ADM to PCM Conversion" NTC-76

"Two Dimensional Delta Modulator for Picture Encoding" I. S. I. T-76

"SNR Analysis on the SONG ADM for a Sinusoidal Input", I. S. I. T-76

V. Doctoral Student Graduated

Joseph LoCicero, Dissertation: Arithmetic Processing and Digital Conversion of ADM Encoded Signals - 1977

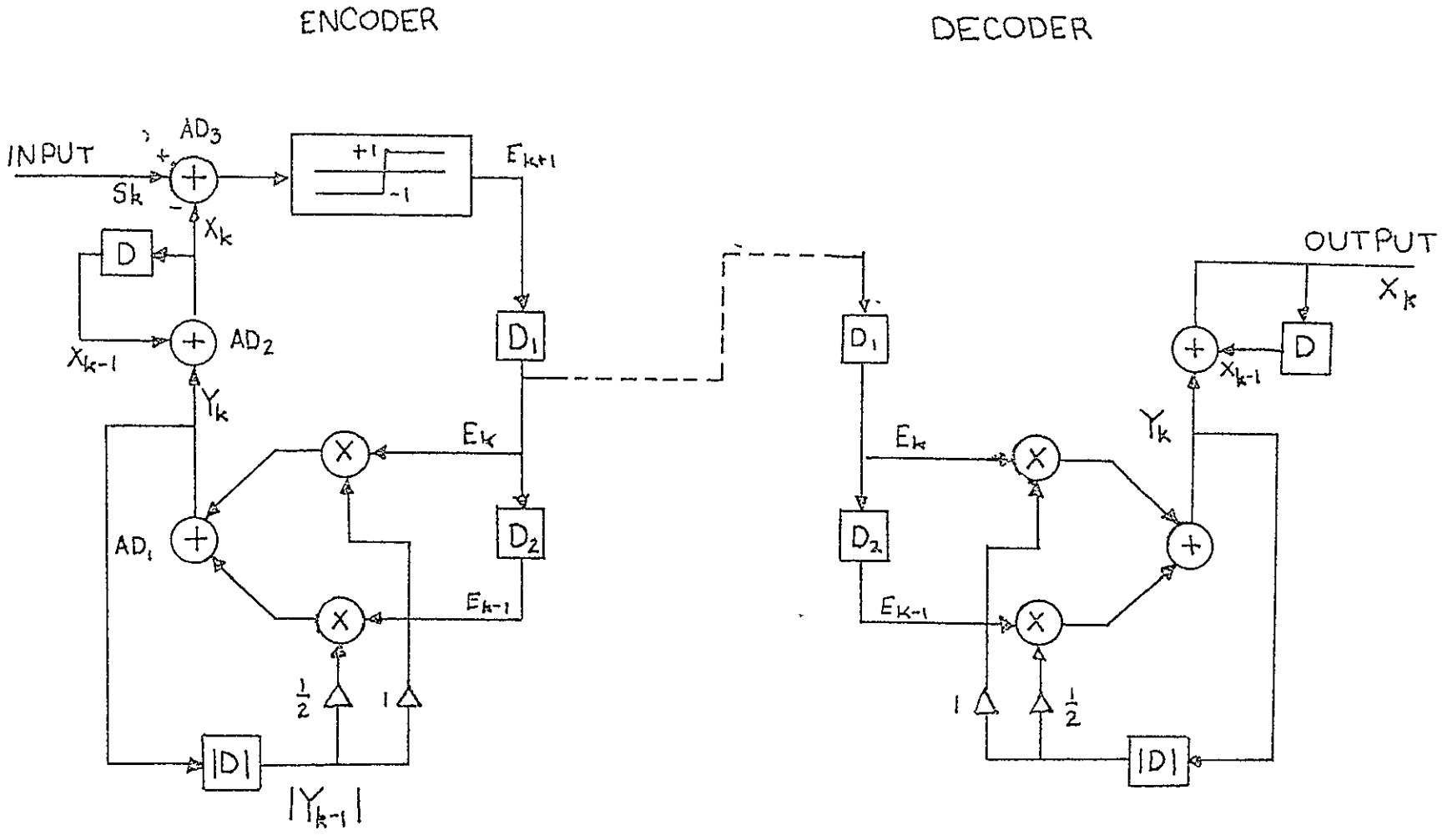

FIG. 1 DIGITAL ADAPTIVE DELTA MODULATOR

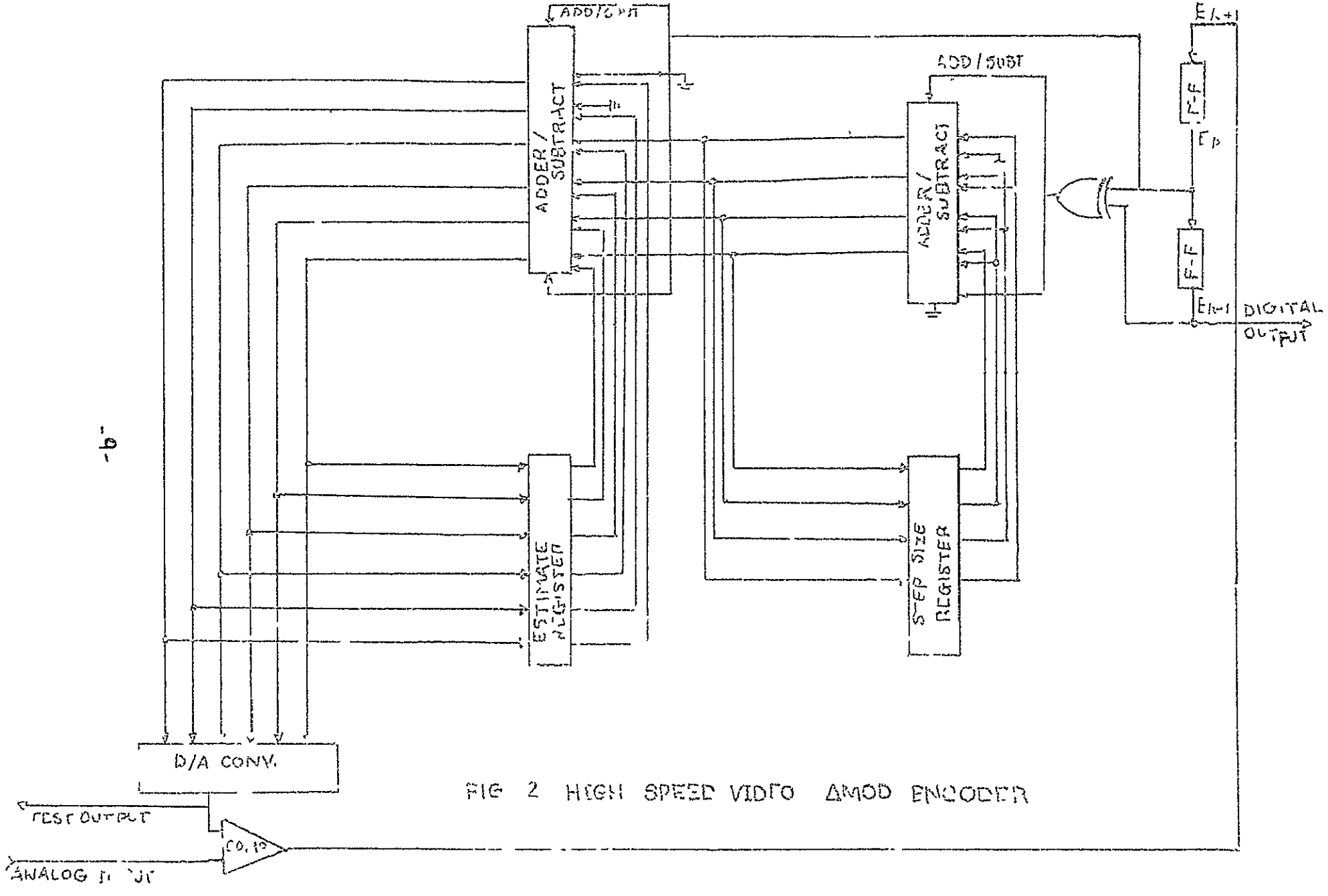

FIG 2 HIGH SPEED VIDEO ΔMOD ENCODER

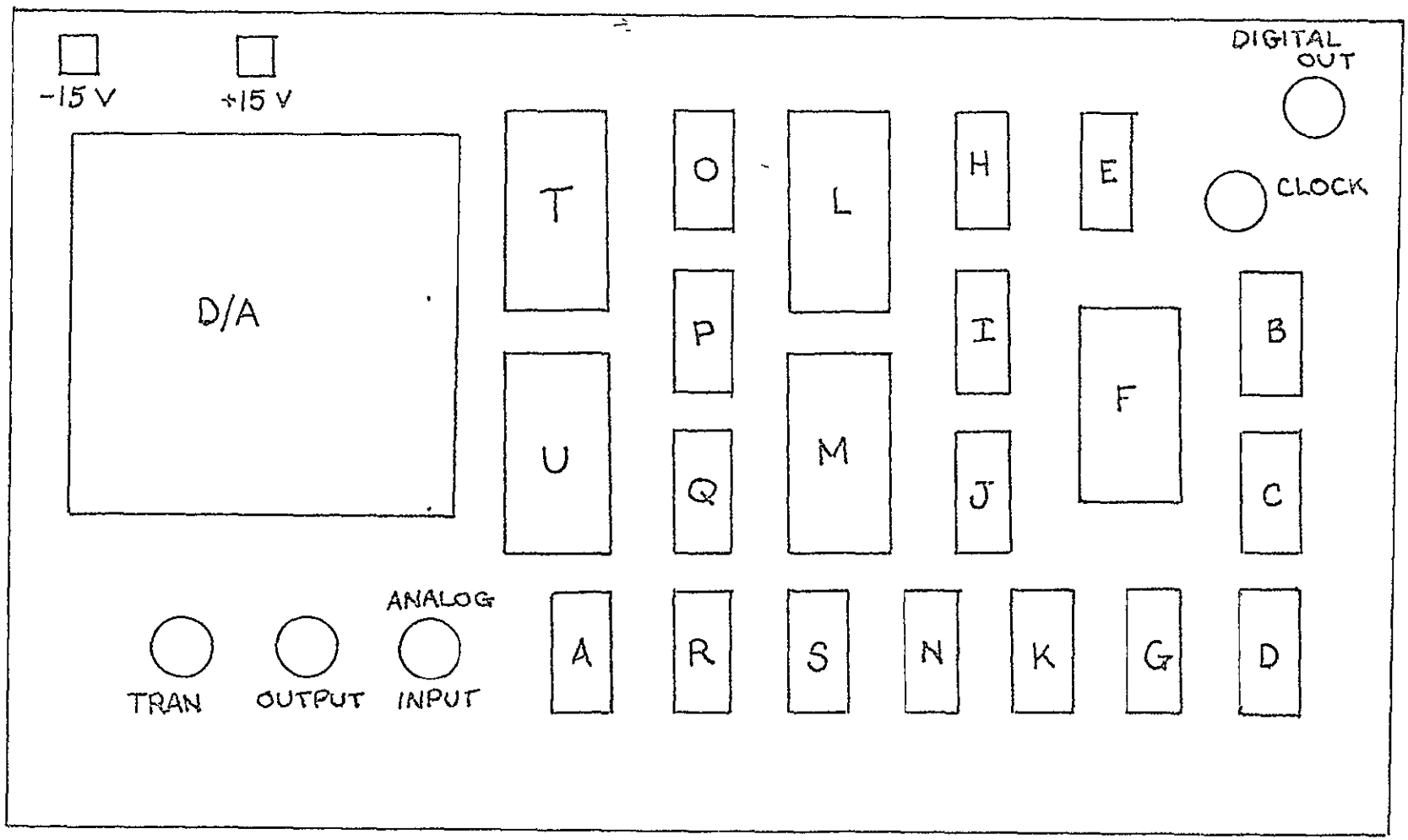

FIG 3a ONE DIMENSIONAL DELTA MOD TRANSMITTER

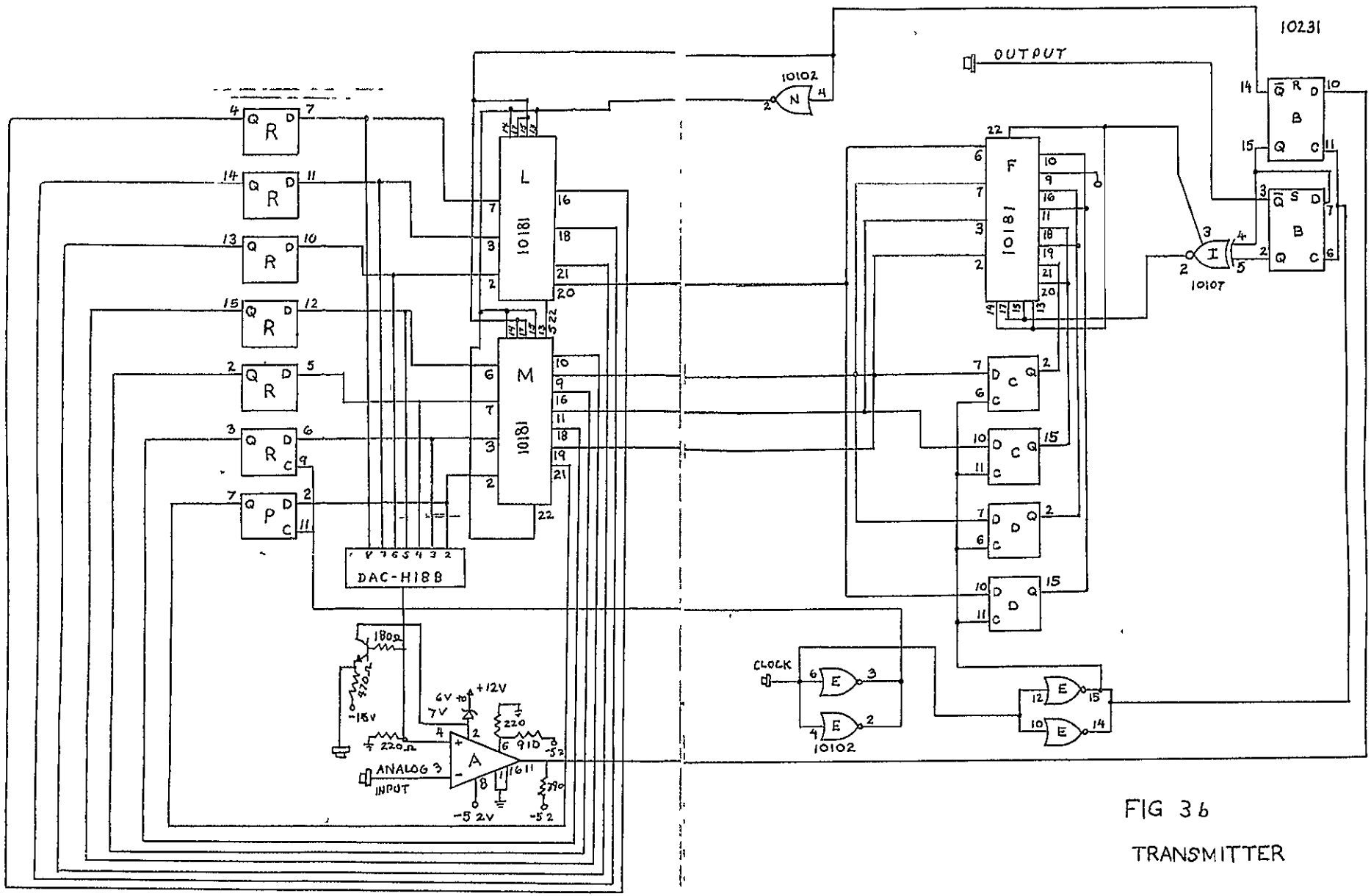

FIG 3b

TRANSMITTER

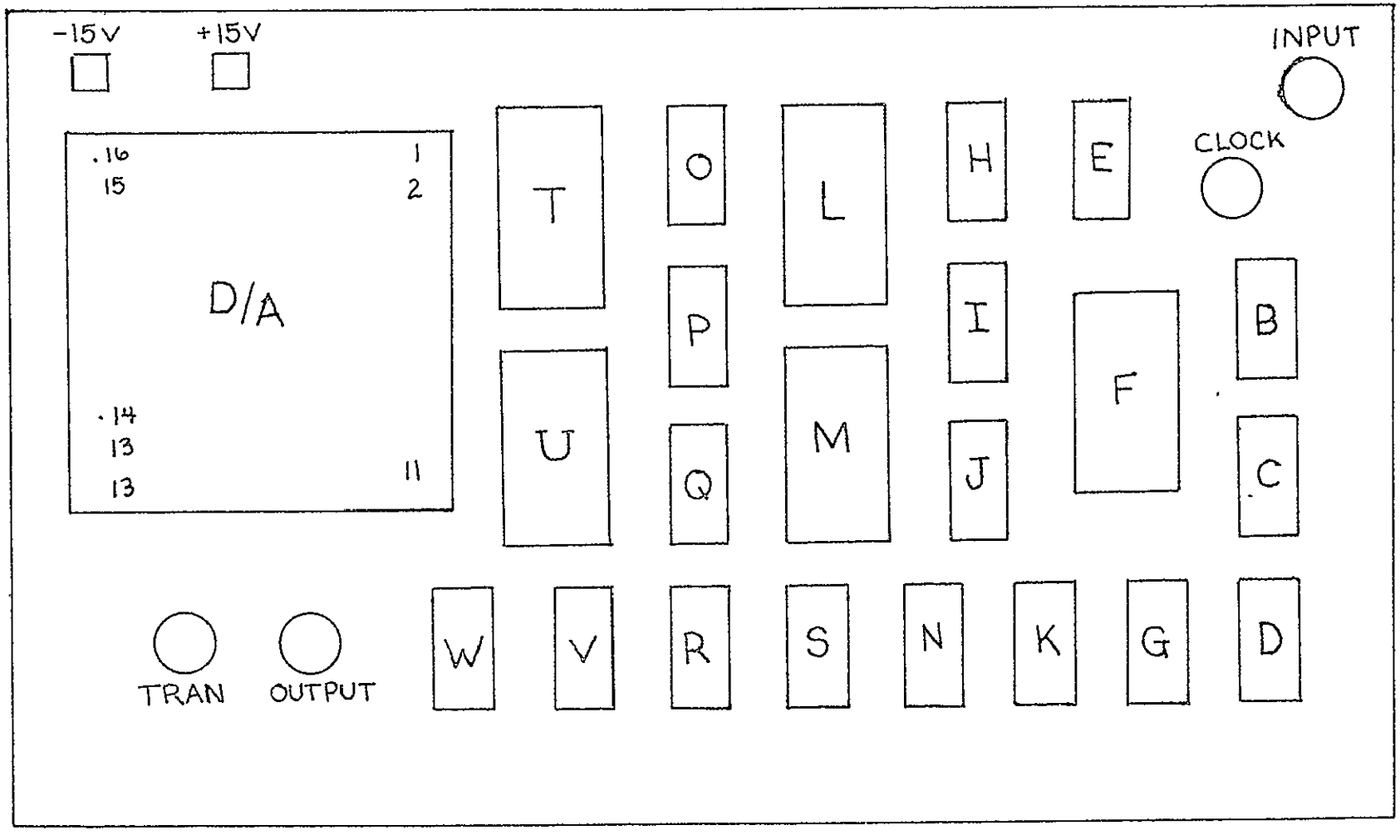

FIG 4a ONE DIMENSIONAL DELTA MOD RECEIVER

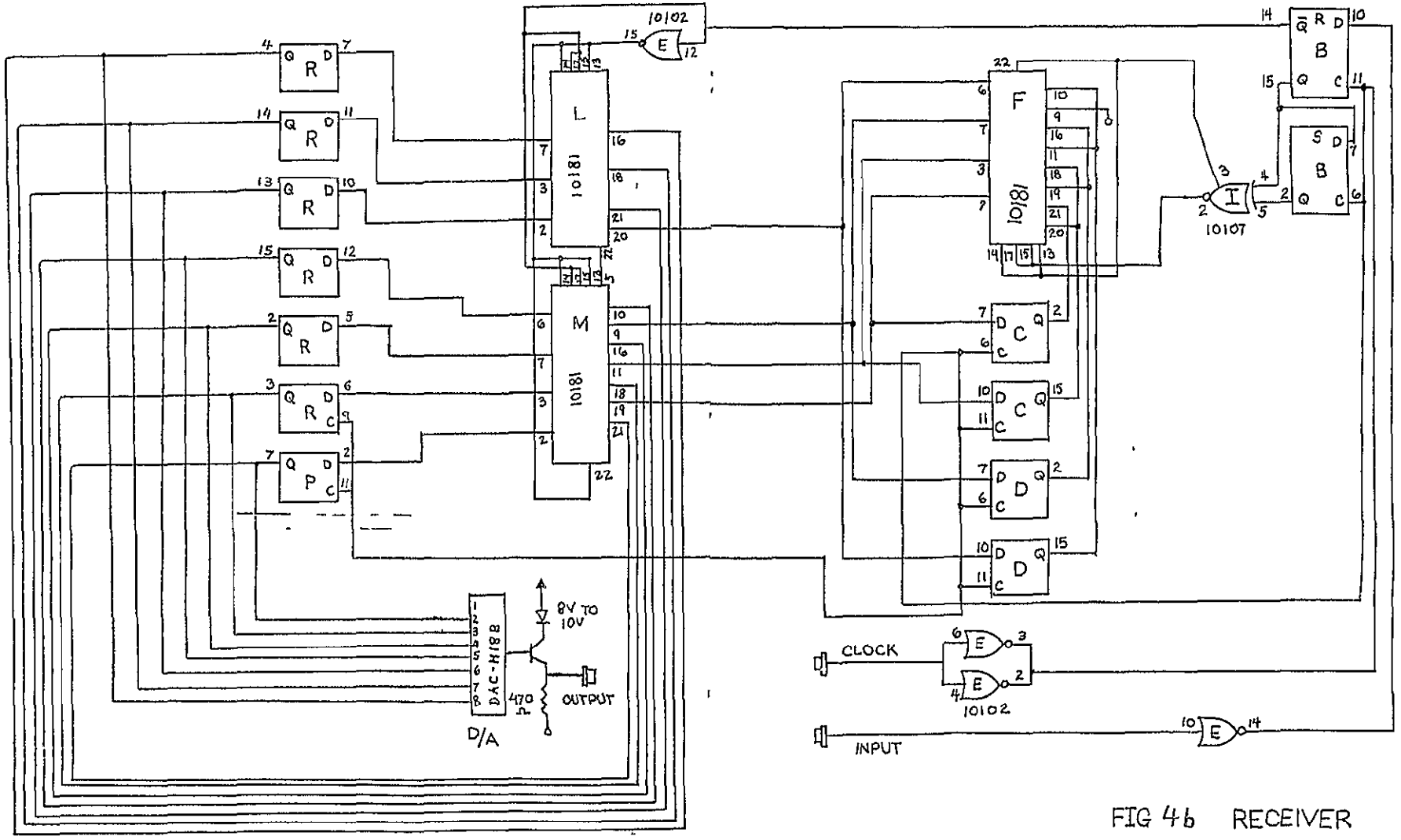

FIG 4b RECEIVER

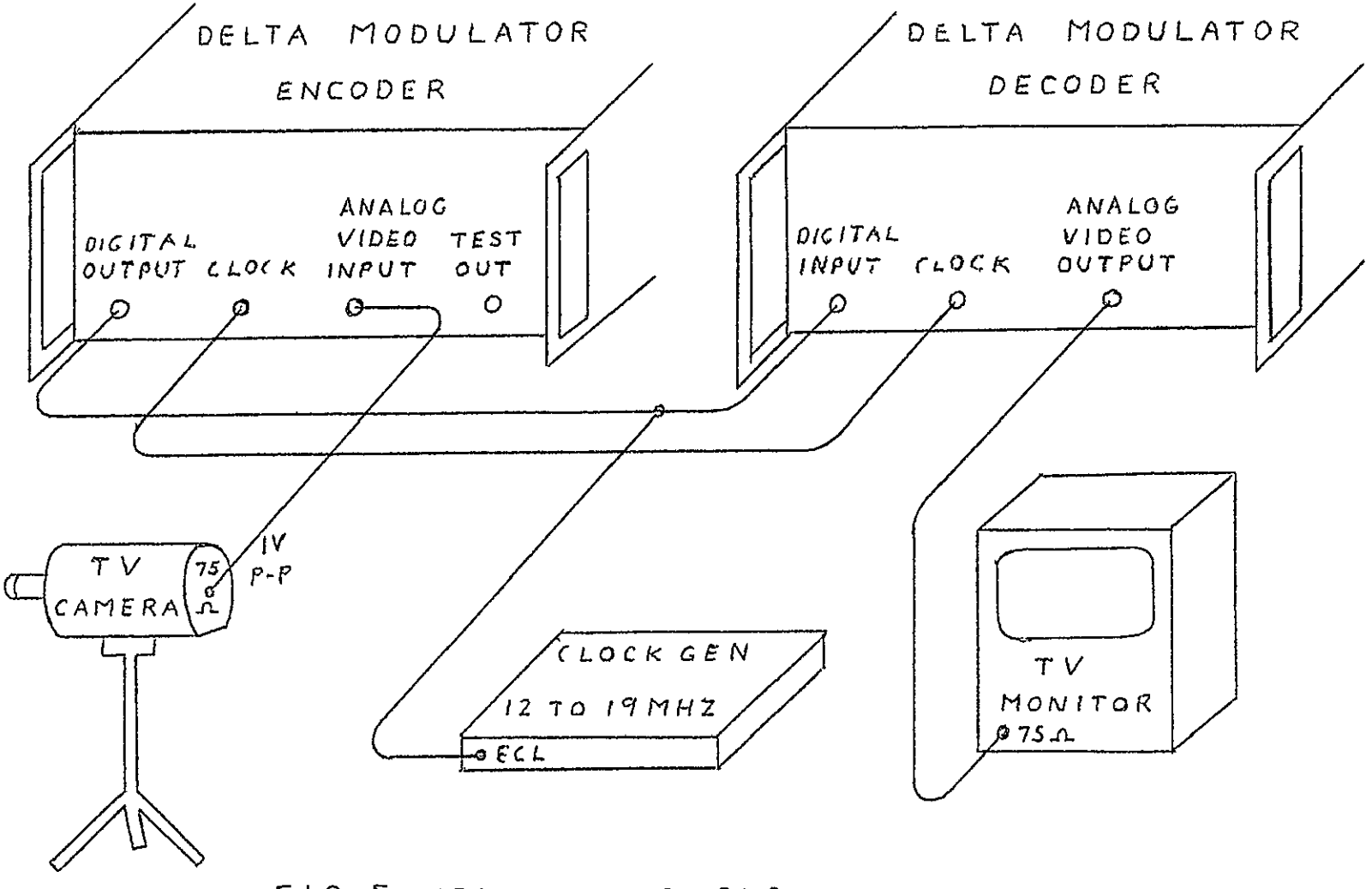

FIG. 5 TEST SETUP FOR DELTAMODULATOR

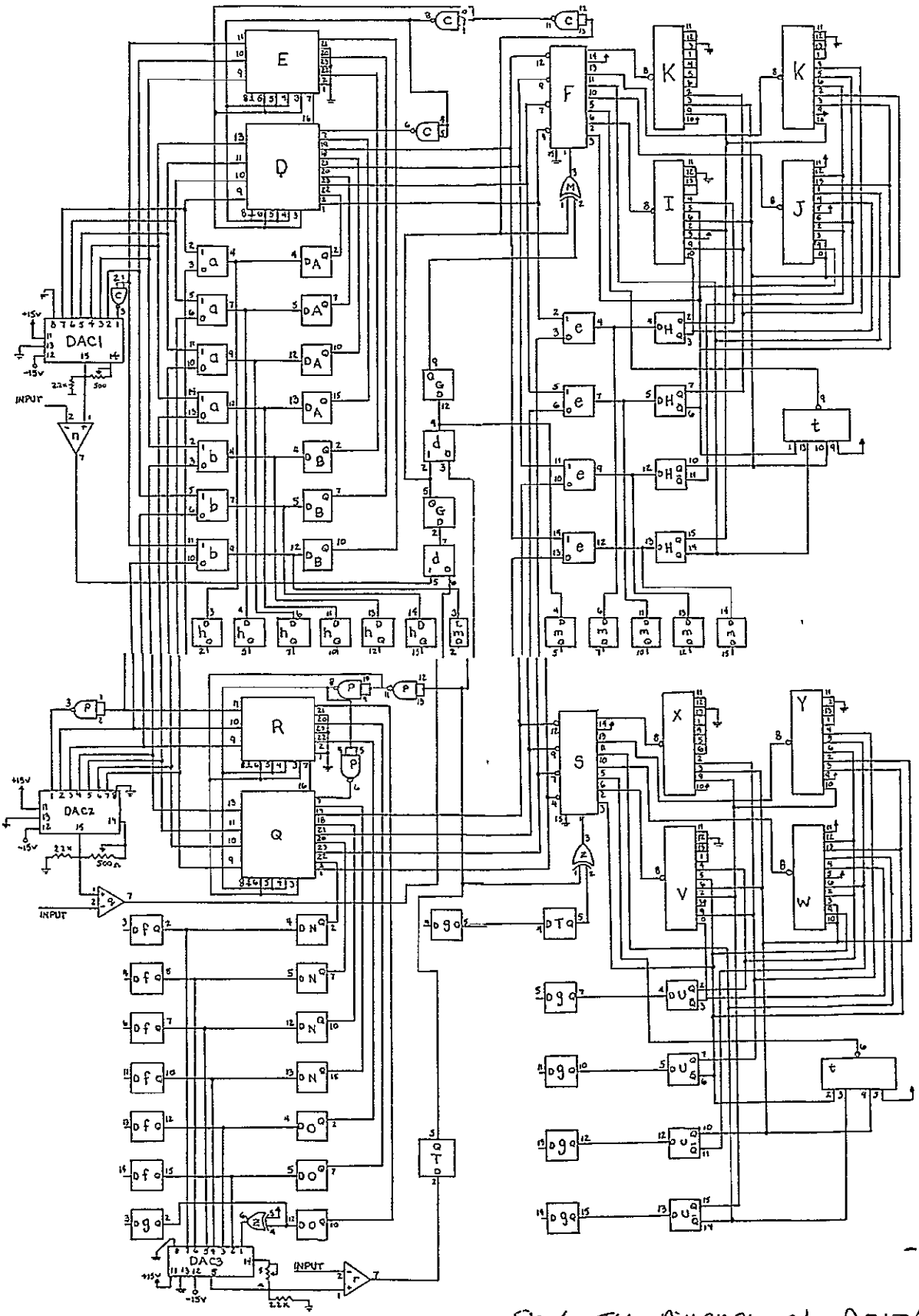

Fig 6 Two Dimensional DEITA MODULATOR

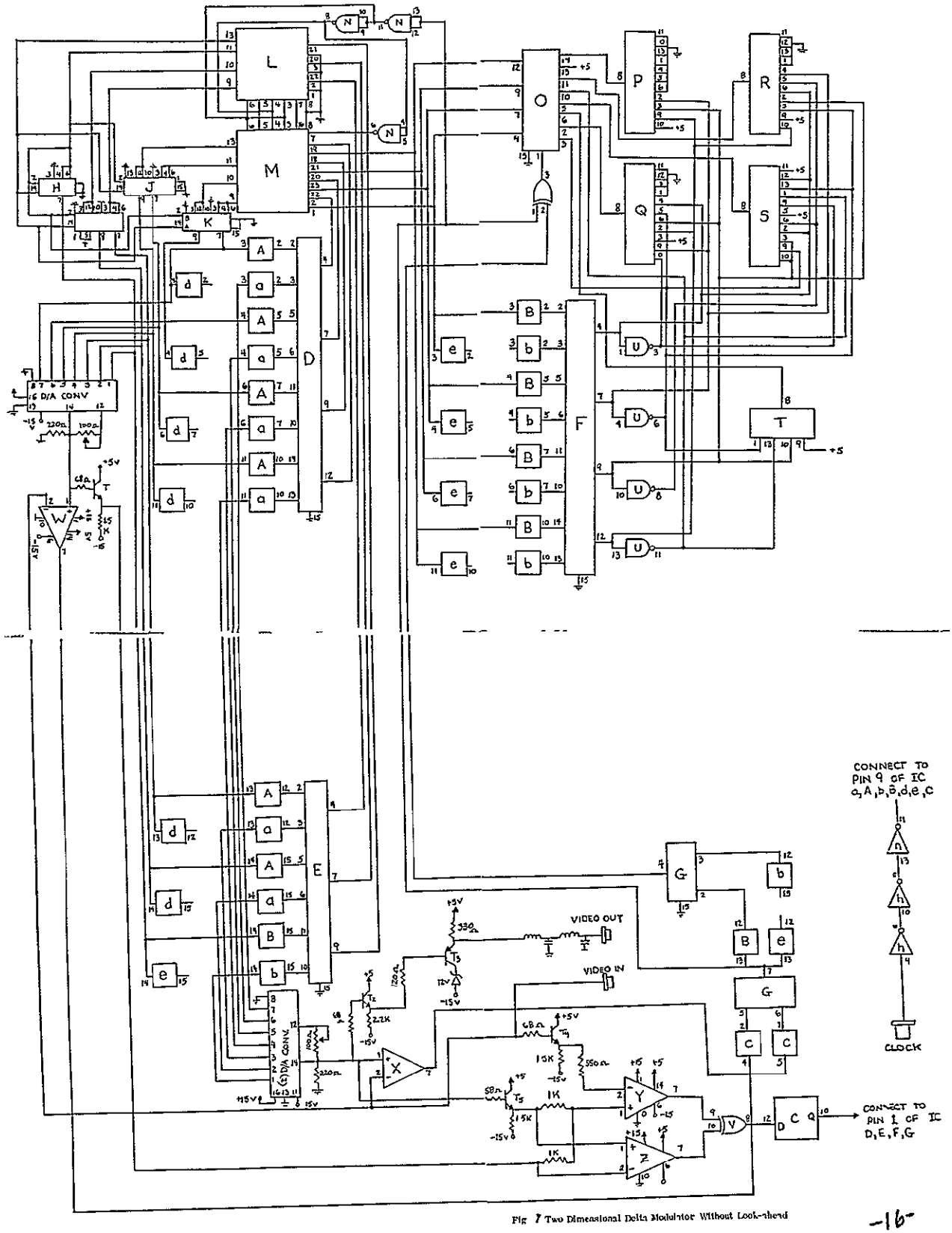

Fig 7 Two Dimensional Delta Modulator Without Look-ahead

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by

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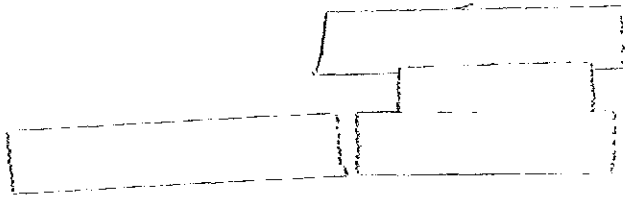
Separations Engineering Division

November 1960



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