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ADAPTATION OF ION BEAM TECHNOLOGY TO MICROFABRICATION OF SOLID STATE DEVICES AND TRANSDUCERS

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16. Abstract

A study has been conducted to determine the potential applications of ion beam techniques in the construction of solid state devices and transducers. It has been found that ion beam texturing of silicon surfaces can be used to increase the effective surface area of MOS capacitors. There is, however, a problem with low dielectric breakdown. Preliminary work was begun on the fabrication of ion implanted resistors on textured surfaces and the potential improvement of wire bond strength by bonding to a textured surface.

In the area of ion beam sputtering, the techniques for sputtering PVC were developed. A PVC target containing valinomycin was used to sputter an ion selective membrane on a field effect transistor to form a potassium ion sensor.

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ADAPTATION OF ION BEAM TECHNOLOGY TO MICROFABRICATION
OF SOLID STATE DEVICES AND TRANSDUCERS

I. Introduction

In the area of solid state device fabrication the use of ion beam systems has been directed primarily at ion milling for improved control of surface feature linewidths and to a lesser extent the sputtering of conventional materials used in solid state processing. The work being pursued under this grant can be classified under two categories which are rather different from those mentioned above. They are (1) a study of textured silicon surfaces and how they can be used in the fabrication of semiconductor devices and (2) the sputtering of unconventional materials, as far as solid state processing is concerned, such as teflon or polyvinylochloride for use as protective coatings or as ion selective membranes for chemical sensitive field effect transistors. The characterization of the texturing process is being done by personnel at NASA Lewis[1] and others and is not part of the work presented here.

This report will cover the use of textured silicon surfaces for (1) the fabrication of MOS capacitors with larger effective surface areas to increase the component density on integrated circuits, (2) the fabrication of ion implanted resistors in order to investigate its effects on the resulting sheet resistances and (3) the fabrication of bonding pads on IC's to increase bond strength and improve reliability.

In the area of sputtering ion selective membranes all of the work to date has been on polyvinylochloride containing valinomycin. The electrical properties were characterized using current-voltage and capacitance-voltage measurements. The chemical composition of the sputtered films were analyzed using electron spectroscopy and compared to the target composition. Using the results of the initial tests, a film consisting of polyvinylochloride and valinomycin was sputtered on an FET to form a potassium ion sensitive device which was tested and characterized.

II. Textured Silicon Surfaces

A. MOS Capacitors

Six silicon wafers have been received which were textured at NASA Lewis under varying conditions. The sputtering parameters are tabulated in Table I. Both the size and shape of the surface structure varied from wafer to wafer. Some samples had cone-like structures, while others had ridges. The peak height, as determined from SEM photos, varied between 0.1 micron and 1.6 microns. Photomicrographs of cones and ridges are given in Figure 1. To date, no significant differences in the measured properties have been observed which could be correlated with either the surface structure or size. As more samples are analyzed some trend may show up but one is not apparent at this time.

The ion beam group at NASA Lewis is working on the understanding and characterization of the texturing process and thus that aspect of the project is not addressed in this progress report.

All of the textured wafers received underwent the following processing to form MOS capacitors.

1. One minute etch in buffered HF.
2. Standard cleaning procedure.
3. One hour oxidation in dry O_2 at 1050°C.

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TABLE I. TEXTURING PARAMETERS

SAMPLE	BEAM ENERGY	BEAM CURRENT	EXPOSURE TIME	SEED ANGLE	SURFACE STRUCTURE
A-10	1keV	165 mA	1 hr.	---	cones
A-7	1keV	2.7 mA	1 hr.	20°	cones
A-9	1keV	140 mA	2 hrs.	25°	ridges
B-8	1.2keV	160 mA	2 hrs.	---	ridges
B-10	1.2keV	148 mA	3 hrs.	27°	ridges
B-11	1.2keV	162 mA	3 hrs.	15°	cones and ridges

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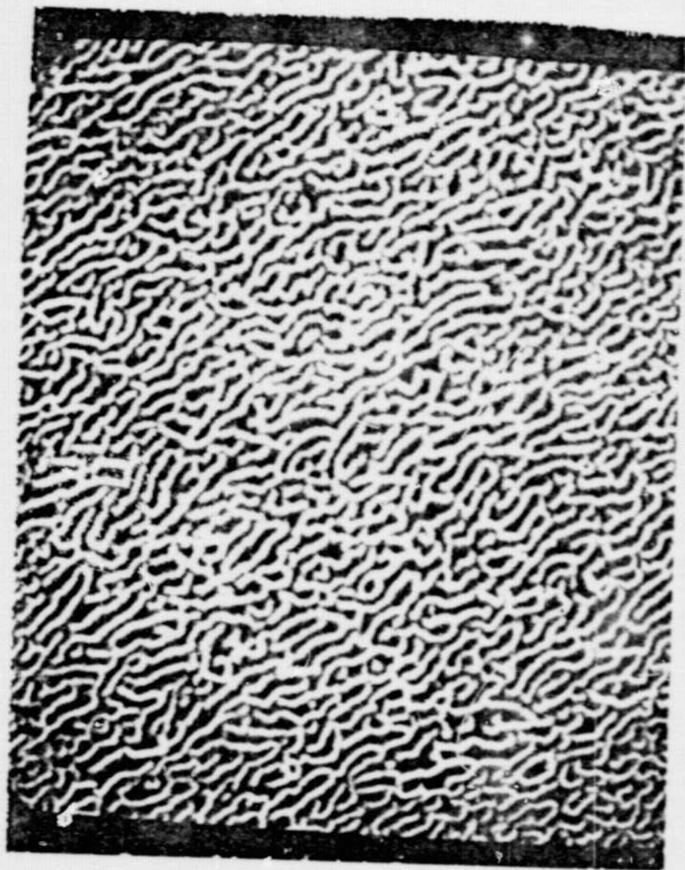
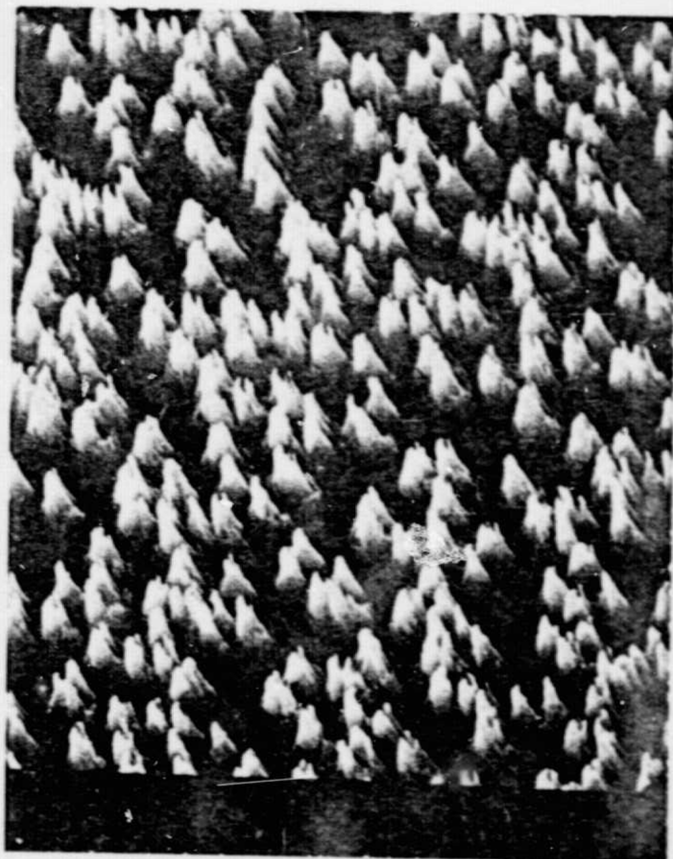


Sample A-9
10,000 x magnification



Sample A-7
3000 x magnification

FIGURE 1. EXAMPLES OF TEXTURED SURFACES WITH RIDGES AND CONES

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4. Top side metalized with aluminum and patterned.
5. Back side etched.
6. Back side metallized with aluminum.

When samples A-7, A-9 and A-10 were probed to measure their current voltage (I-V) characteristicts, the results obtained were very similar but quite unexpected. In the masked regions where no texturing occurred, good capacitor characteristics were observed. In the textured regions, non-linear I-V characteristics similar to Schottky diodes were observed. Such a characteristic from sample A-7 is shown in Figure 2. The reason for this behavior will be discussed below in conjunction with the results reported for the second batch of textured wafers studied.

In order to determine the effect of the high temperature oxidation on the resulting surface structure and the quality of the aluminum coverage, each wafer was broken into two pieces. The aluminum and oxide were etched off one piece to reveal the underlying surface structure. The surface after oxidation, metallization and etching were looked at using an SEM at NASA Lewis. For the regions that had approximately one micron cones, there was very little difference in appearance after oxidation. One was not, however, able to determine quantitatively the changes in size because of the variations in cone size across the wafer. There is a granular appearance to the aluminum after metallization but that is due solely to the evaporation process. There was no apparent problem in metal coverage, nor with our standard photolithographic process even though the wafer surface was no longer flat. After etching the aluminum and silicon dioxide, it became apparent that some of the silicon cone had been consumed during the oxide growth. This manifested itself as a rounding off of the cone peak, but its effect is not enough to reduce the effective surface area significantly. On portions of the wafers where the cones were only a fraction of a micron high, they were almost completely consumed during the oxidation. It appears that 1 micron cones are about the optimum size for increasing effective surface area when oxide thickness and

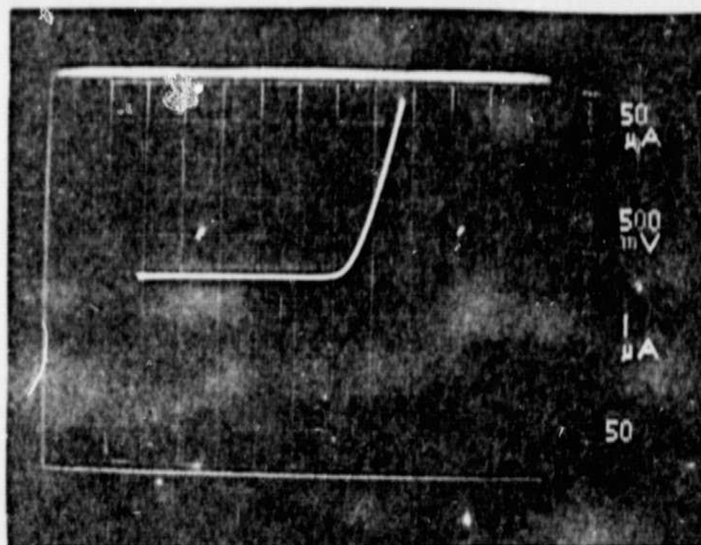

FIGURE 2. I-V CHARACTERISITCS FOR A "CAPACITOR" ON THE TEXTURED SURFACE OF A-7

TABLE II
ZERO BIAS CAPACITANCE OF MOS CAPACITORS FABRICATED ON TEXTURED SILICON

SAMPLE	TEXTURED	NONTEXTURED
B-8	7100 pf	3100 pf
B-10	6500 pf	2800 pf
B-11	4000 pf	3000 pf

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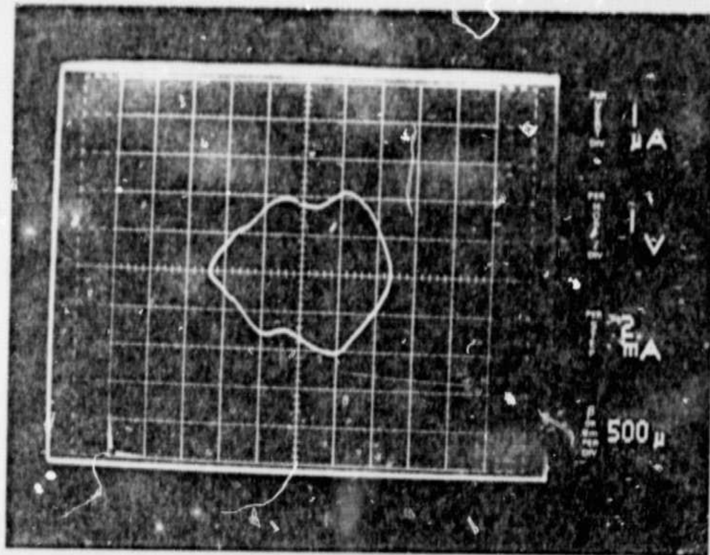
minimum surface features to be produced by the photolithography are both considered.

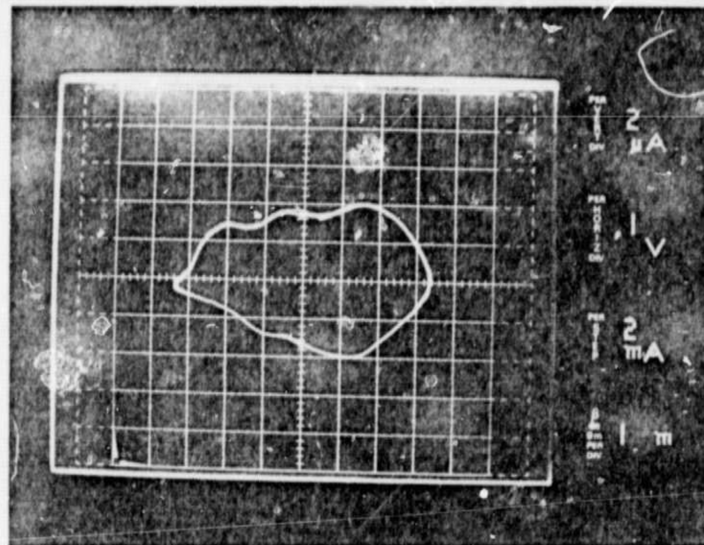
The etched portions of the wafers were analyzed using a hot probe and a four point probe. The hot probe showed that the silicon remained n-type over the entire surface of each wafer and the four point probe gave a sheet resistance measurement of approximately 500 Ω per square, regardless of the region probed. These results indicated that there is no doping effect due to the tantalum seed material used in the texturing procedure.

The second batch of textured wafers received, samples B-8, B-10 and B-11 were processed in the same manner as listed above and then characterized. Samples B-10 and B-11 were "washed" with an argon ion beam immediately after texturing in an effort to remove the tantalum seed material. The zero bias capacitance for the textured and nontextured surfaces for the three samples is listed in Table II. Samples B-8 and B-10 show approximately a 2.3 increase in capacitance per unit area while sample B-11 showed only a 1.33 increase in capacitance per unit area. The results are reasonable though since SEM photographs have shown a much finer structure on sample B-11. Thus, during the oxidation process a greater percentage of the textured surface is consumed by the oxide resulting in the smaller surface area.

These samples, like the previous batch, showed the diode-like current voltage characteristics. It was thought that the probing process may have damaged some of the cones in the previous batch and, therefore, these samples were coated with approximately 17,000 Å of aluminum to provide a sturdy probing pad. Even with careful lowering of the probe, I-V characteristics similar to that shown in Figure 2 were always obtained on the textured surfaces. This was true whether or not the surface was "washed". Figure 3a and 3b show the I-V characteristics for capacitors formed on the nontextured surfaces. The loops are characteristic of a good capacitor. Some of the capacitors on the nontextured surfaces also exhibited the diode-like characteristics so, at this point, one cannot be certain



(a) B-8



(b) B-11

FIGURE 3. I-V CHARACTERISTICS OF CAPACITORS FORMED ON NONTEXTURED SURFACES

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if the phenomena is due to the texturing process, the presence of tantalum on the surface, or some unknown contamination problem.

Samples B-8, B-10 and B-11, which had been previously textured, oxidized and tested, underwent the following additional processing:

1. RCA etch used to remove the aluminum on the front and back.
2. BHF used to etch the oxide.
3. Standard clean.
4. 10 min. dry O_2, 30 min. wet at 1050°C.
5. Aluminum dots evaported through a mask on the front side, 4640 Å.
6. Etch back side in BHF.
7. Metallize back side, 2000 Å.

Wafer B-11 did not have as "textured" an appearance as the others, but this is consistent with the SEM photos which showed a much smaller initial surface structure which was subsequently consumed by the growing oxide. Table III gives the average measured capacitance and breakdown voltage for the textured and nontextured surfaces. The larger effective surface area, as indicated by the measured capacitance correlates with the size of the surface structure and the effects of the oxide growth. It should be noted that the electrical properties improved after the second processing sequence, but the effective surface area decreased as expecte

Figure 4, 5, and 6 show the capacitance versus voltage characteristics (C-V) for samples B-8, B-10 and B-11, respectively. The lower trace in each figure is for the nontextured surface while the upper traces are for the textured surfaces. Two facts are apparent from the figures. (1) These devices exhibit a turn-on voltage of approximately -5 volts (point A on the figures) which is large for MOS devices. The value of -5 volts for the nontextured surfaces is more than three volts larger than one would theoretically expect for a good quality oxide. Tests were performed on virgin silicon wafers in order to evaluate the oxide growth process and those samples showed the expected turn-on voltage.

TABLE III. ELECTRICAL PARAMETERS OF MOS CAPACITORS FABRICATED ON TEXTURED SILICON

	TEXTURED		NONTEXTURED	
SAMPLE	CAPACITANCE	BREAKDOWN	CAPACITANCE	BREAKDOWN
B-8	630 pF	20 V	440 pF	200 V
B-10	530 pF	15 V	430 pF	200 V
B-11	490 pF	70 V	430 pF	200 V

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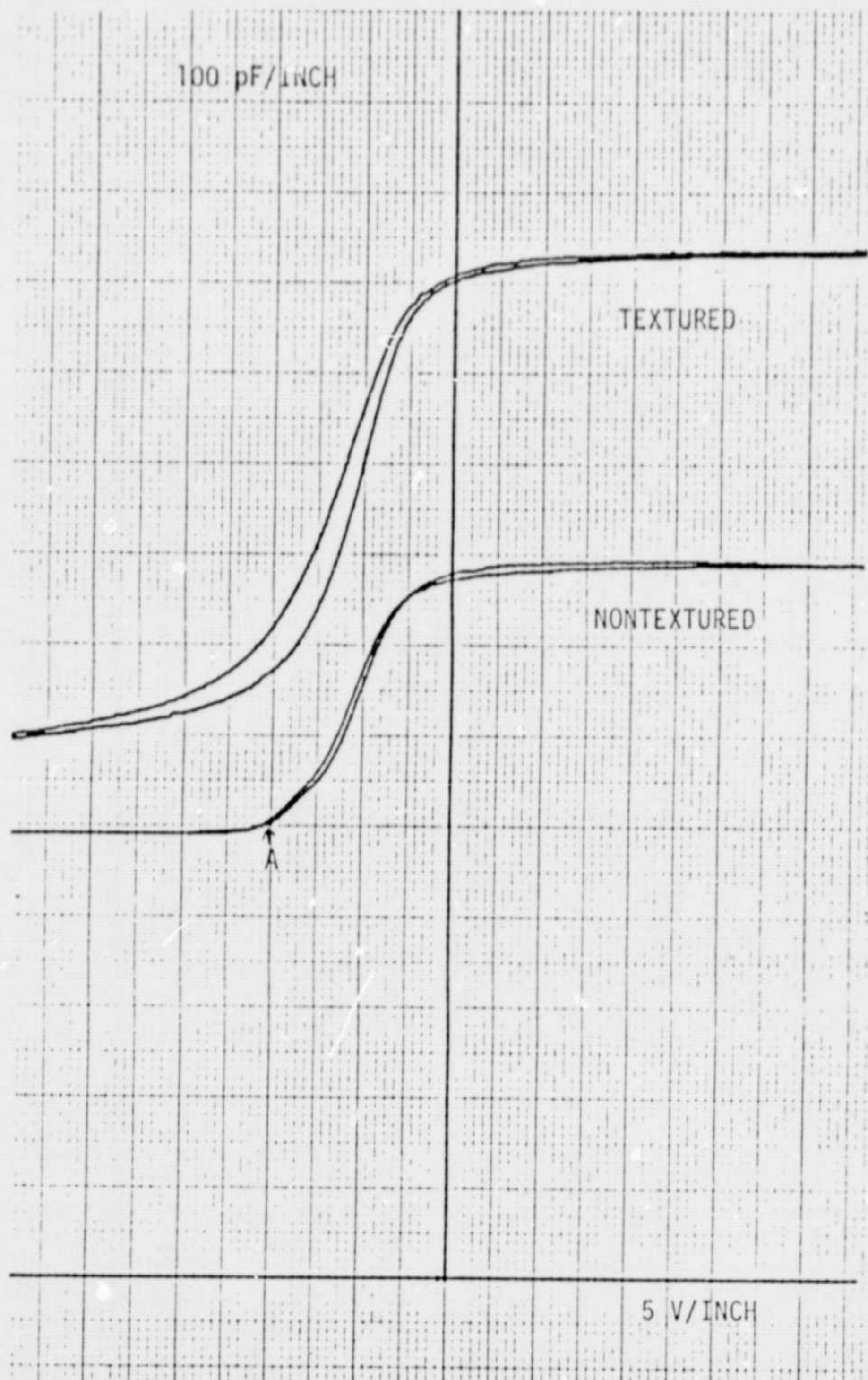

FIGURE 4. C-V Characteristics for B-8.

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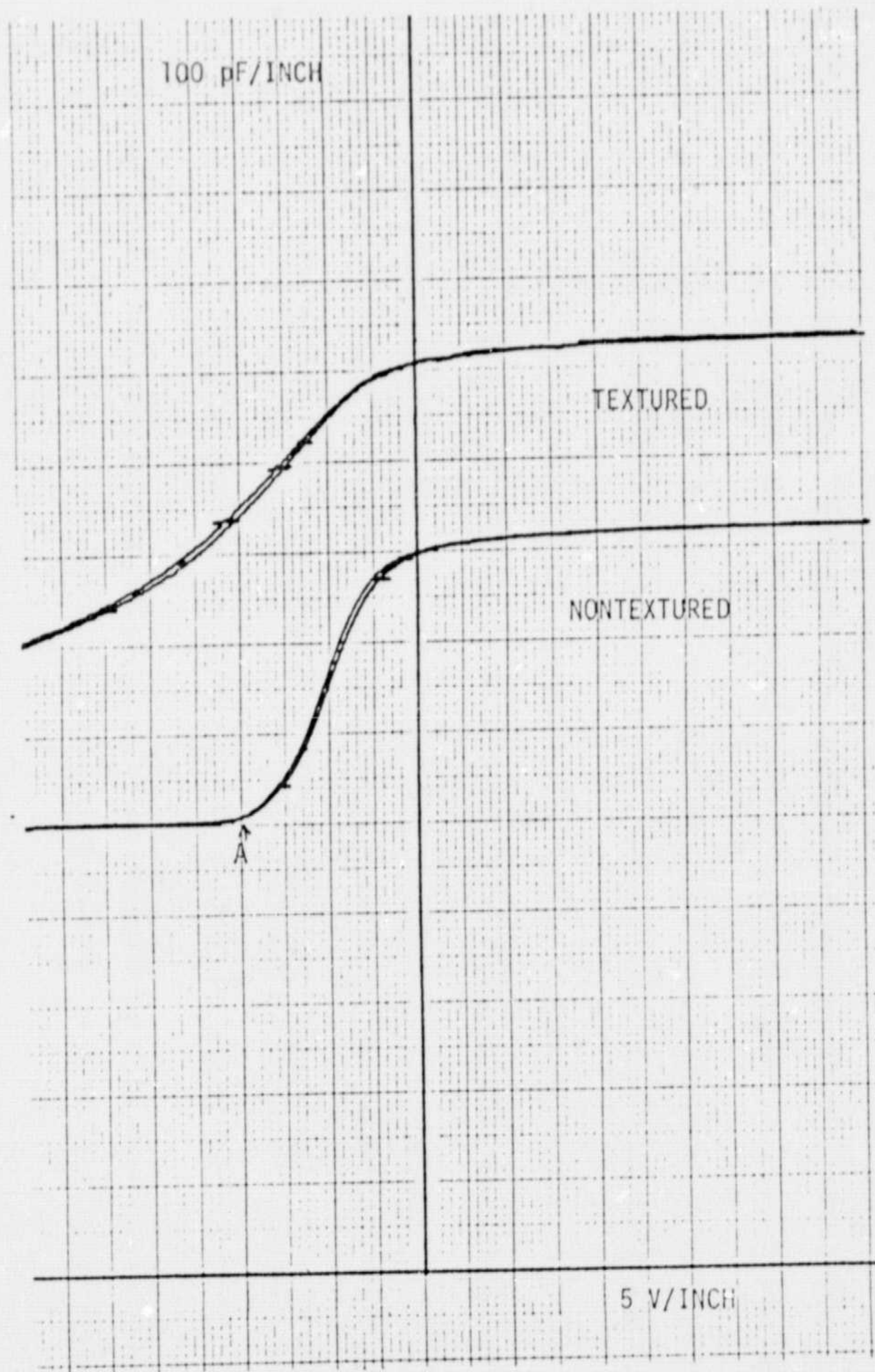

FIGURE 5. C-V Characteristics for B-10.

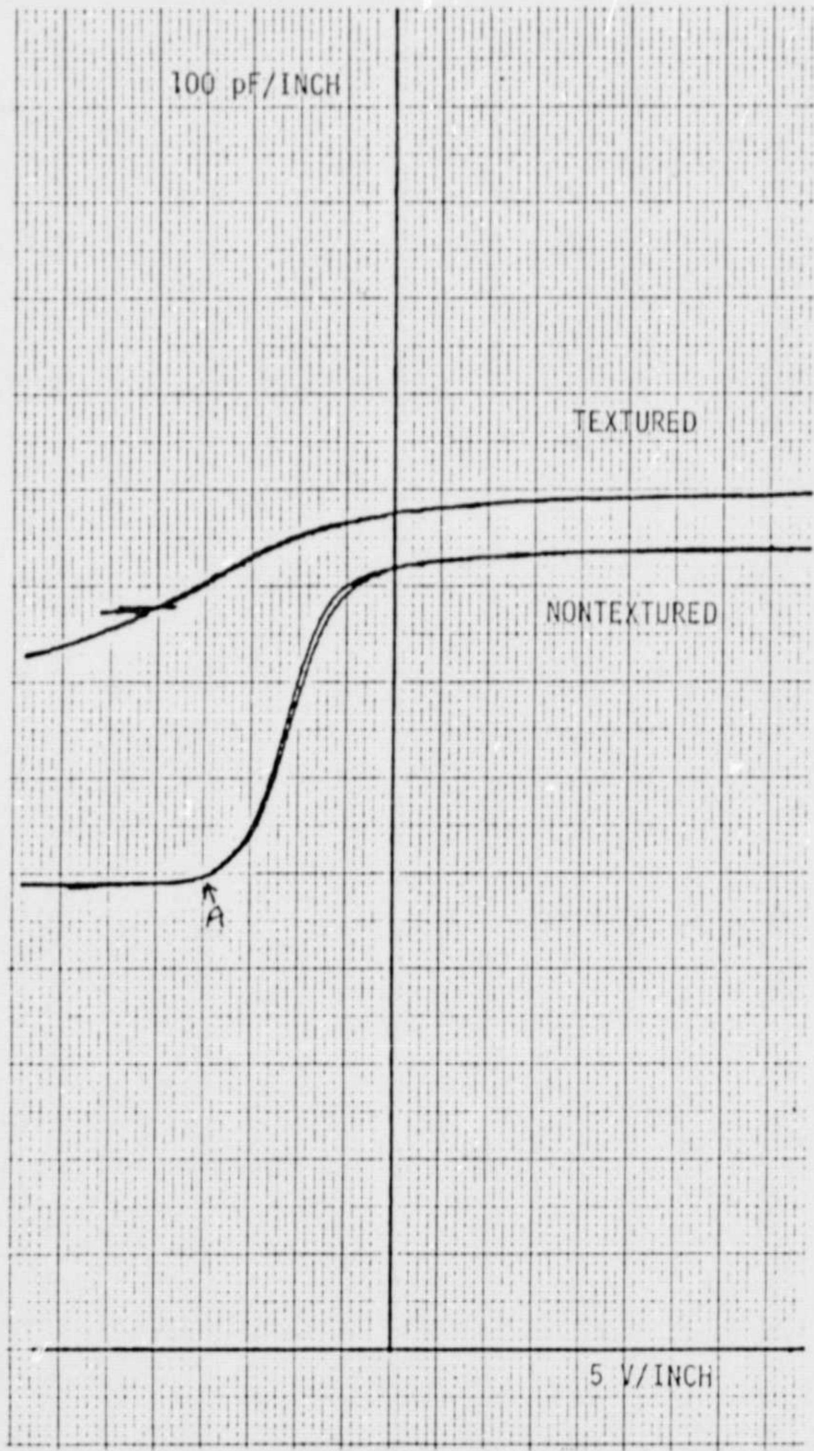

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FIGURE 6. C-V Characteristics for B-11.

(2) The textured surfaces exhibit an excessive number of surface states as indicated by the stretching of the C-V characteristic for negative voltages.

Although a higher effective surface area can be obtained using the ion beam texturing technique, the surface quality would not be suitable for active MOS devices. This does not mean that the technique cannot be used to fabricate high density MOS capacitors for integrated circuits. A great deal of work must be done to determine the origin of the diode-like characteristics of MOS capacitors formed on textured surfaces.

B. Ion Implanted Resistors

A second area in which it was felt that a textured surface may prove useful would be for resistors in integrated circuits. Resistors, like capacitors, consume a large amount of surface on an integrated circuit when compared to transistors, thus a method of reducing the needed area would be of value. Since the resistance value is a function of the length to width ratio on the silicon surface, a textured surface should effectively increase this ratio because the current flowing parallel to the long side will tend to avoid the peaks. This would cause the carriers to crowd into the regions between peaks thus reducing the effective width. In addition, those carriers which do partially climb the peaks will have a longer path to follow, thus increasing the effective length.

To test this hypothesis, five of the previously studied textured wafers (A-7, A-9, B-8, B-10 and B-11) were reprocessed to form ion implanted resistors. The wafers underwent the following processing:

1. Etch of aluminum and oxide
2. Standard clean
3. Grow 2000 Å oxide in wet O_2 at 1050°C.
4. Ion implant P+ contact pad after photo step.
5. Ion implant P resistor after photo step.

6. 900°C anneal
7. Open contact cutouts
8. Metallize and pattern
9. Sinter contacts.

Measurements were then made on the resulting resistors using micromanipulator probes and a curve tracer. Table IV gives the average resistance values for both textured and nontextured resistors on samples A-9 and B-10.

TABLE IV
ION IMPLANT RESISTOR VALUES

Sample	A-9	B-10
Textured	41.3 kΩ	42.7 kΩ
Nontextured	56 kΩ	50.4 kΩ

As the data shows, the resistors fabricated in the textured regions had a lower resistance value than those fabricated in the nontextured regions. This result was the opposite to what was expected. There are a number of possible explanations for the observed results which need to be more fully investigated. One is that there is increased conduction at the silicon-oxide interface due to surface states. This would be supported by the C-V characteristics which do show a large increase in surface states after the texturing process.

Another possibility is that during the ion implant step and the subsequent annealing, the impurities may have redistributed themselves such that the pn junction position is fairly flat when compared to the textured surface. If this is the case, the effective area perpendicular to the direction of current flow would be increased thus decreasing the measured resistance.

It is unlikely that there was a decrease in the length to width ratio due to poor photolithographic reproduction. In fact, microscopic inspection showed that the photoresist adherence was better on the textured regions and

that there was less undercutting.

Further testing is needed to fully evaluate the potential usefulness of fabricating resistors on textured surfaces.

C. Textured Silicon and Improved Wire Bonding

A third area investigated in conjunction with the texturing of silicon surfaces was the potential improvement in wire bond strength and reliability due to the presence of a roughened surface under the gold wire. The tests were conducted using the contact pads of the resistors discussed above. One mil diameter gold wires were thermocompression bonded from resistor to resistor to form wire loops. This was done in both the textured and nontextured areas. The samples were then taken out to the NASA Lewis Reliability and Quality Assurance Laboratory where lead bond pull tests were conducted. The results can be summarized as follows: Fourteen wire loops were pulled on the nontextured area of sample B-8. Of the fourteen leads pulled, only two bonds lifted. The force at which they lifted were 5 gm and 5.25 gm. The other twelve leads broke at forces between 4.75 and 8 gms with an average of 5.73 gm. Eight leads were pulled on textured contacts. In every case the mode of failure was wire breakage. The leads broke at forces between 5.0 gm and 8.25 gm with an average of 6.13. Since the weak link in the bonding was the wire and not the bond, no further tests were conducted. The experiment will be repeated but with 1.5 or 2 mil gold wire so that the actual bond can be evaluated.

III. Sputtered Ion Selective Membranes

A. Electrical Properties

The first ion selective material which we wished to study was polyvinylchloride containing valinomycin. Because of the cost of the valinomycin, this constituent was not put into the polymer mixture until the sputtering process was perfected. Targets were dip-coated using a mixture of 500 mg of polyvinylchloride,

1 cc of dioctyladipate and 8 cc of tetrahydrofuran. The tetrahydrofuran is a solvent and should not appear in the resulting film.

The initial experiments were used to determine the appropriate range of sputtering parameters such as accelerating voltages and current densities and led to the evolution of the present target holder. Because the polymer must be kept relatively cool, (less than 100°C), a quarter inch thick, three inch diameter aluminum plate is bolted to a water cooled copper coil. The quarter inch thickness was needed in order to maintain the flatness of the plate and, subsequently, good thermal contact with the water cooled coil. The edges of the target were rounded to avoid thin spots when the target was dip-coated.

Table V shows the deposition parameters for the four batches of samples received to date. The one sample from the first batch showed very good uniformity across the wafer and extremely good adherence compared to coatings placed on silicon wafers either by dip coating or spin-on techniques. There were no obvious film defects when observed under a microscope (400X).

The thickness, as determined by the quartz crystal monitor during the deposition (2700 Å) agrees quite well with the color bands observed under a microscope. The first order reddish-violet color combined with the published index or refraction of 1.54 would indicate a thickness between 2600 and 2800 Å.

Capacitors were formed using the PVC as the dielectric by evaporating aluminum through a metal mask to form metal dots with an area of 0.0896 cm^2. The capacitance, as measured with a capacitance bridge, averaged 3400 pF across the wafer. Using the formula

$$C = \frac{\varepsilon \varepsilon_o A}{d}$$

the dielectric constant for the PVC was calculated to be 11.5. This is well above the value of 3.39 published by the B. F. Goodrich Company. This measurement was made at 1 kHz.

Current voltage (I-V) measurements, using the aluminum dots as one electrode and the silicon as the other, showed diode-like characteristics after

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TABLE V. PVC SPUTTERING PARAMETERS

BATCH	BEAM ENERGY	BEAM CURRENT	EXPOSURE TIME	FILM THICKNESS
1	300 eV	11 - 32 mA	93 hrs.	2700 Å
2	300 eV	11 - 20 mA	57.5 hrs.	2000 Å
3	300 eV	13 mA	78.6 hrs.	1500 Å
4	300 eV	20 mA	48 hrs.	1900 Å

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a forward bias (aluminum positive with respect to the silicon) of more than 3 volts was applied. This is shown in Figure 7. The degradation was permanent once the breakdown voltage was exceeded. The forward turn-on voltage after breakdown was between 0.5 and 1 volt. Figure 8 shows an I-V characteristic obtained using a micromanipulator probe directly on the PVC. The circular trace is typical of a capacitor. When the voltage was increased to ± 60 volts, the PVC broke down beneath the probe. The resulting I-V characteristics are shown in Figure 9. Note that the curves in Figures 7 and 9 are similar in the forward direction but not in the reverse direction. This is most probably due to the difference in effective surface areas.

The I-V curves obtained using the aluminum dots seem to indicate that there are pinholes in the sputtered PVC which allows the aluminum to form Schottky diodes with the silicon. The relatively small area of the pinholes should not significantly affect the measured capacitance under zero bias conditions.

Because of the high quality of the PVC under visual observation, there was some question as to what caused the pinholes. One hypothesis, which was looked into further, was that the hot evaporated aluminum may have caused localized degradation of the PVC. One sample of the first batch had the aluminum dots etched off using concentrated hydroflouric acid (HF). The HF apparently does not attack the PVC. Microscopic inspection at X50 and X400 magnification showed no difference in surface appearance between the previously metal-coated areas and the uncoated areas. The sample was then etched in a silicon etch called CP4. Microscopic examination showed that the CP4 does not appear to attack the PVC, but pinholes are evident by the existence of etched silicon beneath the PVC. Figure 10 is a photomicrograph of the pinholes under X50 magnification. The ten second etch resulted in an observed pinhole density of about 3000 per cm^2. The distribution was quite uniform over the entire surface and showed no preference for the aluminum coated areas. This would disprove the

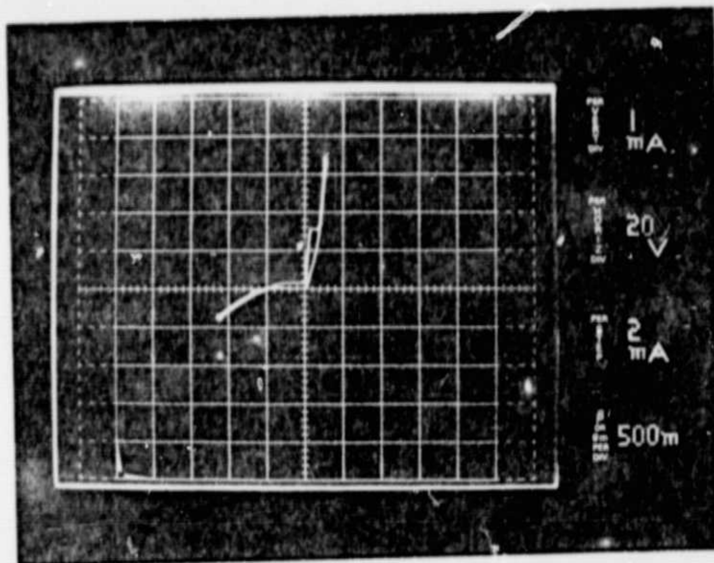

FIGURE 7. I-V CHARACTERISTICS OF PVC WITH ALUMINUM DOT

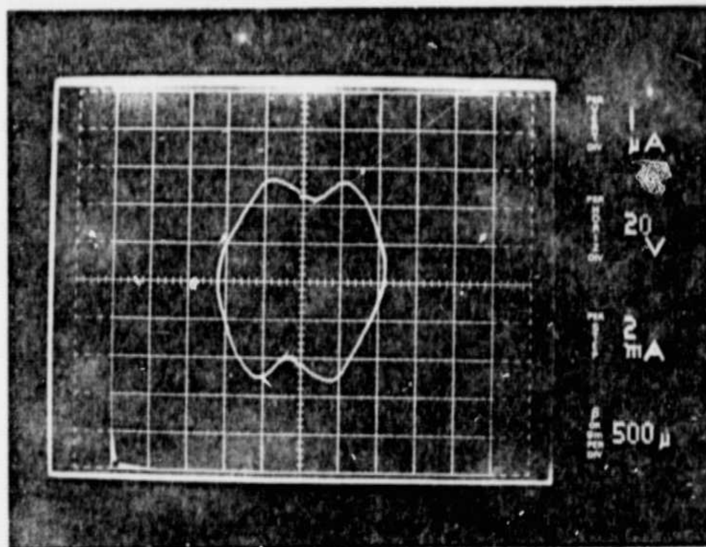

FIGURE 8. I-V CHARACTERISTICS OF PVC WITH POINT PROBE

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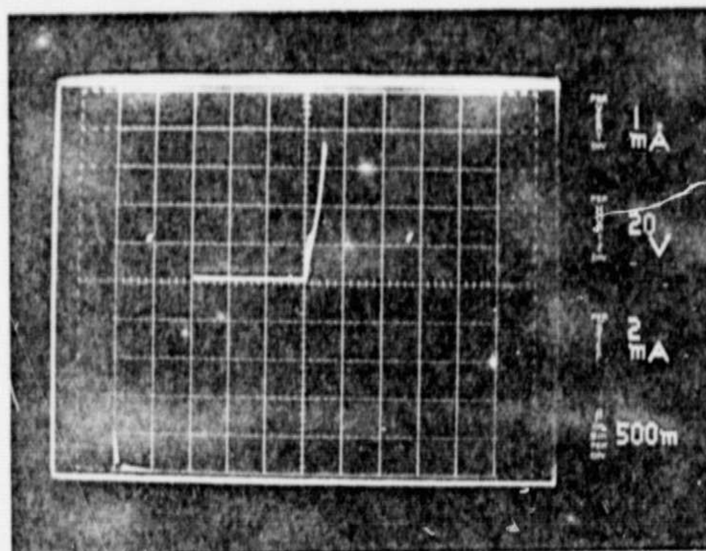

FIGURE 9. I-V CHARACTERISITCS OF PVC WITH POINT PROBE AFTER BREAKDOWN

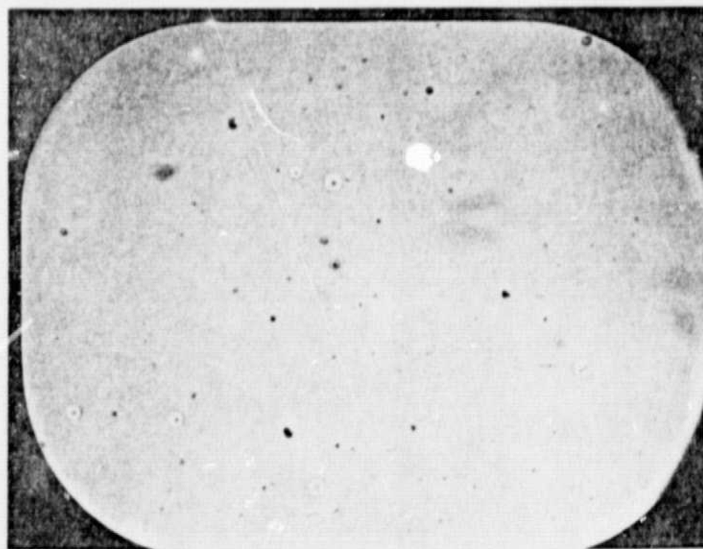

FIGURE 10. PVC SAMPLE ETCHED WITH CP4 TO REVEAL PINHOLES

hypothesis that the hot evaporated aluminum was causing the pinholes.

The size and density of the pinholes increased with increasing etch time. Thus, there is the possibility that the CP4 attacks the PVC. The same etchant (CP4) was used on sample 1 of the second batch of PVC coated wafers. Similar pinhole densities were observed.

Figure 11 and 12 show current versus voltage characteristics recorded using a jig which allows contact to be made to a circular area with a diameter of approximately 1/8 inch by means of a conductive solution, in this case, water. Figure 11 shows a loop typical of a capacitor. Figure 12 shows the same area after dielectric breakdown which occurred in the vicinity of +2 volts. The breakdown is believed to be due to the pinholes which exist in the film.

Table VI shows conduction data for a region of sample 1 which had not been previously broken down by a positive applied voltage. The data shows that conduction through the film has actually decreased with time up to the point of writing this report. These results would indicate that the sputtered PVC is impervious to water and, therefore, may prove to be a valuable protective coating.

Sample 3 of the second batch of PVC coated wafers had aluminum dots evaporated on the front side and aluminum on the reverse side for good electrical contact. Some of the test devices broke down at a few hundred millivolts positive which is similar to the results for the very first PVC sample. Some devices, however, did not break down as readily. This is shown by the I-V characteristics in Figure 13. These devices exhibited short bursts of current as tiny regions of the PVC broke down. This breakdown could be visually observed under a microscope and manifested itself as the appearance of small "bubbles" in the aluminum. This type of breakdown commenced at about 20 volts and increased with higher applied voltages. The density of "bubbles" was uniform across the dot. These broken down regions did not short out the device, but instead, they opened, thus allowing for further testing of the device. At 70 volts, there was a continuous current flow. This phenomenon was the same for both polarities of

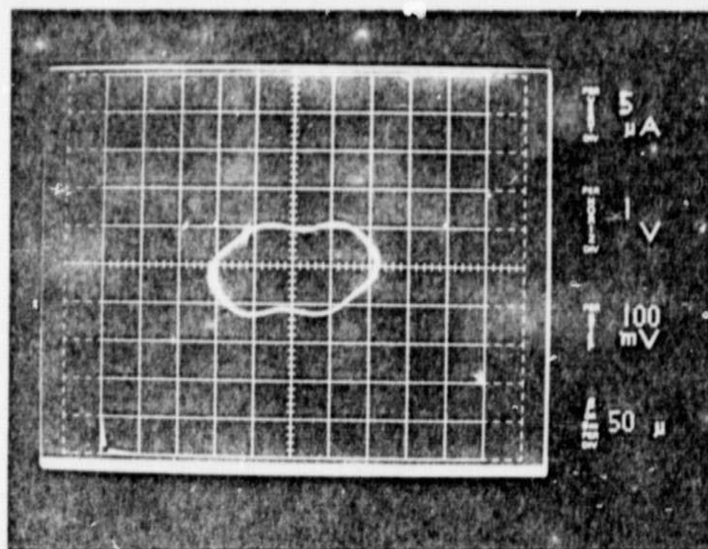

FIGURE 11. I-V CHARACTERISTICS FOR PVC SAMPLE BEFORE BREAKDOWN

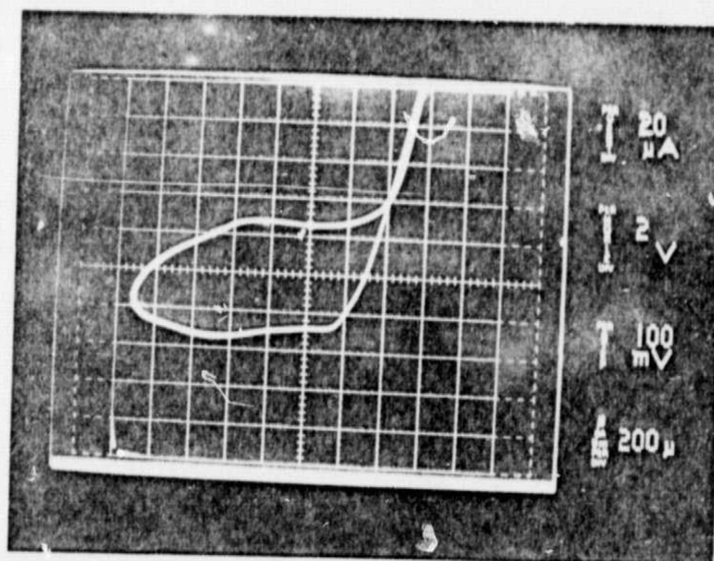

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FIGURE 12. I-V CHARACTERISTICS FOR PVC SAMPLE AFTER BREAKDOWN

TABLE VI

LEAKAGE CURRENT THROUGH PVC SOAKING IN WATER

DATE	I AT + 1V	I AT - 1V
5/19/77	25 nA	20 nA
5/20/77	5 nA	2 nA
5/23/77	5 nA	1 nA
5/26/77	2 nA	1 nA
6/01/77	2 nA	1 nA

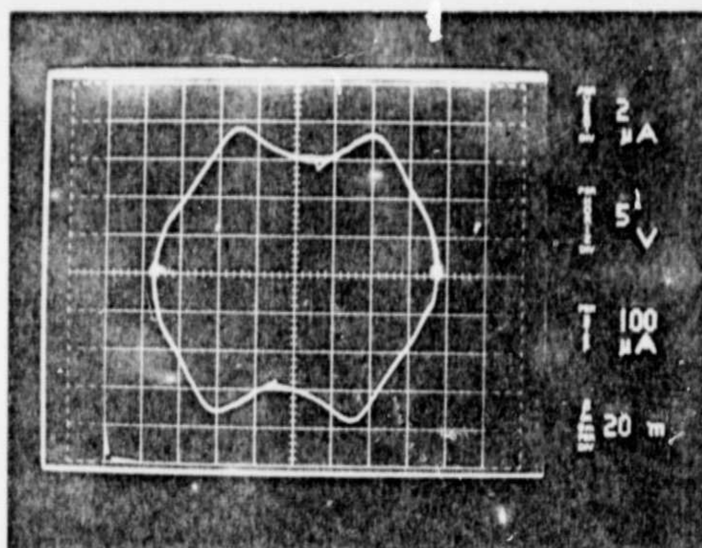

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FIGURE 13. I-V CHACTERISTIC OF A GOOD REGION OF THE PVC DIELECTRIC USING AN ALUMINUM DOT.

TABLE VIII

ESCA PEAK INTENSITIES FOR TARGET MEMBRANE, DIP COATED SAMPLE AND SPUTTERED FILM

SAMPLE	ELEMENT	PEAK INTENSITY (counts per channel)	O:C:Cl
TARGET	O	2545	1:1.92:0.194
MEMBRANE	C	4878	
(after sputtering)	Cl	495	
DIP	O	1753	1:1.7:0.193
COATED	C	2991	
SAMPLE	Cl	338	
SPUTTERED	O	1636	1:1.66
FILM	C	2714	
SPUTTERED	O	1321	1:1.79:0.124
FILM	C	2366	
REANALYZED	Cl	164	

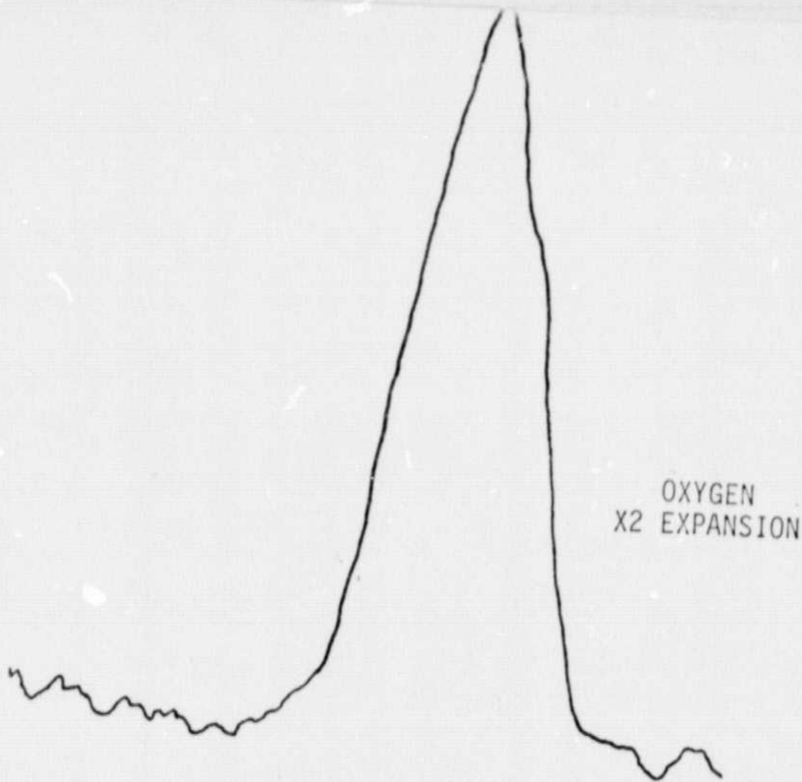
applied voltage.

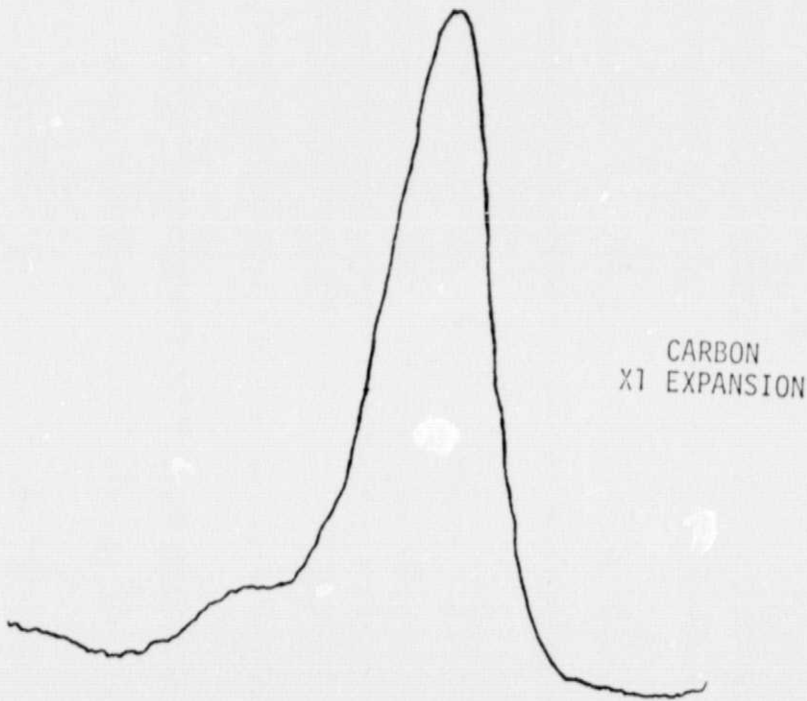
The capacitance at zero bias as measured by an HP 4260A Universal Bridge varied little regardless of the device's terminal I-V characteristics. Whether the device exhibited low voltage rectification, high voltage breakdown, or had the bubbles formed in the dielectric, the measured capacitance was always in the vicinity of 850 pF. Using 0.0372 for the area of the capacitor and 2000 Å for the thickness of the PVC as determined by the QCM and a color chart, a dielectric constant of 5.16 was calculated for the PVC film. This is quite a bit less than the 11.5 calculated for the first sample, but closer to the 3.39 published by the B. F. Goodrich Company. At this point, it seems that the electrical and physical properties of the PVC would be suitable for our ion sensor, but further characterization needs to be done.

B. ESCA Analysis

Electron spectroscopy for chemical analysis (ESCA) was used to characterize a dip-coated sample, a sputtered sample and the target material. From the ESCA data shown graphically in Figure 14a, 14b and 14c and numerically in Table VII, a number of observations can be made.

1. The composition of the dip-coated and sputtered films seems to be the same as far as oxygen and carbon content are concerned. Unfortunately, the operator who ran the samples for us initially omitted the chlorine region for the sputtered sample. The sputtered PVC film was analyzed again using ESCA. The data showed that the peak intensities for oxygen, carbon and chlorine were in the ratio 1:1.79:0.124. These results indicate that there is very little compositional change due to the sputtering process. Nothing is known, however, of the changes in structure which may have occurred.
2. The decrease of oxygen in the target after sputtering is most





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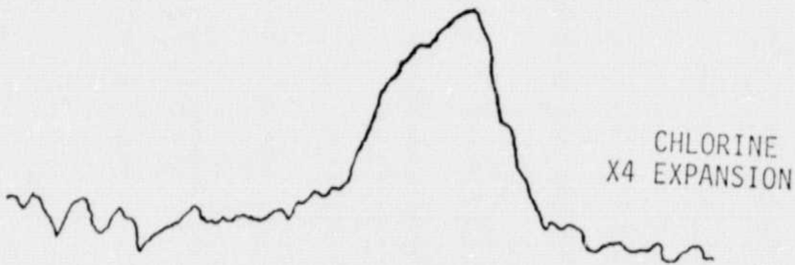


FIGURE 14(a). ESCA SPECTRA FOR DIP COATED PVC

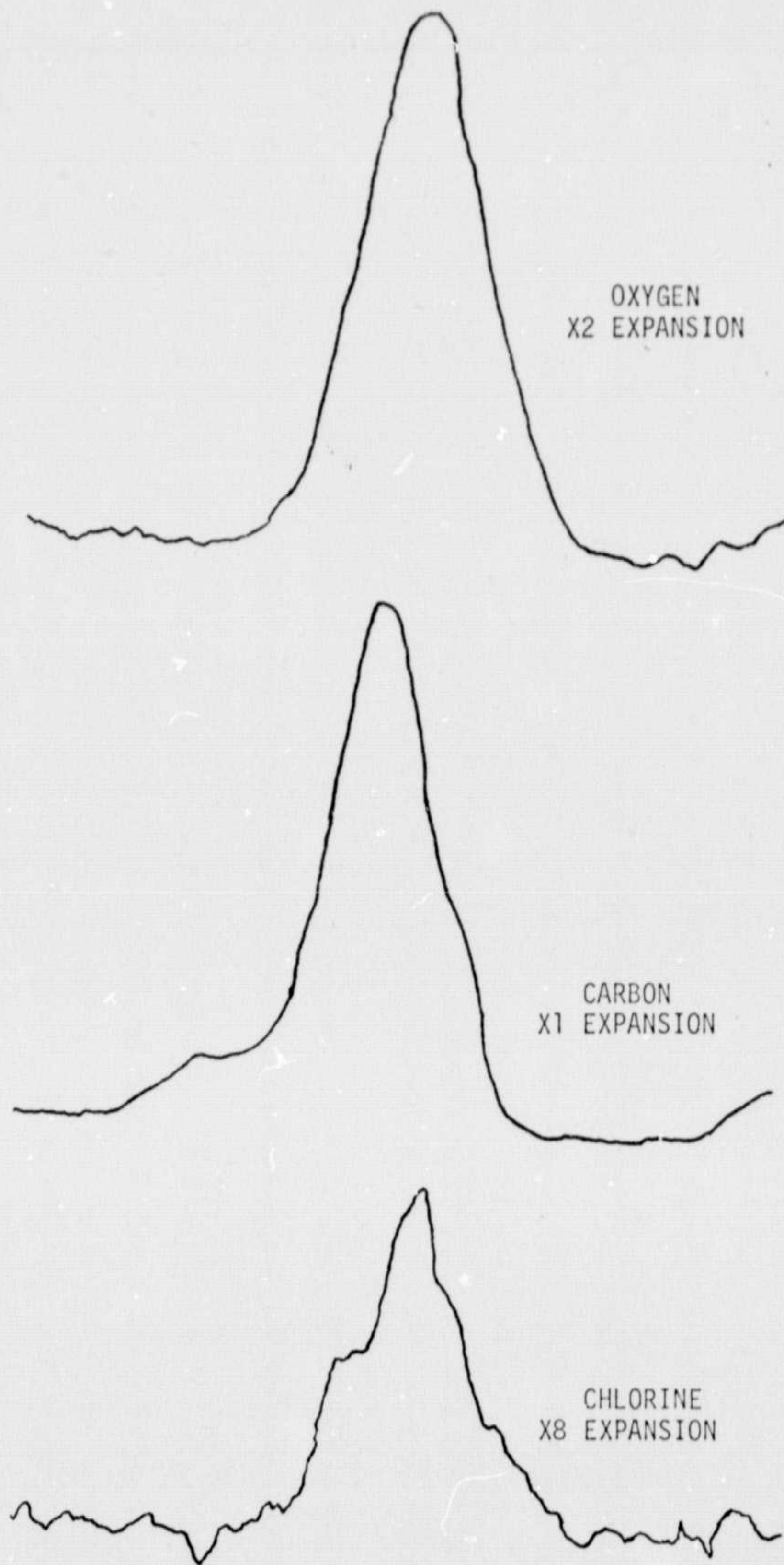
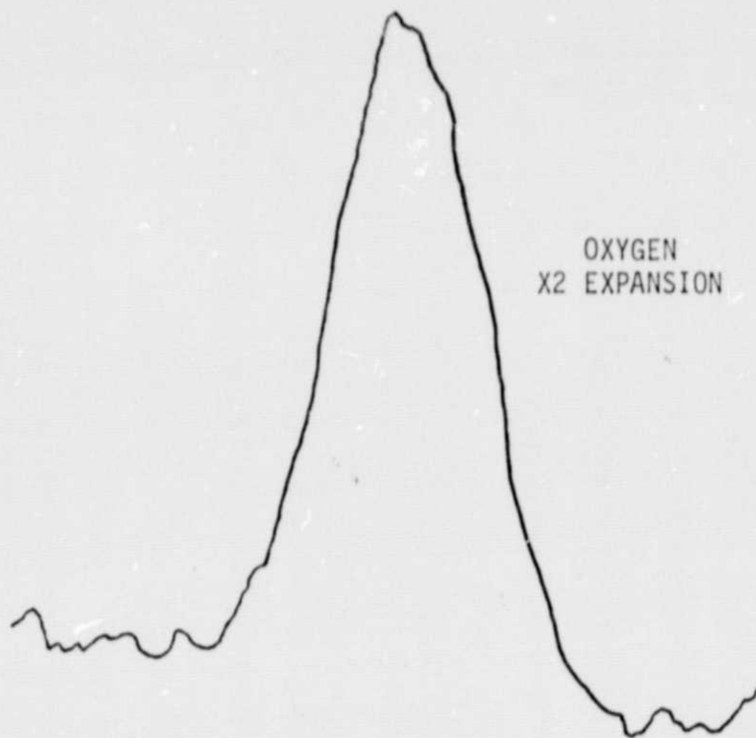


FIGURE 14(b). ESCA SPECTRA FOR TARGET MEMBRANE



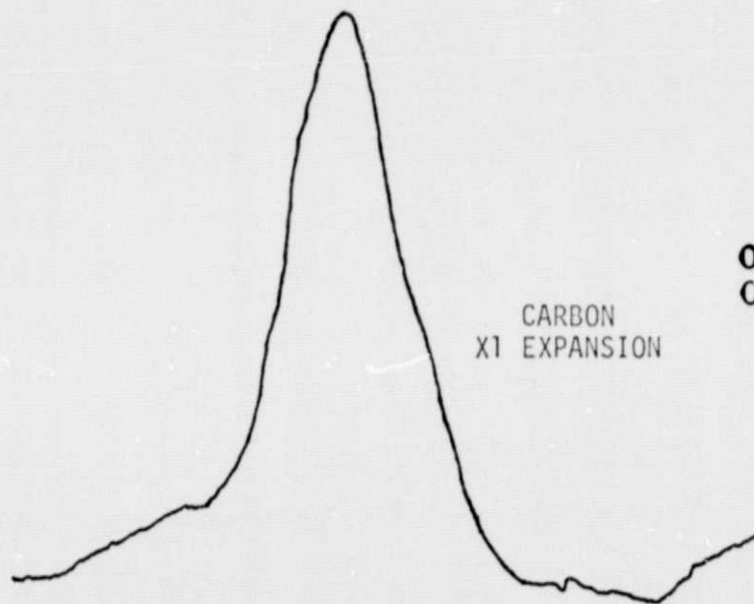


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FIGURE 14(c). ESCA SPECTRA FOR SPUTTERED PVC

likely due to the different sputtering rates for carbon and oxygen. The deposited film has the same apparent stoichiometry as the dip-coated film because of the compensation effect of the increased sputter rate and the decreased concentration.

3. The oxygen peak of the sputtered film is shifted approximately 1.4 eV toward higher binding energies and the half peak width has increased by approximately 20%. This would indicate not only a slightly different bonding structure, but also a mixture of bonding structures.

It is still too early to draw any definite conclusions at this point. Further tests must be performed.

Samples from the third batch were coated with PVC containing a small quantity of valinomycin and were evaluated. Measurements aimed at determining the sensitivity of these membranes to potassium ions were not conclusive. A number of times the measured interface potential changed by approximately the 59 mV per decade of ion activity predicted by theory, but at other times, the voltage change was erratic. This seemed to be due to the effects of static charges in conjunction with the high impedance of the electrometer and the PVC membrane. To avoid this problem, the next sputtered PVC membrane was deposited on the exposed gate dielectric of a p-channel enhancement mode field effect transistor. The low output impedance of the FET has been shown to simplify the measurement procedure for ion selective membranes.

C. Potassium Sensor

Two N channel FET's were sent to NASA Lewis to have a coating of PVC containing valinomycin sputtered over the active gate area. These devices were die bonded in flatpacks and all but the active gate area covered with a silicon rubber to protect the leads from the solutions used in the measurements. Prior to having the devices sputter coated, they were tested for sensitivity to pH.

The device designated #35 had a pH response of 16 mV/pH while device #H103 had a response of 25 mV/pH. These numbers indicate the change in gate voltage which would have to be applied to produce the same change in source voltage as caused by the pH solution. The measurement set up is shown in Figure 15.

During the sputtering process, the entire package was coated with the PVC membrane. No attempt was made to place the sputtered membrane only on the active gate area. The problem of using photolithography to define the areas covered by the membrane is yet to be investigated.

A bare silicon wafer was also sputter coated with the PVC. This was done in order to measure the electrical properties of the deposited film. For some unknown reason, the resulting film had a rather uniform distribution of irregular holes which were on the order of 10 mils across. These holes prevented the fabrication of capacitors for the measurement of dielectric constant, breakdown voltage and leakage current.

When tests were begun on device #35, it was discovered that none of the four field effect transistors was operational. This included two ion sensitive devices as well as two conventional MOS FET's. Because of the manner in which they are packaged, it is difficult to determine the cause of failure and no attempt has yet been made. For device #H103, there was no detectable response when subjected to buffer solutions ranging from pH 6 to pH 8. Figure 16 shows the measured response of the device when exposed to potassium ion solutions ranging from 0.01 M to 1 M. The slope for the three curves is approximately 18 mV per decade of potassium ion concentration. When this number is combined with the input to output transfer curve shown in Figure 17, the equivalent change in gate voltage is approximately 57 mV per decade which is quite close to the theoretical value of 59 mV per decade. Although the response is not truly linear, the results are still encouraging. A potassium ion sensor with similar characteristics has been fabricated[2] using a casting technique but the procedure is unattractive for batch processing or for producing multiple devices on a chip

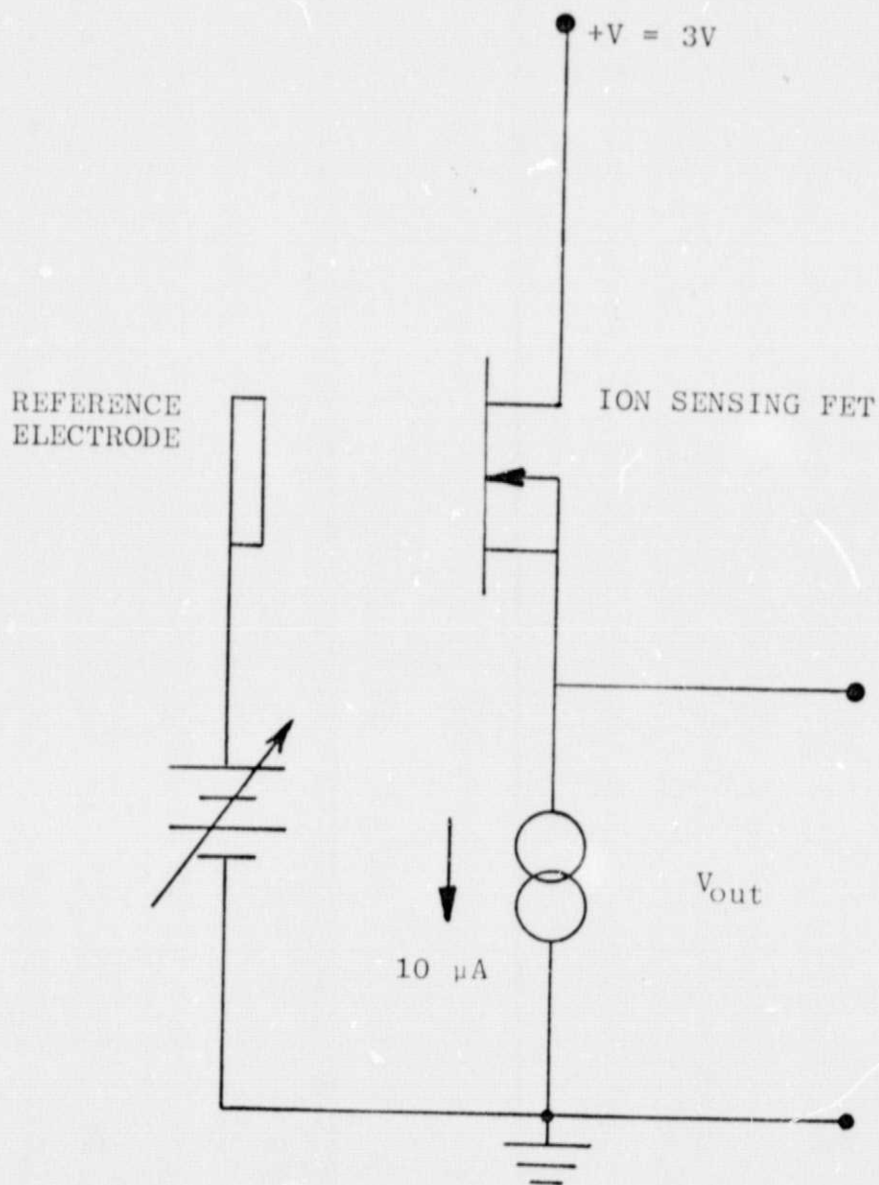

FIGURE 15. MEASUREMENT CIRCUIT FOR ION SENSING FET'S

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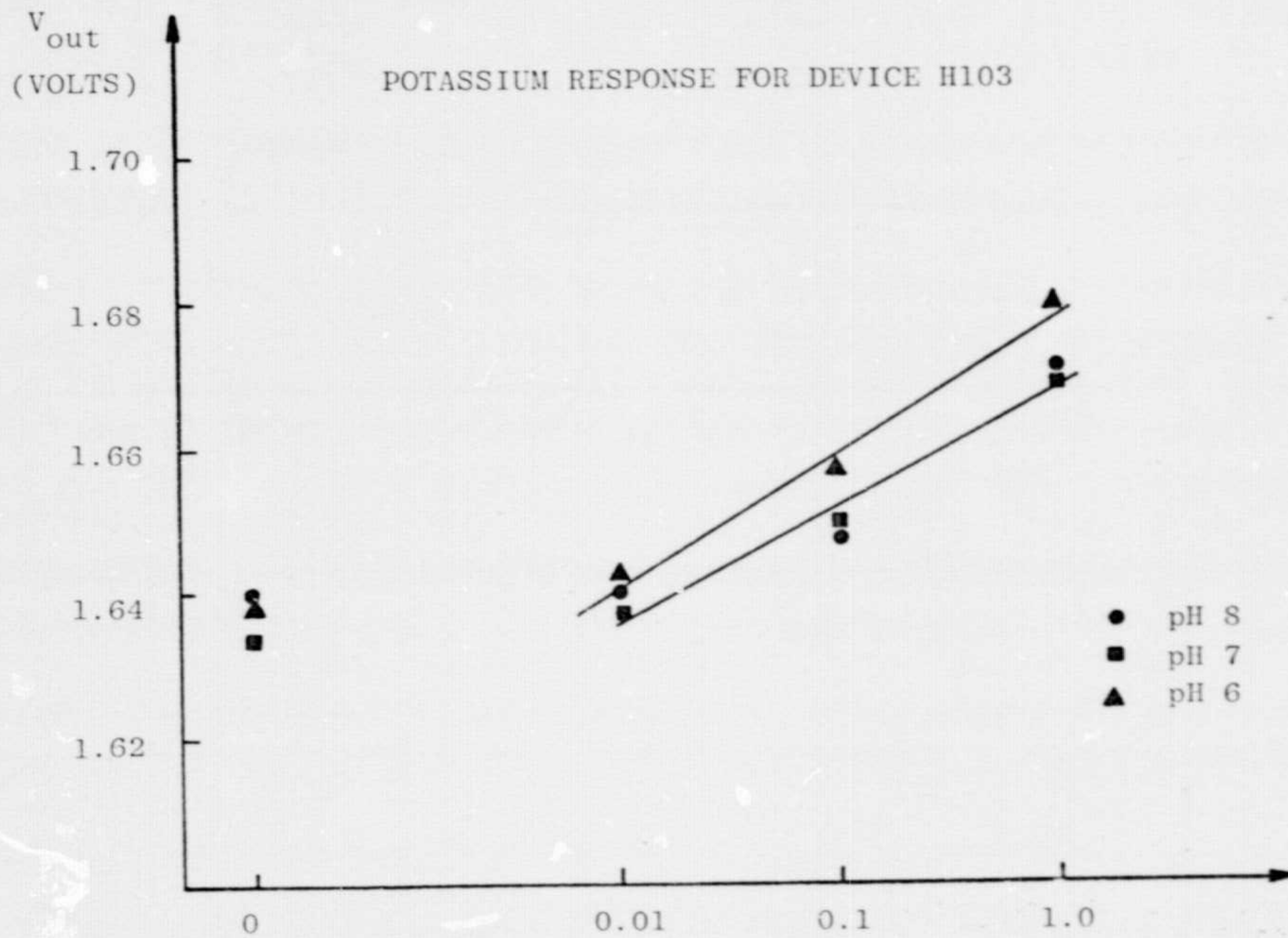

FIGURE 16. MOLAR CONCENTRATION OF POTASSIUM
POTASSIUM RESPONSE FOR DEVICE H103

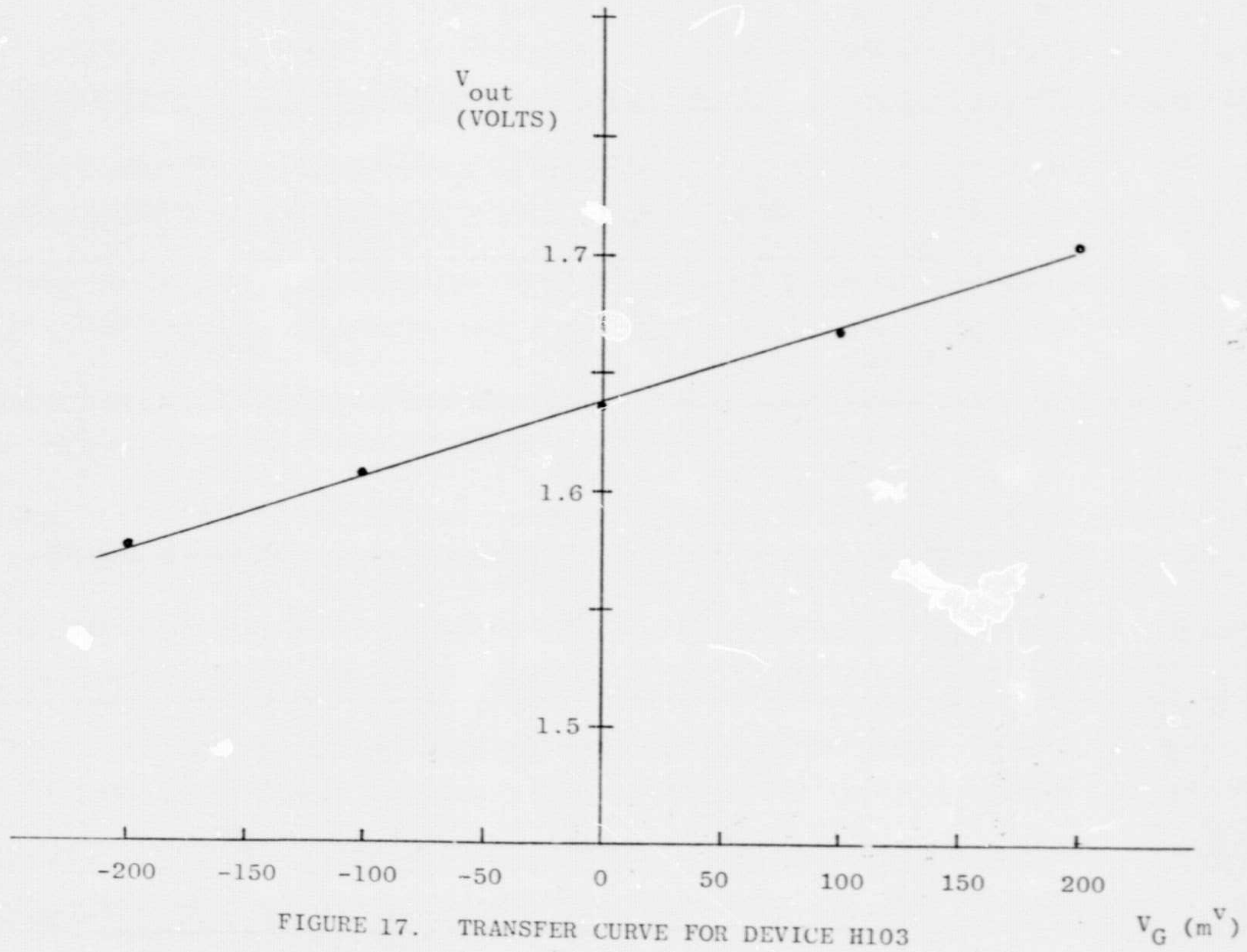

FIGURE 17. TRANSFER CURVE FOR DEVICE H103

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each sensitive to a different ion. With the proper photolithographic procedure, we should be able to use ion beam sputtering for fabricating multiple sensors on a single chip.

IV. Conclusion

The work of the first year has been used primarily to point out the areas which need to be investigated before textured silicon surfaces and ion beam sputtered membranes can be effective used in solid state devices and transducers.

In the area of textured silicon surfaces it has been shown that a two to three fold increase in effective surface area can be achieved for MOS capacitors. Work still remains on solving the low oxide breakdown voltage problem and studying the effects of the seed material on device characteristics. The large number of surface states at the oxide-silicon interface make the use of textured surface in active devices unlikely. A technique for selectively texturing silicon must be developed.

The tests on ion implanted resistors are not conclusive and further experiments needs to be performed to determine the effects of the textured surface on the resulting sheet resistance.

The study on increasing wire bond strength by the use of a textured bonding pad will be done again with larger diameter gold wire so that the bond will fail before the wire breaks, thus enabling us to compare textured and nontextured bonding pads.

In the area of ion beam sputtered membranes, the technique for sputtering PVC has been developed. ESCA analysis shows that there is some changes in the chemical bonding stucture after sputtering but the composition of the film is not changed significantly. The sputtering of a complex moleculer such as valinomycin in the PVC, with the retention of its chemical properties is encouraging. The fabrication of a potassium ion sensitive FET using ion beam

sputtering demonstrates the potential for multiple sensors each sensitive to a different ion on the same silicon chip.

In the future, work will continue in the two areas covered in this report with emphasis on the problems encountered. The sputtering of other ion selective membranes will be investigated as well as the sputtering of polymer materials as protective coatings for microelectronic devices.

V. REFERENCES

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2. S. D. Moss, J. Janata, C. C. Johnson, "Potassium Ion Sensitive Field Effect Transistor", Analytical Chemistry, Vol. 47, No. 13, November 1975, p. 2238.