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SILICON ON CERAMIC PROCESS

Silicon Sheet Growth Development for the Large-Area Silicon Sheet Task of the Low-Cost Silicon Solar Array Project

Annual Report No. 2

by

J. D. Zook, J. D. Heaps
R. B. Maciolek, B. Koepke,
C. D. Butter and S. B. Schuldt

Period Covered: 9/17/76 - 9/19/77

Published Sept. 30, 1977

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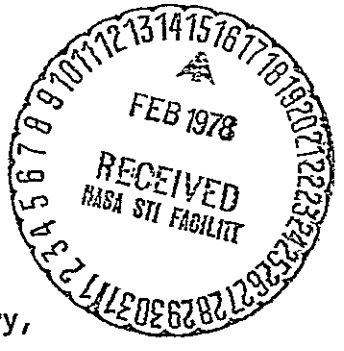

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the U.S. Energy Research and Development Administration, Division of Solar Energy.

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SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt. In the past year significant progress was made in all areas of the program.

The physical and chemical properties of the standard mullite refractory used for the majority of the coating runs (McDanel MV20 and Coors S1SI) have been characterized. A number of experimental compositions have been identified and procured from Coors. Characterization of the standard compositions revealed that the thermal expansion of mullite depends on both relative amounts of glass phase and on the impurity level in the glass. Since the thermal expansion in mullite exceeds that of silicon, the silicon coating should be in a state of compression. This was confirmed by x-ray measurements.

After modifying and cleaning the dip-coating facility, silicon on ceramic (SOC) solar cells were fabricated which demonstrate that the SOC process can produce silicon of solar cell quality. SOC cells having 1 cm^2 active areas demonstrated measured conversion efficiencies as high as 7 2 percent. Typical open-circuit voltages (V_{oc}) and short-circuit current densities (J_{sc}) were 0. 51 volt and 20 mA/cm^2, respectively. Since the active surface of these solar cells is a highly reflective "as-grown" surface, one can expect improvement in J_{sc} after an anti-reflection (AR) coating is applied. It is significant that single-crystal comparison cells, also measured without benefit of an AR coating had efficiencies in the 8. 5 percent range with typical V_{oc}'s and J_{sc}'s of 0 54 volt and 23 mA/cm^2, respectively. Therefore, improvement in cell design and junction diffusion techniques should increase the efficiency of both the SOC and single-crystal cells.

The surfaces of the SOC coatings are predominately {331} with a growth direction of <211>. This texture permits {111} twin planes to occur perpendicular to the substrate and propagate as the grain grows. This texture is similar to that observed in EFG ribbon silicon. Preliminary seeding experiments have been tried and while single-crystal silicon was not forthcoming, results were nonetheless encouraging.

As previously reported, mullite dissolves slightly in molten silicon. It is therefore encouraging to note that even when the melt is given a significant exposure to mullite, SOC solar cells can be made from the resulting silicon with V_{oc}'s and J_{sc}'s that are

within 9 percent of those obtained in single-crystal comparison cells. One method for inhibiting this substrate dissolution is to coat the substrate with a vitreous carbon which is impervious to molten silicon. "Vitre-Graf" coatings have demonstrated the feasibility of this concept. Another method is to modify the silicon coating technique in such a way as to reduce the contact area and time the substrate has with the silicon melt. A new continuous-coating facility has been designed and constructed to accomplish this and will soon be in operation. To date, chemical analysis techniques have not revealed any impurity segregation at grain boundaries, either before or after the junction diffusion process.

Electron beam-induced current (EBIC) and light beam-induced current (LBIC) techniques have been used to measure the base region minority carrier diffusion length (L_n). Both methods gave similar results but the LBIC method shows that L_n varies considerably, being relatively constant within a grain, and significantly reduced at grain boundaries.

Since the ceramic is an insulator it is anticipated that electrical contact will be made to the base region of the solar cell via small slots in the substrate. A contact-modeling study reveals that the slotted substrate concept leads to an appreciable series resistance problem unless the slots are made electrically conducting and the base of the silicon has a high conductivity layer at the back. Several carbon coating techniques have been investigated, some of which show promise of providing this needed additional conductivity.

An economic analysis of the SOC process has been completed. The study reveals that in a scaled-up process it is desirable to have silicon coating growth rates greater than 0.2 cm/sec. To date our best solar cells have been made on coatings grown at approximately one-fourth that rate. Emphasis is presently being given to increasing this growth rate without sacrificing the quality of the silicon coating.

INTRODUCTION

This research program commenced October 21, 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offer an outstanding cost-effective way to manufacture large-area solar cells. The dip coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers $25cm^2$ in area have been achieved with single-crystal grains as large as 4mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and rate at which the substrate is withdrawn from the melt.

The solar cell potential of this (SOC) sheet silicon is promising. To date 1 cm^2 solar cells have been fabricated, without the benefit of an antireflection (AR) coating and minimized series resistance, that have conversion efficiencies in the 7 percent region. Such cells typically have open-circuit voltages and short-circuit current densities of 0.51 volt and 20 mA/cm^2, respectively. Application of an AR coating to these cells would improve their efficiency in the direction of the program's ultimate 12 percent goal.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination and optimization of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The aluminum and other impurities of the substrate are believed to adversely affect solar cell conversion efficiency. A special type of graphite coating on the substrate has shown a potential for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar cell performance should be forthcoming. An alternate method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, as previously mentioned, a silicon coating facility has been constructed which is designed to coat large (10 cm x 100 cm) substrates in a continuous manner. It is expected that this new facility will not only improve the growth rate, but also minimize the silicon melt's contact with the substrate. This should reduce the rate at which the melt becomes contaminated. Further, this new facility will permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process.

TECHNICAL DISCUSSION

SUBSTRATE CHARACTERIZATION (B. G. Koepke, S. J. Marquardt and M. S. Smeltzly)

Introduction

The characterization and properties of the ceramic substrates are discussed in this section. To date, the ceramic found to be most suitable for coating with silicon is a refractory clay product (i. e. fireclay in the silica-alumina system containing about 55 wt. % Al_2O_3. The ceramic is a two-phase material containing interlocking crystallites of the mineral mullite (nominal composition $3Al_2O_3 \cdot 2SiO_2$) in a continuous glass matrix. The mullite-based refractory can be economically produced by firing naturally occurring clays and other minerals and has good high temperature properties and thermal shock resistance.

Two types of substrates are being produced for this program. Small, 1 1/2 x 2 x 0.100-inch substrates are used for coating experiments run in the small-dipping facility. Large 4 x 40 x 0.100-inch substrates will be used for coating experiments run in the scale-up continuous coating facility. Substrates are being obtained from two sources, the Honeywell Ceramics Center and Coors Porcelain Co. The types of substrates produced and the characterization of these substrates form the bulk of this section.

Substrate Compositions

Most of the substrates produced for this program have been a commercial fireclay refractory containing alumina and silica in the approximate ratio 55 wt percent/45 wt. %. The substrates of this composition produced at the Honeywell Ceramics Center were manufactured from premixed McDanel MV20 composition by rolling, drying and firing. Substrates of this composition obtained from Coors were designated S1SI and were produced by cold pressing and sintering. A number of substrates with experimental compositions based on variations of the MV20 - S1SI "theme" have also been produced and will be described.

Table 1 lists the approximate compositions of the McDanel MV20 and Coors S1Si mullite ceramic substrates. The data for the McDanel ceramic was obtained from a company brochure. The Coors analysis was based on analyses of the starting materials. The only notable difference between the two is the higher Ti in the S1SI.

Table 1. Composition of Mullite-Based Ceramic Substrates
(in wt. %)

Code	Material	Al_2O_3	SiO_2	Fe_2O_3	CaO	MgO	K_2O	Na_2O	TiO_2	B_2O_2	MnO	CaO	V_2O_5	Comments
						Commercial Compositions								
I	McDanel MV20	55.4	42.0	0.8	0.1	0.04	0.7	0.5	0.5					Nom. McDanel
		52.6	43.7	0.45	0.09	0.14	0.74	0.74	0.82					Coors Anal.
				1.27	0.15	0.33		0.38	1.30		0.07	0.01	0.07	Emission Spec
A	Coors SlSI	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12					Coors Anal.
II	McDanel MV30	60.0	38.0	0.5	0.1	0.2	0.5	0.08	0.5					Nom McDanel
		58.3	38.9	0.82	0.19	0.19	0.48	0.10	0.83					Coors Anal.
				0.79	0.04	0.33		0.13	0.90		0.012	0.01	0.03	Emission Spec
						Experimental Compositions from Coors Porcelain Co.								
B	High Mullite	67.2	31.4	0.45	0.02	0.01	0.16	0.18	0.54					Coors Anal
C	High Silica	52.2	44.7	0.56	0.13	0.22	0.83	0.22	1.01					Coors Anal
D	Boric Acid	56.7	38.3	0.61	0.13	0.24	0.90	0.24	1.10	1.50				Coors Anal
E	Open Porosity	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12					Coors Anal
F	High Purity	59.5	39.1	0.44	0.21	0.13	0.34	0.05	0.30					Coors Anal
G	Electrically Fused	77.5	21.9	0.12	0.00	0.00	0.00	0.35	0.05					Coors Anal
H	Reducing Fire	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12					Coors Anal

Early in the program a higher Al_2O_3 substrate was also obtained from the Honeywell Ceramics Center. The material was produced by slip casting from McDanel MV30 composition mix and contained about 60 wt percent Al_2O_3. The nominal chemical analysis of McDanel MV30 mullite is included in Table 1 along with analyses run at Coors. The agreement is reasonable. Semi-quantative chemical analysis using emissions spectroscopy was also performed on samples of MV20 and MV30 at Honeywell to determine the major metallic impurities. These results are also shown in Table 1. The major impurities from the standpoint of the electronic performance of a photovoltaic silicon coating are Ti and Fe.

The success of the coating experiments run with MV20 mullite prompted an effort to see if the properties of the substrate could be optimized by compositional modification. Based on discussions with M. Leipold of J. P. L. and engineers at Coors Porcelain Co. substrates with experimental compositions based on variations of the 55 wt. % Al_2O_3 composition were identified and have been produced by Coors. The experimental compositions are lised in Table 1 and briefly discussed below.

The high mullite and high silicon modifications were produced to determine whether the mullite or the glass phase dominates the thermal behavior of the substrate during the coating operation.

The boric acid modification is intended to be a body in which the glass phase is doped with B_2O_3 to produce a low-expansion glass and possibly act as a source of B in the silicon coating. The open porosity modification is a body intentionally produced with higher porosity. The higher porosity will enhance the thermal shock resistance and will allow deeper penetration of the silicon coating into the substrate. The high-purity modification is a body produced from starting materials selected for their low impurity content. As noted in Table 1 the Fe, Na and Ti are noticeably low in this material. The electrically fused mullite is produced from a mixture of electrically fused mullite and silica powders. The impurity levels in this material are understandably low. The reducing fire modification is a standard SISI mullite body that has been fired in a reducing atmosphere. The intent is to produce a material with high porosity that contains residual carbon in the form of unoxidized binder materials.

Since none of the experimental compositions have been coated with silicon at this time comments pertaining to compositional optimizations of the substrate will have to be referred to future reports.

A better idea of the phase relationships existing in fireclay refractories can be obtained from the alumina-silica equilibrium phase diagram of Aksay and Pask[1] shown in Figure 1.

Mullite is a compound that exists over a measurable range of compositions, and, according to Aksay and Pask, melts incongruently. Disagreements on the melting behavior of mullite still exist in the literature. Referring to Figure 1, the equilibrium structure at room temperature of a composition containing about 55 wt. % Al_2O_3 consists of mullite crystallites in a eutectic matrix consisting of a finely divided mixture of SiO_2 and mullite. In reality, the liquid present at the firing temperature (~1600°C) does not crystallize at the eutectic temperature and instead forms a continuous glass matrix around the mullite crystallites. It should be further mentioned that the clay starting materials do not contain any mullite but decompose during firing into a high-silica liquid into which the mullite crystallizes as firing proceeds.

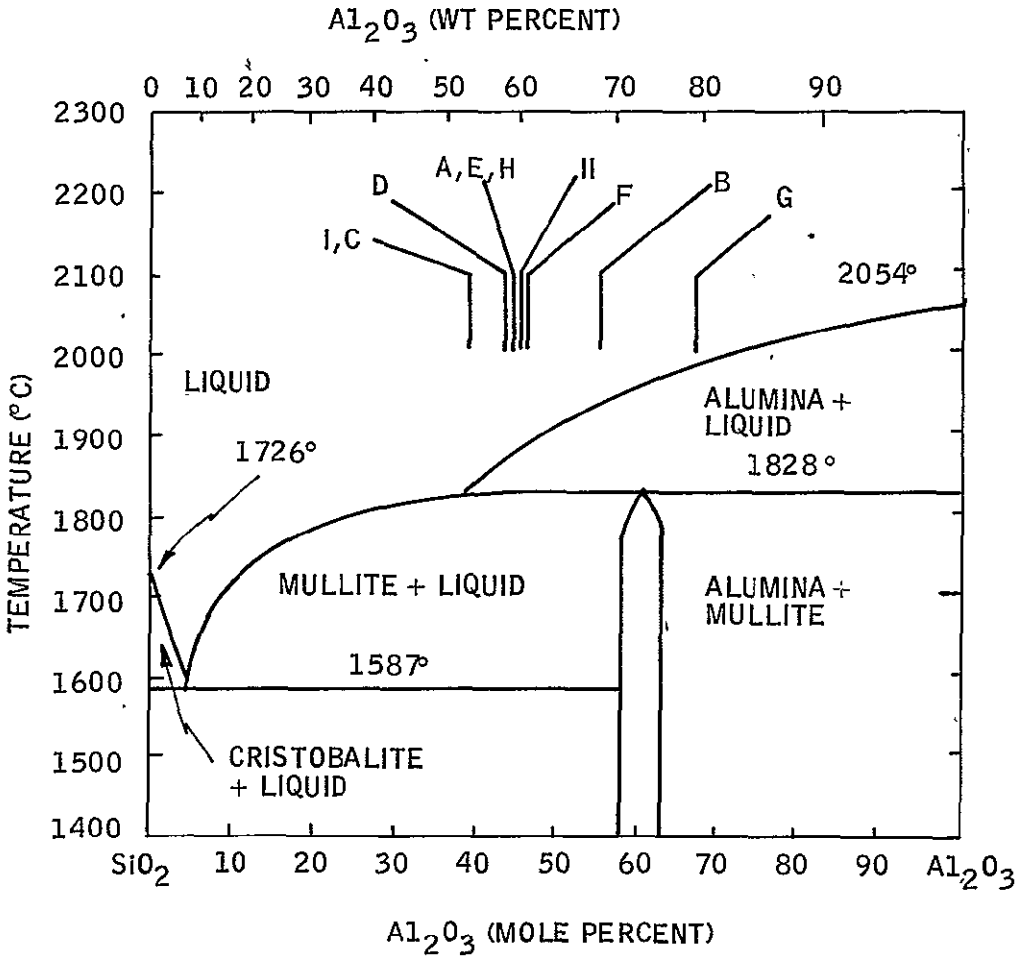


Figure 1. The Alumina - Silica Phase Diagram According to Askay and Pask. Also shown are the compositions of the various substrate materials currently being examined (the code letters are explained in Table 1).

Structure and Properties of Ceramic Substrates

The structures and properties of the substrates were measured at Honeywell and at Coors Porcelain Co. Microstructure, density and modulus of rupture (MOR) determinations were made at Honeywell's Corporate Materials Science Center (CMSC) and density, firing shrinkage, thermal expansion and x-ray percent of mullite were determined at Coors. The Honeywell Ceramics Center provided firing shrinkage data on the MV-20 and MV-30 substrates. A summary of the properties measured to date is given in Table 2. The thermal expansion of these materials is in accordance with the good thermal shock resistance of fireclay refractories. As shown in Figure 2 the thermal expansion of the mullites is slightly greater than silicon. Thus, after cooling to room temperature the silicon coating should be under a compressive stress. Preliminary x-ray measurements (discussed later) of residual stress in the silicon have indicated this to be the case.

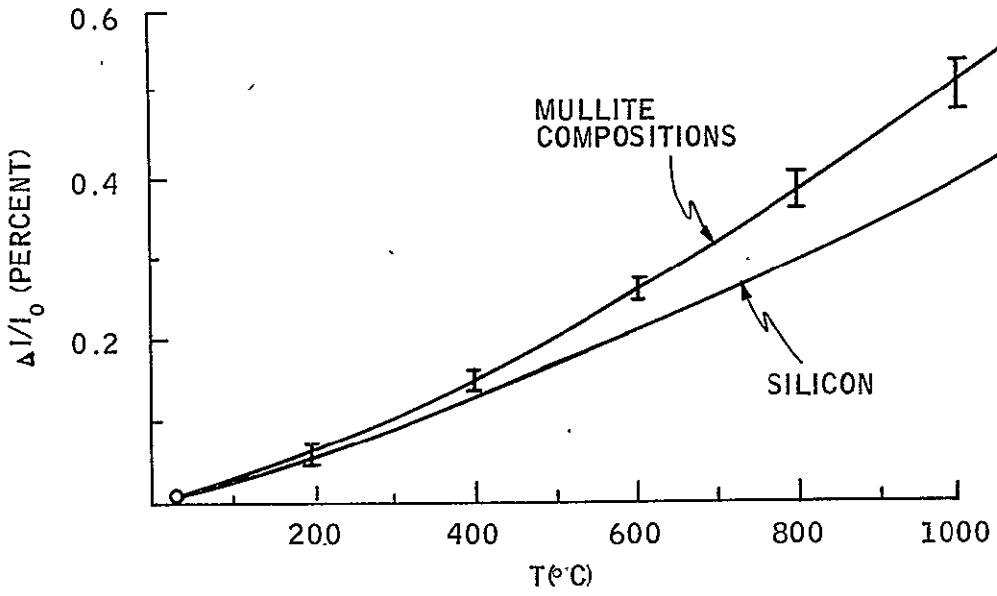


Figure 2. Thermal Expansion of Mullite Compared to Silicon

The strengths of the MV20 and boric acid modifications were the lowest of the group. The strongest samples were those containing greater amounts of mullite, i.e. S1SI and the high mullite modification and the material fired in a reducing atmosphere. Both the strength and thermal expansion affect the thermal shock resistance. Materials with low expansion and high strength, such as the high mullite modification, are expected to have good thermal shock resistance.

Table 2. Properties of Mullite-Based Ceramic Substrates

Code	Material	Density (gm/cc)	% Porosity	Thickness Shrinkage (%)	Length Shrinkage (%)	X-Ray % Mullite	Equil % Mullite	Thermal Expansion R.T.-1000C (%)	MOR (KPSI)
				Commercial Compositions					
I	McDanel MV20	2.50		14.0	10.2		74	0.495	15.3±1.5
A	Coors S1SI	2.70	0.32	12.1	16.7	76.5	81	0.520	23.7±1.4
II	McDanel MV30						82	0.470	
				Experimental Compositions from Coors Porcelain Co.					
B	High Mullite	2.86	0.22	12.1	12.7	70.2	95	0.485	25.9±1.2
C	High Silica					56.1	74	0.480	
D	Boric Acid	2.60	0.19	11.7	13.7	66.8	80	0.535	15.6± .7
E	Open Porosity	2.55	7.27	11.6	13.8	66.4	81	0.525	18.8±1.8
F	High Purity	2.70	0.53	14.9	19.5	66.8	84	0.510	20.1±1.0
G	Electrically Fused	2.6-2.8		10.4	11.3	84.2	87	0.530	18.6±1.4
H	Reducing Fire	2.7-2.9		12.5	18.1	66.4	81	0.515	23.8±1.6

The average thermal expansion of mullite from R. T. to 1000°C is 0.526 percent[2]. This value is at the upper limit of those listed in Table 2 and, as discussed later, indicates that the thermal properties of the glass phase rather than the mullite are dominating the properties of the substrates.

The microstructures of McDanel MV20 and Coors S1SI mullite refractories are shown in Figure 3. The light regions are mullite crystallites and the dark phase is the glass matrix. The S1SI structure has more mullite and less porosity. This is consistent with the data in Table 2; the S1SI has a higher density and contains more Al_2O_3, which corresponds to a higher mullite content. The microstructures of most of the experimental compositions were similar to those shown in Figure 3. The major differences were in the amounts of the phases (i.e. glass, mullite and porosity). The microstructure of the electrically fused mullite body is shown in Figure 4. The light areas are presumably mullite and the dark regions are silica.

Characterization of Acid-Leached Mullite Refractory

Most of the impurities in a mullite refractory are in the glass phase. In an effort to eliminate some of the impurities prior to coating, a number of pieces of McDanel MV20 were leached in HF to dissolve the glass phase. A scanning electron micrograph of a fractured cross-section of an MV20 substrate that was immersed in HF until about half the total cross-section had been acid leached is shown in Figure 5a. A higher magnification photo of the interface region at the bottom of the leached layer is shown in Figure 5b while a still higher magnification photo is shown in Figure 5c. The acicular morphology of the mullite crystallites that precipitated during firing is readily apparent. The structure appears to contain only the continuous-glass phase and the mullite needles. The results of EDAX analyses of regions in the center and at the edge of the leached sample showed that, as expected, the Al/Si ratio increased and the K and Ti were lower in the leached region. The Fe content was hardly altered by leaching.

Although the leaching operation lowered the surface impurity content it also weakened the substrate. Leached substrates that were carbon coated and dipped in silicon repeatedly fractured during dipping.

Residual Stress State in Silicon Layer

The residual stress in the silicon layer can be estimated from an expression used for stresses in glaze coatings applied to ceramics[3]. For a thin-silicon coating on an infinite substrate the stress at temperature, T is

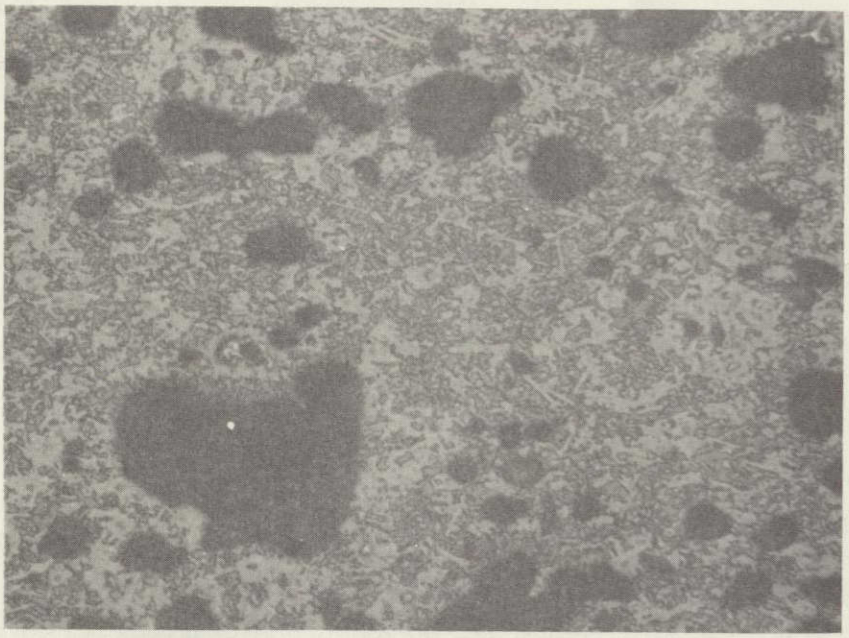


Figure 3(a). Optical Micrograph (325x) of McDanel MV20 Mullite Refractory, Specimen MR114

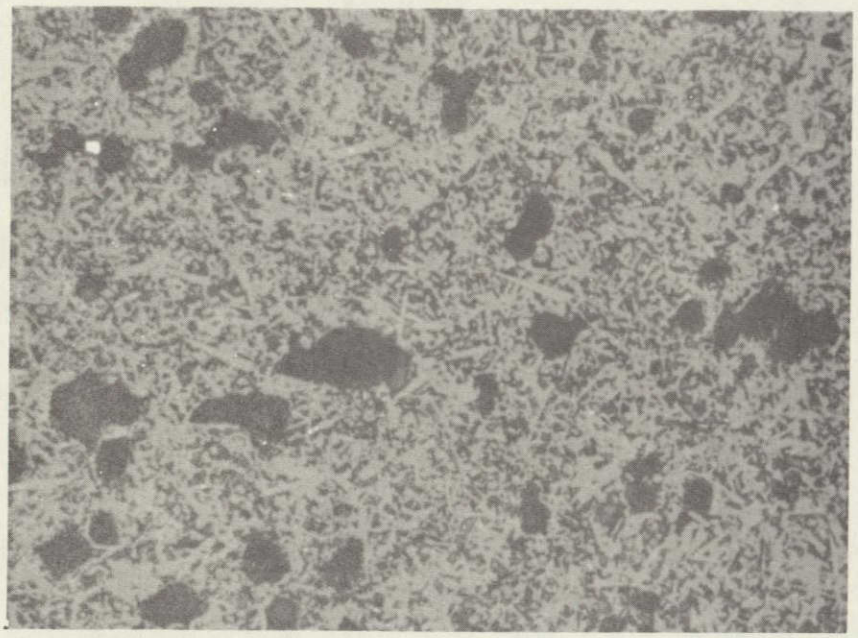


Figure 3(b). Optical Micrograph (325x) of Coors S1S1 Mullite Refractory, Specimen MC1

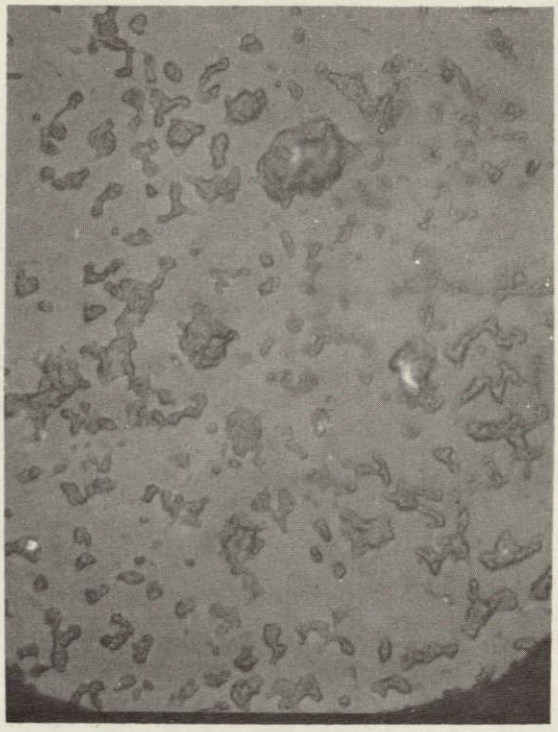
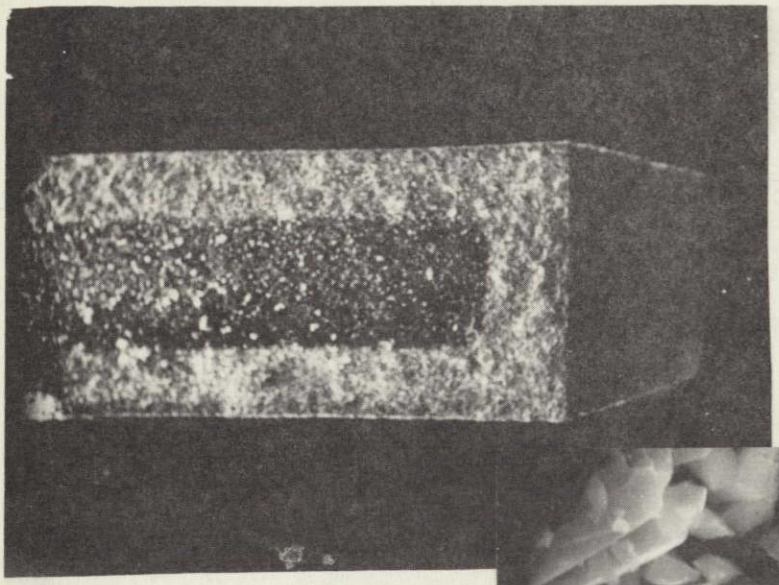
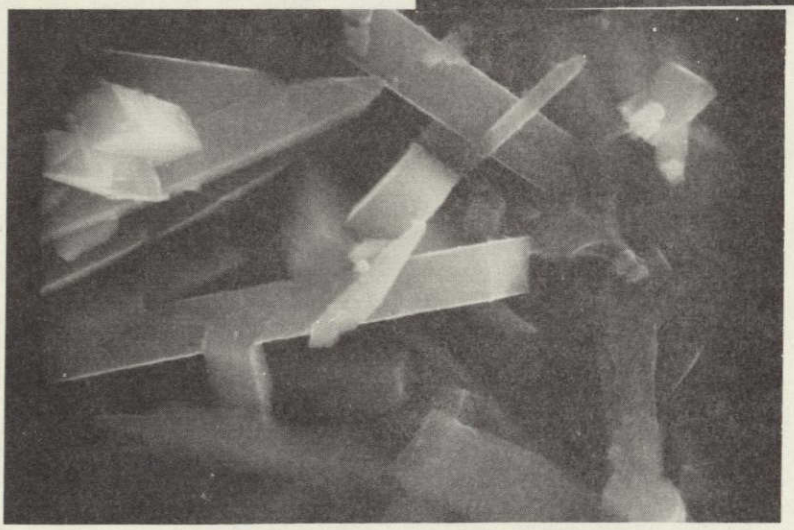


Figure 4. Optical Micrograph of Electrically Fused Mullite Substrate (500x)



(a) Sample at 20x

(b) Region at Base of Leached Zone (2100x)



(c) Region Near Linear Base of Leached Zone (5300x)

Figure 5. Scanning Electron Micrographs of a Fractured Surface of an MV20 Sample that had been Immersed in HF to Leach the Glass Phase to a Depth of Approximately One-Third the Specimen Thickness.

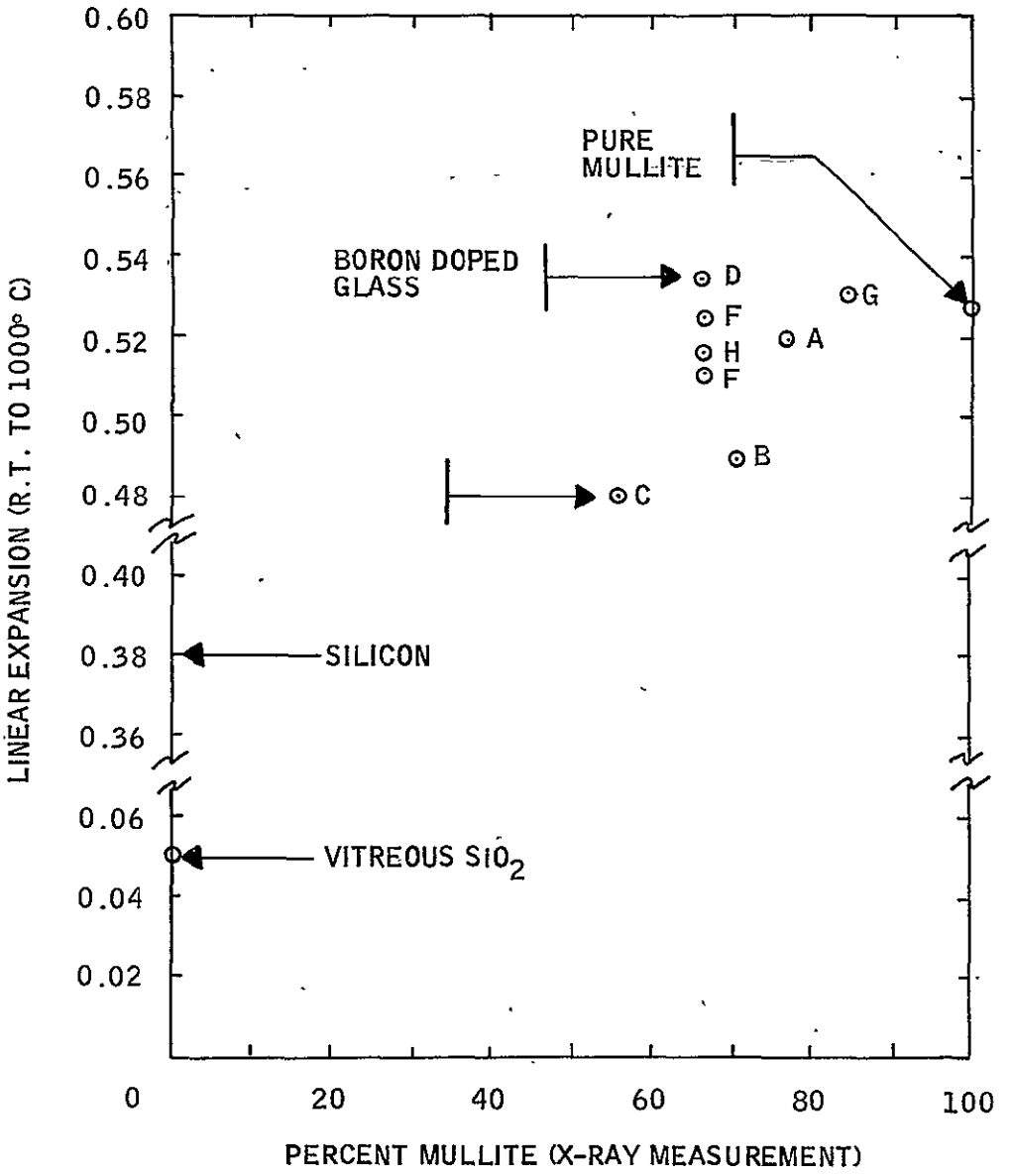


Figure 6. Thermal Expansion from 25°C to 1000°C of Experimental Substrate Materials Plotted as a Function of Mullite Content as Measured by X-rays. (The code letters are defined in Table 1)

as determined from Table 1 increases steadily through the series of samples with similar glass contents as follows: B, F, H, E, D.

The boric acid modification material (sample D) has the highest impurity content of all and the largest expansion. Sample A has the same impurity content as samples E and H but contains more mullite. Sample C has a higher impurity content than B but contains more glass. The conclusion here is that the thermal expansion of a mullite-based refractory is determined not only by the relative amounts of glass and mullite in the

material but also by the impurity content which primarily resides in the glass and alters its expansion. Impurities such as transition metals may be deleterious to the ultimate performance of the photovoltaic coating. Thus, if substrates were to be designed to be more thermally compatible with silicon, the most likely approach would be by altering the glass content rather than the glass chemistry.

SILICON ON CERAMIC COATINGS (R. B. Maciolek, D. Sauvy, S. Marquardt, and K. Wouri)

During the past year several changes were made in the dip-coating system with the objective of improving precision, reliability, ease of operation and coating quality. A 2 cm-diameter viewing port was installed in the top of the apparatus to make possible the direct observation of the melt and dipping process. Previously the process had been observed using a mirror which suffered from thermal distortion and which, in time, was obscured by vapor deposited material.

An unfortunate accident occurred during the second quarter which contaminated the inside of the melt chamber and prevented any dipping experiments from being conducted during most of the quarter. However, while the apparatus was being disassembled and cleaned the opportunity was taken to revamp the temperature control system and pulling mechanism.

It was decided that a poor impedance match between the Honeywell Dialatrol and the power supply controls was responsible for the unsatisfactory control. That system was discarded in favor of a properly matched one consisting of a Honeywell Deviation Set Point amplifier and a Honeywell Electr-O-Volt controller.

The cable-type dipping mechanism, which did not operate as smoothly as desired, was replaced with a ball screw drive mechanism. Both the temperature control system and the drive mechanism have been satisfactorily used in Czochralski-type crystal growth apparatus used in the Honeywell Research Center for the growth of high-quality optical and electro-optic crystals.

After the apparatus was cleaned and reassembled one of the first runs to be made was a dummy during which the melt was held at a typical growth temperature for six hours, but no substrates were dipped. This was done to check the cleanliness of the apparatus. Resistivity measurements made at the conclusion of the run were high, 100-1,000 ohm cm, n-type, indicating the melt had not been contaminated.

Starting with runs 55 through 77 helium, rather than argon, has been used as the atmosphere in the apparatus. The increased thermal conductivity of He permits higher growth rates and helps to suppress the collection of Si vapor on the viewports and chamber walls.

More recently, a gas mixture of He-10%H_2 has been employed as the atmosphere. The benefits, if any, derived from coating in the presence of hydrogen are currently being assessed.

During the third quarter, two more modifications were made onthe apparatus. First, a gas jet was installed inside the growth chamber so that the temperature gradient above the melt can be manipulated. Second, a new pull rod seal was installed and the pull rod itself highly polished to provide smoother mechanical motion upon withdrawal of the samples from the melt. The experiments with the gas jet were only partially successful as the gas flow caused the surface of the melt to solidfy as much as the material on the substrate. Redirection and/or a design of the nozzle should help alleviate this problem.

At the end of run 72 a chromel-alumel thermocouple was inserted into the apparatus in place of the pull rod to measure the temperature gradient above the melt. The result is shown in Figure 7. As expected, the temperature drop immediately above the melt is quite large, $\geq 200°C$ in 0.5 cm. The graph represents average values of continuous scans taken at 0.02 and 0.1 cm/sec. As the distance above the melt increased convection caused temperature fluctuations as large as 100°C.

A new numbering system which has been initiated to identify the samples incorporates certain information about the ceramic substrate and graphite coating. For example, 59-10M6H means the 59th run, 10th substrate dipped in that run; M is for McDanel, 6 is the Ceramic Center's batch identification, and H is for hand-rubbed graphite. The meaning of other letters which may appear is explained in the key at the bottom of the data sheet.

During the past year, 57 runs were made and more than 340 specimens were dipped for an average of six samples per run. The most samples coated in a single run during an eight-hour shift was 26.

Morphology and Microstructure

During one of the first quarter runs, ten substrates were dipped at an angle of 45 deg to the surface of the melt during insertion and withdrawal from the melt. The objective of this experiment was to see if changing the geometry of the meniscus would influence

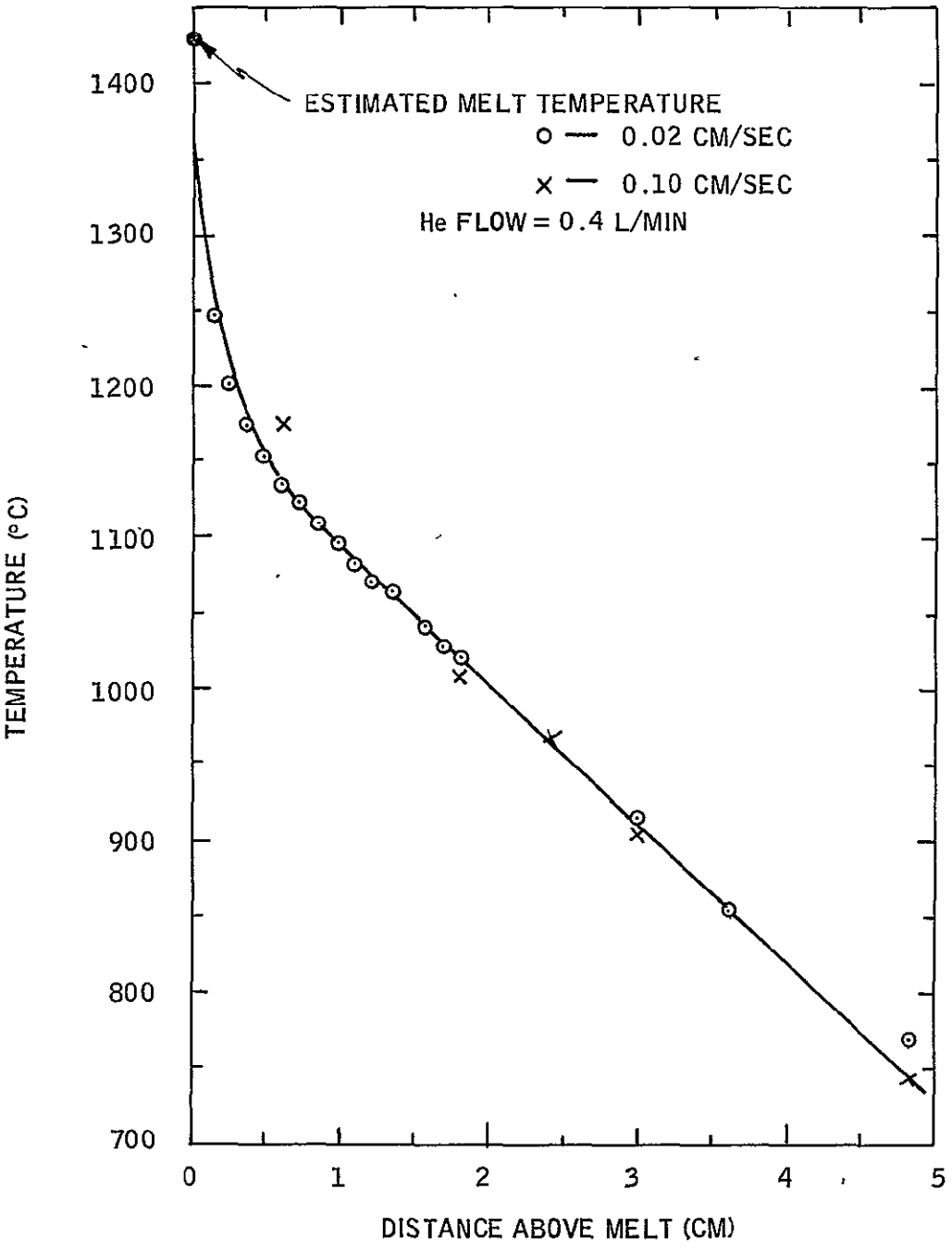


Figure 7. Temperature Gradient Above the Melt in Dip-Coating Facility.

the coating rate and/or quality. The principal parameters that were varied were pull rate and the sign of the dip angle (carbon-coated side of the substrate facing up or down). The pull rate was varied from 0.02 to 0.1 cm/sec.

Examination of the silicon coatings showed that angle dipping did not drastically alter the rate or manner in which the coatings solidified. The coatings looked quite comparable to those dipped vertically, with coating thickness decreasing with increasing pull rate. However, it appeared that the coating thickness of the angle-dipped samples was more uniform than those dipped vertically.

It was also interesting to note that those samples dipped with the carbon coating facing up came out of the apparatus with the silicon side clean (no vapor deposited material) and coated completely to the bottom edge, while those dipped with the carbon-coated side down came out with a light vapor-deposited coating and the last ~ 5 mm of substrate virtually bare. The cleanliness of the silicon surface can be explained by self-shielding of the silicon coating from the vapors coming off the melt, by the substrate in one case and direct exposure to them in the other. The lack of coating at the bottom edge of the samples dipped with the carbon side down is a consequence of the manner in which the liquid "bridge" between the substrate and melt surface is formed and broken at the instant the bottom edge is pulled from the melt.

Four substrates made from segments sliced axially from McDanel's MV-30 slip cast mullite tubing were also dipped. These samples were dipped vertically with the tube axis parallel to the pulling direction. The expected variations in coating thickness were observed as pull rates and temperatures were varied. However, in comparing the nature of the silicon on the convex surfaces to that on the concave surface it appeared that the dendrites formed on the convex surfaces were increasing in width at a somewhat higher rate than that observed on a flat surface. This could be due to either thermal or crystallographic conditions and will be investigated further. These sections of tubing yielded crack-free silicon layers with good adhesion and withstood the thermal shock of being immersed into molten silicon.

In the course of our work during the fourth quarter the effect of substrate width, relative to crucible diameter, on edge nucleation was examined. This was done by dipping substrates of various widths, 37 (standard size), 29, 26, 18 and 12 mm under constant conditions, melt temperature 1440°C and growth rate 0.05 cm/sec, and then examining the nature and extent of the growth at the substrate edge. It appeared that substrate size did not influence edge nucleation and growth. Samples coated under the same conditions showed the same type of edge structure; i.e., on each there was a region 5 mm wide in which the crystals grew in at an angle of 35-45 deg before impinging on the large crystals that were growing down the center portion.

Examination of the coatings grown at different temperatures and rates revealed that the width of the sideways growth region was reduced by the same factors that tend to reduce grain size in general (higher melt temperatures and faster growth rates).

An experiment was also conducted to evaluate the feasibility of coating patterns on the ceramic as defined by the carbon coating. This was done by applying the carbon to the substrate in a series of vertical stripes, 2-7 mm wide with a 2-3 mm spacing. With one run well defined silicon stripes were produced. On a subsequent run the silicon bridged the gaps between the carbon stripes and coated the carbon-free spaces on the substrate. The reason for this cannot be explained at this time but is being investigated.

The crystallographic texture of silicon on ceramic was determined by x-ray diffraction using the Laue method. Laue shots of individual grains were taken on samples MR45 and MR62. The surface of the coating was found to be predominately {331} with a growth direction of <211>. This texture permits a {111} twin plane to occur perpendicular to the substrate and propagate as the grain grows. This texture is similar to that observed in EFG ribbon silicon[5].

In an effort to promote large grain growth, four substrates were dipped with single-crystal Si seeds attached. Thin wafers of single-crystal Si were simply clamped to the substrate at the top edge of the carbon coating. The results can be seen in Figure 8 which shows the interface between the single-crystal seed and the ensuing silicon film. Although the desired result, single-crystal film growth, did not occur, the procedure shows promise. The seed-film junction is continuous, indicating that with a suitably oriented seed, large grain growth may be induced.

Dislocation density of the silicon coating was investigated using the etch pit technique. Figure 9 is an optical photomicrograph of the etched as-grown surface of sample MR114. Note that certain areas between twin boundaries are dislocation free. The dislocation count obtained from this surface was $\sim 9 \times 10^6$ cm^{-2}. Figures 10 and 11 show optical photomicrographs of polished and etched cross sections of sample MR114 taken parallel and perpendicular to the pulling direction; the dislocation counts from these two surfaces were $\sim 8 \times 10^6$ and $\sim 6 \times 10^6$ cm^{-2}, respectively.

Carbonization

In an effort to identify alternative methods of carbonizing the ceramic, several different techniques were tried during the year. First, four mullite substrates which had a Vitre-Graf graphite coating on all surfaces were dip-coated. The coatings were prepared by

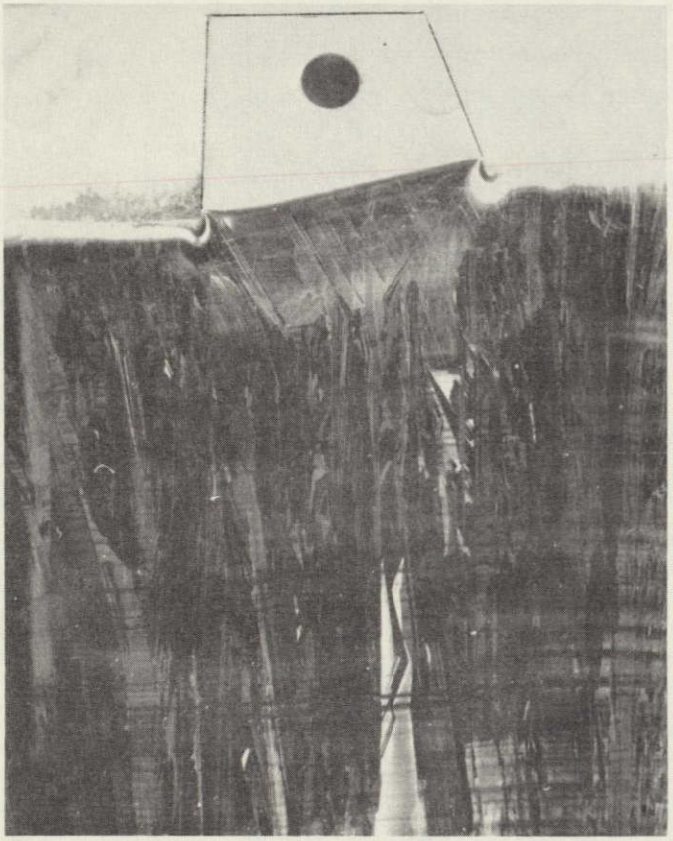


Figure 8. Seeded Si Sheet Growth. The seed in the trapezoidal shape at the top of photo (Wright etch, 2.5x).

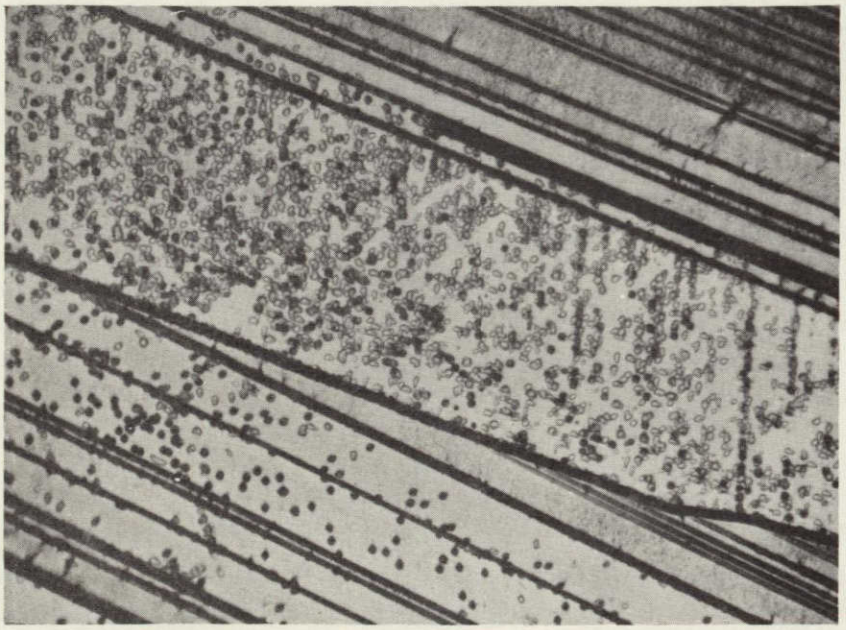


Figure 9. Optical Micrograph (500x) of Etched As-Grown Surface (Sample MR114) Showing Dislocation Etch Pits

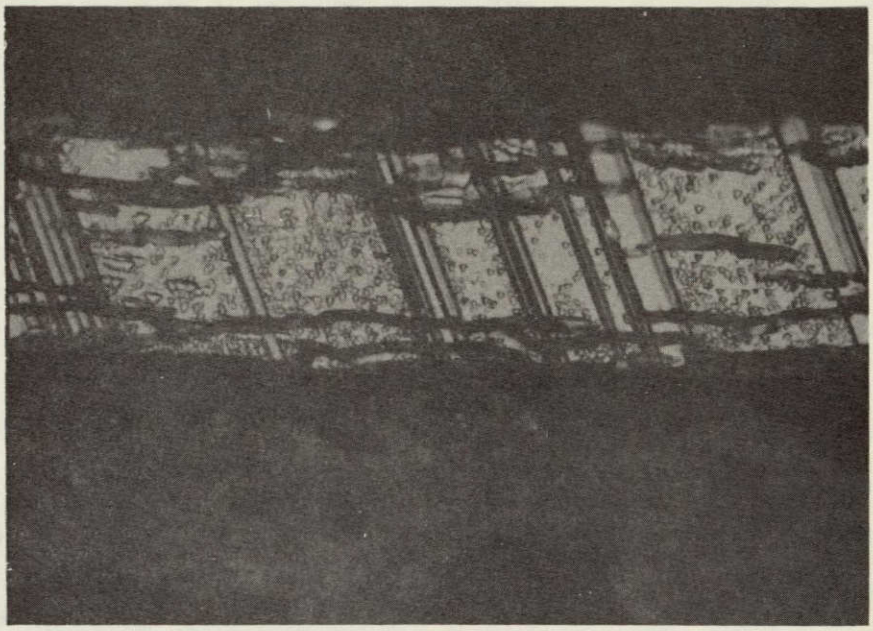


Figure 10. Optical Micrograph (500x)of Polished and Etched Cross Section of Silicon Coating, Sample MR114, Taken Parallel to Pulling Direction; Etch: Sirtyl; Time: 15 Sec. ; Dislocation Count ~8 x 10^6 cm^{-2}.

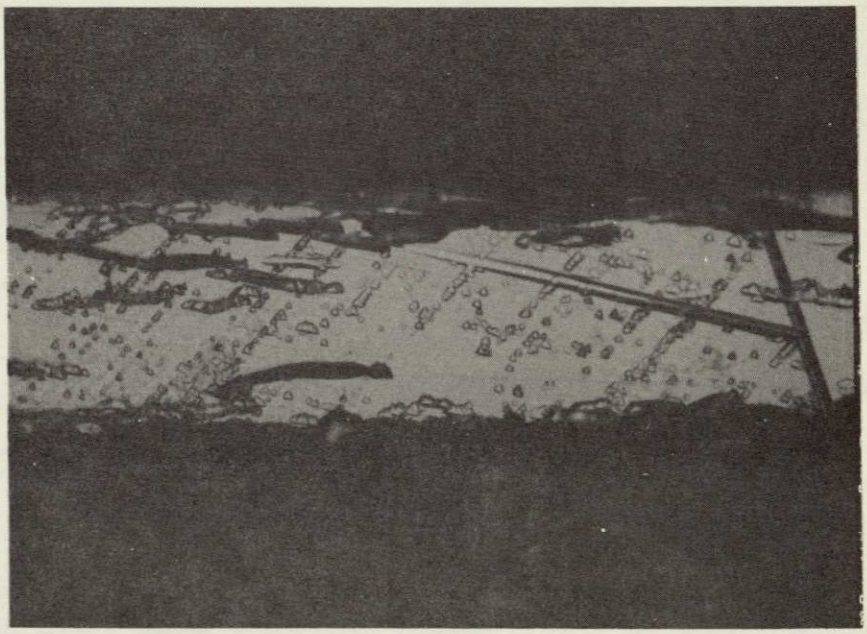


Figure 11. Optical Micrograph (500x) of Polished and Etched Cross Section of Silicon Coating, Sample MR114, Taken Parallel to Perpendicular Direction; Etch: Sirtyl; Time: 15 Sec. ; Dislocation Count ~6 x $10^6 cm^{-2}$.

Tylan Corporation and are reported to be ~7-μm thick. The primary purpose for dip-coating these substrates was to evaluate the passivation capability of these particular graphite coatings in preventing dissolution of the mullite in the silicon melt. Since the resistivity of the silicon layer is a convenient method for obtaining the amount of mullite dissolved, thick (150-400 μm) silicon coatings were grown on the substrates to improve the accuracy of the resistivity measurements.

The Vitre-Graf coatings are comparable in wettability to the rubbed-on graphite coatings typically used, but their rate of dissolution in molten silicon is considerably less. Part of the passivation study included soaking a Vitre-Graph coated mullite substrate in molten silicon for a period of one hour. Upon withdrawal of the substrate from the melt after this prolonged soaking, the substrate possessed a smooth, uniform silicon coating, thereby demonstrating the durability of these particular graphite coatings in molten silicon. By comparison, the rubbed-on graphite coatings completely dissolved in molten silicon in less than an hour.

Due to the length of time the substrate was immersed in the molten silicon and the amount of carbon present a silicon carbide layer was formed and is shown in the photomicrograph of Figure 12. Although occasional carbide particles are seen in the silicon layers on hand-rubbed graphite, usually neither the time in the melt nor the amount of carbon present are sufficient to generate an observable layer.

Figure 12. Optical Micrograph (500X) of Silicon Carbide Layer on Vitre-Graf Coated Substrate MR78 that had been Soaked in Melt for 1 Hour.

Five different liquid carbon coating compounds were purchased from Dylon Industries. These coatings had the viscosity of latex paint and were water soluble. A total of 22 substrates were dipped that had been coated with the various Dylon compounds. It was found necessary to oven dry these coatings, as residual moisture caused them to blister or "boil" off when dipped in the molten silicon, as shown in Figure 13. It was also noted that the granular nature of most of these coatings promoted nucleation which decreased the grain size, and that carbides formed throughout the Si layer. However, in cases where the granular surface was smoothed by wiping off the excess graphite and the coating was oven dried, the Dylon coatings gave large grain size similar to the hand-rubbed graphite coatings. Unfortunately our chemical analysis of these coatings has revealed that they contain from 1 to 2 percent impurities--a fact the vendor would not reveal--and are probably unsuited for our application.

Another somewhat novel method of carbon coating was also investigated - plasma decomposition of propane gas in an RF sputtering apparatus. The carbon is deposited uniformly and its purity reflects that of the gas. The morphology and grain size of the silicon film formed on such substrates is comparable to those on hand-rubbed graphite coatings.

Several methods of incorporating the carbonization with the ceramic processing were also examined. These were rolling graphite or silicon carbide particles into one surface of the substrate and then firing in an inert atmosphere or just firing the ceramic in an inert atmosphere so that the residue from the organic bonders would form a carbon film. Unfortunately none of these approaches worked with the dipped samples. The plain ceramic fired in an inert atmosphere shattered in the temperature gradient above the melt before it could be dipped. The substrate with silicon carbide developed large blisters and it appeared that the silicon did not wet the surface. The substrate with the graphite particles appeared to have been wet by the silicon, but either there wasn't sufficient carbon or the particles didn't stay embedded to permit the growth of a silicon layer.

Some very promising looking experiments have been conducted using colloidal carbon suspensions obtained from Acheson Colloids Co., Port Huron, Michigan. Four different mixtures are being tested; Dag 154, Electrodag 154, Electrodag 155, and Electrodag 502. The 154 mixtures are graphite in isopropyl alcohol with a dellulosic binder. Electrodag 155 is a mixture of graphite in trichlorethylene with a cellulosic binder. Electrodag 502 is a graphite and carbon black mixture in methyl ethyl ketone (2-butanone) with a fluro elastomer binder. Drying poses no problems and coating thickness is relatively easy to control.

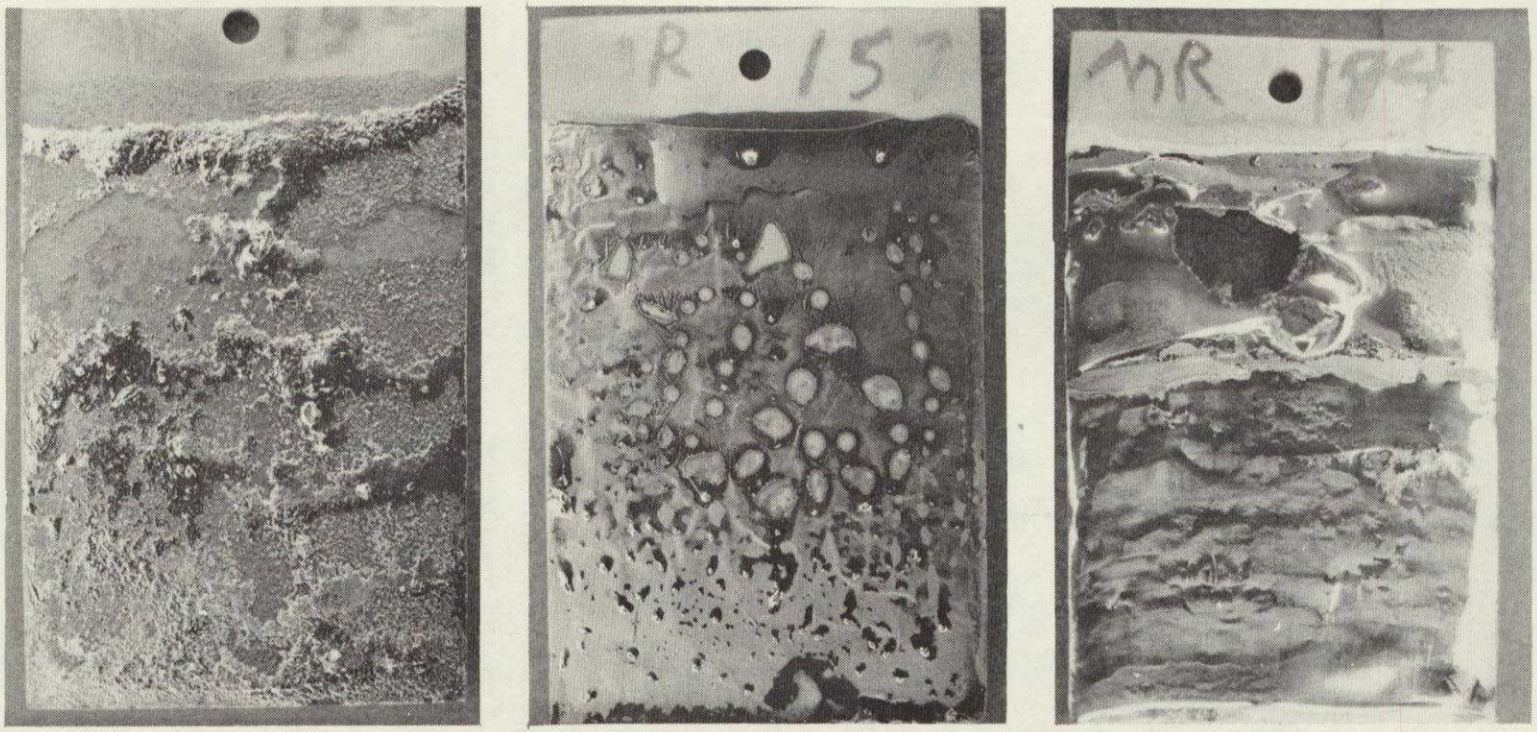


Figure 13. Blistered and Spotty Si Film Formation as the Result of Incomplete Drying of Dylon Carbon Coatings (1.7x)

Spectrographic analysis shows that the dags should be suitable for solar cell application. The results of the analysis are shown in Table 3.

Table 3. Spectrographic Analysis Results of Colloidal Carbon Suspensions from Acheson Colloid Co., Values in ppm.

Element	Dag 154*	Dag 154	E'dag 502	E'dag 154	E'dag 155
AR	88	ND < 10	110	20	33
Mo	100	ND < 33	34	ND < 33	ND < 33
Sn	52	ND < 10	ND < 10	ND < 10	ND < 10
Ca	180	43	68	39	56
V	33	ND < 33	ND < 33	ND < 33	ND < 33
Ti	24	8	53	7	8
Ni	15	2	2	2	2
Si	220	35	72	73	51
Pb	35	ND < 33	ND < 33	ND < 33	ND < 33
Mg	4	2	14	2	3
B	3	ND < 1	37	ND < 1	3
Mn	4	2	3	2	3
Na	200	ND < 100	270	ND < 100	ND < 100
Fe	1500	260	370	285	290

*Older stock.

The growth morphology of the silicon is not adversely affected by the dags. Metallographic examination of cross sections of silicon-on-ceramic which were carbonized with Dag 154 showed excellent wetting of and bonding to the ceramic surface by the silicon as shown in Figure 14.

Because of the ease of application of the dag mixtures they are now used instead of hand-rubbed graphite to carbonize the ceramic. The dags also lend themselves to conducting carbon doping experiments with the intention being to use the doped carbon layer as a back contact. For this purpose, boron silicate - Dag 154 mixtures were applied to several substrates and dipped. The silicon coatings appeared no different from those on undoped dag and will be fabricated into diodes and cells for further evaluation.

Figure 14. Silicon-Ceramic Interface Carbonized with Dag 154 (500x)

In general, from our experiments, it appears that any means of applying a smooth, uniform, dense coating of carbon of suitable thickness and purity will promote the coating of ceramic with silicon.

CONTINUOUS-COATING FACILITY (J. D. Heaps, C. D. Butter, L. D. Nelson and H. A. Wolner)

Introduction

During this reporting period a continuous-coating facility was designed and at this reporting date its construction is 95 percent completed. It was scheduled to be in operation on 27 September, but due to a scheduling error on the part of the power supply vendor, its operational date has been delayed for two weeks.

This newly constructed facility described below is expected to overcome some of the inherent problems of the dip-coating technique. Its principal advantages are as follows:

1.) Its coating principle vastly reduces the area of, and the time that the substrate is in contact with the silicon melt. This feature lessens the possibility of the melt being progressively contaminated by the substrate.

2.) The new facility permits the use of much larger substrates which should allow the individual crystalline grains to develop larger in size.

3.) The scale-up coating through-put of this new technique is potentially superior because it eliminates the dipping and soaking time required with the dip-coating technique.

4.) The thermal stability of the solidification zone of the continuous coater should also be superior to the dip-coater since its melt temperature will not be constantly upset by the immersion of unheated substrates.

The principle of the continuous coating concept is shown in Figure 15. Graphite-coated ceramic substrates are passed over a silicon-filled side arm of a crucible containing molten silicon. The level of the molten silicon is adjusted so that the surface of the liquid silicon bulges up above the walls of the side arm. The path that the substrate takes over the side arm is such that it comes in contact with the molten silicon but does not touch the walls of the side arm. It is expected that with an appropriate temperature gradient in the solidification zone that the resulting liquid solid interface will be similar to that of the dip coating method and that silicon will continue to nucleate from previously grown silicon.

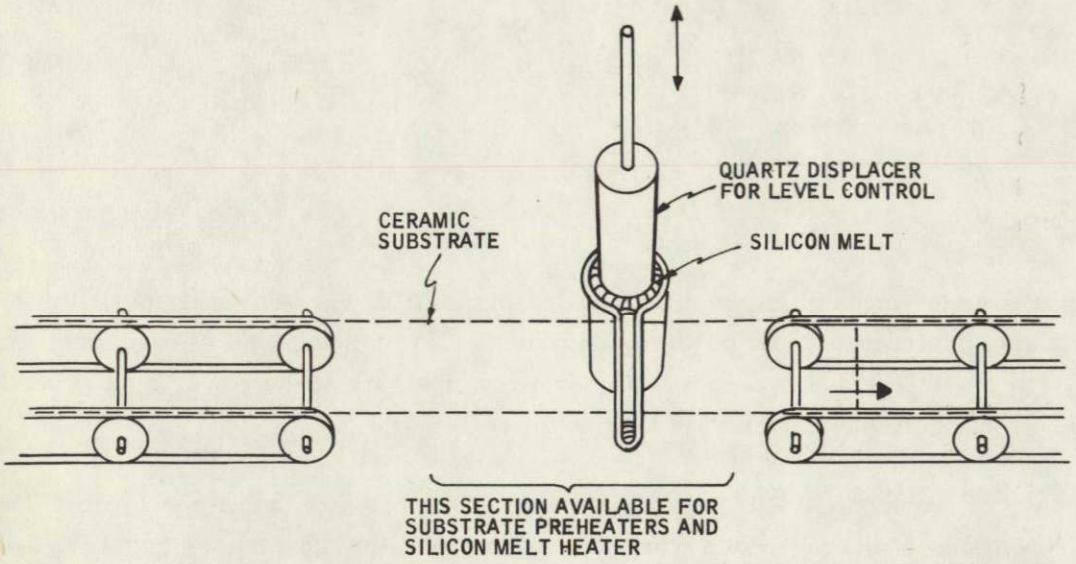


Figure 15. Silicon Coating by Inverse Meniscus (SCIM)

Description of Continuous-Coating Facility

Figure 16 is a photograph* of the coater component of the continuous-coating facility. As shown in Figure 17 the coater is divided into three sections: (1) a fore compartment (for substrate loading), (2) a growth chamber (for silicon coating) and (3) an after compartment (for substrate removal). The coater permits 10 cm x 100 cm graphite - coated ceramic substrates to pass (coated face down) over a silicon-filled trough-like quartz side arm which is attached to a crucible containing molten silicon (Figure 17). The level of the molten silicon is adjusted so that the surface of the liquid forms a meniscus above the walls of this quartz side arm. As molten silicon in this side arm is used up, it will be automatically replenished by a quartz plunger which displaces the silicon in the main crucible (see Figures 18 and 19). The position of this plunger will be controlled by the use of a laser beam whose path to a light sensor will be interrupted by the silicon meniscus in the side arm when the desired silicon level is achieved.

The growth chamber of the facility is surrounded by a water-cooled copper box (see Figure 17). Three separately controlled graphite furnaces provide temperature zones to perform the following functions:

*Note: This photograph was taken prior to the coater's present state of completion. Reporting time did not permit a current photograph.

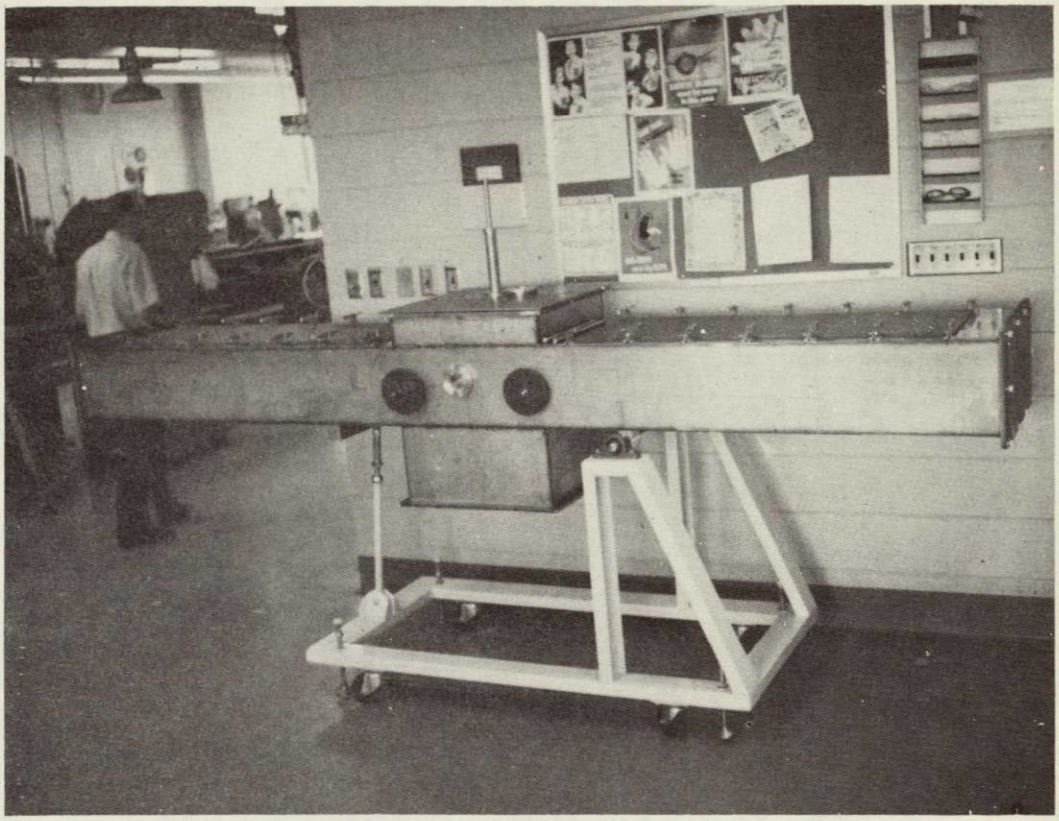


Figure 16. Photograph Showing Early Construction Status of Continuous Coater

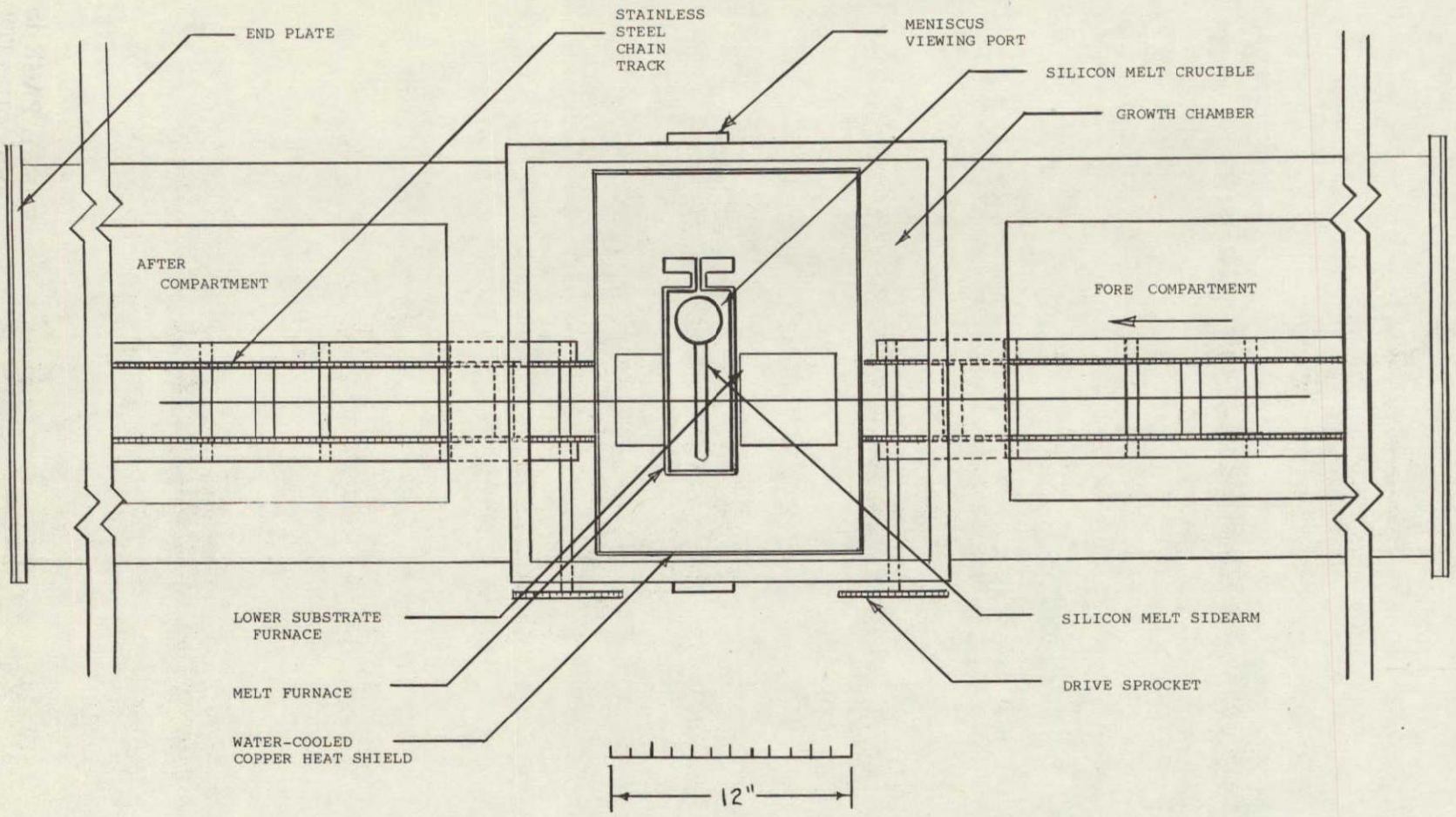


Figure 17. Exposed top view of continuous coating facility (Top covers are removed and upper substrate furnace and carbon felt insulation are not shown).

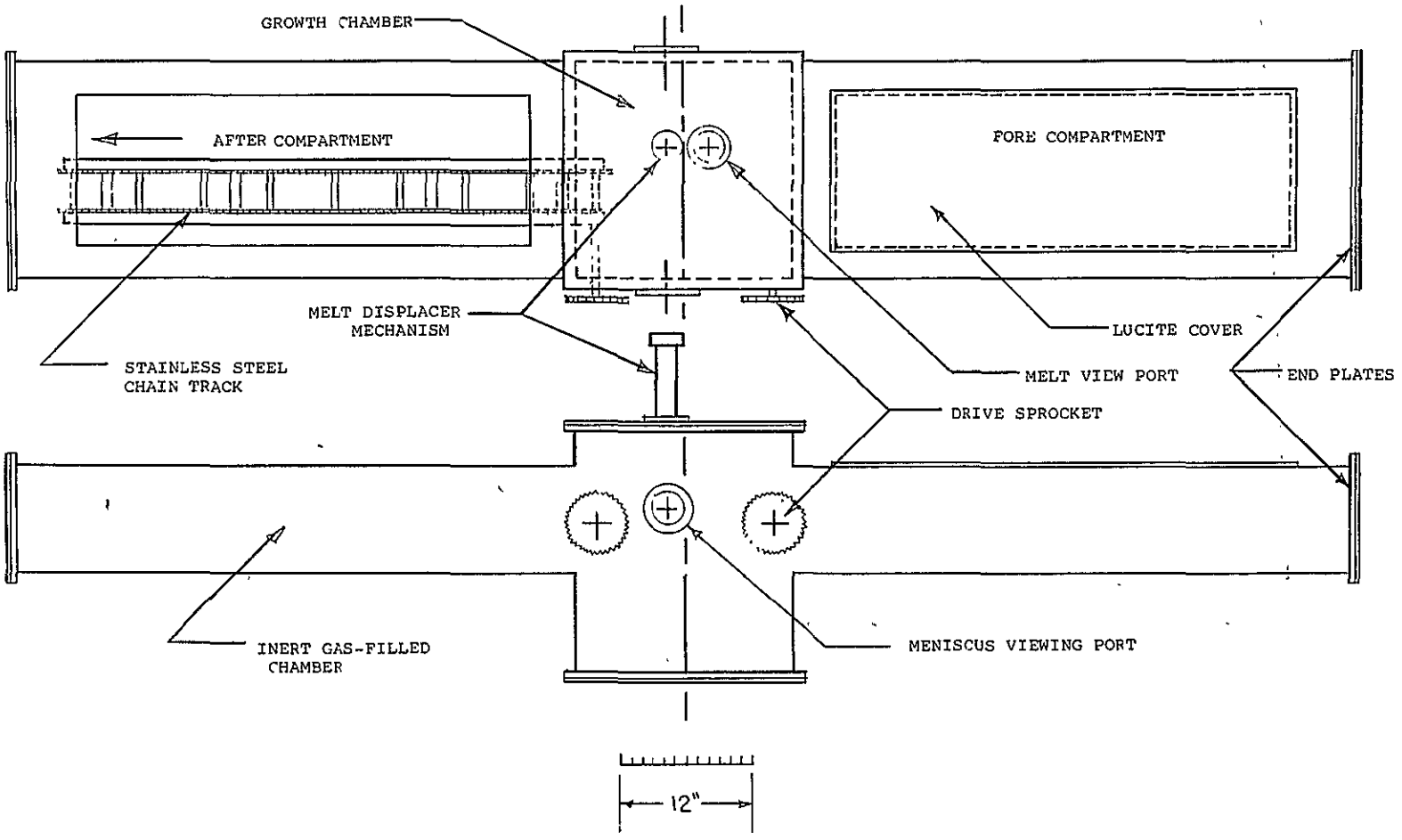


Figure 19. Top and side view of continuous coating facility.

1. Gradually heat the substrate to the coating temperature.
2. Control the temperature of the molten silicon in the main crucible and side arm.
3. Provide, as needed, the temperature profile required for desirable crystalline solidification and minimum thermal stress.

The first and second zones are individually powered by SCR-regulated 0-30 Volt, 0-1500 amp, d-c power supplies. Their temperatures are also individually controlled by Honeywell three-mode controllers. The third zone is powered and temperature controlled by a Honeywell Electrodyne-controlled power supply. Each of these furnaces is surrounded by insulating blocks of graphite and carbon felt. Viewing ports are provided for observation of the main crucible during melt-down and for viewing the silicon meniscus in contact with the substrate (see Figure 19).

The inert gas-filled enclosure which houses the growth chamber also includes fore and after compartments for handling uncoated and coated substrates. These compartments contain stainless-steel chain conveyors which carry the substrates to, through, and from the growth chamber. The chain conveyors are driven by a "Digilok" controlled variable-speed drive system which is adjustable for growth velocities of tenths of mm/sec to many cm/sec. Given an ideally flat substrate, the fore and after chain conveyors are spaced to allow the substrate's center of gravity to carry it from one conveyor to the other. For substrates that are less than flat, rollers assist in positioning the substrate. Until the growth parameters are established for producing acceptable crystalline silicon coatings, several substrates to be silicon coated will be loaded into the facility's fore compartment (see Figures 17 and 19) via the top opening. They will subsequently be placed on and removed from the chain conveyors using "dry box"-type rubber gloves which are installed in the coater's end plates. Once proper growth parameters have been established, the end plates on the fore and after compartments will be replaced with plates that permit substrates to pass through with a minimum of inert gas leakage.

While the facility was primarily designed to horizontally coat substrates, provision has been made for tilting the entire facility through about ± 30 degrees. With minor modifications the facility can be adapted to vertically coat substrates. Vertical coating does, however, place a more severe requirement on substrate flatness.

MATERIAL EVALUATION AND SOLAR CELL FABRICATION
(J. D. Zook, T. Schuller, R. Hegel, C. Knudson, and A. Peterson)

Chemical Characterization of SOC

During the first year of the contract it was established by IR spectroscopy at low temperatures that the mullite does contribute aluminum to the melt. Although other techniques for identifying trace impurities have been investigated during the past year, none of these has been very satisfactory. The studies performed are summarized below.

Neutron activation analysis--Neutron activation analysis was performed by General Activation Analysis, Inc., of San Diego. Samples were prepared from the top edge of the melt (first to solidify) for melts 16, 27 and 28, and a multi-element survey was performed. The result was that no impurities were detected in melts 16 and 28, whereas, in sample 27 Mn, Sm, Na, La, Eu and Br were detected at the ppma level, as shown in Figure 20. This finding makes sense since melt 27 was one in which MV20 mullite had been dipped for over an hour. Melt 16 was boron-doped with no dipping, and melt 28 was a contamination check with no boron doping or dipping. The disappointing aspect of this is that the elements of interest, namely Al, B, P, Fe, Ti and V, cannot be detected in Si at the ppma level by this technique.

Ion Beam Microprobe--Analyses were performed by McCrone Associates of Chicago, Ill. and Applied Research Laboratores (ARL) in Sunland, Ca. The analyses were found to be very sensitive, but were very sensitive to contamination. The impurites B, C, Na, Mg, Al, P, K, Ca, Ti, V, Cr, Fe, Ta, and Pb were found. The quantities of Na, K, and Ta were significantly greater than upper limits found by neutron activation analysis. On the other hand, Fe, Mu, Mg, Ca, Na, Ti and V are known to be present in the ceramic from emission spectrographic analysis.

Several diode areas were examined in the imaging mode using the IMMA machine at ARL. One region was selected as having a fairly large-angle grain boundary and a region of irregular surface texture, indicating small crystal size. This area was sputtered to a depth such that most of the n^+ phosphorus-diffused layer had been removed. After profiling, the area still showed some mass 27 (Al), 31 (P), 48 (Ti), and 54 (Fe). Images taken with a 10 μm ion beam showed no preferential distribution of any of these impurities.

In general, all of the search for segregation at grain boundaries by this technique gave negative results. The only images which showed nonuniform distribution of impurities were on surfaces that had not been sputtered. Sample MR105 showed clustering of masses 23 (Na), 27 (Al), 48 (Ti), and 54 (Fe?). These did not appear to correlate with structural features.

SILICON SAMPLE 27 FOR J DAVID ZOOK HONEYWELL DEC 1976

ELEMENT	CONCENTRATION (PARTS PER MILLION)	PRECISION (+ OR -)
MN	.092600	.019000
SM	.060300	.012000
NA	.685000	.140000
LA	.051700	.012000
EU	.000912	.000340
BR	.052900	.013000

ELEMENT	UPPER LIMIT (PARTS PER MILLION)	ELEMENT			ELEMENT			ELEMENT		
AG	< 3.500000	FE	<	190.000000	NB	<	1100.000000	SI	<••••••••••••	
AL	<••••••••••••	GA	<	.100000	ND	<	.990000	SM	<••••••••••••	
AR	< .340000	GD	<	1.100000	NE	<••••••••••••		SN	<	75.000000
AS	< .039000	GE	<	12.000000	NI	<	21.000000	SR	<	3.400000
AU	< .001100	HF	<	.140000	O	<••••••••••••		TA	<	.047000
BA	< 7.200000	HG	<	.075000	OS	<	.170000	TB	<	.030000
BR	<••••••••••••	HO	<	.014000	P	<••••••••••••		TE	<	3.400000
CA	< 5500.000000	I	<	1.400000	PB	<	5900.000000	TH	<	.180000
CD	< .670000	IN	<	.004100	PD	<	.120000	TI	<••••••••••••	
CE	< .720000	IR	<	.001500	PR	<	.720000	TL	<	2700.000000
CL	< 2.300000	K	<	5.000000	PT	<	.330000	TM	<	.100000
CO	< .290000	KR	<	13.000000	RB	<	6.900000	U	<	.057000
CR	< 1.700000	LA	<••••••••••••		RE	<	.009100	V	<	4700.000000
CS	< .350000	LU	<	.012000	RH	<••••••••••••		W	<	.028000
CU	< .120000	MG	<	71000.000000	RU	<	1.600000	XE	<	2.800000
DY	< .250000	MN	<••••••••••••		S	<••••••••••••		Y	<	480.000000
ER	< .380000	MO	<	.530000	SB	<	.023000	YB	<	.058000
EU	<••••••••••••	N	<••••••••••••		SC	<	.018000	ZN	<	5.100000
F	< 45000.000000	NA	<••••••••••••		SE	<	.510000	ZR	<	37.000000

•••••••••••• INDICATES THE UPPER LIMIT COULD NOT BE COMPUTED

GENERAL ACTIVATION ANALYSIS, INC
11575 SORRENTO VALLEY ROAD * 214
SAN DIEGO, CALIFORNIA 92121
PHONE 714/755-5121

Figure 20. Multi-Element Survey of Melt 27 by Neutron Activation Analysis

The QMAS machine was used to look for impurities in the SOC samples. Comparison with a silicon standard from JPL containing 2 ppma aluminum gave 26 ppma using the standard calibration program. The numbers depend on the presputtering (preburn) time with lower concentrations after longer times. Thus surface cleanliness is clearly important for good results. All the samples were grown from melts which had been exposed to mullite for long times. The only independent check is the Al content, which should correlate with resistivity measurements. This correlation was quite poor. Sample MR78TC should have had considerably less Al than MR47, whereas they both showed the same amount, both higher than the values indicated from resistivity. The Al content indicated for sample MR105 was beyond the solubility limit. The discrepancy could well be due to residual Al from the surface.

We basically believe in the capability of the IMMA and QMAS systems, but need a consistent procedure for cleaning samples to avoid "driving in" of impurities.

Other Techniques--In addition, SIMS and Auger analyses were performed at Physical Electronics Industries, but no impurities were detected, showing that these systems are not sufficiently sensitive for our problem.

Electrical Characterization of SOC

Earlier in the program, low-temperature infrared spectroscopy was used to determine that some dissolution of the mullite occurs in molten silicon. Part of the aluminum atoms from the $3Al_2O_3 \cdot 2\ SiO_2$ enter the silicon lattice to become electrically active acceptors. The extent and rate of dissolution were examined in a series of experiments using resistivity measurements to determine the aluminum concentration. The extent to which the mullite dissolution can be inhibited by a vitreous carbon coating, prepared by Tylan Corporation, was also investigated.

A summary of investigative experiments is shown in Figure 21 which gives resistivity as a function of time in the melt. Samples were prepared from the tops of solidified melts and resistivity measurements were made, where possible, within single grains of silicon. The top of the solidified melt was chosen to be representative of the solidification rates involved in actual dip-coated layers of silicon and thus should more accurately simulate the effects of impurity segregation.

An undoped silicon charge was melted and a 125-μm-thick silicon layer was dip-coated on a MV-20 mullite substrate (MR45). Following this, an uncarbonized substrate (MR46)

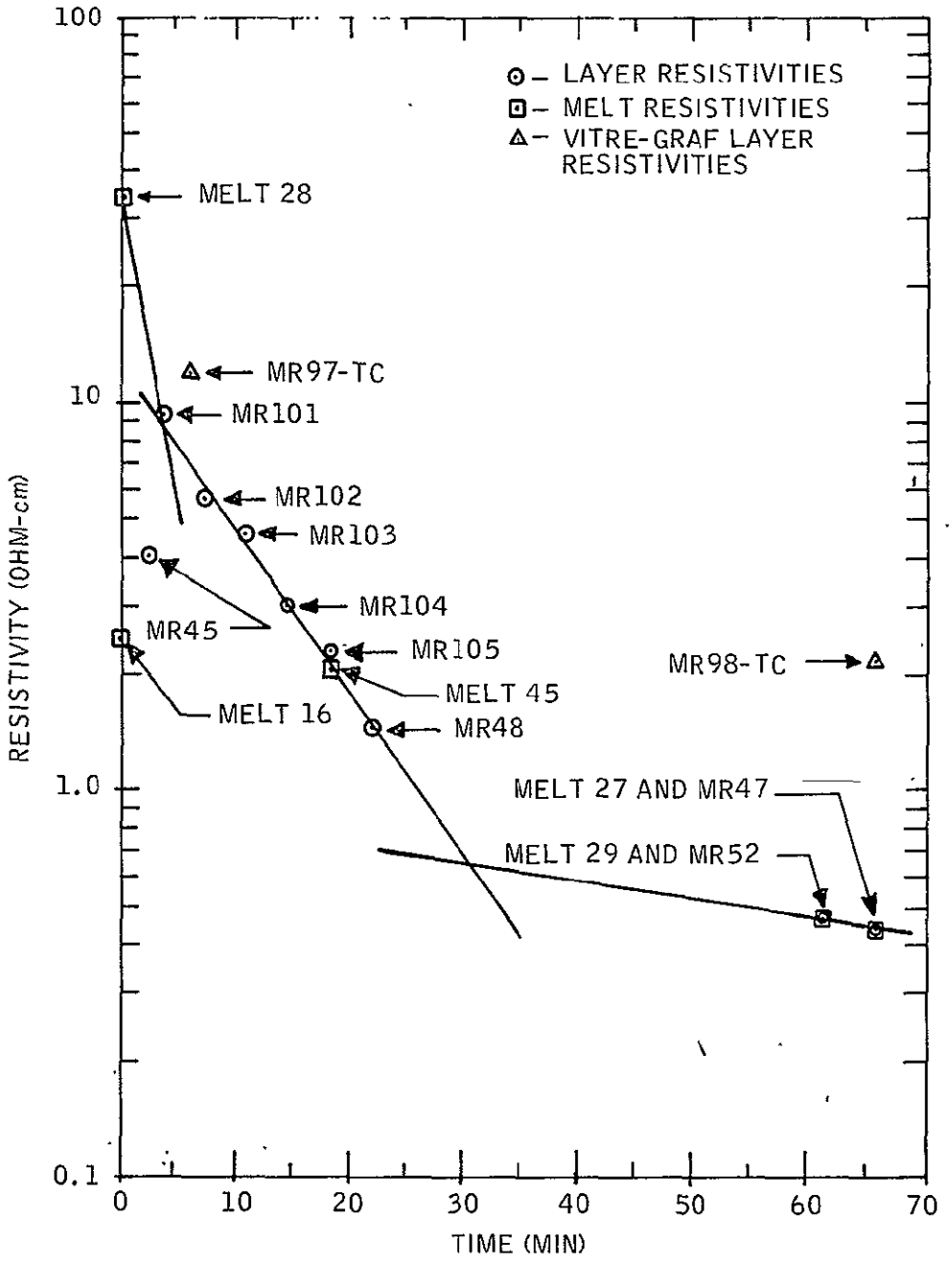


Figure 21. Layer and Melt Resistivities Versus Accumulated Time that the Undoped Melts were Exposed to Mullite.

was dipped and soaked in the melt for a period of ~63 minutes. A third substrate (MR47) was also dip-coated with a 125-μm thick layer of silicon, and resistivity measurements of the above layers, as well as of the respective melt, were made. The results are shown in Figure 21.

The above experiment with a new silicon charge was repeated with substrates which were fully coated with graphite on all sides and edges. The first dipped substrate (MR48) was in the melt for 22 minutes. As shown in Figure 21, the rubbed-on graphite coating neither helps nor hinders the final impurity level of the melt.

Using another undoped silicon charge, five MV-20 mullite substrates (MR101 through MR105) were progressively dip-coated with silicon layers using identical growth conditions. Their respective resistivities, as the melt became progressively contaminated, are also shown in Figure 21.

Figure 21 shows that the aluminum impurity level of the melt increases rapidly during the first two or three minutes of contact time with the substrate, and then increases exponentially at a lesser rate, becoming very nearly saturated after an hour of contact time.

The initial rate of dissolution would be proportioned to the amount of exposed surface area with the rate decreasing as the solution approached saturation. The effective surface area of the mullite depends on the surface roughness and on the degree of wetting of the substrate. The saturation solubility of the aluminum is determined by the amount of oxygen in the melt. Because of the quartz crucible, the silicon is saturated with oxygen, limiting the amount of dissolved aluminum to a concentration well below the solubility limit of aluminum by itself. Since several chemical reactions are involved, the detailed kinetics are undoubtedly not simple, as indicated by the several slopes in different regions of Figure 21.

Figure 21 also shows the effect of the vitreous carbon coating in inhibiting the mullite dissolution rate in molten silicon. Vitreous carbon-coated substrates MR97-TC and MR98-TC were successively dip-coated in an undoped silicon melt. Substrate MR98-TC was allowed to soak in the melt for one hour before it was removed with a smooth, uniform silicon layer. MR97-TC and MR98-TC layer resistivities are also plotted in Figure 21 for the purpose of comparing them with the more generally used rubbed-on graphite coated substrate silicon layers.

It is interesting to note that for reasons not yet understood and contrary to what is generally expected, resistivities measured on the SOC layers where the current ran across

grain boundaries are frequently substantially lower than those where the current ran along the single grains. This anomaly occurred in the vitreous carbon-grown silicon layers, regardless of their impurity levels. The data points shown in Figure 21 are an average for both current orientations.

As reported in an earlier section of this report, sectioning MR78-TC caused portions of the vitreous carbon silicon layer to separate from the substrate. This made it possible to measure the sheet resistance of the silicon layer as well as that of the attached vitreous carbon coating. Since the sheet resistance of the silicon layer was ~20 times that of the vitreous carbon, it is evident that some type of conductivity barrier exists between the two. The sheet resistance of vitreous carbon on the uncoated portion of the dip-coated layer was very similar to that attached to the silicon layer, giving further evidence that little, if any, of the vitreous carbon coating was dissolved by the molten silicon after soaking in it for a period of one hour.

In recent months a number of dag (alcohol colloidal suspension) carbon coatings have been used. A run is planned to determine the extent to which these coatings inhibit dissolving of the melt.

During the course of the year the system became inadvertently contaminated. It was then thoroughly cleaned and a contamination check was run. The results showed that an undoped melt never exposed to mullite should have a resistivity in the 10^3 ohm-cm range.

Electrical Characterization of Carbon Layers

There are several important aspects of the electrical resistivity of carbon layers. First, the electrical resistance can be used to evaluate the uniformity and reproducibility of the carbon-coating process. Secondly the sheet resistance of the carbon may affect the resistivity measurement of the silicon. Thirdly, it would be desirable to use the carbon as a back contact to the silicon to decrease parasitic series resistance of solar cells. Table 4 summarizes our measurements on sheet resistance of carbon layers.

It is clear from Table 4 that the rubbed and the dag-borosilicate coatings graphite are almost entirely removed by the melt. The dag layer is partially removed, but has the appearance of being continuous and intact after removal of the SOC by etching or spalling.

The vitreous carbon layers, on the other hand, are almost wholly intact after contact with the melt, even after one hour of contact with the melt (sample MR78TC). Since the sheet

resistivity of the vitreous carbon is only 2 to 5 ohms/□, it is much lower than the sheet resistivity of the p-type silicon layer (50-500 ohms/□) and could seriously affect the sheet resistivity measurement if there is low resistance contact between p-silicon and vitreous graphite. The nature of this contact was therefore investigated and the results are reported in the next subsection.

Table 4. Typical Carbon Sheet Resistivities

Carbon Type	As Deposited (ohms/□)	After CP4 Etching To Remove SOC Layer (ohms/□)
Graphite Rubbed On Rolled Mullite (MV20)[a]	10-25	250-600
Graphite Rubbed On Pressed Mullite (Amer. Lava)	100-150	1K-60K
Vitreous Carbon (Vitregraf) On MV20	2.5-5	2.5-5
Dag (colloidal carbon in alcohol) On MV20	20k-40k (unfired) 20-40 (fired)	120-600 70-450 (where SOC Spalled off)
Dag and Borosilicate glass (1:1)		5K-1M

[a]The thickness of the layer based on weight gain is 7μm which would give a sheet resistivity of about 2.5 ohms/□.

Silicon - Carbon Interface

A number of interesting observations have been made regarding the silicon-carbon interface. Samples were mounted in a metallurgical mount, and cut and polished to show the cross section. The microscope showed that there was an interface layer that was harder than either the carbon or the silicon - a strong suggestion of silicon carbide formation.

These samples were then removed from the potting compound and the cross section was examined using scanning Auger microscopy (SAM) at Physical Electronics, Inc. Some

of the results are shown in Figure 22. A complete Auger spectrum of the interfacial material showed only silicon and carbon, and no impurities (at the 0.1 percent level). It is interesting, however, that the shape of the carbon peak and the silicon to carbon stoichimetry varied from that of a polycrystalline silicon carbide standard. It is not known whether these discrepancies are significant, but they suggest that the form of silicon carbide is different from the usual form.

At any rate, several comments on the silicon-carbon interface are in order. The SiC appeared thickest at the top of sample MR78 which had been in the melt for an hour. Since it was much thicker than the carbon coating, the SiC must be formed from carbon particles which float to the top of the melt. There was no detectable SiC at the top of sample MR106 which had been in the melt a minimum amount of time. Away from the surface the SiC thickness appeared about the same in the two samples, varying from 2 to 10 μm. Typically, the SiC was somewhat thinner than the vitreous carbon coating remaining.

The samples were etched in Sirtyl etch after polishing, which revealed the presence of cracks. The region shown in Figure 22 was selected because the SiC was of maximum thickness and because it showed some cracks in the silicon and at the silicon-SiC interface. These cracks may be responsible for the nonuniformity of the electrical contact, or it may be due to variations in SiC thichness.

To measure the current-voltage relationship of the contact between the p-silicon and the vitreous carbon layer, samples were prepared by selectively etching away the silicon, leaving pads of silicon on the exposed graphite. The geometry was the same as used for the contact resistance measurements discussed below. Current flowed from one pad to another, and the voltage drop between the silicon and the graphite at the edge of the silicon was measured. Typical results are shown in Figure 23.

The resulting I-V characteristics for sample MR78 were quite nonlinear, characterized by a Schottky diode-like behavior. The slope at zero voltage gave contact resistance values of averaging about 6 ohm-cm^2. This sample had been in the melt for over an hour and so a rather thick layer of SiC is presumed to have formed.

Sample MR106D had a much shorter time in the melt, about 80 seconds at the top of the SOC layer and about 3 minutes at the bottom. Three contacts were evaluated. A, B, and C had increasing times in the melts and had zero voltage contact resistivities of 0.03, 0.04 and 0.13 ohm-cm^2, respectively. The former values are quite low, and contacts A and B in particular, were quite linear in their behavior.

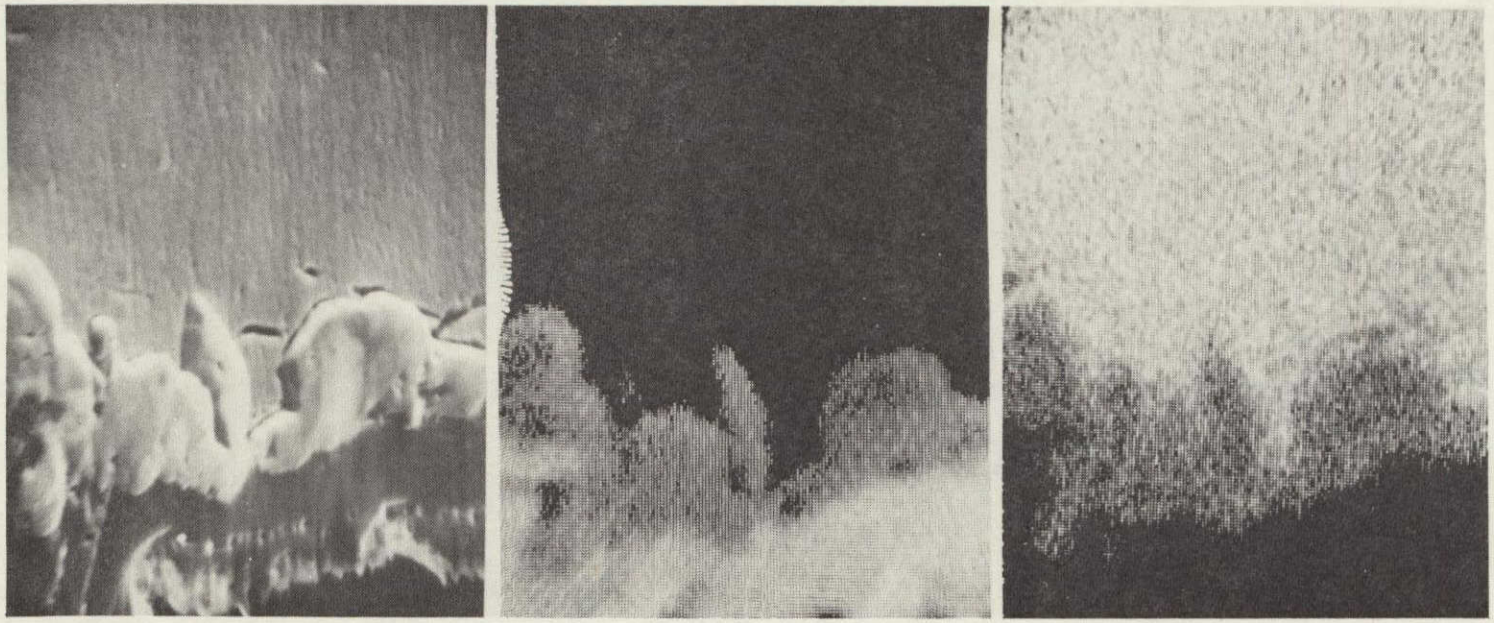
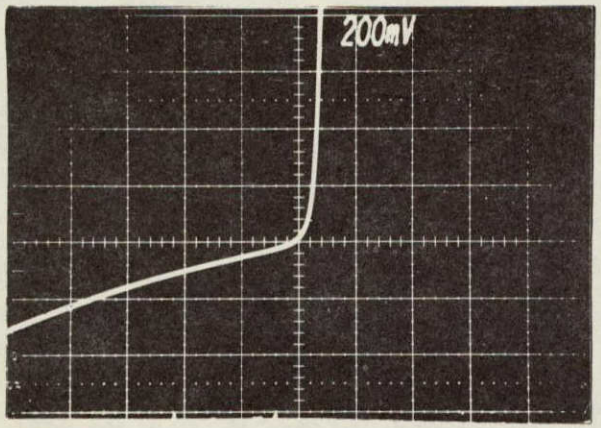
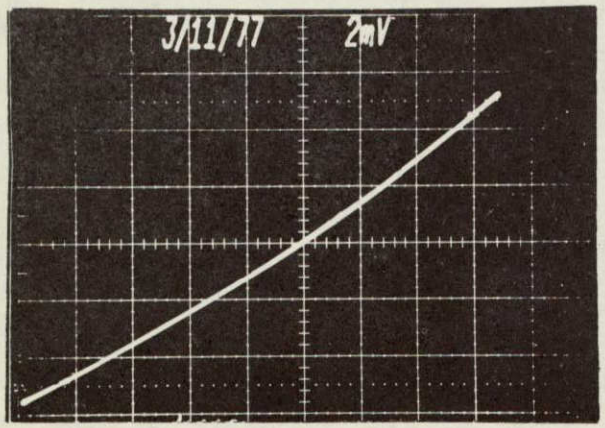


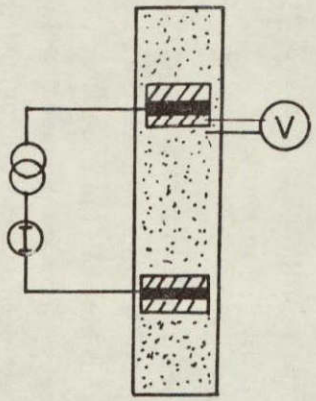
Figure 22. Scanning Auger Micrographs of the Silicon-Vitreous Graphite Interface at 2500x. Photo at left is a secondary electron image, the center photo is the carbon image, at right is the silicon image of a section of sample MR106. Silicon is at the top, carbon is at the bottom, and the silicon carbide is in between.



(a)



(b)



(c)

SILICON CERAMIC

SILICON ETCHED AWAY TO EXPOSE VITREOUS CARBON LAYER.

Figure 23. Silicon-Vitreous Carbon Electrical Contact. (a) current-voltage relationship for sample MR78TC which had been in silicon melt 1 hour; (b) sample MR106TC, 2 minutes in melt; (c) four-terminal method measurement. Both (a) and (b) had 10-mA/cm vertical current scale.

These results are particularly encouraging because they indicate that the vitreous carbon can provide an adequate base contact to the p-layer. On the other hand, it means that sheet resistance measurements on these SOC layers can be in error because of shorting by the graphite. In fact, four-point probe measurements of sheet resistivity were made on sample MR106D and were found to vary by a factor of 30 from region to region, with the low readings corresponding to the readings for the carbon. Thus the silicon-carbon electrical contact is not uniform on this sample.

The dag alcohol-colloidal graphite coatings have been shown to be quite attractive from the coating and purity viewpoint. It appears that they may also be helpful in the problem of contamination of the melt from the mullite. In several cases where the dag was not diluted the silicon layers separated from the ceramic. The surprising feature was that the carbon layer underneath remained intact, while some of the carbon remained attached to the separated silicon. This behavior contrasts with that of the rubbed-on graphite and the vitreous carbon coatings. In those cases, when silicon separation occured, the carbon layer adhered to the silicon.

The encouraging aspect of this is that no white mullite was visible, suggesting that the silicon may not be making direct contact to the mullite. Thus, dissolution of the mullite and consequent contamination of the melt may be prevented.

Sheet resistance measurements on SOC layers spalled off of dag coatings suggest the carbon on the substrate does not disappear into the melt as does the hand-rubbed graphite. The data also shows that the contact between the silicon and the carbon is nonohmic. However, in one sample the sheet resistance measurements, though erratic, suggest that there is fairly good ohmic contact between the silicon and the carbon.

Clearly this is an area that needs further investigation. Certainly we plan to do a run, using an undoped melt and dipping only substrates that are completely coated with the dag coating, to see if dissolution of aluminum from the mullite is indeed prevented by the dag. In addition, we would like to experiment with multiple coatings and with boron-doped coating.

Reflectivity Measurements

To correct for reflectivity losses in calculations of inherent efficiency of solar cells, it is necessary to know the reflectivity of silicon averaged over the solar spectrum. It is therefore of interest to measure reflectivity of our SOC material. For this purpose a

Cary 14 spectrophotometer with a reflectivity attachment was used. Three samples were measured: (1) a polished wafer with HF etch only; (2) a polished wafer that had been etched for 8 minutes in a 3:2:1; acetic:nitric :HFetch to remove any polishing damage; and (3) a SOC sample (MR107) that had an HF etch only.

The shape of the reflectivity spectrum between 300nm and 1200nm for all samples was essentially identical. The polished samples had the highest reflectivity, while the etched sample was a factor of 0.983 lower. The SOC samples had an average value that was 0.859 lower than the polished sample. There were slight deviations from proportionality, but these were in a direction to be explained by the fact that there was more scattering by the etched and SOC samples.

In fact, the variations between the samples can be almost certainly attributed to the variations in surface flatness, which causes small angle scattering. An antireflection layer on the sample would reduce the small angle scattering losses by the same extent as the specular reflection, so we feel the usual assumption of 40 percent reflectivity is applicable to our SOC cells as well as to our comparison (etched) single-crystal cells for calculating inherent efficiency calculations. However, in the calculations reported below, we have assumed a reflectivity of 35 percent as a conservative estimate.

Solar Cell and Photodiode Fabrication

Our initial technique for fabricating photodiodes was to use P_2O_5 diffusion and hand-painted black wax to define mesa diodes. Electroless nickel (e-Ni) was used as the electrical contact to the p-type base region and silver paste was used for contact to the diffused layer.

During the second and third quarters of this year we have improved our fabrication procedure significantly. We always make single-crystal control cells and photodiodes by the same techniques used for the SOC. The performance of the control cells improved considerably with the new fabrication process.

At the present we are using the following processes, some of which are illustrated in Figure 24:

1. P_2O_5 diffusion at 875°C for 20 minutes
2. Kodak 747 microresist for the photoresist
3. Fe_2O_3 patterns on glass to expose the photoresist by contact printing

4. Plasma etch for exposing the base region for base contact and then final mesa
5. Sputtered PtSi contact to base, followed by sputtered nickel
6. Sputtered nickel contact to n^+ region
7. Indium solder to the nickel film.

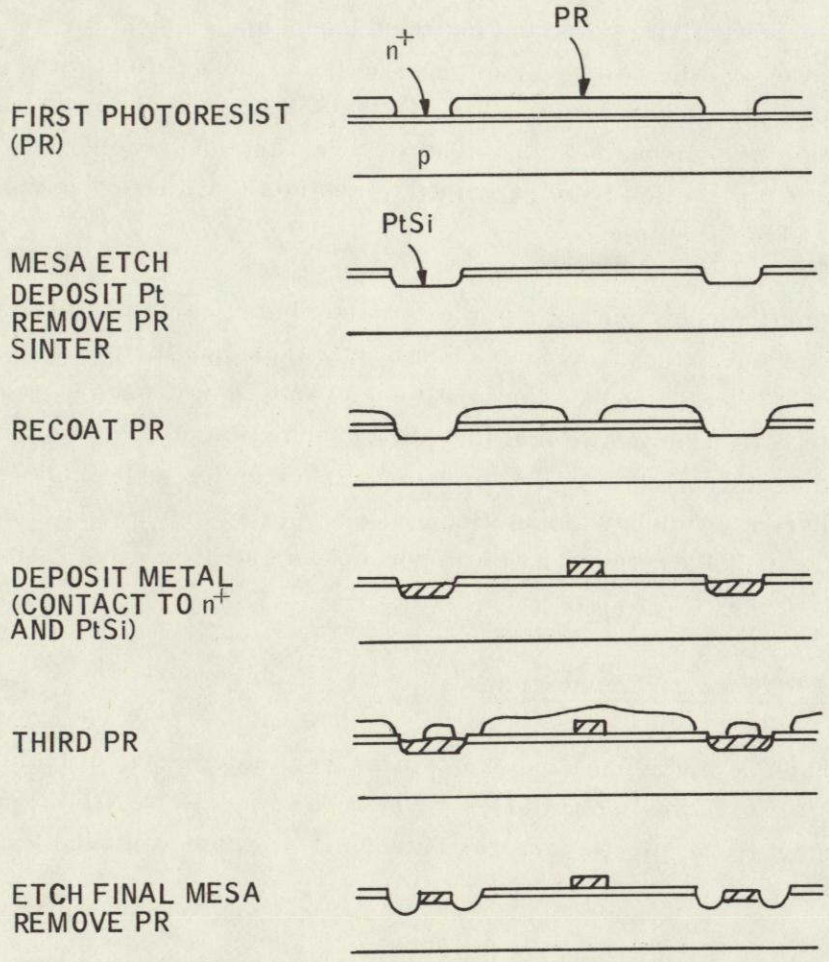
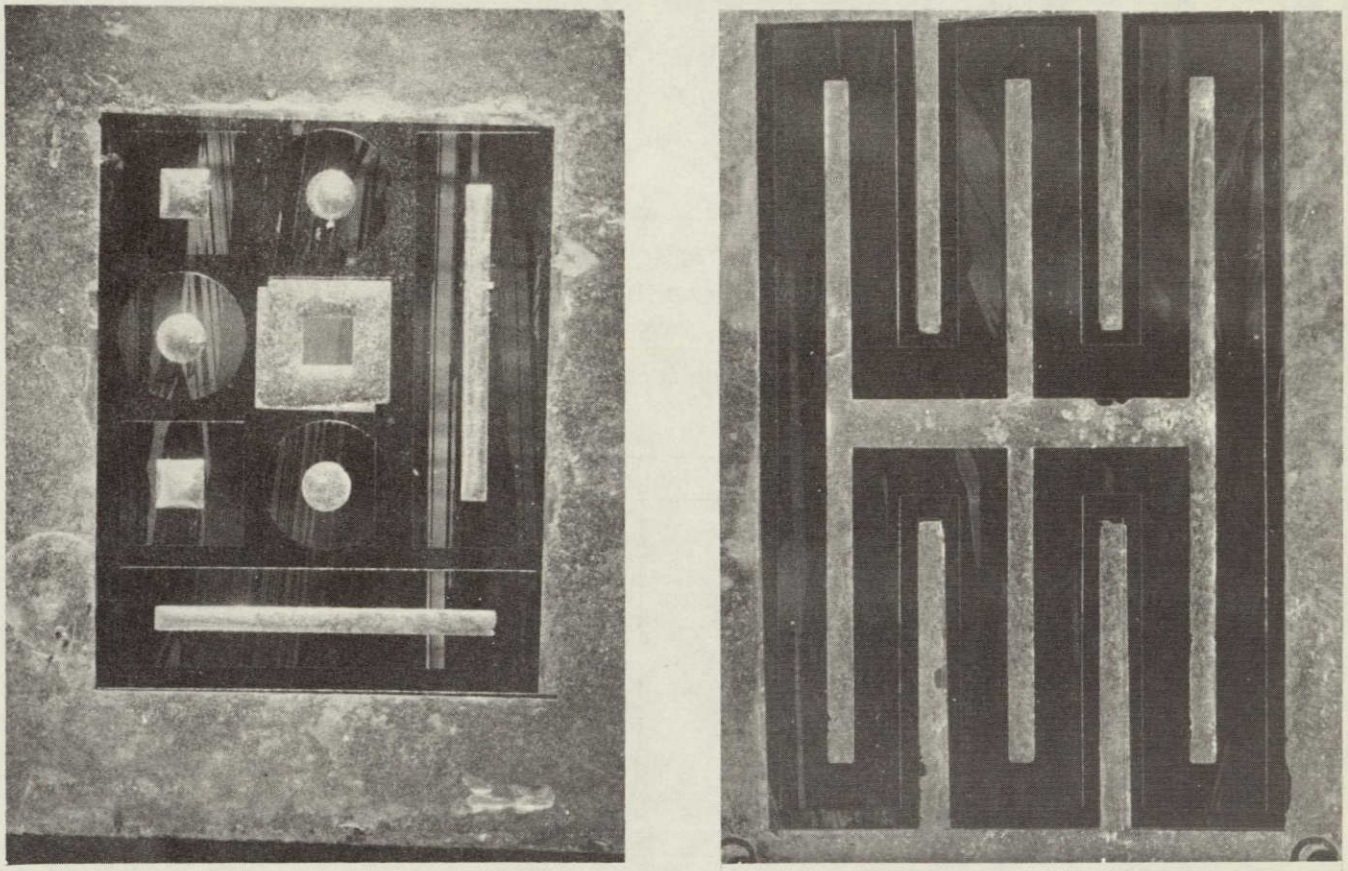


Figure 24. Present Fabrication Procedure. (The sketches show the crossection after the step described on the left.)

In this process the exposed mesa is not subjected to any high-temperature process, namely the sintering of the Pt at 600°C. The Fe_2O_3 patterns on glass facilitate mask registration and do not shrink during development so that the areas are precisely defined. Two types of patterns are presently being used, as illustrated in Figure 25. The photodiode pattern in Figure 25a is convenient for evaluating uniformity of the material and for EBIC, LBIC, and lifetime measurements. The 1 cm^2 cell pattern was designed to have wide line widths and large tolerances on mask alignment for ease of fabrication. We have also laid out a 10 cm^2 pattern as shown in Figure 26.



(a) (b)

Figure 25. SOC Solar Cells (6x). (a) An array of diodes. The central square is a base contact, as well as the outer region. (b) a solar cell with $1cm^2$ active area.

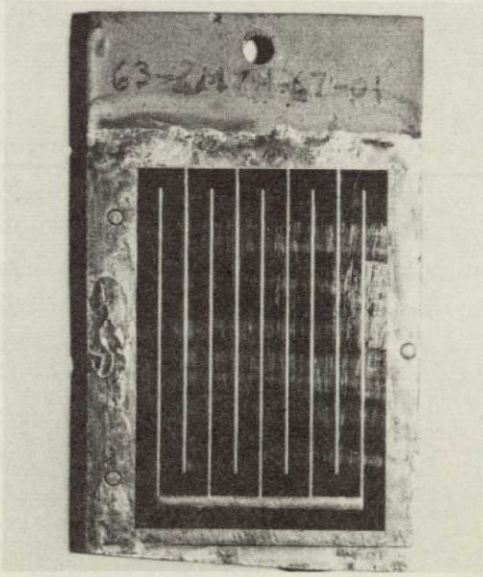


Figure 26. Solar Cell with $10cm^2$ Active Area

In laying out the pattern for the $10cm^2$ cell, we were forced to use narrower line widths and 50 percent greater width between lines, so tolerances are smaller and the effect of spreading resistance is more detrimental.

The interdigital electrode pattern is essential at present because of the spreading resistance in the base layer. We plan, of course, to use slots in the ceramic to make contact to the base on the back side of the ceramic as illustrated in Figure 27. This, in combination with conducting layers between the ceramic and the base region, will lead to a series resistance comparable to that of cells made from single crystal wafers.

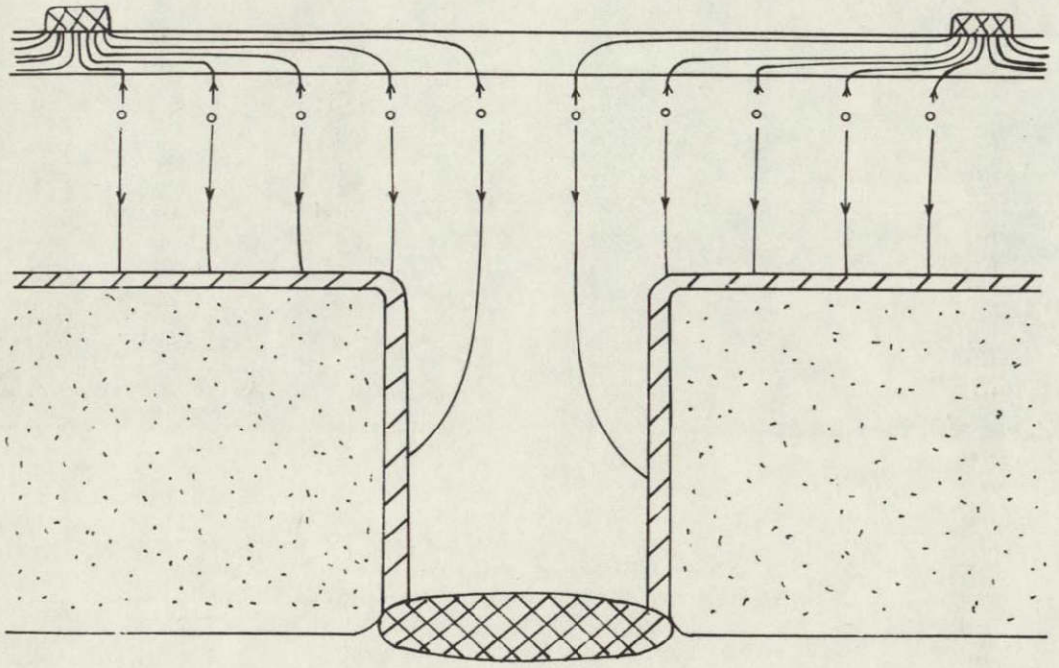


Figure 27. Cross-Section of a Portion of a Solar Cell on a Slotted Ceramic Substrate.

We also plan to modify our diffusion procedure. A new five-inch diffusion furnace has been purchased and set up for diffusions using a phosphine source. We have also evaluated several liquid spin-on diffusion sources and have ordered a spinner which will enable us to follow the procedure recommended by the manufacturer. Two other methods - spray on and dip coating - are also being investigated. The latter would be applicable if areas larger than 4 in. x 4 in. are to diffused.

Characterization of Electrical Contacts

Important progress was made during the past year in characterization and optimizing the electrical contacts to the silicon. We changed from nickel to platinum metalization for the contact to the p-type base region of photodiodes and solar cells.

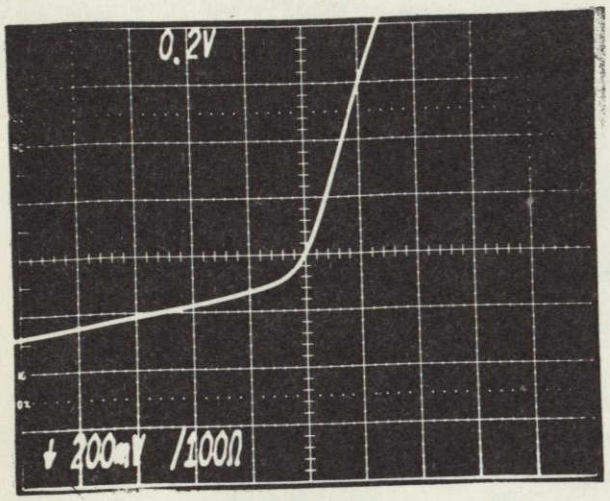
Contact resistance has been a problem for two reasons: (1) lack of low contact resistance has resulted in poor cell performance, and (2) in a cell design with top contacts to the base region the base contacts must be small in area and therefore must have low contact resistivity. The definition and measurement of contact resistivity is not always straight-forward, as pointed out by Berger.[6] It is convenient experimentally to measure contact resistance using a planar resistor, which complicates the analysis since the current density is not uniform. We have used both circular geometry and linear geometrics to measure contact resistance. Our technique illustrated in Figure 28, is somewhat different from the techniques described for planar diffused resistors[6] because our samples are much larger, and we can use tungsten probes to measure voltage at a point using a high-impedance (1000-megohm) buffer amplifier.

Measurements were first made on electroless nickel (e-Ni) contacts using various geometries. We found that, in some of the photodiodes using e-Ni, the contact's resistance to the p-type base was quite nonlinear and variable. Sputtered nickel was more reproducible if sintered at least at 450°C but gave contact resistivities of 0.3 ohm-cm^2 or greater, and were nonlinear.

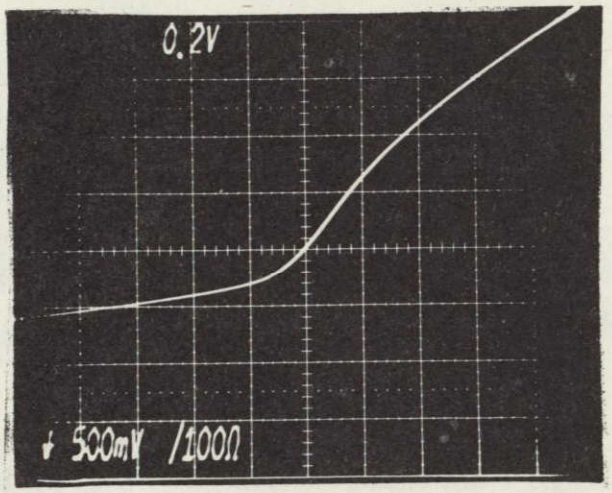
We discussed our contact problems to the p-type silicon with various people at Honeywell's Solid State Electronic Center, and they suggested the use of platinum silicide (PtSi) or palladium silicide (Pd_2Si) as a contact material. These materials are formed by sputtering the metal and sintering at temperatures in the range of 500°C.

The probe method showed that the contact resistance was much lower than in the case of e-Ni. In fact, it was difficult to measure, because with low-contact resistance the current density in a planar contact becomes quite nonuniform.

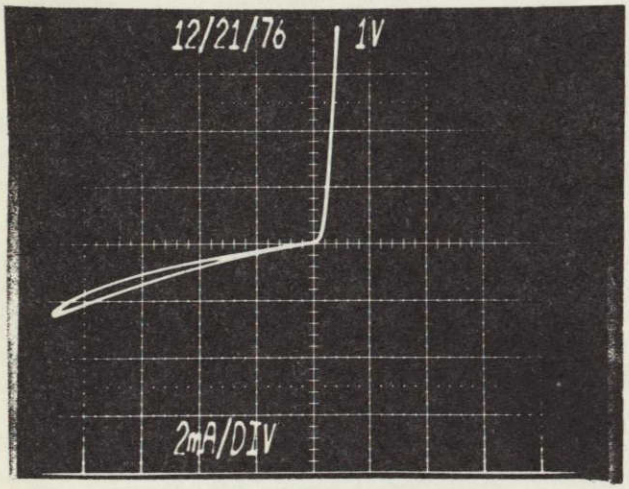
An approximate method was used to estimate the contact resistivity of PtSi to 3-ohm-cm p-type silicon to be about 0.03 ohm-cm^2. This compares to values of 0.001 to 0.003 ohm-cm^2 in the literature.



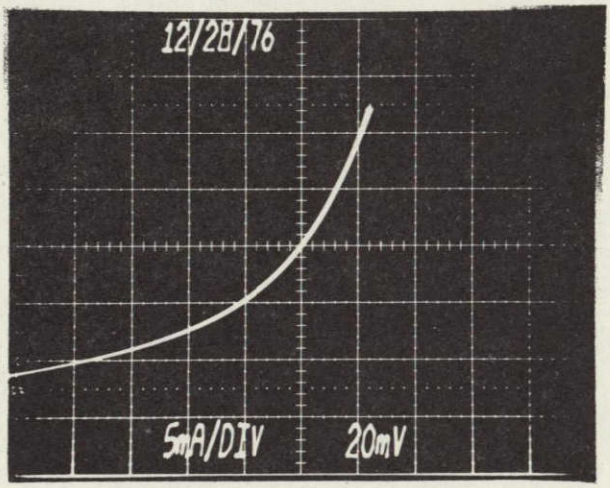
a) Unsintered sputtered nickel, .01 cm^2 2 ma/div vertical



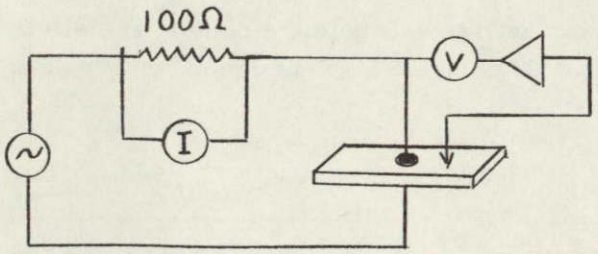
b) Sintered sputtered nickel, .01 cm^2 5 ma/div. vertical



c) Unsintered electroless nickel, .18 cm^2



d) Sintered electroless nickel, .28 cm^2



e) Three terminal measurement method

Figure 28. Contact Current-Voltage Relationship and Method of Measurement

EBIC Measurements

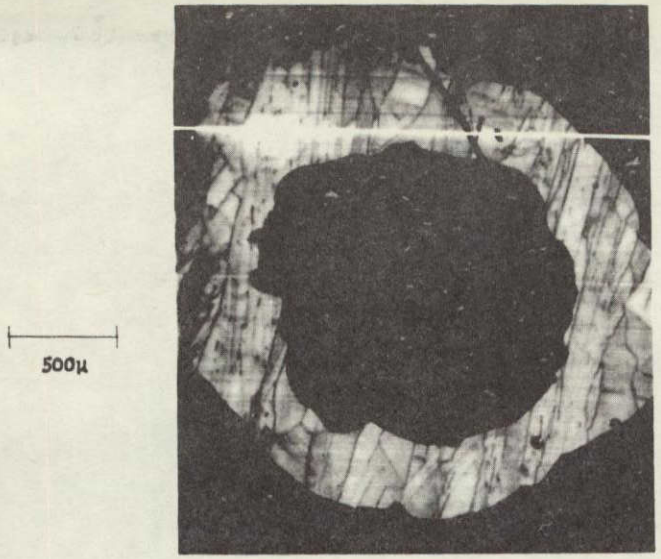
Numerous EBIC measurements of SOC diodes have been performed during the past year, and several problems with this technique have been identified. The main problem is related to the e-beam charging of an oxide at the surface of some samples which causes an inversion layer, effectively enlarging the diode. Hopefully, this is avoided in point-by-point measurements of EBIC which look at a virgin area and approaching the diode from a distance. Thus, even if inversion occurs at the point of measurement, these inversion regions are not connected to each other nor to the diode, so that no current is induced in the diode.

Such point-by-point measurements have been made using a Keithley 602 electrometer to measure the current, spending about 30 seconds at each point. Diffusion lengths varying between 6μm and 25μm have been determined in this way. The problems related to surface inversion seem to be considerably reduced with the photolithographic diode fabrication procedure described below, because the mesa is defined as the last step and there is less chance for oxide formation. Figure 29 shows some diode uniformity results obtained on diode R78D-42-6. The diodes show fairly uniform EBIC response in spite of poor structure. This diode had an actual efficiency of 6.5 percent, and a short-circuit current of $22 ma/cm^2$, so it appears that reasonably good performance can be obtained in spite of poor crystallinity.

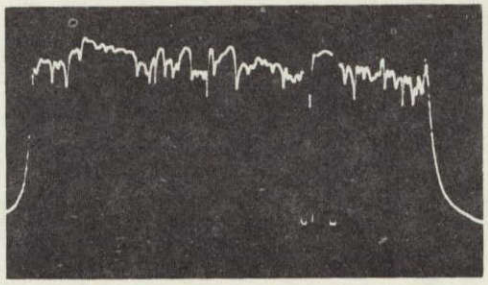
We have found that the offset current (EBIC current with the e-beam striking the base region) is significantly larger for larger diodes. This, together with amplifier problems, has prevented us from obtaining many point-by-point measurements of diffusion length (L_D). Although we expect to correct these problems, we have shifted our efforts to measure diode uniformity and L_D by using spectral response measurements with a focused light beam.

Scanned Light Beam and Diffusion Length Measurements

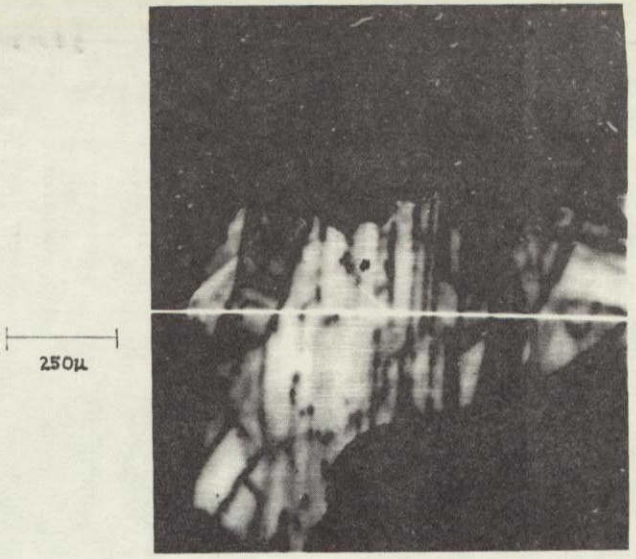
Instrumentation has been set up for measuring spectral response and diode uniformity. The system consists of a xenon lamp, a prism monochromator, and related optics. A pinhole which can be varied is imaged onto the sample surface with an F/2.8 Cassegranian reflective object whose focal length is independent of wavelength. The diode is scanned using a motorized stage and the short-circuit current is used to measure diode uniformity.



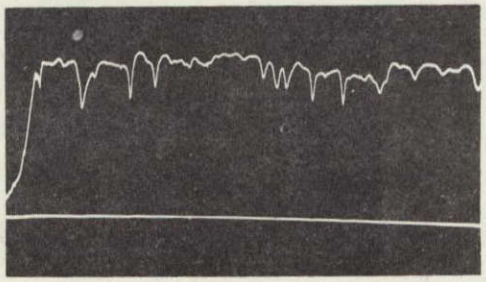
(A) EBIC image of silicon-on-ceramic photodiode. R78D-42-6



(B) EBIC line scan of bright line in (A) showing zero current level where beam crosses wire and particles.



(C) Same as (A) showing detail of grain structure



(D) Line scan of (C) showing quantitative loss of EBIC signal at grain boundaries.

Figure 29. EBIC measurements of diode uniformity

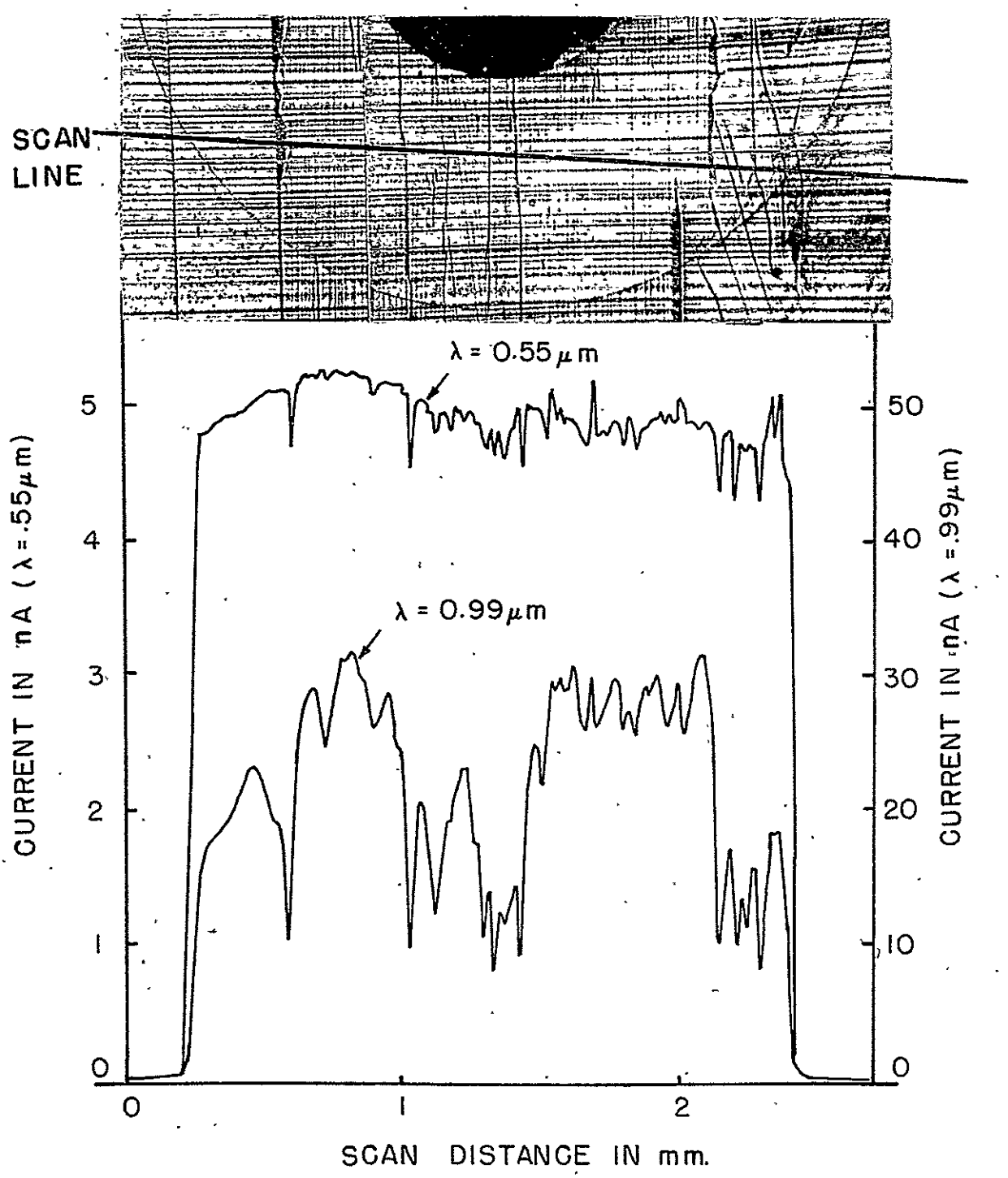


Figure 30. Light Beam Scans of Diode R169A-616-1-5. In the photograph of scan, the horizontal lines are growth strictions. The vertical lines are low-angle grain boundaries, and twin lines.

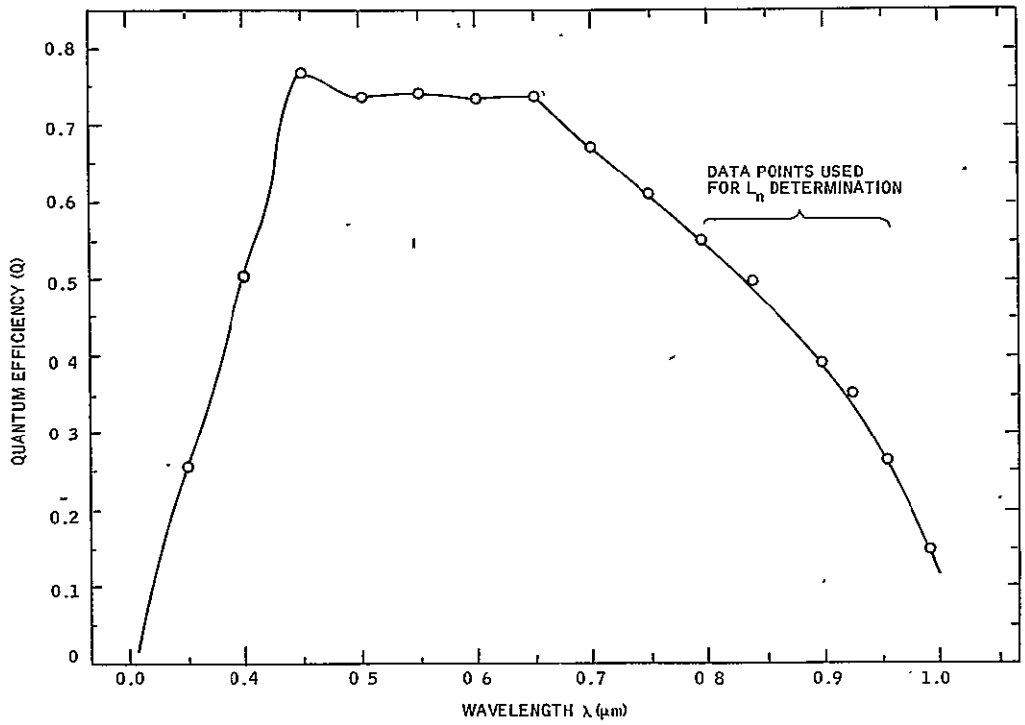


Figure 31. External Quantum Efficiency Q as a Function of Wavelength

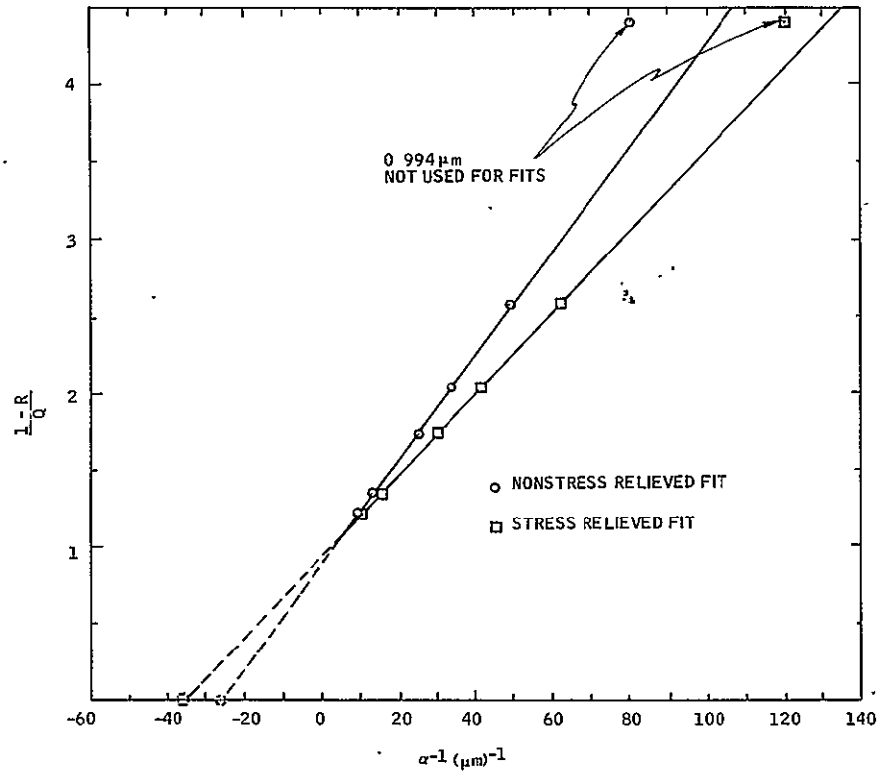


Figure 32. Plot of reciprocal Quantum Efficiency Versus Reciprocal Absorption Coefficient α

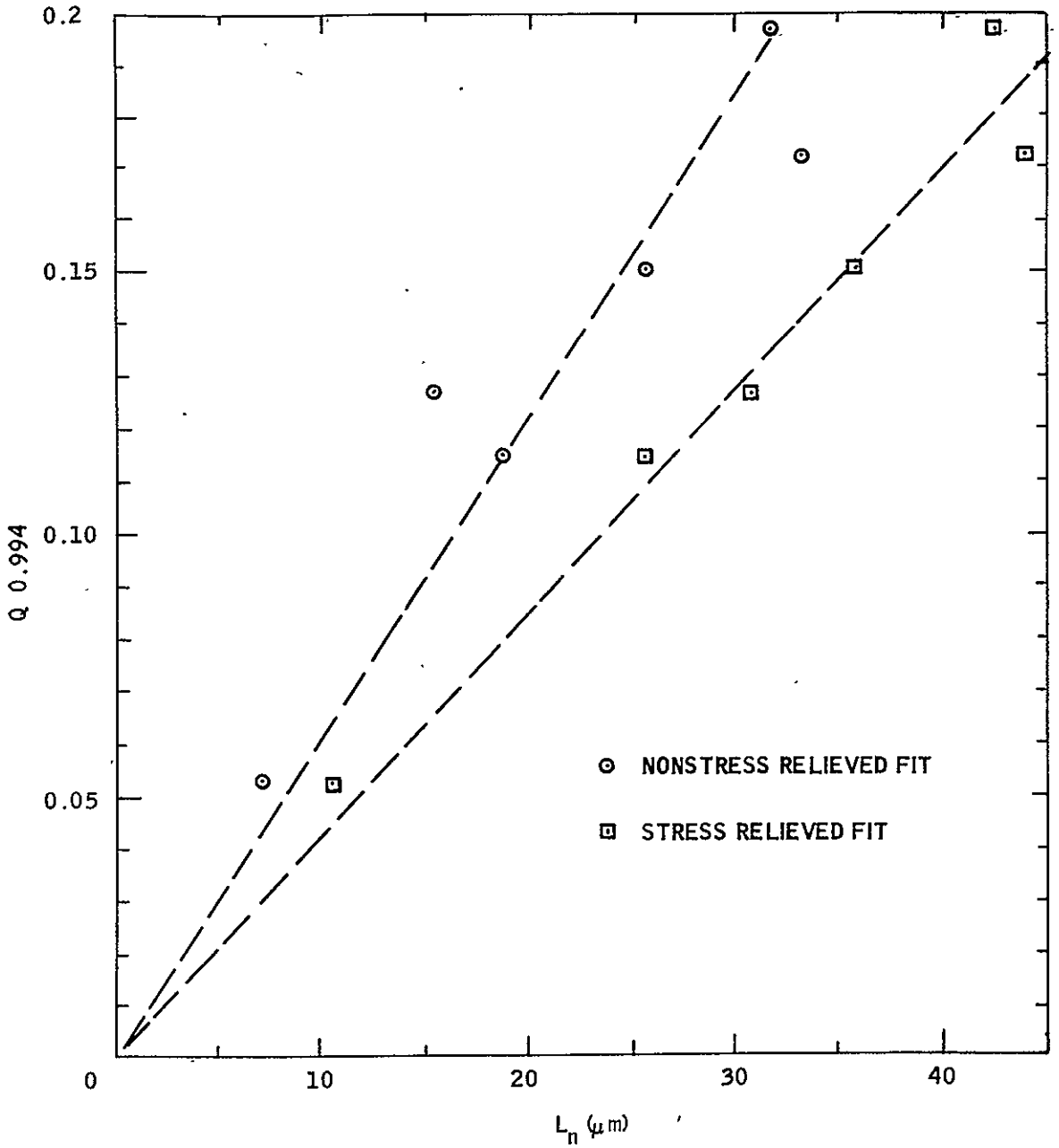


Figure 33. Plot of Q at .994μm Versus L_n for Various Samples.

We should also note that the scans at 0.994μm give currents in the range of 10-30 na. If the pinhole is in perfect focus, the area illuminated has a diameter of 8μm, or an area of 5×10^{-7} cm^2. Thus the current density is in the range of current density observed at one sun (20-30 ma/cm^2).

Solar Cell and Photodiode Performance

As stated previously, our fabrication process has changed considerably during the course of the year. Our procedures for making the single-crystal comparison cells and setup for measuring solar cell performance have also been improved.

Solar cell characterictics are measured with a new setup using two ELH 300W tungsten-iodide slide projection lamps which have a color temperature of 3400°K and an internal dichroic reflector which fliters out some of the IR. This source more closely simulates the solar spectrum than the previous system using a flood lamp. We also built a ramp generator to automatically sweep out an I-V characteristic, although the manual mode can still be used if desired.

The results of measurements on single crystal comparison cells are summarized in Table 5. In principle these cells should be made with exactly the same fabrication procedure as the SOC cells.

However, the surface preparation must necessarily be different. The SOC cells are given an HF etch and sometimes a very light surface etch. The single-crystal cells have been made with a heavy CP4 etch on the polished wafers to remove polishing damage. It was observed, as shown in Table 5, that the best single-crystal results are not obtained in this way, but are obtained with a lapped surface. The higher value may be due to lower reflectivity of the surface, or it may be due to gettering action of the front surface. At any rate, we feel that the heavily etched surface most closely resembles the as-grown surface of the SOC and that this process should be used for comparison cells.

Early in the year, aluminum-doped single-crystal cells were prepared from a Czochralski ingot grown at Honeywell. Four diodes made on an Al wafer averaged 10.2 percent conversion efficiency, whereas four cells made from a boron-doped comparison cell averaged 11.2 percent efficiency. Both V_{OC} and J_{SC} were slightly lower in the aluminum-doped wafer. It should be mentioned that both wafers had lapped (1000-grit) front surfaces but had no antireflection coating. The cells had the conventional geometry with a back contact of electroless neckel and a front contact of silver paste. The diffusions were done at 900°E for 20 minutes.

Table 5. Performance of Selected Single Crystal Control Cells.

Diode No.	Diffusion Temp(°C)[a]	Time (min)	Number of Diodes Averaged	Active Area (cm^2)	^{o}S (ohms/□)	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor	Efficiency (%)	Comments
SC36 B1	904	20		0.042	23	0.55	25.4	0.66	9.2	Etched surface bottom base contact
SC36 B2	904	20		0.036	23	0.55	23.9	0.70	9.2	
SC37 A1	904	20		0.083	23	0.54	22.2	Poor		Electroless nickel top base contact
SC38 C1	900	20		0.111	20	0.55	21.8	0.713	8.6	$PtSi$ top base contact
SC39 A2	902	15		0.094	25	0.51	29.4	0.51	7.8	Top e-Ni, top base contact
SC40 A2	904	60		0.084	14	0.53	26.1	0.525	7.3	
SC42 A3	904	20	4	0.057*		0.51*	27.2*	0.73*	10.2*	Al-doped base, lapped surface
SC42 B3	904	20	4	0.064*		0.53*	29.1*	0.72*	11.2*	Lapped surface
SC42 C2	904	23		0.080		0.54	25.7	0.59	8.2	Polished surface
SC41 C2	901	20		0.039	26	0.52	22.3	0.73	8.5	Polished surface, Al-doped base
SC44-02	966-1017	14		1.0		0.53	23.8	0.64	8.0	$PtSi$ contacts, etched surfaces
SC44-04	966-1017	14		1.0		0.54	21.4	0.71	8.3	
SC47-1	904	20	5	0.02*		0.54*	24.6*	0.76*	10.1*	$PtSi$ + Ni base contact
SC50-4	904	20	6	0.07*	24	0.55*	25.1*	0.73*	10.0*	Photolithography pattern
SC50-3	904	20		1.00		0.53	23.0	0.59	7.1	
SC52-3	908	20	4	0.03*	16	0.54*	26.0*	0.77*	10.8*	
SC52-4	908	20	4	0.05*		0.36*	21.5*	0.63*	4.9*	Sandblasted surface
SC54	832	20	4	0.04*	92	0.53*	29.8*	0.75*	11.5*	
SC61	870	30		1.0		0.54	23.3	0.68	8.6	
SC61a-1	870	30	6	0.07*		0.53*	23.6*	0.72*	9.0*	
SC68	857	25		10	68	0.55	25.0	0.36	5.0	10 cm^2 cell
SC69	863	30		1.0	32	0.53	23.7	0.58	7.4	
SC71a	866	25		1.0	45	0.54	25.7	0.61	8.3	Spin on diffusion
SC71b	866	25		1.0	45	0.54	25.7	0.65	9.0	
SC74	862	25		1.0	62	0 51	25.3	0.61	7.9	

[a]Average values.

These results show that the Al doping introduced by the mullite does not degrade the solar cell performance. This conclusion is in agreement with studies by Professor C. T. Sah (University of Illinois) that show that recombination centers involving aluminum complexes only form if the material is processed above 1000°C. Of course, in our continuous-coating method we expect that a minimum amount of aluminum will be dissolved, and that the performance of Al - doped solar cells will be irrelevant.

Table 5 also illustrates the effects of using different cell geometries and contacting methods, the effects of different diffusion times and temperatures and different diffusion sources. We have found that with improved ohmic contact to the base region, there was no difference in performance between cells with base electrodes on the top and those with electrodes on the bottom. We expect other improvements in processing will lead to higher efficiency and more uniform performance.

The performance of SOC solar cells is summarized in Table 6. The results are listed in chronological order of processing. Our first photodiodes were only a few square millimeters in area. The diode patterns made with the photolithographic process described above have shown significantly better performance than the cells made by the earlier process.

Both the results of measurements on small (few mm^2) photodiodes and on $1cm^2$ solar cells are summarized in Table 6. In taking averages, cells that were atypically poor were not included. Usually these were a small fraction of the total number.

Substrates MR78 and MR106 had vitreous carbon (Vitregraph) instead of rubbed graphite as the coating on the ceramic. There appear to be enough variations in processing that it is difficult to attribute any significant difference to the Vitregraph.

A number of diodes were made on Substrate R107A that had been diffused once, lightly etched to remove the diffused layer, then rediffused and processed. Although some of the diodes were the best to date, the statistical scatter is large enough that it is not clear if the gettering had any effect. The diffusion at 870°C should have given a sheet resistance higher than the observed ρ_s = 18 ohms/sq.

We developed the 1 cm^2 solar cell patterns (shown in Figure 25b) during the third quarter and, after initial runs that were not successful because of obvious problems like misregistration, produced the results shown for substrates R172D and R169A in Table 6 and in Figure 34a and b.

Table 6. Summary of SOC Solar Cell Performance.

Sample	No. of Diodes	Average Active Area cm^2	ρ Ohm-cm	ρ_s Ohms /□	Average V_{oc} Volts	Average J_{sc} ma/cm^2	Average FF	Maximum η %	Average η %	Comments
R12-9-3	1	0.004	1.7	22	0.38	5.6	0.62		1.2	
R45B-27-3	1	0.01	4.0	--	0.44	14.8	0.68		4.4	
R47A-27	8	0.02	0.6	--	0.40	6.0	0.64	3.3	1.5	Melt exposed to mullite for 1 hour
R78A-33	8	0.02	2.3	10	0.45	15.0	0.69	5.9	4.6	Vitreous carbon
R78D-42	5	0.03	2.3	21	0.46	20.0	0.65	6.5	6.1	Vitreous carbon
R107D-47	9	0.07	5.0	--	0.48	18.0	0.59	6.25	5.1	
R106J-46	4	0.01	--	17	0.45	14.0	0.68	4.9	4.3	Vitreous carbon
R106A-45	5	0.05	--	--	0.45	14.0	0.66	4.5	4.3	Vitreous carbon
R107C-50	6	0.07	5.0	23	0.50	21.0	0.67	7.5	7.0	
R107A-51	9	0.05	5.0	18	0.49	20.0	0.69	7.8	6.9	Gettered substrate
R169A-61	1	1.0	--	--	0.50	20.0	0.68		6.9	
R172E-62-1	1	1.00	1.5	20	0.50	17.0	0.68		5.7	
65-7F-66	1	1.00	1.2	~60	0.50	21.0	0.67		7.2	Dag carbon
65-2A-65	1	1.00	1.2	40	0.50	22.0	0.65		7.0	
65-2C-65	7	0.08	1.2	40	0.49	21.0	0.69	8.0	7.3	
R169A-6aB-1	3	0.09			0.51	23.6	0.69	8.6	8.1	
R169A-61B-2	5	0.05			0.50	22.5	0.68	8.1	7.7	
R169B-61B-1	7	0.08			0.50	20.5	0.71	7.9	7.2	
R172A-70	7	0.08	1.5	40	0.45	20.4	0.59	7.0	5.4	
R172D-59	1	1.00	1.5	53	0.50	20.6	0.68		6.7	
R169B-61b	1	1.00			0.50	21.3	0.68		7.1	
63-2	1	10.0		54	0.49	12.4	0.35		2.8	First 10 cm^2 cell
76-1B-77-7	6	0.085	2.3	31	0.49	17.1	0.71	6.7	6.0	Dag carbon
59-8B-63	7	0.08		45	0.50	13.5	0.68	5.0	4.6	Small grain size
76-1A-77	1	1.00	2.3	31	0.49	17.5	0.68		5.9	Dag carbon
76-2A-78	1	1.00	2.3	37	0.47	15.8	0.59		4.4	Dag carbon

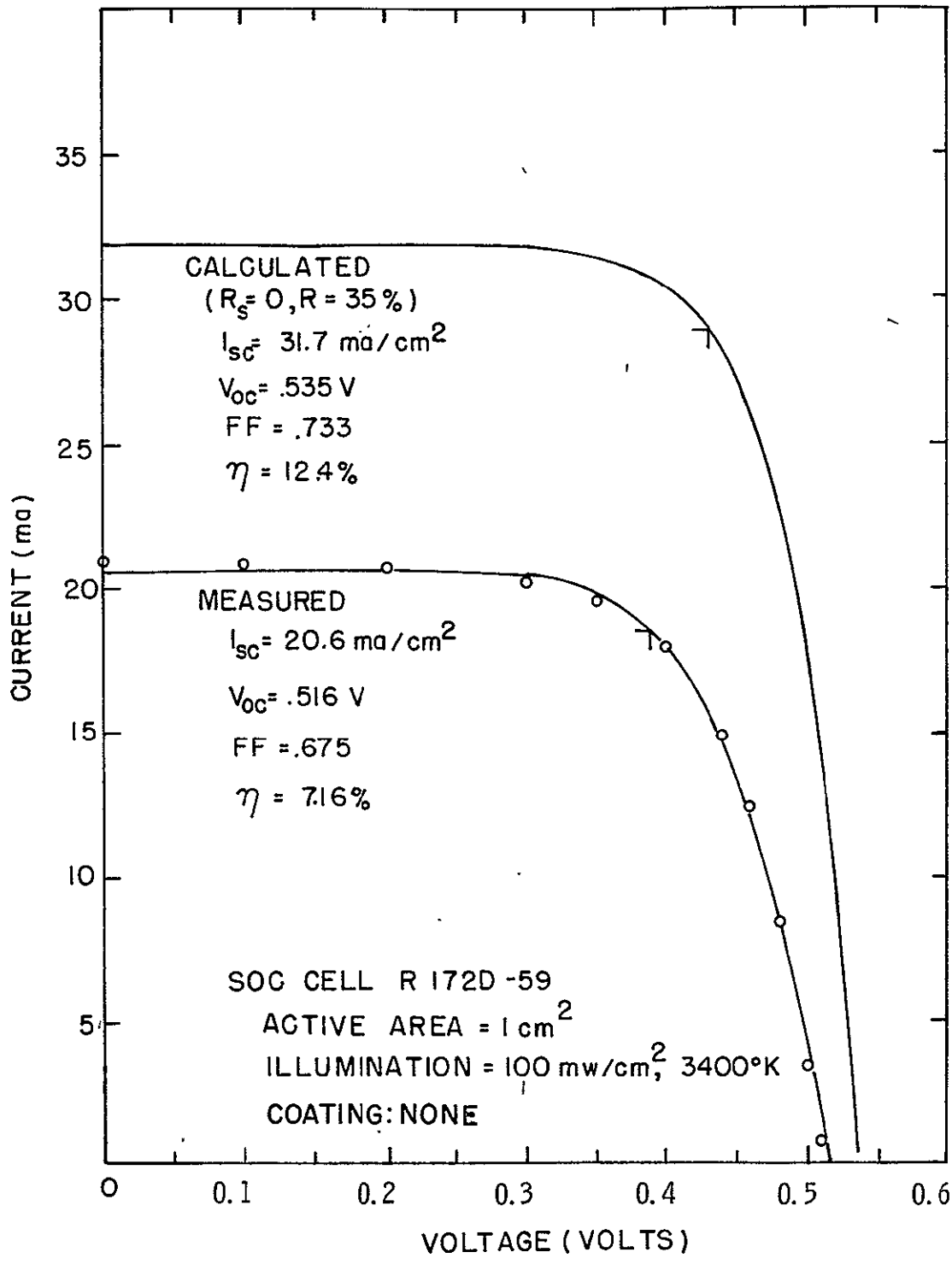


Figure 34a. IV Characteristics of an SOC Solar Cell.

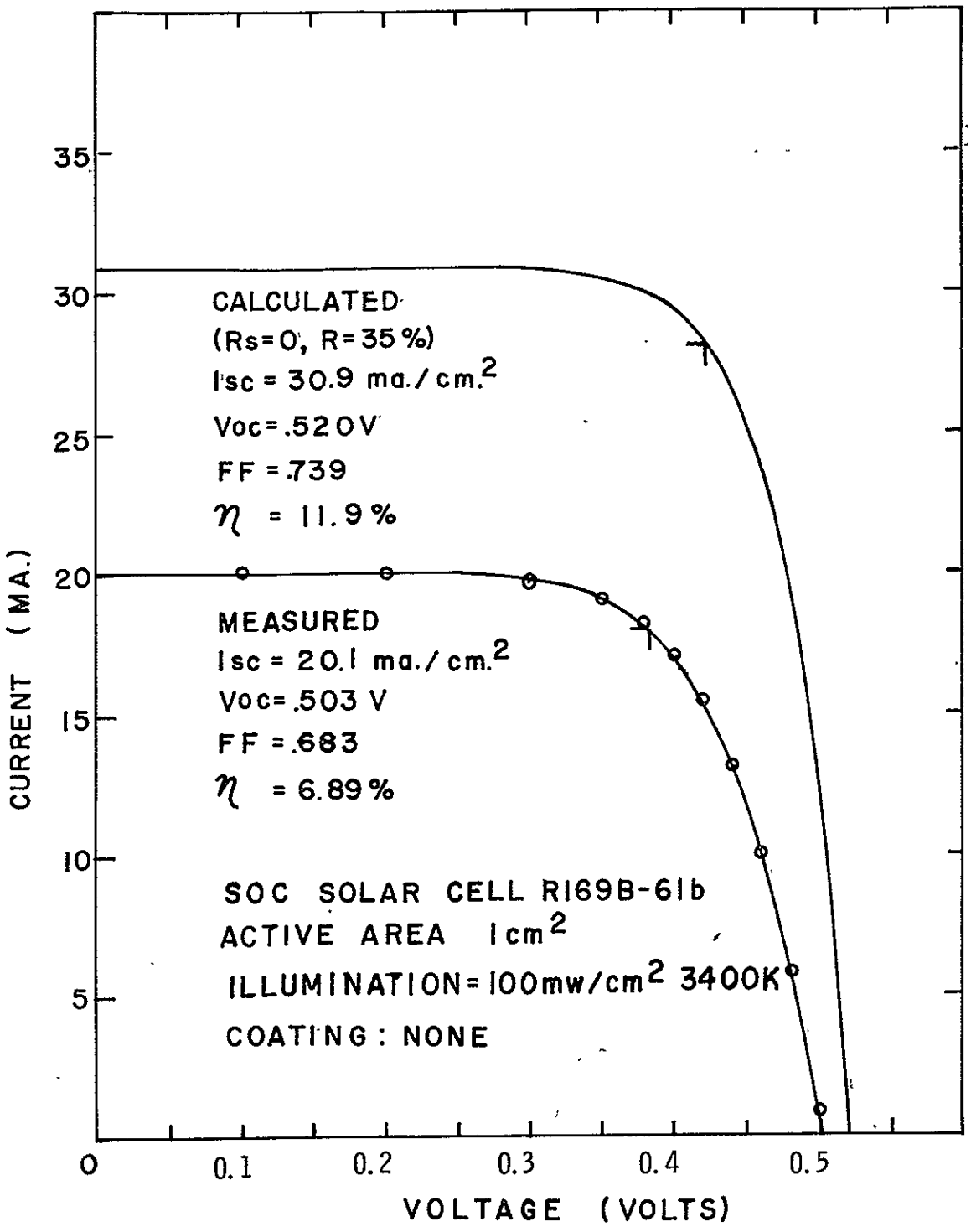


Figure 34b. IV Characteristics of an SOC Solar Cell.

In these figures the inherent efficiency is also shown. The data points were measured on the x-y plotter. The data points were fit by the procedure described in Quarterly Report No. 4 (published 12/28/76). With the fitting process a value of R_s the series resistance is derived. For the diodes shown, the value of R_s was 1.5 ohms both for the poly cells and for the single-crystal cell shown in Figure 35.

The inherent efficiency curves are derived by setting $R_s = 0$ and correcting for the reflectivity. As discussed in the section above on reflectivity measurements, a reflectance of 35 percent was assumed. The inherent efficiency values as discussed by Hovel[7] are a truer indication of the capabilities of the material than the actual efficiences which are sensistive to the fabrication procedure.

Another way of indicating the quality of the material is to compare the efficiency of the SOC cells to those of single-crystal cells made by the same process. Such a comparison is shown in Figure 36 for $1cm^2$ cells. Such a comparison obviously depends on which cells are compared. The average for the three best SOC $1cm^2$ cells to date is 7.1 percent while the average for the three best single-crystal comparison cells is 8.5 percent. The comparison in Figure 36 represents these averages since it compares the second best of each type.

The first $10cm^2$ active area SOC cell was fabricated during this report period on substrate 63-2M7H. The results were quite encouraging. The V_{0c} was 0.49 compared to 0.53 for single-crystal cells. The fill factor was quite poor probably due to the bulk resistance of the base. The value of J_{sc}, obtained by extrapolating to negative voltages, was 190ma, or $19ma/cm^2$ compared to 220 ma or $22\ ma/cm^2$ for the single-crystal control cells. Thus the performance on this cell is comparable to that of smaller cells expect for the low fill factor which led to an uncoated deficiency of 2.8 percent. The efficiency in the diodes made from run 76 was not as high as some of the previous cells.

Although these cells were made with the dag carbon, it is probably not the factor causing poor performance since diode 65-7F-66 also used the dag carbon and did not show poor performance. The single-crystal comparison cells processed in parallel with these cells showed a poorer fill factor than normal. Thus some of the decrease in performance may be due to the relocation of the processing equipment and the change in personnel during the last quarter. However, the J_{sc} and V_{co} values of the single cells were typical, so that the reduced value of these parameters in the SOC diodes may reflect a possible contamination problem in the SOC material.

In summary, we consider the above results to be highly significant for the following reasons:

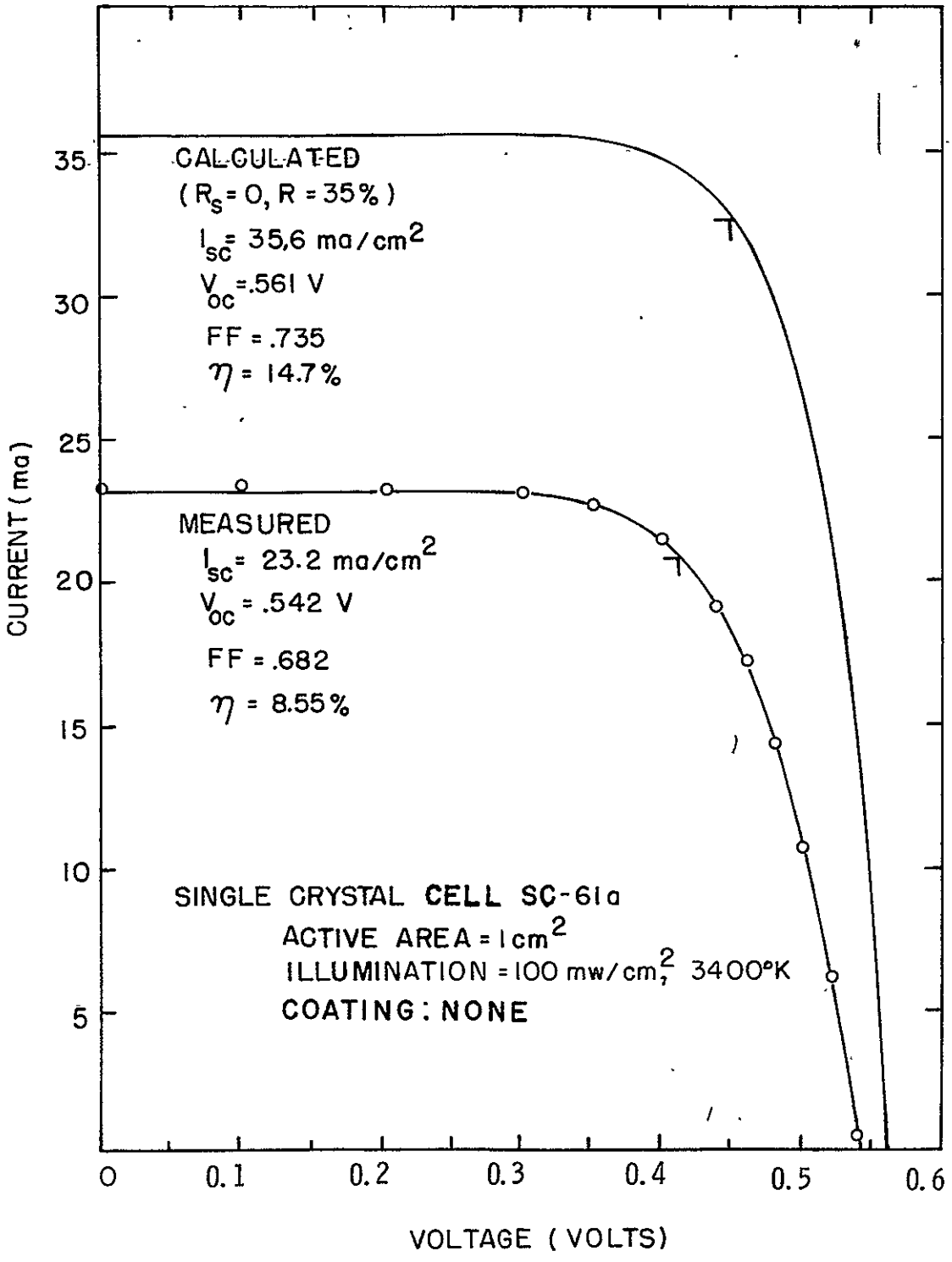


Figure 35. IV Characteristics of a Single-Crystal Comparison Cell.

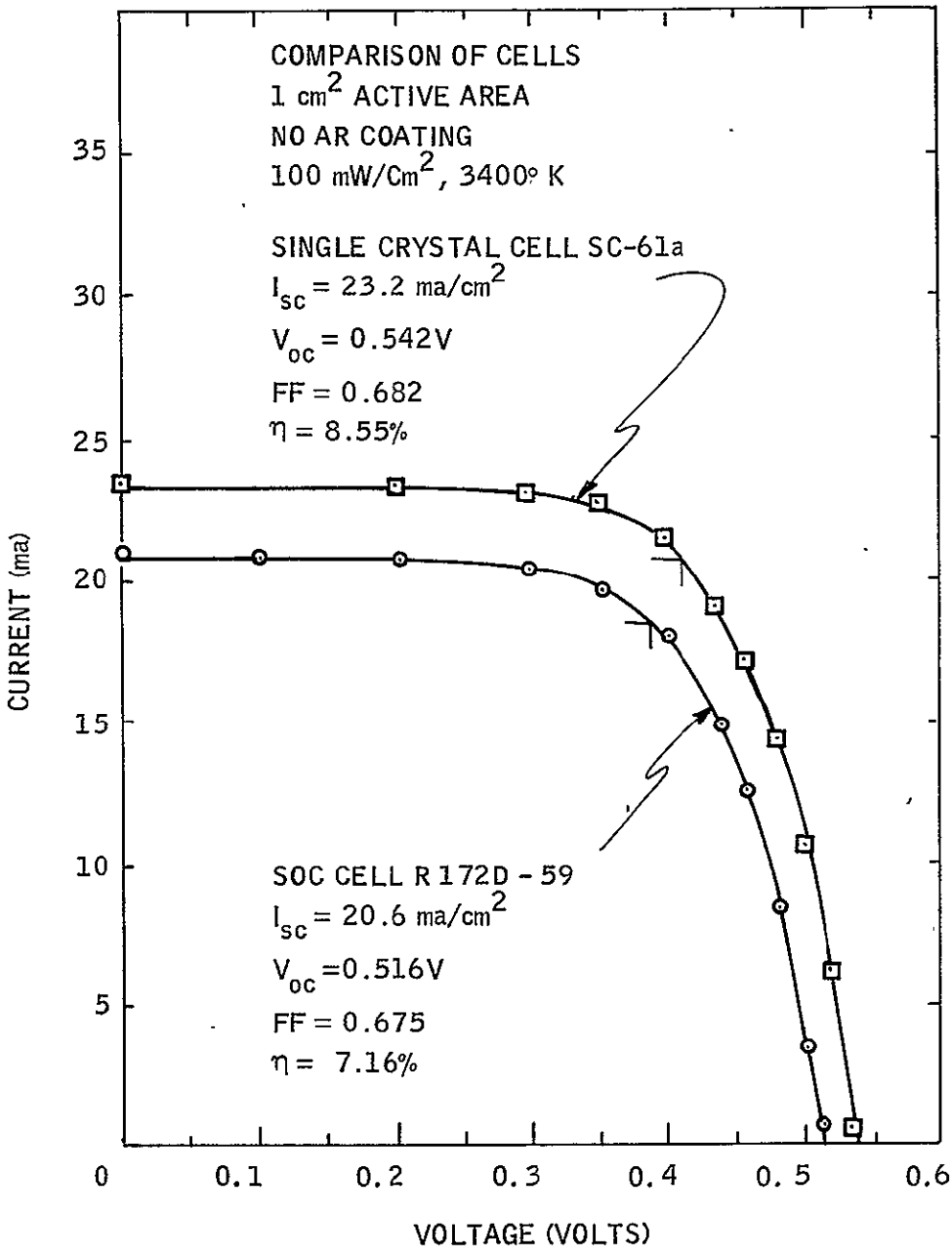


Figure 36. I-V Characteristics Comparing on SOC Solar Cell with a Single-Crystal Control Cell

- A number of small photodiodes made from the same substrates show nearly the same results. They have not been fully evaluated, however, and therefore were not included.

- The performance of the SOC cells is almost as good as that of the single-crystal comparison cells (Figure 35): the V_{oc} and J_{sc} values were within 9 percent of the single-crystal values. Thus some improvement might result from improved processing. In particular, we expect to change from using a P_2O_5 source to a phosphiene source during the next quarter.

- Substrates MR172 and 65-7F-66 which show more than 7 percent efficiency, were the seventh substrate dipped in the series. Thus they were grown from silicon exposed to impurities from the mullite.

- After correcting for relfectivity losses (assumed to be 35 percent) and series resistance, the calculated inherent efficiency was greater than 12 percent, compared to 15 percent for the single crystal.

- If one allows a reasonable value for series resistance, AR coating, and electrode area, the efficiency of these cells would have been about 10 percent.

The results for the $10cm^2$ cell show the values of J_{sc} and V_{oc} are not significantly degraded even though the area is changed by a factor of 200. On the other hand the series resistance problem with the interdigital electrodes is serious.

We are therefore very encouraged by these results and believe that they demonstrate that the SOC process can produce solar cell quality material. Of course, other significant hurdles remain: production of high-quality material at fast growth rates and demonstration of a suitable base contact method. Our work on device modeling and cell design is a key to the series resistance problem, and permits us to evaluate the potential of proposed solutions.

PARASITIC RESISTANCE ANALYSIS (S. B. Schuldt)

Introduction

This subsection deals primarily with the resistive losses which are inherent in the SOC approach to low-cost solar cell arrays. Some of these losses are unique to the SOC concept with its unusual method of electrically terminating the base layer. Full device optimization is not attempted here. A possible approach to optimization could be along the lines of a recent paper by Crook and Yeargan, [8] but using the more detailed series resistance model presented here. Although short-circuit current, open-circuit voltage and fill factor remain to be optimally determined, [9] these are assigned arbitrary fixed values in the calculations in this report.

The basic electrical structure of the SOC concept is illustrated in cross-section in Figure 37. For definiteness, an N^+ on P structure is assumed, giving the cell polarity shown in the figure. The illuminated front surface is provided with regularly spaced striped electrodes which are modeled as a top metallic layer contacting the N^+ diffused layer through an intermediate metal-semiconductor interface. The interface is characterized by a specific contact resistivity ρ'_C ohm cm^2. Photogenerated minority carriers which diffuse to, and traverse the junction, are responsible for the photocurrent. This enters the structure through the interconnected (negative) front contacts, spreads through the diffused layer, crosses the junction, and converges through the base layer to the (positive) back contacts. A carbonized layer on the ceramic substrate may provide part of the current path on the back side of the junction. The back contacts are at the ends of fins of base silicon material projecting through slots in the ceramic substrate, and therefore differ significantly from the front contacts. Moreover, the spacings of the two sets of contacts are not necessarily the same. It is presumed throughout the report that the back-contact spacing b may exceed the front-contact spacing b′ but that the ratio b/b′ is an integer. A unit of the periodic structure will be taken as the b x w rectangular area bounded by the lines centered on adjacent back electrodes, and having arbitrary width w perpendicular to the plane of Figure 37. Current flow is assumed everywhere parallel to the plane of Figure 37. This amounts to ignoring the collecting effect of the contact bars which connect the stripes together. [10]

Parasitic resistances occur at contact interfaces and in the front and back (diffused and base) layers. These not only reduce the maximum power available to the load, but shift the maximum power point toward both lower voltage and lower current density. This may be illustrated qualitatively by means of Figure 38. The upper curve gives the hypothetical ideal illuminated cell characteristic (no parasitic losses). In this case the load voltage is the same as the voltage V_D across the junction, here assumed to be uniform. Maximum power density (product $V_D J$) is labelled W_o^*. The lower curve represents a

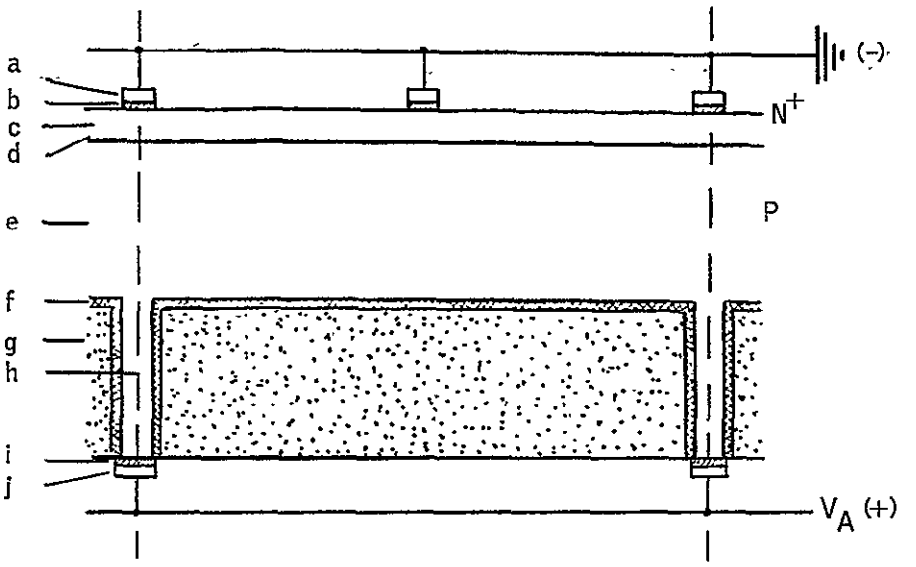


Figure 37. One Unit of the Periodic Structure of a SOC Solar Cell. Features (not drawn to scale): (a) contact metal, (b) metal-semiconductor interface, (c) diffused layer, (d) junction, (e) base layer, (f) vitreous carbon layer, (g) ceramic substrate, (h) base layer extrusion or fin, (i) metal-semiconductor interface, (j) contact metal.

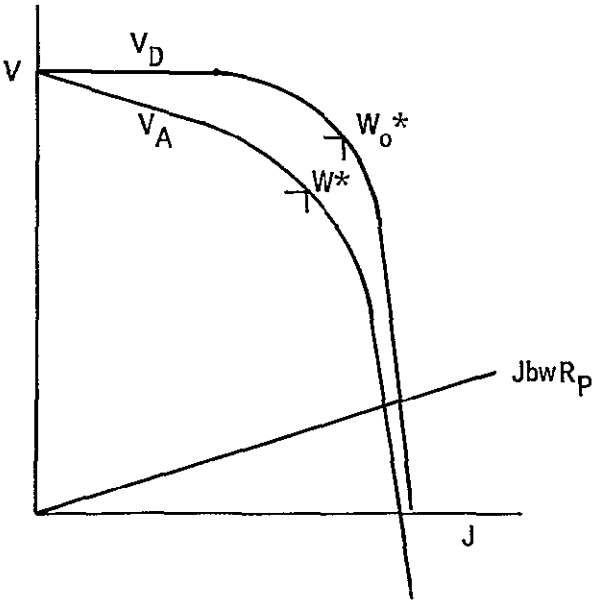


Figure 38. Determination of Optimum Solar Cell Operating Point According to Lumped Model for Parasitic Resistances.

particular nonideal characteristic due to a specific parasitic resistance R_P. The available load voltage differs from V_D by the series IR drop; i.e., $V_A = V_D - J\,bw\,R_P$. Maximum power density on this curve is labelled W^*.

The foregoing illustration makes use of two assumptions: that the internal resistances can be lumped and that V_D and J are constant along the junction. These assumptions cannot be strictly true due to the obviously distributed nature of the device. The parasitic IR effect varies from a maximum at the middle of a unit to near zero at the ends so that V_D is not exactly constant. Moreover the bulk and contact components of the resistance are not strictly separable because of so-called current crowding in the semiconductor layers near the contacts. Fortunately, if certain reasonable auxiliary conditions are satisfied, the assumptions are justified to a good approximation. Specifically, the dissipated power should be relatively small, and the contact spacings b and b′ should be large compared to the diffused layer thickness and base layer thickness, respectively, and the metallized areas should be small fractions of the total area.

The following subsections develop an approximate lumped resistance model and discuss some of its implications with respect to cell performance. The appendices offer a more exact analysis of the distributed system as a logical basis for the approximations.

The Solar Cell Junction Parameters

The illuminated solar cell characteristic (Figure 38) is assumed to follow the single-exponential model [11]

$$J = J_o - J_1 (e^{AV_D} - 1) \qquad (1)$$

locally at any given point in the junction plane*. J_o is the illuminated short-circuit current density and J_1 the reverse saturation current density. The parameter A has an ideal theoretical maximum of $q/kT = 38.7\ \text{volt}^{-1}$ but in silicon solar cells is always considerably smaller. J_o, J_1, and A are strongly dependent on the material and junction fabrication technology. The choice of numerical values is therefore somewhat arbitrary and subject to speculation. This should be borne in mind when interpreting the calculated results included in this report. The output may depend critically on the parameters. The present choice is based on a short-circuit density $=0.03\text{a/cm}^2$, open-circuit voltage $=0.55$V, and $A = 30$. This value of J_o corresponds to AM1 sunlight and is not corrected for reflection losses. J_1 is then found to be

$$J_1 = J_o/(e^{AV_{oc}} - 1) = 2.05 \times 10^{-9}\ \text{a/cm}^2.$$

*The depletion layer width may not be negligible. However the word "plane" here implies that current passes through the depletion layer perpendicular to its boundaries and with negligible ohmic effects.

These parameters yield a power density maximum = 12.9 mw/cm^2 and fill factor = 78 percent.

Power Dissipation

The ideal performance figures are degraded in practice by series and shunt parasitic resistances and by front electrode masking. The shunt component is not included here since its causes [12] are related more to diode fabrication than to device geometry considerations and should therefore respond to improved processing techniques. Electrode masking is omitted also; if the masked area is not too great, a multiplicative masking factor on J_o should serve this purpose within the accuracy of the model.

Dissipation occurs serially through front contact interfaces (R_c'), front silicon layer (R_L') back silicon and carbon layers (R_L) and back fins and contact interfaces (R_c). The lumped equivalent circuit for a single-cell unit is shown in Figure 39, and total parasitic resistance is $R_P = R_c' + R_L' + R_L + R_c$.

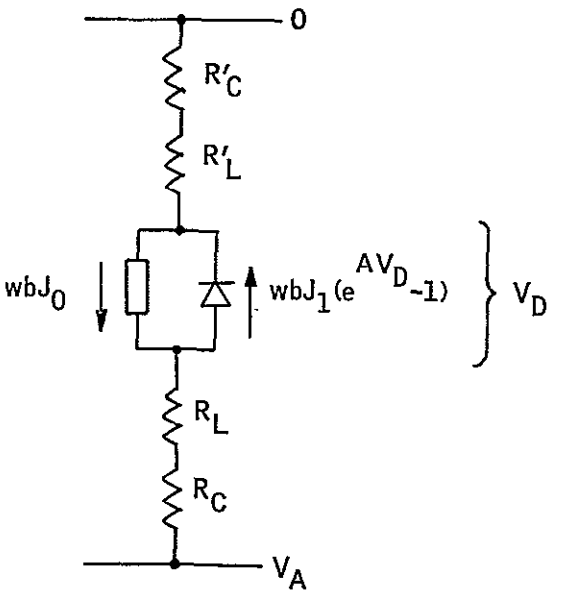


Figure 39. Lumped Components of Parasitic Resistance of a Cell Unit.

The operating characteristic J versus V_A for a given R_P (lower curve of Figure 38) may be expressed parametrically in terms of the junction voltage V_D as

$$J = J_o - J_1 (e^{AV_D} - 1) \tag{2}$$

$$V_A = V_D - bwJR_P, \quad 0 \leq V_D \leq V_{oc}. \tag{3}$$

The desired operating point is obtained by maximizing the product JV_A with respect to V_D. This gives the following condition on V_D, which is easily solved numerically:

$$\{J_o - J_1 [e^{AV_D} - 1]\} [1 + 2bwJ_1R_PA] - AV_DJ_1e^{AV_D} = 0 \tag{4}$$

The power density decreases as the cell width b increases for two reasons. First, for a fixed R_P the cell current increases with b causing the IR_P drop to increase. Second, R_P itself increases with b. The first effect is demonstrated in Figure 40, where maximum available power density is plotted as a fraction of the ideal 12.9 mw/cm^2 (R_P = 0). From this plot it can be seen that bwR_P must be restricted to 0.83 ohm cm^2 or less to keep the relative efficiency from falling below 95 percent. More specific inferences may be drawn from this arbitrary criterion after the components of R_P have been quantitatively identified.

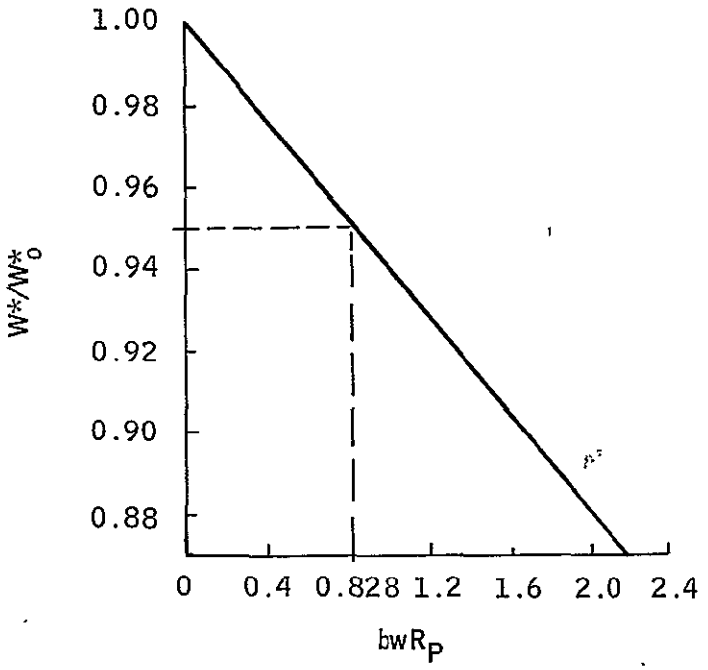


Figure 40. Maximum Available Power Density (Relative) as a Function of Cell Area Times R_P.

Components of Parasitic Resistance

Front Contact Resistance -- As noted earlier, the unit cell width b is a multiple of the front contact spacing b′, so that the front area contains b/b′ (see Figure 41) subunits per cell unit. From the symmetry of a subunit, assuming uniform J, it is obvious that the cell current bwJ is shared equally by 2b/b′ half-contacts each with area equal to d′w/2. According to the extended transmission line model (ETLM) [13, 6], the series resistance due to one of these strips is approximately

$$(h'/w) \cdot R_{\square}' = \sqrt{\eta' + 0.2}\, \coth\{(d'/2h')/\sqrt{\eta' + 0.2}\}$$
$$\eta' = \rho_c'/[(h')^2 R_{\square}'] \qquad (5)$$

where $R_{\square}'$ is the sheet resistance (ohms/□) of the N^+ layer and ρ_c' is the specific contact resistivity (ohm cm^2) of the contact interface. Since the 2b/b′ half-contacts are in electrical parallel, the net front contact resistance for the cell unit is

$$R_c' = (b'/2b)(h'/w) \cdot R_{\square}' \cdot \sqrt{\eta'+0.2} \cdot \coth\{(d'/2h')/\sqrt{\eta'+0.2}\}. \qquad (6)$$

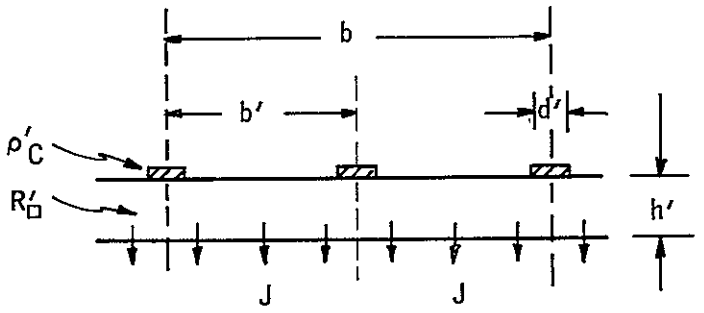


Figure 41. Front Subcell Geometry for the Case b/b′ = 2 (Distorted Scale).

A more exact result is obtained by solving the two-dimensional Laplace equation representing semiconductor layer and contacts. Contact resistance may be calculated from the potential function (see Appendix A).

Front Silicon Layer Resistance -- the subunit of area wb′ is modelled here as a sheet with current Jwb′/2 entering at each edge and exiting with uniform density J through the surface (junction). The exact current path with finite sheet thickness is found in

Appendix A. If positive current is from left to right and x is the coordinate measured from from edge to edge ($0 \le x \le b'$), the sheet current in the present approximation is

$$I(x) = wJ\,(b'/2-x), \tag{7}$$

and the voltage relative to the edges, not including the voltage drop in the contacts, is

$$V(x) = -\frac{1}{w} R_{\square}' \int_0^x I\,(z)dz = -JR_{\square}'(b'x-x^2)/2. \tag{8}$$

The minus sign is required because positive current flows away from the edges. The power dissipated in the subunit is

$$P' = \int_0^{b'} |wJV(x)|\,dx = J^2 R_{\square}' wb'^3/12. \tag{9}$$

The front layer resistance is power (for the whole bxw unit) divided by the square of the current:

$$R_L' = (b/b')P'/(wbJ)^2 = \frac{1}{12}\left(\frac{b}{w}\right)\left(\frac{b'}{b}\right)^2 R_{\square}'. \tag{10}$$

Back Layer Resistance-- Because of the direction of current from the junction toward the back contacts, the voltage in the back layer increases toward the center of the unit. By a one-dimensional model analogous to the one in the subsection on Front Silicon Layer Resistance, the back surface voltage relative to the silicon side of the back contacts is

$$V(x) = JR_{\square}(bx-x^2)/2. \tag{11}$$

Dissipated power is

$$P = J^2 R_{\square} wb^3/12, \tag{12}$$

and back layer resistance is

$$R_L = \frac{1}{12}\left(\frac{b}{w}\right) R_{\square}. \tag{13}$$

The effective sheet resistance $R_{\square}$ may be lower than the p-silicon layer sheet resistance $R_{\square B}$ because of the finite conductance through the vitreous carbon layer on the

ceramic. The effective sheet resistance for Equation (13) is given by the following formula, derived in Appendix C:

$$R_{\square} = [R_{\square B} R_{\square V} / (R_{\square B} + R_{\square V})][1 + 3\frac{R_{\square B}}{R_{\square V}} \frac{\beta \coth \beta - 1}{\beta^2}] \qquad (14)$$

$$\beta = [b^2 (R_{\square B} + R_{\square V})/4\rho_{BV}]^{1/2}.$$

As seen in Figure 42, $R_{\square}$ approaches $R_{\square B}$ as the dimensionless parameter $\beta \to 0$, and it approaches $R_{\square B} R_{\square V}/(R_{\square B} + R_{\square V})$ as $\beta \to \infty$. Hence, for large b or small ρ_{BV}, the p-silicon and carbon layers are effectively in parallel.

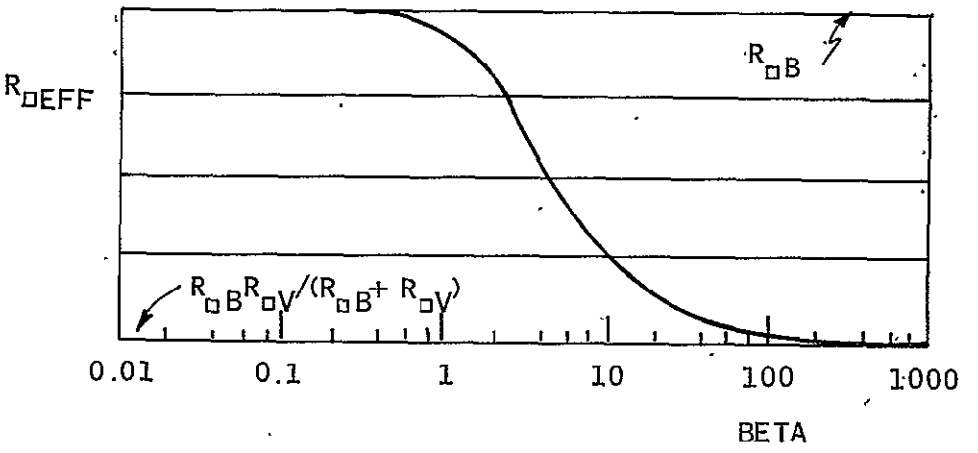


Figure 42. Effective Sheet Resistance vs. Beta from Eq. (14).

Back Contact Resistance -- The back contacts are the entire structures below the back surface plane of the p-layer, and include the fins of silicon projecting through the slotted ceramic, as well as the metal-silicon interfaces. Analysis by conformal mapping (Appendix D) gives the resistance including terms to correct for the curved current paths near the top corners of the fins. These terms are normally quite small, and to a good approximation the current density is uniform in the fins over the whole length t. Then the back contact resistance is simply

$$R_c = (\frac{t}{w})(\frac{h}{d}) R_{\square B} + \rho_c / wd, \qquad (15)$$

where the dimensions are shown in Figure 43. If the vitreous carbon layer extends along the slots in the ceramic, then an effective sheet resistance may be used in

place of $R_{\square B}$:

$$R_{\square} = R_{\square B} R_{\square V} / (R_{\square B} + R_{\square V}) \cdot [1 + (R_{\square B}/R_{\square V}) \tanh \beta/\beta] \qquad (16)$$

$$\beta = [t^2 (R_{\square B} + R_{\square V})/4\rho_{BV}]^{1/2}$$

Equation (16) was derived on the assumption that the carbon layer current falls to zero at both top and botton of the fin.

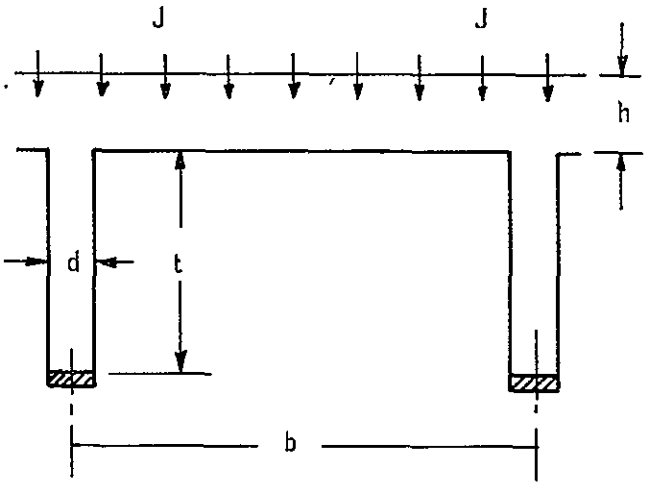


Figure 43. Back Cell Geometry.

Calculation of bwR_P

Under Power Dissipation it was observed that dissipative losses are closely related to the product bwR_P. For the simple junction model and its parameters given earlier in the Solar Cell Junction Parameter subsection, bwR_P should not be allowed to exceed 0.83 ohm cm^2 if 95 percent relative efficiency is to be maintained. A short computer program was written to calculate bwR_P and its components bwR_c', bwR_L', bwR_L and bwR_c. Several parameters in the program and their nominal values are as listed below:

b/b' = 1

ρ_c' = 10^{-5} ohm cm^2 [Ref. 6]

ρ_B' = 1.5×10^{-3} ohm cm

h' = 3×10^{-5} cm

d' = 0.03 cm

ρ_B = 0.3, 1.0, 3.0 ohm cm

ρ_c/ρ_B = 5×10^{-4} cm [Ref. 6]

h = 0.0125 cm

d = 0.03 cm

t = 0.3 cm

It should be noted that the calculations do not depend on w because the w in the product bw cancels the 1/w factor in each component of R_P. The printout (Figure 44) shows the results depending on the base electrode spacing b, for three different base resistivities. The back layer resistance-lowering effect of vitreous carbon was not included.

These tabulations show clearly that a critical problem exists with respect to the back structure resistances, particularly in the cases ρ_B = 1 and ρ_B = 3. A drastic reduction of back layer and electrode resistances, by vitreous carbon shunting or some other means, is necessary if electrode spacing is to be maintained at a few millimeters.

ECONOMIC ANALYSIS (S. Schuldt, R. Winter)

An attempt has been made to model the economics of a large-scale facility for coating ceramic panels with silicon. Following the lead of other companies in the program who have already contributed economic analyses, we chose to set up an economic structure which identifies major categories and subgroupings of cost factors. To each of these factors is assigned, either directly or indirectly, a numerical value which contributes in some way to the price which the customer will pay for the product. Up to this point, the primary emphasis has been placed on completeness of structure rather than accurate assessment of numerical values. To this end, the economic model is formulated as a computer subroutine with some of the required numbers supplied from the main program as independent variables.

W= 1.0000E 00
BRATIO= 1.0000E 00
RHOCP= 1.0000E-05
RHOBP= 1.5000E-03
DP= 3.0000E-02
HP= 3.0000E-05
T= 3.0000E-01
D= 3.0000E-02
H= 1.2500E-02

RHOB= 0.30

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	2.000E-02	3.005E-01	3.633E-01
0.2	2.237E-03	1.667E-01	8.000E-02	6.010E-01	8.499E-01
0.3	3.356E-03	3.750E-01	1.800E-01	9.015E-01	1.460E 00
0.4	4.474E-03	6.667E-01	3.200E-01	1.202E 00	2.193E 00
0.5	5.593E-03	1.042E 00	5.000E-01	1.502E 00	3.050E 00
0.6	6.711E-03	1.500E 00	7.200E-01	1.803E 00	4.030E 00
0.7	7.830E-03	2.042E 00	9.800E-01	2.103E 00	5.133E 00
0.8	8.948E-03	2.667E 00	1.280E 00	2.404E 00	6.360E 00
0.9	1.007E-02	3.375E 00	1.620E 00	2.704E 00	7.710E 00
1.0	1.119E-02	4.167E 00	2.000E 00	3.005E 00	9.183E 00

RHOB= 1.00

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	6.667E-02	1.002E 00	1.111E 00
0.2	2.237E-03	1.667E-01	2.667E-01	2.003E 00	2.439E 00
0.3	3.356E-03	3.750E-01	6.000E-01	3.005E 00	3.983E 00
0.4	4.474E-03	6.667E-01	1.067E 00	4.007E 00	5.744E 00
0.5	5.593E-03	1.042E 00	1.667E 00	5.008E 00	7.722E 00
0.6	6.711E-03	1.500E 00	2.400E 00	6.010E 00	9.917E 00
0.7	7.830E-03	2.042E 00	3.267E 00	7.012E 00	1.233E 01
0.8	8.948E-03	2.667E 00	4.267E 00	8.013E 00	1.496E 01
0.9	1.007E-02	3.375E 00	5.400E 00	9.015E 00	1.780E 01
1.0	1.119E-02	4.167E 00	6.667E 00	1.002E 01	2.086E 01

RHOB= 3.00

B (CM)	FRNT CNCT	FRNT LAYR	BACK LAYR	BACK CNCT	TOT BWR
0.1	1.119E-03	4.167E-02	2.000E-01	3.005E 00	3.248E 00
0.2	2.237E-03	1.667E-01	8.000E-01	6.010E 00	6.979E 00
0.3	3.356E-03	3.750E-01	1.800E 00	9.015E 00	1.119E 01
0.4	4.474E-03	6.667E-01	3.200E 00	1.202E 01	1.589E 01
0.5	5.593E-03	1.042E 00	5.000E 00	1.502E 01	2.107E 01
0.6	6.711E-03	1.500E 00	7.200E 00	1.803E 01	2.674E 01
0.7	7.830E-03	2.042E 00	9.800E 00	2.104E 01	3.288E 01
0.8	8.948E-03	2.667E 00	1.280E 01	2.404E 01	3.952E 01
0.9	1.007E-02	3.375E 00	1.620E 01	2.704E 01	4.663E 01
1.0	1.119E-02	4.167E 00	2.000E 01	3.005E 01	5.423E 01

Figure 44. bwR_P Product as a Function of b for Three Different Base Si Resistivities.

A partial cost breakdown, through the first two levels of the hierarchy, is as follows:

- Capital installation, including amortization and debt interest-
  - Building
  - Production equipment
  - Plant equipment
- Materials and electric power-
  - Ceramic substrate
  - Polysilicon
  - Carbon
  - Argon
  - Power
- Direct labor-
  - Production
  - Engineering
- Burden-
  - Indirect labor and salaries
  - Supplies
  - Services
  - Department management and production planning
  - Allocation based on headcount, wages, and salaries
  - Other allocations
- General and administrative
- Profit

The primary output of the model is price per square meter of silicon-coated ceramic. Parameters of the model are in three categories: independent variables, soft constants, and hard constants.

The independent variables, already mentioned as being passed to the model from the main program, are so designated mainly for the purpose of doing sensitivity studies These quantities are both critical and difficult to assign fixed number to. Having chosen tentative values, it is instructive, therefore, to calculate the incremental effects due to each of them upon the total cost. Independent variables include unit costs as those of silicon, ceramic substrate, and ceramic coating machines. Other independent variables, such as the linear coating (pulling) rate, ceramic thickness, and (Si) coating thickness have important indirect effects on costs. For example, the pulling rate determines the number of coating machines required to produce a given annual quota, and therefore affects both labor and capital costs.

The soft constants are handled as data internal to the subroutine but may be charged as warranted by updated information. These include process yield factor, plant efficiency, thermal loss factor, argon loss factor, labor and burden rates, certain capital costs, and interest rate.

The hard constants are the physical densities, specific heats, and Si heat of fusion.

An early iteration based on best available parameter estimates yielded a price of $12.21 per square meter, including profit. In this determination, the major cost items were poly Si ($2.91 per square meter), labor and burden ($2.50 per square meter), and the ceramic substrate ($2.50 per square meter). A pulling rate of 1 cm/sec was assumed. The added value, excluding poly Si cost, is $9.29 per square meter. The burden rates taken for this calculation represent a somewhat different production situation and are not necessarily realistic for the silicon coating operation. The details of the estimate are presented in the accompanying computer printout (Figure 45). All amounts are in terms of 1977 dollars.

Iterations of the model under varying input conditions show that the pulling rate becomes a cost-critical factor below 0.2 cm/sec. At 0.1 cm/sec the price is $25.37/$m^2$ (1977 dollars). The price decreases rapidly as the pulling rate increases, reaching $17.80/$m^2$ at 0.2 cm/sec. At higher pulling rates, the price begins to level off. (see Figure 46).

Since the model was developed prior to receiving the Solar Cell Manufacturing Industry Costing Standards (SAMICS) Workbook, the methods and assumptions for the allocation of expenses do not totally conform with SAMICS standards. The procedures used, however, were identical to those used by Honeywell costing experts for comparably-sized factory operations. The basic ground rules for the model are outlined next.

JUNE 14, 1977

HONEYWELL CORPORATE RESEARCH CENTER COST ANALYSIS FOR COATING SILICON ON CERAMIC. LATEST REVISION APRIL 7, 1977.

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE FOLLOWING INPUT DATA:

OCTUPLE COATING UNITS	100000.	$ EACH
POLY SI	10.00	$/KGM
CERAMIC	2.00	$/SQ M
ARGON	4.00	$/100 CU FT
PULLING RATE	1.00	CM/SEC
SHEET WIDTH	30.00	CM
SI THICKNESS	100.	MICRONS
SUBSTRATE THICKNESS	0.50	CM
ELECTRIC RATE	4.00	CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 9

COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.011	
PRODUCTION EQUIPMENT	0.066	
PLANT EQUIPMENT	0.004	
		0.081
DIRECT LABOR		
PRODUCTION	1.106	
PRODUCTION ENGINEERING	0.028	
INSPECTION	0.025	
		1.160
BURDEN OVERHEAD		1.433
DIRECT MATERIALS		
SILICON	2.912	
CERAMIC	2.500	
CARBON	0.264	
ARGON	0.392	
		6.069
ELECTRIC POWER		0.253
FACTORY COST (SUBTOTAL)		8.995
GEN. & ADM.		1.619
TOTAL COST		10.614
PROFIT		1.592
PRICE		12.206
ADDED VALUE		9.294

FIGURES LISTED BELOW GIVE THE PERCENT INCREASE (DECREASE) IN PRICE AND ADDED VALUE, WHICH WOULD BE THE RESULT OF INCREASING EACH OF THE INPUT VALUES 1% WHILE MAINTAINING ALL THE OTHER VALUES FIXED. FIRST COLUMN GIVES THE % CHANGE IN PRICE AND SECOND COLUMN GIVES THE % CHANGE IN ADDED VALUE.

OCTUPLE COATING UNIT PRICE	0.003	0.004
POLY SI PRICE	0.324	0.112
CERAMIC PRICE	0.278	0.365
ARGON PRICE	0.044	0.057
PULLING RATE	-0.110	-0.145
SHEET WIDTH	-0.065	-0.086
SILICON THICKNESS	0.325	0.413
SUBSTRATE THICKNESS	0.026	0.034
ELECTRIC RATE	0.028	0.037

Figure 45. Economic Analysis for Growth Rate of 1.0 cm/sec.

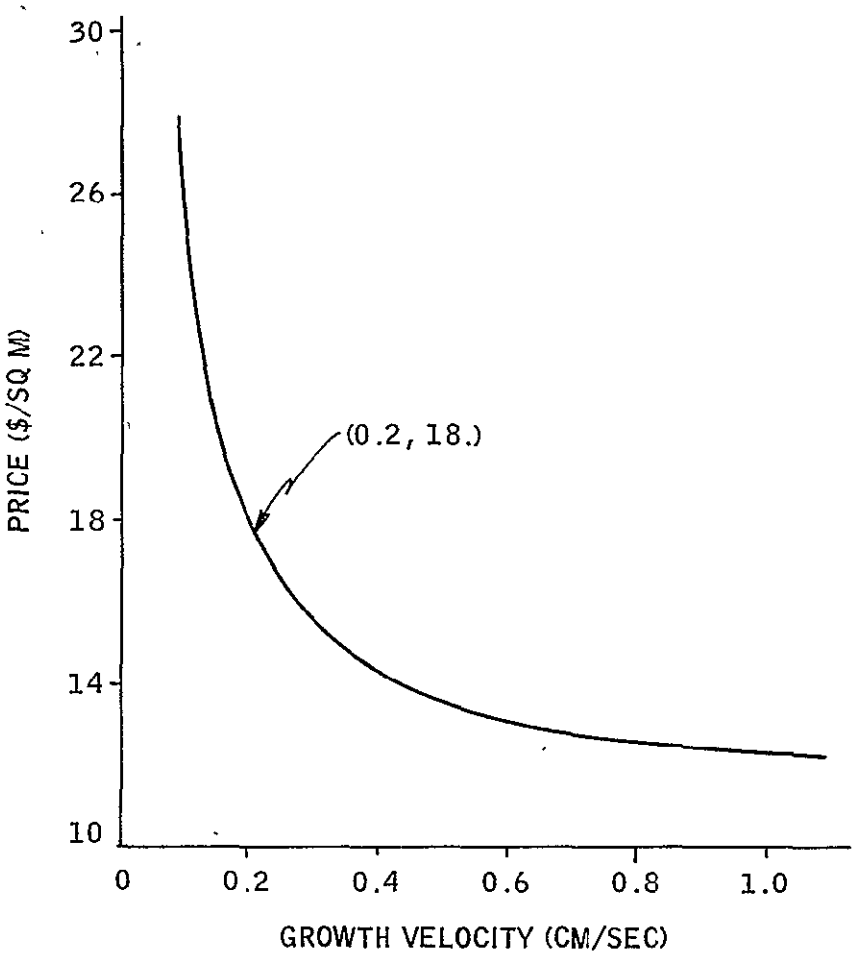


Figure 46. Price Versus Growth Velocity.

Because many costs do not scale exactly with the factory size as measured by the number of production units, a separate detailed cost analysis was performed by Honeywell experts for two factories representing supposed opposite ends of the spectrum. In each case, the total annual production was assumed to be five million square meters per year, but the linear pulling rates were respectively 1.0 and 0.1 cm/sec, representing the most optimistic and most pessimistic conditions. Production units required to meet the annual quota were respectively nine and 92. Detailed estimates of direct and indirect labor were itemized for each factory, as well as burden allocations, materials, and capital expenditures.

Since the economic model is supposed to be valid for any pulling rate between these extremes, a linear interpretation in terms of production units is employed. For example, let A_o be the required factory floor area assuming a pulling rate of 1.0 cm/sec (9 machines), and A_1 the area required for 0.1 cm/sec (92 machines). The area computation for an intermediate speed r, $0.1 \leq r \leq 1.0$, proceeds as follows:

$$\text{Number of machines } M = 9.2/r$$

$$\text{Area } A = A_o + \frac{M-9}{92-9}(A_1 - A_o)$$

The second computer printout (Figure 47) represents the slow pulling rate, with the other parameters unchanged. A comparison of the two printouts summarizes the cost analysis for the two extreme cases, where the figures have been reduced to dollars per square meter.

JUNE 14, 1977

HONEYWELL CORPORATE RESEARCH CENTER COST ANALYSIS FOR COATING SILICON ON CERAMIC. LATEST REVISION APRIL 7, 1977.

THIS ANALYSIS ASSUMES AN ANNUAL PRODUCTION OF 5.0 MILLION SQUARE METERS OF SI-COATED CERAMIC AND IS BASED ON THE FOLLOWING INPUT DATA:

OCTUPLE COATING UNITS ,	100000.	$ EACH
POLY SI	10.00	$/KGM
CERAMIC	2.00	$/SQ M
ARGON	4.00	$/100 CU FT
PULLING RATE	0.10	CM/SEC
SHEET WIDTH	30.00	CM
SI THICKNESS	100.	MICRONS
SUBSTRATE THICKNESS	0.50	CM
ELECTRIC RATE	4.00	CENTS/KWH

NUMBER OF COATING UNITS REQUIRED IS 92
COST BREAKDOWN IN DOLLARS/SQ M:

CAPITAL INSTALLATION		
BUILDING	0.066	
PRODUCTION EQUIPMENT	0.350	
PLANT EQUIPMENT	0.034	
		0.451
DIRECT LABOR		
PRODUCTION	3.042	
PRODUCTION ENGINEERING	0.061	
INSPECTION	0.053	
		3.155
BURDEN OVERHEAD		5.138
DIRECT MATERIALS		
SILICON	2.912	
CERAMIC	2.500	
CARBON	0.264	
ARGON	3.924	
		9.600
ELECTRIC POWER		0.353
FACTORY COST (SUBTOTAL)		18.698
GEN. & ADM.		3.366
TOTAL COST		22.063
PROFIT		3.309
PRICE		25.373
ADDED VALUE		22.460

FIGURES LISTED BELOW GIVE THE PERCENT INCREASE (DECREASE) IN PRICE AND ADDED VALUE, WHICH WOULD BE THE RESULT OF INCREASING EACH OF THE INPUT VALUES 1% WHILE MAINTAINING ALL THE OTHER VALUES FIXED. FIRST COLUMN GIVES THE % CHANGE IN PRICE AND SECOND COLUMN GIVES THE % CHANGE IN ADDED VALUE.

OCTUPLE COATING UNIT PRICE	0.015	0.017
POLY SI PRICE	0.156	0.046
CERAMIC PRICE	0.134	0.151
ARGON PRICE	0.210	0.237
PULLING RATE	-0.623	-0.704
SHEET WIDTH	-0.407	-0.460
SILICON THICKNESS	0.156	0.047
SUBSTRATE THICKNESS	0.012	0.014
ELECTRIC RATE	0.019	0.021

Figure 47. Economic Analysis for Growth Rate of 0.1 cm/sec.

PROCESSING EFFORTS

The following processing efforts were performed during this reporting period:

- Two types of processes were investigated for fabricating 10 cm x 100 cm mullite substrates.
- A process was developed for making narrow slots in the substrate prior to firing the substrate.
- A process was tried for producing ceramic substrates with an inherent carbon coating by firing the ceramic in an inert atmosphere.
- A process was tried for producing ceramic substrates with a carbon coating by embedding graphite particles in the surface of the mullite clay and firing in an inert atmosphere.
- A process was tried for producing ceramic substrates with a carbon coating by mixing graphite particles throughout the mullite clay and firing in an inert atmosphere.
- A process was tried for producing ceramic substrates with a silicon carbide coating by embedding silicon carbide particles in the surface of the clay and firing in an inert atmosphere.
- A process was tried for producing ceramic substrates with a carbon coating by mixing silicon carbide throughout the mullite clay and firing in an inert atmosphere.
- A process for carbonization of the ceramic by using colloidal carbon suspensions (Dag) is being implemented. Such coatings can be applied using an airbrush.
- Dag-borosilicate graphite coatings on the substrate were also tried to investigate whether or not the carbon layer would enhance the electrical contact between the silicon and graphite coating by boron doping the silicon carbide (SiC) at the Si-SiC interface.
- A process was investigated for applying carbon coatings to the substrate by plasma decomposition of propane gas in an R. F. sputtering apparatus.

- The gas used for the silicon coating environment has been changed from Ar to He or a He + 10 %H_2 mixture.
- A process for seeding the grain growth of the silicon coating is being developed by attaching single-crystal seeds to the ceramic substrate.
- A process for applying the silicon in various patterns as determined by the carbon coating is being investigated.
- A gas jet has been installed inside the coating chamber of the dip coater to increase the temperature gradient above the melt and increase growth rates.
- A coating facility was designed and constructed for the purpose of silicon coating 10-cm x 100-cm substrates in a continuous manner.
- A process was developed for fabricating 1-cm^2 and 10-cm^2 area solar cells plus various small-diode configurations for material evaluation purposes.
- A process was developed for applying sputtered PtSi contacts to solar cells.
- Liquid spin on, spray and dip coating diffusion sources were tried with varying degrees of success.
- A solar cell checker was constructed where by using a ramp generator an I-V characteristic is automatically swept out and the signals applied to an X-Y recorder.
- Electron beam-induced current (EBIC) and a light beam-induced current (LBIC) scanning processes were developed for measuring the base region minority carrier diffusion length and for evaluating crystalline imperfections in the silicon coatings.

PROJECTION OF FUTURE ACTIVITIES

Work will continue in characterization of substrates with respect to the distribution of impurities between the glassy and crystalline phases, and measurement of mechanical properties. The coating properties will be investigated as a function of substrate thickness.

The adhesion of the silicon coating to the substrate will be measured as a function of carbon coating type and such substrate properties as porosity and glass content. The residual stress state in the silicon coating as a function of dipping parameters will also be measured.

Work will also continue on the development of large-area (100-cm X 10-cm) substrates and a superior method will be developed for adding uniform slots to the mullite substrate prior to firing it.

During the next six months one primary concern will be to increase the silicon coating growth rate without sacrificing its quality. This will be done by further experimentation involving changes in, and control of, the temperature gradient above the melt. Additional types of cooling jets and heat sinks will be tried.

Further studies will be done on the seeding of the silicon coating to promote large-grain or single-crystal growth.

Solidification studies of horizontal films of silicon will be conducted by contacting the surface of the melt with substrates held horizontally. These experiments should provide valuable information for the silicon coating by inverse meniscus (SCIM) technique. In parallel with this effort, the continuous-coating facility will be in operation also investigating growth parameters associated with the SCIM method.

Slotted substrates will be coated to establish the feasibility of using this design to make back contact to the silicon. The potential of this concept will be evaluated theoretically as well as experimentally.

The study of substrate carbon coatings will continue with the goal of defining a carbon coating method which will serve to enhance the sheet resistance of the base layer. It also must provide good wetting for the silicon coating and prevent dissolution of the melt. Among other things, doped colloidal carbon suspensions (Dag) will continue to be evaluated. Ultimately, in the interest of improved electrical base layer conduction, it would be desirable to develop a cost-effective coating technique which would permit a metallic film on the substrate beneath the carbon coating. Such a coating, however, must be insoluble and isolate the molten silicon from the metallic film.

Phosphine will be used as a diffusion source rather than P_2O_5. In addition to the $1cm^2$ and $10cm^2$ evaluation solar cells, $2 \times 2cm^2$ cells will also be fabricated and antireflection (AR) coatings of SiO will be applied to the solar cells.

Crystalline imperfection studies will continue relating light beam scans of photodiodes to lifetime as determined by open-circuit voltage decay.

Solar cell modeling will continue and include the effects of such parameters as back surface field and variations in L_n on projected solar cell performance.

A new solar cell geometry will be investigated using a stripe configuration and an integral optical collector.

NEW TECHNOLOGY

A surprising result of our measurements of the silicon-vitreous carbon interface is that the electrical resistance between the two can be quite low if the contact time is sufficiently short. Since the vitreous carbon coatings can have quite low sheet resistance (2 to 5 ohms/□), they could contribute significantly to the reduction of series resistance. Carbon is basically a low-cost material and could thus provide a cost-effective means of contacting the silicon.

The uniformity of the contact is certainly a problem, even when the contact time is kept low. Further effort is needed to isolate the reasons for the variations and to minimize them.

SUMMARY OF ANALYSIS AND CHARACTERIZATION DATA

The analysis and characterization data is given above in detail in the appropriate section of the report. These analyses are summarized in the following brief statements:

- The mullite-based refractory can be economically produced by firing naturally occurring clays and other minerals and it has good high-temperature properties and thermal shock resistance.
- The major impurities in mullite which affect solar cell performance are Ti, V and Fe. When the substrate has limited contact with the silicon melt the effect of these impurities on cell performance is apparently not serious.

- The experimental mullite substrates tried have a porosity which promotes good adhesion of the silicon coating.
- The strongest mullite samples examined were those containing lowest amounts of excess silica and those fired in a reducing atmosphere.
- Both strength and thermal expansion affect the thermal shock resistance.
- Acid leaching of the mullite lowers the surface impurity content, but also weakens the substrate.
- The thermal expansion of mullite exceeds that of silicon, hence the silicon coatings are in a state of compression.
- Initial efforts to increase the silicon coating growth rate by directing a gas jet on the substrate were only partially successful since the jet also caused the surface of the melt to solidify.
- The SOC coatings are predominately {331} surfaces with a growth direction of <211>. This texture permits {111} twin planes to occur perpendicular to the substrate and propagate as the grain grows. This texture is similar to that observed in EFG ribbon silicon.[5]
- Initial seeding experiments show promise. The seed-film junction is continuous, indicating that with a suitably oriented seed, large grain growth may be induced.
- It was observed that while the dislocation count from a silicon coating surface was as high as $9 \times 10^6 cm^{-2}$, that certain areas between twin boundaries are dislocation free.
- Tylan Corporation's "Vigre Graf" coated substrates produce higher-purity silicon coatings by inhibiting the dissolution of mullite in molten silicon.
- All substrate carbonizing methods tried, where the carbon was smooth and uniform with a suitable thickness and purity, promoted a good silicon coating on the substrate.
- To date chemical analyses techniques have not revealed any impurity segregation at grain boundaries.
- Electrical contact studies revealed that lack of low contact resistance to the base region of the initial solar cells fabricated was a reason for their poorer performance.

- EBIC measurements reveal that reasonably good cell performance can be achieved in spite of poor crystalline structure.
- Short wavelength light-beam scans across a diode give a uniform response whereas long wavelengths, because of their absorption depth, show non-uniform response due to variations in the diffusion length that occurs, especially in the vicinity of grain boundaries.
- A phosphorus gettering process has yielded improved efficiency in an SOC solar cell, but due to the statistical spread in the results, it is not clear that it was a factor in the diode performance.
- The proposed concept of using slotted substrates to contact the cell's base region leads to an appreciable series resistance unless the slots are made electrically conductive and the base region has high conductivity.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 48, 49, and 50.

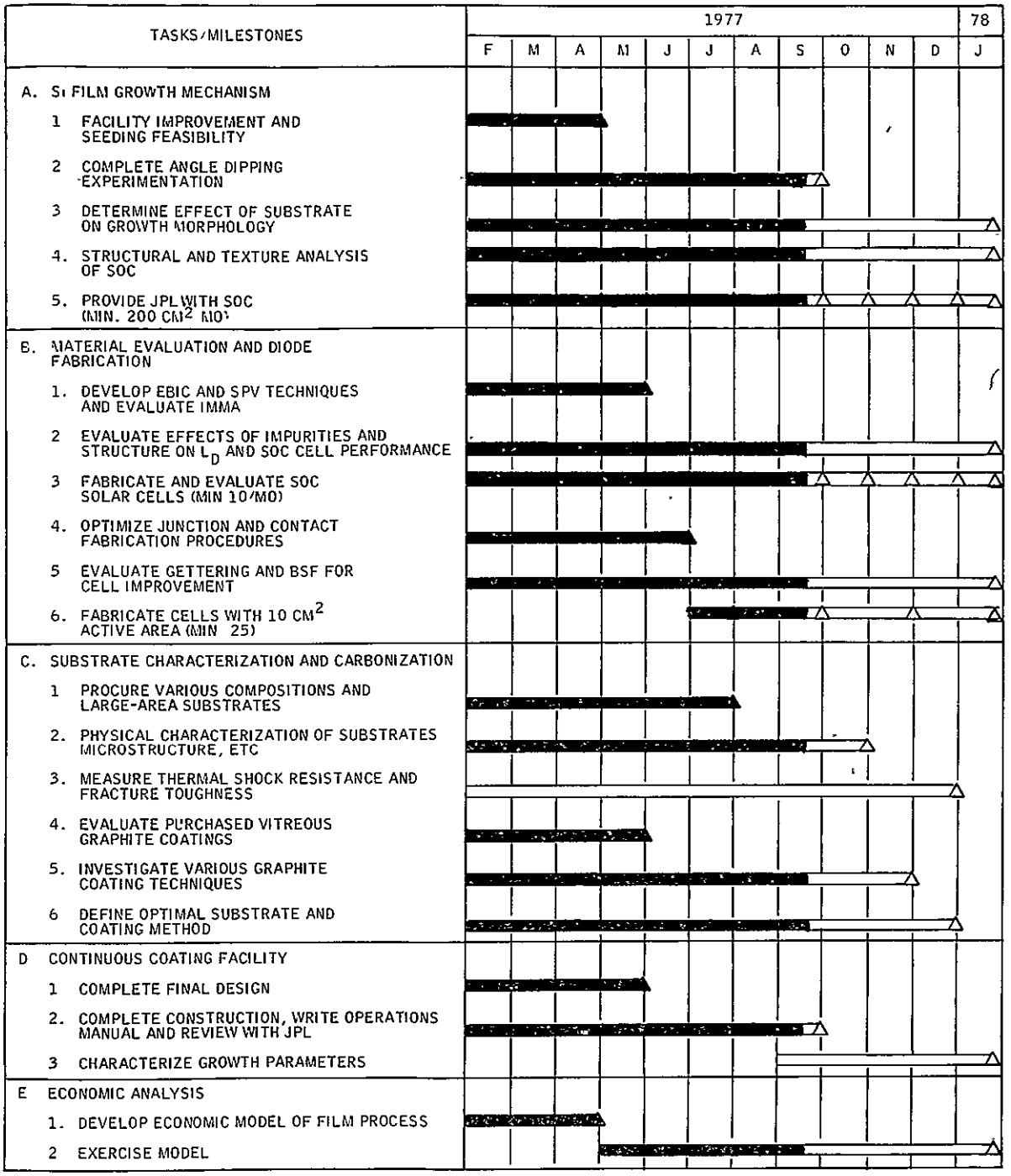


Figure 48. Updated program plan

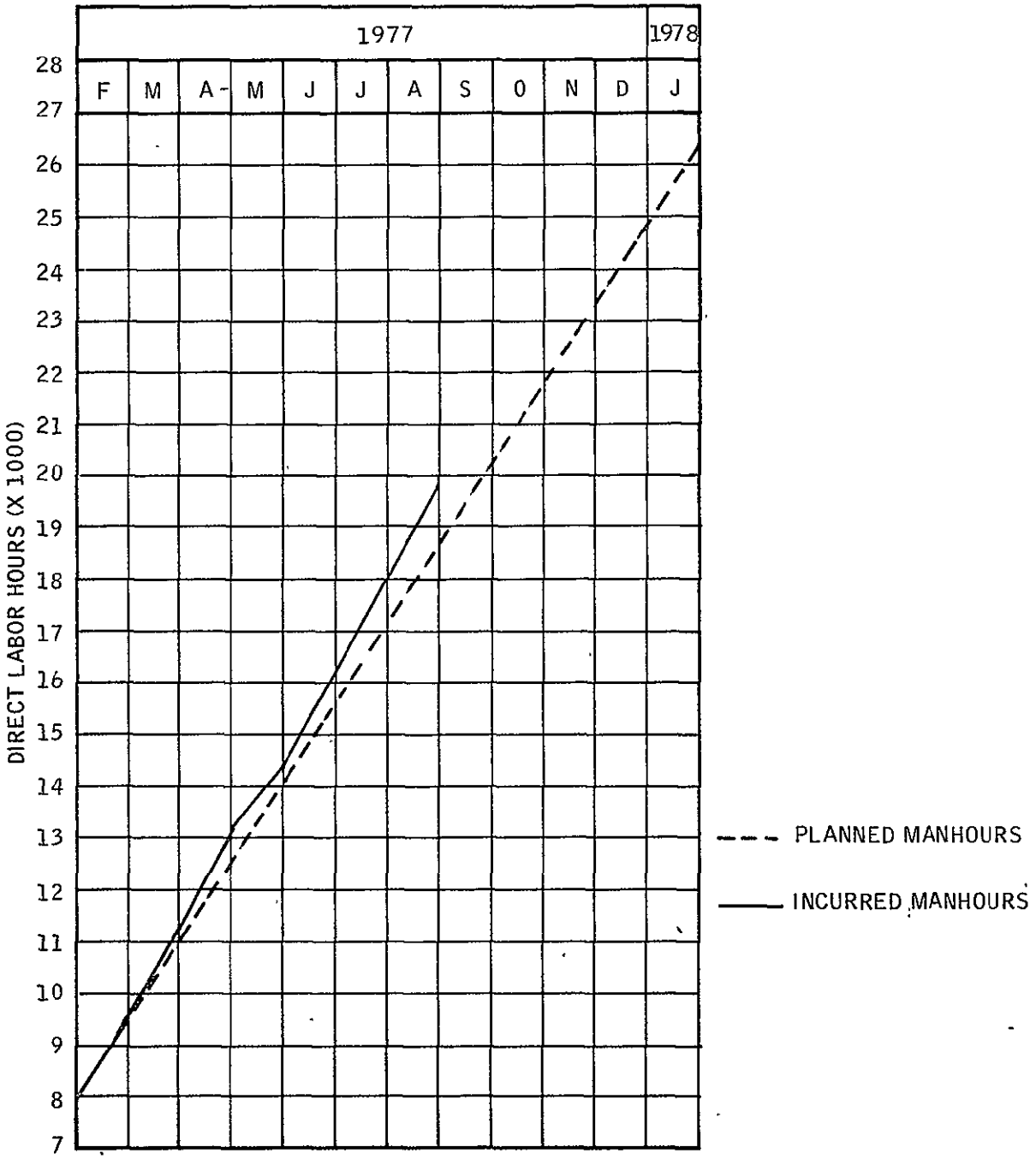


Figure 49. Updated program labor summary

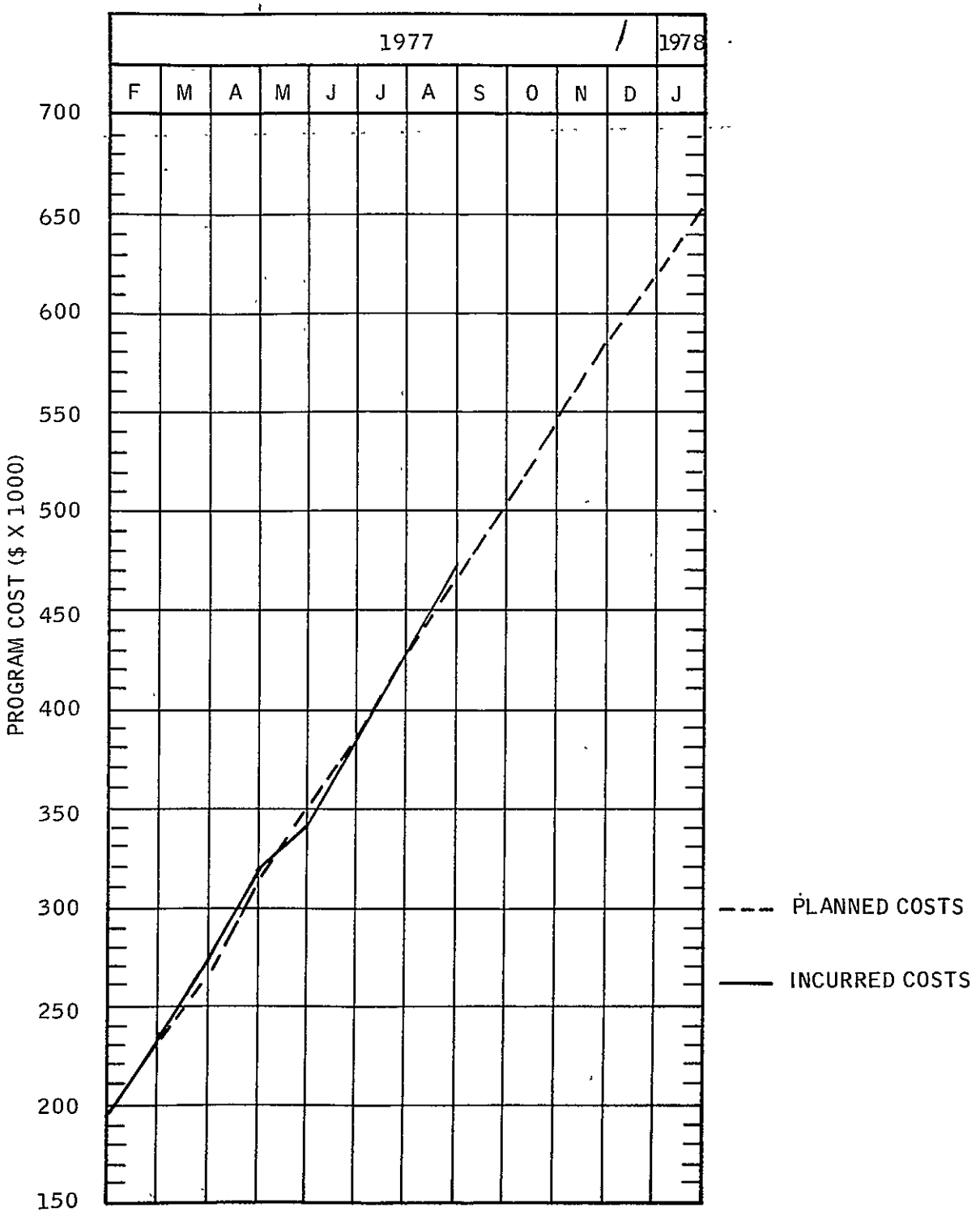


Figure 50. Updated program cost summary

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APPENDIX A

HARMONIC ANALYSIS OF FRONT STRUCTURE (S. B. Schuldt)

The purpose of this analysis is to justify the approximations for the planar contact resistances. The approach will be to derive the electric potential distribution in the volume bounded by the front surface (y = 0), the junction (y = -h), and electrode centers (x = 0 and x = b) as shown in Figure A1. The primes are omitted to simplify notation.

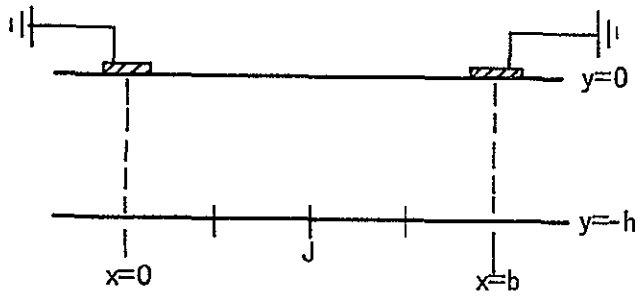

Figure A1. Portion of Diffused Region. (Primes omitted.)

From the potential distribution, the series resistance is readily obtained.

A uniform current density J is assumed across the junction. Appendix B considers nonuniform J resulting from large IR drops in the diffused layer. The metal electrode surfaces are assumed to be at ground potential, but there is a potential drop across the metal-semiconductor interface due to the finite specific contact resistivity ρ_c.

The potential distribution satisfies the two-dimensional Laplace equation

$$\Delta V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0, \tag{A1}$$

subject to

$$\partial V/\partial y\ (x, -h) = -\rho_B J \tag{A2}$$

$$\partial V/\partial x\ (0, y) = \partial V/\partial x\ (b/2, y) = \partial V/\partial x\ (b, y) = 0 \tag{A3}$$

$$-\frac{1}{\rho_B}\partial V/\partial y\,(x,\,0) = \begin{cases} \frac{1}{\rho_c} V(x,\,0) & 0 \le x < d/2 \text{ and } b - d/2 < x \le b \quad \text{(A4a)} \\ 0 & d/2 < x < b - d/2 \quad \text{(A4b)} \end{cases}$$

Condition (A2) is an expression of Ohms law at the junction; (A3) follows from the periodicity and symmetry of the structure. (A4a) and (A4b) express current continuity at the surface $y = 0$. The left hand side is the normal component of current density just below the surface, and the right hand side gives the same quantity just above the surface: in (A4a) this is the electrode current density; in (A4b) it is zero because between electrodes the surface is in contact with an insulator (air).

If the solution is written in the form

$$V(x, y) = h\rho_B J \{ y/h + a_o + \sum_{n-1}^{\infty} a_n \cos \lambda_n x \cdot \cosh \lambda_n (h+y) \} \quad \text{(A5)}$$

with $\lambda_n = 2\pi n/b$, then (A1), (A2), and (A3) are satisfied. It remains to determine the Fourier coefficients $a_o, \ldots . a_n, \ldots .$ so that (A4a) and (A4b) are satisfied. This gives rise to an infinite system of algebraic equations in the a_n's.

Let $\eta = \rho_c/h\rho_B$ and $A_n = a_n \cosh \lambda_n h$, $n = 0, \ldots$ Also let $\sin ax/x = a$ when $x = 0$. Then the a_n's must satisfy the system (A6) and (A7):

$$\sum_{n=0}^{\infty} A_n \frac{\sin \lambda n\, d/2}{n} = -\pi \eta \quad \text{(A6)}$$

$$\sum_{n=0}^{\infty} A_n \left[\frac{\sin(\lambda m + \lambda n)\, d/2}{m+n} + \frac{\sin(\lambda m - \lambda n)\, d/2}{m-n}\right] = -\frac{2\pi^2 h}{b} \eta\, m A_m \tanh \lambda_m h \quad \text{(A7)}$$

$$m = 1, \ldots$$

Series resistance of the structure in Figure A1 is defined here as dissipated power divided by current squared:

$$R_C + R_L = \left| w \cdot \int_o^b JV(x, -h)dx \right| \Big/ (bwJ)^2 = \rho_B (1 - a_o)\, h/wb. \quad \text{(A8)}$$

This is to be compared numerically with the sum $R_C' + R_L'$ calculated from the lumped expressions given in the subsection on Parasitic Resistance Analysis, Components of Parasitic Resistance contained in Section II.

The required term $a_o = A_o$ is found by inverting a finite approximation of the system (A6) and (A7). A 71 x 71 approximation has been found to be adequate. Resistances $R_C + R_L$ by the two methods generally agree within a few percent. Table A1 shows comparisons for a few cases. For both methods, the normalized resistance is determined by the dimensionless quantities η, b/h, and d/h.

Table A1. Normalized Resistances Computed by Methods of Appendix A and Section II

			Calculated From:			
			Section II			Appendix A
η	b/h	d/h	$R_C w/\rho_B$	$R_L w/\rho_B$	Total	Total
1	100	1	8.09	1.20	9.29	9.41
1	100	5	7.14	.24	7.38	7.70
1	100	10	6.08	.12	6.20	6.56
1	50	1	3.92	1.20	5.12	5.26
1	50	5	3.04	.24	3.28	3.57
1	50	10	2.13	.12	2.25	2.55
.001	50	1	3.92	.20	4.12	4.14
.001	50	5	3.04	.04	3.08	3.17
.001	50	10	2.13	.02	2.15	2.25
10	50	1	3.92	10.2	14.12	14.27
10	50	2.5	3.57	4.08	7.65	7.89
10	50	5	3.04	2.04	5.08	5.44
10	50	10	2.13	1.02	3.15	3.64
200	10^4	10^3	607.5	.2	607.7	611.8

APPENDIX B

DISTRIBUTED CELL MODEL (S. B. Schuldt)

In the lumped approximation for R_L it was assumed that diode current density was uniform. If the IR drop through the base and diffused layers is taken into account, the diode voltage and thus current density vary with distance from the electrodes. In the limit of very large b, the diode voltage can approach cut-off so that portions of the cell near x = b/2 may contribute little or no current. Figure B1 represents diode voltage as a function of position for the case of equal front and back electrode separation (b' = b). Local current density is assumed given by the simple diode formula

$$J(x) = J_o - J_1 (e^{AV_D(x)} - 1), \tag{B1}$$

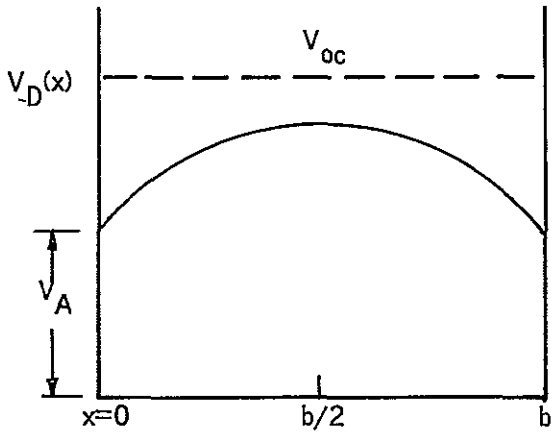

Figure B1. Nonuniform Diode Voltage.

and transverse current (positive from left to right) in the base layer is

$$I(x) = w\int_{b/2}^{x} J(z)dz \tag{B2}$$

so that

$$\frac{1}{w}\frac{dI}{dx} = J_o - J_1(e^{AV_D(x)}-1). \tag{B3}$$

An equal and opposite current flows in the diffuse layer. Hence diode voltage (Figure B1) follows the equation

$$\frac{dV_D}{dx} = - I(x) \cdot R_{\square}/w, \tag{B4}$$

where $R_{\square}$ is the total effective sheet resistance of the two layers.

Equations (B3) and (B4) combine to give

$$\frac{d^2V_D}{dx^2} + R_{\square} [J_o - J_1(e^{AV_D(x)} - 1)] . \tag{B5}$$

Boundary conditions are $V_D(0) = V_D(b) = V_A$, (V_A = load voltage), provided contact resistance is ignored. A second integral of (B5) is not available, so that some kind of numerical integration is necessary, using successive estimates of dV_D/dx (0) until both boundary conditions, or their equivalent, are satisfied. Then the output current I_A is determined from (B4) as

$$I_A = 2 \mid I(0) \mid = (2w/R_{\square}) \cdot dV_D/dx(0). \tag{B6}$$

Given the load voltage V_A, $0 \leq V_A \leq V_{oc}$, the load current can therefore be found, by a procedure which is considerably more laborious than the one outlined in Section II for the lumped resistance model. The I-V characteristic, and in particular the maximum power point, may differ significantly from the lumped resistance model. (See Figure B2.) However the maximum power densities (JV products) according to the two models are remardably close, over a wide range of $R_{\square}$ and b, as demonstrated in Figure B3. This agreement is the principal justification for the lumped resistance model.

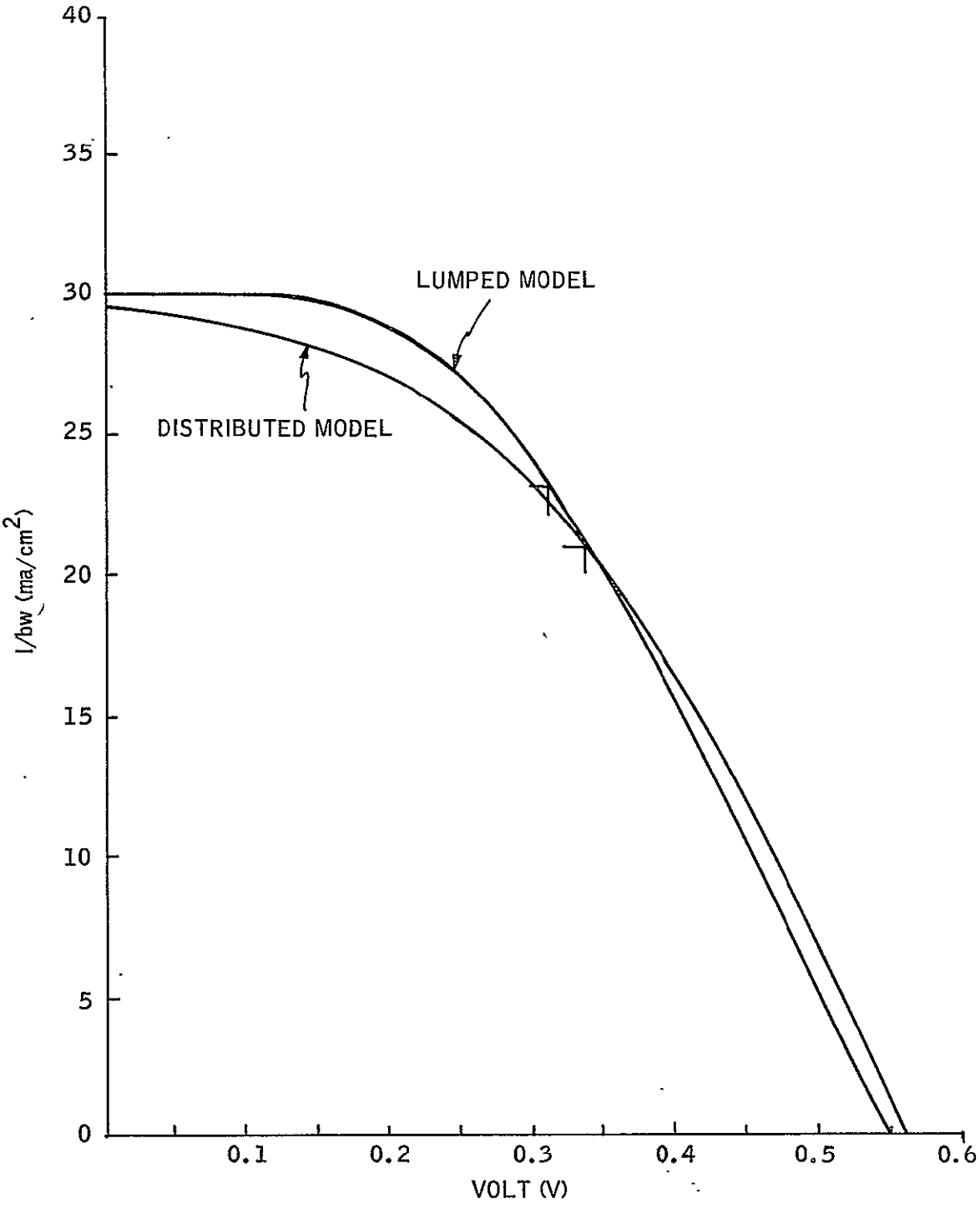

Figure B2. I-V Characteristic for Lumped and Distributed Models. $R_{\square}$ = 100 ohms/□ and b = 1.0 cm. Maximum power points are indicated.

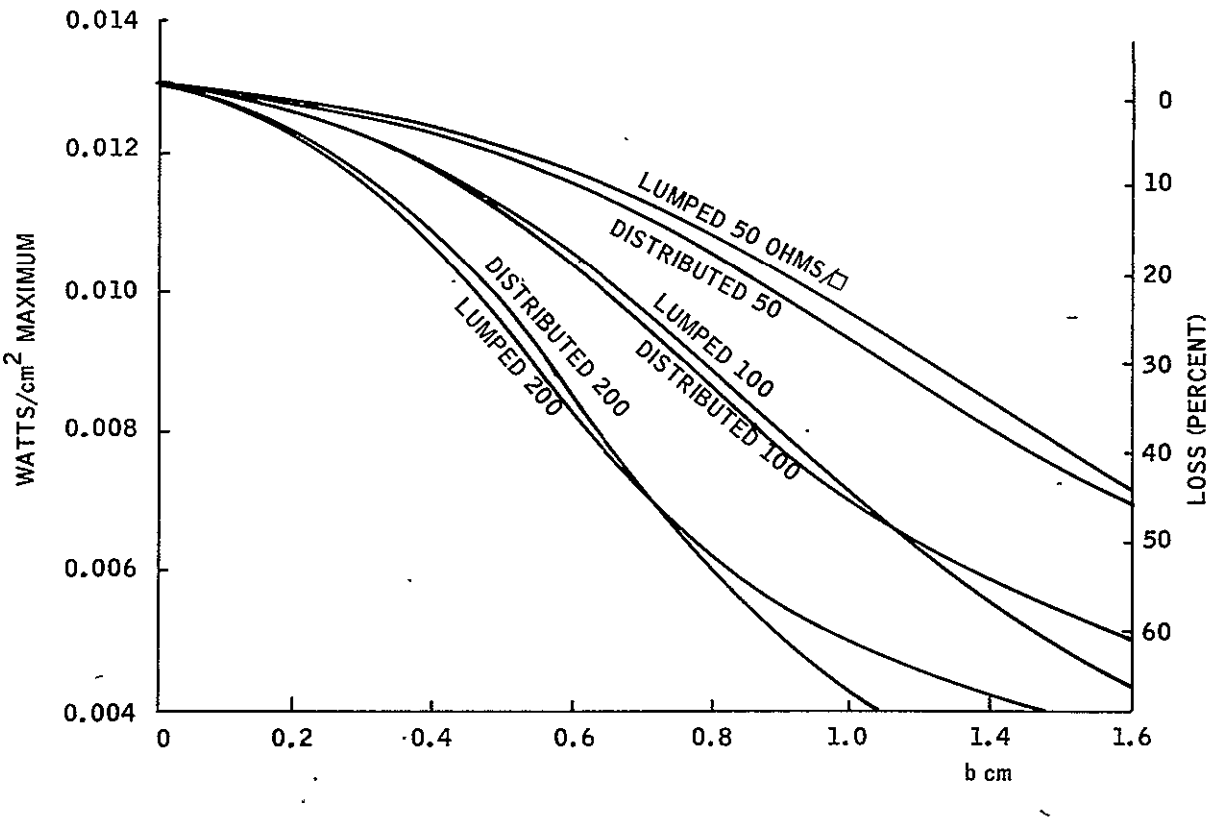

Figure B3. Maximum Power Densities as a Function of Contact Spacing, According to Lumped and Distributed Models. Total effective sheet resistance 50, 100, and 200 ohms/□. J_o = .030 amp/cm^2, A = 30 volt^{-1}, V_{oc} = .55 volt. Contact resistance omitted.

APPENDIX C

SHEET RESISTANCE REDUCTION BY
CONTACTING CARBON FILM (S. B. Schuldt)

One of the conclusions of the body of the report was that the base layer resistance would be a potential problem with the SOC approach. The shunting effect of the carbon layer on the ceramic could alleviate the problem if there is adequate ohmic contact between silicon and carbon. This effect can be estimated if the carbon sheet resistance and specific contact resistivity are known. A distributed model is used to derive current and voltage profiles in the two layers (Figure C1). Contact resistivity is ρ_{BV} ohm cm^2, and the silicon and carbon sheet resistances are $R_{\square B}$ and $R_{\square V}$ respectively. Constant diode current density J is assumed.

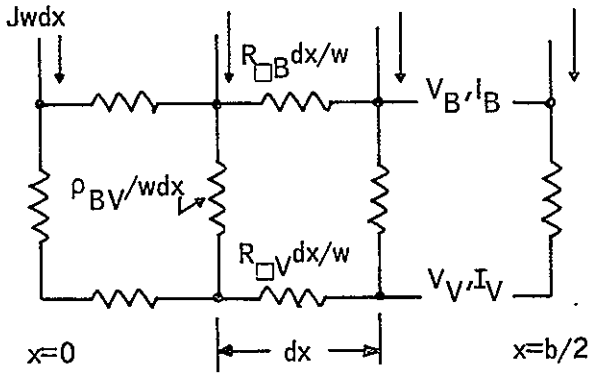

Figure C1. Distributed Resistance in and Between Silicon and Carbon Layers.

By applying Ohm's and Kirchoff's laws, we find that voltage and current in the base layer locally satisfy

$$d V_B/dx = R_{\square B} I_B/w \qquad \text{(C1)}$$

$$\frac{1}{w} dI_B/dx = -J + (V_B - V_V) / \rho_{BV} \qquad \text{(C2)}$$

Similarly in the carbon layer,

$$dV_V/dx = R_{\square V} I_V/w \tag{C3}$$

$$\frac{1}{w}\, dI_V/dx = -(V_B - V_V)/\rho_{BV}. \tag{C4}$$

When current is eliminated from Equations (C1) - (C4), one obtains a second order equation in the voltage difference $\Delta V(x) = V_B(x) - V_V(x)$:

$$d^2\Delta V/dx^2 = -R_{\square B} J + [(R_{\square B} + R_{\square V})/\rho_{BV}]\, \Delta V. \tag{C5}$$

It is unlikely that the carbon layer will carry current directly to the electrode. Hence at x = 0 all current is in the base layer:

$$I_B(0) = bwJ/2 \tag{C6}$$

$$I_V(0) = 0. \tag{C7}$$

The relevant boundary condition is therefore (from (C1) and (C3))

$$d\Delta V/dx(0) = R_{\square B} bJ/2. \tag{C8}$$

Also since $I_B(b/2) = I_V(b/2) = 0$ by symmetry,

$$d\Delta V/dx\,(b/2) = 0. \tag{C9}$$

According to (C8) and C9), the solution of (C5) is

$$\Delta V(x) = \rho_{BV} J R_{\square B}/(R_{\square B} + R_{\square V})$$

$$+ (R_{\square B} Jb/2\alpha)\,[\sinh \alpha x - (\coth \alpha\, b/2) \cosh \alpha x] \tag{C10}$$

where

$$\alpha = [R_{\square B} + R_{\square V})/\rho_{BV}]^{1/2}.$$

The effective series resistance is equal to the average base IR divided by the total current I = Jwb:

$$R = \overline{V_R}/Jwb \tag{C11}$$

$V_B(x)$ is obtained from V(x) by successively integrating (C2) and (C1):

$$I_B(x) = wJ(b/2-x) + w/\rho_{BV}\int_{b/2}^{x}\Delta V(x')\,dx' \tag{C12}$$

$$V_B(x) = R_{\square B}/w \int_0^x I_B(x')\,dx' \tag{C13}$$

$$V_B(x) = R_{\square B}R_{\square V}J/(R_{\square B}+R_{\square V}) \cdot \{ (bx-x^2)/2 + (R_{\square B}\rho_{BV}/R_{\square V}) \left[\frac{\sinh\alpha x}{\alpha} - \coth\frac{\alpha b}{2}\,\frac{\cosh\alpha x-1}{\alpha}\right]\}. \tag{C14}$$

Finally,

$$R = (b/12w)\left\{\frac{R_{\square B}R_{\square V}}{R_{\square B}+R_{\square V}}\left[1+3\frac{R_{\square B}}{R_{\square V}}\,\frac{\beta\coth\beta-1}{\beta^2}\right]\right\}$$

where $\beta = [(R_{\square B}+R_{\square V})/\rho_{BV}]^{1/2}\alpha/2 = \alpha b/2$ (C15)

The quantity in curly brackets is an effective sheet resistance which ranges from $R_{\square B}$ when $\beta << 1$, to $R_{\square B}R_{\square V}/(R_{\square B}+R_{\square V})$ when $\beta >> 1$.

Note that the latter value corresponds to the two sheets in electrical parallel. The dependence of effective sheet resistance upon β is shown in Figure C2.

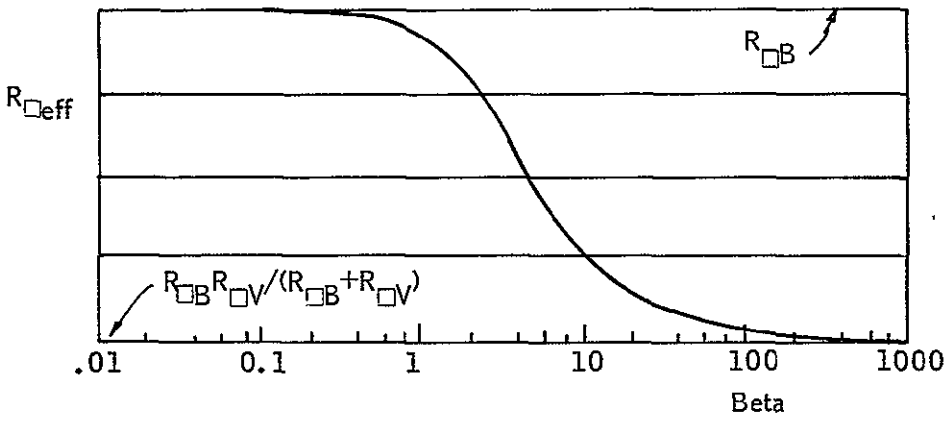

Figure C2. Effective Sheet Resistance vs Beta from Equation (C15).

APPENDIX D

RESISTANCE OF ELECTRODE FINS (S. B. Schuldt)

One half of an electrode fin plus part of the base layer is modeled as a right-angled structure as shown in cross-section in Figure D1.

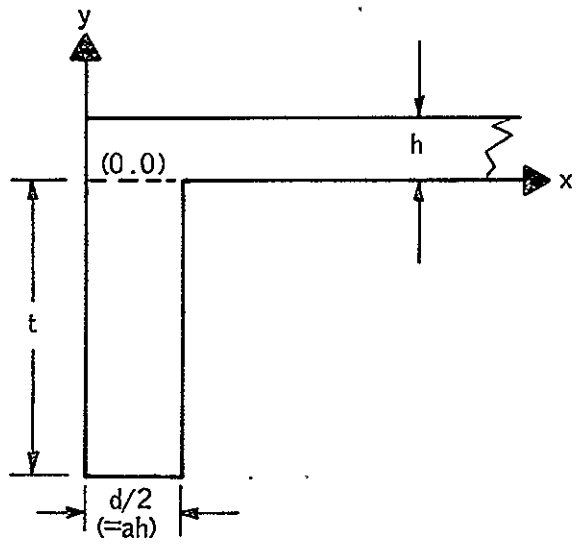

Figure D1. Back Structure for Electrode Resistance Calculation.

If the current per unit width I is assumed constant (i. e., ignoring the distributed nature of its source) the resistance of this structure is

$$R = (R_{\square B}/w)[\, x + \frac{t}{a} + f\,(h, a)] \qquad \text{(D1)}$$

where a = d/2h and f is a function to be determined. The first term is the resistance of a portion of the base layer x units long. The second term will be recognized as twice the resistance of the silicon portion of the back electrodes, according to the earlier approximation. (The solar cell unit contains two half-electrodes in electrical parallel of which only one is considered here; hence the factor 2). The third term is a correction to account for current distortion near the corner. This will be calculated using a Schwarz-Christophel transformation.

We first do a simple translation and rotation

$$z = x + iy = i\,(h - z') \tag{D2}$$

and allow the ends to extend toward infinity in the positive x' and y' directions, as in Figure D2.

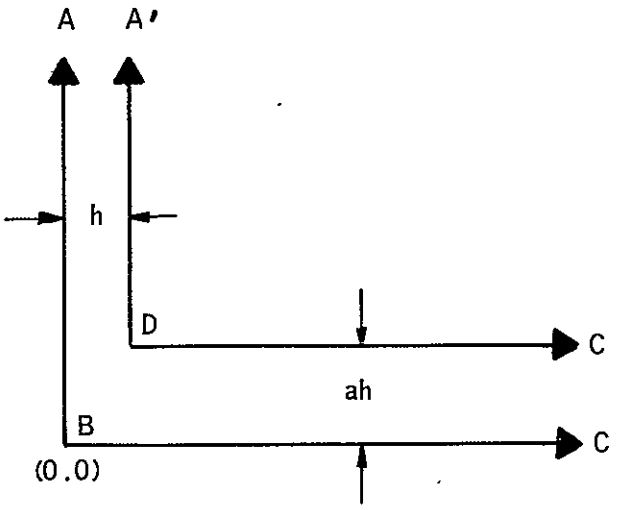

Figure D2. Linear Transformation and Extension of Back Structure into z'-plane.

The current source and sink are at $y' = \infty$ and $x' = \infty$, respectively. Next the transformation

$$z' = \frac{h}{\pi}\left[\cos^{-1}\frac{e-2w}{e} + \sqrt{e-1}\,\cosh^{-1}\frac{ew + e - 2w}{(1-w)\,e}\right] \tag{D3}$$

$$e = a^2 + 1, \quad w = u + iv$$

maps the elbow in Figure D2 into the upper half-plane $v \geq 0$ with the current sink C at $w = (1, 0)$ (Figure D3).

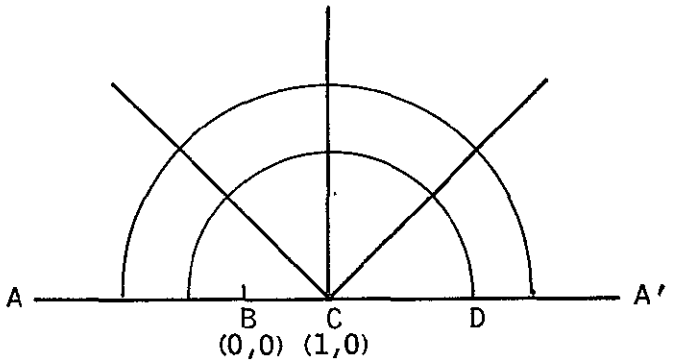

Figure D3. Radial Current Streamlines in w-plane.

The source is now distributed over the half-circle AA' at infinity, and current streamlines are the radii converging to the point C. Note that current is tangent to the line ABCDA', as it must be since this is the transformed boundary of the elbow in Figure D2. The electric potential satisfying these conditions is

$$V(w) = \frac{I\rho_B}{\pi} \ell n \mid w - 1 \mid . \qquad \text{(D4)}$$

Upon applying the reverse transformations to (D4) and evaluating V(z) at points far out on the respective link of the elbow, we find

$$\Delta V = \lim_{x \to \infty} V(x, 0) - \lim_{y \to \infty} V(0, -y)$$

$$\Delta V = \frac{I\rho_B}{h} \left[x + \mid y/a \mid - \frac{a^2-1}{a} h - \frac{2h}{\pi} \ell n \frac{4a}{a^2+1} + \frac{h(a^2-1)}{\pi a} \cos^{-1} \frac{a^2-1}{a^2+1} \right] . \qquad \text{(D5)}$$

Dividing by the total current Iw and setting $\mid y \mid = t$, we obtain

$$R = (R_{\square B}/w) \left[x + \frac{t}{a} + f(h, a) \right] \qquad \text{(D1)}$$

$$\text{with } f(h, a) = - \frac{a^2-1}{a} h - \frac{2h}{\pi} \ell n \frac{4a}{a^2+1} + \frac{h(a^2-1)}{\pi a} \cos^{-1} \frac{a^2-1}{a^2+1} \qquad \text{(D6)}$$

Our primary interest is in whether f (h, a) is negligible compared to t/a. Suppose t = .3 cm, d = 2 ah - .03 cm, h = .0125 cm. Then t/a = 0.25 cm and f (h, a) = - 0.008 cm, so that we are justified in omitting the correction terms.