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PRELIMINARY DESIGN FOR A STANDARD 10^7 BIT
SOLID STATE MEMORY (SSM)

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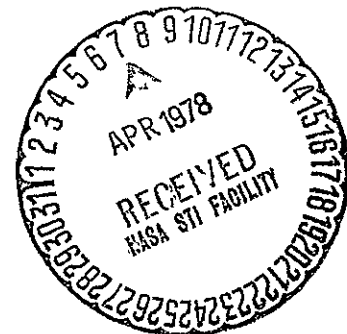


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PRELIMINARY DESIGN FOR A STANDARD 10^7 BIT

SOLID STATE MEMORY (SSM)

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SUMMARY

A preliminary design is presented for a Standard 10^7 Bit Solid State Memory (SSM). The design satisfies a set of requirements developed jointly by NASA and the Air Force and is based on bubble domain technology. The design employs a modular concept with three separate modules roughly separating bubble domain technology, control logic technology, and power supply technology. These modules are respectively the Standard Memory Module (SMM), the Data Control Unit (DCU), and the Power Supply Module (PSM). The storage medium is provided by bubble domain chips organized into memory cells. These cells and the circuitry for parallel data access to the cells make up the SMM. The DCU provides a flexible serial data interface to the SMM. The PSM provides adequate power to enable one DCU and one SMM to operate simultaneously at the maximum data rate. The SSM is designed to handle asynchronous data rates from dc to 1.024 Mbs with a bit error rate less than 1 error in 10^8 bits. Two versions of the SSM, a Serial Data Memory (SDM) and a Dual Parallel Data Memory (DPDM), are specified using the standard modules. The SDM and DPDM are expected to weigh 8.6 kilograms (19 pounds) and 10.8 kilograms (24 pounds) respectively and have a volume of 6230 cc (380 in.³) and 7050 cc (430 in.³) respectively. The SSM specification

includes requirements for radiation hardness, temperature and mechanical environments, dc magnetic field emission and susceptibility, electromagnetic compatibility (EMC), and reliability.

INTRODUCTION

Many NASA and Air Force spacecraft require data storage equipment onboard to meet mission needs. In the past the data storage function has been accomplished by magnetic tape recorders. Concerns for reducing the high rate of mechanical failures due to moving parts (Ref. 1) has led NASA to undertake the development of two standard tape recorders having approximate storage capacities of 10^8 and 10^9 bits. Standardization of the tape recorder should improve reliability; however, other limitations such as cost and versatility will still pose problems for some users.

At the present time, there is no standard digital data recorder for relatively low capacity (10^7 bits) applications. Users must suffer the penalty of excessive costs in resorting to larger capacity (10^8 bits) tape recorders and/or developing custom design memories. In addition, some applications require buffer-type storage with flexible record to playback capability. The requirements to simultaneously record and playback cannot be met by a single standard tape recorder. In other applications, the effectiveness of a large tape recorder can be enhanced by use with a smaller buffer recorder. A buffer recorder capable of handling asynchronous data down to d.c. data rates would enable simpler tape recorder functions and, hence, improve overall reliability. It has been recognized that the implementation of bubble domain technology as a data recorder offers advantages in versatility, potential reliability, and cost.

In an effort to begin to demonstrate these advantages NASA is developing a 10^8 bit Solid State Data Recorder (SSDR) under contract NAS1-14174. This

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effort is based on bubble domain materials and device work (Refs. 2, 3, 4) extending back to 1969, the successful design and fabrication of a small three-track feasibility model recorder (Ref. 5) in 1974, and the development of a large capacity (10^5 bits) memory chip (Ref. 6) in 1975. The bubble domain device technology and magnetic and electronic concepts developed on the 10^8 bit SSDR program (Ref. 7) are applicable to a bubble memory of any size up to 10^8 bits. The development of an adequate memory cell technology is viewed as a prerequisite for beginning development of a standard bubble memory. The 10^8 bit SSDR program is demonstrating that a memory cell technology already exists for meeting the electronic, magnetic, and environmental needs of a versatile spacecraft data recorder.

A preliminary design for a Standard 10^7 Bit Solid State Memory (SSM) has been conceived using bubble domain technology. The design employs a modular concept to maximize the SSM's utility in a broad range of applications. The purpose of this technical memorandum is to establish the baseline technical requirements to which the modularized SSM is being developed.

MEMORY SYSTEM CONCEPT

SYSTEM GOALS

The memory system to be developed must be nonvolatile, versatile, adaptable to both serial data and parallel data applications, highly

reliable, and cost effective. The reliability and cost goals are respectively a mean time before failure (MTBF) of over 60,000 hours and a cost in production of less than \$100K per flight qualified unit. In addition, the memory should afford reasonable radiation hardness to meet the bulk of potential applications. The combination of all of these system needs with the general spacecraft goals to minimize weight, volume, and power has led to a set of requirements which can effectively be met by a modular system design. The modular system design separates bubble technology, control logic technology, and power supply technology in such a fashion to 1) afford the immediate development of a serial data memory and a redundant parallel data memory and 2) afford potential users the capability of expandable storage capacity and adaptability to custom data control systems.

DESIGN CONCEPT

Three basic subsystem modules form the basic building blocks for the Standard 10^7 Bit Solid State Memory (SSM), (Ref. 7). These modules are the Standard Memory Module (SMM), the Data Control Unit (DCU), and the Power Supply Module (PSM). Figure 1 depicts the use of the modules in assembling a Serial Data Memory (SDM) and a Dual Parallel Data Memory (DPDM). In the case of the SDM the user interfaces to the DCU whereas for the DPDM, the user interfaces directly to each SMM. Detailed specifications for the subsystem modules, baseline specifications for the SDM and DPDM, and system environmental requirements are discussed herein.

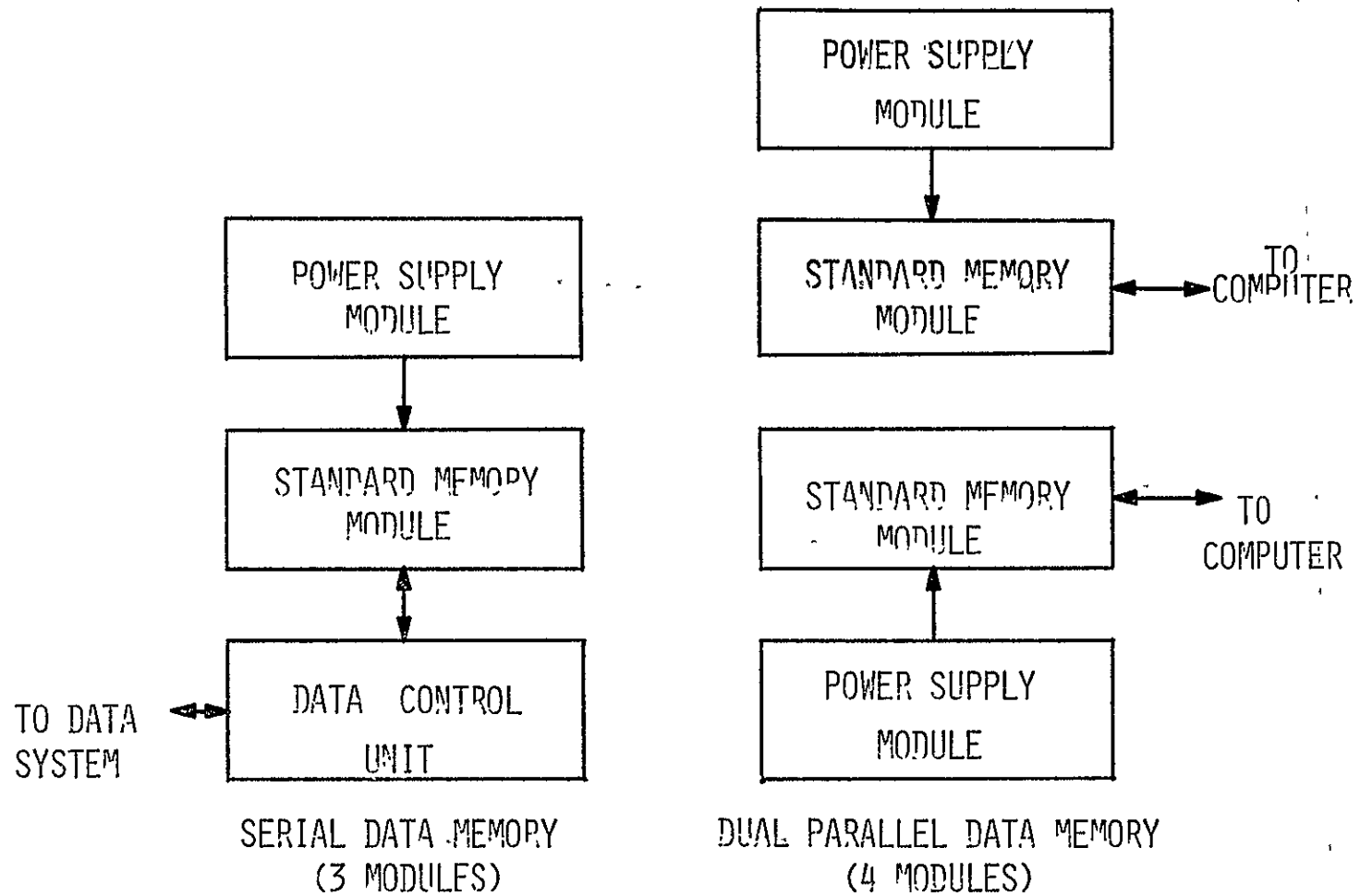


FIGURE 1. BLOCK DIAGRAM OF THE TWO VERSIONS OF THE SSM.

SUBSYSTEM MODULES

STANDARD MEMORY MODULE (SMM)

General SMM Features

The Standard Memory Module (SMM) is the key module in this modular approach to the SSM. Each of the data storage systems (reference Figure 1) will contain at least one SMM. The SMM will contain memory cells using magnetic bubble domain memory devices for the data storage. The SMM is a self contained memory module with all functions (except power supply) necessary to store and retrieve data from the memory cells contained within the SMM. However, no address pointers are contained within the memory module and maintenance of cell alignment and other data address pointers is the responsibility of the DCU or other user controller to which the SMM is interfaced. The SMM will be designed in such a manner as to allow multiple SMM's to be connected together in a data storage system.

The memory module is capable of operating in an incremental or burst mode. An incremental mode is defined as the asynchronous access to cell data on a single-cycle basis. Cell drive cycles are initiated by execute pulses and are self completing. A burst mode is defined as the synchronous access to cell data in bursts of cycles at the maximum cell drive cycle rate. Bursts are initiated by a level signal on the execute which acts as a burst gate signal.

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Memory Cell Philosophy

The SMM is organized into cells, each consisting of a number of bubble domain chips, an accompanying set of magnetic drive coils, and a bias and shielding structure. The chips in each cell operate as a group under the same bias field and rotating field coils. The number of cells required in the SMM depends on the storage capacity of each cell. The useful data storage capacity of the SMM will be at least 1.28×10^7 bits.

The memory chips to be included in the memory cell are LPE grown single crystal magnetic bubble domain devices having not less than 102.4 kilobits of useful data storage capacity per memory chip. Other electronic components may be included within the cell. The cell will operate over the temperature range -10°C to $+60^{\circ}\text{C}$. A cell will be a separate system component with clearly documented engineering drawings and fabrication procedures and methods. The cell is a component which, after initial internal adjustments, will operate both separate from the system or installed in the system without further internal adjustments. Each cell is operationally, mechanically, and electrically interchangeable with all other cells in the system.

SMM Functional Specifications

The SMM is composed of five major subsections as illustrated in Fig. 2. These are 1) the memory cells, (2) the coil drive circuitry, (3) the sense/operator electronics, (4) the memory module controller, and (5) data

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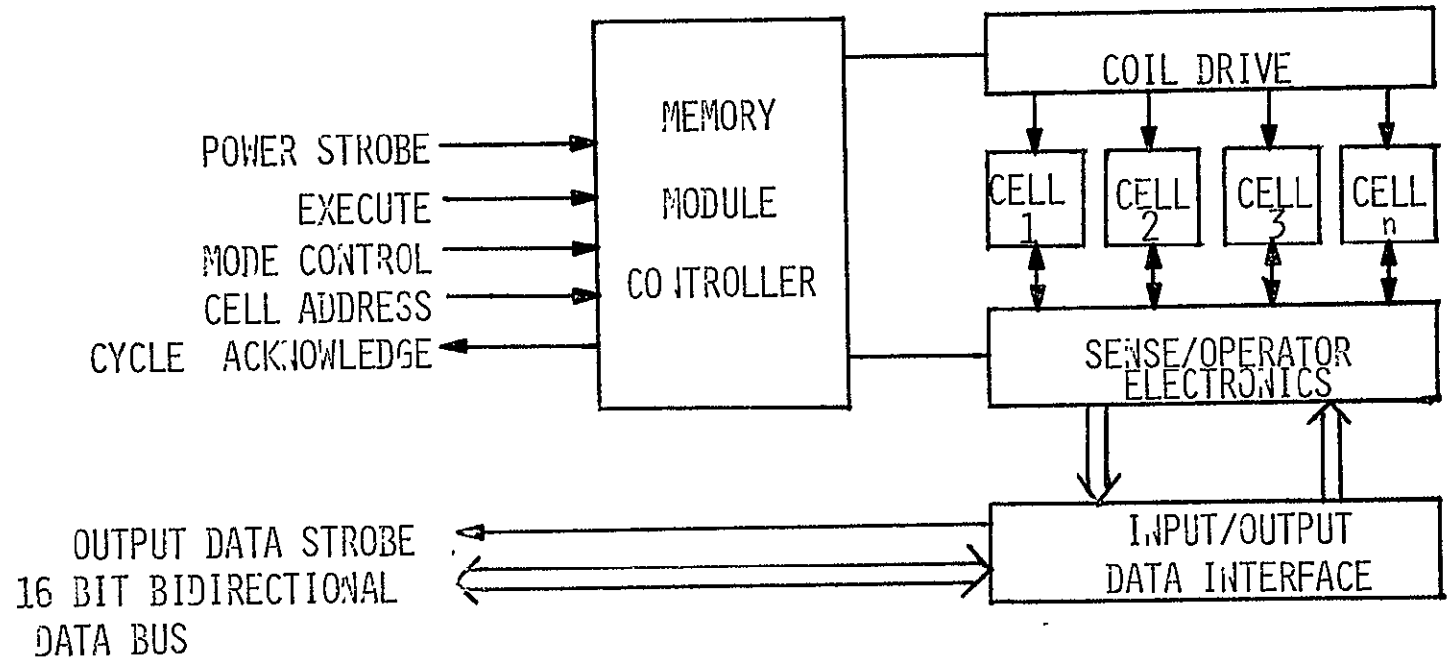


FIGURE 2.- STANDARD MEMORY MODULE FUNCTIONAL BLOCK DIAGRAM.

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input-output. The cells interface with the coil drive and the sense operator electronics. The memory module controller interfaces with the coil driver, sense/operator electronics, and input/output. The memory module controller interprets control signals, cell addresses, and execute signals, generates the timing and control for the coil drive and sense/operator circuits, and transfers data to and from the memory cells.

Memory Module Controller

The memory module controller has the following input signals:

Power Strobe. - This signal powers up and initializes the controller in preparation for the receipt of an execute signal.

Cell Address. - This is a parallel binary coded cell address signal used to select the cell to be active for the next operation.

Mode Control. - Control lines will be provided to select the operation mode for the next cycle of the SMM. The modes to be provided are READ, WRITE, ERASE, AND ALIGN (rotate cells without reading or writing).

Execute. - This signal begins the execution of the next data cycle. The cell address, and the mode control must have been previously set up. The execute serves two functions. If the execute goes low (active low) and remains low, the memory module controller continues to execute cycles of the cell addressed until the execute returns to a high state. Thus, a burst mode is executed. If the execute goes low and returns high within less than approximately half of the cycle time (exact timing to be established during the design phase) the cycle terminates itself

in a controlled manner and awaits another execute pulse. Thus, an incremental access mode is implemented. This requires an internal clock oscillator and timing circuitry within the memory module controller to provide the sequencing operations necessary to operate and interface with the memory cells.

Cycle Acknowledge. - This signal is an output signal to the user (or DCU) which acknowledges the execution of a cycle. The trailing edge of the cycle acknowledge signal must occur before the half way point in the cycle and early enough in the cycle to allow a user to react and terminate the execute within that cycle. For example, if the user is searching for a specific address within a cell, the memory system controller to which the SMM is connected may be counting the cycle acknowledge pulses until the desired number of rotations have occurred. At the proper time, the controller would reset the execute and the cell rotation would terminate within the cycle.

Memory Module Controller Interface

The interfaces to the memory module controller are TTL compatible and able to operate reliably over short lines approximately 6 feet in length.

Data Input/Output

The data input/output (I/O) interface is 16 bits wide parallel. The interface is a bidirectional bus used for both read and write modes.

The normal mode is the read mode with the change to the write input mode being made external to the SMM through the read/write mode control signal. An output data latch is provided and the data presented in NRZ-L format with a data strobe signal available when the data are valid. The I/O interface is also TTL compatible and able to operate reliably with cable lengths approximately 6 feet in length.

Data Rate

The data rate of the memory module depends on whether or not the module is operating in the incremental mode. If operating in the incremental mode, the data rate is user dependent and can vary from 0 to 50K, 16 bit words/second. The data rate in this mode is determined by the pulse rate of the execute signal. In the burst mode, the effective data rate is a function of the duration of the burst and the cell rotation rate which is controlled by the internal clock. The instantaneous data rate during a burst shall not be less than 1.28 MHz.

Interfacing Timing Definitions

The following interface timing parameters are illustrated in Figure 3 with design values given in Table 1:

- t_{ec} - Execute pulse period (defined for incremental mode only).
- t_{ps} - Power strobe setup time required before first execute pulse.
- t_{ew} - Execute pulse width (defined for incremental mode only).
- t_a - Delay between falling edge of the execute pulse and the rising edge of the cycle acknowledge.

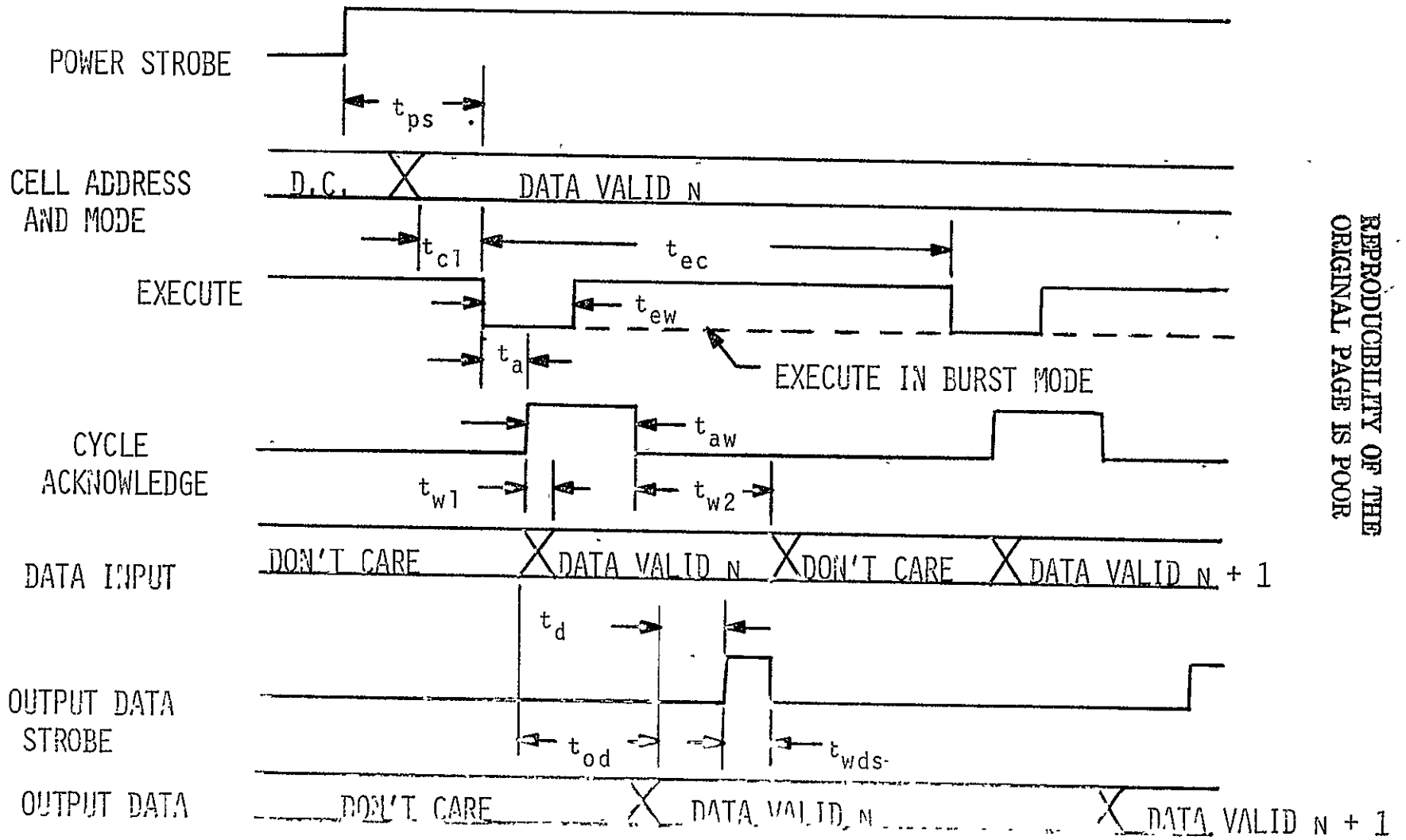


Figure 3. SMM Interface Timing

	<u>MIN</u>	<u>NOM</u>	<u>MAX</u>
t_{ec}	20 μ S	NA	NA
t_{ps}	1 MS	NA	NA
t_{ew}	TBD	TBD	10 μ S
t_a	TBD	100nS	TBD
t_{aw}	TBD	10 μ S	TBD
t_{el}	TBD	100nS	NA
t_{w1}	NA	NA	500nS
t_{w2}	100nS	NA	NA
t_d	500nS	NA	NA
t_{od}	TBD	TBD	TBD
t_{wds}	1 μ S	TBD	TBD

Table 1. Memory Module Interface Timing Characteristics.

- t_{od} - Delay between cycle acknowledge & output data valid.
- t_d - Delay between output data valid & leading edge of the output data strobe.
- t_{wds} - Output data strobe pulse width.
- t_{aw} - Cycle acknowledge pulse width.
- t_{cl} - Setup time for cell address and mode control prior to execute pulse.
- t_{wl} - Delay between the rising edge of the cycle acknowledge and input data valid.
- t_{w2} - Hold over time following falling edge of cycle acknowledge during which data must be valid.

SMM Physical Description

The SMM will be built in a modular fashion such that the module can be connected together with other modules (additional memory modules, digital control units, and power supplies) or used in a stand-alone fashion.

Weight Requirements

The weight of a fully populated 10^7 bit standard memory module is approximately (7) seven pounds. This weight does not include cover plates or other mounting hardware which would be required only in a stand-alone application.

Power Requirements

The Standard Memory Module is designed in such a way that it can be power strobed. The power required is a function of frequency and the design goal for this development is illustrated in Figure 4.

DATA CONTROL UNIT (DCU)

General Features

The purpose of the DCU is to provide a flexible serial data interface to the SMM. This module, illustrated in functional block form in Fig. 5, provides command control of configurational and functional performance of the Serial Data Memory (SDM). All housekeeping information is contained within the DCU so that the user "sees" only a serial memory having the features of the selected configuration.

DCU Configurations

The DCU, upon command, will operate in one of three possible configurations -- single channel, dual channel, and buffer. Brief descriptions of these configurations are as follows:

Single Channel Configuration

In the single channel configuration, the entire capacity of the SSM is under the control of the No. 1 command input and the No. 1 data input/output port.

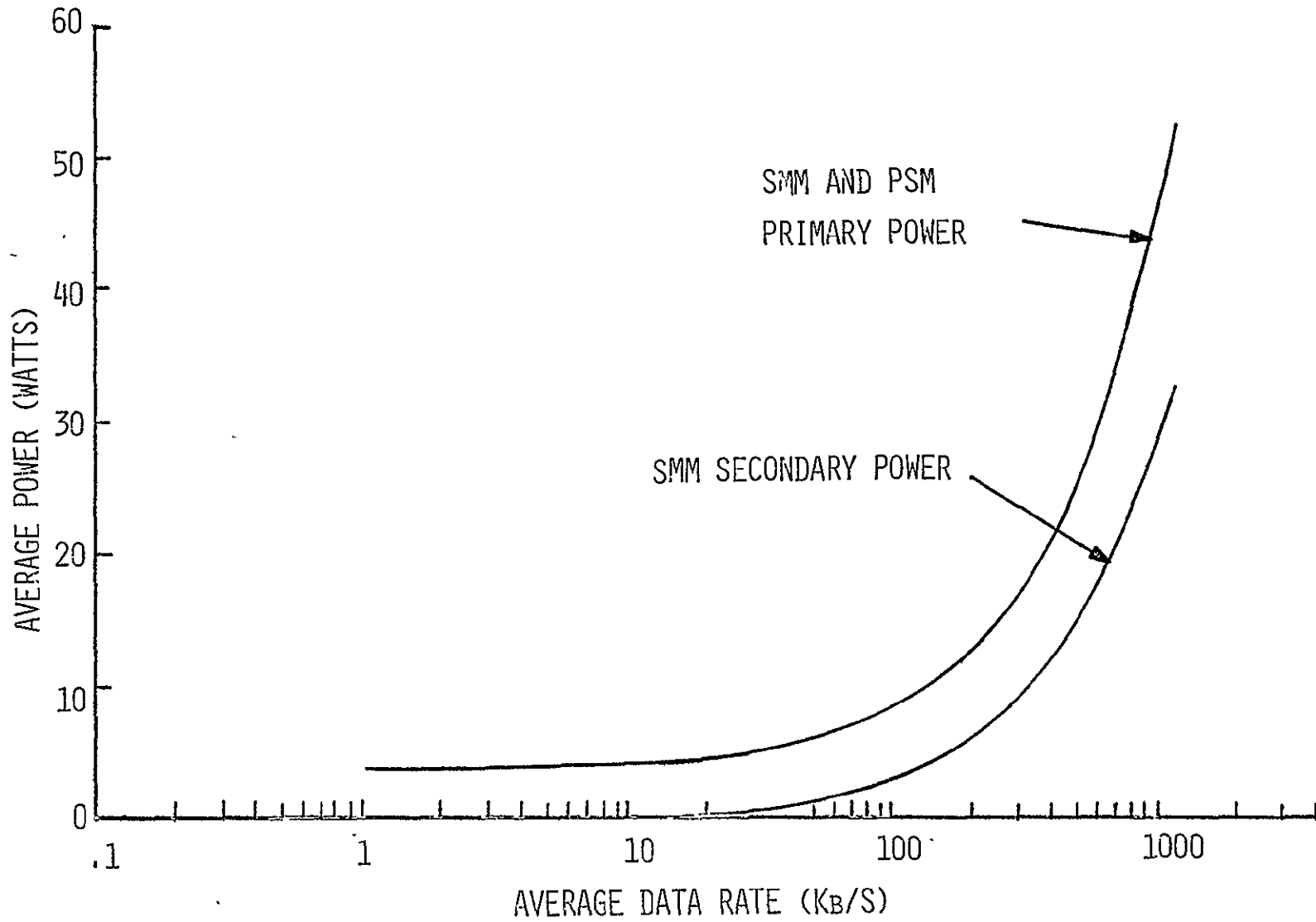


FIGURE 4.- POWER GOALS FOR SMM.

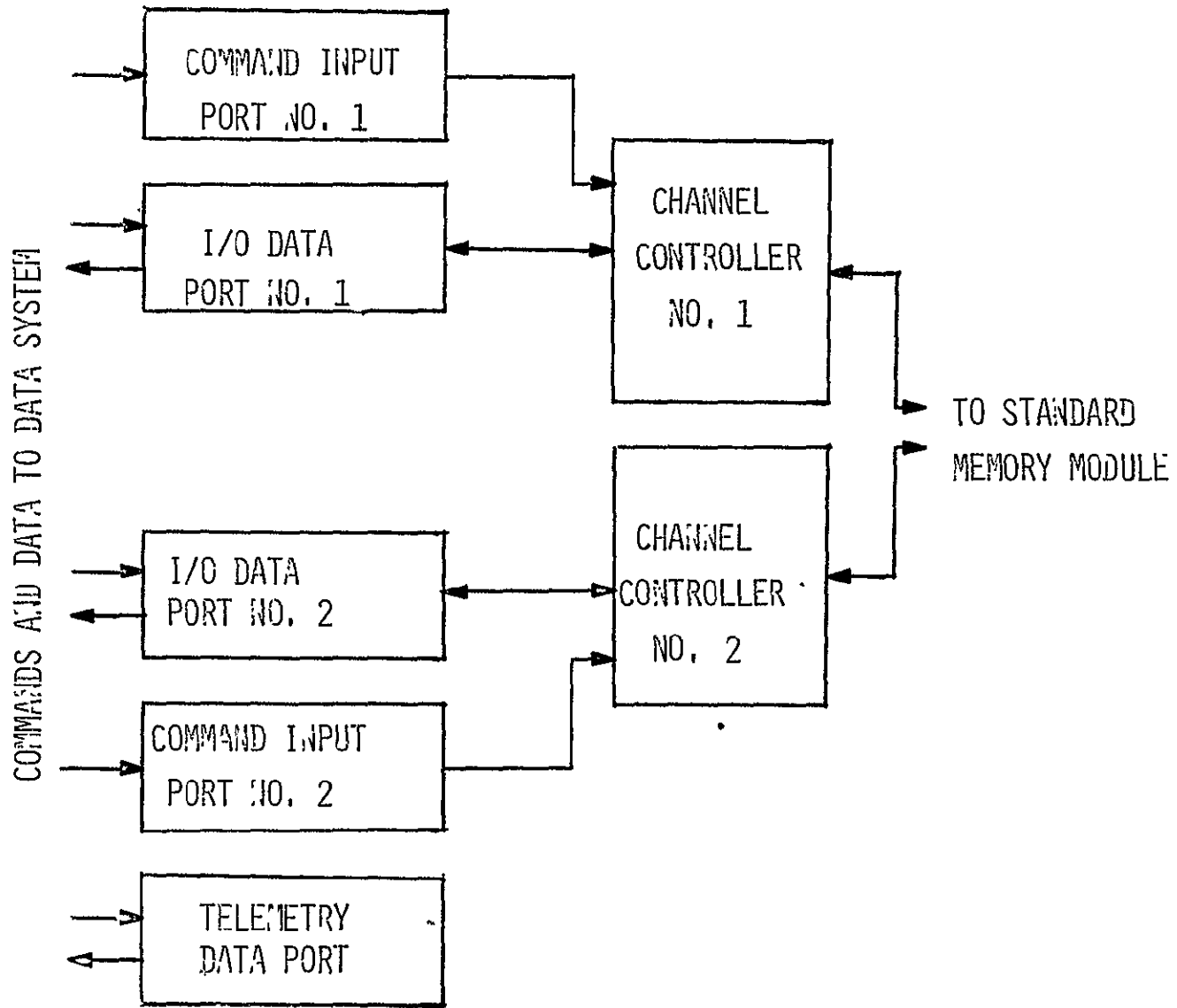


FIGURE 5.- DCU FUNCTIONAL BLOCK DIAGRAM.

Dual Channel Configuration

In the dual channel configuration half of the capacity of the SSM is under the control of the No. 1 command input and the No. 1 data input/output port. The other half of the capacity of the SSM is under the control of the No. 2 command input and the No. 2 data input/output port. The two halves of the memory are functionally independent.

Buffer Configuration

The buffer configuration uses a combination of single channel and dual channel features. While internally divided into two channels, the memory appears to the user to be a single channel. This configuration is intended for use in applications which require the ability to record data continuously and without interruption during intermittent playback of the data. The No. 1 command input controls the memory, the No. 1 input/output data port handles input data, and the No. 2 input/output data port handles the output data. Data output and data input can occur simultaneously and at different user-controlled data rates from dc to 512 kbs.

Configuration Control

The configuration of the DCU is controlled through the serial command interface of either command port. Unique serial command words will be assigned to the configurations. Upon receipt of a configuration control command word, the DCU initializes the channel controllers for the commanded configuration and stores the configuration's status in nonvolatile storage.

The commanded configuration continues to control the operation of the DCU through any combination of commands and power on/off sequences until a new configuration command is received. New configuration commands are not received unless the memory is in an idle state, with the following exception. If the memory is in a state other than idle, and two configuration commands are received in sequence without any other command between them, the memory will execute the second configuration command overriding whatever the memory was doing at that time. The SSM is not required to maintain any of the previous status pointers should such an override occur.

Data Address Marker Definitions

The following data address marker definitions are given for the purpose of simplifying the functional description of the DCU.

Beginning of Cell (BOC)

The beginning of cell (BOC) address is the zero address of the cell in question and is equal to the current position of the cell immediately following a reset command. The status of cell rotations relative to this BOC address must be maintained by the DCU to meet requirements for first-in/first-out record and then play back of data.

Beginning of Storage (BOS)

Beginning of storage is defined as the BOC of the first cell within the channel's allocated storage.

End of Cell (EOC)

End of cell is defined as the last data byte recordable in a cell without over writing previously recorded data within the cell and is equal to BOC-1.

End of Storage (EOS)

End of storage is defined as the EOC of the last cell within the channel's allocated storage.

Write Pointer (WP)

Write Pointer is the address of the next contiguous data byte available for the storage of recorded data.

Read Pointer (RP)

Read Pointer is the address of the next contiguous data byte to be read in the playback mode.

Cell Pointer (CP)

Cell Pointer is the byte address of the currently active cell.

Cell Address (CA)

The Cell Address is cell number of the currently active cell.

Memory Channel Address (MCA)

The Memory Channel Address is the combined address of the CP and CA and defines the active byte within a channel.

SSM Commands

Command Definitions

Reset. - The Reset Command clears all status pointers for the channel and initializes the Write Pointer (WP) and the Read Pointer (RP) to Beginning of Storage (BOS) without requiring rotation of any cells.

Record. - The record command initiates the recording of data and prepares the SSM to accept data from the channel's input/output port and store the data sequentially in the data storage allocated to the channel. The data valid flag for the channel is set to the true state (high) and data are accepted into the channel's input buffer at the user clock rate. Any clock data rate up to the maximum channel rate is permissible. Data rates in excess of the maximum channel rate will not damage the SSM, however, some data loss may be encountered due to periodic overflow of the input buffer. The data are transferred periodically from buffer to the SSM, using the burst mode as required to prevent overflow of the input data buffer. Storage in the SSM begins at the Write Pointer (WP) and continues until a Stop command is received or the End-of-Storage (EOS) for the channel is encountered. If EOS is encountered, recording stops and the data valid flag for the channel's input/output port goes false and the SSM assumes an idle mode for that channel. While recording the Memory Channel Address (MCA) and the Write Pointer (WP) track one another. At EOS or upon receiving a Stop command, the WP is stored in nonvolatile storage and no cell realignment takes place.

If a record command is executed while the DCU is in the buffer configuration, data input through the No. 1 input/output port is stored at the Write Pointer (WP) similar to the above description with the following exceptions. When half of the capacity of the memory is full of data, a signal indicating the half full point is generated (see interface type described in Figure 7). This signal normally will indicate to the user's system controller that a playback command should be issued to playback the data stored in the first half of the memory. Data continues to be stored in the second half of storage. Normally by the time the second half of the memory is full, the playback command will have played back the data in the first half and reset the half full indicator. Thus, when the second half becomes full, the half full flag is set again and storage begins again at the BOS of the first half. Should the first half not have been played back by the time the second half of the memory is full, the DCU shall stop storing data, reset the data valid flag at the input, store the appropriate pointers in nonvolatile storage and assume an idle mode.

Playback. - The playback command initiates the playback of previously stored data and prepares the SSM to transfer data from the SMM to the channel's input/output port.

Data are transferred from the SMM to the channel's output buffer starting at the Read Pointer, using the burst mode until the buffer is full. Additional data are transferred periodically to the buffer as required to prevent the output buffer from becoming empty. The data valid signal goes true as soon as there is data in the buffer. The manner in which data are clocked out of the buffer depends on whether the SSM has

previously received an internal or external command. If an internal command has been received, the data are clocked out of the output buffer at the maximum data rate for the channel by the internal clock. If an external command has been received, the data are clocked out of the output buffer by an external clock provided by the user. External clock rates exceeding the maximum channel rate will not damage the SSM, however, some data errors may occur due to premature emptying of the output buffer. Data transfer continues until a Stop command is received or the Read Pointer equals the Writer Pointer. At that point, data transfer from the SSM stops; and as soon as the output buffer becomes empty, the data valid flag goes false, and the SSM assumes an idle mode for the channel.

If a playback command is executed while the DCU is in the buffer configuration, operation of the SSM is similar to that described above with the following exceptions. When one of the half full boundaries is encountered, its half full indicator shall be reset. At this point, the status flag indicating whether or not the other half is full is interrogated. If the other half is not full, the playback is terminated. If the other half is full, playback continues until the end of the second half is encountered, etc.

A playback command will be valid even if the half-full flag has not been set. For example, if recording is stopped, leaving a partially filled area in one half of the memory, a playback command will output the remaining data and stop at the write pointer. For the case where data are currently being recorded in one-half, but the half full point has not

been reached, the other half is empty, and a playback command is received, the recording in the current half is stopped and automatically resumed at the start of the second half to enable playback of the currently available data in the first half.

Stop. - The Stop command is used to terminate the recording or playback of data. When a Stop command is received, all status pointers (WP, RP, etc.) are stored in nonvolatile storage, data transfer is terminated as described in the various command descriptions and the idle mode is assumed.

External. - The External command is used to select the external clock mode for playback commands. A status flag indicating the commanded external mode will be stored in nonvolatile storage. This flag is set by the External command and will be interrogated by the DCU before executing a playback command to insure that the SSM operates in the required output mode. Provision will be made for independent status flags for configuration 2, the dual channel configuration.

Internal. - The Internal command is used to reinitialize the Internal/External status flag to the Internal mode. In this mode, Playback commands transfer data at the maximum channel data rate synchronized with the internal clock.

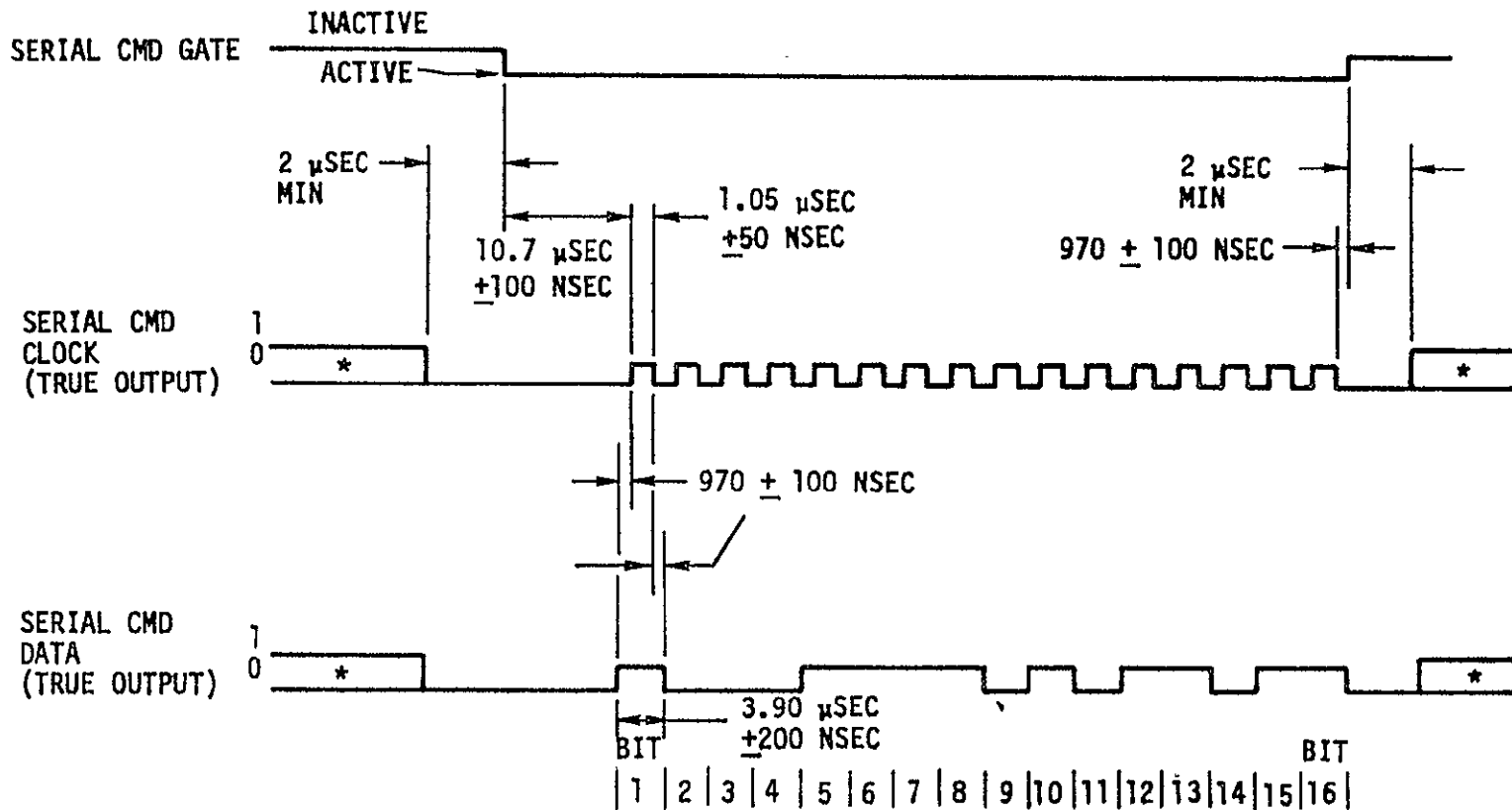
Replay. - The Replay command functions similarly to the Playback command except that data transfer always begins at beginning of storage (BOS) rather than at the Read Pointer (RP). All other functions are the same as for the Playback command.

Skip (N). - The Skip (N) command flags the N^{th} cell such that it is skipped automatically in subsequent record or playback operations. N command codes are required to accomplish this command.

Skip Reset (N). - The Skip Reset (N) command resets the skip flag for the N^{th} cell, hence enabling the N^{th} cell for subsequent record or playback operations. N command codes are required to accomplish this command.

Command Interface

Figure 5 illustrates the relationship of the command input ports to the rest of the DCU. The DCU has two command input ports which are utilized in the various configurations. Each command interface has three control signals -- a command data input, a command clock input, and a command gate input (Ref. 8). The timing relationships for these signals are presented in Figure 6. The command sequence is described as follows: The command gate goes low, the serial 16 bit command data word is clocked into the command interface clock by the command, and then the command gate goes high. The low to high transition of the command gate is a signal to the SSM that the serial command is ready to be decoded. The command word will be 16 bits in length and use odd parity. The command interface checks for odd parity of the command word. The bit count of the command clock is checked when the command gate goes high to verify that 16 command clock pulses have been received. If the parity and bit count are as specified, the command interface will output to the user a command acknowledge signal indicating receipt of a valid command. The command interface is capable of operating with any command clock pulse



UNDETERMINED SIGNAL LEVEL

Figure 6. - Timing Diagram for Serial Command Transmission.

rate up to 1.0 MHz. The command interface will be of the type indicated in Fig. 7 with final interface type selection to be made by the Government prior to final assembly of each unit.

Input/Output Interface

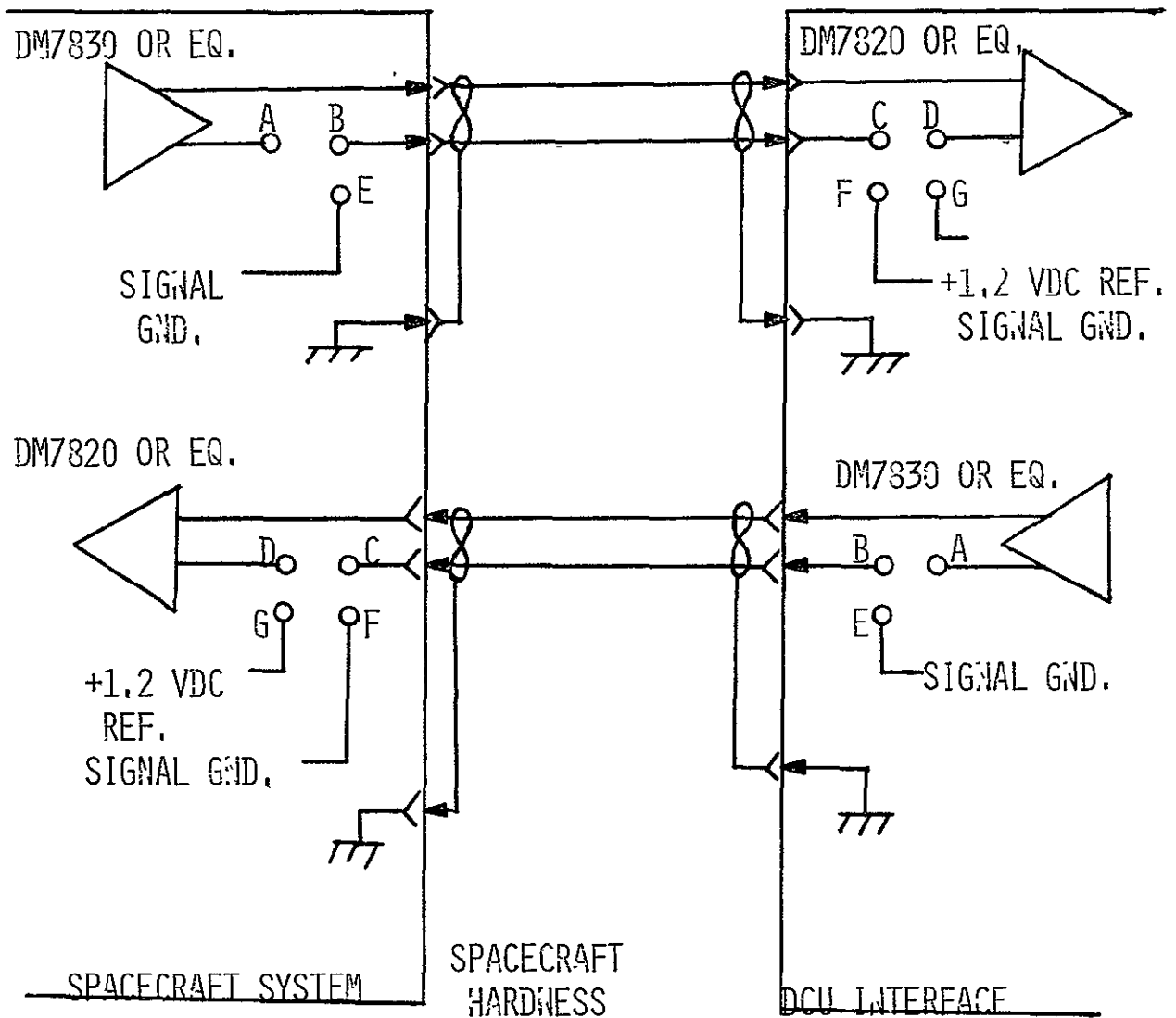
Figure 5 illustrates the relationship of the Input/Output interfaces to the rest of the DCU. The DCU has two identical, independent input/output ports. The functional operation of these input/output ports is determined in part by the configuration of the SSM. The following are configuration-independent specifications applicable to both input/output ports: (Where Fig. 7 is specified as the interface type, the final selection of interface type is to be made by the Government prior to final assembly of each unit.)

Data Buffer

Each input/output port will have a data buffer to provide input and output data rates asynchronous to and independent of the operating data rates of the SMM.

Data Input

Data input to each input/output port will be NRZ-L. The input interface is a differential line receiver which can be strapped for balanced differential or single ended operation. See Figure 7 for the interface description.



TYPE I INTERFACE (TTL COMPATIBLE) - JUMPER B-E, C-F, D-G

TYPE II INTERFACE (BAL. DIFFERENTIAL) - JUMPER A-B, C-D

Figure 7. - Input/Output Interface Description

Input Data Clock

An input data clock will be provided by the user, coherent with the input data. Any data rate not exceeding the maximum data rate of the channel is permissible. The input data may lead or lag the input data clock by a maximum of 7% of the bit period. Rise and fall times for the input data clock will not exceed 10% of the input bit period or 10 microseconds, whichever is least. Figure 7 specifies the interface type and figure 8 defines the data and clocking waveforms.

Output Data

Output data from each input/output port will be capable of operating in a NRZ-L mode or a Bi-Phase level mode (Split Phase, Manchester 11 + 180° where "one" is represented by a 1/0 transition and a "zero" is represented by a 0/1 transition.)

Output Data External Clock

When in the external output mode, the output data rate is under the control of the output data external clock. Timing relationships for the output data and output data clock are indicated in Figure 9. Figure 7 specifies the interface type.

Internal Data Clock Output

A symmetrical internal data clock output coherent with the output data is made available to the user whenever data are output in the internal clock mode. This clock output utilizes the interface type described in Figure 7. The timing relationships of the clock signal are shown on

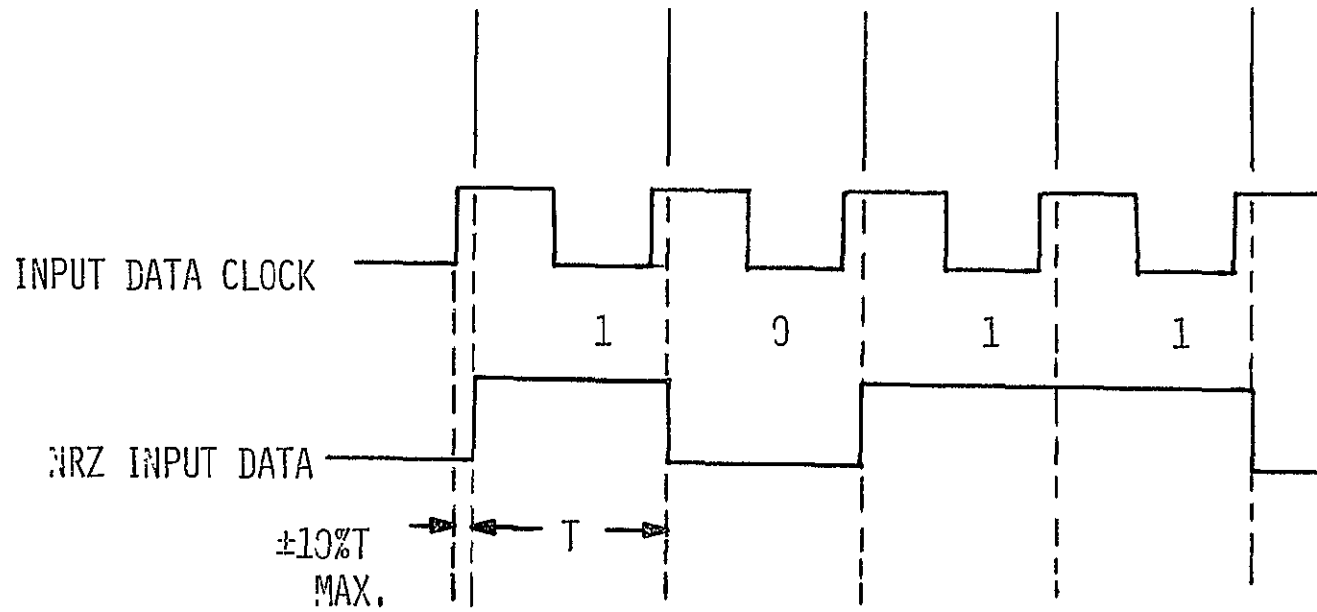


Figure 8. - Input Data to Input Data Clock Phase Relationships.

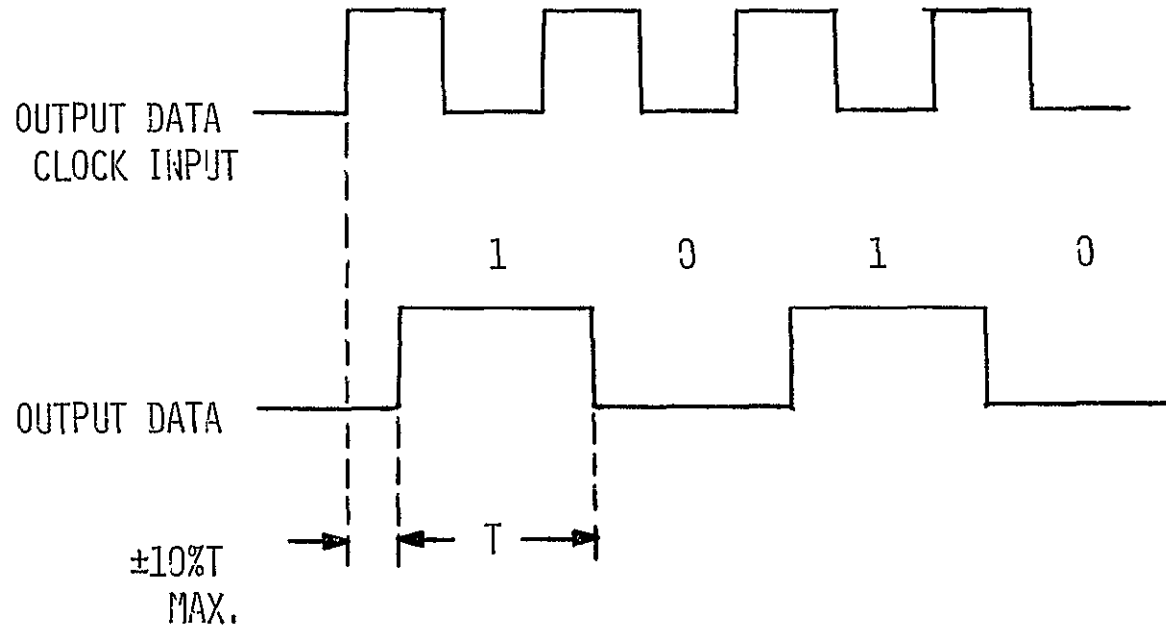


Figure 9. - Output data and data clock phase relationships for the External Clock Playback mode.

Figure 10. The rising edge of the internal output data clock will not lead or lag the data by more than 7% of the clock period. Whenever the DCU is in the external clock mode or data are not being transferred in the internal mode, the output level on the internal data clock output remains in the low (zero) state.

Data Valid Indicator

A data valid indicator is provided at each input/output port and is utilized as specified in the various configurations and modes. The data valid indicator utilizes the interface type described in Figure 7.

Data Rate

In configuration 1, the SSM will record or playback asynchronous data from d.c. to 1.024 Mbps. In configurations 2 and 3, the data rate will be d.c. to 512 kbps for each channel. The data rate for each channel will be completely independent of that in the other channel. The SSM will be designed such that user data rates and clock rates inadvertently in excess of the maximum rates will not damage the SSM.

Playback Inhibit

A control line is provided at each input/output port which can inhibit the internal or external clock controlling the output data buffer. A low input on the Playback Inhibit line has no effect on the data transfer at the Input/Output Interface. However, a high state on the Playback Inhibit

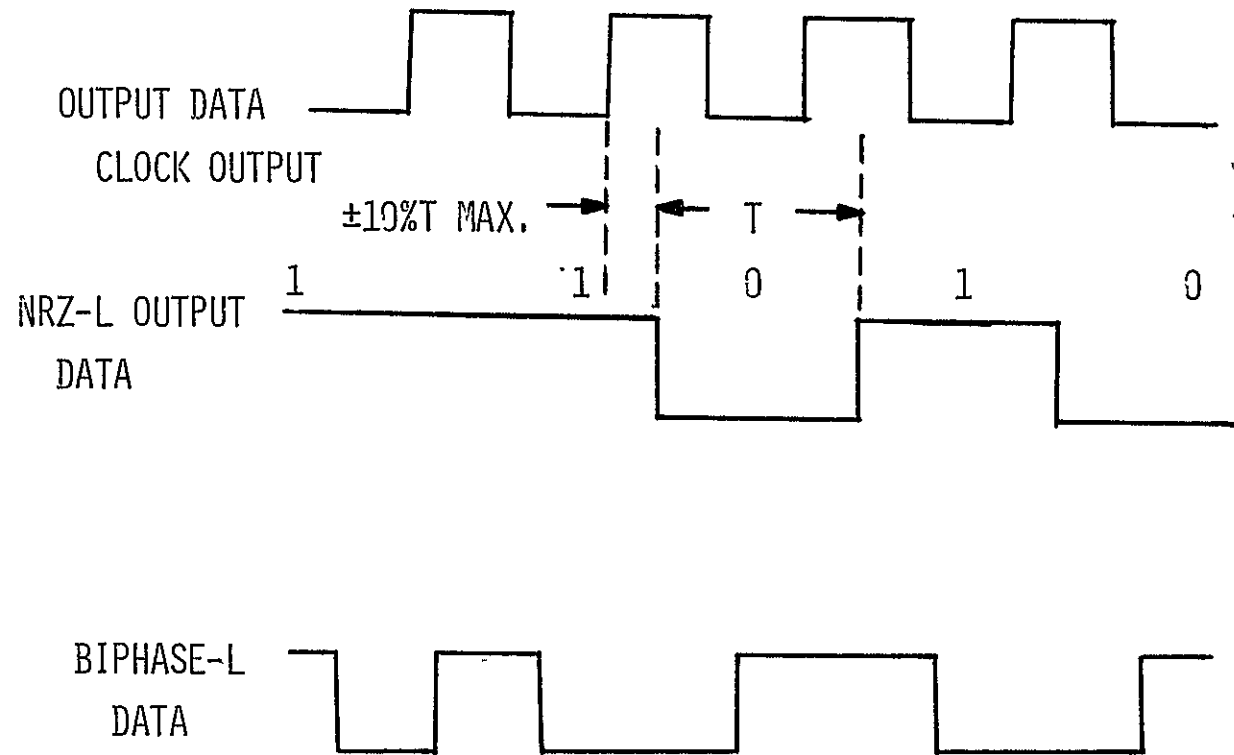


Figure 10. - Output data and clock phase relationships for the Internal Clock Playback mode.

line inhibits the transfer of data out of the output buffer via either an internal or external clock source. See Fig. 7 for the interface type.

Emergency Shutdown

The DCU will store the active channel cell pointer in nonvolatile storage each time a cell boundary is crossed. In the event that an emergency shutdown occurs without an emergency shutdown warning, the DCU will not be damaged and at worst will scramble the data in the current cell and lose data in the buffers. When power is again restored, the DCU will cause the SSM to come on in an idle mode, requiring new commands to either renew the function interrupted by the emergency shutdown or initiate new functions.

The DCU shall have an emergency shutdown warning line which, when given a "low" signal pulse with a minimum duration of 1 msec, will cause the SSM to interrupt the current mode, terminate the input of data, orderly empty the input buffers, store the channel MCA's in nonvolatile storage, and place the SSM in the idle mode. Since output buffers may not be under the control of the SSM, data in output buffers could be lost. A copy of the lost data will always be available in bubble storage, however, it will be the user's responsibility to transmit the commands necessary to repeat it. If the user output data clock rate is high enough, no data loss should occur. The data rate below which user output buffer data could be lost will be identified during system development.

The warning signal may be expected to precede actual power shutdown by no more than 50 msec. Reapplication of power will cause the SSM to come on in an idle mode, requiring new commands to renew the interrupted function or initiate new functions.

Telemetry Interface

Monitored Parameters

The DCU provides a separate telemetry port for telemetry and testing purposes. Analog measurements proportional to the following parameters will be provided:

- 1) All primary and secondary voltages of the power supply module.
- 2) Total primary current of the power supply module.
- 3) Drive field power supply current for the memory module.
- 4) The temperature of the hottest region of each module of the SDM. If the hottest region of the SMM is not one of the memory cells, then the temperature of the hottest memory cell shall also be monitored.

The following digital parameters used in the DCU are provided via a serial multiplexed digital data system.

- 1) Quantity of data stored in each channel (to 4 bits resolution).
- 2) Write pointer for each channel.
- 3) Read pointer for each channel.

- 4) Cell status. - This data represents a cell map indicating which cells if any, have been marked off by a skip cell command.
- 5) Current mode of operation for each channel.
- 6) Last command received and executed or being executed for each channel.
- 7) An indication that End of Storage has been encountered while in a write mode. Required for each channel.
- 8) An indication that Playback has been completed (i.e., RP = WP) for each channel.
- 9) Current configuration.

Analog Data Format

Each analog measurement is provided on a separate pin on a telemetry interface connector. The signals will be calibrated and scaled to interface with a 0 - 5V analog data acquisition system.

Digital Data Format

The digital status and measurements will be formatted and output serially. Figure 11 illustrates a block diagram of the digital telemetry interface. The telemetry interface will be of the type indicated in Fig. 7 with final interface type selection to be made by the Government prior to final assembly of each unit.

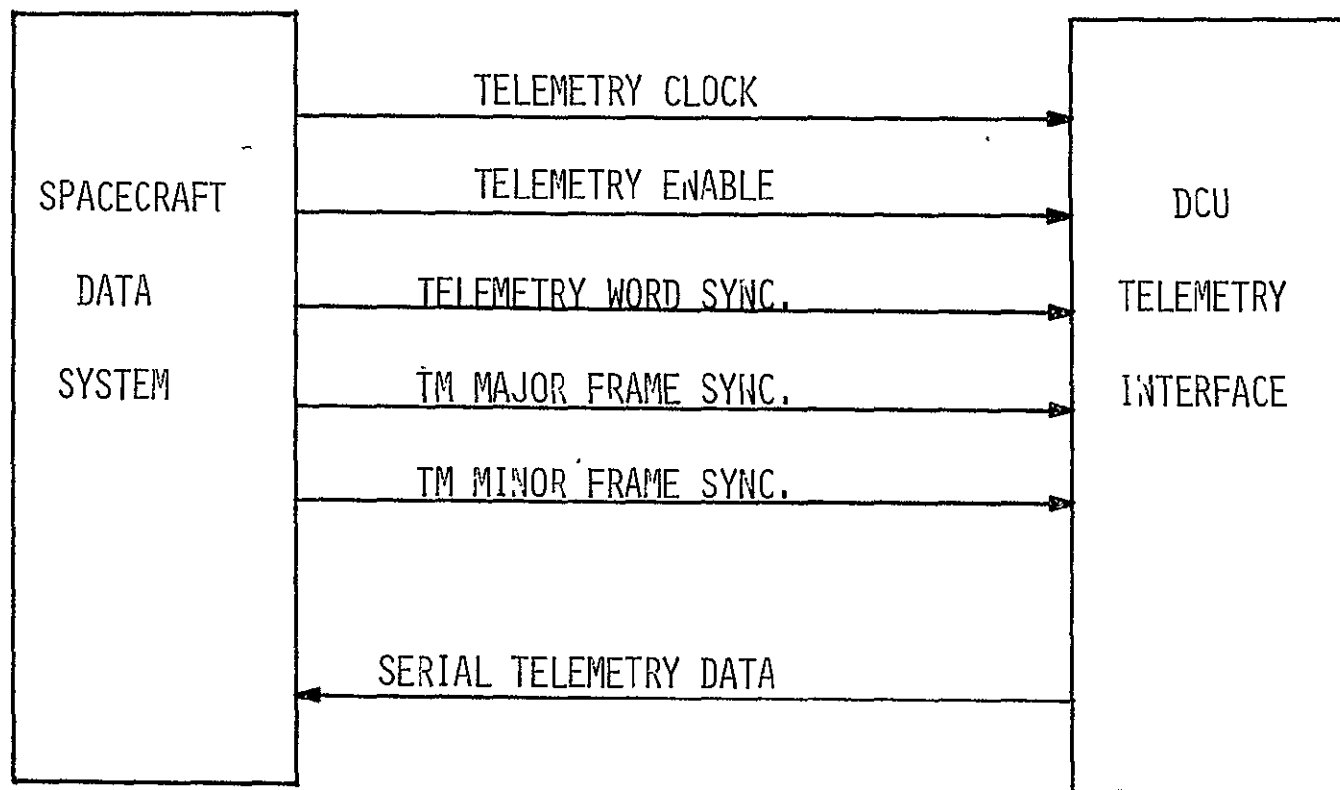


Figure 11. - Digital telemetry interface.

POWER SUPPLY MODULE (PSM)

Input Voltage

The input voltage will be 28 ± 7 V d.c. The SSM performance will not be degraded when exposed to ripple and noise transients on the power line as specified in MIL-STD-461/462, Methods CS01, CS02, and CS06.

Power Consumption

The PSM will provide the voltages and currents required to power either the SDM or the DPDM. In the DPDM, the PSM will supply power to only one SMM. In the SDM the PSM will supply power to both the DCU and SMM.

Reverse Voltage Protection

The power supply will be designed such that inadvertent reversal of the input power supply voltage will not damage or degrade the SSM in any way.

Power Supply Grounding

A 4-wire grounding system is provided such that power ground, data signal ground, telemetry, and chassis ground are kept separate and made available at an interface connector. Telemetry and chassis grounds are not necessarily isolated from each other.

Power Interface Requirements (Ref. 9)

Turn-On/Turn-Off Transients

Transient turn-on currents will not exceed the following limits:

- a) The initial in-rush current due to distributed capacitance, EMI filters, etc. will not exceed 10 amperes peak for 10 microseconds.
- b) The rate of change of in-rush current after the initial surge will not exceed 20 milliamperes per microsecond.
- c) For loads of 50 watts or less, the transient current will not exceed 300 percent of the maximum steady state current.
- d) For loads greater than 50 watts, the transient current will not exceed 200 percent of the maximum steady state current.
- e) Steady state operation will be attained within 50 milliseconds from the start of the transient.

The peak voltage of transients generated on the power lines during turn-off due to inductive effects of the load will not exceed +55 or -20 volts d.c. with respect to ground.

Operational Transients

Operational transients, those occurring after initial turn-on, will not exceed 125 percent of the maximum peak operational current drawn during normal operation. The maximum duration of the transients will not exceed 50 milliseconds. The rate of change of current during the transients will not exceed 20 milliamperes per microsecond. The maximum incremental change in load will not exceed 500 watts during a one second time interval for increasing or decreasing loads.

Reflected Ripple Current

The peak-to-peak amplitude of steady state load current ripple will not exceed 5 percent of the maximum, average, steady state current. Any

d.c. to d.c. converters used in the PSM will not have fundamental switching frequencies above 50 kHz.

Current Limiting

Passive or active current limiting will be employed as required to limit in-rush currents.

SERIAL DATA MEMORY (SDM)

GENERAL SPECIFICATIONS

This version of the SSM will consist of three modules, the Standard Memory module, the Data Control Unit, and the Power Supply Module as depicted in Figure 1. These modules will be interconnected and mounted together in one chassis to form a serial data memory. The functional characteristics shall be controlled by the functional specifications of the Data Control Unit. The weight of the SDM will be no greater than 19 pounds (8.6 kilograms). The volume of the SDM will be no greater than 380 in.³ (6230 cc). The largest dimension will not be greater than four times the smallest dimension. The goal for Mean Time Before Failure (MTBF) is in excess of 60,000 hours.

POWER CONSUMPTION

The SDM is a nonvolatile system requiring zero power to maintain data integrity when off. The power consumed will be rate dependent and less than the values given in Table 2.

Table 2. SDM Power Requirements

Total Bit Data Rate	Total Power (Watts)	
	1 Chan.	2 Chan.
OFF	0	0
IDLE	9	13
1K	11.5	17.5
10K	12	18
100K	16	22
1M	57	63

BIT ERROR RATE

The SDM will operate with a bit error rate not greater than 1 error in 10^8 bits through all specified configurations, commands, modes, input power variations, data rates, operational environmental conditions, and following submission to non-operational survival environmental conditions.

DUAL PARALLEL DATA MEMORY (DPDM)

GENERAL SPECIFICATIONS

This version of the SSM will consist of four modules, two SMMs and two PSMs, as shown in Figure 1. Each SMM will be connected to a separate PSM such that two completely independent, parallel access, data memories are established. The memory modules for this version will be half populated in order to save weight. The functional specifications for this version are the same as the functional specifications for the SMM since the memory

modules interface directly to the user's flight computer without a DCU internal to the DPDM. The weight of the DPDM will be no greater than 24 pounds (10.8 kilograms). The volume of the DPDM will be no greater than 430 in³ (7050 cc). This version of the SSM will be designed with a goal of a .95 probability that at the end of 5 years the contents of at least one memory block of at least 10⁶ bits (one or more cells) can be read out without a bit error rate greater than 1 error in 10⁸ bits. Power consumption will be governed by the SMM requirements. Bit error rate requirements are the same as those specified for the SDM.

DPDM TELEMETRY

The DPDM will have a telemetry port which shall provide analog measurements proportional to the following parameters:

- 1) All primary and secondary voltages of each power supply module.
- 2) Total primary current of each power supply module.
- 3) Drive field power supply current of each memory module.
- 4) The temperature of the hottest region of each module. If the hottest region of the SSM is not one of the memory cells, then the temperature of the hottest memory cell shall also be monitored.

These measurements will be made for each half of the DPDM in such a manner that failure in one-half of the DPDM will not effect the other half of the DPDM.

ENVIRONMENTAL REQUIREMENTS

THERMAL AND ATMOSPHERE

The SSM will operate over a range of -10°C to $+50^{\circ}\text{C}$ and within the humidity limits shown in Figure 12. (However, the feasibility of expanding the temperature range to -34°C to $+71^{\circ}\text{C}$ is to be studied.) The SSM will survive without degradation and without loss of data integrity over the temperature range -40°C to $+85^{\circ}\text{C}$ within the humidity limits of Figure 12. These operational and survival temperature ranges also apply to the SSM in a vacuum environment.

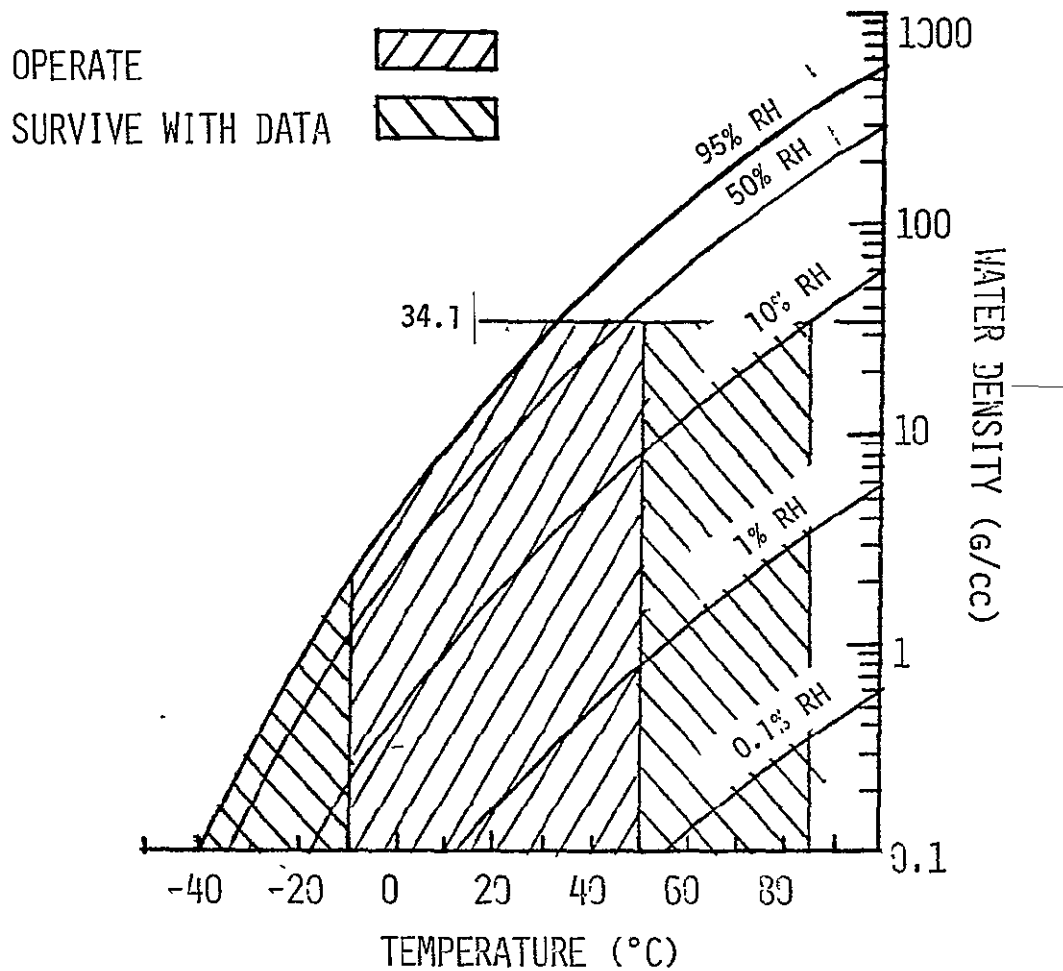


Figure 12. - Operating and Survival Temperature/Humidity Range (Ref. 10)

MECHANICAL

To ensure that the SSM design and workmanship are adequate to withstand the shock and vibration environment to be encountered during spacecraft launch, separation, and deployment, a number of mechanical tests (Refs. 10 and 11) will be imposed. Sinusoidal vibration levels for qualification and flight acceptance testing are given in Tables 3 and 4 respectively. Gaussian random vibration levels for qualification and flight acceptance will correspond to the spectrum analyses of Tables 5 and 6 respectively.

Table 3

Design Qualification Sinusoidal Vibration Requirements

Axis	Frequency	Level
All	5-28	0.50 in. DA
	28 - 100	20 G
	> 100 - 200	15 G

Sweep Rate: 2 octaves/minute

Table 4

Flight Acceptance Sinusoidal Vibration Requirements

Axis	Frequency	Level
All	5-28	0.33 in. DA
	28-100	13.3 G
	100-200	10 G

Sweep Rate: 4 octaves/minute

Table 5

Design Qualification Random Vibration Requirements

Axis	Bandwidth	PSD	Grms
All	20-200	0.17 g^2/Hz	24.4 G
	200-400	+6 dB/oct.	
	400-600	0.70 g^2/Hz	
	600-1200	-6 dB/oct.	
	1200-2000	0.17 g^2/Hz	

Duration: 2 min/axis

Table 6

Flight Acceptance Random Vibration Requirements

Axis	Bandwidth	PSD	Grms
All	20-200	0.075 g^2/Hz	13.2 G
	200-400	+6 dB/oct.	
	400-600	0.31 g^2/Hz	
	600-1200	-6 dB/oct.	
	1200-2000	0.075 g^2/Hz	

Duration: 2 min/axis

A shock transient where positive and negative acceleration shock response spectra satisfy the requirements of Figure 13 for qualification tests and Figure 14 for flight acceptance tests will be applied to the SSM. Accelerations of $\pm 33g$ will be applied to the SSM.

Each type of mechanical test will be applied along each of 3 orthogonal axes and system functional tests will be made during pre-test, test, and post-test periods.

RADIATION

The SSM design will provide no more than 0.5 gram per square centimeter aluminum shielding and system components will be selected to provide the minimum radiation requirements given in Table 7.

Table 7
Minimum Radiation Dose Levels

<u>Subsystem Module</u>	<u>Total Dose of 1 Mev electrons</u>
SSM	100k rad (si)
PSM	100k rad (si)
DCU	50k rad (si)

It is recognized that the minimum dose levels of Table 7 restricts potential military users. Therefore it is a goal of the SSM development program to increase the radiation hardness of the SSM as far as practical consistent with performance requirements and system goals stated previously in this document.

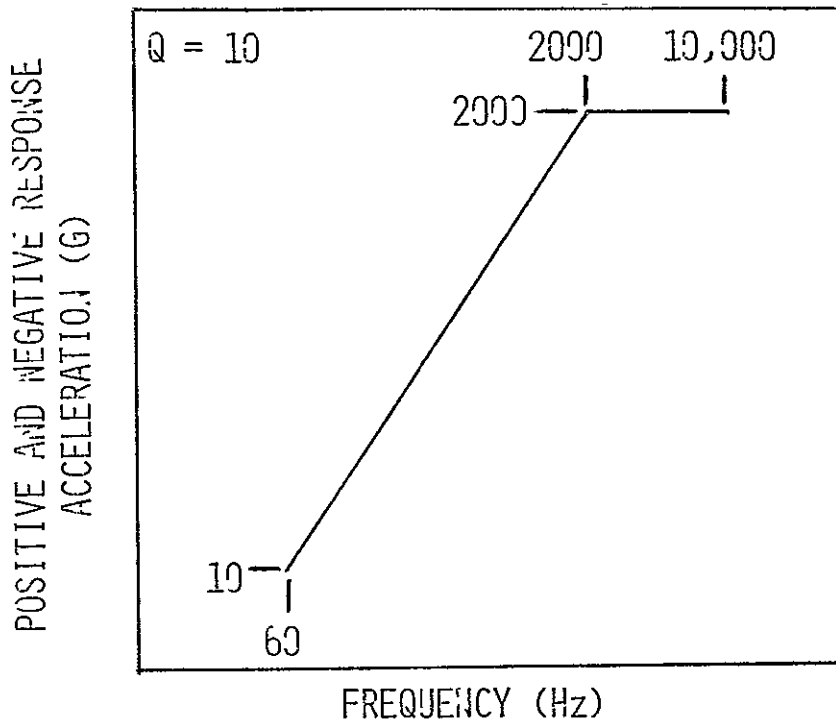


Figure 13. - Design Qualification Mechanical Shock Requirements

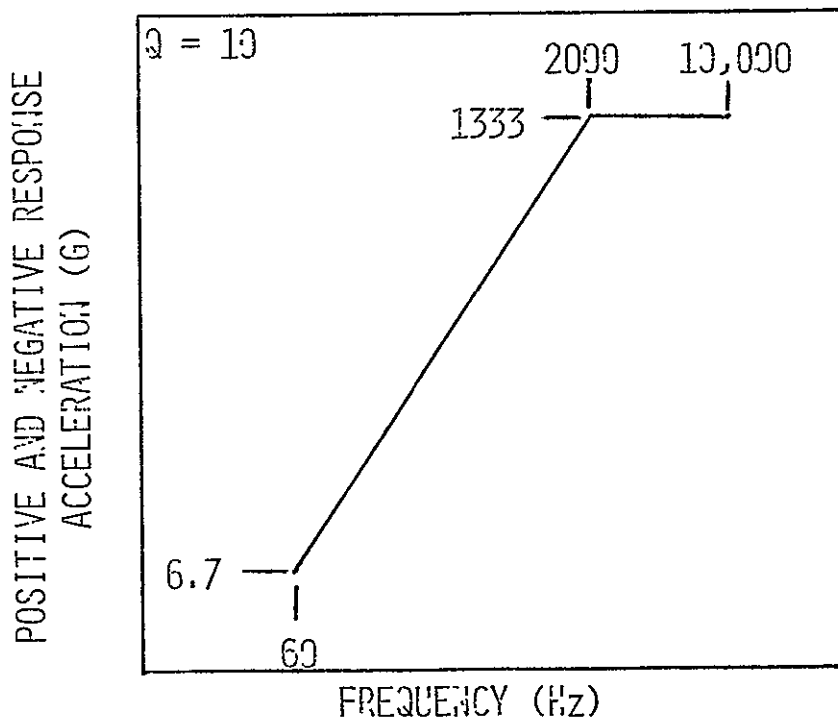


Figure 14. - Flight Acceptance Mechanical Shock Requirements

DC MAGNETIC FIELD

Susceptibility

The SSM will be tested to demonstrate that its performance is not degraded during exposures to ± 10 oersted d.c. magnetic field. The ± 10 oersted field will be applied along three orthogonal axes with one axis being the direction of the cell bias field (six exposures). This test will be applied in both qualification and acceptance tests.

Emission

The SSM will be subjected to magnetic measurements at one meter from the component. These tests are to insure that the component does not generate a magnetic field incompatible with scientific mission objectives. The measurements will be made in a facility with zero tesla background field. The maximum dc and ac stray fields at a distance of one meter will be less than 10 n tesla and 3 n tesla, respectively.

ELECTROMAGNETIC COMPATIBILITY (EMC)

Electromagnetic compatibility (EMC) testing will be done to demonstrate that the SSM will be neither susceptible to, nor a source of electromagnetic interference which could degrade flight performance (Ref. 10). The tests listed in Table 8 will be applied in the qualification of the SSM using the requirements and limits of MIL-STD-461/462.

TABLE 3

EMC REQUIREMENTS

<u>Type</u>	<u>Test No.</u>	<u>Description</u>
Emission	CE01	Conducted (powerline)
	CE03	Conducted (powerline)
	RE02	Radiated (E field)
	RE04	Radiated (H field)
Susceptibility	CS01	Conducted (powerline)
	CS02	Conducted (powerline)
	CS06	Conducted (transient)
	RS03	Radiated (E field)

CONCLUSIONS

A modular memory design has been presented which should facilitate the immediate development of an SSM meeting joint NASA/SAMSO goals. With bubble technology as the storage medium, users are afforded high reliability, radiation hardness, and system versatility in an all solid state concept. The inherent flexibility in the modular design affords adaptability to system needs conceived in the future. In particular, the ability of one or more standard memory modules to be interfaced with custom data control systems could meet many storage needs not yet identified. The DCU is intended to meet the serial data storage requirements identified by the NASA centers and SAMSO.

Finally, this memory design is based on bubble chips in the capacity range of 60k to 100k bits. As chip capacities increase with further maturing of bubble technology, the capacity of the system could be enlarged to meet an even broader range of needs by substitution of higher density chips.

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16 Abstract A preliminary design is presented for a Standard 10^7 Bit Solid State Memory (SSM). The design employs a modular concept with three separate modules roughly separating bubble domain technology, control logic technology, and power supply technology. These modules are respectively the Standard Memory Module (SMM), the Data Control Unit (DCU), and the Power Supply Module (PSM). The storage medium is provided by bubble domain chips organized into memory cells. These cells and the circuitry for parallel data access to the cells make up the SMM. The DCU provides a flexible serial data interface to the SMM. The PSM provides adequate power to enable one DCU and one SMM to operate simultaneously at the maximum data rate. The SSM is designed to handle asynchronous data rates from dc to 1.024 Mbs with a bit error rate less than 1 error in 10^8 bits. Two versions of the SSM, a Serial Data Memory (SDM) and a Dual Parallel Data Memory (DPDM), are specified using the standard modules. The SSM specification includes requirements for radiation hardness, temperature and mechanical environments, dc magnetic field emission and susceptibility, electromagnetic compatibility (EMC), and reliability.					
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