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AUTOMATED ARRAY ASSEMBLY TASK PHASE I

Texas Instruments Report No. 03-77-44

Final Report

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October 1977

JPL Contract No. 954405

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The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DoE.

ABSTRACT

This contract, a subtask of Task 4 of the LSSA Project, consists of an assessment of state-of-the-art technologies that are applicable to silicon solar cell and solar cell module fabrication. The assessment consists of a technical feasibility evaluation and a cost projection for high-volume production of silicon solar cell modules.

The cost projection was approached from two directions: a design-to-cost analysis assigned cost goals to each major process element in the fabrication scheme and a cost analysis built up projected costs for alternate technologies for each process element. A technical evaluation was used in combination with the cost analysis to identify a baseline low-cost process. Since some of the technologies called for in the baseline process are still in a feasibility stage for solar cell fabrication, two alternates to the baseline process were also identified.

A novel approach to metal pattern design based on minimum power loss was developed. These design equations were used as a tool in the evaluation of metallization technologies. The quantitative nature of the design equations provided a solid technical basis for the choice of a metallization technology.

A hermetic module was proposed that has a high probability of meeting the 20-year life goal. Solar cell processing and module fabrication cost projections exceed the 1985 cost goal by only a factor of ≈ 3.

A solar cell process sensitivity study using models, computer calculations, and experimental data was used to identify process step variation and cell output variation correlations. Several in-line test patterns were defined.

A 1982 factory study using $25.00 per kg polycrystalline silicon and Czochralski grown ingots was made. It appears feasible to meet the 1982 selling price goal of $2.00 per watt using a high-efficiency module.

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SECTION I
INTRODUCTION

This is the 1977 Final Report under JPL contract number 954405, a subtask of Task 4 of the Low-Cost Silicon Solar-Cell Array (LSSA) Project. The goal of this study is an assessment of existing process technologies and encapsulation technologies as applied to solar cell module manufacture. From this assessment, low-cost solar cell processes and module configurations shall be proposed.

During this investigation several quantitative and semiquantitative evaluation methods were developed. These evaluation methods were used as tools in the evaluation and choice of process step technologies. The metal pattern design equations developed to minimize power loss in the cell were particularly useful in the evaluation of various options available for front surface metallization.

A large number of solar cell process step alternatives were evaluated from a technical acceptability viewpoint and detailed costing was calculated on technically promising steps assuming a reasonable degree of automation. Using technical and cost criteria, a baseline low-cost solar cell process was proposed. The assessment assumes only evolutionary changes in process technology and does not depend on any technical breakthroughs.

A similar approach to module fabrication led to a technically weighted choice of a higher cost module. The choice was made on the basis of a high probability of meeting the 20-year life goal.

Comparison of projected process and module costs against design-to-cost goals, based on a 1985 price of $0.50 per watt, shows that a cost gap still exists. The gap has been reduced from a factor of 30-50 based on the existing terrestrial solar cell market to a factor of ≈ 3. Improvements in module efficiency coupled with selected cost improvements should allow this gap to be closed.

A solar cell process sensitivity analysis has been made. A combination of derivation, computer analysis, and experimental results has been used to compare process variations to solar cell output characteristics. At least one cell process test device has been identified.

The study of a 1982 factory capable of producing solar cell modules at $2.00 per peak watt has defined a high-efficiency module produced from square solar cells that has the capability of meeting the 1982 selling price goal. A factory size of 25-30 MW per year is required.

SECTION II
TECHNICAL DISCUSSION

A. DESIGN-TO-COST CONCEPT

One of the key uses of the design-to-cost concept is to allocate portions of the total cost to the various process elements so that each process element can be tested against its individual cost goal. In this fashion, key cost barriers can be identified for individual consideration. This evaluation then points the way to the required technical innovation for cost reduction.

The allocation of the total cost to the individual process elements is not an exact science and must be weighted by known factors and engineering judgment. The cost allocations for solar cell module fabrication used in this analysis were arrived at in this fashion. Since solar cell manufacture is a material intensive process, up to 50% of the total cost is allocated to silicon sheet fabrication. Junction formation, metallization, and antireflection (AR) coating are each allocated 10% of the total cost. Module substrate, assembly, and encapsulation are allocated 20% of the total cost. Testing costs must be included with the process element where testing is used and does not represent a separate cost element in this analysis.

The cost goal of the LSSA project is \$500/kW peak power in 1985. An intermediate goal of \$2000/kW peak power can be assigned to the 1980-81 time period.

Manufacturing costs for solar cell modules are a function of the number of units and the area of modules processed and can be related to a cost per watt as shown in equation (1):

$$\text{cost/meter}^2 = (\text{cost/watt})\,(\text{solar flux})\,(\text{conversion efficiency}) \qquad (1)$$

where conversion efficiency = η_M = conversion efficiency of the module. The cost/watt is the project goal of \$500/watt and the solar flux at the earth's surface is taken as 1.00 kW/m^2. Figure 1 is a plot of cost/meters^2 versus conversion efficiency. The left ordinate is scaled to a cost/watt goal of \$500/watt and the right ordinate is scaled to the intermediate cost/watt goal of \$2000/watt.

The allowed cost/meters^2 can be easily read for any given module efficiency, e.g., at $\eta_M = 0.10$ cost/meter^2 = \$50 in 1985. Using the above allocated percentages of the total cost, the data in Table 1 is obtained.

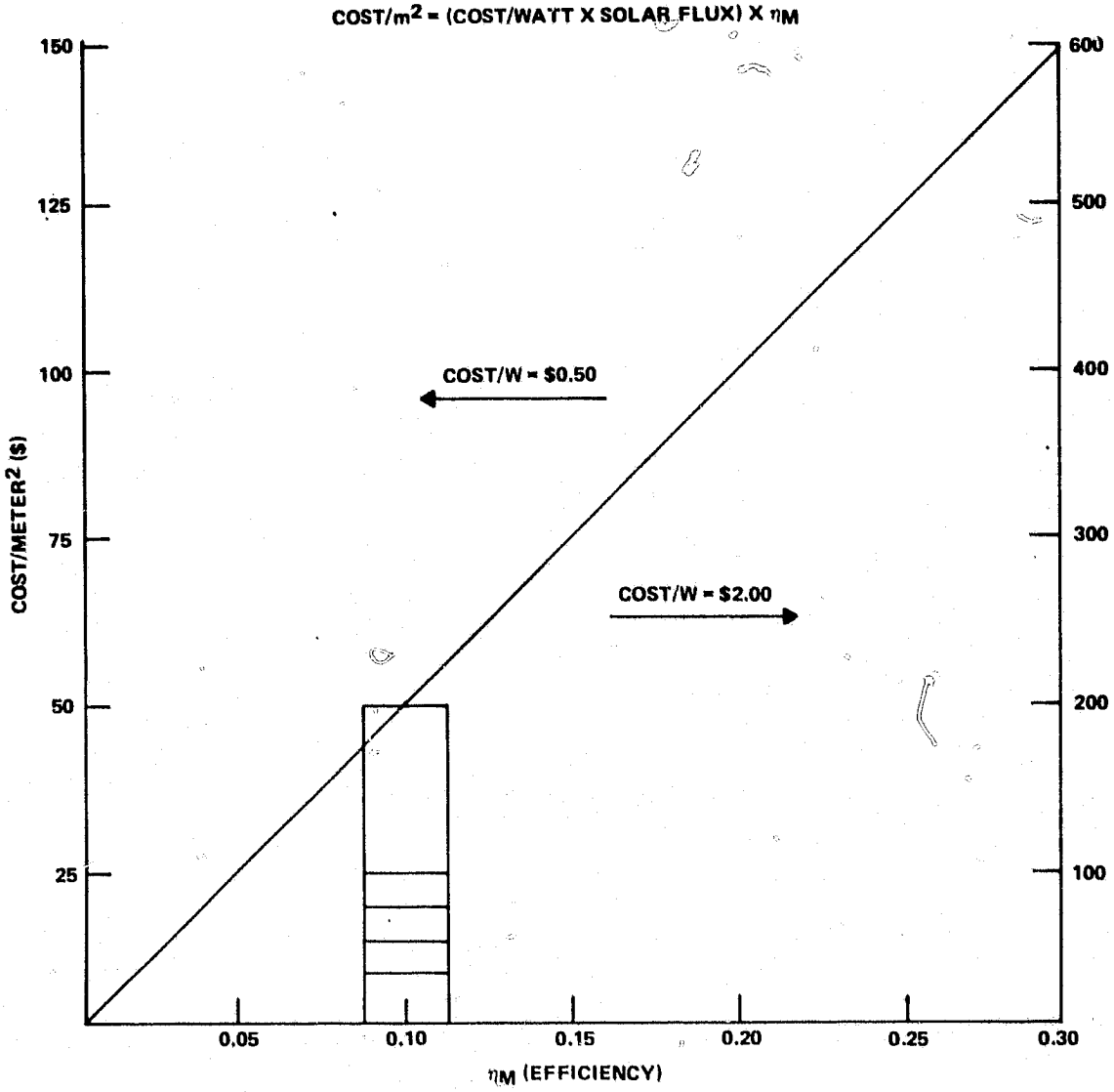


Figure 1. Cost/Unit Area versus Module Efficiency

Table 1. Design-To-Cost Allocation
Cost/Meter^2 (Module)

Si sheet	$25
Junction formation	$ 5
Metallization	$ 5
AR coating	$ 5
Module assembly and encapsulation	$10
Total	$50

The cost of the solar cell manufacture is related to module cost allocation by using the board utilization factor shown graphically in Figure 2. Using a utilization factor of 0.85 for circles or hexagons, the process element costs for cell manufacture given in Table 2 are obtained. The process element costs are for solar cells with a cell efficiency (η) of 11.8% obtained by dividing the module efficiency by the board utilization as in equation (2):

$$\eta = \frac{\eta_M}{B.U.} \tag{2}$$

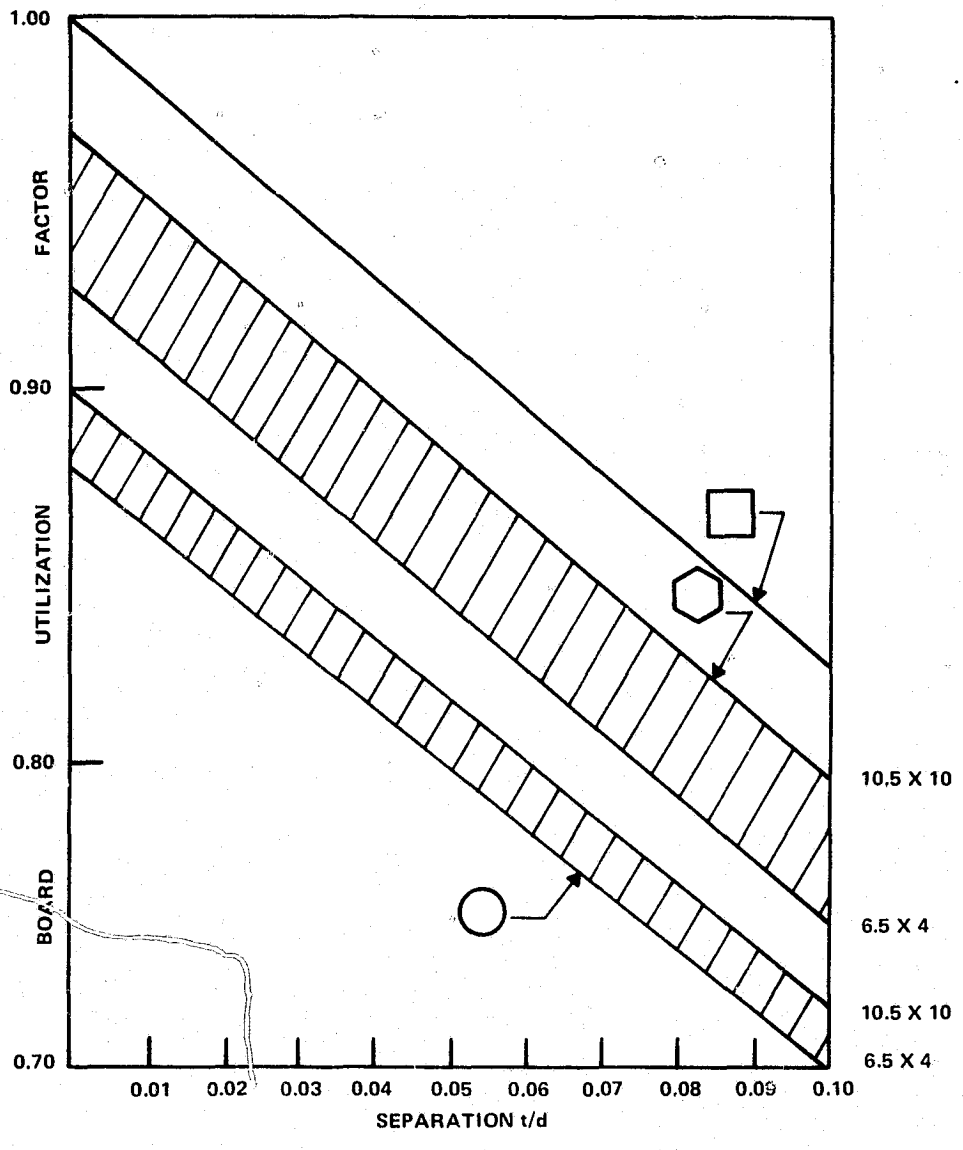


Figure 2. Board Utilization as a Function of Cell Separation

Table 2. Design-To-Cost Goals for Solar Cell Manufacture
Cost/Meter^2 (Cell)

Si sheet	$29.41
Junction formation	5.88
Metallization	5.88
AR coating	5.88
Total	$47.05

Solar cell efficiencies greater than 11.8% would allow corresponding larger cost/meter allocations than those shown in Tables 1 and 2. Single crystal silicon solar cell efficiencies of 15% to 18% in the early 1980s appear to be a reasonable extrapolation from existing technology. Using board utilization of 0.85, this gives an allowable module manufacturing cost per square meter of $64 to $76 to meet the 1985 cost goal of $500/watt peak power.

This analysis can now be used to assess the compatibility of various approaches for each of the module fabrication process elements to the overall cost goal and initial technical confidence (or risk) factors can be assigned. For example, the Si sheet cost goal of $29.41/m^2 for a 10% efficient module compares favorably with the $30/m^2 projection for a semicontinuous Czochralski process.[1] A cell efficiency of 11.8% should be readily achieved leading to a high confidence factor (0.9) that this Si sheet process is compatible with the overall module goal. Other Si sheet processes that had comparable cost projections but lower confidence factors would be higher risk options.

This analysis can also be used to define some limiting criteria (keeping in mind the assumptions included in the analysis). Each process element has a lower limiting value that is finite at any point in time. If it is assumed that the allocated costs for junction formation, metallization, AR coating, and module assembly and encapsulation shown in Table 1 are at the limiting value for 1985, then the cost of the Si sheet is the only cost that varies with module efficiency. Inspection of Figure 1 shows that at $\eta_M = 0.05$, the allowed cost allocation for Si sheet is zero. Therefore, Si sheet processes that inherently yield modules of less than 5% efficiency are unacceptable, and for module efficiencies greater than 5%, a cost allowance derived from Figure 1 must be met, e.g., at $\eta_M = 0.08$, the allowed cost for Si sheet = $15/m^2 (module) or with a board utilization of 0.85, allowed cost for Si sheet = $17.65/m^2(cell).

Another trend that can be derived from this analysis is that cost per area is a function of module efficiency, therefore higher conversion efficiency processes allow higher cost processing. For example, a solar cell fabrication process that yields a value for $\eta = 0.18$ at a board utilization of 0.85 gives $\eta_M = 0.18 \times 0.85 = 0.153$, this gives an allowable module fabrication cost of $76.50.

In summary, the analysis of module efficiency (η_M), cell efficiency (η), board utilization, cost per watt and allowable cost per unit area allow one to test each of the module fabrication process elements, prioritize various options for each process element, and evaluate overall module fabrication processes. As more data and projections become available, optimum processes can be identified.

B. LABOR AND CAPITAL COST MODELING

Direct labor and capital cost for any operation can be calculated from the following parameters:

Operator Hours/Year = OHPY = (work hours/day) (work days/week) (work weeks/year)

Annual Throughput/Machine = ATPM = (machine throughput/hour) (work hours/day) (work days/week) X (work weeks/year) (Utilization factor)

$$\text{Annual Capital Recovery} = \text{ACR} = (\text{capital cost})(\text{interest rate}) \times \left[1 + \frac{1}{(1+R)^N - 1}\right]$$

where

R = interest rate

N = number of years

$$\text{Capital Recovery Factor} = \text{CRF} = (\text{interest rate}) \left[1 + \frac{1}{(1+R)^N - 1}\right]$$

Solar cells will be manufactured in units that will then be assembled into modules. The labor cost per unit (cell, for direct labor, is given in equation (3).

$$\text{Labor Cost/Unit} = \text{LCPU} = \frac{\text{OHPY}}{\text{ATPM}} \times (\text{operator pay/hour}) \times \text{OPM} \qquad (3)$$

where

OPM = (number of operators/machine)

Labor cost per unit is independent of the number of hours worked per year.

Depreciation cost per unit is given in equation (4).

$$\text{Depreciation Cost/Unit} = \text{DCPU} = \frac{\text{ACR}}{\text{ATPM}} \tag{4}$$

Combining equations (3) and (4), an allowable capital cost as a function of DCPU and LCPU [equation (5)] can be derived:

$$\text{Capital Cost} = \text{CC} = \frac{\text{DCPU}}{\text{LCPU}} \text{ X } \frac{\text{OHPY X OPPH}}{\text{CRF}} \text{ X OPM} \tag{5}$$

where OPPH = operator pay/hour.

CRF, OHPY, and operator pay/hour are definable terms that can be evaluated as follows:

CRF (7 yr life, 9% interest) = 0.1987/year

OHPY = (24 hour/day) (7 day/week) (50 week/year)

= 8400 hour/year

Operator pay/hour = \$3.50/hour

Then:

$$\text{Capital Cost} = 147962 \text{ X } \frac{\text{DCPU}}{\text{LCPU}} \text{ X OPM}$$

or (6)

$$\text{Capital Cost/OPM} = 147962 \text{ X } \frac{\text{DCPU}}{\text{LCPU}}$$

Using these relationships and the design-to-cost goals in Table 2, a set of boundary conditions for a solar cell factory that meets the \$500/kW peak power goal can be described.

OPM can be defined as the equipment run by one operator, i.e., OPM = 1, and one square meter of solar cells, independent of the shape or size of the individual cells, is a unit and the utilization factor is 0.80 (allowing 20% of the time for equipment down time, R&M, etc.) (Table 3).

The cost associated with processing one unit is the sum of material, labor, overhead, and depreciation in equation (7).

$$\text{CPU} = \text{MPU} + \text{LCPU} + \text{OH} + \text{DCPU} \tag{7}$$

where

CPU = cost per unit

MPU = material consumed per unit

OH = overhead associated with LCPU

If OH = LCPU, where 50% of the OH is labor associated and 50% is allocated to cover supervisory wages, management costs, building cleaning and maintenance, then equation (7) reduces to:

$$CPU = MPU + LCPU + LCPU + DCPU$$

$$= MPU + 2\ LCPU + DCPU$$

Using the design-to-cost goals and assigning a value of 25% of CPU to MPU, total allowable labor and depreciation costs to a process element in solar cell manufacture, such as metallization, can be defined.

$$\$5.88 = 0.25\ (\$5.88) + 2\ LCPU + DCPU$$

$$\$4.41 = 2\ LCPU + DCPU$$

Substituting this into equation (6)

$$\text{Capital Cost} = \frac{147962 \times 4.41}{LCPU} - 295924 \qquad (8)$$

Table 3. ATPM and LCPU as a Function of Machine Throughput/Hour

Machine Throughput/Hour m^2/hour	ATPM m^2/year	LCPU \$/m^2
1.00	6,720	4.375
2.00	13,440	2.188
3.00	20,160	1.458
4.00	26,880	1.094
5.00	33,660	0.875
6.00	40,320	0.729
7.00	47,040	0.625
8.00	53,760	0.547
9.00	60,480	0.486
10.00	67,200	0.4375

or

$$\text{Capital Cost} = \frac{147962 \text{ X } 2 \text{ X DCPU}}{4.41 - \text{DCPU}} \tag{9}$$

or

$$\text{Capital Cost} = \frac{147962 \text{ X } 4.41}{4.375} \text{ MTPH} - 295924 \tag{10}$$

These equations are plotted in Figures 3, 4, and 5. One interesting observation that is shown in Figure 5 is that for a given set of assumptions, there is a threshold throughput rate below which no capital expenditure will meet the cost goal. Above this threshold, the allowed capital cost is a linear function of the machine throughput rate. For the set of assumptions used in this analysis, the threshold limit for machine throughput is 2 square meters per hour.

The allowed DCPU as a function of MTPH can also be derived from equation (4). This relationship is given in equation (11).

$$\text{DCPU} = \frac{\text{ACR}}{\text{MTPH (work hours/day) (work days/week) (work weeks/year) (utilization factor)}} \tag{11}$$

$$= \frac{\text{ACR}}{\text{MTPH X } 6720}$$

for 7-year depreciation and 9% interest rate ACR = 0.19869 X Capital Cost

$$\text{DCPU} = \frac{\text{Capital Cost}}{\text{MTPH}} \text{ X } \frac{0.19869}{6720}$$

and substituting equation (10):

$$\text{DCPU} = \frac{149145.69 \text{ MTPH} - 295924}{\text{MTPH}} \text{ X} \left(\frac{0.19869}{6720}\right)$$

$$= 4.4098 - \frac{8.7496}{\text{MTPH}}$$

DCPU versus MTPH is plotted in Figure 6.

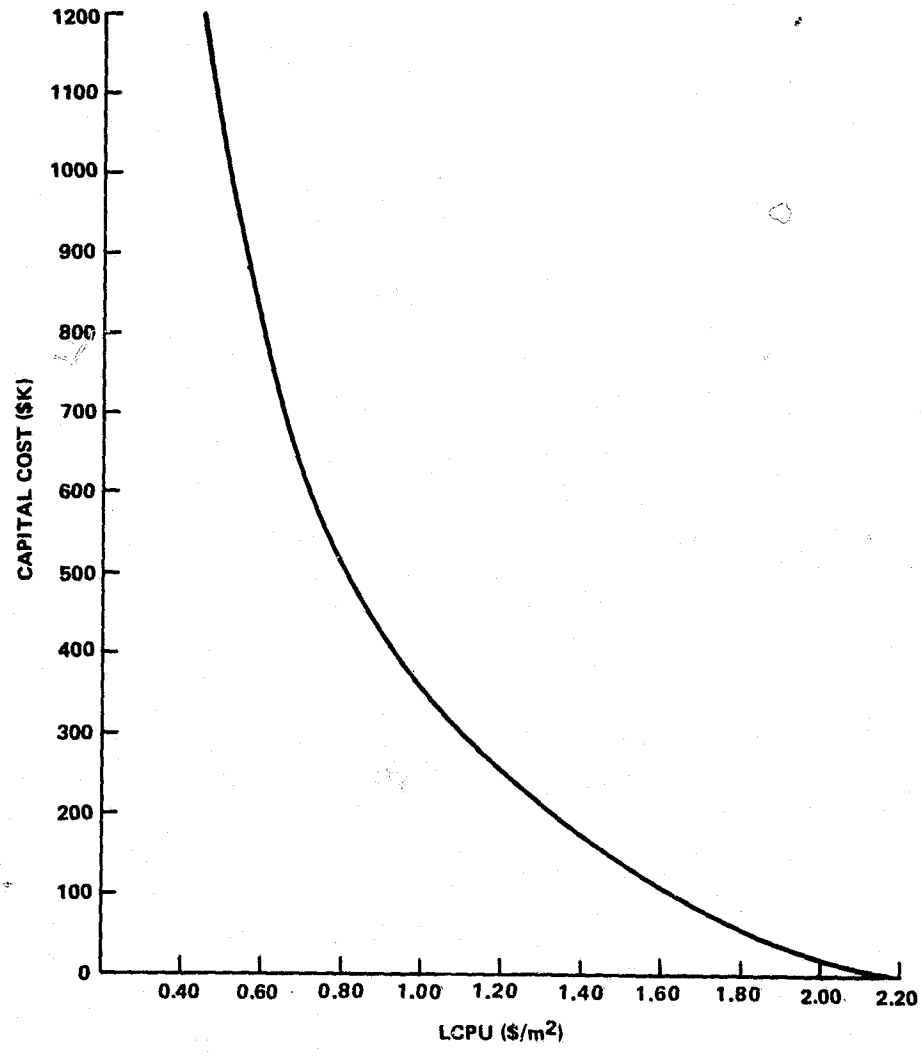


Figure 3. Capital Cost versus LCPU

Similarly, the allowed LCPU can be expressed as a function of MTPH, equation (12) and given in Table 3.

$$\text{LCPU} = \frac{\text{OPPH X OPM}}{\text{MTPH X Utilization Factor}} = \frac{4.375}{\text{MTPH}} \qquad (12)$$

Equation (12) is plotted in Figure 7.

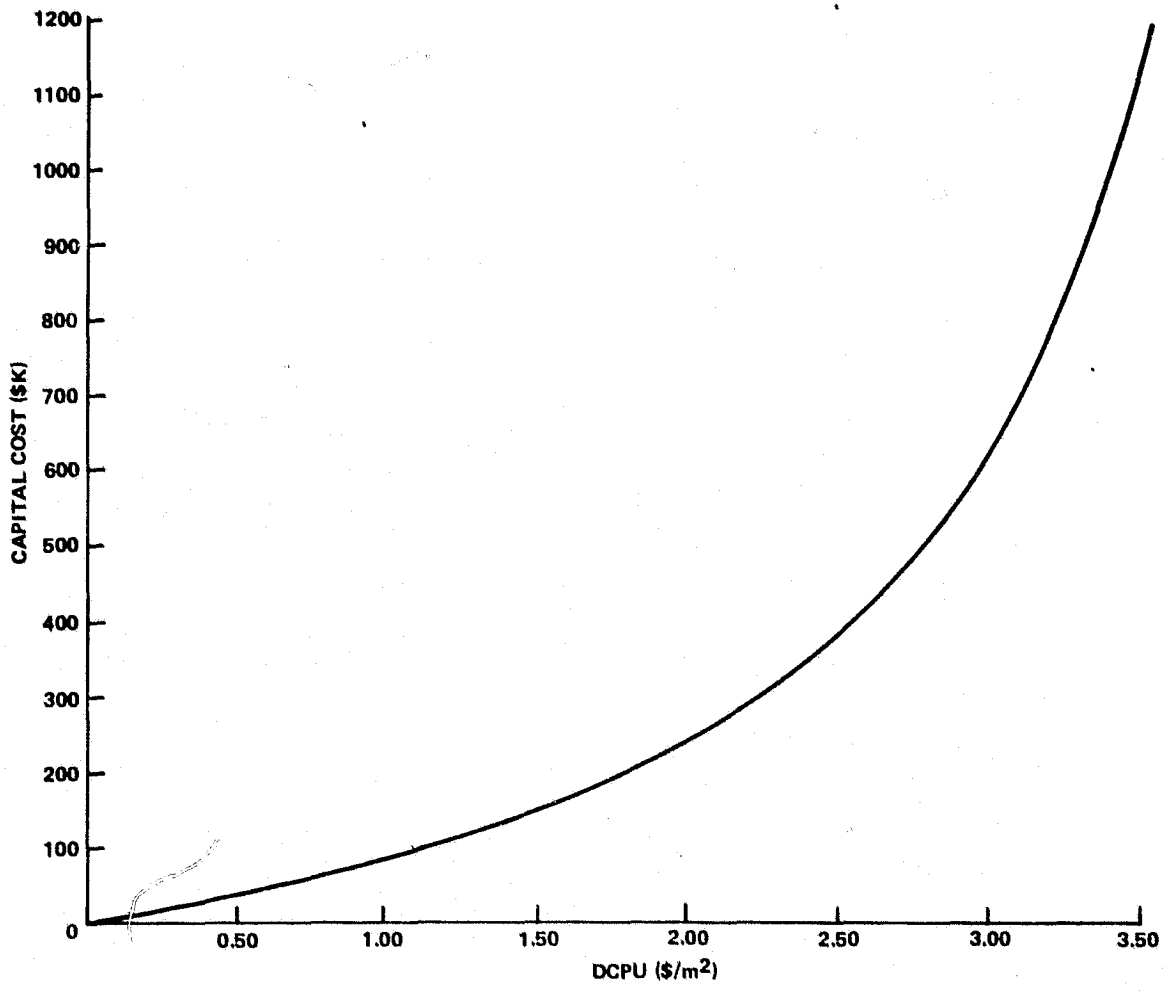


Figure 4. Capital Cost versus DCPU

The key parameter in this analysis is MTPH. For the values used in this design-to-cost simulation, a MTPH threshold of 2 m^2 per hour exists before any capital or depreciation cost can be tolerated. This leads to a description of a model metallization system that will meet the program goals. Table 4 describes this model system.

Any of the parameters in a design-to-cost model can be varied according to engineering judgment within the constraint of the total cost. The most impactive change would be to improve the module efficiency and thereby generate more available cost dollars per square meter.

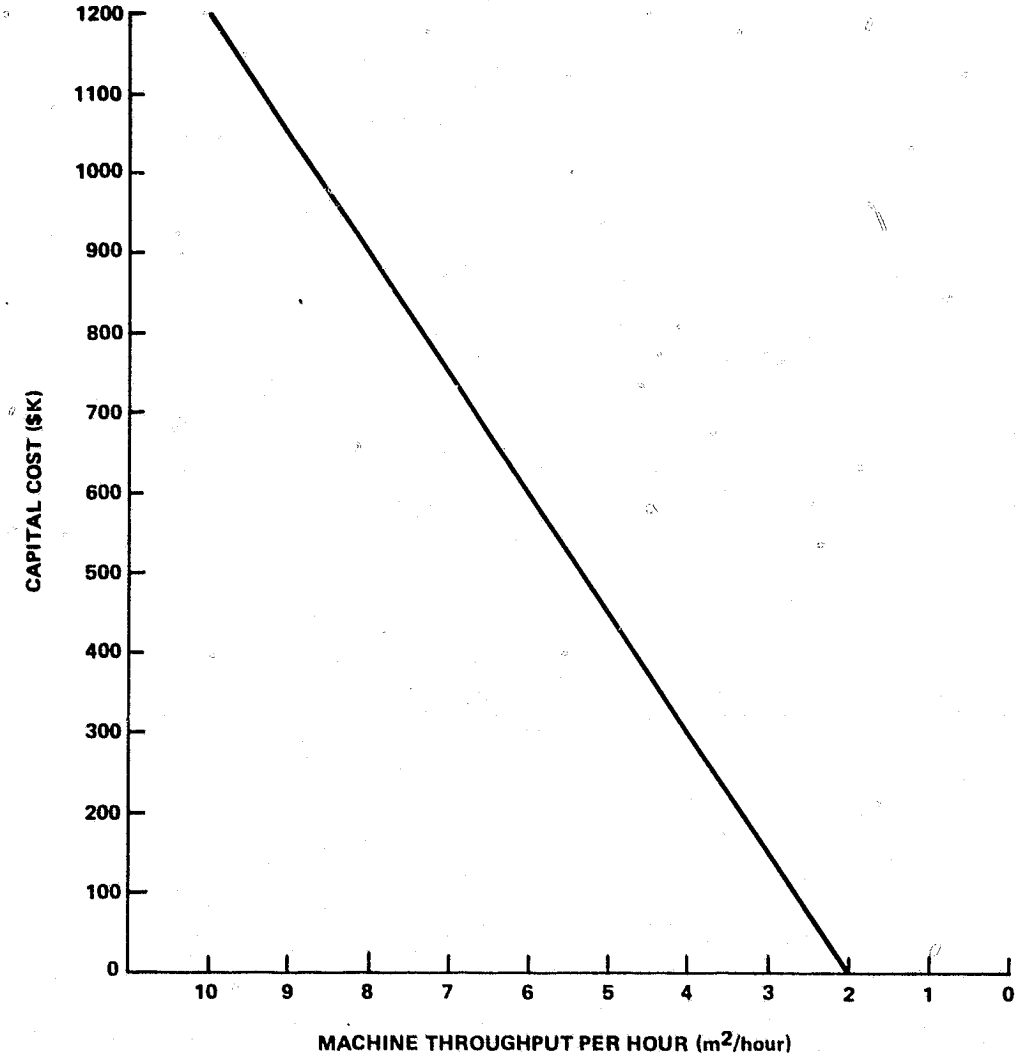


Figure 5. Capital Cost versus Machine Throughput

For purposes of comparison, one can relate square meters of cell to 10.16-cm (4.00 inch) diameter round cells. The area of a 10.16 cm diameter round cell is 81.07 cm^2. This corresponds to 123.4 cells/m^2. Therefore the threshold value of 2 m^2/hour is equivalent to a throughput of 246.7 round cells (10.16-cm diameter) per hour. Table 5 gives the CC, LCPU and DCPU for a metallization module as a function of slice (10.16-cm diameter round cells) throughput per hour.

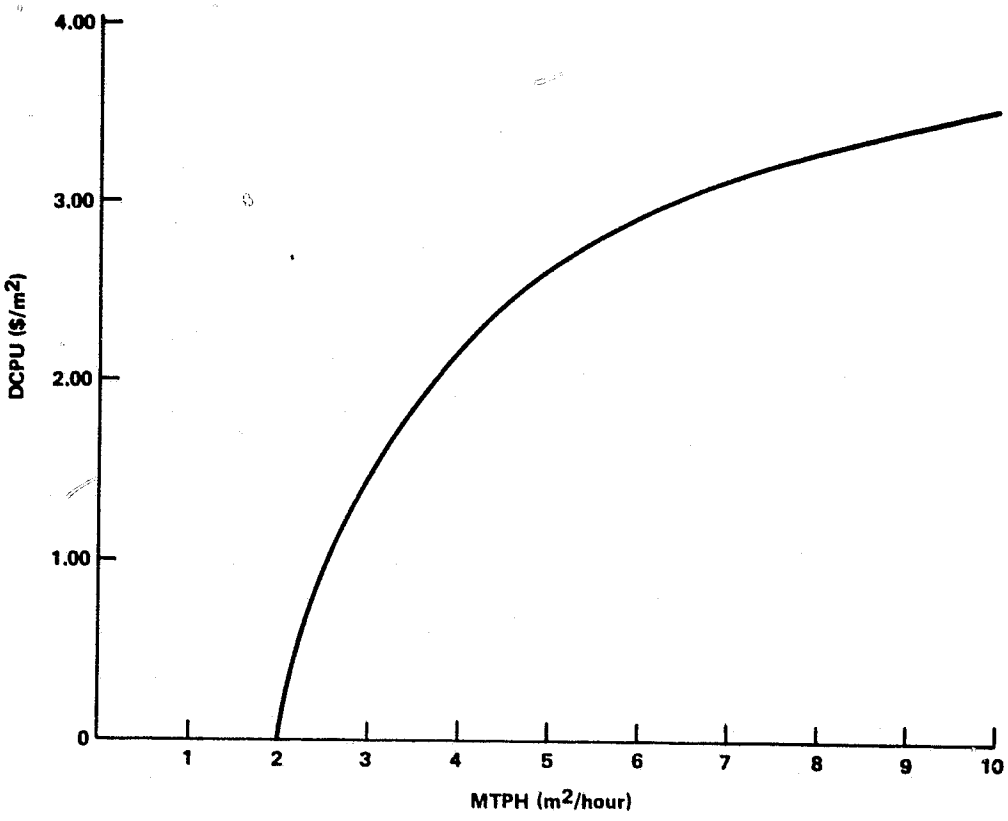


Figure 6. DCPU as a Function of MTPH

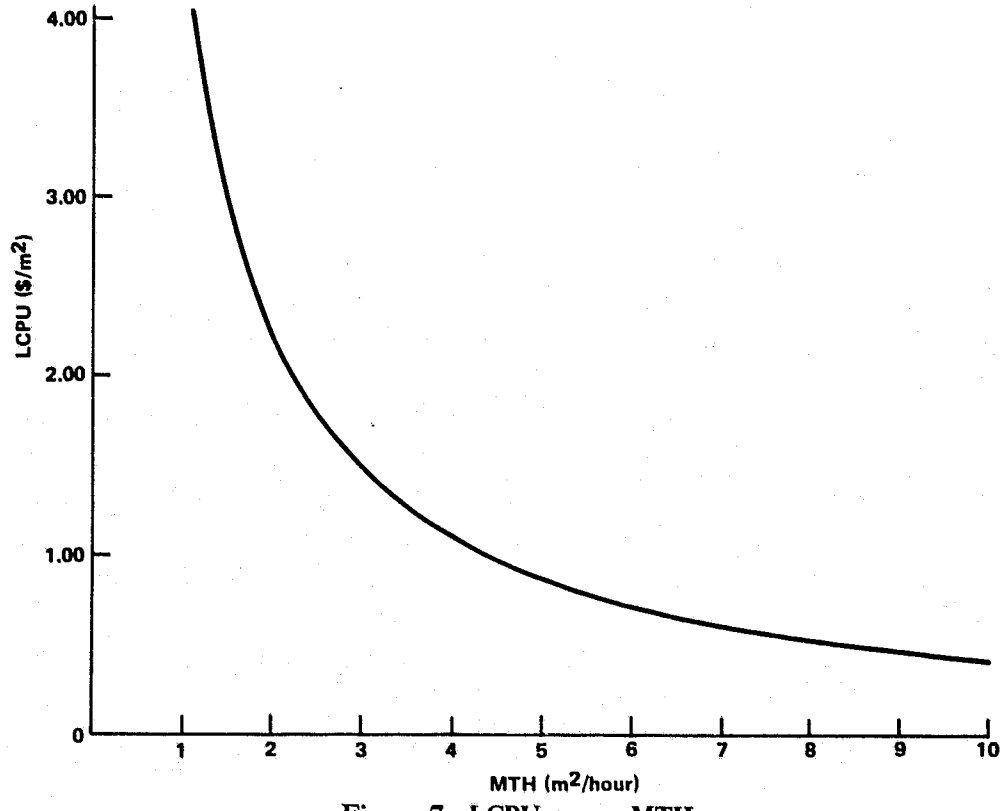


Figure 7. LCPU versus MTH

Table 4. Model Metallization System

OPM	1 technician
OPPH	$3.50/hour
OH	100% of OPPH
CPU	$5.88/m^2
MPU	$1.47/m^2
MTPH	>2 m^2/hour
LCPU	See Figure 7
DCPU	See Figure 6
CC	See Figure 5
Work Year	50 weeks 7 days/week 24 hours/day

Table 5. LCPU, DCPU and CC as a Function of Machine Throughput (10.16 cm diameter slices/hour)

Machine Throughput/Hour (10.16 cm diameter slices)	LCPU $/slice	DCPU $/slice	CC $K
200	.0219	(Below Threshold)	
250	.0175	.0005	2
300	.0146	.0064	65
350	.0125	.0106	125
400	.0109	.0137	185
450	.0097	.0161	245
500	.0088	.0180	305

C. SOLAR CELL DEVICE AND MODULE MODELING

Modeling was used in this study as a tool to define the impact of various parameters on output of solar cells and modules. A simple solar cell model consisting of a current generating source with a diode and a resistor in parallel and a resistor in series was found to be inadequate to describe actual solar cell I-V characteristics. Module modeling was done using a 4 X 4 cell array as a basic unit.

1. Solar Cell Modeling

A solar cell model was developed that includes a light generated current source with two diodes and a resistor in parallel with the current source and a resistor in series with the current source. The two diodes represent an ideal and a nonideal diode. The nonideal diode represents deviations from ideal diode behavior due to various defects or junction edge leakage. The two resistors represent series and shunt resistance in the solar cell. The values of the various components

in the equivalent circuit were varied to attain a "best fit" with actual solar cell characteristics. Figure 8 is a schematic of the equivalent circuit with observed values for the various components of the equivalent circuit for a solar cell with significant deviation from ideal diode behavior.

Families of I-V characteristic curves were generated by fixing the "best fit" model parameters and varying only one parameter. Figure 9 is the family of I-V characteristic curves generated by varying only the series resistance. From this family of curves, a quantitative assessment of the impact of series resistance can be gained. Figure 10 is a plot of maximum power versus series resistance (R_S) for this model. It is evident from an inspection of Figure 10 that series resistance at any level is a source of power loss in a solar cell. The design of an improved solar cell must therefore minimize series resistance in order to minimize power loss.

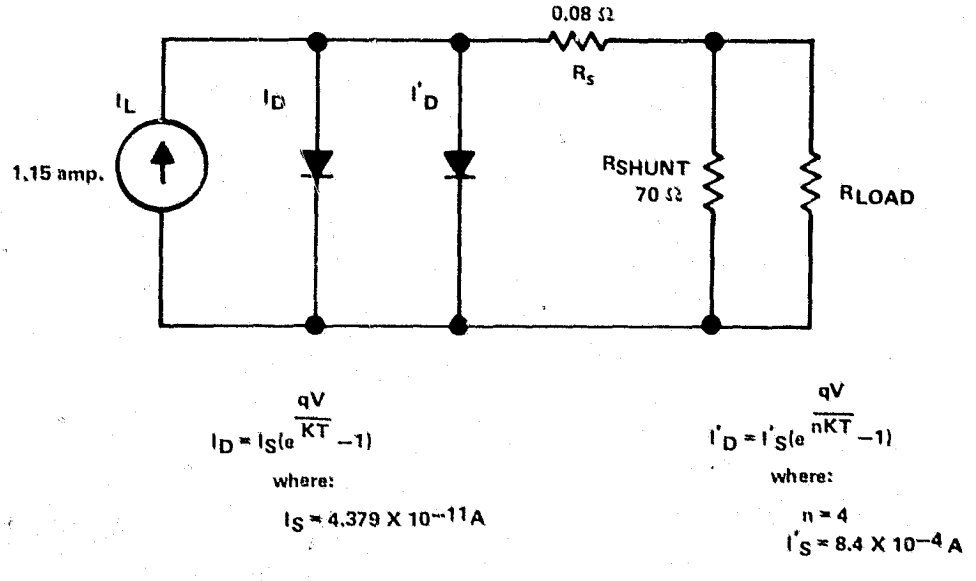


Figure 8. "Best Fit" Model of Actual Solar Cell Characteristics

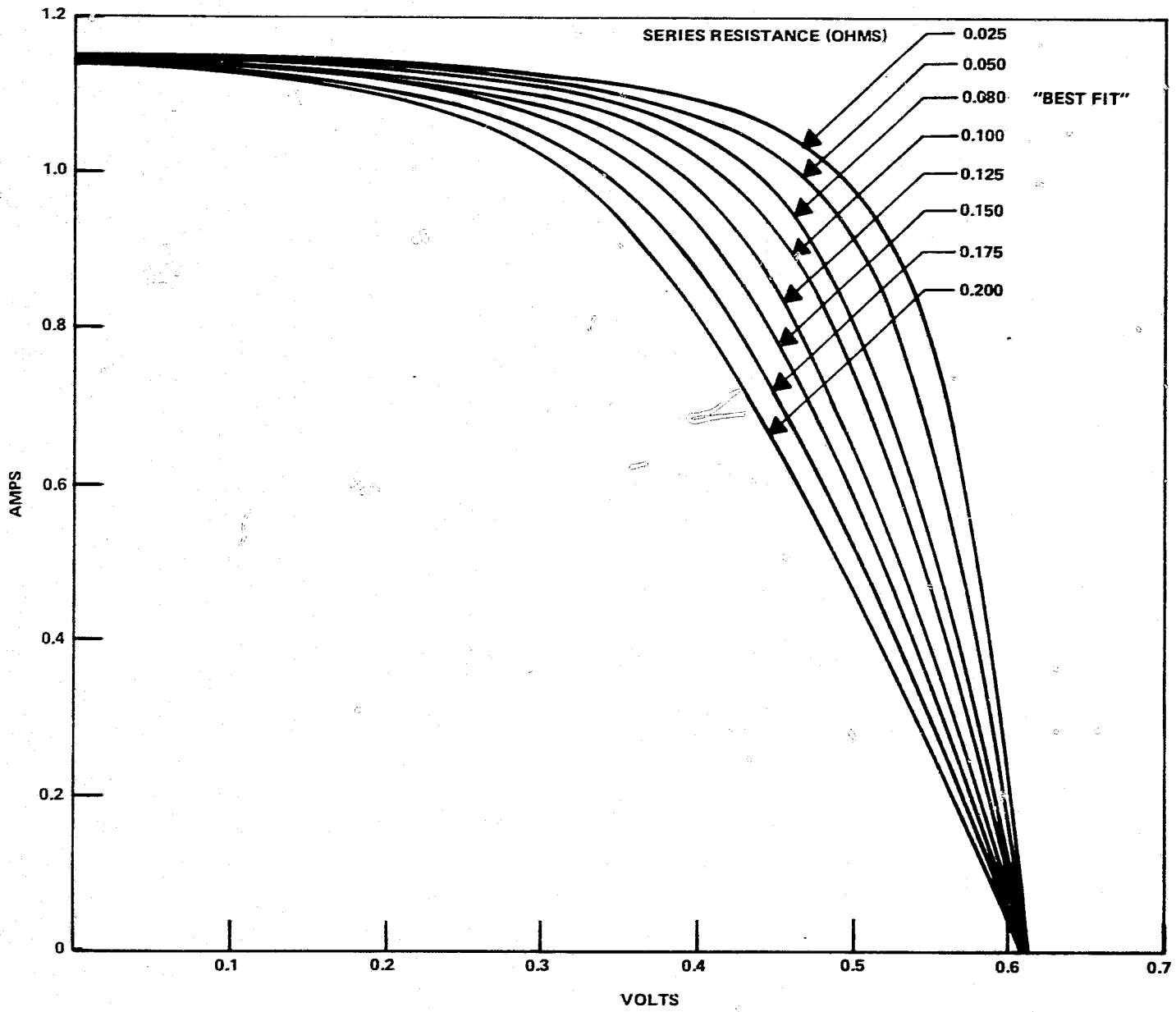


Figure 9. "Best Fit" Model I-V Characteristics with R_S as a Variable

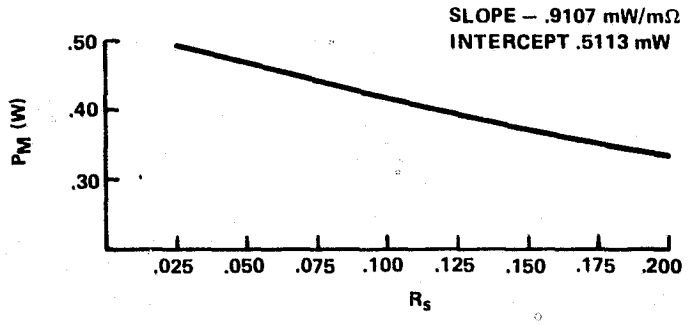


Figure 10. "Best Fit" Model Maximum Power as a Function of Series Resistance

Figure 11 is the family of I-V characteristic curves generated from the "best fit" model by varying only the excess component of current, I_S'. As I_S' increases, the impact on the solar cell performance is very severe. Decreasing values of I_S' give a marked increase in cell efficiency with maximum power going from 0.4373 W at $I_S' = 8.4 \times 10^{-4}$ ampere to 0.4869 at $I_S' = 1.05 \times 10^{-4}$ ampere. Figure 12 is a plot of maximum power (P_M) versus the log of I_S'. From an inspection of Figure 12, it is obvious that excess component of current can cause a very severe degradation in output current. This model data shows the importance of good diode characteristics on solar cell performance. Changes in I_S' over the life of a solar cell caused by improperly passivated junctions can lead to severe degradation of output power. Cell design, cell fabrication, and module fabrication processes must all be optimized to provide stable diode characteristics over the life of a solar cell module. It is also obvious from Figure 12 that improvement in I_S' (to lower values) is only beneficial to a point. For this model, values of I_S' below 10^{-5} ampere give no improvement in output power.

Variations of shunt resistance (R_{SH}) and the value of "n" in the "best fit" model confirm that series resistance (R_S) and nonideal diode characteristics are the key parameters affecting cell efficiency. For 7.6-cm cells, shunt resistance values $\geq$ 70 ohms cause no degradation in cell efficiency – below 70 ohms power output decays.

2. Module Modeling

A model of a 16-cell module was developed using the simple solar cell model shown in Figure 13. The solar cell characteristics are $V_{OC} = 0.55$ V and $I_{SC} = 1.272$ A with an internal resistance of 0.015 Ω. With an optimum load of 0.38 ohm, the series-parallel module would deliver 8.79 W at 4.81 A and 1.83 V if all cells are identical. Figure 14 is a schematic of the balanced array module. The I-V curve for the balanced array module is shown in Figure 15. A computer run with cell 11 generating no photocurrent, $R_L = 0.38$ ohm predicts that the module should deliver 5.52 W at 3.81 A and 1.27 V. With 25% of the module inoperative (one series leg of the 4 X 4 cell module),

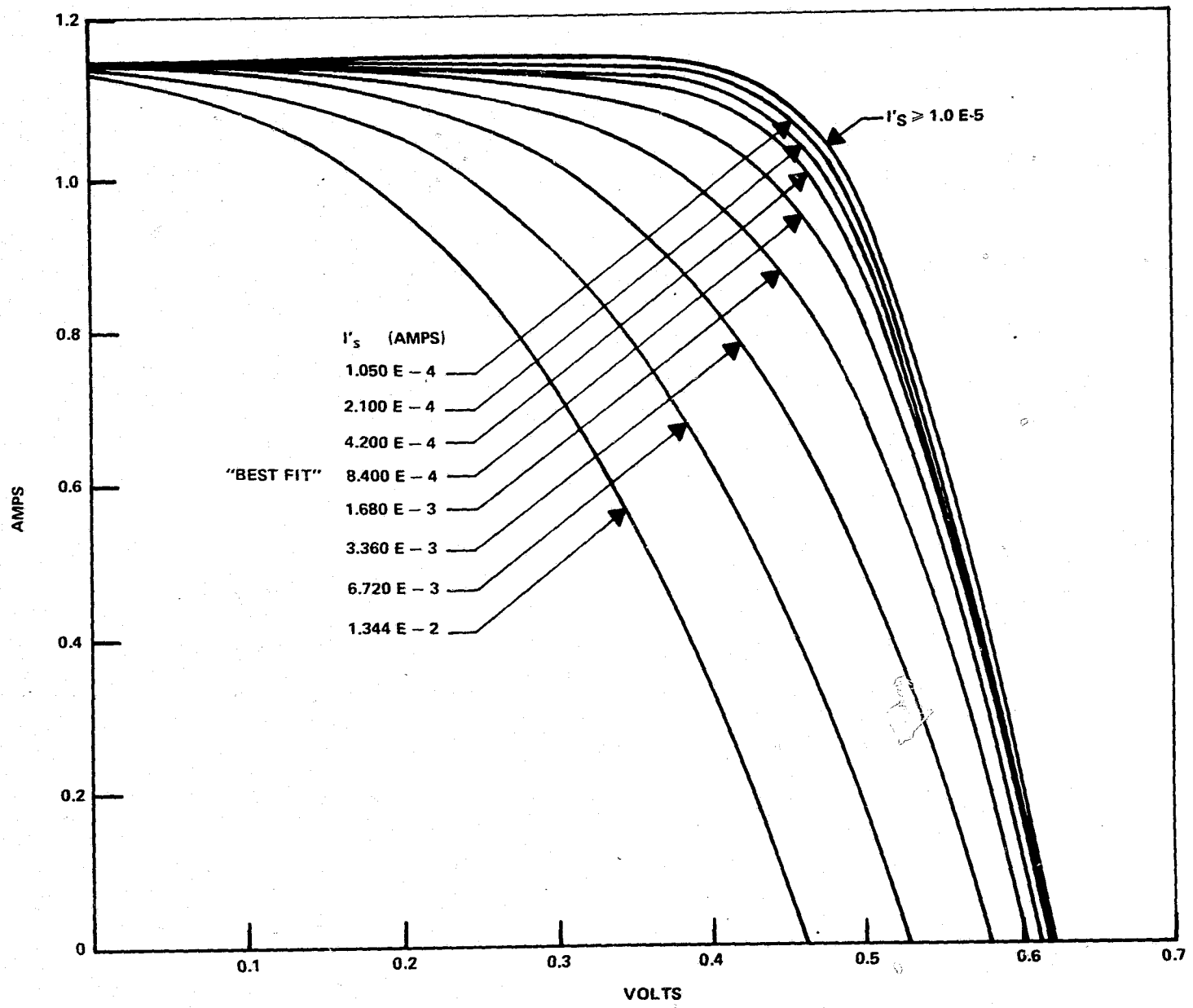


Figure 11. "Best Fit" Model I-V Characteristics with I_S' as the Variable

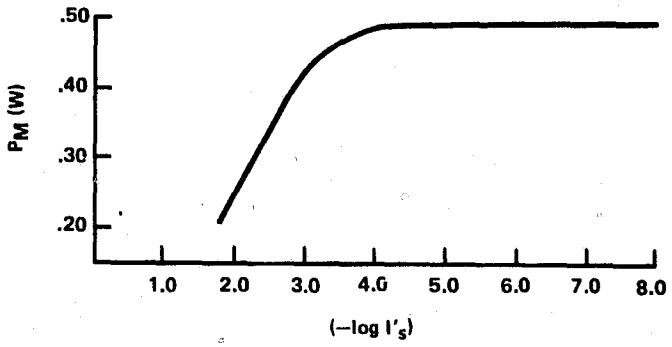


Figure 12. "Best Fit" Model Maximum Power as a Function of Excess Component of Current (I_S')

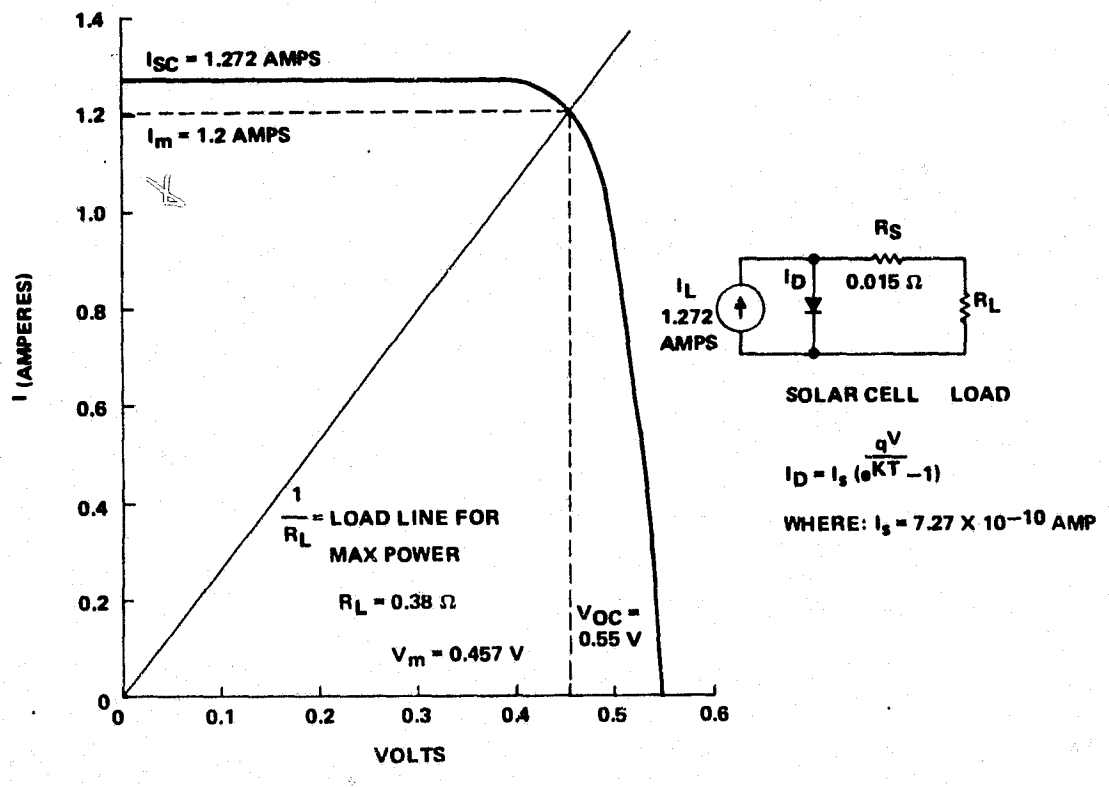


Figure 13. I-V Curve of Computer Modeled 7.6-cm Solar Cell

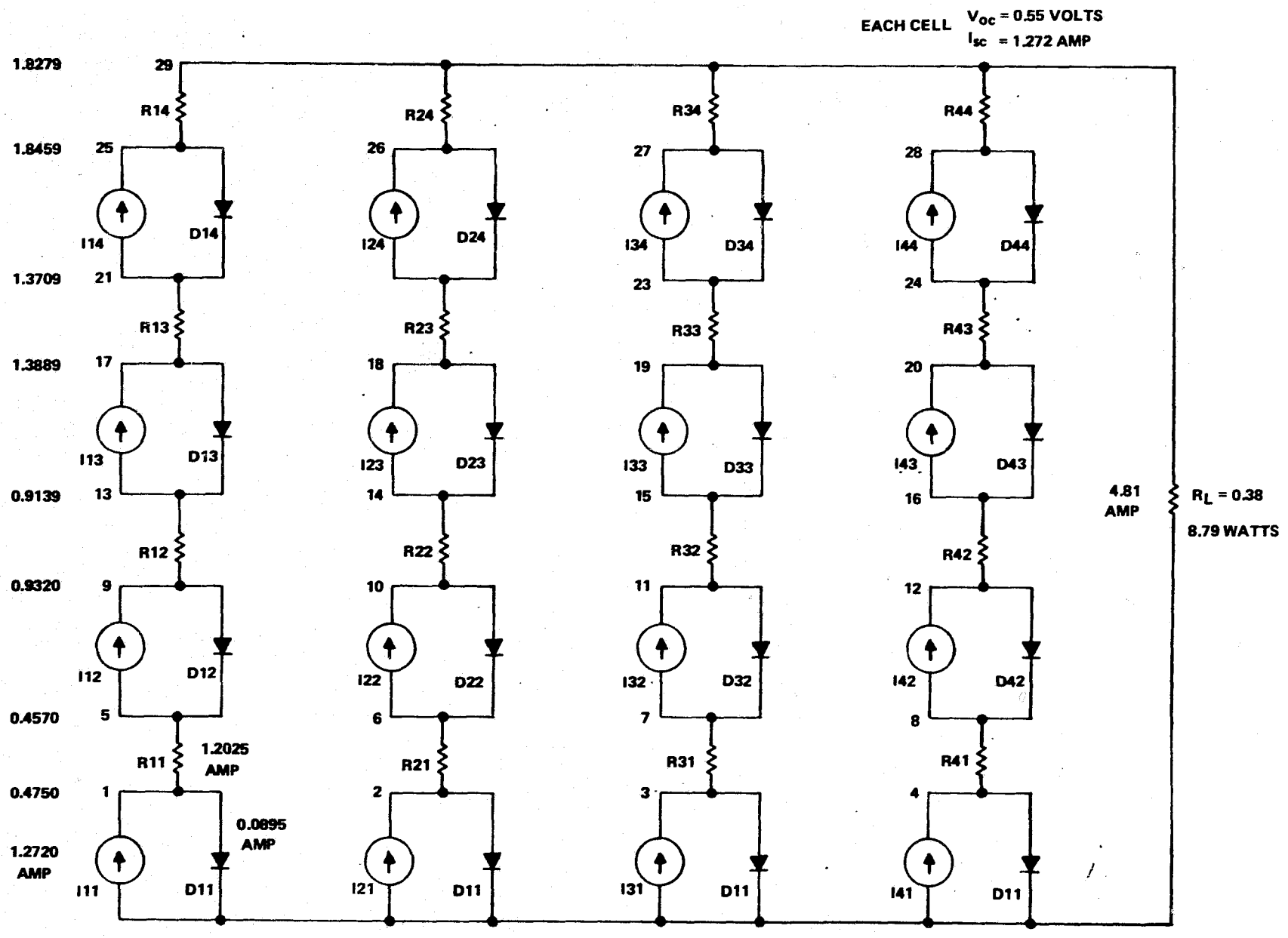


Figure 14. Solar Cell Module Model with Balanced Cells

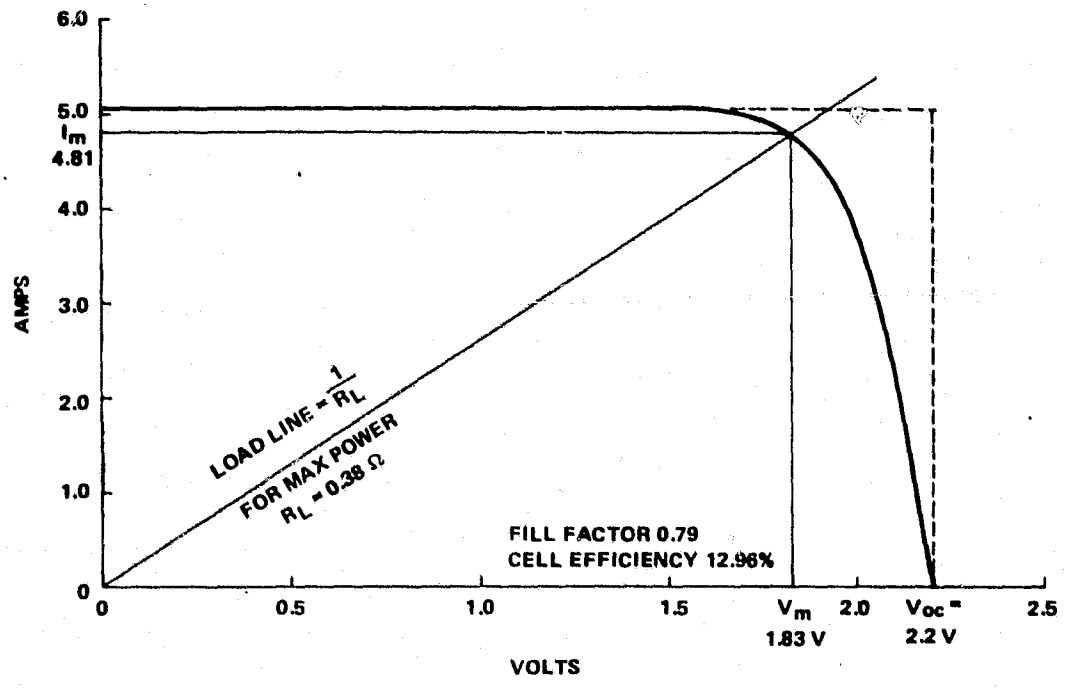


Figure 15. Solar Cell Module I-V Curve from Computer Model

the 3 X 4 portion of the module delivers only 63% of the original power. The 37% power loss due to a 25% loss of active cells is caused by the nonoptimum load conditions for the effective 3 X 4 module. The optimum load resistance for the damaged module would be 0.51 ohm. Figure 16 shows the model schematic for the array with cell 11 inoperative.

Two failure mechanisms have been investigated to date. One cell of the 4 X 4 module model was selected as the failing cell and one of its parameters varied from 0 to 120% nominal value.

The first parameter varied was light generated current. A graph of normalized power output versus I_L of one cell is shown in Figure 17.

The second parameter varied was open circuit voltage. A graph of normalized power output as V_{OC} is varied as shown in Figure 18. A module schematic is shown in Figures 14 and 16. From Figures 17 and 18, a variation of ±10% in V_{OC} or I_{SC} of one cell of a 16-cell module would cause less than a 2% variation in module output power. A variation of ±20% in one cell would cause less than a 5% variation in module output.

Analysis of the 4 X 4 array connected in a parallel-series arrangement instead of a series-parallel gives essentially the same result.

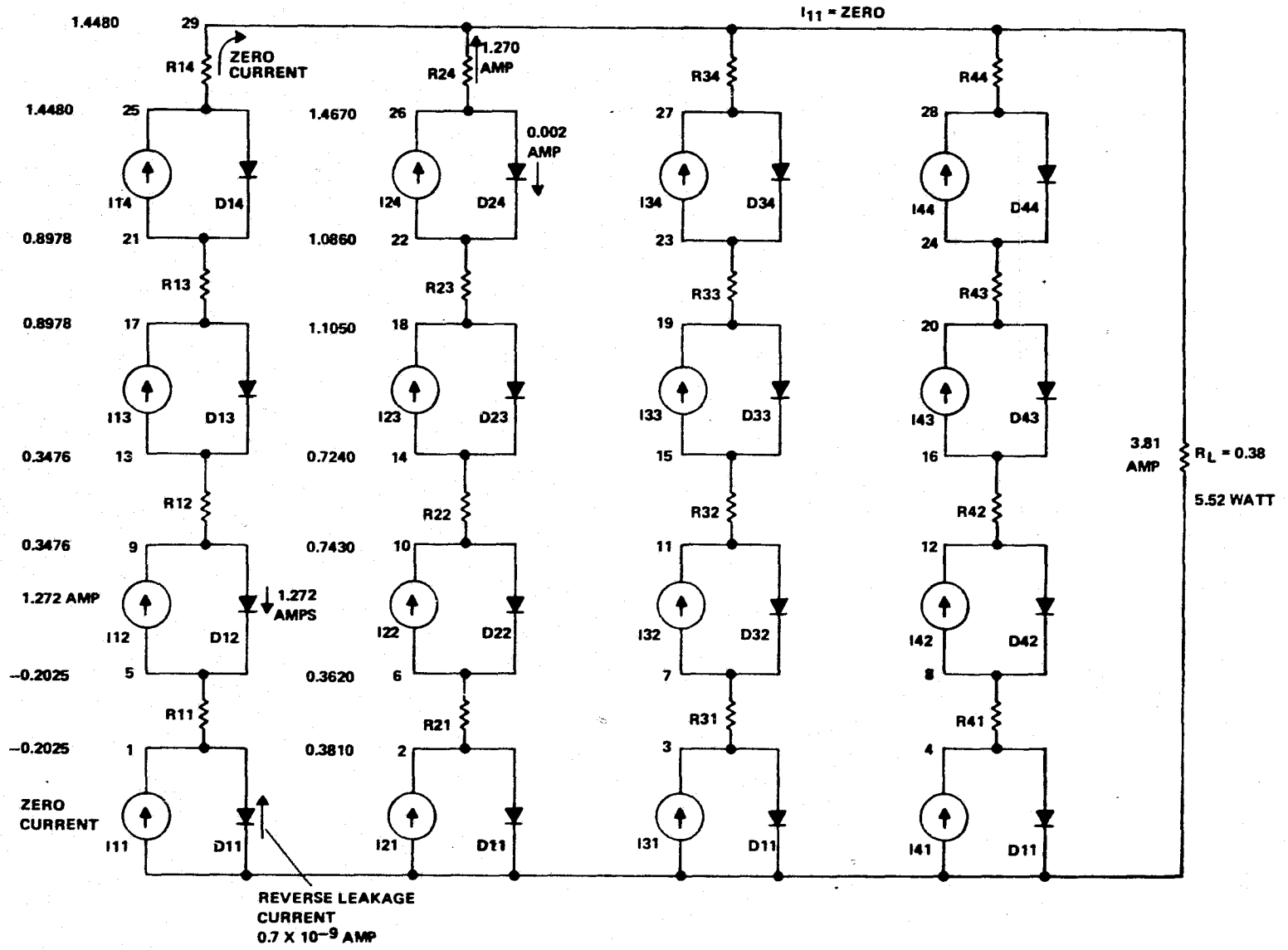


Figure 16. Solar Cell Module Model with One Inoperative Cell

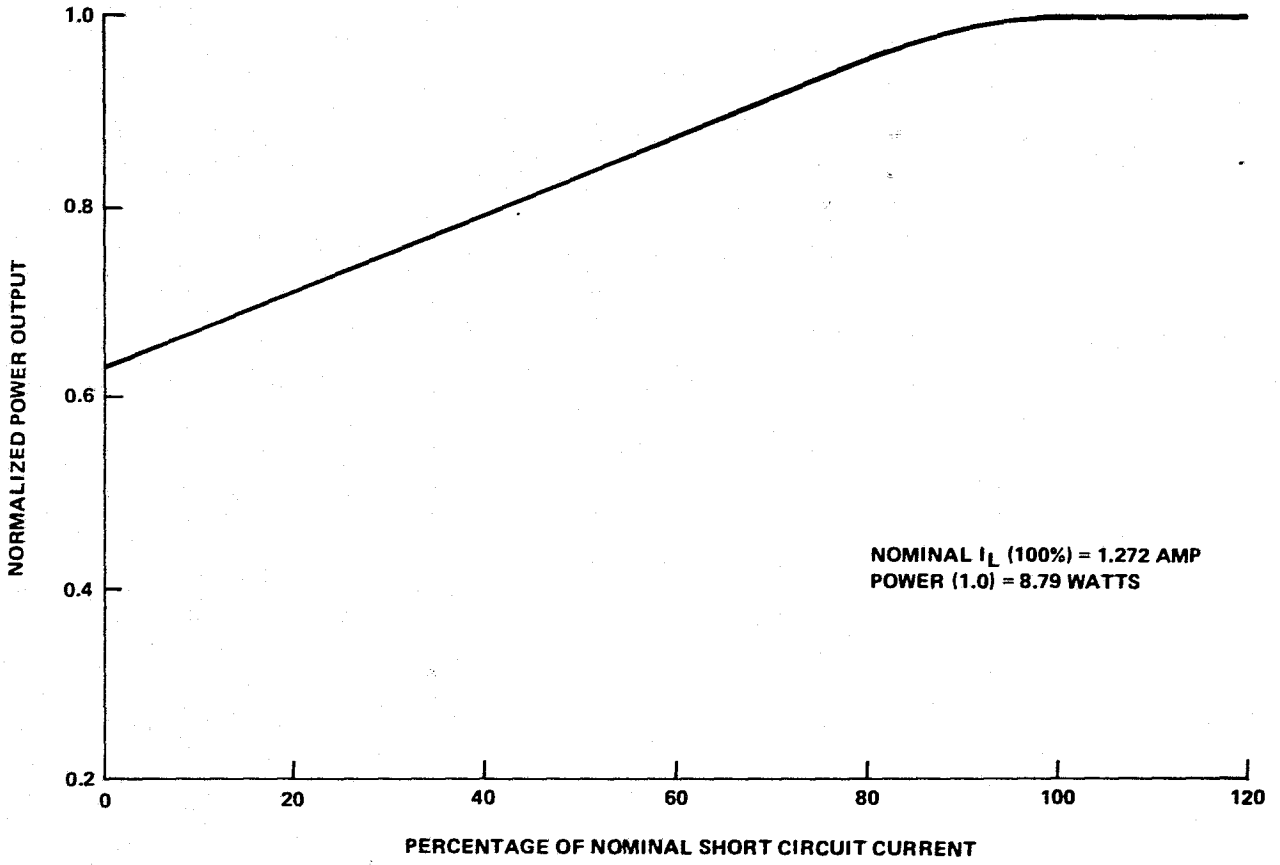


Figure 17. Normalized Power Output of 16-Cell Module as I_L of One Cell Varies

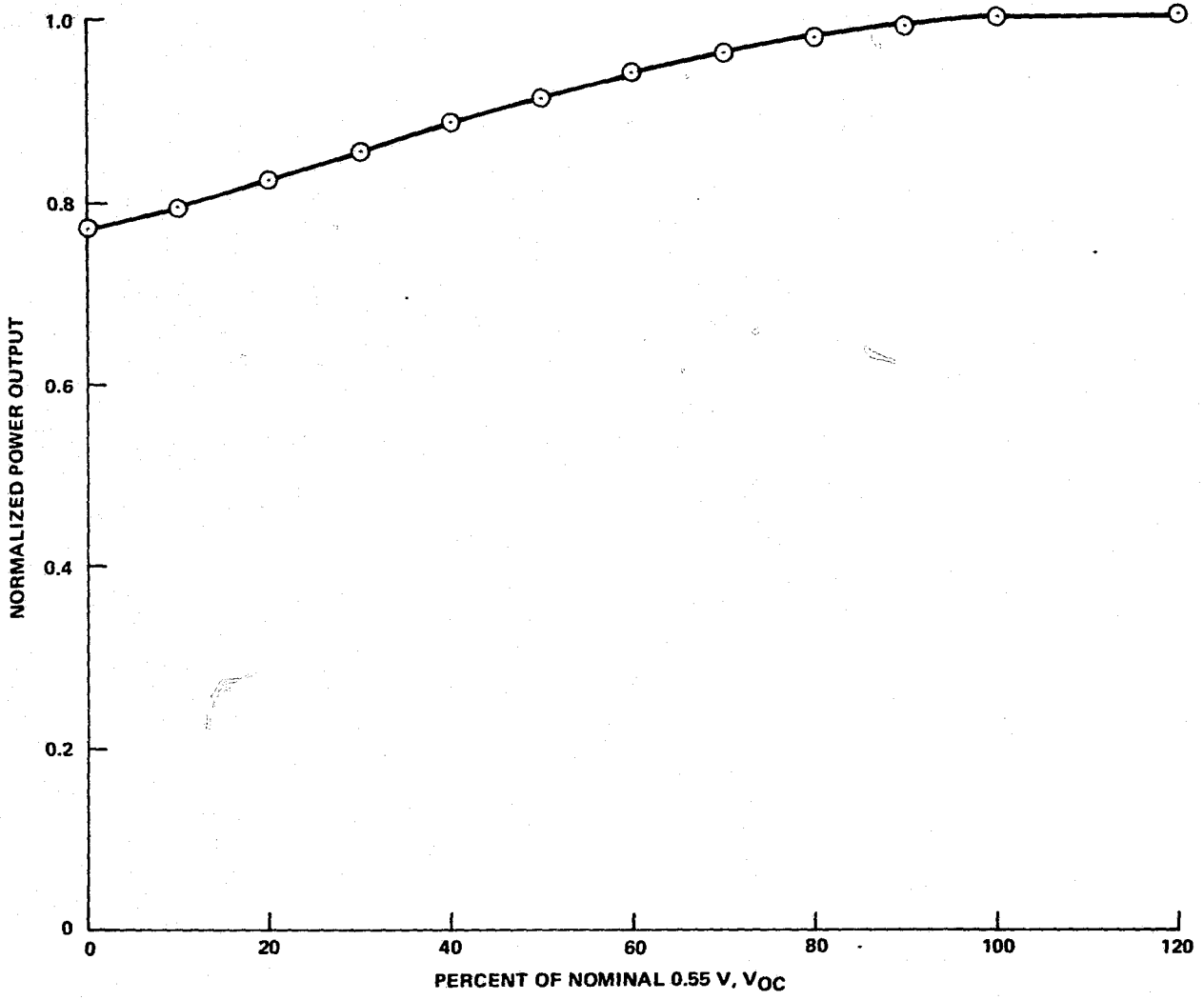


Figure 18. Sixteen-Cell Module V_{OC} of One Cell Varying

D. COMPUTER OPTIMIZATION OF METALLIZATION PATTERN

The LSSA project goal of $500/W for silicon solar cell modules is obviously dependent upon module and cell efficiency. Cost per watt is inversely proportional to efficiency. Therefore a metallization pattern design study was undertaken to define a technique for optimizing the front-side metal pattern as a function of design constraints and as a quantitative tool in the evaluation of metallization process technologies. For example, what is the efficiency impact of using a metallization process technology that can form a metal pattern with a minimum line width of 100 μm? or 10 μm?

1. Scope

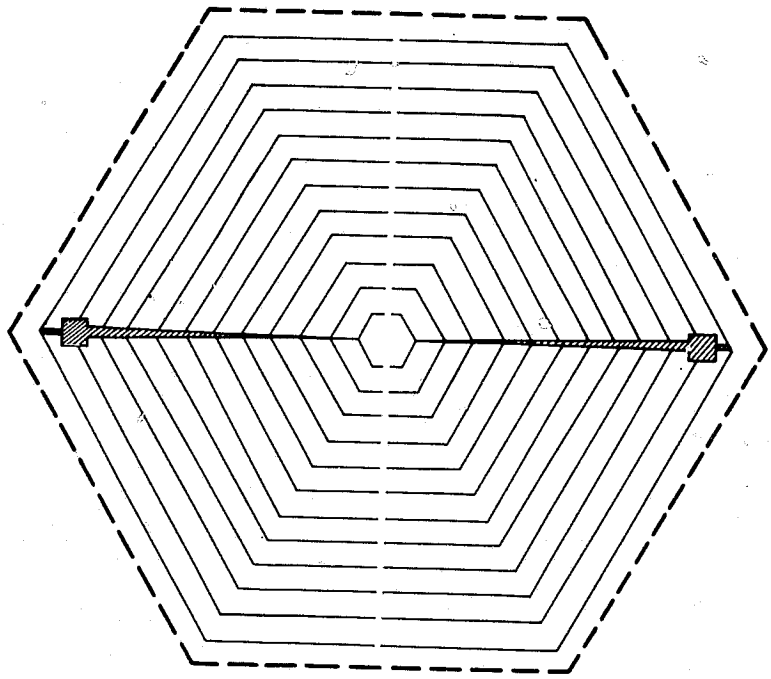
Design of the front surface metallization pattern for solar cells requires a trade-off between resistive power losses and metal shadowing loss. The objective of this part of the program was to provide design data for minimizing the sum of these losses.

The analysis presented here applies primarily to large-area silicon solar cells for terrestrial solar panels. Design constraints have been imposed which are consistent with this application. For example, bond pads are at the cell edge; the number of pads is restricted for compatibility with panel assembly.

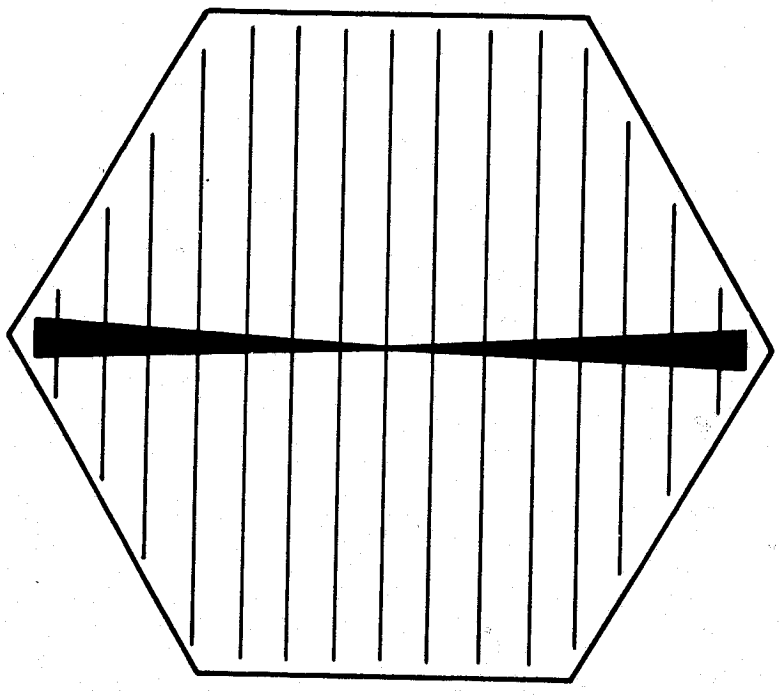
Cell configurations analyzed include hexagonal and rectangular shapes. A computer program was developed to calculate spacing of metal fingers which minimizes the sum of resistive and shadowing losses. Optimum spacing and cell efficiency were calculated for a range of cell sizes and metal finger widths.

The analysis was carried out using representative values of process parameters, assuming AM1 illumination and uniform current density over the cell. Resistive loss in the homogeneous base (1.0 ohm-cm) and contact resistance have been neglected.

Details of the computer program are illustrated first for a hexagonal cell with concentric metal fingers, shown in Figure 19(a). The analysis was also carried out for a hexagonal cell with a "fishbone" pattern and for a rectangular cell. These configurations are shown in Figures 19(b) and 26(a). For the latter two cases, program modifications are discussed and results are shown for comparison to the concentric hexagon.



a. CONCENTRIC HEXAGONAL PATTERN



b. FISHBONE HEXAGONAL PATTERN

Figure 19. Hexagonal Solar Cell Metallization Patterns

2. Concentric Hexagonal Pattern

The concentric metal pattern for the hexagonal cell is shown in Figure 19(a). Current is collected by concentric metal fingers which are connected to the bond pads by tapered metal trunk lines. The metal fingers are parallel and of constant width for a given cell.

Losses associated with the metal fingers are illustrated by the cell segment shown in Figure 20(a). The segment is bounded by the center lines of two metal fingers of width, T, length, L, and spacing, S.

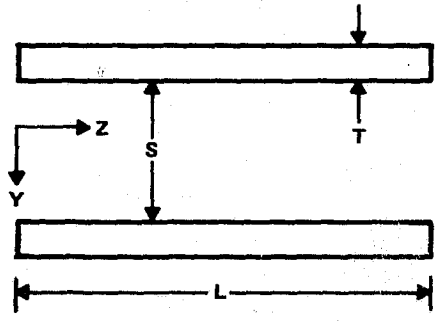
The components of power loss associated with the cell segment are:

1) Resistive loss due to current in the diffused layer

2) Resistive loss in the metal fingers

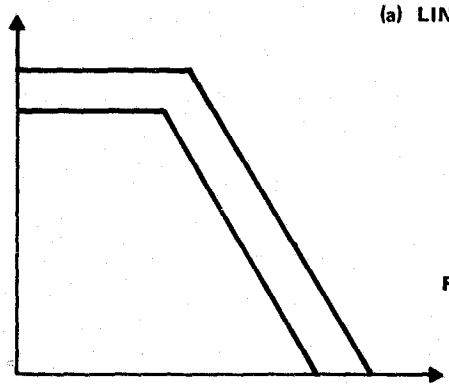
3) Shadowing loss from the metal fingers.

If the finger width, T, is held constant and the spacing, S, is varied, there is a value of S for which the total power loss per unit area of the cell segment is minimized.



LOSS COMPONENT	FRACTIONAL LOSS (POWER LOSS/POWER AVAILABLE)
DIFFUSED RESISTANCE	$a\frac{S^3}{S+T}$
METAL RESISTANCE	$b\frac{L^2S^2}{T(S+T)}$
METAL SHADOWING	$\frac{T}{S+T}$

(a) LINEAR SEGMENT



$$F = a'\frac{S^3}{(S+T)} + b'\frac{X^2S^2}{T(S+T)} + \frac{T}{S+T}$$

(b) HEXAGONAL SEGMENT

Figure 20. Loss Components for Solar Cell

Power loss per unit area is evaluated in terms of fractional loss components. The fractional loss component is defined as

$$F = P_{loss}/P_S \tag{13}$$

where P_{loss} is a power loss component and

$$P_S = (j)\,(V_m)\,(A_S)$$

is the maximum power which can be delivered to the load, assuming no shadowing or resistive losses. In the above expressions, j and V_m are current density and voltage, respectively, at the load for maximum power, and

$$A_S = L\,(S + T)$$

is the area of the cell segment.

Resistive losses in the diffused region and the metal fingers are calculated using a technique similar to other reported work.[2] The interpretation is different, in that power loss is considered rather than voltage drop.

The power loss due to transverse current flow through the diffused region is

$$P_D = 2\int_{y\,0}^{S/2} [i(y)]^2\, dR_D \tag{14}$$

where

$$i(y) = jLy$$

is current flow through the diffused region,

$$dR_D = \rho\,\frac{dy}{L}$$

is the incremental transverse resistance of the diffused region, and ρ is the sheet resistivity of the diffused region. The fractional loss for the diffused region resistance is

$$F_D = \frac{P_D}{P_S} = \frac{1}{12} \frac{j\rho}{V_m} \frac{S^3}{(S+T)} \tag{15}$$

For the resistive loss in the fingers, the fractional loss is

$$F_F = \frac{P_F}{P_S} = \frac{1}{P_S} \int_{Z=0}^{L} [i(Z)]^2 \, d\, R_F \tag{16}$$

where

$$i(Z) = j\, S\, Z$$

is the current in each of the metal fingers and

$$dR_F = \frac{M}{T} d\, Z$$

is the incremental resistance of a metal finger. The sheet resistance of the metal finger is M. In terms of the above equations, the fractional resistive loss in the metal fingers is

$$F_F = \frac{j\, M\, L^2\, S^2}{3\, V_m\, T\, (S+T)} \tag{17}$$

The fractional loss component due to coverage by the metal fingers is

$$F_c = \frac{T}{S+T} \tag{18}$$

A segment for the hexagonal cell is shown in Figure 20(b). The length of the segment is $L = 1.5\, X$ where X is the distance along a major diagonal from the center of the hexagon. The sum of the loss factors for the hexagonal segment is

$$F_S = \frac{a'\, S^3}{S+T} + \frac{b'}{(S+T)} \frac{X^2\, S^2}{T} + \frac{T}{S+T} \tag{19}$$

where

$$a' = \frac{1}{12}\,\frac{j\rho}{V_m}$$

and

$$b' = \frac{3}{4}\,\frac{jM}{V_m}$$

It is seen from the above equation that F_S will have a minimum which depends upon the values of S, X, and T. For a constant value of T, the optimum value of S will vary with X.

The optimum value of S might be determined analytically by differentiating F_S with respect to S and solving a cubic equation for S as a function of T and X. The alternative approach taken here was to use a computer program to calculate and minimize the sum of the fractional loss components for each cell segment.

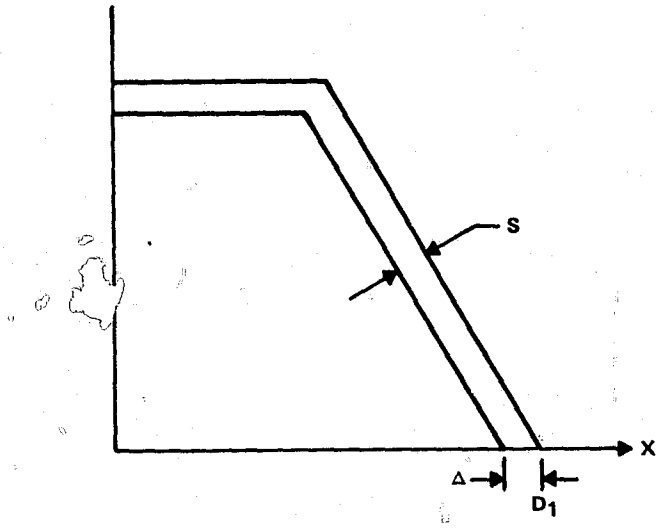
A computer program was developed which determines optimum spacing of metal fingers of a hexagonal cell as a function of distance from the center and finger width. Additionally, the program calculates power loss components for this optimized spacing from which metal-shadowing efficiency and series-resistance efficiency are determined.

The technique used for the computer analysis is illustrated in Figure 21(a). Fractional loss components are calculated for a segment at the cell periphery. The width S of the segment is varied by incrementing Δ along the x-axis. Losses are calculated initially for a small value of Δ; calculations are repeated for successive values of Δ, as Δ is increased by small increments. The first value of Δ which causes the sum of the three fractional loss components to increase is selected as the optimum value, Δ_{opt}, for the initial value of $X(X = D_1)$; i.e., the optimum spacing is given by

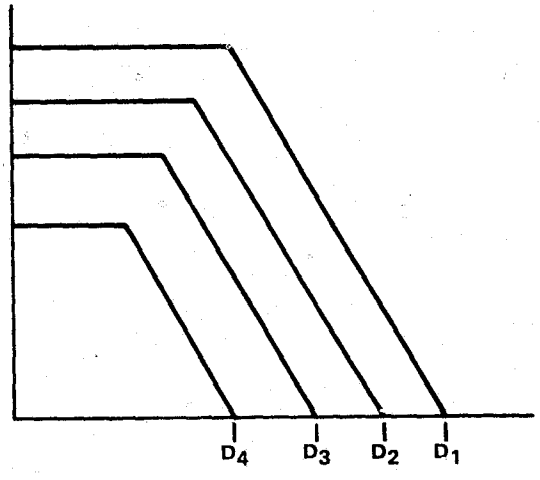
$$S + T = \Delta_{opt}\,(\cos 30^\circ) \tag{20}$$

As shown in Figure 21(b), the first hexagonal segment is then defined by D_1 and D_2 where

$$D_2 = D_1 - \Delta_{opt} \tag{21}$$



(a) INITIAL SEGMENT



(b) SUCCESSION OF SEGMENTS

Figure 21. Hexagonal Segments Used in Computer Analysis

Successive hexagonal segments are determined by repeating the procedure until $D_n \leq 0$. The metal fingers in each case are located midway between the values of D_n and D_{n-1}.

The above procedure was used to determine optimum spacing as a function of distance from the center of a hexagon. This data is shown in Figure 22 for a range of values of metal finger width.

Losses for the trunk line were also calculated by the computer program. The configuration of the trunk lines is shown in Figure 19(a). Current from the fingers is carried by the trunk lines to the bond pads located at the outer edge of the trunk lines. The trunk configuration was designed to minimize the sum of resistive and shadowing losses.

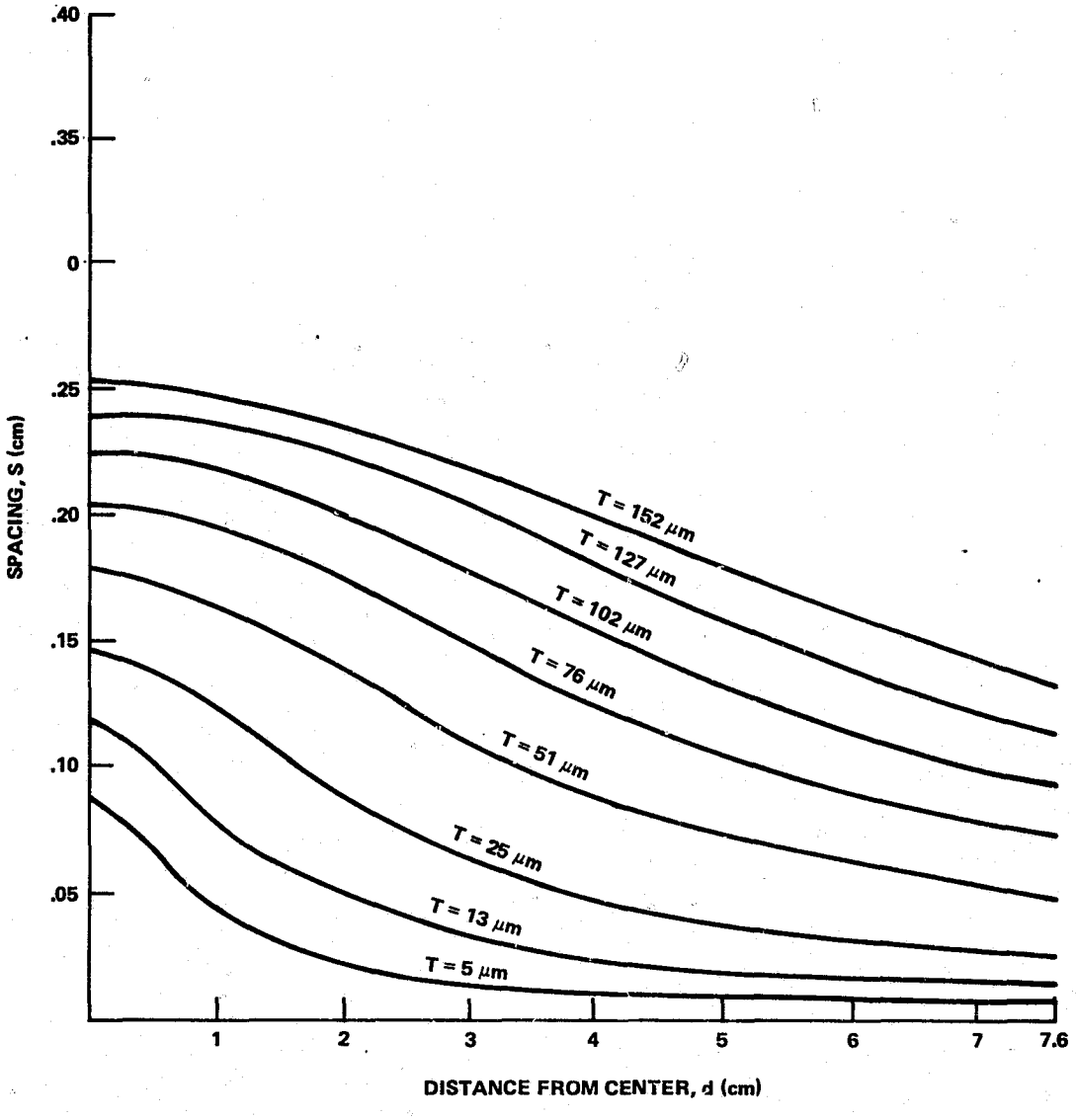


Figure 22. Optimum Metal Line Spacing versus Distance from Center as a Function of Metal Line Width for Hexagonal Solar Cells

The current in each trunk line as a function of distance, X, from the center of the hexagon is

$$i(x) = \frac{3\sqrt{3}}{4} X^2 j \tag{22}$$

where j is the current density. The incremental resistance of the trunk line is

$$d R = \frac{M}{T_T (x)} d x \tag{23}$$

where M is the sheet resistance of the metal, and the width of the trunk line is assumed to increase with X according to the relationship

$$T_T(x) = K X^n.$$

The resistive power loss in each trunkline is

$$P_{RT} = \int_o^D [i(x)]^2 \, dR \qquad (24)$$

$$= \frac{27}{16} \frac{M}{K} j^2 \frac{D^{(S-n)}}{(5-n)}$$

where $D = (DIAG)/2$

and (DIAG) is the major diagonal.

The power loss due to metal coverage for each trunk line is

$$P_{CT} = \int_o^D K x^n \, dx \qquad (25)$$

$$= \frac{KD^{(n+1)}}{n+1}$$

The fractional resistive loss component is

$$F_{RT} = \frac{2 P_{RT}}{P_A} \qquad (26)$$

where P_A, the total available power is

$$P_A = A_T \cdot V_m \cdot j \qquad (27)$$

and

$$A_T = \frac{3\sqrt{3}}{8} (DIAG)^2 \qquad (28)$$

is the area of the hexagon. From the above equations

$$F_{RT} = \frac{3\sqrt{3}}{4\,(5-n)}\ \frac{Mj}{K}\ \frac{D^{(3-n)}}{V_m} \tag{29}$$

The fractional loss due to metal coverage is

$$F_{cT} = \frac{2\,P_{cT}}{A_T} \tag{30}$$

$$= \frac{4}{3\sqrt{3}}\ \frac{K\,D^{(n-1)}}{(n+1)}$$

The sum of the fractional loss components for the trunk,

$$F_{RT} + F_{cT} = \frac{3\sqrt{3}}{4\,(5-n)}\ \frac{Mj}{K}\ \frac{D^{(3-n)}}{V_m} + \frac{4}{3\sqrt{3}}\ \frac{K\,D^{(n-1)}}{(n+1)} \tag{31}$$

is minimized when

$$K^2 = \frac{27}{16}\ \frac{(n+1)}{(5-n)}\ \frac{(Mj)\,D^{(4-2n)}}{(VM)}$$

Hence

$$F_{RT} = F_{cT} = \frac{D}{\sqrt{n+1}\ \sqrt{5-n}}\sqrt{\frac{Mj}{V_m}} \tag{32}$$

These losses will be minimized when

$$n = 2.$$

For this case

$$F_{RT} = F_{cT} = \frac{D}{3}\sqrt{\frac{Mj}{V_m}} \tag{33}$$

$$= \frac{DIAG}{6}\sqrt{\frac{Mj}{V_m}}$$

Note that for n = 2, the current density in the trunk line is constant. Intuitively, we would expect this condition to minimize the losses. For an optimized linear taper, used in the first design, losses are higher by a factor of 1.06.

When the optimum spacing has been determined for a segment, the power loss components are computed for that segment; e.g., the power loss components for the j^{th} segment are

$P_{D(j)}$ diffused resistive power loss

$P_{F(j)}$ finger resistive power loss

$P_{C(j)}$ finger coverage power loss

These power loss components are summed to give total power loss components for the n segments of the cell; i.e.,

$$S_D = \sum_{j-1}^{n} P_{D(j)}$$

$$S_F = \sum_{j=1}^{n} P_{F(j)}$$

$$S_C = \sum_{j=1}^{n} P_{C(j)}$$

Loss factors for the cell are defined as

$F_{DR} = S_D/P_A$ diffused resistive loss factor

$F_{FR} = S_F/P_A$ finger resistive loss factor

$F_{FC} = S_C/P_A$ finger coverage loss factor

where

$$P_T = A_T \cdot j \cdot V_m$$

is the total power available at the maximum power point, A_T is the total cell area, and j and Vm are current density and voltage for maximum available power.

The total loss factor for metal coverage is

$$F_{TC} = F_{FC} + F_{CT} \tag{34}$$

where F_{CT} is the trunk coverage factor.

Total resistive loss factor is defined as

$$F_{TR} = F_{DR} + F_{FR} + F_{RT} \tag{35}$$

where F_{RT} is the trunk resistive loss factor.

Efficiency for metal coverage is

$$E_C = (1 - F_{TC})\,100 \tag{36}$$

and efficiency for resistive loss is

$$E_R = \left(1 - \frac{F_{TR}}{(1 - F_{TC})}\right) 100 \tag{37}$$

The efficiency product for metal coverage and series resistance is

$$E_P = \frac{(E_C)(E_R)}{100} \tag{38}$$

Constants used for calculation of optimum spacing, loss components, and efficiencies are shown in Table 6.

Optimized fractional loss components for the total cell were calculated as a function of finger width for a hexagonal cell of 7.6 cm diagonal. As shown in Figure 23, finger resistance loss and finger coverage loss are of comparable importance for small finger widths. However, finger coverage loss dominates for wide fingers.

Table 6. Design Assumptions for Improved Solar Cells

- 2 Contact pads on opposite points
- AM1 (no concentrator)
- Diffused layer sheet resistance, r ≅ 80 Ω/□
- 6 μm Ag, m = 0.00333 Ω/□
- Design equations based on minimized power loss (based on minimizing the sum of resistance loss and metal shadowing loss)
- Contact resistance and bulk resistance assumed negligible
- Voltage output for maximum power = 0.50 V
- Current density for maximum power = 32.5 mA/cm^2

The product of series-resistance efficiency and metal-coverage efficiency was calculated for a range of values of finger width and for a range of diameters of hexagonal cells. This data is plotted in Figure 24. It is noted that for large cells, the product is not significantly improved by use of very narrow finger widths.

3. "Fishbone" Pattern

The "fishbone" configuration, shown in Figure 19(b), consists of trunk lines along a major diagonal of the hexagon with perpendicular metal fingers on each side of the trunk. Optimum spacing for the metal fingers is calculated from the sum of the fractional losses

$$F = a'' \frac{S^3}{S+T} + b'' \frac{S^2}{S+T} + \frac{T}{S+T} \tag{39}$$

where S is the spacing between fingers, T is the finger width, and a″ and b″ depend upon fabrication parameters. The length, L, of the fingers is related to distance, X, from the center of the hexagon by the relationships

$$L = \frac{\sqrt{3}\,D}{2} \qquad 0 < X < \frac{D}{2}$$

$$L = \sqrt{3}\,(D - X) \qquad \frac{D}{2} < X < D$$

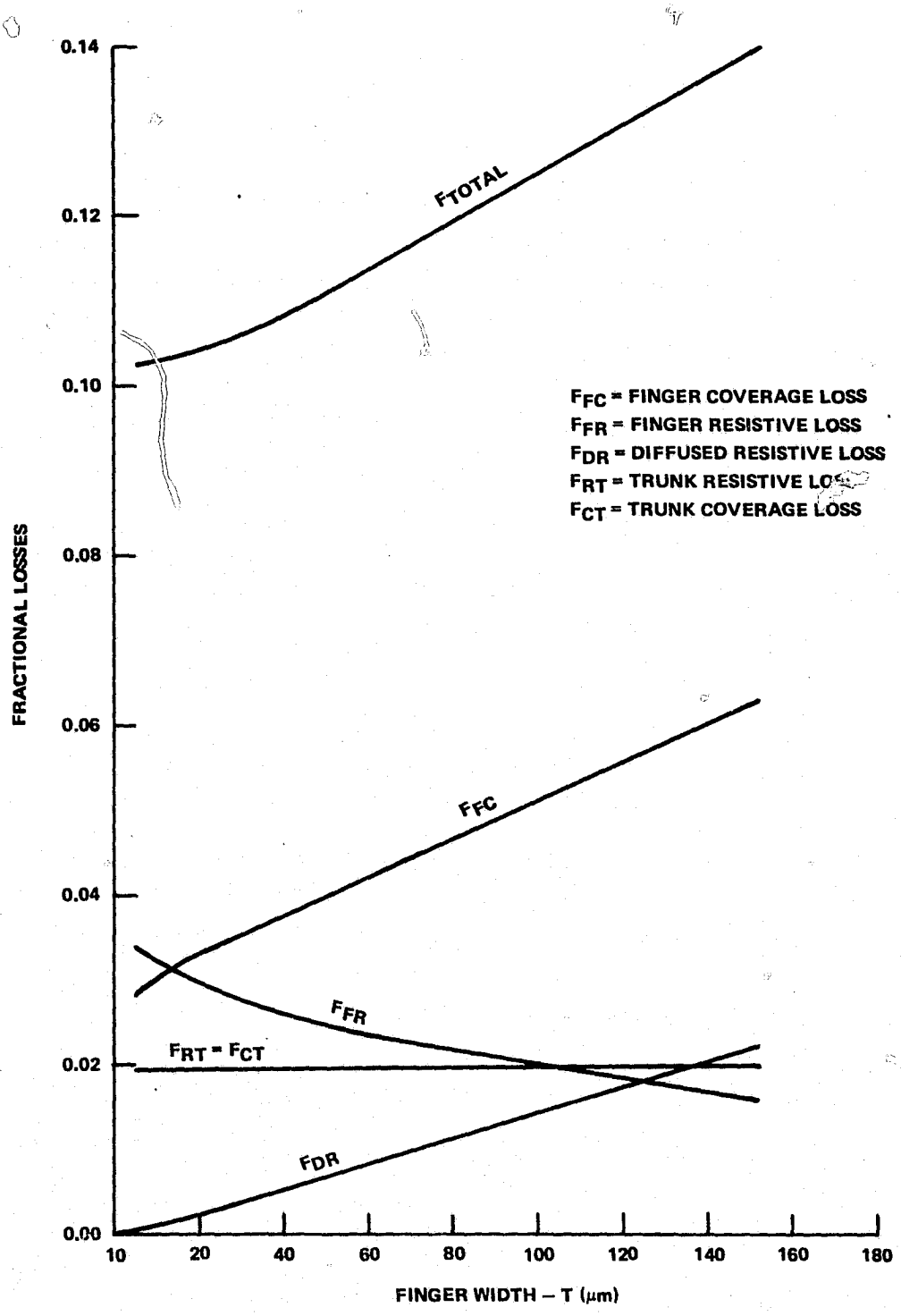


Figure 23. Fractional Loss Components for 7.6-cm Hexagonal Solar Cell as a Function of Metal Finger Width

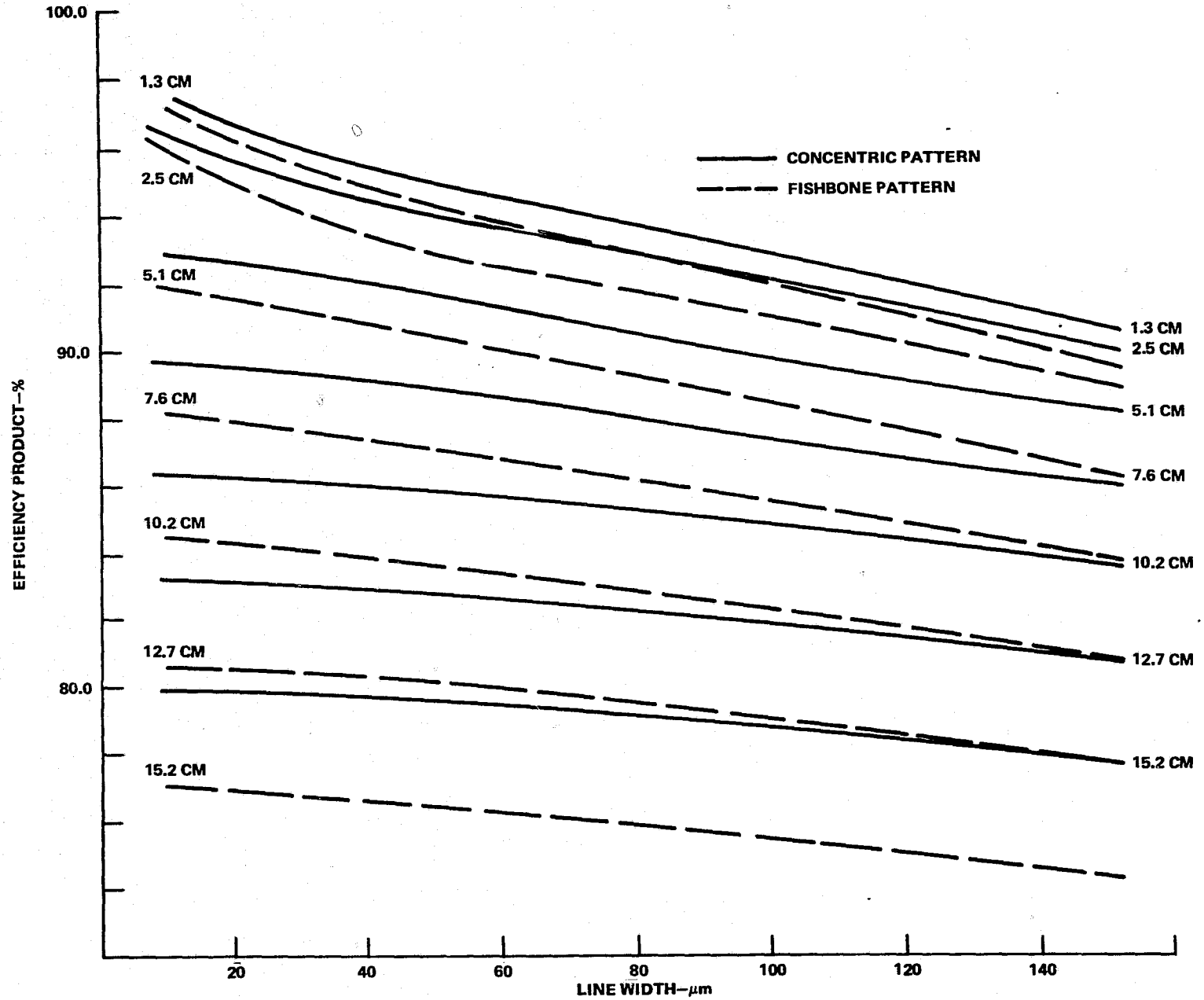


Figure 24. Efficiency Product for Metal Coverage and Series Resistance versus Metal Finger Width as a Function of Cell Diagonal for Hexagonal Cells

As for the concentric hexagonal pattern, the computer program determines optimum spacing as a function of X, computes power loss components and increments to the next segment.

The trunkline is tapered such that current density is the same for all values of X. For $X \leq \frac{D}{2}$,

$$i(X) = \sqrt{3}\, j\, D\, X$$

In this region, the width of the trunk line is

$$T_T(X) = K\, X.$$

Current density for the trunk line is

$$j_T = \frac{2\,(X)}{T_T\,(X)} = \sqrt{3}\,\frac{jD}{K} \qquad (40)$$

For the region $D/2 < X < D$, current in the trunk line is

$$i\,(X) = j\sqrt{3}\,(2\,D\,X - D^2/4 - X^2)$$

For constant current density, trunk width in this region is

$$T_T\,(X) = \frac{i\,(X)}{\sqrt{3}\; j\; D/K}$$

trunk resistive and coverage loss factors are calculated as

$$F_{RT} = \frac{2}{P_A}\int_o^D [i(X)]^2\,\frac{M}{T_T(X)}\,dx \qquad (41)$$

and

$$F_{CT} = \frac{2}{A_T}\int_o^D T_T\,(X)\,dx \qquad (42)$$

where P_A and A_T are total available power and total area as defined before. The sum of these losses is minimum when

$$F_{RT} = F_{CT} \tag{43}$$

For this condition

$$K^2 = \frac{3}{4}(DIAG)^2 \frac{jM}{V_m}$$

and

$$F_{RT} = F_{CT} = \frac{11}{36}(DIAG)\sqrt{\frac{jM}{V_m}}$$

The product of metal-coverage efficiency and series-resistance efficiency is plotted in Figure 24 vs metal line width, as a function of cell diagonal for hexagonal cells. Efficiency products for both the fishbone metal pattern and the concentric metal pattern are shown for comparison. In Figure 25, efficiency products are plotted versus cell diagonal for the concentric and fishbone hexagonal patterns with 100 μm metal line width.

In both Figures 24 and 25, we note that the efficiency product for the concentric pattern is always higher than for the fishbone pattern with the same diagonal and line width.

4. Rectangular Pattern

The basic rectangular pattern, shown in Figure 26(a), consists of parallel metal fingers connected to one edge of a trunk. The trunk is a tapered line with a bond pad at the larger end. As shown later, efficiencies for other rectangular configurations can be deduced from combinations of this pattern.

For one segment of the cell, the sum of fractional losses due to diffused region resistive loss, finger resistive loss, and finger shadowing loss, is

$$F = a\frac{S^3}{S+T} + 6\frac{W^2S^2}{(S+T)T} + \frac{T}{S+T}. \tag{44}$$

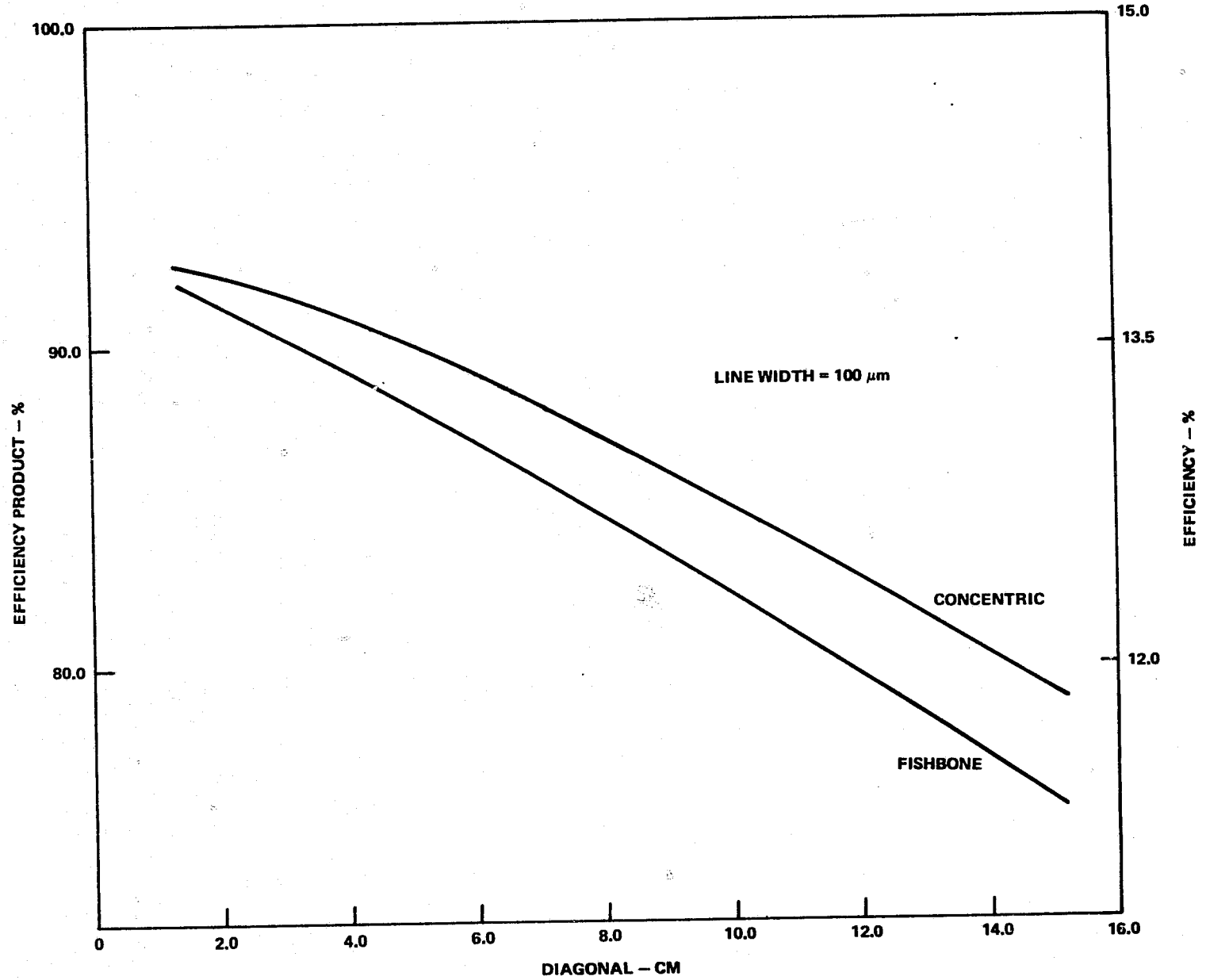
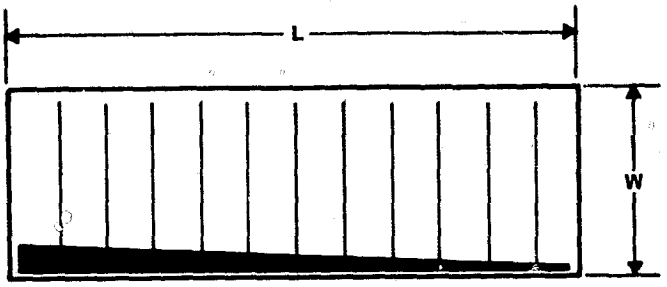
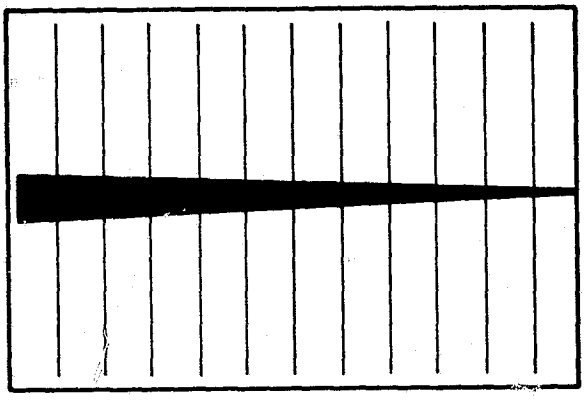


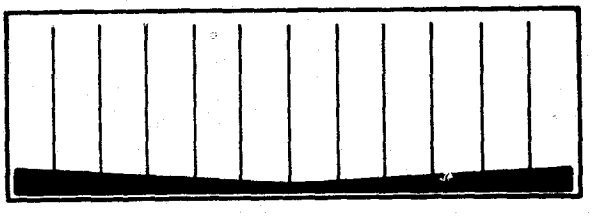
Figure 25. Efficiency Product and Efficiency as a Function of Cell Diagonal



a. RECTANGULAR COMB PATTERN



b. RECTANGULAR FISHBONE PATTERN



c. RECTANGULAR BOW-TIE PATTERN

Figure 26. Rectangular Solar Cell Metal Patterns

The computer program determines the value of spacing, S, which minimizes F and computes the values of F and efficiency product for that spacing. It is assumed that the length, H, of the cell is much larger than S so that all segments are of optimum width. Hence, the efficiency product for the cell is the same as for a segment. The efficiency product, Ep, for diffused region loss and finger loss is plotted in Figure 27 versus finger width, T, as a function of cell width, W.

Resistive loss for the trunk line is

$$P_{RT} = \int_o^H [i(X)]^2 \, d\,R \tag{45}$$

where X is the distance along the length, H, of the cell, j is the current density, M is sheet resistance of the metal,

$$i(X) = j\,W\,X$$

and

$$d\,R = \frac{M}{T(X)}\,dX$$

Width of the trunk line is assumed to vary as

$$T_T(X) = K\,X^n$$

From these relationships, the resistive loss factor for the trunk is

$$F_{RT} = \frac{P_{RT}}{H\,W\,V_m\,j} \tag{46}$$

$$= \frac{j\,W\,M\,H^{(2-n)}}{V_m\,K^{(3-n)}}$$

The shadowing loss for the trunk is

$$P_{CT} = \int_o^H T(X)\,dx \tag{47}$$

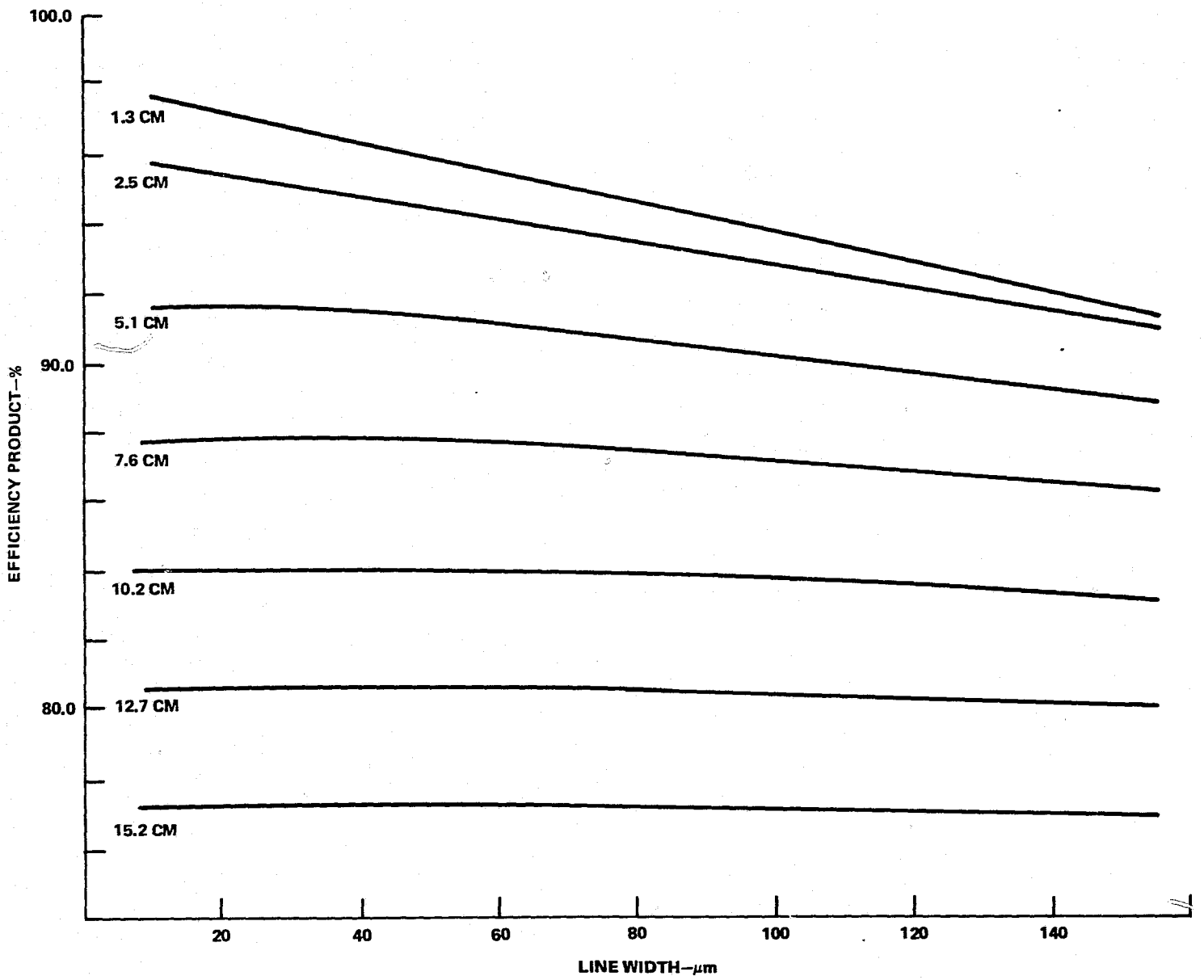


Figure 27. Efficiency Product for Metal Coverage and Series Resistance vs. Metal Finger Width as a Function of Cell Width for Rectangular Cells, Excluding Trunk Losses

and the shadowing loss factor is

$$F_{CT} = \frac{P_{CT}}{HW} \qquad (48)$$

$$= \frac{K H^n}{W(n+1)}$$

The sum of these losses is minimum for

$$K^2 = \frac{n+1}{3-n} \frac{H^{(2-n)}}{H^n} W^2 \frac{jM}{V_m}$$

So that

$$F_{RT} = F_{CT} = \frac{H}{\sqrt{(n+1)(3-n)}} \sqrt{\frac{jM}{V_m}} \qquad (49)$$

These loss factors will have their lowest value for n = 1 (i.e., a linear taper). In this case

$$F_{RT} = F_{CT} = \frac{H}{2} \sqrt{\frac{jM}{V_m}} \qquad (50)$$

The trunk loss factor ($F_{RT} - F_{CT}$) is plotted in Figure 28 as a function of cell length, H.

In terms of the efficiency product, E_P (Figure 27) for diffused region and finger losses of the cell and the loss factor for the trunk ($F_{RT} = F_{CT}$), the overall efficiency product E_{PT} for the rectangular cell is

$$E_{PT} = E_P - 2 F_{RT} (100) \qquad (51)$$

5. Improved Designs

Several alternate metallization pattern designs can be used to improve the efficiency product of rectangular solar cells, providing that the array bonding is compatible. Two examples are discussed below.

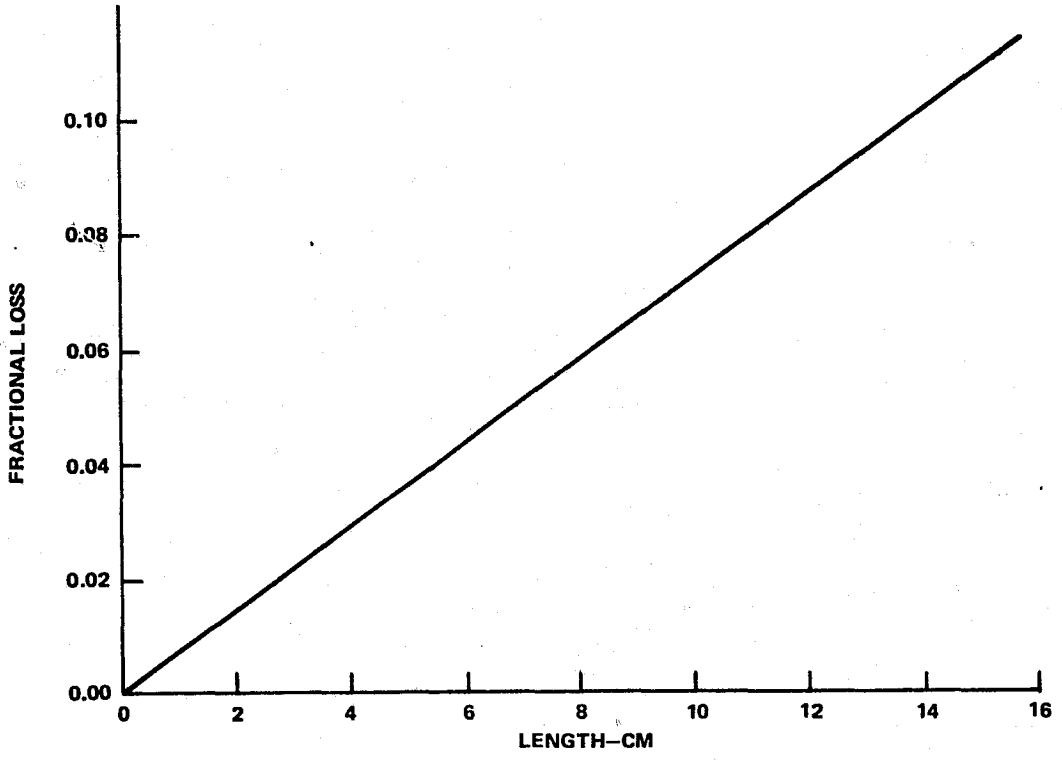


Figure 28. Fractional Trunk Loss due to Resistance or Shadowing as a Function of Length for Rectangular Cell

1) For a wide rectangle, the efficiency product is lower than for a narrow rectangle. From Figure 27, a 15.2-cm wide rectangular cell with 100-μm finger widths has an efficiency product of 0.772, while a 7.6-cm wide rectangle with 100-μm finger widths has an efficiency product of 0.872. By using the rectangular fishbone pattern shown in Figure 26(b), one can achieve the effect of two comb patterns back-to-back and thus achieve the higher efficiency product of the half width cell, 0.872, on the full 15.2 cm width. Of course, one could use two comb patterns front-to-front if it was desirable to keep the bonding areas on the cell edges.

2) For a long rectangle, the trunk line losses can become excessive. If one imagines two rectangular comb patterns end-to-end, we arrive at the rectangular bow-tie pattern shown in Figure 26(c). Now the effective length of a cell is one half the total length and the trunk losses are similarly halved, yielding higher efficiency for the bow-tie pattern.

In a fashion similar to the above examples, the basic patterns can be iterated on wide or long rectangles to achieve the effect of higher efficiency small rectangles. It must be kept in mind however that each subcell unit must be attached to the outside world to achieve large arrays, and in practice, the number of subcell iterations that can be used will depend on the allowed interconnect scheme.

As a general rule for large-area rectangular solar cells, the fishbone pattern will be the most efficient configuration when one bonding site is allowed and a bow-tie-fishbone (two fishbone patterns head-to-head) will be the most efficient configuration when two bonding sites are allowed. A brief study of Figure 26 will show that many more variations of the basic comb pattern are possible.

The structures described were selected as practical configurations for fabrication of cells and arrays. There may be other design variations which give higher efficiencies, e.g., the width of a finger might be decreased with distance from a trunk line. A specific example is calculated here to illustrate the potential improvement and limitations of tapered fingers.

A rectangular cell segment of width, W and spacing, S, is illustrated in Figure 29. The current as a function of distance, Z, along the finger is

$$i(Z) = j\,S\,Z \tag{52}$$

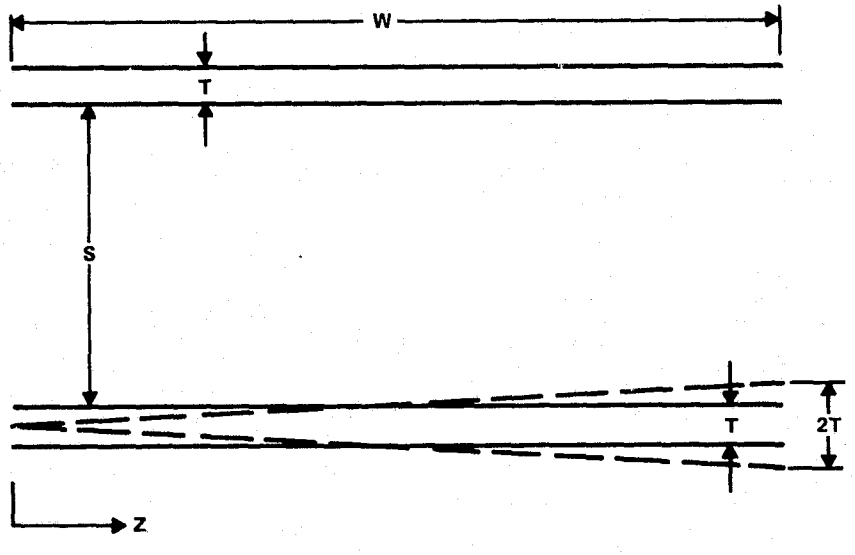


Figure 29. Cell Segment for Comparison of Constant-Width and Tapered Fingers

A triangular shaped finger having the same area is shown by the dotted line. Width of the end connected to the trunk is 2T and thickness as a function of distance from the small end is

$$T(Z) = \frac{2T}{W} Z$$

For the tapered finger, the resistive power loss is

$$P_F' = \frac{j^2 M S^2 W^3}{4T} \tag{53}$$

The resistive finger loss is reduced 25% by tapering the fingers, without changing metal coverage loss or diffused region resistive loss. However, in practice, photolithographic processes would be required to fabricate the triangular shaped fingers due to the fine geometry incurred at the narrow end of the finger.

6. Conclusion

Computer analysis of solar cell front surface metallization design equations provides a powerful tool for optimization of process alternatives. Significant comparisons can be made without resorting to the time consuming and costly process of cell fabrication. Optimum efficiency as a function of metal line width and cell diameter can be predicted.

Equally important, a quantitative assessment can be made of the impact of various process technology choices. This quantitative assessment is a key factor in the evaluation of alternatives for low-cost high-efficiency solar cell fabrication.

While this calculation covers only a hexagonal and rectangular solar cells, it can be extended to cover other pattern geometries and other cell geometries. The quantitative assessment of competing geometries can be used to identify the optimum pattern geometry that matches a given cell geometry.

Finally, a fractional loss calculation can be used as one of the parameters in establishing the maximum practical sheet area for various large area silicon sheet processes.

E. SILICON SHEET CONSIDERATIONS

The choice of a low-cost silicon solar cell process for a 1985 high-volume production goal is dependent on a number of factors. One important factor, silicon sheet form and quality, is not covered in depth in this study. A few comments on the impact of silicon sheet form and quality are in order at this point.

1. Shape

Semiconductor industry experience is based on round single crystal silicon wafers. Existing mechanical handling equipment is designed to operate with round wafers. Simple geometric shapes other than round, e.g., hexagons, squares, and rectangles, can be accommodated by straightforward mechanical redesign. Caution must be observed to prevent breakage at the pointed corners. Process techniques, such as spin-on coating, can be adapted using spray, dip, or screen-on techniques, as appropriate. Long continuous ribbons of silicon will present much more complex problems if processing is envisioned as a continuous process. Although many semiconductor processes can be adapted to continuous processing, it is not practical to fabricate very large-area solar cells. Solar cells are high-current, low-voltage power supplies and if solar cells become too large, the I^2R power losses become excessive. Therefore at this time, it is envisioned that continuous ribbons of silicon would be cut into rectangles for processing.

2. Crystallinity

Silicon sheet can be obtained in different degrees of crystallinity. For purposes of this discussion, three forms are considered: single-crystal, two-dimensional polycrystalline and three-dimensional polycrystalline silicon sheet material. Amorphous silicon will not be included at this time. The behavior of single-crystal silicon is well known and all other things, e.g., cost, performance, etc., being equal, this is the material of choice. Within the realm of polycrystalline material, one can distinguish between two-dimensional polycrystalline material where the typical crystal dimension in the vertical (front to back) direction is greater than the sheet thickness, therefore, grain boundaries exist primarily in the vertical direction and three-dimensional polycrystalline material where the typical crystal dimension is less than the sheet thickness and grain boundaries exist in all dimensions.

Processes that are accelerated along grain boundaries, such as impurity diffusion, will have to be modified for use with polycrystalline silicon sheet. For example, in the case of impurity introduction, ion implantation would undoubtedly be more desirable than standard diffusion techniques. Front and backside contact techniques would also have to be altered to accommodate polycrystalline material.

Two dimensional polycrystalline silicon sheet has been shown to yield solar cells of reasonable efficiency, $\approx$ 10%, and must be considered as a viable alternate for solar cell applications. Three-dimensional polycrystalline silicon sheet is still in the speculative stage at this time.

Silicon sheet in the form of polycrystalline silicon on a substrate is not considered a viable alternate at this time. Access to the back side for back-side contact imposes added process complexity and cost that does not appear to be performance cost effective in the near future. No further consideration of this form of silicon sheet is planned at this time.

3. Surface

Although most of the existing solar cell technology has been developed on chemically polished surfaces, surface roughness is not envisioned as a problem area. Low-cost solar cell processes will probably utilize junction formation technologies and thick-film metallization technologies, e.g., screen print or electroless plate, that are very tolerant of surface irregularities. A preferred surface on ⟨100⟩ single-crystal silicon sheet is a texture etched surface that has chemically formed surface pyramids of approximately 5-μm height. Highly polished surfaces are undesirable because of their loss of incident light by reflection.

Processing techniques must be optimized if textured or roughened surfaces are used. The main cause for concern is mechanical damage such as chipping on the wafer surface.

4. Thickness

Silicon sheet thickness will impact solar cell cost and performance. Cost will be directly impacted by the quantity of silicon used per unit area. The more silicon volume that is used, the more raw silicon cost that must be included.

Balanced against raw silicon cost will be solar cell performance and wafer processing yield. Thicknesses below 250 μm appear to exert a negative effect on cell efficiency. A quantitative relationship is not available. Semiconductor manufacturing experience indicates that with increasing wafer size, thicker wafers are required to minimize wafer warpage and breakage. The breakage is related to mechanical handling and to a degree can be controlled by proper design of automated handling equipment. Warpage may be more of an intrinsic problem that may impose a lower limit on wafer thickness. This will be a factor of silicon sheet formation technology and absolute limits cannot be predicted at this time.

F. SOLAR CELL PROCESS STEPS

The manufacture of silicon solar cells involves a number of process operations or steps. The choice of a preferred process will be dependent on many factors. The key factors used in this analysis are process step cost, ultimate cost potential, ease of automation, technical feasibility, and process compatibility. A number of process step alternatives have been evaluated. The process step alternatives have been grouped into surface preparation and cleaning, junction formation, metallization and optical coating groups for comparison and evaluation. Each group is discussed below. Costing is discussed in the following section.

1. Surface Preparation and Cleaning

Masking operations have been downgraded as nonproductive and costly operations. Photoresists are material intensive and other methods can be used to define patterns. Mask stencils are costly and can only be used in a low-cost process if no buildup or deposit accumulates. Mask stencil cleaning is too expensive. Mask stencils might be useful in plasma etching operations.

Surface cleaning techniques can be divided into chemical and mechanical. The chemical cleaning techniques can be subdivided into water based (including acids and bases), organic solvent based and gaseous (plasma). Water-based cleaning techniques are best suited for the removal of inorganic residues, such as metals, metallic ions, and water soluble anions. Organic solvent-based cleaning techniques are best suited for removal of organic residues, such as waxes, greases and polymeric materials. In general, organic solvents do not remove inorganic residues. Gaseous cleaning techniques, such as oxygen plasma and reverse sputtering are excellent for removing organic residues that do not leave ash residues (inorganic oxides). Plasma cleaning is easily automated and has a low-cost potential.

Mechanical cleaning is particularly suited to removal of particulate matter and is easily automated. Ultrasonic agitation can be used to augment any of the chemical cleaning techniques.

The ideal process would require no cleaning operations at all. However, in the real world, cleaning will be required and the choice of a cleaning process will depend on the type of contaminant to be removed.

Surface texturing can have a beneficial effect on solar cell performance. Textured surfaces produced on ⟨100⟩ silicon surfaces substantially reduce light reflection and improve metal adhesion. Two methods are known to produce uniform texture on ⟨100⟩ silicon surfaces, NaOH and hydrazine etching. The NaOH technique is preferred on the basis of lower material cost, ease of control and safer conventional chemical handling. On sawed single-crystal material, the NaOH etch can be used

both for removal of surface damage and texture etching. Feasibility evaluation at Texas Instruments has shown that this combined damage removal and texture etching is possible. With a suitable choice of processing conditions, it is also feasible to polish one side of a wafer while texturing the other side. The process includes an acetic acid rinse so that no subsequent cleaning operation is necessary.

2. Junction Formation

The characteristics of the front-side (collecting) junction are very critical in the fabrication of high-efficiency solar cells. Sheet resistance, surface concentration, juntion depth and diode characteristics must be carefully controlled to achieve optimum performance. The minority carrier lifetime of the base region should not be degraded during the junction formation process. A back-side contact region and back surface field are also required.

An ideal process for the N^+PP^+ solar cell structure would introduce both N^+ and P^+ regions at the same time and leave no detrimental surface residue. Two processes approach this ideal: ion implantation and polymer dopant technologies. Both allow the introduction of opposite conductivity type impurities on opposing wafer faces and simultaneous thermal treatment (diffusion). Both offer good control of sheet resistivity, surface concentration and junction depth. Although diode characteristic data and base minority carrier lifetime data are not complete at this time, both processes are excellent candidates for a solar cell process. Ion implantation would probably be preferred for polycrystalline material due to the lower temperature thermal treatment and probable smaller effect at grain boundaries. On the basis of projected cost, we favor polymer dopant at this time.

Open-tube diffusion using a gaseous source, e.g., $POCl_3$ or PH_3, has been used to make solar cells for many years. Excellent results have been achieved. The primary disadvantage of this technique is that the gaseous diffusion source dopes all exposed surfaces with one conductivity type impurity. Separate steps with attendant masking are required to produce both the N^+ and P^+ regions. Operations such as depositing and alloying Al through the N^+ diffusion on the back side have been used. The extra processing steps make this technique a poor third choice.

Other technologies such as epitaxy, alloying, doped oxides, and solid source diffusion do not offer good enough control or low enough cost to merit further study for this application.

3. Metallization

The front-side contact metallization plays an important role in the collection and transmission of photo-generated current in solar cells. Metal resistivity, thickness, adhesion, contact resistivity and bondability must be carefully controlled to achieve optimum performance.

Metallization technologies can be broadly categorized into two groups, vacuum and nonvacuum processes. The vacuum processes include evaporation and sputtering technologies. Vacuum deposition of metal is wasteful of material since not all of the evaporant stream can be directed onto the substrate and on the front side only a small portion, <5%, of the metal that condenses on the surface is used in the metallization pattern. Vacuum equipment is costly, difficult to maintain and throughput is low. Very good metal properties can be attained with the exception of metal thickness. Thickness buildup can be achieved with a subsequent plating or solder coating operation. Vacuum deposition through a mask stencil is preferred, to avoid the extra processing steps involved in photomask and etching operations. The problem of mask cleaning and fixturing remains, however. Although vacuum deposition has been used to fabricate solar cells for many years and the metal properties are good, vacuum deposition is not a preferred choice for a low-cost process.

Among nonvacuum metallization processes, two candidates appear most promising, thick-film screen printed metallization and electroless plating of metals. Both of these technologies have considerable industry experience but not in the application on silicon solar cells.

Thick-film screen printed metallization has been used extensively in the metallization of ceramics. The majority of commercial pastes or inks contain precious metals, Au, Pt, Pd or Ag and are fired at high temperatures, >800°C in air. The pastes also contain significant amounts of glass frit, 5 - 15%, whose function is to promote bonding to a ceramic substrate. Experimental pastes are becoming available that contain base metals, Cu, Ni, and Al. The screened printing process prints a paste pattern on the substrate through a mask stencil (screen). Little or no paste is wasted since the paste that is left on the screen can be used on subsequent substrates. Patterns as narrow as 100 μm can be printed. The glass frit found in commercial pastes presents a problem in contact printing on silicon. The glass is not conductive and can inhibit contact to the silicon solar cell. The high firing temperatures used with commercial pastes are not readily compatible with solar cell processing. Screen printed metal is typically 15 to 25 μm thick and does not require subsequent plating or solder dipping to improve conductivity.

Experimental work at Texas Instruments on this contract with Cu and Ni inks demonstrated that these commercial pastes show promise but are not ready for implementation in a manufacturing process. The commercial Cu paste alloyed into the silicon surface and penetrated the shallow N^+P junction on the front side of the solar cell. Commercial Ni paste could be fired on solar cells without shorting the junction.

This technology holds much promise as a low-cost readily automated metallization technology for silicon solar cells and should be pursued as a development program. Silicon solar cells are being fabricated using specially formulated Ag pastes.[3]

Electroless plating of nonprecious metals is the alternate metallization technology of choice. Electroless Ni plating has been used for many years in the semiconductor industry on deep junction devices. Typical Ni plates contain significant amounts of P or B depending on the plating solution. The plated metal must be sintered to enhance contact resistivity and adhesion.

Unless the metal plate can be patterned as part of the plating operation, masking techniques must be used. The requirement for separate masking would be a serious cost impediment in the incorporation of electroless plating into a low-cost silicon solar cell process. A low-cost patterning process that did not add material cost would be very desirable.

A patterned electroless plating process called PIMDEP, photo impeded metal deposition, has been used on plastic and ceramic substrates. The process uses a sensitizer, $SnCl_2$, that can be desensitized by light, followed by an activator, $PdCl_2$, that activates the nonexposed regions, followed by electroless plating. A photomask is required to expose the sensitizer but the photomask is not consumed and does not accumulate deposits that require subsequent removal. The process has been used to form patterns on Kapton, a polyimide plastic, and ceramics. Pattern geometries as small as 100 μm have been plated. The process has not been demonstrated on silicon devices but there does not seem to be any inherent reason why it would not work on silicon solar cells. The sensitizer and activator steps are also required in conventional electroless plating so these operations do not add significant extraneous cost elements. The PIMDEP process offers the most attractive approach to electroless plated contact metallization.

The problem of making reproducible ohmic contact to shallow junction devices remains a question for electroless plated metals, as it does for all metallization schemes. The shallow front junction, required for efficient collection of photons, presents a delicate structure for low resistivity ohmic contacts. The problem should be solvable and electroless plating, particularly the PIMDEP process, is a good candidate process element for a low-cost silicon solar cell process.

In summary, vacuum metallization processes, while technically good, are not attractive process elements for a low-cost solar cell process. Thick-film screen printed metallization and electroless metal plating, PIMDEP, are good choices for a low-cost process. Significant further development is needed for each of these nonvacuum metallization options.

4. Optical Coating

The optical coating on the front of a silicon solar cell plays an important role in efficiency at which a cell will operate by reducing reflection losses and providing a degree of surface passivation. Since reflection is a function of surface smoothness, roughened or textured surfaces reduce the requirement for good optical matching in the antireflection coating. A good optical coating should provide refractive index matching between the silicon surface and air, have very low absorption (high transmittance) and provide surface passivation for the silicon solar cell.

Several materials have been used in the solar cell industry, evaporated silicon monoxide, tantalum pentoxide and silicon oxide-titanium oxide mixtures. Silicon nitride represents another good optical material. Optical films can be applied by evaporation, sputtering, spin-on or spray-on techniques. Assuming good control of the basic material properties, the key parameter is optical thickness control. Thickness control provides an optimum response at a predetermined wave length with less than optimum response at other wavelengths in the spectrum. Since a terrestrial (or space) solar cell will be operated over a broad spectrum, very tight control over the thickness is not required. Slight deviations in thickness will only shift the point in the spectrum where maximum response occurs. All of the above optical coating techniques are acceptable. Low-temperature silicon nitride deposition and spin-on or spray-on techniques for silicon oxide-titanium oxide films offer the most favorable approaches to an automated process.

For use on rough or textured surfaces, the spin-on or spray-on approach or the low-temperature silicon nitride processes are the most favored. Vacuum techniques could suffer from shadowing if surface roughness interferes with line-of-sight deposition.

5. Interconnection

Metal-to-metal bonding, soldering, welding or ultrasonic bonding offer the most attractive approaches to cell interconnection. Thermal compression bonding requires high pressure per unit bond area and is not considered a viable candidate. Conductive epoxies can introduce series resistance and have not demonstrated long life history. Conductive epoxies are not considered as viable candidates.

Since interconnect of cells is such a key area of module fabrication, it is discussed under module fabrication in a subsequent section of this report.

6. Encapsulation

The main purpose of solar cell encapsulation is to protect the cell and interconnect system from environmental hazards. Data collected in Task 3 of the LSSA Project indicates that plastic encapsulants provide only partial protection from the environment. Complete protection can be provided only by using impermeable encapsulants. Plastics are also expensive and thick layers of plastic required for environmental protection add significantly to module cost.

Glass provides a reasonable cost nonpermeable cover for solar cell modules. The substrate must also be low-cost and provide environmental protection. Several materials have been proposed bot porcelainized steel appears to offer the best balance of cost and material properties.

A more complete discussion of a long life module is found in the discussion of module fabrication.

7. Test

A discussion of final testing of completed solar cells and solar cell modules is found in the section on Solar Cell Testing. Test requirements and a proposed design for test equipment is included.

In-line testing as a process control technique is another aspect of testing. The function of in-line testing is to provide rapid feedback for process control and early detection of possible reject material. The process control function is related to each process step and provides the positive control necessary to optimize each operation. The frequency and extent of the testing must be balanced against the need and cost. For example, if diffused layer resistivity is routinely controlled to ± 10% and the sensitivity analysis shows that diffused layer resistivity does not significantly impact cell efficiency until the variation exceeds ± 30% of nominal value, then frequent in-line testing of diffused layer resistivity is a nonaffordable luxury. If, on the other hand, ± 10% of nominal value is the limit before cell efficiency is impacted, then in-line testing is a necessity.

By definition, a well controlled process will have reproducible process variations and in-line testing will only be required at a few key points in the process. These key points have not been defined for solar cell processes at this time. A sensitivity analysis is the next logical step in the definition of a well controlled automated solar cell process. In-line test costs must be very low so that they do not adversely affect manufacturing cost.

8. Process Uniformity

Two lots (AAAP-16 and 17) of 7.6-cm hexagonal solar cells, 25 slices per lot, were processed using our standard open-tube P diffusion process with sintered Al for back-side contact. These N^+PP^+ cells have Ti-Pd-Ag front-side metallization and were laser scribed into hexagons after processing. Parameter uniformity was very good within a lot and between lots. A total of 45 cells out of 50 slice starts was achieved. At AM0, $I_{SC} = 1.0 \pm 0.1$ ampere and $V_{SC} = 0.59 \pm 0.02$ V. Figures 30 and 31 give the total distribution of I_{SC} and V_{OC} for these lots. The overall yield of 90% is probably greater than one would expect in a production facility but it is indicative of the good process and test yields that might be expected from a properly controlled solar cell process. These cells were used for experiments on module assembly.

G. SOLAR CELL TESTING

A key link in the manufacture of low-cost solar cells is the final test procedure for cells and for modules. Testing rates must be compatible with overall factory throughput rates to minimize costs. Testing should have a low labor content and a reasonable capital cost.

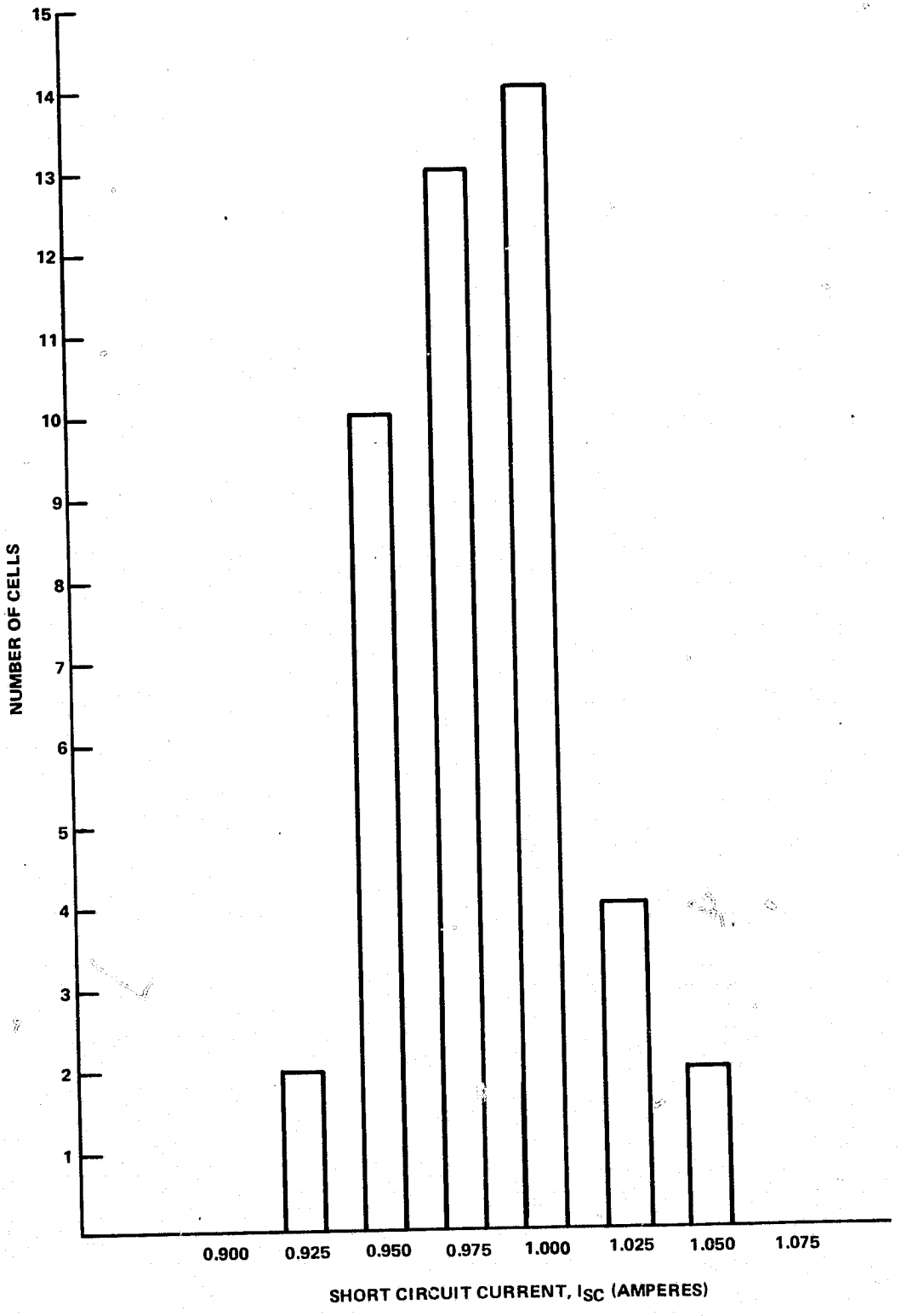


Figure 30. Distribution of Solar Cell Lots AAAP-16 and AAAP-17 as a Function of I_{SC}

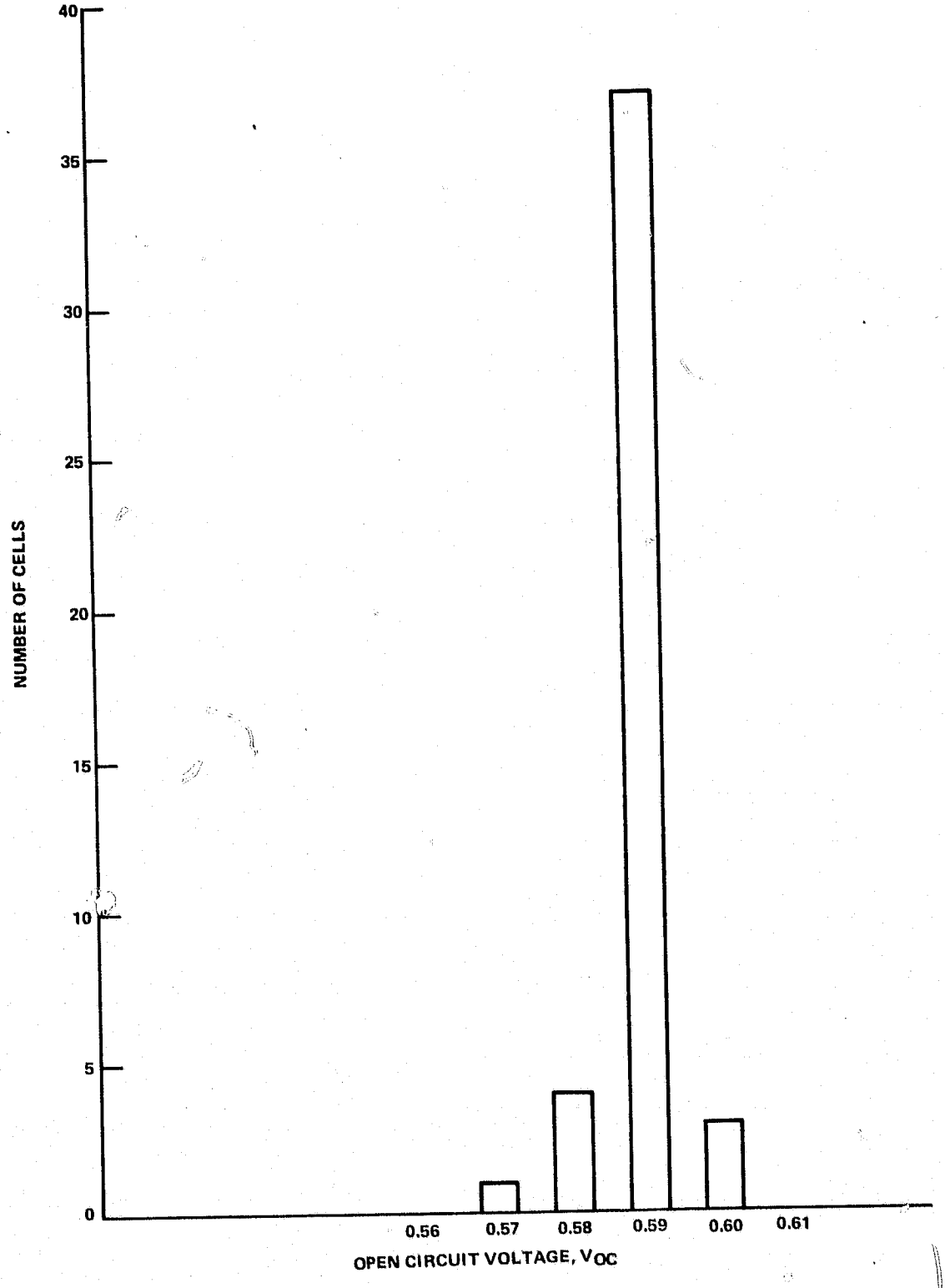


Figure 31. Distribution of Solar Cell Lots AAAP-16 and AAAP-17 as a Function of V_{OC}

A conceptual design of a solar cell test station for a unit factory has been developed. By definition, a unit factory will have an annual output of 3-6 MW (peak power) with a target output of 5 MW. Testing will be done on an individual cell basis to provide "good" cells for module fabrication. A second different test station will be required for module testing.

The solar cell test station is designed to accommodate the parameters in Table 7. All of the specific tests that will be required are not defined at this time but the test station must be versatile enough to accommodate any anticipated electrical tests. Table 8 lists the key known electrical tests, forward and reverse diode characteristics and illuminated I-V characteristics. Two versions of the test station are conceived, the basic version that assumes good process control and tight parameter control so that all good cells are grouped together in one category and a refined version that assumes good cells will be produced with a spread of usable outputs and this distribution of good cells must be grouped into bins of matched cells. The refined test station will require extra unload stations to correspond to the number of good categories or bins and the ability to sort "good-1," "good-2," etc., solar cells.

Table 7. Solar Cell Test Station Parameters

Cell Dimension	12 cm or 10 cm
Shape	Hexagon, round, or rectangle
Positioning in θ	Mechanical index from the flat edge (hexagon, rectangle or round with a flat) — Automatic optical alignment if no flat
Illumination	AM1 (100 mW/cm^2)
Temperature	Room (nominal 25°C)
Electrical Output	V_{OC} – 0.6 V I_{SC} – 2.5 A V_M – I_M 0.5 V, 2.0 A
Throughput	Nominal 1000/hour
Work Year	8400 hour
Down Time	20%
Yield	85%

Table 8. Solar Cell Tests

Dark	
Forward voltage	0.4 – 0.7 V @ 2 A
Reverse voltage	< 10 mA @ 1 V
Illuminated (AM1)	
I-V	Measure several points on I-V curve and software to calculate equation of curve, fill factor, maximum power, etc.

As a basic working premise, the basic test machine is the more desirable choice. The advantages are obvious, lower cost, a simple single "good cell" inventory and reduced record keeping. Module fabrication is also simplified if a tightly controlled cell inventory is available. In a well controlled process, it should be possible to maintain a high yield of a reproducible narrow distribution product. Therefore one of the goals of process and equipment development should be achievement of this well-controlled process using uniform silicon sheet material.

The test rate or throughput in Table 7 is based on the assumption that the factory output will be solar cells with a nominal 1-watt output per cell, with an electrical test yield of 85% and a utilization factor of 80%. Thus, at a throughput rate of 1000 cells per hour, the annual output of good tested cells would be (1000 cells/hour) X (8400 hours/year) X 0.80 X 0.85 = 5,712,000 good cells.

The basic solar cell test machine must contain the following stations in sequence, load, orient, test, sort/unload. To meet the 1000 cells tested per hour throughput rate, the machine must handle and test each cell in 3.6 seconds. Evaluation of the mechanical handling and test requirements indicates that a multitrack approach is the most desirable.

Figure 32 is a schematic of a four-track machine with provision for a single unload-good station. The machine would be fed from a four-carrier carousel using a standard "common carrier" cell holder. The common carrier cell holder concept would be used in the unit factory to interface from one cell fabrication machine to the next where machine boundaries exist. If the machine were built in modular stations which could be bolted together, extra unload stations could be added for sorting good cells into matched categories. Also, an extra load station could be added on the front so that the carousel change would not have to occur at a specific time.

The machine operation would be in a series-parallel-series mode where the cells would advance into the load station in a series fashion loading tracks 1, 2, 3, and 4. Then in a parallel fashion, all four tracks would adrance to the orient station to orient the cells to the test head in the next station. During the orient period, the load station would reload tracks 1 through 4. Depending on the availability of a mechanical asymmetry in the cell, mechanical and/or optical means would be used to position the contact pads on the cell for test. In a parallel fashion, all four tracks transfer to the test station. The test station would be computer controlled for test sequencing and pass/fail. After test, all four tracks would advance to the unload-good or unload-bad station. Then in a series fashion, tracks 4 through 1 would unload into another common carrier carousel. A timing diagram is shown in Figure 33.

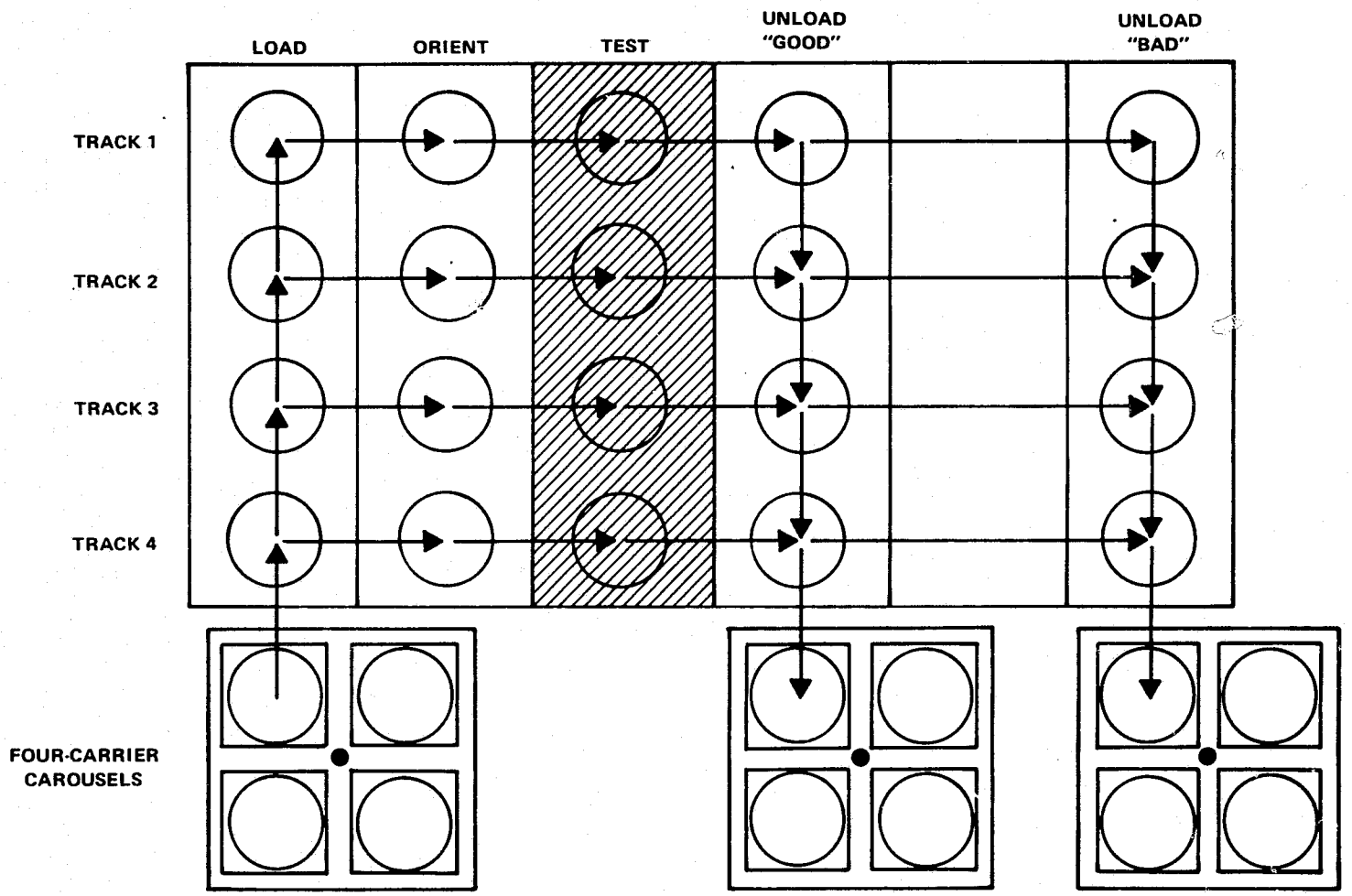


Figure 32. Solar Cell Test Machine

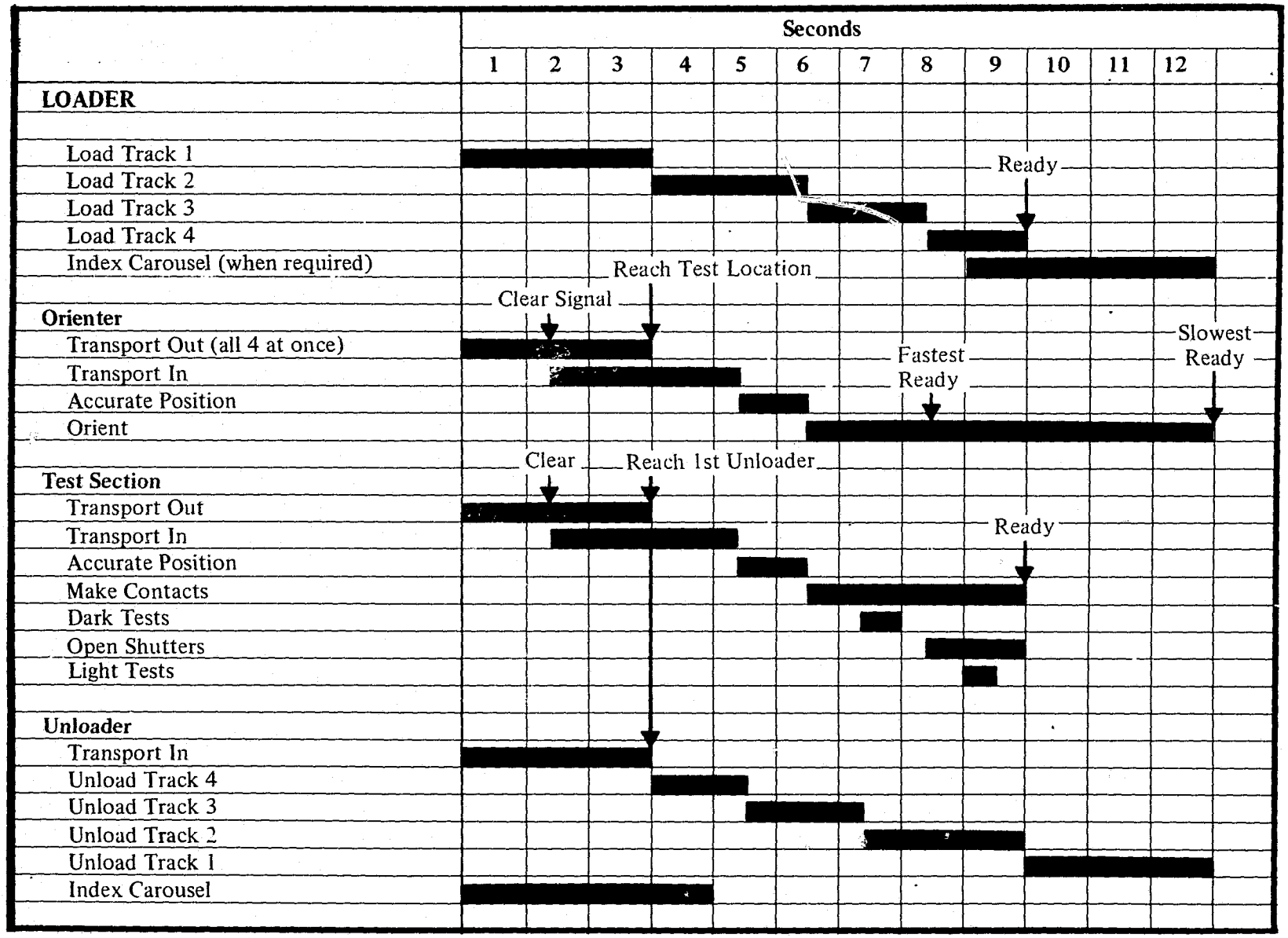


Figure 33. Solar Cell Tester – Timing Diagram

The test station, orient station, and unload stations would be controlled from a central computer or a remote minicomputer. The software in the control system would use curve fitting programs to determine the critical dark and illuminated parameters of the tested solar cells. Critical parameters such as shunt resistance, I_{SC}, V_{OC}, maximum power, voltage and current, and series resistance would be stored in memory and used as process control data to keep the fabrication process in control. This data could be displayed on a CRT or printed in hard copy. Figure 34 is an artist's rendition of a solar cell test machine with a control console at the test site. After design and after production begins, a test machine of this type is estimated to cost $100K-150K.

H. PHOTOVOLTAIC MODULE TESTING

Testing rates for a photovoltaic module test machine are dependent on the size of the module and the number of unit factories (nominal 5 MW/year output) served. A module tester for a single unit factory producing a standard 20 W module would have to test at a rate of 40 panels per hour. Test rates in this range are readily handled by single track testing. A test and mechanical handling time schedule for a photovoltaic module tester is shown in Table 9. The test rate derived from this time schedule is ≈ 200 modules/hour. A module tester with this capability would service 4 or 5 unit factories or operate on a one-shift rather than three-shift schedule.

The design of a module tester would be similar in concept to a solar cell tester, incorporating load, lock and contact, test, and unload-good – unload-bad stations. The module test machine would be larger than the cell test machine but software and control requirements would be similar. Estimated machine costs would be ≈ $100K each after development.

The main area of concern in the design of a module tester would be the availability of a large area, uniform AM1 illumination source. The module area is likely to be in the range 0.25 to 1.0 m^2. One possible solution is the adaptation of photographic enlargement equipment. No further development of the module test machine is planned in this phase of the program.

I. AUTOMATED MODULE FABRICATION

In order to evaluate potential high-volume module fabrication costs, four module configurations have been evaluated. Three of the module configurations feature very low-cost nonhermetic structures and the fourth is a "hermetic" structure that has a very high probability of meeting or exceeding the 20-year life goal.

The three low-cost nonhermetic structures use plastic encapsulants or sealants. The expected lifetime and barrier properties of the plastic encapsulants or sealants cannot be predicted with high degree of accuracy at this time. It is expected that the studies in Task III of the LSSA project will answer these questions.

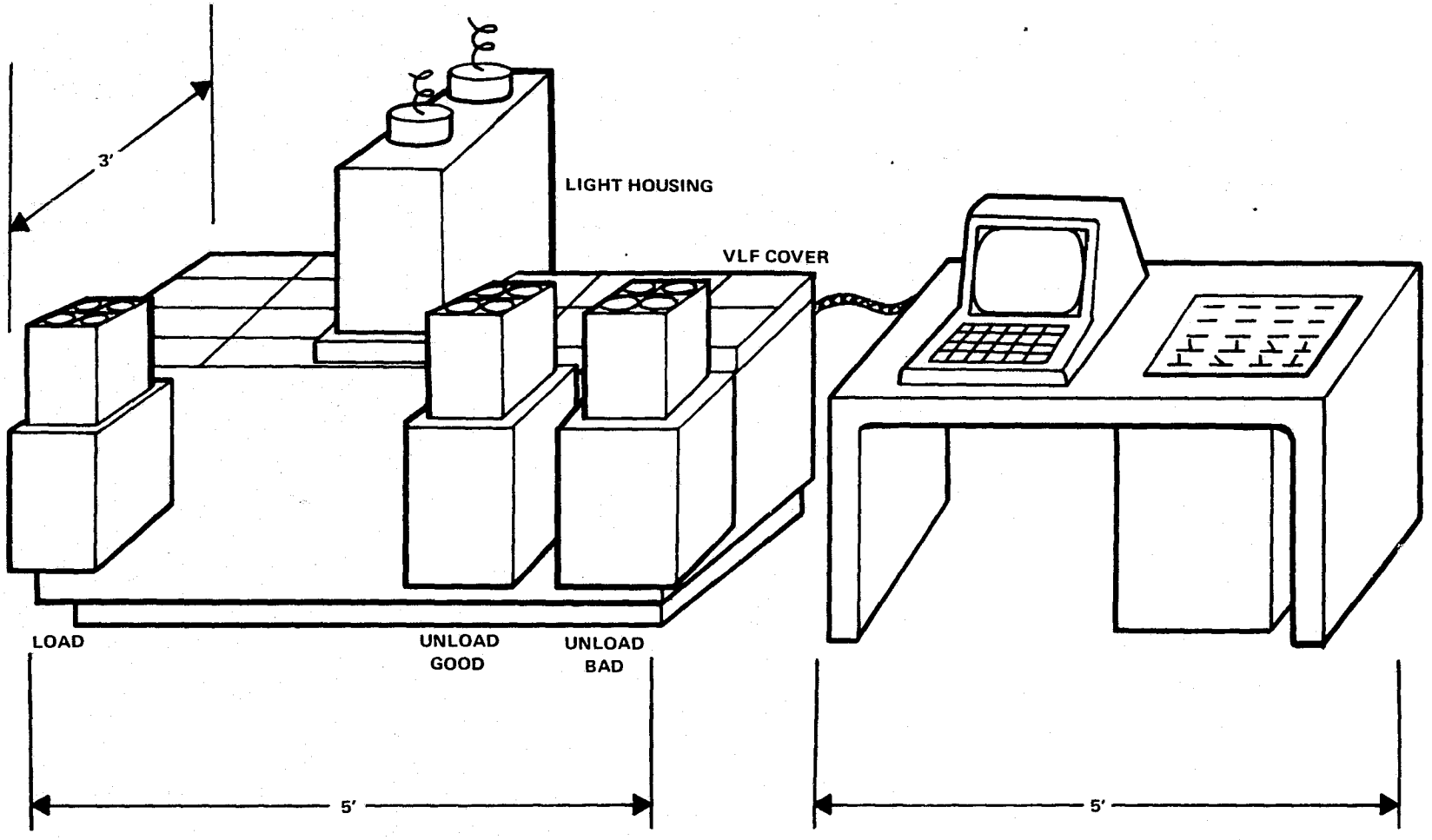


Figure 34. Artist's Rendition of Solar Cell Test Machine and Control Console

Table 9. Photovoltaic Module Test and Handling Time Schedule

Load module onto test tray		5 seconds
Lock and contact		2 seconds
Open shutter, test, close shutter		3 seconds
Eject module		3 seconds
Unload tested module to shipping		5 seconds
	Total	18 seconds

The three structures are: (1) substrate with plastic overcoat, (2) substrate with rigid superstrate, and (3) superstrate with plastic undercoat. Options 1 and 2 were evaluated assuming both N^+ and P^+ contacts are on the back of the cell and can be simultaneously bonded to an interconnect pattern on the substrate. Option 3 assumes a tab or ribbon interconnect is used for electrical connection. Tables 10, 11, and 12 give the estimated material cost per m^2 of module and the labor, overhead (at 100% of labor) and depreciation cost per m^2 of module assuming a throughput rate of 2 m^2 per hour for options 1, 2, and 3. Also, included are capital equipment cost estimates for each option.

Table 10. Option 1 Cost and Capital

COST

Material	**$/m²**
Porcelainized Steel	2.93
Solder Paste	1.20
Encapsulant @ 0.04 mm	.37
Subtotal	**4.50**
Labor	1.75
Overhead	1.75
Depreciation	2.29
TOTAL	**10.31**

CAPITAL – PORCELAIN SUBSTRATE

	$K
Solder Screener	20
Magazine Unloader	10
Magazine	3
Cell Mounter	40
Fixture (holds cells in place)	10
Soldering Oven	20
Clean-up Hood	10
Encapsulate/Cure	40
TOTAL	**153**

Table 11. Option 2 Cost and Capital

COST

Material	$/m^2
Porcelainized Steel	2.93
Solder Paste	1.20
Gasket	0.11
Glass Cover – 3.2 mm	2.63
Subtotal	**6.87**
Labor	1.75
Overhead	1.75
Depreciation	2.29
TOTAL	**12.66**

CAPITAL – PORCELAIN-GLASS SANDWICH

	$K
Solder Screener	20
Magazine Unloader	10
Magazine	3
Cell Mounter	40
Fixture (holds cells in place)	10
Soldering Oven	20
Clean-up Hood	10
Gasket Applier	10
Glass Mounter	10
Cure Oven	20
TOTAL	**153**

For each of these options, the material cost was kept to a minimum value in an attempt to see if the \$10 per m^2 design-to-cost goal could possibly be projected. The lower cost plastics, not the best optical choices, were used. No judgment is or can be drawn at this time regarding the ability of any of these options to meet the 20-year life goal.

It appears that all three of these options have the potential to meet the cost objective when minimum cost and minimum amounts of material are used. While it is doubtful that minimum costs or amounts of material would be optimum, it is encouraging that preliminary costing is this favorable. Of these three options, Option 2 using a glass superstrate and a porcelainized steel substrate is the most attractive technically. Option 2 provides mechanical rigidity, a cleanable hard surface and some protection from mechanical abrasion. Protection from ambient atmosphere is dependent on a plastic adhesive gasket-seal between the glass and the porcelainized steel. In all likelihood this adhesive seal would be the module weak point.

Table 12. Option 3 Cost and Capital

COST

Material	**$/m^2**
Precoated 3.2 mm Glass	3.50
Tabs	1.77
Aluminum wire 0.25 mm dia.	1.24
Encapsulant	0.06
Subtotal	**6.57**
Labor	**1.75**
Overhead	**1.75**
Depreciation	**2.42**
TOTAL	**12.49**

CAPITAL – GLASS SUPERSTRATE

	$K
Magazine Unloader	10
Magazines	3
Tab Applier	25
Tab Bonder	15
Cell Mounter	40
Curing Oven	10
Wire Bonder	40
Encapsulate/Cure	20
TOTAL	**163**

1. LSSA Module

The fourth configuration studied was the "hermetic" module. Because of the high probability that this option could meet the 20-year life goal a more detailed analysis was performed. The major objective for initial design of this module was to obtain lowest cost per exposed m^2 of silicon. The second objective was to have a design which would be suitable for large-scale, high-speed manufacturing, and the third objective was to have a module with long projected lifetime.

The first objective can be achieved by selecting low cost materials and by maximizing the packing density of the solar cells per module.

A design was selected in which the silicon solar cells are directly mounted on the substrate and separate glass cover is used for protection from environment. This design, which is a modification of common flat plate solar-thermal collector requires a positive spacing between the substrate and the cover and separate spacer ring is used for this purpose. Studies with solar-thermal flat plate collectors have shown that decreasing spacing between the transparent cover and the collector plate enhances the thermal losses, therefore, in this case, the spacing was kept as small as possible, however, retaining sufficient spacing for convectional flow between the transparent cover and the front bus bars. Small air volume is also preferred to reduce the elastic deformation of the collector enclosure due to pressure changes caused by temperature fluctuations.

Despite the pressure fluctuation it is desirable to seal the collector cavity as well as possible to prevent the atmospheric corrosion of the interconnection junctions of the solar cell matrix.

To meet the low $/W cost goal, all module designs must have high packing density and generally only low-cost materials are used to reduce the material cost.

High packing density and suitability for mass manufacturing set special requirements for the interconnection arrangement. The hexagonal cells can be packed with minimum spacing, however, this also makes any front to back, P to N, interconnection between the individual cells more difficult. A simple parallel-series arrangement was selected in which the parallel interconnections were made across the cell surfaces with conductor bus bars. The P to N series interconnections are made outside of the parallel connected rows. The assembly of this type of design is easy to automate, and as an added advantage the external conductors reduce the current carrying requirements set for the metallization of the collector pattern trunk lines on the solar cell.

The dimensions of the module were selected to obtain practical size for automated or semiautomated manufacturing and for easy LSSA array assembly and maintenance. With 0.76-mm spacing between the hexagonal cells, 8 cells X 20 cells array can be mounted into 61 X 122 cm^2 substrate and provide sufficient space for series interconnections, external contacts and seal rings. Figure 35 shows the exploded view of proposed LSSA collector module, Design I and Figure 36 shows a cross section of the frame and seal assembly. Figure 37 shows a detail of the back conductor arrangement of Design II.

a. STRUCTURAL MATERIALS

The selected module design dictates some specific requirements for the substrate. The glass cover reduces the thermal dissipation by convection and conduction and blocks the thermal dissipation by infrared radiation through the front cover. To prevent excessive temperature rise in the solar cells, the thermal dissipation through the substrate has to be maximized. Therefore, metallic materials were preferred for this purpose.

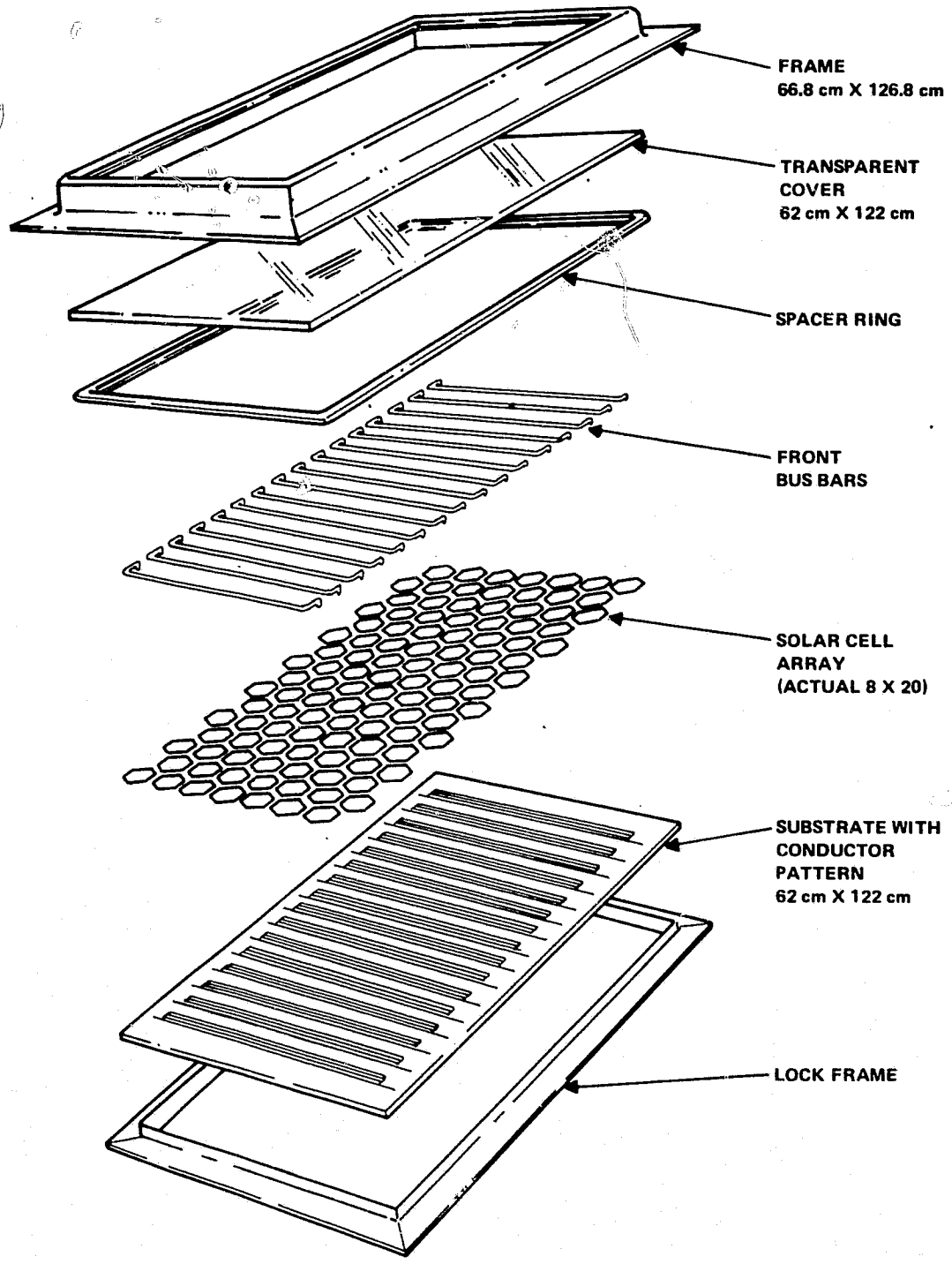


Figure 35. Exploded View of Proposed LSSA Module

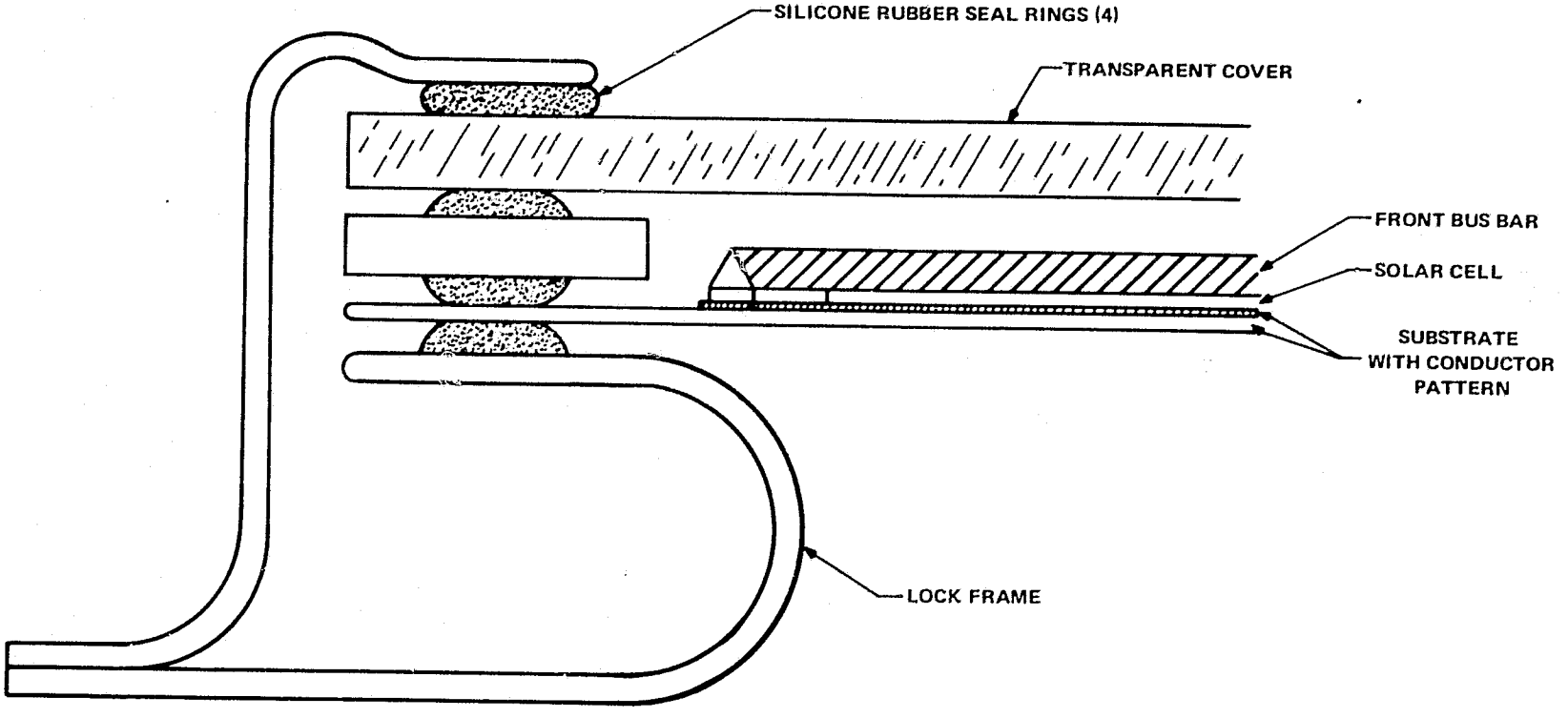


Figure 36. Cross Section of Proposed LSSA Module Frame

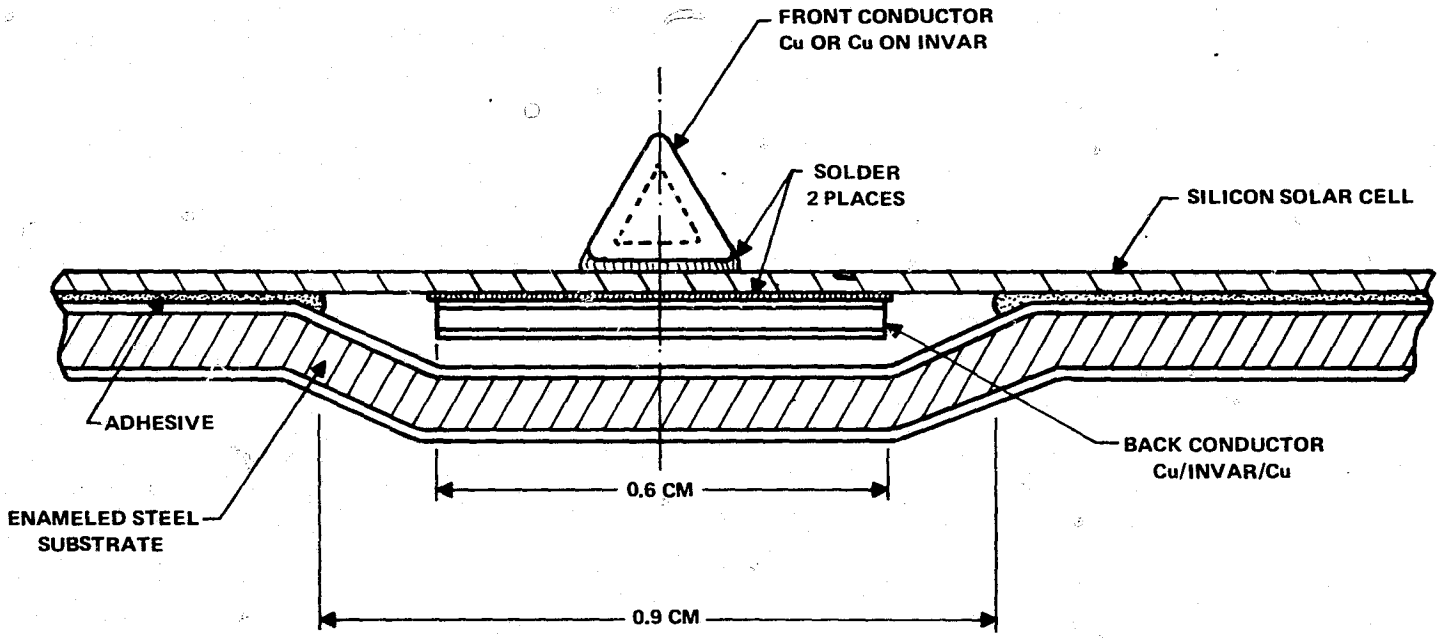


Figure 37. Back Conductor Arrangement of Proposed LSSA Module

Porcelain enameled steel was selected for all structural parts including the substrate. It has a good demonstrated durability in outdoor environment, low per square meter material cost, good thermal conductivity as substrate material and the raw materials are available in large quantities. The good dielectric properties of the porcelain enamel permit direct mounting of the silicon solar cells on the substrate, assuring good thermal contact with the substrate and consequently good thermal dissipation through the substrate.

By having only one material system for all the structural parts offers definite advantages in the module assembly. Notably the same manufacturing equipment and processes can be used for all the structural components and also inventories are reduced.

b. TRANSPARENT COVER

As was pointed out before, glass was selected as cover material, again, because of its demonstrated durability against atmosphere deterioration, good availability and relatively low cost. The fragility of glass is of concern and, therefore, both tempered and untempered glasses are considered in the cost estimation. Regular window glass has a transmittance of 85%. If iron content is reduced as in so-called "Water Clear Crystal #76" transmittance is increased to 91%. Both glasses are considered in cost calculations and the difference in the transmittance is accounted for the $/W values.

c. SEALER STRIPS

Silicone rubber sealer strips, applied to and cured directly on the frame, spacer ring and lock frame, are used to seal the collector from ambient atmosphere. Contacts through the substrate are also sealed using silicone rubber washers.

d. FRONT AND BACK CONDUCTORS

The conductors are soldered or welded directly across the front and the back of the silicon solar cells. In both cases a good electrical conductivity is required to minimize the I^2R losses and the coefficient of thermal expansion of the conductor cannot differ too significantly from that of silicon, $\alpha_{Si} = 2.33 \times 10^{-6}$ cm/cm/°C. Conductor material should be easy to solder. None of the monolithic metals or alloy meet these requirements. However, composite metal technology can be used to manufacture material systems to meet the requirements. For this application the best choice, from the standpoint of manufacturability and cost, is copper-clad Invar.

The coefficient of the thermal expansion of two layer composite metal, parallel to the layers can be calculated from the approximate equation

$$\alpha_c = \alpha_1 + \frac{A_2 E_2}{A_1 E_1} \times \alpha_2 \qquad (54)$$

in which

α_1 = coefficient of thermal expansion of the material with lower α

α_2 = coefficient of thermal expansion of the material with higher α

A_1 and A_2 are cross sectional areas of the component layers

E_1 and E_2 are moduli of elasticity of component metals.

Similarly the resistance per unit of length of the composite metal conductors can be calculated parallel to the layers from the parallel circuit equation.

$$\frac{1}{R_c} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \cdots\cdots \qquad (55)$$

Where R_1, R_2 and R_3 are the respective resistance of the composite metal layers per unit length.

The conductors were dimensioned by permitting a certain I^2R loss per row. For the calculations it was assumed that current pickup was constant per unit length of the conductor, Figure 38. For the length l_1 the I^2R losses can be calculated from equation

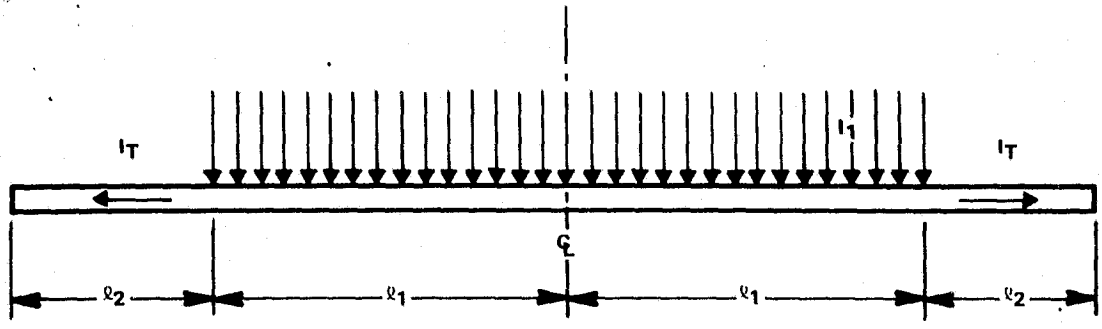
$$\Delta P = \int_0^L (I_L x)^2 R_c \, dx$$

$$\Delta P = \frac{1}{3} I_L^2 R_c L_1^3$$

The total I^2R losses are then

$$\Delta P_T = \frac{1}{3} I_L^2 R_c L_1^3 + I_T^2 R_c L_2 \qquad (56)$$

Assigning specific values for the loss component ΔP, the necessary cross sections of the conductors can be calculated.



ℓ_1 = LENGTH TO WHICH SILICON SOLAR CELLS ARE SOLDERED

ℓ_2 = AVERAGE TERMINATION LENGTH OUTSIDE OF THE CELLS

I_1 = CURRENT PICKUP A/CM

I_T = TOTAL CURRENT FOR HALF LENGTH OF CONDUCTION = $\ell_1 \times I_1$

Figure 38. Schematic of Module Interconnects

1. Front Conductor

Assuming transmittance for the front cover, 13.5% cell efficiency and permitting 2% I^2R loss at peak output, we obtain $R_c = 0.0001757\ \Omega/\text{cm}$ from equation (56). Twenty-five percent of the cross section of the conductor is assumed to be copper and 75% Invar. From equation (55) we obtain

$$\frac{1}{R_c} = \frac{A_1}{\rho_1} + \frac{A_2}{\rho_2} + \ldots\ldots \tag{57}$$

in which

$A_1 = 0.25 \cdot A$ for copper

$A_2 = 0.75 \cdot A$ for Invar

$\rho_1 = 1.7 \times 10^{-6}\ \Omega$-cm for copper

$\rho_2 = 50 \times 10^{-6}\ \Omega$ -cm for Invar

The required cross section of the composite metal conduction

$$A = 0.0408 \text{ cm}^2$$

The front conductor should cause a minimum shadowing of the solar cell and offer a flat surface for soldering to the metallization pattern on the silicon solar cell. An equilateral triangle was selected because some of the incident radiation, blocked by the base of the triangular conductor can be recovered by reflection from the sides of the conductor to the cell surface.

For $A = 0.0409 \text{ cm}^2$, the side of the triangular conductor will be $s = 0.3$ cm.

The apparent coefficient of thermal expansion of the composite metal conductor is calculated from equation (54),

$$\alpha_c = \alpha_1 + k\,\alpha_2$$

in which $k = A_2E_2/A_1E_1$ and

$$\alpha_1 = \alpha_{Invar} = 1.5 \text{ X } 10^{-6} \text{ cm/cm/°C}$$

$$\alpha_2 = \alpha_{Cu} - 16.5 \text{ X } 10^{-6} \text{ cm/cm/°C}$$

$$E_1 = E_{Invar} = 21.4 \text{ X } 10^6 \text{ lb/in}^2$$

$$E_2 = E_{Cu} = 16.0 \text{ X } 10^6 \text{ lb/in}^2$$

$$A_1 = 0.75 \text{ A}$$

$$A_2 = 0.25 \text{ A}$$

$$\alpha_c = 5.7 \text{ X } 10^{-6} \text{ cm/cm/°C}$$

2. Back Conductor

Two different mounting techniques are considered. In the first one, tin-lead solder is used to bond the silicon solar cells to the porcelain enameled substrate and the tin-lead pattern is at the same time used as the conductive path. The second design uses a separate composite metal conductor rail which is tin-lead soldered to the back sides of the silicon solar cells. The cells are adhesively bonded to the porcelain enameled steel substrate.

Design I

The conductor-bonding pattern is silk screened to the porcelain enamel surface using copper or silver ink. The tin-lead-(silver) bonding and conduction layer is wave soldered to the printed pattern. For the back conductors it would be desirable if the I^2R losses would not exceed 1.5%. However, the solder stripes become too wide for the 1.5% I^2R losses. Therefore, for Design I, 2% I^2R loss in back conductor is used in calculations, and also the conductivity of the silk screened copper pattern has to be included in the calculation. Using equation (57) we obtain

$$\frac{1}{R_c} = \frac{w \cdot t_1}{\rho_1} = \frac{w \cdot t_2}{\rho_2} \tag{58}$$

$t_1 = 0.0125$ cm for tin-lead solder

$t_2 = 0.00125$ cm for silk screened pattern

$\rho_1 = 14.5 \times 10^{-6}$ Ω-cm for Sn-40 Pb solder

$\rho_2 = 2 \times 10^{-6}$ Ω-cm for silk screened copper

$R_c = 0.000252$ Ω-cm for 2% I^2R loss

Above calculation gives w = 2.6 cm or four 0.65 cm wide parallel stripes of tin-lead solder for each cell row.

Design II

The width of the back conductor was selected to be 0.6 cm. The conductivity of the 60% Sn-40% Pb solder, which is used to solder the conductor to the back metallization of the silicon solar cell is taken into consideration, however, the contribution of the back metallization of the silicon solar cell is disregarded as in the previous calculations

$$\frac{1}{R} = \frac{w \cdot t}{\rho_1} + \frac{w \cdot t_2}{\rho_2} + \frac{w \cdot t_3}{\rho_3} \tag{59}$$

$t_1 = 0.25\ t$ = total thickness of copper layers

$t_2 = 0.75\ t$ = thickness of Invar layer

$t_3 = 0.0125$ cm = thickness of tin-lead solder

$\rho_3 = 14.5 \times 10^{-6}\ \Omega$-cm for tin-lead solder

$R_c = 0.000189\ \Omega$/cm for 1.5% I^2R loss

The back conductor thickness from the above equation becomes:

$$t = 0.06 \text{ cm}$$

The coefficient of the thermal expansion is the same $\alpha_c = 5.7 \times 10^{-6}$ cm/cm/°C as for the triangular front conductor, because the area ratio between the copper and Invar are the same.

e. LOCK FRAME

Lock frame is designed so that it is elastically formed in the assembly providing necessary spring action to compensate for possible relaxation of the silicone rubber seals. It is pressed to the frame, simultaneously tensioning it, and riveted to the place using hollow rivets.

f. COMPONENT MANUFACTURING

For the following components, labor and overhead cost are included in Tables 13 and 14 as a fraction of the material cost.

1. Frame and Lock Frame

Starting materials: enameling steel strip

porcelain enamel frit

silicone rubber sealant

Slit to width

Stamp fastener holes

Roll form

Cut to length

Weld corners

Table 13. Estimated Material and Component Cost of Proposed LSSA Module, Design I

	Item	Low $/mod	Low $/W	Probable $/mod	Probable $/W	High $/mod	High $/W
1.	Frame						
	Enameled Steel	1.35	0.020	1.72	0.026	2.45	0.034
2.	Glass Cover						
	Ann. window	2.66	0.040				
	Temp. window			3.84	0.057		
	Temp. low iron					9.28	0.130
3.	Spacer Ring						
	Enameled Steel	0.66	0.010	0.88	0.013	1.27	0.018
4.	Sealants 4 places	1.56	0.023	1.88	0.028	2.19	0.031
5.	Substrate						
	Enameled Steel	3.84	0.057	5.04	0.075	8.00	0.112
6.	Front conductor	0.60	0.009	0.75	0.011	1.00	0.014
7.	Substrate conductor						
	a. Screen print						
	Pattern						
	Copper ink	3.59	0.054				
	Average			5.60	0.084		
	Silver ink					7.63	0.107
	b. Tin-lead conductor	2.24	0.034	3.12	0.047	4.01	0.056
8.	Connectors	0.75	0.011	1.00	0.015	1.50	0.021
9.	Lock Frame						
	Enameled Steel	1.60	0.024	2.06	0.031	2.94	0.041
10.	Lock frame fasteners	0.36	0.005	0.72	0.011	1.08	0.015
	Subtotal	18.85	0.282	25.89	0.387	41.35	0.579
	Assembly L + OH	2.37	0.035	3.16	0.047	4.74	0.066
	TOTAL M + L + OH	21.22	0.317	29.05	0.434	46.09	0.645

Table 14. Estimated Material and Component Cost of Proposed LSSA Module, Design II

	Item	Low $/mod	Low $/W	Probable $/mod	Probable $/W	High $/mod	High $/W
1.	Frame						
	Enameled Steel	1.35	0.020	1.72	0.026	2.45	0.034
2.	Glass Cover						
	Ann. window	2.66	0.040				
	Temp. window			3.84	0.057		
	Temp. low iron					9.28	0.130
3.	Spacer ring						
	Enameled steel	0.66	0.010	0.88	0.013	1.27	0.018
4.	Sealants 4 places	1.56	0.023	1.88	0.028	2.19	0.031
5.	Substrate						
	Enameled steel	3.84	0.057	5.04	0.075	8.00	0.112
6.	Front conductor	0.60	0.009	0.75	0.011	1.00	0.014
7.	Back conductor	2.01	0.030	2.41	0.036	2.82	0.039
8.	Adhesive	0.81	0.012	1.22	0.018	1.62	0.023
9.	Connectors	0.75	0.011	1.00	0.015	1.50	0.021
10.	Lock frame						
	Enameled steel	1.60	0.024	2.06	0.031	2.94	0.041
11.	Lock frame fasteners	0.36	0.005	0.72	0.011	1.08	0.015
	Subtotal	16.20	0.241	21.52	0.321	34.15	0.478
	Assembly L + OH	3.64	0.054	4.85	0.073	7.28	0.102
	TOTAL M + L + OH	19.84	0.295	26.37	0.394	41.43	0.580

Clean

Prepare surface for enameling

Apply enamel frit

Fire

Inspect

Apply sealant bead

Cure

→ To the assembly line

2. Spacer Ring

Starting materials: cold drawn carbon steel rod

porcelain enamel frit

silicone rubber sealant

Cut to length

Weld corners

Clean

Prepare surface for enameling

Apply enamel frit

Fire

Inspect

Apply sealant beads

Cure

→ To the assembly line

3. Substrate

Starting materials: enameling steel strip

porcelain enamel frit

Cut in length

Punch connector holes

Draw back conductor grooves (optional)

Clean

Prepare surface for enameling

Apply enamel frit

Fire

Inspect

→ To the substrate assembly area

4. Front Conductor

Starting materials: Invar cored copper 75/25 area ratio

Tin

Draw into profile

Clean

Tin electroplate

Reflow

Draw to mirror finish

Clean

→ To the cell row manufacturing area

5. **Back Conductor (Design II)**

Starting materials: copper clad Invar strip 25/75

area ratio

tin

Tin electroplate

Slit

Clean

→ To the cell row manufacturing area

6. **Connector Lugs, Silicon Gaskets for connectors and Fastening Rivets purchased from outside vendors.**

7. **Cover Glass**

Cut

Clean

→ To the assembly line

g. CELL ROW MANUFACTURING, DESIGN II

Cell rows are soldered and formed in automated manufacturing line. For further process steps, rows are supported by reusable carriers.

	Rate per labor hour				L + OH $7/hr
	Cell	Rows	Modules	Hrs/mod	$/mod
Solder cell rows	720	90	4.5	0.222	1.55
Cut					
Bond ends					
Trim to length					
Clean		600	30	0.033	0.23
Test		360	18	0.056	0.39
Subtotal					2.17

h. SUBSTRATE ASSEMBLY

1. Design I

The manufacturing of back conductor pattern on substrate is included in the assembly operation.

	Rate per labor hour				L + OH $7/hr
	Cell	Rows	Modules	Hrs/mod	$/mod
Clean substrate			360	0.003	0.02
Silk screen pattern			240	0.004	0.03
Dry + fire			240	0.004	0.03
Wave solder conductors			240	0.004	0.03
Clean + inspect			60	0.017	0.12
Solder cell rows	960	120	6	0.167	1.17
Bond front bus bars		240	12	0.083	0.58
Solder interconnect		500	25	0.040	0.28
Clean ultrasonically			60	0.017	0.12
Assemble connector lugs			120	0.008	0.06
Test			360	0.003	0.02
Subtotal					2.46

2. Design II

	Rate per labor hour				L + OH $7/hr
	Cell	Rows	Modules	Hrs/mod	$/mod
Apply adhesive to cells	3600	450	22.5	0.044	0.31
Bond to substrate		120	6	0.167	1.17
Solder interconnect. (weld)		500	25	0.040	0.28
Clean ultrasonically			60	0.017	0.12
Assemble connector lugs			120	0.008	0.06
Test			360	0.003	0.02
Subtotal					1.96

i. MODULE ASSEMBLY , DESIGNS I AND II

Module assembly is done in a continuous assembly line.

	Modules/ labor hr	Hrs/mod	L + OH $7/hr $/mod
Assemble	10	0.1	0.70
Place frame			
Insert glass			
Insert collector plate			
Insert spacer ring			
Apply tensioning load			
Rivet			
Remove from assembly tool and line			
Test	360	0.003	0.02
Subtotal			0.72

j. MODULE ASSEMBLY COST

Tables 13 and 14 give the estimated total material, labor and overhead cost, excluding the silicon solar cells and depreciation. Cost will be shown $/module and $/watt output. Effective peak output of cell per unit area is

$$P_T = \eta_g \cdot \eta_{tb} \cdot \eta_{bb} \cdot \eta_c \cdot I_o \tag{60}$$

η_g = transmittance of the glass

η_{fb} = 1-front conductor losses

η_{bb} = 1-back conductor losses

η_c = efficiency of Si solar cell, includes shadowing by metallization pattern and front conductor

η_g = 0.85 window glass

η_g = 0.91 Water White Crystal #76

$\eta_{fb} = 1 - 0.02 = 0.98$

$\eta_{bb} = 1 - 0.015 = 0.985$

$\eta_c = 0.135$

$I_o = 0.1$ W/cm^2

For Window glass $P_T = 0.01108$ W/cm^2

For W.W.C #76 $P_t = 0.01186$ W/cm^2

In calculating the module output, the total cell area is considered, because the shadowing losses of the metallization and the front bus bar are accounted for in the cell efficiency.

$$P_M = n A_c P_T \tag{61}$$

n = number of cells in module = 160

A_c = area of cell cm^2 = 37.71 cm^2

P_T = effective cell output W/cm^2

For window glass P_M = 66.85 W/module

For Water White Crystal #76 P_M = 71.56 W/module

J. SOLAR CELL PROCESS STEP COSTS

Processing cost data has been generated on a large number of potentially useful process steps. These data are useful for comparing costs for various solar cell process alternatives. These data are calculated on the basis of processing 10.2-cm single-crystal wafers. All costs are based on 1976 dollars with processes projected to be available in the 1981-1982 time period for the implementation into a 1985 500 MW per year factory. Some of the processes require development

but no major technical innovations are assumed. Not all process steps have been experimentally verified at Texas Instruments, but all processes are available in the industry and are either in use in a simplified form or under active investigation.

Material costs include all materials and supplies consumed in the operation. No distinction is made for materials that appear in the final product versus those that are discarded. No allowances are made for material recovery except in places where a chemical may be reused several times, such as a refluxing solvent or an etch bath that is used many times. In general, reclamation costs are considered to be too expensive to be cost effective.

Labor costs are based on a production operator pay rate of $3.50 per hour with no allowance for overtime or shift premium. The overhead (OH) rate of 100% is intended to cover all direct overhead costs such as F.I.C.A., insurance, etc., supervisory and clerical costs and allow for a slight fraction to cover overtime or shift premiums. Labor costs are calculated on the basis of the hourly throughput rate times 0.8. The 20% reduction in throughput rate covers meal and rest breaks plus an allowance for equipment repair and maintenance.

Depreciation is calculated on a straight line 7-year depreciation at 9% annual interest. The depreciation in the first year is the same as the depreciation in the seventh year. Depreciation is based on a 50-week, 7-day, 24-hour operating year. No other allowance is made for vacation or holiday shutdown.

Process yield is the physical yield at the particular process step and no functional or parametric yield is taken before the cell test step. Typical process step yields are 98% or better.

Cell efficiency, in general, is not a function of the individual process step but rather is a function of the composite solar cell process. In most cases, a solar cell process capable of yielding cells of 13.5% efficiency (AM1) is assumed. Higher cell efficiencies would, of course, yield lower cost per watt.

Table 15 is a compilation of the process step cost breakdown. The subsections of Table 15 are cleaning and surface preparation, junction formation, metallization, AR coating, encapsulation and test. A brief discussion of each subsection follows.

1. Cleaning and Surface Preparation

As a general rule, acid cleanup and etching operations are more expensive than equivalent nonacid operations. With the exception of texture etching, all operations assume a polished single-crystal surface. Texture etch costs include a preliminary etch polish operation to remove saw damage.

Table 15. Solar Cell Process Step Cost Breakdown

Process Step		$/W					Process (%) Yield	Investment Cap.	Cell Eff. (%)	Thruput W/hr	Thruput MW/yr	$K Capital Cost
		Mat'l	Labor	O.H.	Dep.	Total						
Cleaning and Surface Preparation												
Scrubbing (Detergent)		.0001	.0088	.0088	.0033	.0210	98	.0167	13.5	4x125	3.36	56
Scrubbing (Alcohol)		.0125	.0088	.0088	.0033	.0334	98	.0167	13.5	4x125	3.36	56
Cleanup — Acid — H_2O		.0043	.0029	.0029	.0015	.0116	98	.0074	13.5	1500	10.0	75
Cleanup Solvent — Acid — Solvent		.0092	.0088	.0088	.0044	.0312	98	.0223	13.5	500	3.36	75
Degrease — Refluxing Solvent		.0001	.0044	.0044	.0035	.0124	99	.0179	13.5	500	3.36	60
Ultrasonic Clean — Solvent		.0002	.0044	.0044	.0030	.0118	99	.0149	13.5	500	3.36	50
Reverse Sputter (50 Å)		.0002	.0023	.0023	.0054	.0102	99	.0271	13.5	1920	12.9	350
Etch Polish — Acid		.050	.0088	.0088	.0044	.0720	98	.0223	13.5	500	3.36	75
Etch Polish — NaOH		.0010	.0088	.0088	.0030	.0216	98	.0149	13.5	500	3.36	50
Oxide Etch — Acid		.0031	.0088	.0088	.0044	.0251	99	.0223	13.5	500	3.36	75
Oxide Etch — Plasma		.0002	.0088	.0088	.0039	.0217	99	.0194	13.5	500	12.9	250
Texture — H_2NNH_2		.0178	.0088	.0088	.0044	.0398	98	.0223	13.5	500	3.36	75
Texture — N_aOH		.0014	.0088	.0088	.0030	.0220	98	.0149	13.5	500	3.36	50
Junction Formation												
Spin-on — Polymer	2 sides	.0023	.0146	.0146	.0059	.0374	99	.0297	13.5	300	2.02	60
Spray-on — Polymer	2 sides	.0023	.0146	.0146	.0059	.0374	99	.0297	13.5	300	2.02	60
Drive-in (diffusion)		.0010	.0073	.0073	.0017	.0173	99	.0087	13.5	600	4.04	35
Silicon Source		.090	.0073	.0073	.0017	.1063	99	.0087	13.5	600	4.04	35
Gas Depositing & Diffusion		.030	.0073	.0073	.0022	.0468	99	.0111	13.5	600	4.04	45
Ion Implant	1 side	.010	.0182	.0182	.0185	.0649	99	.093	13.5	240	1.61	150
Ion Implant (advanced)	1 side	.010	.0088	.0088	.0178	.0454	99	.089	13.5	500	3.36	300
Spin-on Polymer	1 side	.0012	.0073	.0073	.0030	.0188	99	.0149	13.5	600	4.04	30
Metallization												
Vacuum Deposition Ti/Cu	1 side	.035	.0194	.0194	.0513	.1251	98	.265	13.5	225	1.51	400
Vacuum Deposition Ti/pd/Ag	Front	.060	.0194	.0194	.0513	.1501	98	.265	13.5	225	1.51	400
Vacuum Deposition Ti/Pd/Ag	Back	.060	.0194	.0194	.0513	.1501	98	.265	13.5	225	1.51	400
Thick Film, Ag	Front	.0024	.0036	.0036	.0012	.0108	98	.0062	13.5	1200	8.06	50
Thick Film, Ag	Front	.0024	.0036	.0036	.0012	.0324	98	.0062	13.5	1200	8.06	50
Thick Film, Base Metal	Front	.0015	.0036	.0036	.0012	.0099	98	.0062	13.5	1200	8.06	50
Thick Film, Base Metal	Back	.0150	.0036	.0036	.0012	.0234	98	.0062	13.5	1200	8.06	50

Table 15. Solar Cell Process Step Cost Breakdown (Continued)

Process Step	$/W					Process (%) Yield	Investment Cap.	Cell Eff.(%)	Thruput W/hr	Thruput MW/yr	$K Capital Cost
	Mat'l	Labor	O.H.	Dep.	Total						
AR Coating											
Oxide Growth	.0005	.0073	.0073	.0017	.0168	99	.0087	12.0	600	4.03	35
Spin-on	.0023	.0073	.0073	.0030	.0199	99	.0148	13.5	600	4.03	60
Evaporate	.004	.0109	.0145	.0145	.0403	99	.0744	13.5	400	2.69	200
Sputtering	.004	.0109	.0109	.0145	.0403	99	.0074	13.5	400	2.69	200
Bake (Spin-on)	0.0	.0073	.0073	.0015	.0161	99	.0074	13.5	600	4.03	30
Encapsulant											
Glass Superstrate	.066	.0219	.0219	.0241	.1339	96	.1213	13.5	200	1.34	163
Glass with Substrate	.069	.0219	.0219	.0226	.1354	96	.1138	13.5	200	1.34	153
Substrate with Coating	.045	.0219	.0219	.0226	.1114	96	.1138	13.5	200	1.34	153
Hermetic	.247										
Test											
Cells	0.0	.0044	.0044	.0030	.0118	85	.0149	13.5	1000	6.72	100
Modules 80W	0.0	.0003	.0003	.0006	.0012	98	.0010	13.5			

2. Junction Formation

Junction formation represents one of the most critical operations in the solar cell process sequence. Diffused layer resistivity, junction depth, profile, and surface condition are all critical parameters in the control of a high efficiency solar cell process. Both an N^+ and a P^+ layer must be formed in an N^+PP^+ solar cell structure. The P^+ layer forms a region for ohmic contact to the P base region and forms the back surface field. The N^+ layer must form a good diode for efficient solar cell operation.

Processes that allow independent introduction of the N^+ and P^+ layers are desirable. From this standpoint, polymer dopant and ion implantation processes would be favored, assuming equivalent junction parameters. Integrated circuit open tube gas deposition-diffusion techniques, introduce impurity atoms on all exposed surfaces and are not cost effective unless special processes are used, e.g., oxide mask the back side during front-side diffusion or impurity compensation such as Al alloying through an N^+ layer.

Ion implant and polymer dopant processes must be followed by a drive-in diffusion or thermal activation step. Both of these techniques allow one to independently introduce N-type and P-type impurities on opposite surfaces followed by a single drive-in diffusion step.

Ion implantation is well advanced in the semiconductor industry and has found wide acceptance in certain low-dose applications. High-dose applications, such as solar cells, suffer from a low throughput per capital dollar and significant advances in beam current and wafer handling techniques must occur before this technique will become cost effective for low cost operations.

Polymer dopant or paint-on techniques have been used in the semiconductor industry for well over 10 years as a low technology process. In recent years, commercial formulations and proprietary formulations have been developed for specific applications such as diffusion under exitaxial films. Process control is good ($< \pm$ 10%) within the range of interest for solar cells, 30-100 $\Omega/\square$ diffused layer resistivity. Existing formulations suffer from a shelf life problem with typical shelf lives from one month to six months. In a solar cell factory using polymer dopant, the dopant formulation should be included in the factory to ensure good control over product quality.

Techniques such as epitaxy and alloying are too expensive to be considered for low-cost solar cell manufacture. Back side alloying, e.g., Al may have a place in low-cost solar cell manufacture.

3. Metallization

Vacuum deposition, either evaporation or sputtering is too expensive for low-cost solar cell manufacture. Vacuum deposition is wasteful of material, low in throughput, and high in depreciation when compared to thick film or electroless deposition techniques. Mask stencils are more cost effective than photolithography and etching but mask costs and mask cleaning are costly.

Thick-film technology is well developed for hybrid circuit applications. This technology requires further development, however, before it can be readily applied to direct metal-silicon contacts. Present commercial ink or paste formulations typically contain precious metals, Ag, Au, or Pt, and a glassy matrix for adhesion to a ceramic surface. Low-cost inks for solar cell application should ideally contain cheaper base metals and probably no glassy matrix. A small amount of development is in progress to develop inks for solar cell applications. More work needs to be done in this area. High throughputs and low capital investments are typical in this field.

Electroless plating is another low-cost metallization process alternate. Electroless plating techniques are well known in the semiconductor industry. Capital costs are low and throughput is generally high. Typical applications of electroless Ni in the semiconductor industry has been on deep junction devices. Application on shallow junction solar cells will require some development. The key area of concern in the application of electroless plating in low-cost processing schemes is the ability to deposit a metal pattern directly without resorting to masking or etching techniques. Further development should be encouraged in the area of patterned electroless depositions. A technique known as Photo-Impeded-Metal Deposition, PIMDEP, appears to offer a fruitful area for future development.

4. AR Coating

Both spin-on (or spray) and vacuum deposition techniques appear to offer attractive process alternatives. Oxide growth is low cost but suffers from the restriction that the only convenient oxide that can be grown on Si is SiO_2, a relatively low index material. Low index SiO_2 on a textured surface may be acceptable in light of the low cost for oxide growth.

Attractive AR coating will feature high index films ($\approx$ 2.0) and in general, single layers will be more cost effective than multiple layers.

5. Encapsulation

Array encapsulation presents a major cost and reliability barrier. Low-cost approaches using conformal coating do not appear to offer a high probability of achieving the 20-year life goal. Conformal coatings are material intensive in cost, and thick coatings do not appear to offer significant improvement in life time.

The highest probability of achieving a 20-year life module appears to require a costly hermetic encapsulation. This approach is very material intensive and does not, at this time, meet the cost goals. Further investigation is required to find an acceptable compromise between the low-cost high-risk and the high-cost low-risk approaches.

At this time, the closest approximation to an acceptable encapsulation scheme is the glass with substrate (porcelainized steel) approach using a plastic seal at the edges.

6. Test

Solar cell and module test concepts appear to be cost effective and well within existing technology capabilities. Solar cell test yields projected at 85% should be improvable with a well controlled process and good silicon sheet material. Cell test yields in excess of 90% should be possible with a well engineered solar cell process and good process control.

The goal of the solar cell process and the cell test should be to produce a single class of high-quality solar cells. One should avoid the trap of a "cheap" process that produces a distribution. A "cheap" process should not be confused with a low-cost process.

K. LOW COST SILICON SOLAR CELL MODULE COSTING

The design of a low-cost silicon solar cell process requires a number of choices that must be made within the context of some set of constraints. The constraints are not invariant but will change with time and advances in the various process technologies, design windows, and material technologies. Task 4 of the LSSA Project calls for an assessment of existing technologies and an extrapolation into the near future for a guideline to a 1985 high-volume production base. Within these constraints a further set of boundary conditions or philosophies can be imposed. These are:

1) High cell efficiency is a must
2) All process steps must be demonstrated no later than 1982
3) All process steps should be additive
4) The process should yield a tight distribution
5) All process steps that are in a feasibility stage must have an alternate fall-back that is process compatible.

While these conditions are mostly self-evident, a few explanatory comments are in order.

Cell efficiency and module efficiency are key factors driving cost. While some processes may yield cheap solar cells, the module costs and system costs are area related and drive the module and system costs to unacceptable levels. This cost analysis assumes a minimum cell efficiency of 13.5% at AM1.

In order to impact a 1985 high-volume production goal, all process steps must be operating production processes by 1985. The scale-up to a 500 MW annual run rate will require a 2 to 3-year lead time. As a practical corollary, any factory must be capable of absorbing new advances in technology or technical obsolescence will occur.

For minimum cost to be achieved, no extraneous operations should be allowed. Additive processes are those that lead in a direct path to the final product. Process steps such as a deposition followed by partial removal are to be avoided, if possible. An alternate process that would deposit a patterned material is preferred.

A well-controlled process should yield a product with a narrow distribution of parameters. Testing and sorting at the end of the process is a poor substitute for proper process design and control. A factory that relies on the sale of "seconds" to be economically viable is a poorly designed factory.

Some process steps that are included will still be in a feasibility stage. These process steps must have an alternate available so that process development does not depend totally on the success of one or more critical steps. This provides a redundancy that allows rapid advancement of technology with minimum risk.

From the process step cost analysis, one can construct a series of solar cell processes that will work. On the basis of minimum cost and minimum technical risk, the following baseline process sequence was chosen. The process flow and individual process step costs are shown in Figure 39. Yield numbers given for each process step are basically mechanical yield with all electrical yield accounted for at the cell test operation. The column on the far right is the cost per watt yielded through each process operation. The cumulative yielded process and test cost is given at the bottom of the column. The yielded cost of $0.2559 per watt is the cost for cell processing and cell testing and does not include the cost of silicon sheet or module test and assembly. The totals across the bottom are the unyielded material, labor, overhead and depreciation costs.

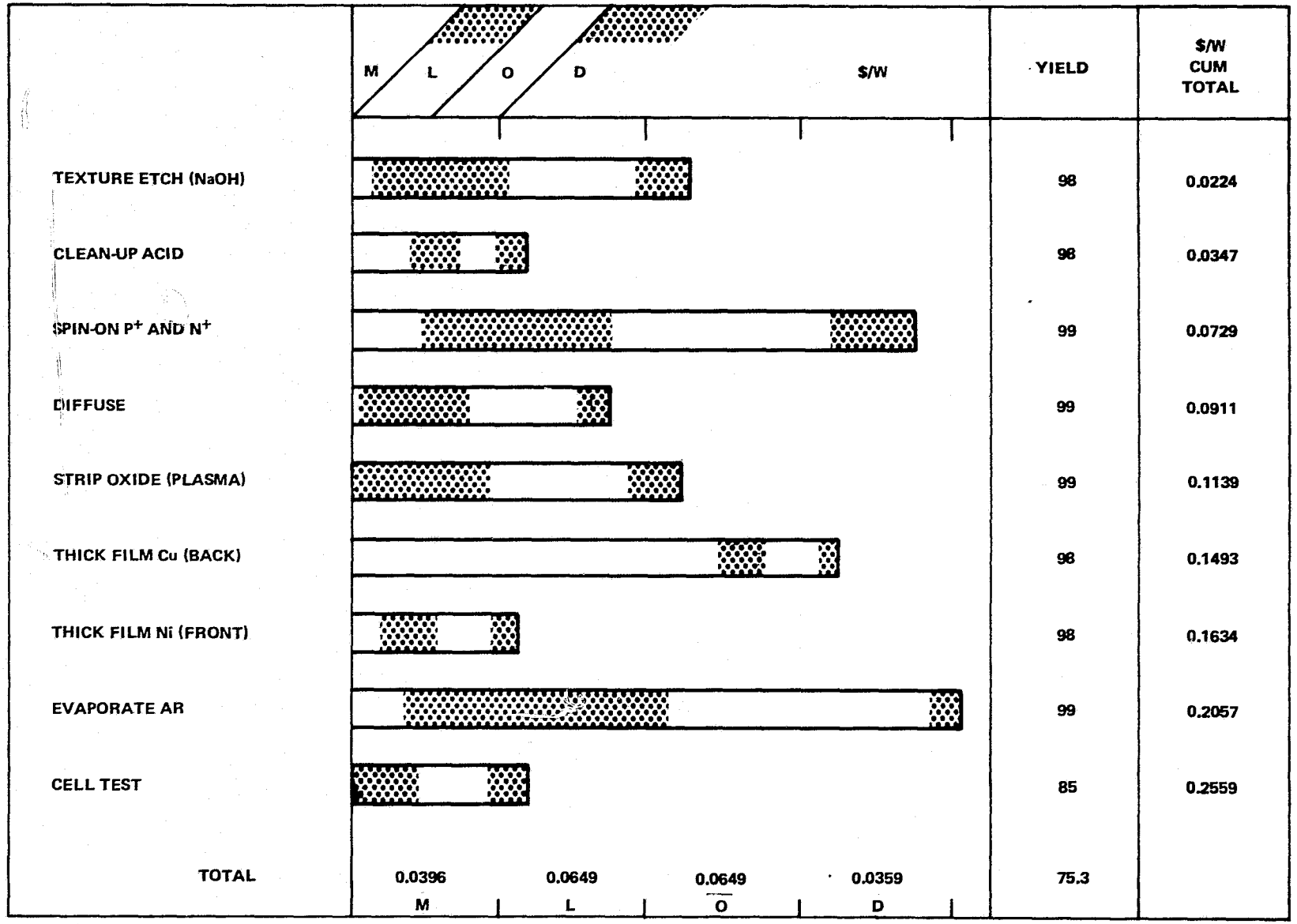


Figure 39. Baseline Low-Cost Cell Process

Several interesting points are evident from inspection of Figure 39. Almost two-thirds of the total material cost is due to the back-side metallization step alone. Since the material cost is directly related to the area printed, a reduction in the area of the back-side metallization should be investigated. The use of spin-on (or spray-on or paint-on) polymer dopant to form the N^+P junction and the P^+ back-side field in one operation is a significant cost reduction.

The two process steps that require alternate backup processes are junction formation and metallization. Figures 40 and 41 give the process flow, process step yield, cumulative yielded cell process and test cost, and unyielded totals for material, labor, overhead and depreciation for Baseline Process – Alternate 1 (Junction), Figure 40, and Baseline Process – Alternate 2 (Metallization), Figure 41. Process steps that differ from the Baseline Process are italicized. All process costs are sensitive to process step and test yields. Improvements in any of these yields will favorably impact cost.

The baseline process and alternates 1 and 2 represent solar cell processes that can be achieved by extensions of today's technology. They do not meet the design-to-cost goals for the LSSA Project goal by more than a factor of two. Labor costs could be impacted by full automation with the ultimate low-cost potential for each process approaching the material cost for that process as a minimum (at infinite throughput labor cost approaches zero and depreciation approaches zero). Material costs will not decrease unless cell efficiency increases. The factor-of-two discrepancy between design-to-cost goals and projected process costs can be overcome by improved throughput and by improved cell efficiency.

Module assembly and test costs present a more serious but not intractable cost barrier. Two module configurations were chosen from the modules discussed in an earlier section of this report. The primary module considered is called the hermetic or LSSA module. This design represents an approach based on a 20-year life requirement. All construction materials are designed to withstand outdoor weathering with minimum degradation. The solar cells are protected from weathering by the module enclosure. All cell interconnects are part of the module fabrication process. Two primary construction materials were chosen, glass, and procelainized steel. These choices are based on cost and durability.

The second option consists of a minimum cost design with no provision made to assure 20-year life. This low-cost option consists of a porcelainized steel substrate and an overcoat of low-cost silicone plastic. Minimum overcoat thickness is used to minimize cost. Studies under Tasks 3 and 5 of the LSSA Project indicate that silicone or plastic overcoats will not provide protection from weathering over long periods of time. The difference in cost between these two options represents the cost incurred to assure weatherability. Further detailed investigation of module construction is necessary.

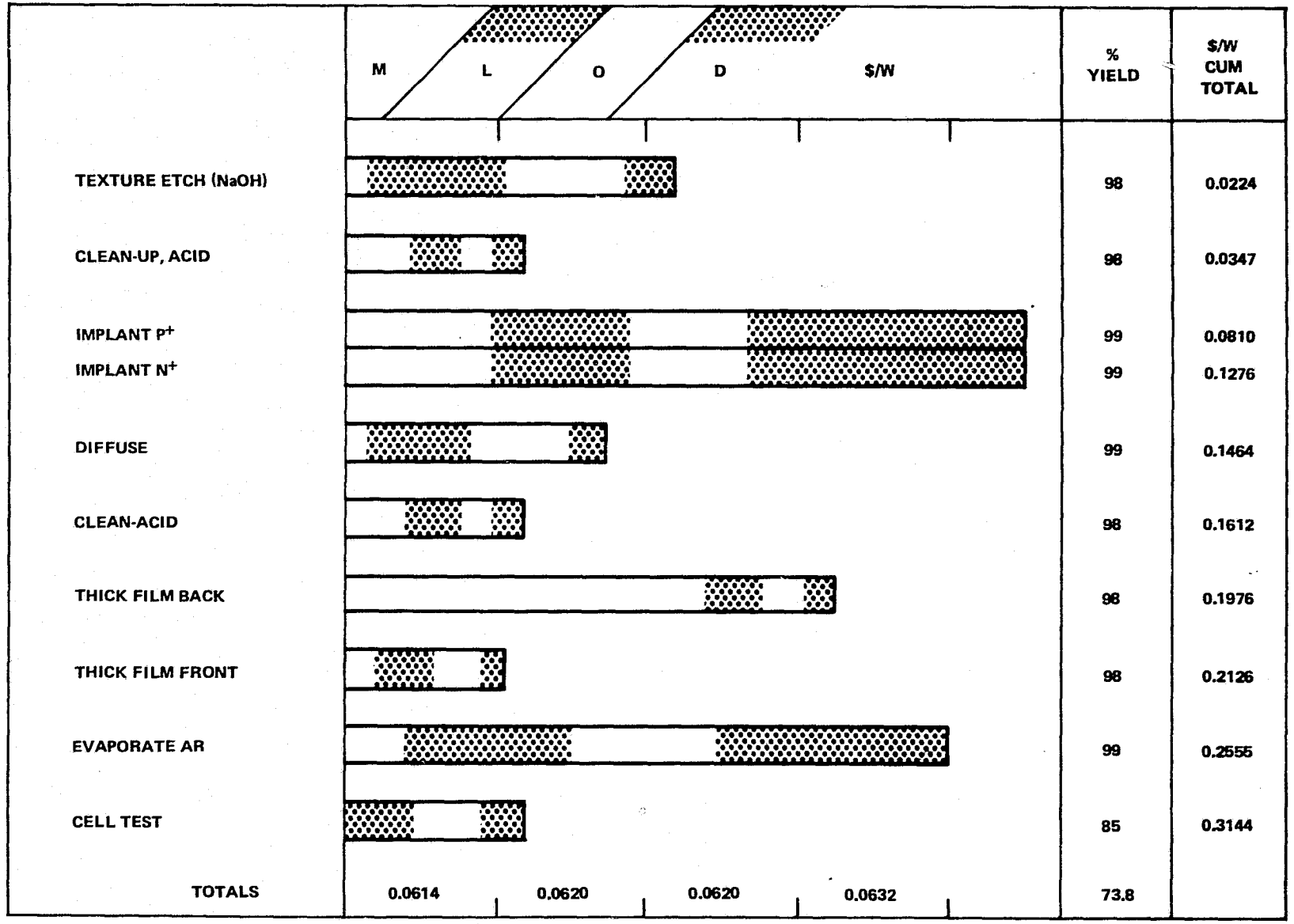


Figure 40. Baseline Low-Cost Solar Cell Process – Alternate 1 (Junction)

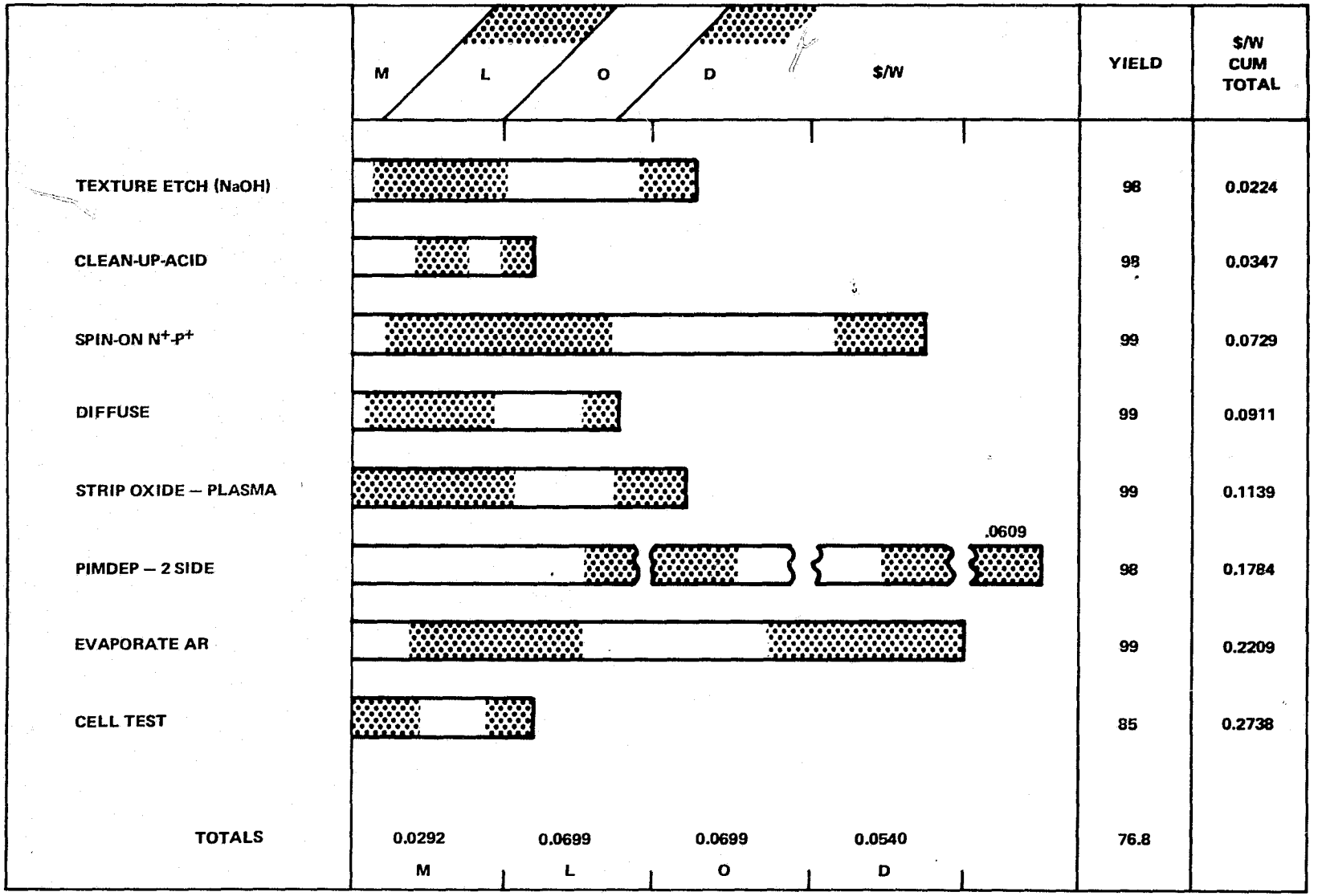


Figure 41. Baseline Low-Cost Cell Process – Alternate 2 (Metal)

In this assessment, all piece parts that go into module construction are treated as purchased material. Some economies could be achieved by fabricating the piece parts in the solar cell module factory. Module add-on costs are given below.

	$/(W)				
	M	**L**	**O**	**Dep.**	**Total**
Hermetic Module	0.247	0.0101	0.0101	0.0048	0.272
Low-Cost Module	0.069	0.0219	0.0219	0.0226	0.1354

The above module add-on costs exceed the design-to-cost goals by a factor of two or three. Since these costs are very sensitive to cell and module efficiency and the final design is still preliminary, this difference from 1985 cost goals is not considered serious.

Overall solar cell process, test, module fabrication and test costs are summarized below for the baseline low-cost solar cell process and alternates 1 and 2 coupled with the hermetic module and the low-cost module.

	$/W (Excluding Si Sheet)	
	Hermetic Module	**Low-Cost Module**
Baseline Low-Cost Cell Process	0.5442	0.4076
Alternate 1	0.6045	0.4685
Alternate 2	0.5627	0.4263

All cost assessments in this report exclude the cost of silicon sheet and are not dependent on the form of the silicon sheet. All costs do assume a minimum cell efficiency of 13.5% at AM1. Silicon sheet costs would have to be yielded through the process.

L. SENSITIVITY ANALYSIS

1. Scope

a. OBJECTIVE

This section describes a study to assess the processes selected for fabrication of the 7.62 cm (3-inch) hexagonal cells in a product facility. The objective of the study is to determine sensitivity of cell performance to manufacturing variances in processing.

b. APPROACH

The approach is to relate variations in individual process steps to output of the cell, and to assess state-of-the-art level of control for the processes. Comparison of sensitivity versus control provides the basis for identifying critical process elements.

The scope of this study includes three separate activities:

1) Development of models relating physical device structure to cell performance.

2) Design of test patterns for measuring physical parameters of the cell.

3) Experimental fabrication of cells with a range of process parameters to evaluate the variances expected in processing.

The hexagonal cell used for this experiment was designed for application with the array assembly technique described elsewhere in this report. The metallization pattern is shown in Figure 42. A triangular shaped bar, 0.3 cm on a side, connects cell rows in the module across a minor diagonal of the 7.6-cm hexagon. A center trunk line is provided for connection of the cell to the bus bar and a fishbone array of fingers, 127-μm wide, feeds into this trunk line. Spacing between fingers varies slightly with distance from the center as required to minimize the sum of resistance and shadowing losses. Test patterns fabricated on the cell allow measurement of physical parameters for each unit.

2. Models

a. APPROACH

This study involves development of analytical and empirical models for solar cells and their fabrication. In order to utilize available modeling techniques, it is useful to visualize the study in terms of the sequence of models shown in Figure 43.

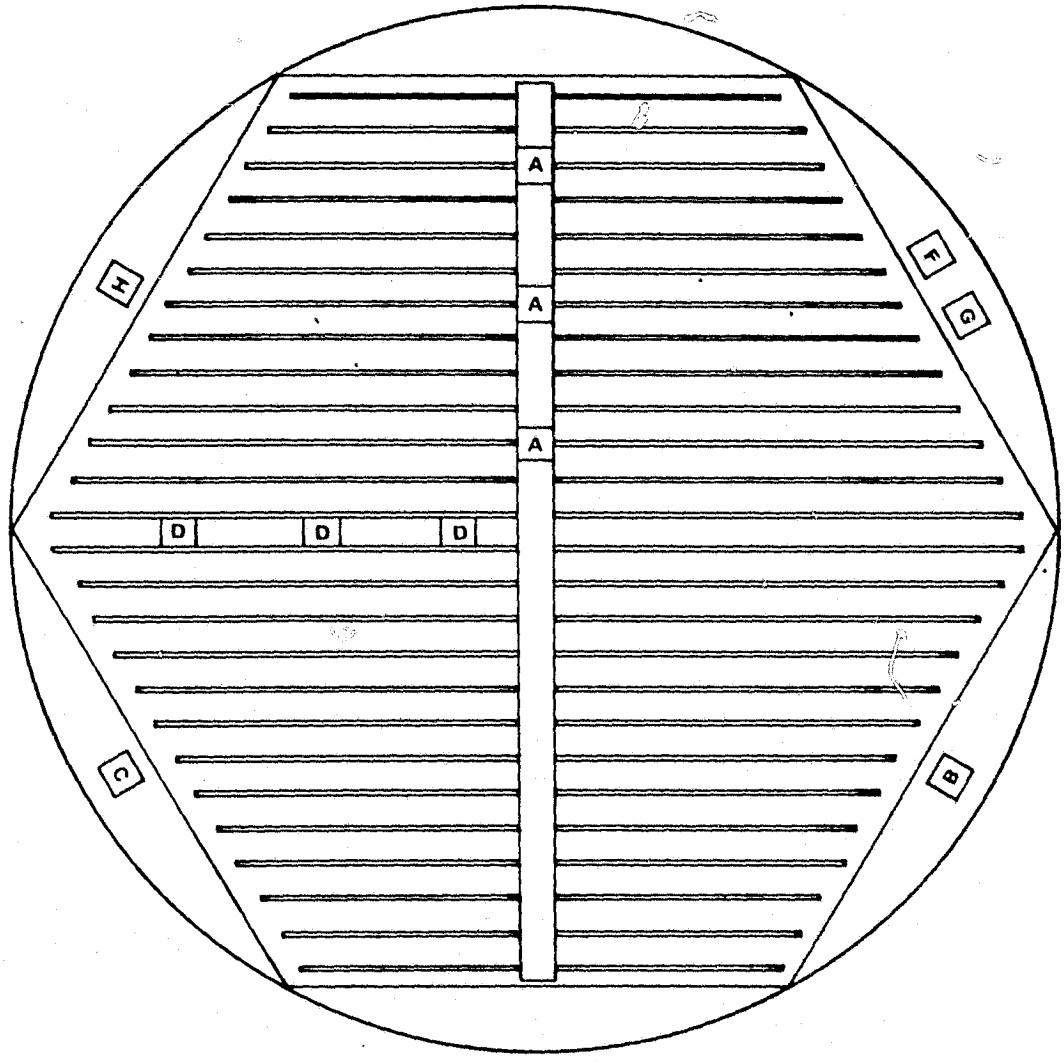


Figure 42. Layout of Cell and Test Devices

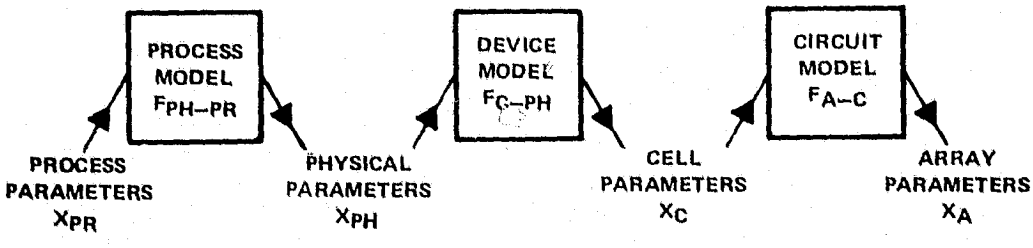


Figure 43. System of Models

In context of this diagram (Figure 43), control of physical parameters in fabrication is a process model. Experimental process models to evaluate control are discussed in a later section.

Sensitivity, defined in this study as the change in power output for a cell resulting from a change in some physical parameter of the cell, involves device models and circuit models. Let

$$F_{C-PH} = \frac{X_{C(i)}}{X_{PH(j)}}$$

be the transfer function (model) relating to cell parameter, $X_{C(i)}$, to a physical parameter, $X_{PH(j)}$, and let

$$F_{A-C} = \frac{X_{A(K)}}{X_{C(i)}}$$

be the transfer function relating the array parameter, $X_{A(K)}$, to the cell parameter, $X_{C(i)}$. (For this study, the array parameter is power output.) Sensitivity can be calculated from these models as the change in $X_{A(K)}$, corresponding to a change in $X_{PH(j)}$. For small changes in $X_{PH(j)}$, sensitivity can be approximated as

$$S_{(K)(i)} = \frac{\Delta X_{A(K)}}{\Delta X_{PH(j)}} = (F'_{C-PH})(F'_{A-C})$$

For this study, we assume that the cell can be represented by the basic equivalent circuit of Figure 44 so that cell parameters are series resistance, R_S, light-generated current, I_L, and junction

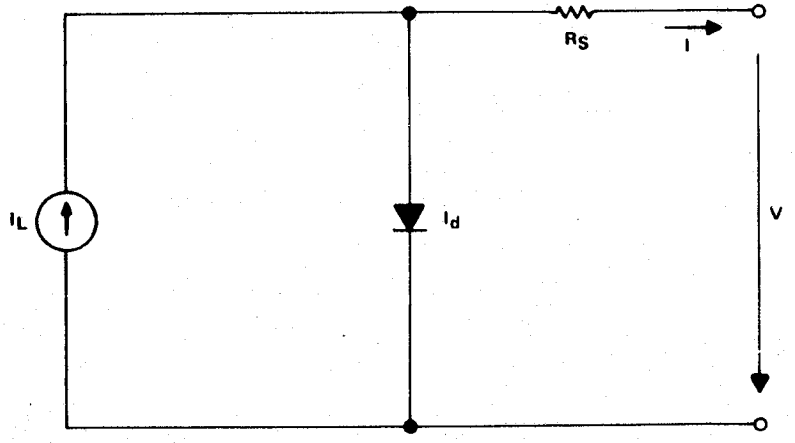


Figure 44. Basic Equivalent Circuit for Solar Cell

saturation current, I_S. The physical parameters upon which each of these cell parameters depend are indicated in the matrix of Figure 45.

The light-generated current is commonly calculated in terms of efficiency components, i.e.,

$$I_L = J_P \cdot A \cdot \eta_{TRAN} \cdot \eta_{MET} \cdot \eta_{COLL}$$

where

J_p = maximum light-generated current density corresponding to a given spectrum and bandgap.

A = active area

η_{TRAN} = efficiency of transmission through the AR coating

η_{MET} = efficiency corresponding to metal coverage

η_{COLL} = collection efficiency

	CELL PARAMETER				
	I_L			I_S	R_S
	η_{TRAN}	η_{MET}	η_{COLL}		
AR COATING THICKNESS	A				
REFRACTIVE INDEX	A				
FINGER WIDTH		A			A
METAL SHEET RESISTANCE					A
METAL CONTACT RESISTANCE					A
DIFFUSED REGION SHEET RESISTANCE					A
JUNCTION DEPTH			X		
BASE RESISTIVITY				X	
BASE LIFETIME			X		

Figure 45. Dependence of Cell Parameters on Physical Parameters

In Figure 45, the dependence of I_L on physical parameters is indicated according to efficiency components.

For the dependences indicated by A's in Figure 45, analytical dependences are developed in this section. Experimental models are developed in a later section for the dependences indicated by X's.

Circuit models for calculating power output due to changes in cell parameters are described in this section.

b. METALLIZATION AND SHEET RESISTANCE LOSSES

Earlier in this report, a computer program was developed to optimize the spacing between metal fingers and calculate the losses due to the metallization pattern. A similar analysis will be used here to calculate variation of shadowing and series resistance loss components with changes in processing parameters.

The metallization fingers are in a "fishbone" pattern as shown in Figure 42. Dimensions for a representative segment of the cell are shown in Figure 46. The width, T, of the fingers is constant; finger length, L, varies with distance of the finger from the center axis of the cell. The spacing, S, is optimized for each finger length to minimize the sum of resistive and shadowing losses.

For this analysis, it is assumed that the cell can be represented by a simple lumped model like that of Figure 44. In terms of this model, the power loss due to shadowing results from an increment, I_Δ, in the light-generated current, I_L. Resistive loss is represented by an effective series resistance, R_S, defined by the relationship

$$R_S = \frac{P_R}{I^2} \tag{62}$$

where P_R is the resistive power loss and I is the output current.

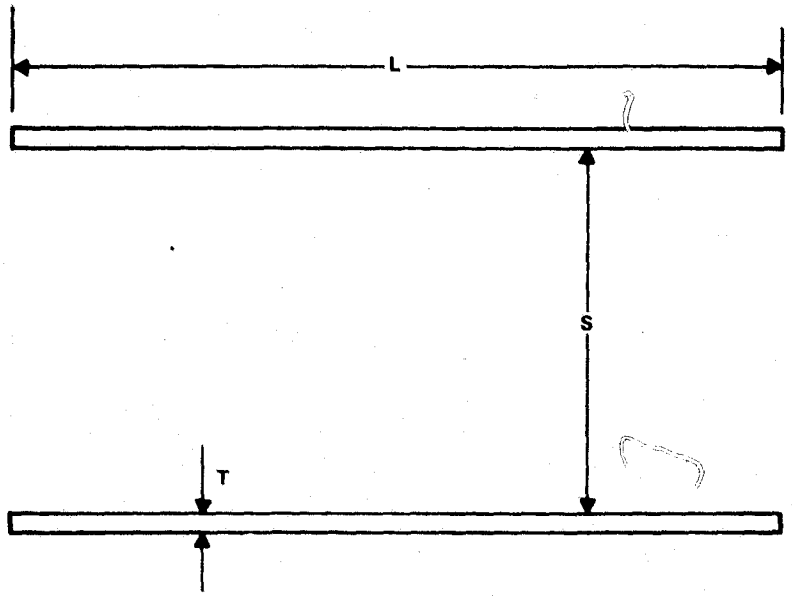


Figure 46. Representative Segment of Solar Cell

For a single segment (Figure 46), the resistive losses in the diffused layer, P_D, and in the fingers, P_F, are

$$P_D = \frac{1}{12} J^2 r\, LS^3 \tag{63}$$

$$P_F = \frac{1}{3} J^2 \frac{M}{T} L^3 S^2 \tag{64}$$

where r is the sheet resistance of the diffused layer, and M is the metal sheet resistance. The output current per unit area is

$$J = \frac{I}{A_T} \tag{65}$$

Where A_T, the total cell area is

$$A_T = \sum_{j=1}^{n} Lj\,(T + Sj) \tag{66}$$

The total series resistance loss is calculated by summing loss components for all segments, i.e.,

$$P_R = S_D + S_F \tag{67}$$

where

$$S_D = \sum P_D \tag{68}$$

and

$$S_F = \sum P_F \tag{69}$$

From equations (62) through (69) the series resistance is

$$R_S = K_D\, r + K_F \frac{M}{T}$$

where

$$K_D = \frac{\left(\sum_{j=1}^{n} \frac{1}{12} Lj\, Sj^3 \right)}{\left(\sum_{j=1}^{n} Lj\, [Sj + T] \right)^2}$$

and

$$K_F = \frac{\left(\sum_{j=1}^{n} \frac{1}{3} Lj^3\, Sj^2 \right)}{\left(\sum_{j=1}^{n} Lj\, [Sj + T] \right)^2}$$

From a similar analysis, the increment, I_Δ, in light-generated current, I_L, due to coverage by the metal fingers is

$$I_\Delta = I_L \cdot T \cdot K_C$$

where

$$K_C = \frac{\sum_{j=1}^{n} Lj}{\sum_{j=1}^{n} (Lj)\,(Sj + T)}$$

The constants, K_D, K_F, and K_C, determined from geometrical calculations for the pattern of Figure 42 are

$$K_D = 0.0001017$$

$$K_F = 0.0185 \text{ cm}$$

$$K_C = 4.23 \text{ cm}^{-1}$$

In Figures 47, 48, and 49, variations of series resistance and I_Δ, an increment of the light-generated current lost due to shadowing, are plotted as a function of process variables. I_Δ is used since this is a more sensitive measure of loss in the light-generated current. The process variables in Figures 47, 48, and 49 are diffused sheet resistance, metal sheet resistance, and finger width, respectively. Only one parameter is varied in each case. Variations of series resistance and light-generated current are normalized with respect to their values for the design value of the process parameters, i.e.,

$$r = 80 \text{ ohms/square}$$

$$M = 0.0033 \text{ ohms/square}$$

$$T = 0.0127 \text{ cm}$$

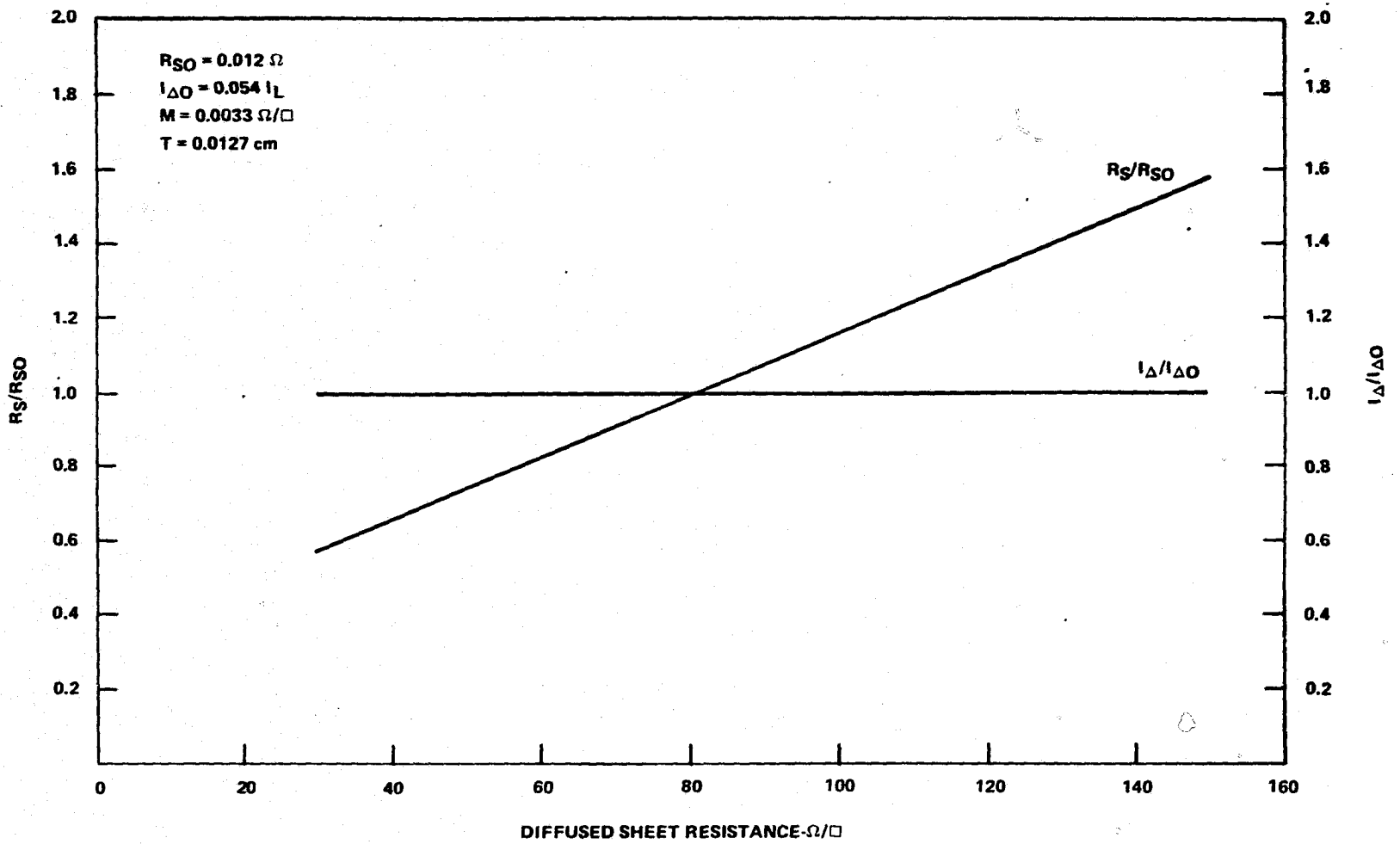


Figure 47. Variation of Series Resistance and Light-Generated Current with Diffused Sheet Resistance for Constant Metal Sheet Resistance and Finger Width

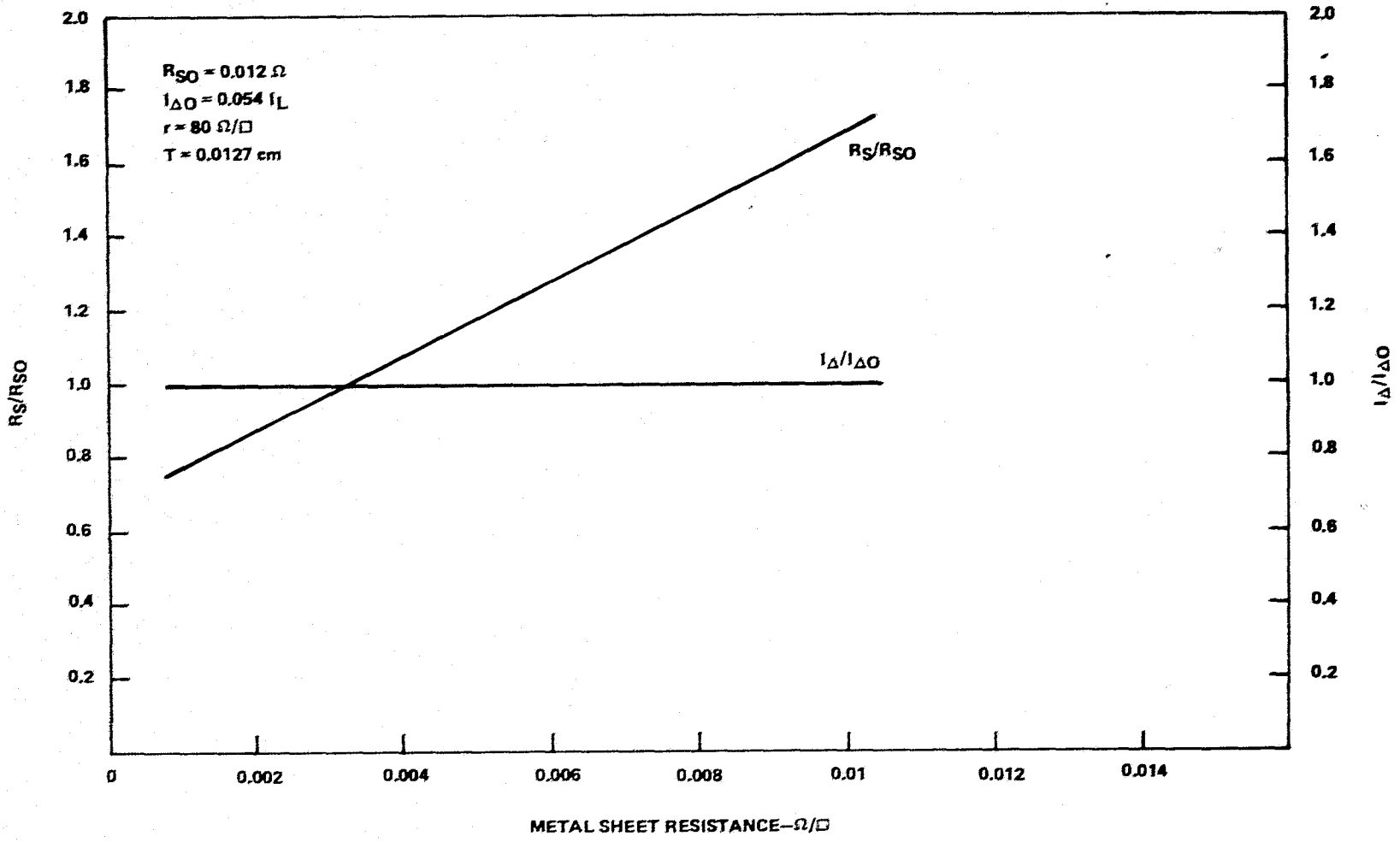


Figure 48. Variation of Series Resistance and Light-Generated Current with Metal Sheet Resistance for Constant Diffused Sheet Resistance and Finger Width

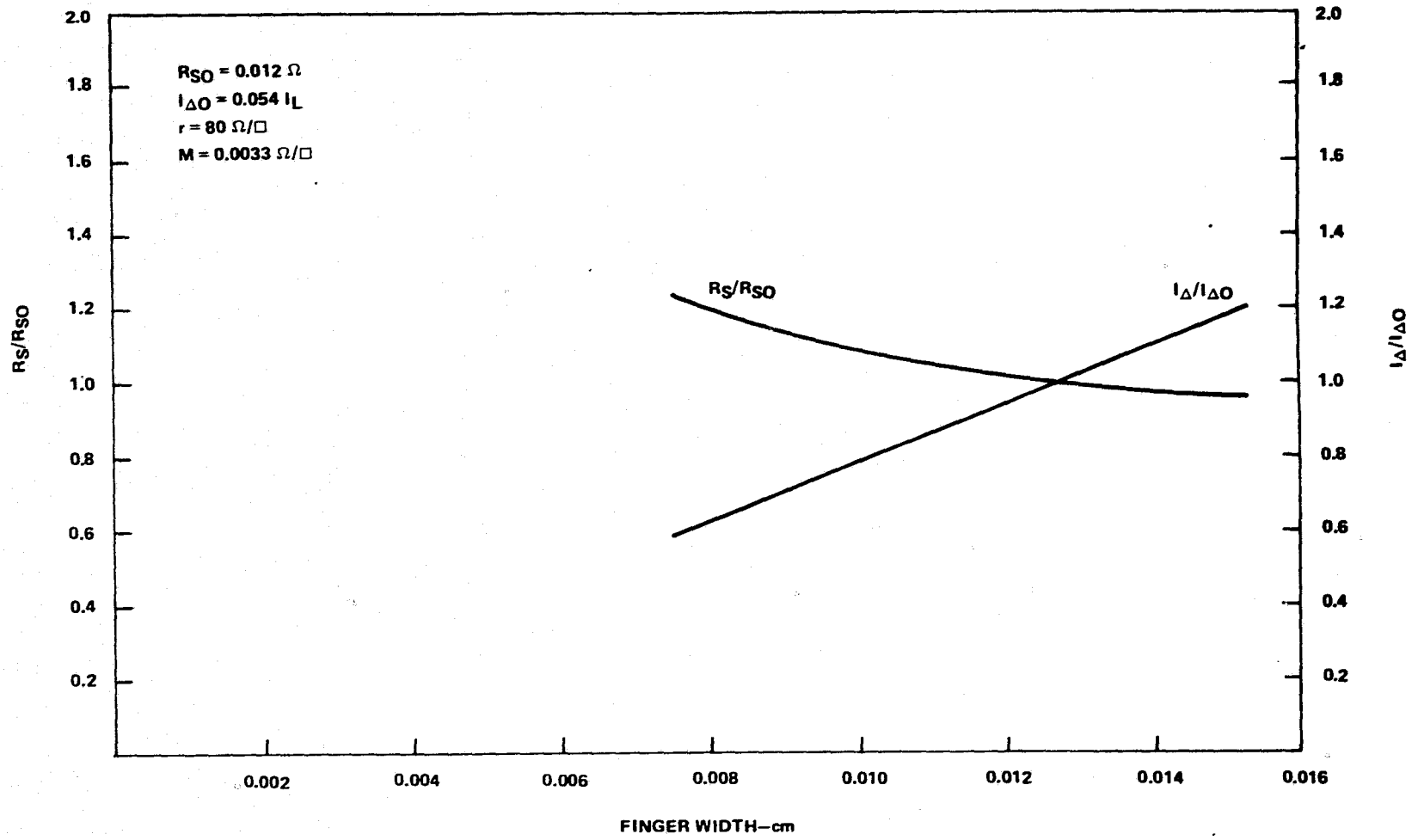


Figure 49. Variation of Series Resistance and Light-Generated Current with Finger Width for Constant Diffused Sheet Resistance and Metal Sheet Resistance

From inspection of Figure 47, it is evident that diffused sheet resistance has no effect on light-generated current, ignoring effects of lower lifetime in the diffused region, and exerts a direct linear impact on series resistance. A change of 20%, 16 ohms/square, in the diffused sheet resistance causes a change of 12%, 1.4×10^{-3} ohms, in the series resistance. This magnitude change in the series resistance, R_S, causes a negligible change in cell performance. Therefore, control of diffused sheet resistance within ±20% of the nominal value is more than adequate for solar cell process control.

From inspection of Figure 48, it is evident that metal sheet resistance has no effect on light-generated current as expected. Series resistance is directly related to metal sheet resistance. An increase of 50% in metal sheet resistance causes an increase of 17%, 2×10^{-3} ohms, in series resistance. This would cause a negligible change in cell performance. Therefore, control of metal sheet resistance within ±25% to 50% of the nominal value is more than adequate for solar cell process control.

From inspection of Figure 49, it is evident that both I_Δ and R_S/R_{SO} change with changes in metal finger width. The changes in I_Δ and R_S/R_{SO} are of opposite sign and tend to compensate one another. For a decrease of 25 μm in finger width, I_Δ decreases 20% ($I_{SC} = I_L - I_\Delta$, I_{SC} increases ≈1%) and R_S/R_{SO} increases ≈8%, 1×10^{-3} ohms. These compensating changes result in negligible change in cell performance. Therefore, control of metal finger width within ±25 μm at a nominal width of 127 μm is more than adequate for solar cell process control.

In summary, diffused sheet resistance, metal finger resistance, and metal finger width are not sensitive variables in the control of a silicon solar cell process. The control evaluation should demonstrate whether specific process controls are required.

c. CARRIER GENERATION

Much previous work has been done on the use of antireflective coatings, but they have been optimized for a single wavelength chosen to be "representative."[4,5] To achieve optimization of such a coating under actual air mass zero or air mass one conditions, the calculations must take into account carrier generation due to all wavelengths of use to the solar cell, the reflectivity of a coated cell to all wavelengths of insulation, and the change of index of refraction of both the antireflection coating and the silicon with wavelength.

In order to examine the sensitivity of photogenerated carrier generation to processing variables in a solar cell process, a computer program has been written to determine generation rate and number of carriers at a given depth within a silicon solar cell when the characteristics of the silicon

and the antireflection (AR) coating are changed. From Lambert's Law, the number of absorbed photons with wavelength between λ and $\lambda + d\lambda$ in a layer of thickness dx is

$$U(\lambda) = \alpha(\lambda)\, N(\lambda) \exp[-\alpha(\lambda)\, x]\, dx,$$

where

$\alpha(\lambda)$ = absorption coefficient

$N(\lambda)$ = number of incident photons at wavelength λ

The total number of carriers generated as a function of depth is given by

$$N(d) = \int_0^d \int_{\lambda_1}^{\lambda_2} \alpha(\lambda)\, N(\lambda) \exp[-\alpha(\lambda)\, x]\, d\lambda dx$$

where

d = depth into the silicon

The number of incident photons on the surface of the silicon is modified by the presence of an AR coating. Fossum[6] has calculated the number of carriers generated under AM0 illumination with no reflection losses. The computational method used here is similar and consistent.

Since the coating is $\approx 0.1\ \mu$m, absorption of the film is negligible. The transmissivity, T, of the AR coating is given by

$$T = 1 - \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos 2\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos 2\theta}$$

where

$r_1 = 1 - n_1/1 + n_1$

$r_2 = n_1 - n_2/n_1 + n_2$

$\theta = 2 \pi t n_2/\lambda$

n_1 = refractive index of the AR coating

n_2 = refractive index of silicon

θ = phase thickness of coating

t = thickness of coating

λ = wavelength of incident radiation

In order to consider the effects of antireflection coatings on cell performance, the refractive index of silicon[7] and silicon monoxide[8] were entered as a series of least squares polynomial regressions so that values were easily retrievable. The refractive index of silicon dioxide was entered as a Sellmeier oscillator expression

$$n^2 - 1 = \frac{E_d E_o}{(E_o^2 - E)}$$

where

E_d = dispersion energy

E_o = effective oscillator energy

E = photon energy

n = refractive index [9,10]

The calculated J_G values in Table 16 assume ideal conditions in which all generated carriers can be collected. In practice, carriers generated in the diffusion layer have a lower probability of being collected than carriers generated in the base layer due to trapping, surface recombination and other loss mechanisms. Therefore it is useful to know how much of the generated current is in the diffused layer and how much is in the base region.

Table 16. Current Density Generation as a Function of Depth with SiO Optical Coating Thickness as a Parameter at AM0

d (μm)	100% Abs.	Optical Coating Thickness (μm)														
		0	0.020	0.030	0.040	0.050	0.060	0.070	0.075	0.080	0.090	0.10	0.11	0.12	0.14	0.15
0.001	0.145	0.063	0.100	0.119	0.124	0.111	0.082	0.090	0.091	0.093	0.099	0.106	0.109	0.091	0.098	0.098
0.002	0.278	0.129	0.194	0.230	0.242	0.217	0.168	0.175	0.177	0.180	0.191	0.206	0.212	0.183	0.190	0.189
0.005	0.629	0.321	0.444	0.529	0.560	0.507	0.414	0.408	0.408	0.412	0.436	0.472	0.491	0.448	0.437	0.434
0.010	1.11	0.593	0.787	0.944	1.01	0.920	0.774	0.735	0.728	0.731	0.770	0.838	0.880	0.827	0.779	0.772
0.020	1.88	1.02	1.32	1.59	1.72	1.58	1.36	1.26	1.23	1.23	1.28	1.40	1.48	1.43	1.32	1.31
0.050	3.47	1.88	2.38	2.88	3.18	3.01	2.63	2.39	2.32	2.28	2.32	2.50	2.67	2.65	2.48	2.44
0.10	5.23	2.85	3.53	4.25	4.75	4.63	4.15	3.76	3.62	3.52	3.50	3.67	3.91	3.94	3.80	3.76
0.20	7.62	4.22	5.08	6.05	6.83	6.85	6.33	5.78	5.55	5.36	5.19	5.29	5.52	5.61	5.62	5.61
0.50	12.01	6.83	7.97	9.30	10.51	10.88	10.46	9.77	9.40	9.07	8.61	8.47	8.56	8.62	8.82	8.97
1.0	16.35	9.52	10.88	12.47	14.04	14.77	14.56	13.88	13.45	13.02	12.32	11.93	11.81	11.73	11.89	12.13
2.0	21.85	13.00	14.59	16.47	18.42	19.55	19.66	19.11	18.66	18.18	17.26	16.61	16.21	15.89	15.82	16.06
5.0	29.81	18.27	20.11	22.30	24.67	26.29	26.88	26.66	26.32	25.87	24.88	23.99	23.26	22.58	21.90	21.95
10.0	35.79	22.31	24.30	26.67	29.89	31.22	32.12	32.19	31.96	31.60	30.69	29.76	28.89	28.01	26.84	26.67
20.0	40.80	25.75	27.84	30.34	33.13	35.26	36.39	36.70	36.57	36.31	35.54	34.66	33.77	32.79	31.28	30.92
50.0	45.34	28.87	31.03	33.62	36.54	38.83	40.14	40.63	40.60	40.43	39.83	39.07	38.24	37.26	35.56	35.05
100.	47.61	30.43	32.62	35.24	38.22	40.57	41.96	42.54	42.55	42.43	41.91	41.24	40.46	39.51	37.78	37.22
200.	49.26	31.56	33.77	36.42	39.43	41.83	43.27	43.91	43.96	43.86	43.41	42.79	42.07	41.14	39.42	38.83
250.	49.69	31.85	34.07	36.73	39.74	42.15	43.61	44.27	44.32	44.24	43.80	43.20	42.48	41.57	39.85	39.25
J_G/J_{G0}	1.000	0.641	0.686	0.739	0.800	0.848	0.878	0.891	0.892	0.890	0.881	0.869	0.855	0.837	0.802	0.790
$J_G/J_{G\ OPT}$		0.719	0.769	0.829	0.897	0.951	0.984	0.999	1.000	0.998	0.988	0.975	0.958	0.938	0.899	0.886
0.28	9.06	5.06	6.02	7.12	8.05	8.18	7.67	7.06	6.77	6.53	6.27	6.30	6.49	6.59	6.69	6.73
0.30	9.38	5.25	6.23	7.36	8.32	8.47	7.97	7.34	7.05	6.80	6.51	6.52	6.71	6.81	6.92	6.97
0.32	9.68	5.43	6.44	7.58	8.58	8.76	8.26	7.62	7.32	7.06	6.75	6.74	6.92	7.02	7.15	7.21

Calculations have been made with SiO and SiO_2 as the AR coating at air masses zero[11] and one with incident flux density of 135.3 and 88.9 mW/cm^2, respectively. Optimized coating thicknesses were obtained for each set of conditions. This data is given in Tables 16, 17, 18, and 19 as generated current density, J_G, versus AR coating thickness as a function of depth into the silicon for planar solar cell surfaces. The textured surface case would be expected to be even less sensitive to AR coating thickness.

d. REFRACTIVE INDEX AND OPTICAL THICKNESS

The sensitivity of generated current density, J_G as a function of optical coating thickness for 250-μm cells is plotted at AM0 and AM1 for SiO and SiO_2 coatings in Figures 50 and 51, respectively. Optimum AR coating thicknesses are given in Table 20.

From inspection of Figures 50 and 51, it is obvious that J_G is not highly sensitive to AR coating thickness near the optimum thickness values. Thickness control in the range ± 0.01 μm around the optimum appears to be acceptable.

Refractive index plays a somewhat more significant role. Comparison of Figures 50 and 51 shows an $\approx 5\%$ difference in J_G for SiO and SiO_2 at AM1. This difference is due to the improved refractive index match between silicon and air. This parameter should be easily controlled, however, since different AR coatings are deposited by techniques that give reproducible films. Other high index, ≈ 2, materials such as silicon nitride, tantalum oxide, or mixed oxides should give results similar to SiO. The choice of an AR coating for an LSSA module should be determined by process compatibility and economics within the range of acceptable high index materials.

e. CIRCUIT MODELS

Circuit models used for the sensitivity analysis are relationships for power output in terms of cell parameters. Power output for an array of cells can be calculated using the cell equivalent circuit in circuit analysis codes such as SPICE. SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose circuit simulation program, developed by the Electronics Research Laboratory, College of Engineering, University of California, Berkeley.

Computations were presented earlier in this report for power output of an array as a function of cell parameters; parameters of one cell were varied individually with parameters of other cells and load resistance unchanged. Such results have limited value for a sensitivity analysis since they are highly dependent upon the array configurations.

Table 17. Current Density Generation as a Function of Depth With SiO2 Optical Coating Thickness as a Parameter at AM0

	100%	Optical Coating Thickness (μm)											
d (μm)	Abs.	0	0.020	0.040	0.060	0.080	0.100	0.105	0.110	0.120	0.125	0.085	0.093
0.001	0.145	0.063	0.088	0.109	0.109	0.092	0.089	0.083	0.088	0.090	0.091	0.093	0.091
0.002	0.278	0.129	0.171	0.211	0.214	0.183	0.173	0.171	0.171	0.175	0.177	0.182	0.176
0.005	0.629	0.321	0.392	0.482	0.502	0.433	0.396	0.392	0.392	0.400	0.407	0.424	0.407
0.010	1.11	0.593	0.693	0.855	0.905	0.789	0.707	0.697	0.694	0.706	0.719	0.766	0.729
0.020	1.88	1.02	1.16	1.43	1.54	1.36	1.20	1.18	1.17	1.18	1.20	1.31	1.24
0.050	3.47	1.88	2.01	2.58	2.85	2.58	2.25	2.20	2.17	2.15	2.16	2.49	2.35
0.100	5.23	2.85	3.14	3.83	4.29	4.00	3.51	3.41	3.34	3.26	3.26	3.87	3.67
0.20	7.62	4.22	4.59	5.52	6.26	6.01	5.33	5.18	5.05	4.88	4.84	5.85	5.57
0.50	12.01	6.83	7.33	8.63	9.86	9.82	8.93	8.70	8.48	8.13	8.00	9.64	9.28
1.0	16.35	9.52	10.13	11.74	13.40	13.65	12.71	12.42	12.13	11.62	11.42	13.49	13.11
2.0	21.85	13.00	13.73	15.68	17.83	18.49	17.62	17.28	16.94	16.28	15.98	18.38	18.04
5.0	29.81	18.27	19.13	21.48	24.23	25.49	24.94	24.62	24.26	23.50	23.13	25.50	25.29
10.0	35.79	22.31	23.26	25.85	28.97	30.65	30.42	30.15	29.83	29.08	28.70	30.76	30.69
20.0	40.80	25.75	26.75	29.51	32.90	34.90	34.96	34.75	34.47	33.80	33.42	35.09	35.13
50.0	45.34	28.87	29.91	32.80	36.38	38.64	38.97	38.81	38.59	38.01	37.68	38.89	39.05
100.0	47.61	30.43	31.48	34.42	38.09	40.46	40.92	40.79	40.60	40.07	39.76	40.75	40.95
200.0	49.26	31.56	32.63	35.60	39.33	41.77	42.32	42.21	42.05	41.56	41.27	42.08	42.32
250.0	49.69	31.85	32.93	35.91	39.65	42.12	42.68	42.58	42.42	41.95	41.66	42.43	42.68
J_G/J_{G0}	1.00	0.641	0.663	0.723	0.798	0.848	0.859	0.857	0.854	0.844	0.838	0.854	0.859
$J_G/J_{G\ OPT}$		0.746	0.772	0.841	0.929	0.987	1.00	0.998	0.994	0.983	0.976	0.994	1.00
0.28	9.06	5.06	5.48	6.53	7.44	7.24	6.48	6.30	6.14	5.91	5.84	7.07	6.76
0.30	9.38	5.25	5.68	6.76	7.70	7.52	6.74	6.55	6.38	6.14	6.07	7.35	7.02
0.32	9.68	5.43	5.17	6.98	7.95	7.78	6.99	6.79	6.62	6.37	6.29	7.61	7.28

Table 18. Current Density Generation as a Function of Depth with SiO Optical Coating Thickness as a Parameter at AM1

	Optical Coating thickness (μm)										
d (μm)	0.	0.020	0.030	0.050	0.060	0.075	0.080	0.090	0.100	0.110	0.130
0.001	0.023	0.028	0.034	0.037	0.033	0.028	0.027	0.027	0.029	0.032	0.031
0.002	0.045	0.055	0.067	0.074	0.066	0.056	0.054	0.053	0.057	0.063	0.062
0.005	0.110	0.134	0.164	0.146	0.137	0.138	0.133	0.131	0.140	0.153	0.153
0.010	0.213	0.260	0.318	0.353	0.317	0.268	0.259	0.254	0.270	0.296	0.296
0.020	0.403	0.491	0.597	0.670	0.605	0.513	0.494	0.482	0.508	0.553	0.560
0.050	0.883	1.06	1.28	1.47	1.35	1.15	1.10	1.06	1.09	1.17	1.22
0.10	1.51	1.79	2.13	2.50	2.33	2.01	1.92	1.83	1.84	1.94	2.04
0.20	2.46	2.86	3.36	4.02	3.85	3.37	3.22	3.02	2.97	3.05	3.22
0.50	4.37	4.97	5.72	6.95	6.87	6.22	5.97	5.56	5.33	5.30	5.46
1.0	6.43	7.18	8.14	9.90	9.98	9.31	9.00	8.41	7.99	7.79	7.77
2.0	9.13	10.06	11.23	13.60	13.93	13.36	13.01	12.26	11.63	11.21	10.86
5.0	13.23	14.36	15.78	18.87	19.58	19.35	19.02	18.21	17.38	16.69	15.79
10.	16.29	17.54	19.10	22.62	23.57	23.65	23.39	22.64	21.76	20.95	19.67
20.	18.71	20.03	21.68	25.48	26.60	26.92	26.73	26.06	25.22	24.37	22.88
50.	20.63	22.00	23.71	27.68	28.92	29.41	29.28	28.71	27.93	27.11	25.57
100.	21.58	22.97	24.70	28.74	30.03	30.60	30.49	29.98	29.25	28.46	26.94
200.	22.39	23.79	25.54	29.64	30.96	31.60	31.51	31.04	30.36	29.61	28.12
250.	22.63	24.03	25.78	29.90	31.23	31.89	31.81	31.35	30.67	29.94	28.46
$J_G/J_{G\ OPT}$	0.710	0.753	0.808	0.938	0.979	1.00	0.997	0.983	0.962	0.939	0.892
0.28	3.06	3.53	4.12	4.97	4.81	4.26	4.08	3.81	3.70	3.76	3.95
0.30	3.20	3.69	4.29	5.18	5.03	4.46	4.28	3.99	3.87	3.92	4.11
0.32	3.33	3.83	4.46	5.38	5.24	4.66	4.47	4.17	4.04	4.07	4.26

Table 19. Current Density Generation As A Function Of Depth With SiO2 Optical Coating Thickness As A Parameter At AM1

	Optical Coating Thickness (μm)								
d (μm)	0	0.020	0.040	0.060	0.080	0.090	0.100	0.110	0.130
0.001	0.023	0.024	0.030	0.034	0.032	0.030	0.027	0.026	0.025
0.002	0.045	0.049	0.059	0.068	0.063	0.059	0.055	0.051	0.050
0.005	0.110	0.119	0.146	0.167	0.156	0.145	0.134	0.127	0.122
0.010	0.213	0.231	0.282	0.323	0.303	0.282	0.262	0.246	0.237
0.020	0.403	0.437	0.532	0.610	0.576	0.537	0.499	0.470	0.450
0.050	0.883	0.953	1.15	1.33	1.27	1.19	1.11	1.04	0.985
0.10	1.51	1.62	1.94	2.24	2.19	2.07	1.93	1.81	1.69
0.20	2.46	2.62	3.10	3.59	3.58	3.42	3.21	3.02	2.78
0.50	4.37	4.63	5.38	6.21	6.38	6.17	5.86	5.56	5.07
1.0	6.43	6.76	7.74	8.91	9.29	9.11	8.76	8.35	7.62
2.0	9.13	9.55	10.79	12.34	13.05	12.93	12.57	12.09	11.10
5.0	13.23	13.76	15.32	17.33	18.51	18.56	18.30	17.81	16.60
10.	16.29	16.89	18.63	20.94	22.45	22.64	22.47	22.05	20.79
20.	18.71	19.35	21.21	23.71	25.46	25.75	25.69	25.33	24.12
50.	20.63	21.30	23.24	25.86	27.76	28.15	28.16	27.87	26.75
100.	21.58	22.26	24.23	26.91	28.88	29.30	29.35	29.10	28.04
200.	22.39	23.08	25.08	27.79	29.81	30.26	30.35	30.13	29.13
250.	22.63	23.31	25.32	28.05	30.08	30.54	30.63	30.42	29.44
$J_G/J_{G\ OPT}$	0.739	0.761	0.827	0.916	0.982	0.997	1.00	0.993	0.961
0.28	3.06	3.26	3.83	4.43	4.47	4.29	4.05	3.81	3.49
0.30	3.20	3.41	3.99	4.62	4.67	4.48	4.24	3.99	3.65
0.32	3.33	3.55	4.15	4.81	4.87	4.68	4.42	4.17	3.81

Table 20. Optimum AR Coating Thickness

Material	Illumination	Optimum Thickness (μm)
SiO	AM0	0.075
	AM1	0.075
SiO_2	AM0	0.10
	AM1	0.10

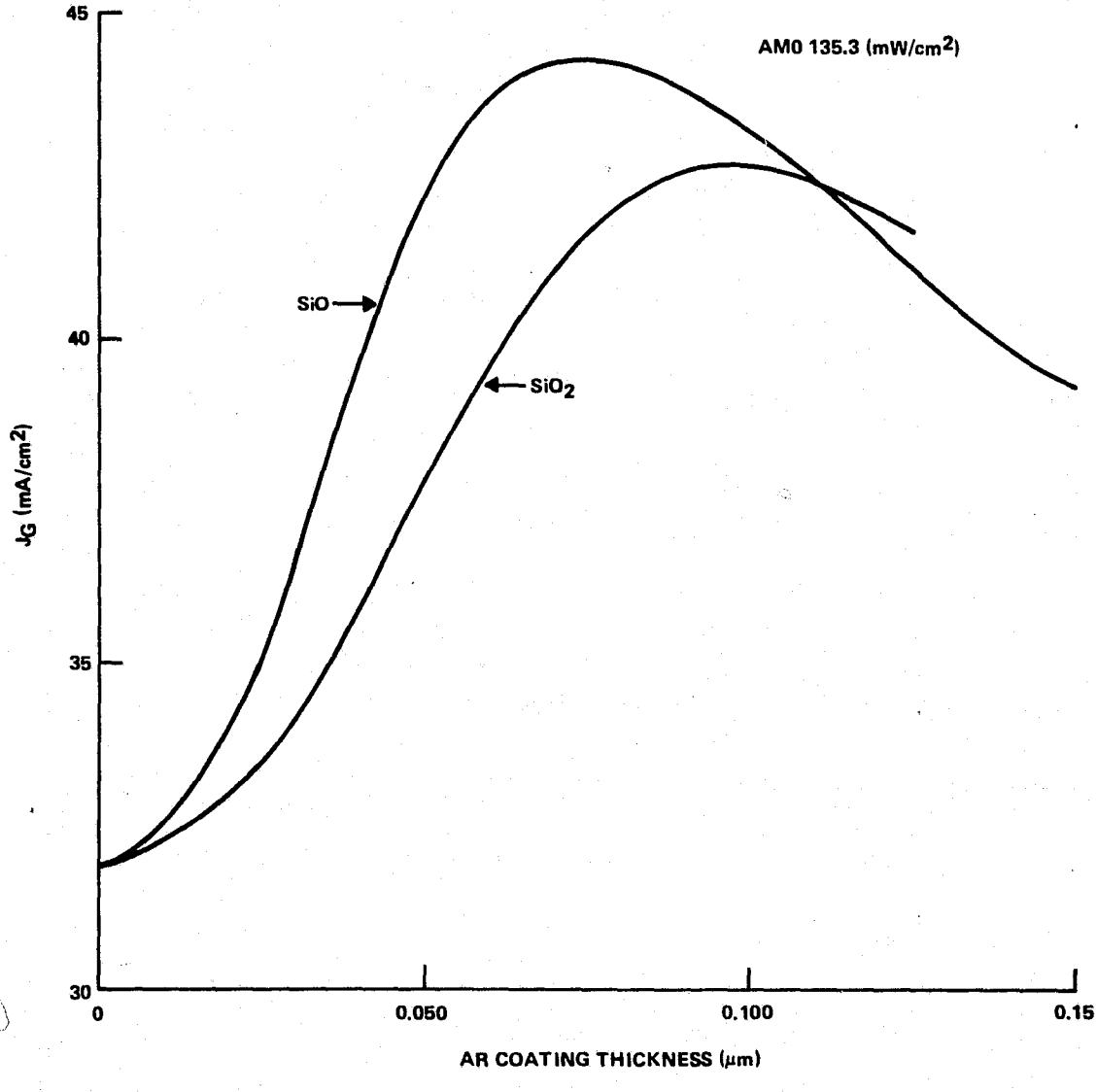


Figure 50. Sensitivity of Generated Current Density as a Function of AR Coating Thickness at AM0

For our study, power output is calculated for a single cell in a circuit like that of Figure 52. The load resistance has the value which gives maximum power output for nominal parameters of the cell. Change in power output is calculated for a range of cell parameters. Changes for a single cell in an array will be substantially less; however, the circuit of Figure 52 provides a basis for uniform comparison.

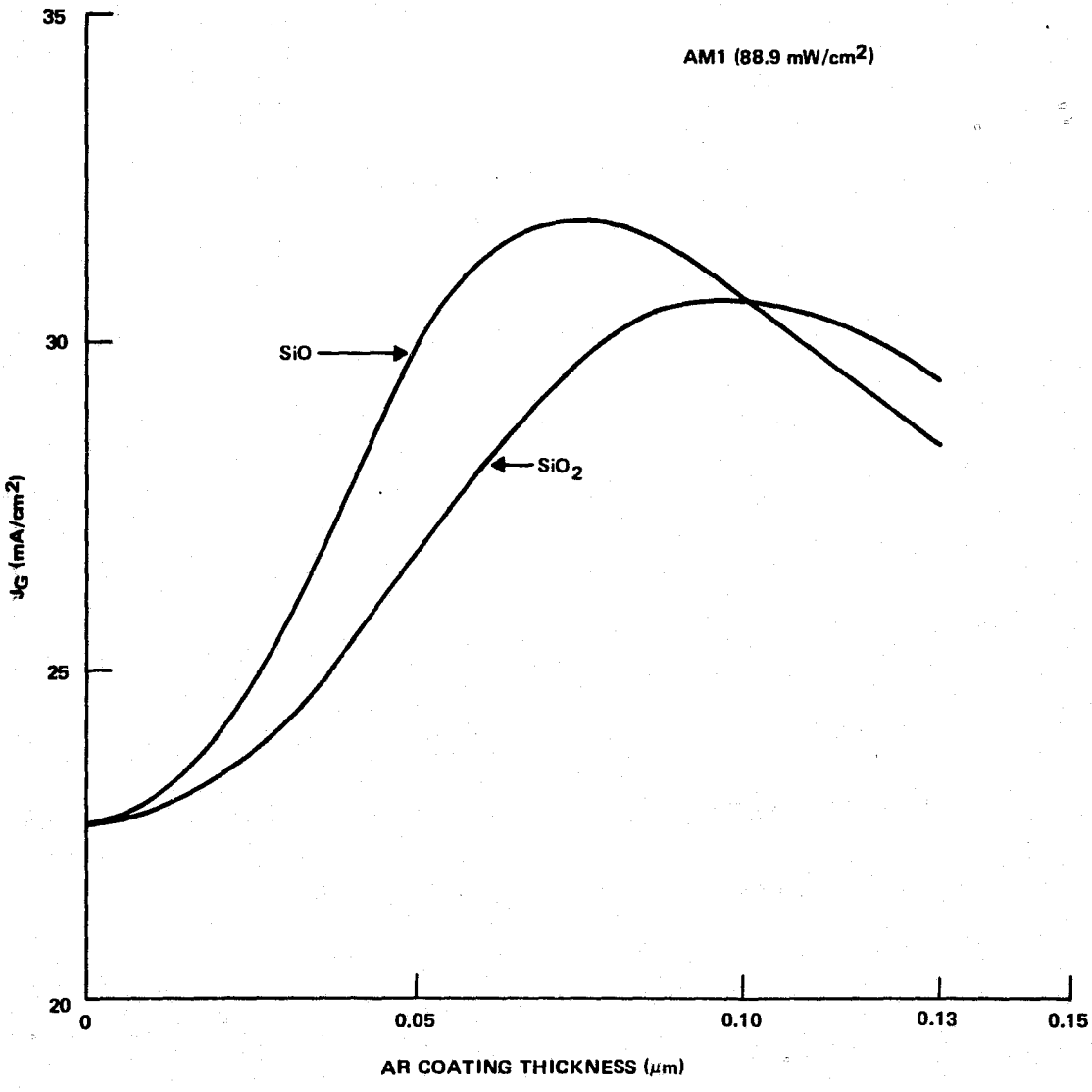


Figure 51. Sensitivity of Generated Current Density as a Function of AR Coating Thickness at AM1

Expected parameters for the cell of this report are:

$$R_S = 0.0123 \text{ ohm}$$

$$I_L = 1.3 \text{ amps}$$

$$I_S = 7.86 \times 10^{-11} \text{ amps}$$

Using these parameters and SPICE analysis, the load resistance for maximum power was determined to be

$$R_L = 0.4054 \text{ ohm}$$

Power output was calculated varying R_S and I_L individually using the SPICE program. These results are shown in Tables 21 and 22, respectively.

Table 21. Change of Power Output for Changes of Light-Generated Current

I_L (amps)	I (amps)	P_O (SPICE) (watts)	P_O (EQ 75) (watts)
1.23	1.207	0.59022	0.60006
1.25	1.222	0.60452	0.61047
1.27	1.235	0.61762	0.62089
1.29	1.247	0.62974	0.63131
1.31	1.258	0.64108	0.64172
1.33	1.269	0.65214	0.65214
1.35	1.279	0.66227	0.66256
1.37	1.287	0.67104	0.67297
1.39	1.296	0.68014	0.68339
1.41	1.303	0.68785	0.69381
1.43	1.310	0.69522	0.70422

Table 22. Change of Power Output for Changes of Series Resistance

R_S (ohms)	I (amps)	P_O (SPICE) (watts)	P_O (EQ 76) (watts)
0	1.286	0.66988	0.67129
0.00615	1.278	0.66137	0.66171
0.0123	1.269	0.65214	0.65214
0.01845	1.259	0.64209	0.64257
0.0246	1.249	0.63199	0.63299

Dependence of power output could also be estimated analytically. From the circuit of Figure 52, we have the relationships

$$I_L = I_S \exp (qV/kT) + I \tag{70}$$

$$V = I (R_L + R_S) \tag{71}$$

and

$$P_O = I^2 R_L \tag{72}$$

where I is the current in R_L, P_O is the power output and the cell parameters are those previously defined. For small changes in I_L, the incremental change in power output is

$$\Delta P_O = 2 IR_L \frac{\Delta I}{\Delta I_L} \Delta I_L \tag{73}$$

From equations (70) and (71),

$$\frac{dI}{dI_L} = \frac{r_d}{r_d + R_L + R_S} \tag{74}$$

where

$$r_d = \frac{kT}{qI_d}$$

and

$$I_d = I_S \exp (qV/kT)$$

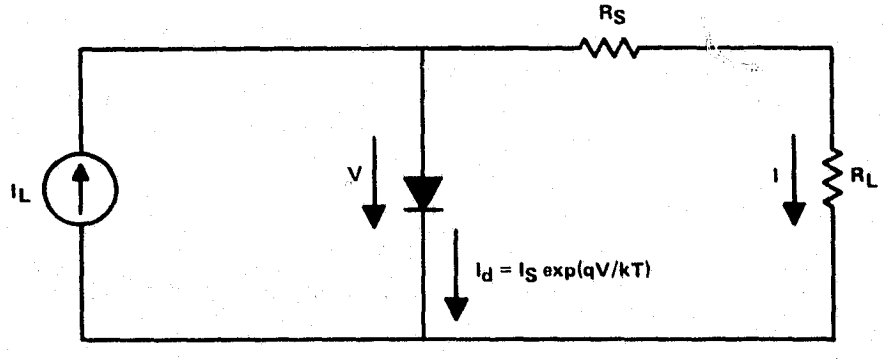


Figure 52. Equivalent Circuit for Calculating Power Output for Solar Cell

is the current through the P-N junction. Power output is approximated from equations (72), (73), and (74) as

$$P(I_L) = P_{OH}\,[1 + K_{PI}\,\Delta\, I_L] \tag{75}$$

where

$$K_{PI} = \frac{2r_d}{r_d + R_L + R_S}\,\frac{1}{I}$$

From a smiliar analysis, power output for small changes in series resistance may be approximated as

$$P(R_S) = P_O\,[1 + K_{PR}\,\Delta R_S] \tag{76}$$

where

$$K_{PR} = -\frac{2}{r_d + R_L + R_S} \tag{77}$$

Parameters for the circuit of Figure 52 are

I_L = 1.33 amps

I = 1.269 amps

I_d = 0.061 amp

r_d = 0.4246 ohm

R_L = 0.4050 ohm

R_S = 0.0123 ohm

P_O = 0.6522 watt

Using these values and equation (89)

$$K_{PI} = 0.79865$$

From equation (77)

$$K_{PR} = -2.387$$

values of power output approximated from equations (75) and (76) are compared in Tables 21 and 22, respectively to the precise values calculated with SPICE.

For practical cells in which R_S, $<<$ R_L, the approximation of equation (90) is good even for very large changes in R_S. The validity of equation (75) is limited to small changes in I_L, i.e.,

$$\frac{\Delta I_L}{I_L} \leqslant 0.05$$

3. Test Patterns

Test patterns are fabricated on the solar cells for measurement of physical parameters. For this study, the test structures are used to evaluate tolerances which can be maintained in the process steps. For production devices, it would be desirable to have in-line tests for continuous process control. Design of the test patterns was based on the following criteria:

1) Test patterns should be compatible with in-line probing on 100% of cells.

2) Test patterns should add no additional complexity to processing of cells.

3) Test patterns should not deteriorate cell performance or reduce useful area of cell.

4) Test patterns should be compatible with various process options; e.g., screen printing versus photolithographic metallization; etched versus planar junctions; N on P versus P on N cells.

The test patterns selected and the parameters which they measure are listed in Table 23. Drawings of the test patterns are shown in Figure 53. Location of these test devices on the cell is indicated in the cell drawing of Figure 42. Letters in this drawing correspond to those of Figure 53.

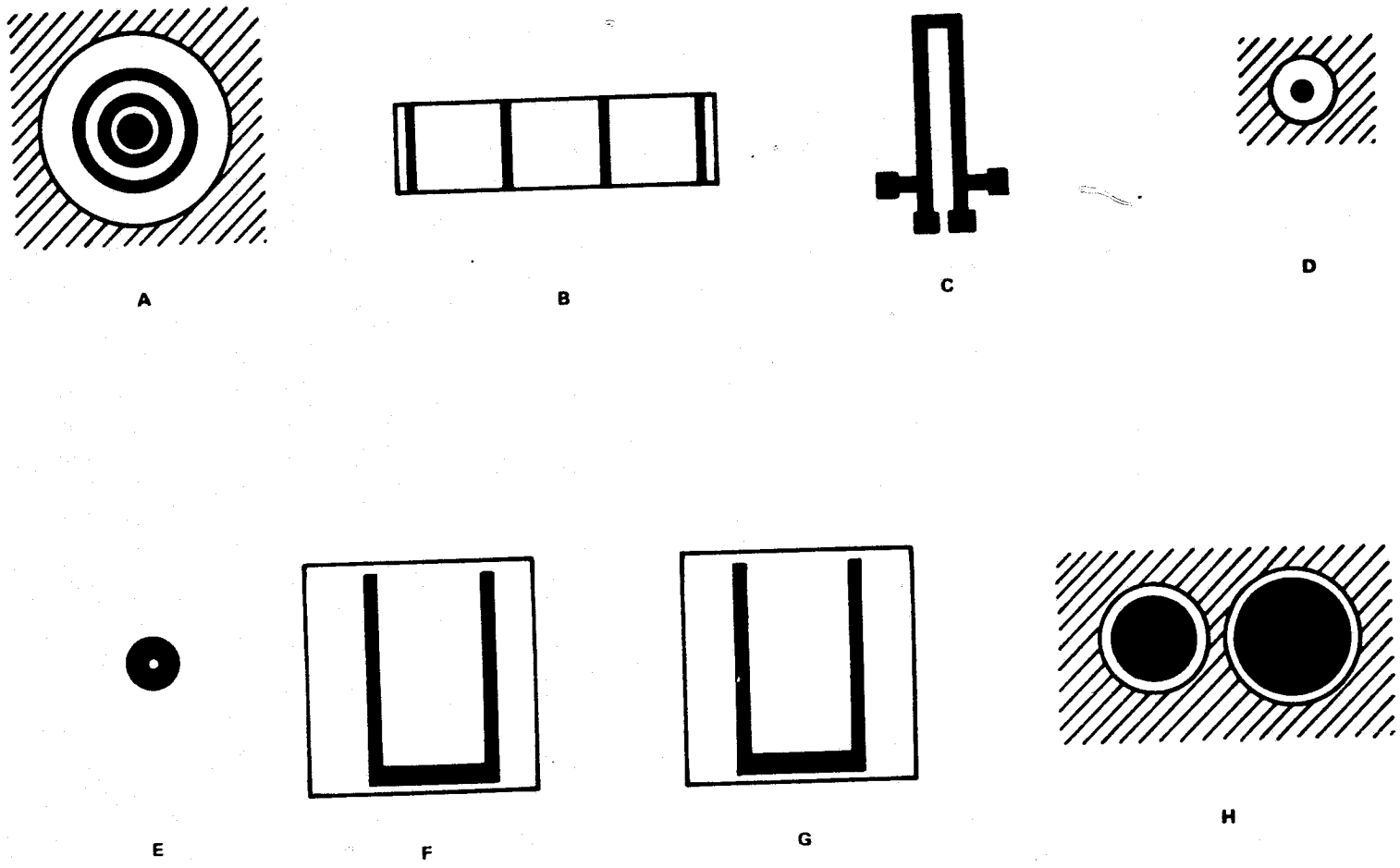


Figure 53. Test Devices

Table 23. Test Patterns and Their Functions

TEST PATTERN		PARAMETER MEASURED
(A)	Concentric ring pattern contacted to the diffused region (3 each)	Diffused sheet resistance, specific contact resistance
(B)	Parallel stripes contacted to the diffused region	Diffused sheet resistance, specific contact resistance
(C)	Metal pattern on top of oxide	Metal sheet resistance
(D)	Diode (3 each)	Junction saturation current density, base lifetime
(E)	Spreading resistance contact to base region on back side (2 each)	Base resistivity
(F)	Small area solar cell with AR coating	Light-generated current density, reflection efficiency
(G)	Small area solar cell with no AR coating	
(H)	MOS capacitor (2 each)	Surface states

The purpose of devices (A) and (B) is to measure the diffused region sheet resistance and specific contact resistance of the top side metallization. Device (B) has been described previously; diffused region resistance can be separated from contact resistance since width of the stripes is small compared to spacing between stripes. However, this pattern cannot be used universally; e.g., in planar N on P cells, a P^+ guard ring would be required to prevent inversion of the P-type base material. Such a guard ring is not compatible with cell processing. An analysis for extracting sheet resistance and specific contact resistance is discussed later. The parallel stripe pattern can be used to verify and calibrate parameters determined from the ring pattern. Three ring patterns allow measurement of resistance as a function of distance from center of the cell.

Two types of patterns are included for measurement of metal sheet resistance. One of the metal fingers of the main cell has four pads defined to denote 4-point probe locations for resistivity measurements. This is the preferred test pattern since essentially no space is lost from the cell. However, shunting by the diffused region will cause some inaccuracy. A second 4-point probe pattern (C) is included in one of the peripheral segments. This metal pattern is deposited over the oxide so that the diffused region does not shunt the current path. The latter pattern can be used to check accuracy of sheet resistance readings as measured on the metal finger patterns.

Small area diodes (device D) are included in the active portion of the cell to give convenient measurement of cell parameters, such as recovery time and dark IV characteristics. The diode area is 10^{-3} cm^2 for each of calculating current densities. There are three diodes at varying distances from the center of the cell.

Spreading resistance contacts (device E) are patterned in the back side metallization. After back side metal and before sintering, a concentric circular section is etched away to leave a 0.005-cm diameter contact. Sintering provides ohmic contact for the measurement of spreading

resistance R_{SR}. Then base resistivity can be calculated from the expression

$$R_{SR} = \rho_B \frac{1}{2d}$$

where d is the diameter of the contact; i.e.,

$$\rho_B = 0.01\ R_{SR}$$

Two small area solar cells are located in a peripheral segment. The area of each cell is 10^{-1} cm^2. One of the cells, device F, has the same AR coating as the large cell. Open-circuit voltage, short-circuit current density, and fill factor for this small area cell should approach those of an ideal cell. The second cell (device G) is identical except that there is no AR coating. Short-circuit current density for an optimized cell can be projected from measurements of this cell. Comparison with the AR cell gives an evaluation of the AR coating effectiveness.

Two MOS capacitors (pattern H) are included in another peripheral segment of the cell. Areas are 10^{-1} and 2×10^{-1} cm^2. For the planar cells, measurements of surface states may give useful information on excess diode currents or surface recombination velocity.

a. PROCESSING

Seven mask levels have been designed for versatility of processing. The levels required for the different patterns and for various process alternatives are shown in Table 24. Level three is for back side patterning; all other levels are for the front side.

Both N on P and P on N cells can be processed with either planar or mesa junctions. Level one defines the diffusion area for planar cells; level seven protects the cell when a mesa junction is etched. For planar P on N cells, level two protects the oxide over the junction during boron deglaze. Level four is for cutting contacts when the AR coating is applied before metallization. Level five is used for metal difinition in all process variations. For the case where AR coating is applied after metal, level six is used to expose metal pads; however, level six is needed in all cases to remove AR coating from one of the small test cells (device G).

b. CONCENTRIC RING TEST PATTERN

The concentric ring test pattern was designed for measurement of diffused region sheet resistance and specific contact resistance. This structure, shown in Figure 54, consists of concentric metal rings which make contact to the diffused region. The geometry and number of rings can be

Table 24. Mask Level/Test Pattern Matrix

Mask	Level	7.6 cm Hex		Planar								Mesa							
		N on P	P on N	A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H
$N^+(P^+)$ Diffusion	1	X	X		X		X		X	X									
Deglaze O.R.	2				X		X		X	X									
Al Etch	3	X	X					X								X			
Contact O.R.	4	X	X	X	X		X		X	X		X	X		X		X	X	
Metal Definition	5	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X
Overcoat O.R.	6	X	X	X	X	X	X		X	X	X	X	X	X	X		X	X	X
Mesa Etch	7	X	X										X		X		X	X	

Concentric Ring
Contact Stripes
4 PT – Metal
Diode
Spreading Resistance
Small Cell AR
Small Cell W/O AR
MOS Capacitor
Concentric Ring
Contact Stripes
4 – PT Metal
Diode
Spreading Resistance
Small Cell AR
Small Cell W/O AR
MOS Capacitor

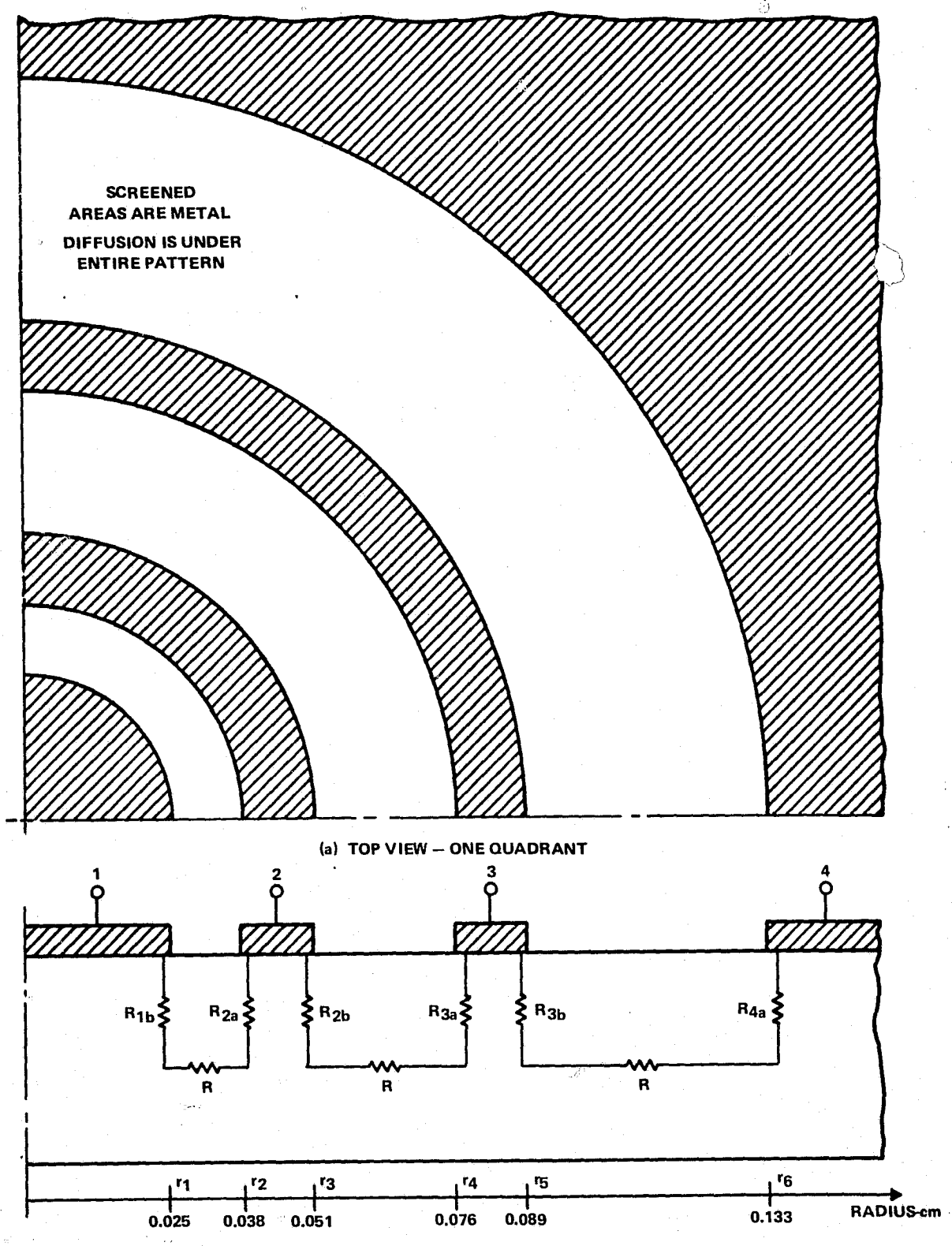


Figure 54. Concentric Ring Test Pattern

varied. For ease of analysis, the ratios of inner to outer diameters were made equal for each concentric semiconductor section.

Resistance values are measured between each pair of adjacent terminals. The lateral resistance of each circular semiconductor section is given by

$$R_o = \frac{\rho_s}{2\pi} \ln \frac{r_a}{r_b} \tag{78}$$

where

ρ_s = sheet resistance of the diffused region

r_a = outside radius of the semiconductor section

r_b = inside radius

In the structure of Figure 54, the ratio for each section is the same, i.e.,

$$\frac{r_a}{r_b} = \frac{r_2}{r_1} = \frac{r_4}{r_3} = \frac{r_6}{r_5} = 1.5$$

If contact resistance is negligible, the resistance measured between each pair of contacts would be

$$R_o = 0.06453\, \rho_s$$

In practice, the resistance between contacts decreases as contact radii increase. Sheet resistance of the diffused region and specific contact resistance can be determined from a set of these measurements.

The test structure can be designed such that the contact resistance from diffused region to metal is inversely proportional to the radius of the boundary between contact and semiconductor. Then, the resistance of the semiconductor ring bounded by two concentric contacts, M and N, is of the form

$$R_{MN} = R_o + A\left(\frac{1}{r_M} + \frac{1}{r_N}\right) \tag{79}$$

where

M = outer contact

r_M = inner radius of M

N = inner contact

r_N = outer radius of N

The values of R_o and A may be determined from a plot of R_{MN} versus $(1/r_M + 1/r_N)$ for each set of adjacent terminals, i.e., R_o is the intercept and A is the slope. Sheet resistance, ρ_s, is determined from R_o using Equation (78).

The slope A increases with specific contact resistance, ρ_c, and sheet resistance, ρ_s. Quantitative relationships can be established for specific geometries. Depending upon the expected range of sheet resistance and specific contact resistance, the magnitudes of the radii can be set for ease of interpreting the measured values R_o and A.

Current flows from the diffused region to the metal contact through a distributed resistive network. For high values of the ratio ρ_s/ρ_c, current flow is confined to a narrow band at the periphery of the contact, and the contact resistance approximates the characteristic impedance of a transmission line; i.e.,

$$R_c = Z_o = \frac{1}{W} = \sqrt{\rho_s \rho_c}$$

where

$W = 2\pi r$

is the width of the line and r is the radius at the periphery of the contact. The slope A of equation (79) is given by

$$A = \frac{1}{2\pi}\sqrt{\rho_S \rho_C} \tag{80}$$

For typical values of ρ_S and ρ_C, equation (80) is a good approximation.

As shown in Figure 42, the concentric ring structure (Pattern A) is in the metal trunk line; since the trunk line is later covered by a bus bar, the pattern does not reduce the active area of the cell. The structure of Figure 54 was fabricated on the first cells. The design was later modified to the pattern of Figure 55, consisting of four metal contact rings of equal width. The latter design more nearly approximates the conditions assumed for equations (79) and (80).

The essential feature of the test pattern discussed here is the use of successive closed bands on the surface of a semiconductor to measure sheet resistance and contact resistance of a surface layer (e.g., a diffused region). Since this surface region extends under the entire pattern, the conduction paths are defined by the metal geometry rather than by planar diffusions.

The dimensions and shape of the metal bands may be varied. Selection of geometries is based on compatibility with process steps for the device to be monitored, and ease of interpretation of resistance readings. Specific relationships for determining sheet resistance and contact resistance from measured values of resistance must be developed for individual designs.

4. Experimental Results

a. MEASURED PARAMETERS

Slice runs were processed for a range of diffusion variables. This experiment was used as a vehicle for evaluating the test patterns as well as to develop device and process models.

The measured results of this experiment are summarized in Table 25. The definition of these parameters and methods of measurement are discussed in the following paragraphs.

The cell parameters V_{OC} and I_{SC} of Table 25 were measured for simulated AM0 conditions. Power output, curve factor, and conversion efficiency are for AM0 conditions and neglect series resistance. Power output, so defined, was determined experimentally as a function of diffusion variables. Optimum spacing of metal stripes for each value of sheet resistance and the corresponding series resistance losses can be determined by the technique described earlier in this report.

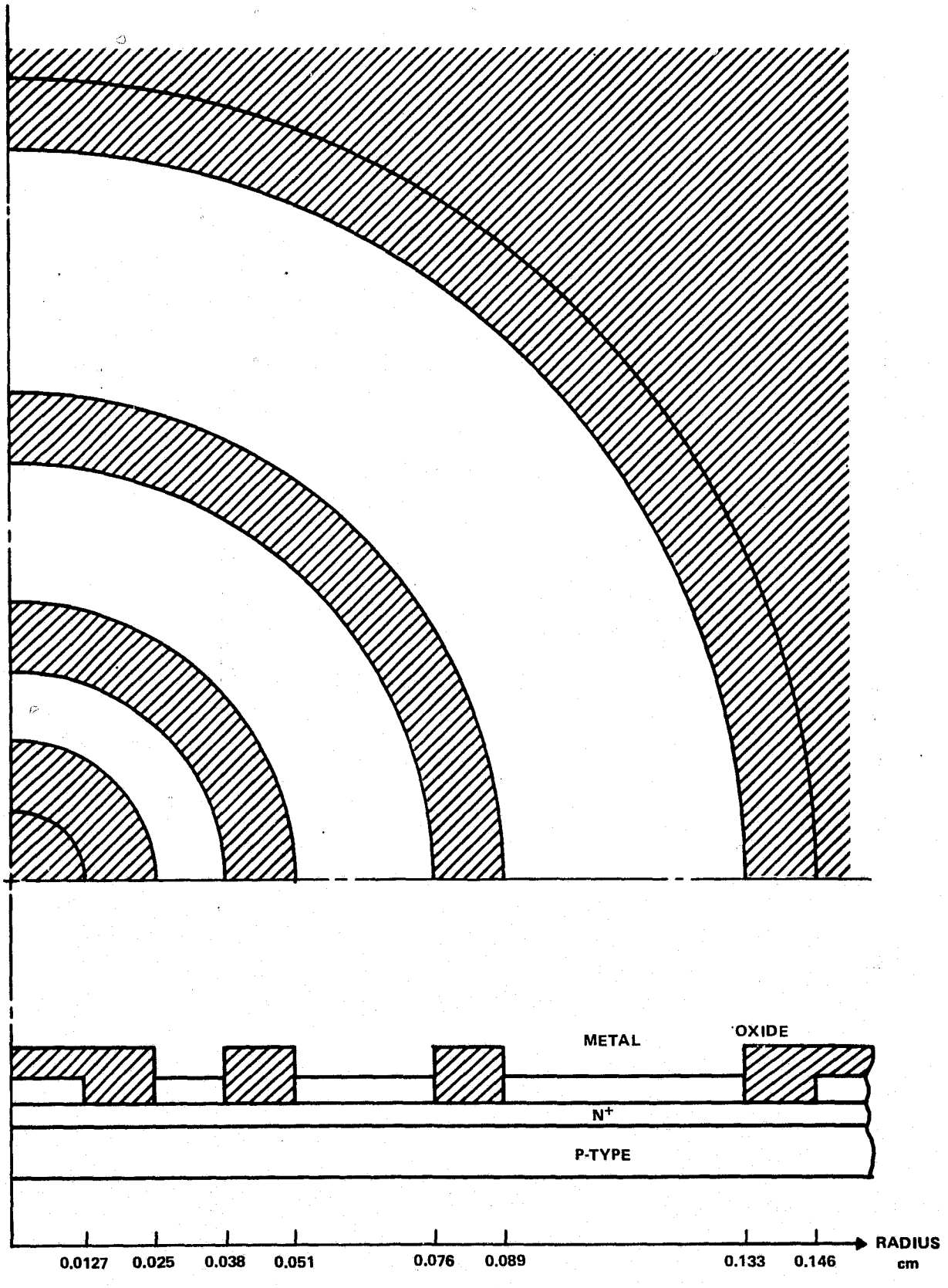


Figure 55. Concentric Ring Test Pattern for Hexagonal Solar Cell

Table 25. Summary of Parameters For Experimental Diffusion Runs

Parameter	Units	A-1	A-2	A-3	B-1	B-2	B-3	C-1	C-2	C-3
Diffusion Temperature	°C		850			850			850	
Diffusion Time	MIN		15			7			45	
Heat Treatment Time	MIN		20			12			50	
Sheet Resistance - Pilot	Ω/□		73			133			37	
Open Circuit Voltage (AM0)	Volts	0.588	0.591		0.565		0.588	0.599		0.600
Short Circuit Current (AM0)	Amps	1.03	1.01		1.00		1.12	0.93		0.94
Curve Factor (AM0)		0.81	0.82		0.75		0.80	0.80		0.79
Power Output (AM0)	Watts	0.49	0.49		0.43		0.53	0.45		0.45
Conversion Efficiency (AM0)	%	9.6	9.6		8.3		6.3	8.0		8.7
Diffused Sheet Resistance	Ω/□	93	86	87	185	170	160	47		44
Specific Contact Resistance	$\Omega\ cm^2$	$<6X10^{-5}$	$<6X10^{-5}$	$<6X10^{-5}$	$<1X10^{-4}$	$<1X10^{-4}$	$<1X10^{-4}$	$<3X10^{-5}$		$<3X10^{-5}$
Metal Sheet Resistance - Stripe	Ω/□	0.02	0.005		0.0051		0.0045	0.0046		0.0051
Metal Sheet Resistance - Pattern C	Ω/□	0.023	0.0075	0.0089	0.0074			0.0064		0.0068
Metal Thickness	μm	2.2	3.8	3.0	3.5		3.8	3.5		3.8
Reverse Recovery Time	μs	28	28	30	28		30	28		28
Constant I_{SC} Lifetime	μs	8.6			8.2			11.7		

Table 25. Summary of Parameters for Experimental Diffusion Runs (Continued)

Parameter	Units	D-1	D-2	D-3	E-1	E-2	E-3	F-1	F-2	F-3
Diffusion Temperature	°C		850			850			850	
Diffusion Time	MIN		135			15			15	
Heat Treatment Time	MIN		140			140			20	
Sheet Resistance - Pilot	Ω/□		25			64			283	
Open Circuit Voltage (AM0)	Volts		0.596	0.593	0.600	0.595	0.588	0.548	0.533	
Short Circuit Current (AM0)	Amps		0.94	0.94	1.06	1.04	1.06	1.03	1.05	
Curve Factor (AM0)			0.78	0.74	0.81	0.79	0.71	0.74	0.78	
Power Output (AM0)	Watts		0.44	0.42	0.51	0.49	0.44	0.41	0.44	
Conversion Efficiency (AM0)	%		8.6	8.1	10.1	9.5	8.6	8.1	8.6	
Diffused Sheet Resistance	Ω/□	25	25	26	75	75	73	330	370	
Specific Contact Resistance	Ω cm^2	$<2X10^{-5}$	$<2X10^{-5}$	$<2X10^{-5}$	$<5X10^{-5}$	$<5X10^{-5}$	$<5X10^{-5}$	$3X10^{-4}$	$2X10^{-4}$	
Metal Sheet Resistance - Stripe	Ω/□		0.0052	0.0055	0.0059	0.005	0.0056	0.0042		
Metal Sheet Resistance - Pattern C	Ω/□		0.0087		0.0069		0.0075	—	0.0081	
Metal Thickness	μm		3.3	2.9	3.5	4.0	3.2	3.5	3.0	
Reverse Recovery Time	μs		26	26	28	28	26	28	30	
Constant I_{SC} Lifetime	μs		9.1		7			8.6		

Table 25. Summary of Parameters for Experimental Diffusion Runs (Continued)

Parameter	Units	G-1	G-2	G-3	H-1	H-2	H-3	I-1	I-2	I-3
Diffusion Temperature	°C		800			800			800	
Diffusion Time	MIN		45			135			15	
Heat Treatment Time	MIN		50			140			140	
Sheet Resistance - Pilot	Ω/□		104			74			178	
Open Circuit Voltage (AM0)	Volts		0.583	0.585	0.598	0.596	0.599	0.584	0.561	0.584
Short Circuit Current (AM0)	Amps		1.08	1.04	1.00	1.01	1.02	1.05	1.06	1.04
Curve Factor (AM0)			0.79	0.75	0.81	0.81	0.80	0.79	0.73	0.79
Power Output (AM0)	Watts		0.50	0.46	0.48	0.49	0.49	0.49	0.43	0.48
Conversion Efficiency (AM0)	%		9.7	8.9	9.5	9.6	9.6	9.5	8.5	9.4
Diffused Sheet Resistance	Ω/□		120	120	78	76	77	210	260	220
Specific Contact Resistance	Ω cm^2		$<8X10^{-5}$	$<8X10^{-5}$	$5X10^{-5}$	$<5X10^{-5}$	$<5X10^{-5}$	$<1X10^{-4}$	$<1X10^{-4}$	$<1X10^{-4}$
Metal Sheet Resistance - Stripe	Ω/□	0.0034	0.0051	0.0057	0.0042	0.0046	0.0063	0.0049	0.0005	0.0058
Metal Sheet Resistance - Pattern C	Ω/□		0.0078	0.012	—	0.0065	0.0079	0.0078	0.0075	
Metal Thickness	μm	3.8	3.0	2.7	3.0	3.0	3.0	3.5	3.0	3.2
Reverse Recovery Time	μs		30	28	30	28	30	30	28	30
Constant I_{SC} Lifetime	μs	9.4			8.7			7.5		

Table 25. Summary of Parameters for Experimental Diffusion Runs (Continued)

Parameters	Units	J-1	J-2	J-3	K-1	K-2	K-3	L-1	L-2	L-3
Diffusion Temperature	°C		900			900			900	
Diffusion Time	MIN		7			15			45	
Heat Treatment Time	MIN		12			20			50	
Sheet Resistance - Pilot	Ω/□		47			29			15	
Open Circuit Voltage (AM0)	Volts	0.601	0.600	0.601	0.603		0.603		0.603	
Short Circuit Current (AM0)	Amps	1.05	1.05	1.05	0.89		0.91		0.91	
Curve Factor (AM0)		0.80	0.81	0.79	0.79		0.79		0.80	
Power Output (AM0)	Watts	0.49	0.51	0.50	0.42		0.44		0.44	
Conversion Efficiency (AM0)	%	9.6	10.0	9.8	8.3		8.5		8.6	
Diffused Sheet Resistance	Ω/□	57	54	57		36	36	20	20	20
Specific Contact Resistance	Ω cm^2	$<4X10^{-5}$	$<4X10^{-5}$	$<4X10^{-5}$		$<2X10^{-5}$	$<2X10^{-5}$	$<1X10^{-5}$	$<1X10^{-5}$	$<1X10^{-5}$
Metal Sheet Resistance - Stripe	Ω/Ψ	0.0056	0.0052	0.0042	0.0043	0.0005			0.0049	0.0056
Metal Sheet Resistance - Pattern C	Ω/□	0.0077		0.0055	0.0059		0.0063		0.0071	0.0078
Metal Thickness	μm	3.8	3.8	3.8	2.7				3.7	3.7
Reverse Recovery Time	μs	30	30	28	28		28		28	28
Constant I_{SC} Lifetime	μs	8.2			8.8		8.9		9.1	

Table 25. Summary of Parameters for Experimental Diffusion Runs (Concluded)

Parameter	Units	M-1	M-2	M-3	N-1	N-2	N-3	O-1	O-2	O-3
Diffusion Temperature	°C		900			950			950	
Diffusion Time	MIN		15			7			15	
Heat Treatment Time	MIN		50			12			20	
Sheet Resistance - Pilot	Ω/□		27			22			13	
Open Circuit Voltage (AM0)	Volts		0.603	0.604	0.603	0.601	0.603	0.600	0.600	0.599
Short Circuit Current (AM0)	Amps		1.00	1.01	0.99	0.99	0.99	0.88	0.88	0.88
Curve Factor (AM0)			0.79	0.80	0.81	0.79	0.79	0.80	0.80	0.76
Power Output (AM0)	Watts		0.48	0.49	0.48	0.47	0.47	0.42	0.42	0.40
Conversion Efficiency (AM0)	%		9.4	9.6	9.4	9.2	9.2	8.3	8.3	7.8
Diffused Sheet Resistance	Ω/□	36	32	33	26	26	26	14	16	16
Specific Contact Resistance	Ω cm^2	<2X10^{-5}	<2X10^{-5}	<2X10^{-5}	<2X10^{-5}	<2X10^{-5}	<2X10^{-5}	<1X10^{-5}	<1X10^{-5}	<1X10^{-5}
Metal Sheet Resistance - Stripe	Ω/□		0.005	0.0052	0.0066	0.0049	0.0049	0.0040	0.0050	
Metal Sheet Resistance - Pattern C	Ω/□		0.0071	0.0077	0.006	0.0092	0.0069	0.0066	0.0071	0.0053
Metal Thickness	μm		3.1	3.3	2.5	3.3	3.5	5.1	3.8	3.8
Reverse Recovery Time	μs		28	28		28	28	28	28	26
Constant I_{SC} Lifetime	μs		5.7		6.2			6.3		

Power output was determined from the equivalent circuit model of Figure 44, assuming $R_S = 0$. The light-generated current, I_L, for the model was the measured short circuit current at AM0. The diode characteristic, $I_d(V)$, was obtained using the "diode forward characteristic" method described by Wolf and Rauschenback;[12] i.e., measuring open circuit voltage and short circuit current as light intensity is varied. It is shown later (Figure 60) that this characteristic is the same as the forward dark characteristic, for low currents where the series resistance drop is negligible.

The measured V_{OC} - I_{SC} characteristic for a typical cell is plotted in Figure 56. The "photovoltaic output characteristics,"[12] obtained graphically from this characteristic, i.e., $I(V) = I_L - I_d(V)$ is plotted in Figure 57. From this plot, the maximum power point (V_M, I_M) is obtained graphically. The curve factor is calculated from

$$CF = \frac{(V_M)\,(I_M)}{(V_{OC})\,(I_{SC})} \tag{81}$$

It is noted that the curve factor approaches the theoretical value ($\approx$ 82% for V_{OC} = 0.6 volt). This is to be expected since the planar junctions give low values of excess ($I \times \alpha \exp [qV/nKT]$) currents, and series resistance is neglected.

The remaining physical parameters of Table 25 are discussed in conjunction with the corresponding measurement techniques.

The resistance characteristic for a concentric ring pattern of a cell typical of those fabricated early in the contract is shown in Figure 58. Resistance between adjacent contacts is plotted as a function of reciprocal radius [as defined for Eq. (79)]. Resistance should increase with reciprocal radius if contact resistance is significant. The characteristic of Figure 58 after oxide thinning was first interpreted as resulting from high contact resistance. However, the three resistance values were all about equal to R_o prior to oxide thinning. Physical observations indicated that undercutting of contacts occurred during the oxide thinning process. It can be see from Eq. (78) that undercutting will cause increase of resistance for small radii.

The concentric ring pattern proved valuable for identifying the undercut problem. The process sequence has since been modified to avoid this contact degradation.

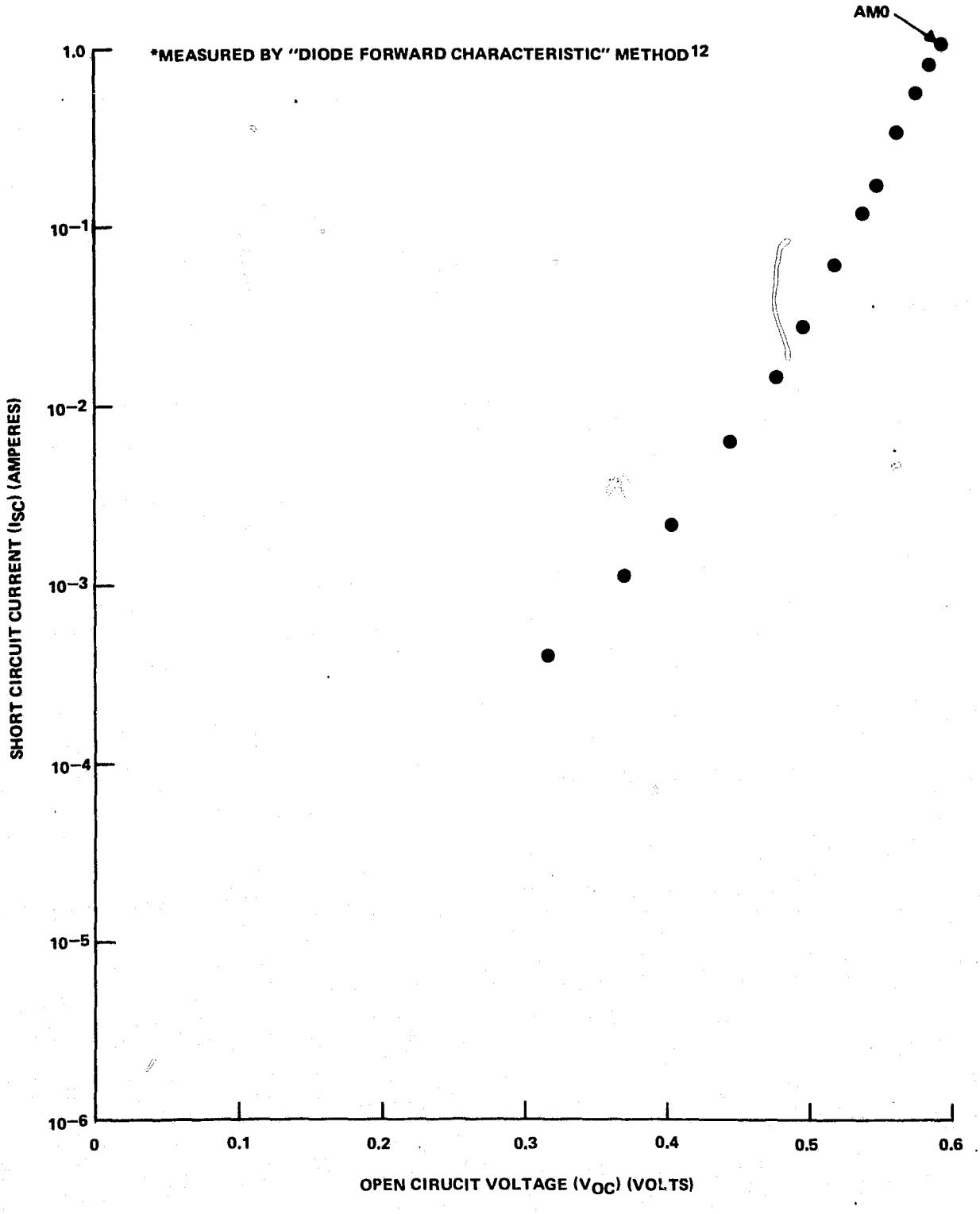


Figure 56. Volt Ampere Characteristic* for Typical Hexagonal Cell (A-2), Neglecting Series Resistance Loss

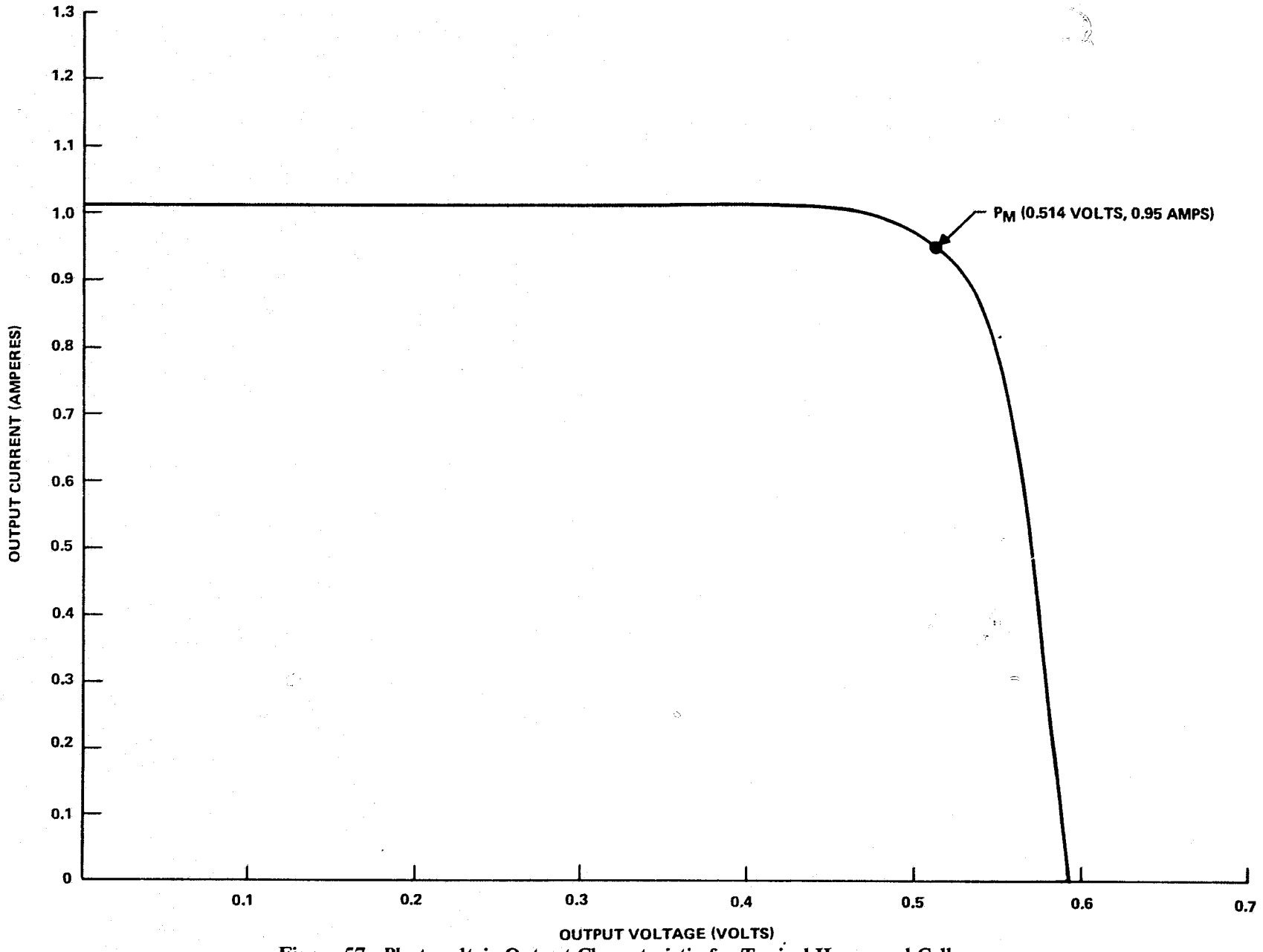


Figure 57. Photovoltaic Output Characteristic for Typical Hexagonal Cell (A-2), Neglecting Series Resistance Loss

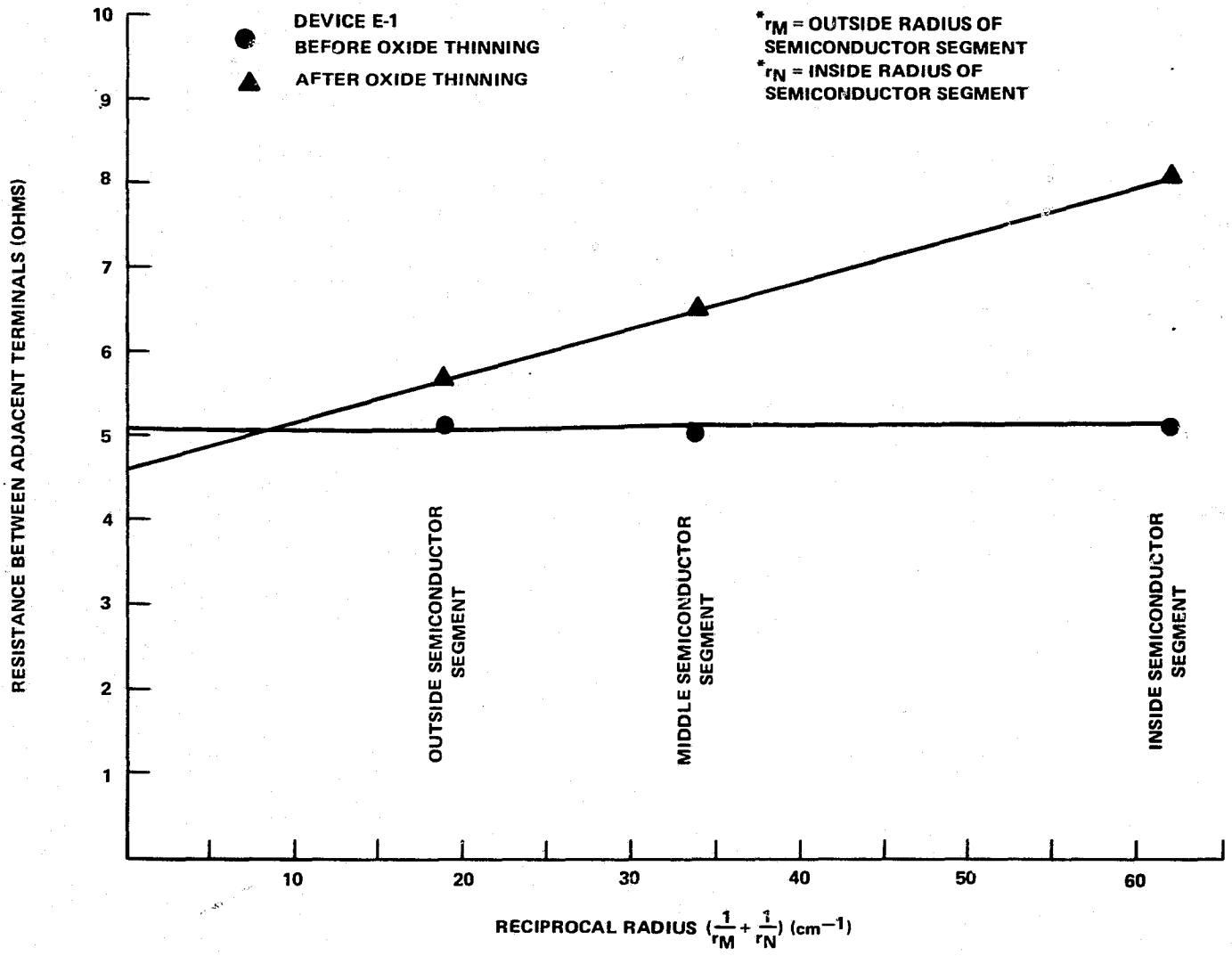


Figure 58. Resistance Between Adjacent Terminals of Concentric Ring Test Pattern vs. Reciprocal Radius $(1/r_M + 1/r_N)^*$

For cells which had not had the oxide thinned, slight variations of resistance with radius were observed. Generally, these were random and attributed to patterning tolerances. It was assumed for this analysis that contact resistance R_C could not be resolved if

$$R_C < 0.1\ R_o$$

From Equations (78) and (80), the above condition is equivalent to

$$\rho_C \leq (1 \times 10^{-4})\ (\rho_S)\ (R_C/R_O)^2$$

Values of diffused sheet resistance and specific contact resistance from measurements of concentric ring patterns are listed in Table 26. Sheet resistance values from concentric ring measurements average about 20% higher than sheet resistance values determined from the corresponding pilot slices. This could be due to misalignment of the metal rings with the contact rings, since the metal rings were designed with no overlap. In future designs, metal rings *will* overlap the contact rings.

For most of the cells, limits were obtained for contact resistance rather than absolute values. Future designs should allow better resolution, e.g., by using smaller radii and smaller width of contact rings.

Sheet resistance was also measured using the parallel stripe test pattern [Figure 53 (b)]. Comparative measurements for the three techniques are shown in Table 26. Assuming the pilot slice values to be correct, the parallel stripe pattern appears to give better accuracy than the concentric ring. (Inversion layers are apparently not a problem for these cells). However, the concentric ring pattern is more compatible with in-line processing and has reasonable accuracy. Accuracy should be improved by redesign as discussed above.

Metal resistance was measured using the four-point probe method for both metal test pattern C (Figure 53) fabricated over the oxide, and a four-piont test pattern formed on one of the metal stripes contacting the diffused region in the active area. An enlarged diagram of the latter is shown in Figure 59. It was observed that the sheet resistance values obtained from the active stripes were substantially lower than for test pattern C. Furthermore, the values increased as the current source probes (initially on pads 1 and 4) were moved closer to the voltmeter probes (on pads 2 and 3). The interpretation is that the current is shunted by the diffused layer and by adjacent metal stripes. When the voltage probes were moved to pads 1 and 2, with the current probes just outside these pads, the sheet resistance more closely approached that obtained from test pattern C. The metal

Table 26. Comparison of Measured Values of Sheet Resistance

Slice No.	Measured Sheet Resistance—ohms Per Square		
	Pilot Slice	Concentric Ring Pattern	Parallel Stripe Test Pattern
A-3	73	87	77
B-3	133	160	121
C-3	37	44	40
D-	23		
E-3	64	73	66
F-2	283	370	323
G-3	104	122	110
H-3	74	77	77
I-2	178	260	150
J-	47		
K-3	29	36	37
L-3	15	20	19
M-	27		
N-3	22	26	24
O-3	13	16	14.5

sheet resistance values obtained from both patterns are listed in Table 25. The ratio of metal sheet resistance obtained from pattern C to that determined from the active cell stripe ranges from 1.2 to 1.6 in most cases. Readings for pattern C were omitted for cells in which the metal of the peripheral segment obviously did not plate. The ratio of the two values is not correlated with diffused region sheet resistance. Metal thickness after plating, as measured by Talysurf on the wide trunk line, is also listed in Table 25. In general, sheet resistance calculated from metal thickness is in reasonable accord with measured sheet resistance.

It is concluded that metal sheet resistance can be measured on the active cell stripes for diffused region sheet resistance as low as 13 ohms per square. Future designs should be modified to minimize spacing between voltage probes and position them at the end of the stripe.

Measurement of base resistance from the spreading resistance pattern on the back of the slice had limited success. The pad size (2 mils diameter) made probing extremely difficult. Resistance of the probe was of the order of 0.3 ohms. Use of a smaller probe would cause significant error.

Base resistance as determined from measurements of the spreading resistance test patterns is shown in Table 27 for several cells. These are in good agreement with four-point probe measurements on the slices prior to processing.

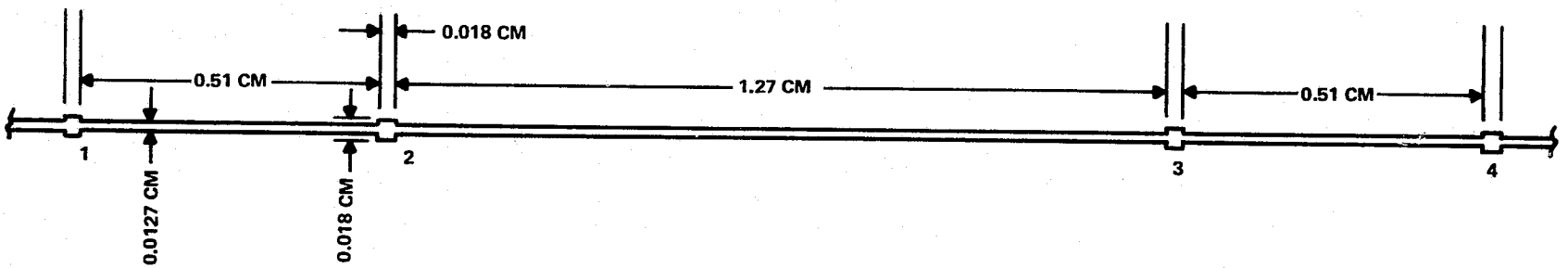


Figure 59. Four-Point Probe on Contact Stripe of Cell

Table 27. Base Resistivity of Cells as Measured From Spreading Resistance Test Patterns and Four Point Probe

Cell	Base Resistance ohm-cm	
	Spreading Resistance Test Pattern	Four-Point Probe Starting Slice
G-3	0.59	0.58
H-3	0.62	0.57
I-3	0.63	0.58
L-3	0.62	0.57
M-3	0.61	0.58

The test pattern appears useful; however, larger diameter pads are needed to facilitate probing. Larger diameter pads should be investigated to determine if there is a pad size which gives both accuracy and ease of probing.

Volt ampere characteristics for a typical hexagonal cell are plotted in Figure 60. The characteristic was measured in two ways. Curve A is the dark current characteristic measured with an external battery. Curve B is the "diode forward characteristic"[12] from measurements of open circuit voltage and short circuit current for varying light intensity. Also plotted (Curve C) is the volt ampere characteristic for a small diode fabricated on the cell. All three curves are plotted in terms of current density for comparison.

Curves A and B are in good agreement for low values of current. For larger values of current IR drops are significant in Curve A, and Curve B is the correct characteristic. The higher dark current density for the small diode (Curve C) is probably due to higher current density injected into the N^+ diffused region. This might be expected since half the surface of the diode is contacted by metal and has high surface recombination velocity.

Comparison of the two volt-ampere characteristics (Curves B and C) warrants further study but was not pursued here due to lack of time.

The purpose of the small test cells was to evaluate the AR coating. It was intended that Pattern F would have an AR coating like that of the hexagonal cell and that AR coating would be removed from Pattern G in a final etch step. The mask for this etch step was also intended for opening contacts when the AR coating was deposited after metal. Contact openings were mistakenly made the same size as the metal pattern (for the hexagonal cell). This imperfect alignment caused catastrophic undercutting when the AR coating was etched. A future design for this mask should open oxide only in bond (or probe) areas and the active area of test pattern G.

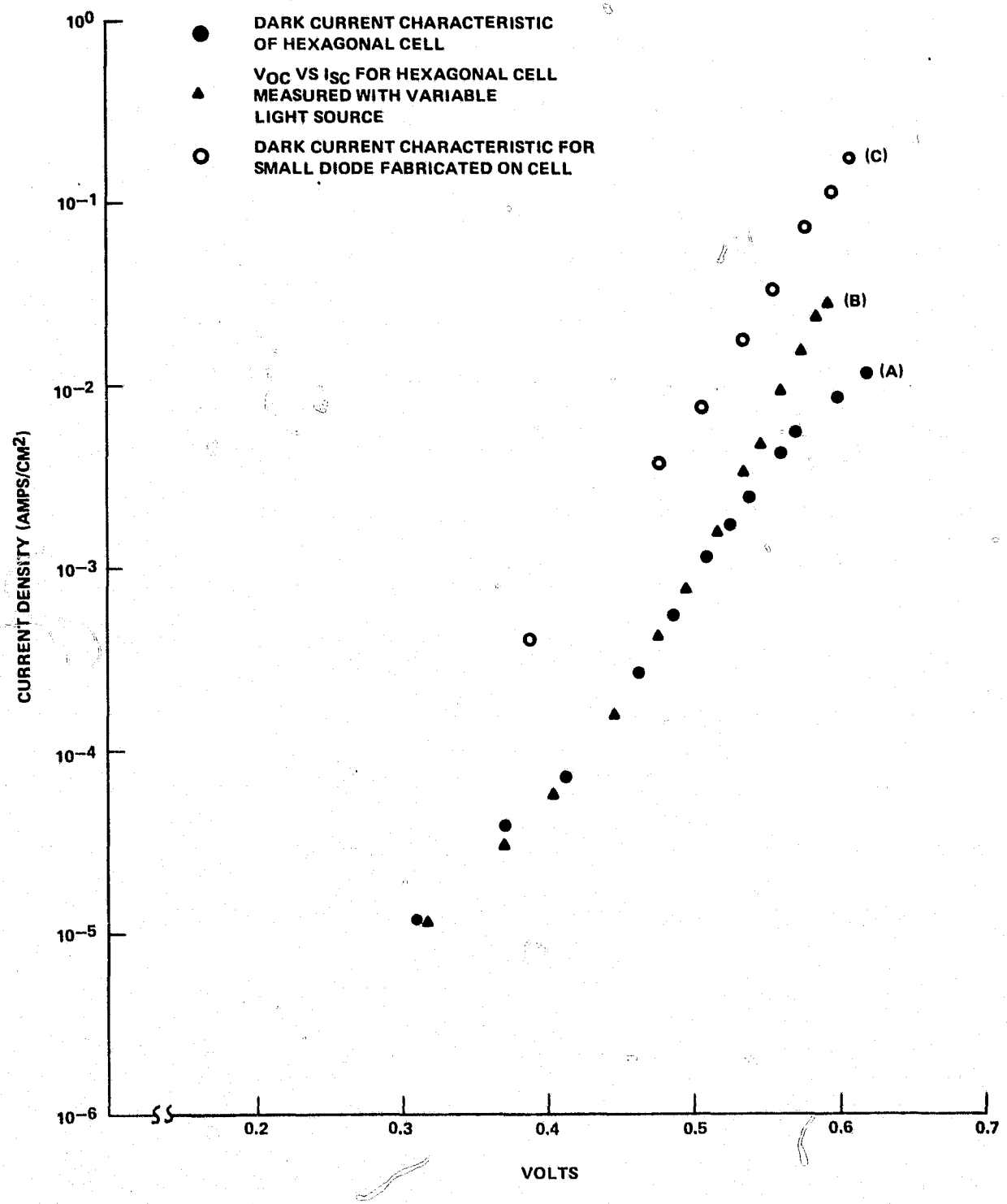


Figure 60. Current Density versus Forward Voltage for Typical (A-2) Hexagonal Cell

b. CELL PERFORMANCE VS DIFFUSION VARIABLES

Experimental diffusion runs were carried out for N on P-type cells using the hexagonal cell with test patterns shown in Figure 42. Material characteristics for the substrate are:

Type	P
Dopant	Boron
Resistivity	0.55 to 0.62 ohm-cm
Orientation	⟨111⟩
Lifetime	30 μs
Thickness	0.041 cm

The diffusion source was $POCl_3$. Fifteen groups of three slices each were processed, varying time at four diffusion temperatures. The diffusions were performed in a single furnace operation.

Times at the various diffusion temperatures are indicated in Table 25. Slow-push, slow-pull was used in all cases. Diffusion time, T_D, includes time of source deposition plus a 3-minute flush time after deposition. Heat treatment time, T_{HT}, is the total time at the diffusion temperature. For most runs, this is the sum of diffusion time plus a 5-minute stabilization time prior to application of the source. However, for runs E, I, and M, longer stabilization times were used so that diffusion profile effects could be separated from heat treatment effects. For example, slices A and E should have similar profiles but different heat treatment times; D and E have the same heat treatment time with different profiles.

Sheet resistance was measured on P-type pilot slices for each run. These readings are plotted as a function of diffusion time in Figure 61. For each temperature, a best-fit straight line is plotted with a slope of $-1/2$ on the log-log scale (i.e., for $\rho_s \propto T_D^{-1/2}$). Most points for a given temperature are very close to the straight line approximation. The inference is that surface concentration does not vary and junction depth increases as a square root of time for a constant temperature.

Junction depth was also measured where practical on the pilot slices. Because optical techniques were used, it was not possible to measure the very shallow junctions, accuracy is poor even for the deeper diffusions. Measured values of junction depth are plotted in Figure 62. A best-fit line with slope 1/2 has been drawn for each temperature.

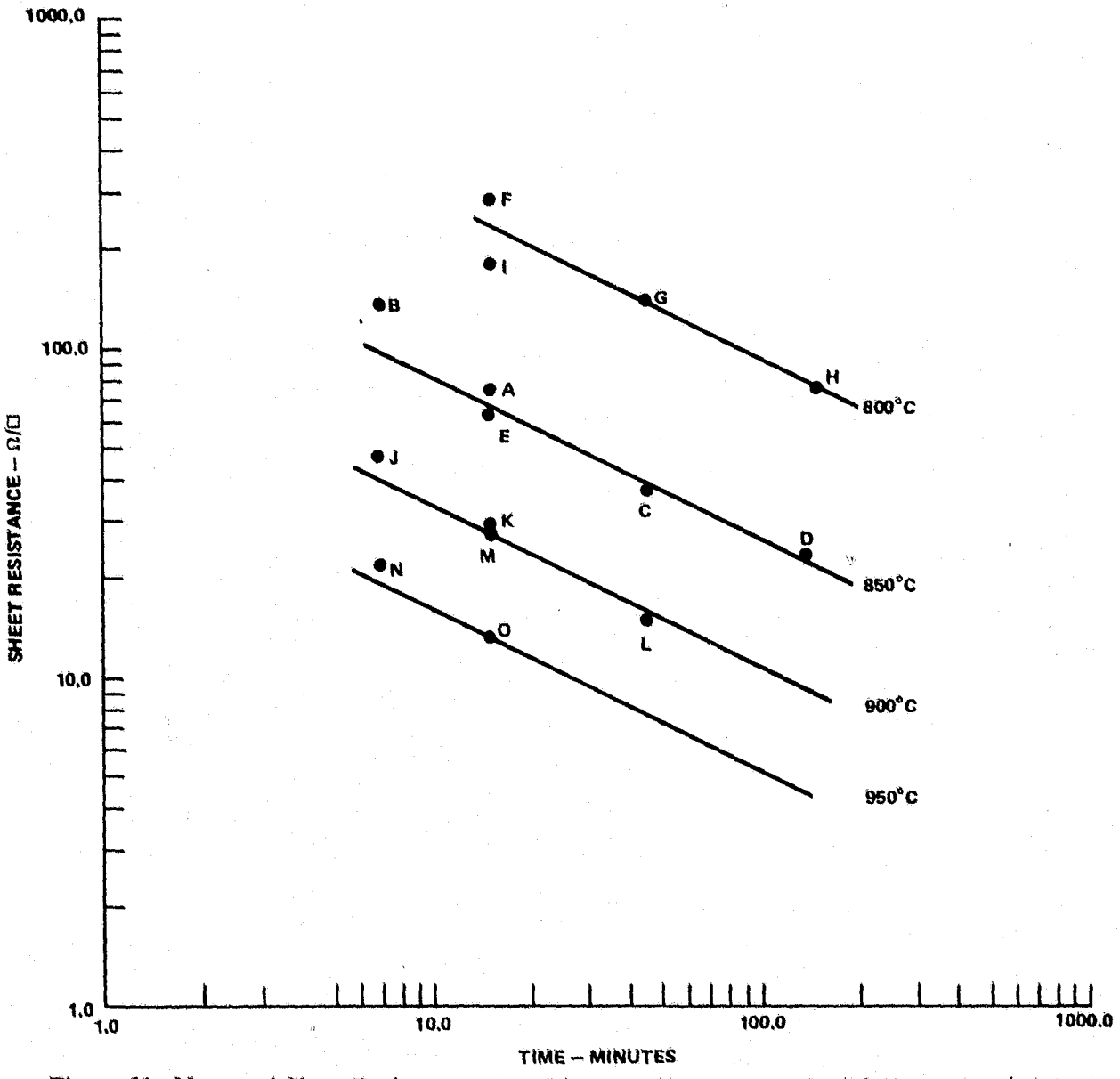


Figure 61. Measured Sheet Resistance versus Time and Temperature for $POCl_3$ (100 cc/min)

Base lifetime was measured on each cell using the constant short circuit current technique.[13] Lifetime is plotted in Figure 63 as a function of diffusion time and temperature.

The trends indicated in this plot are:

- Lifetime increases slightly with phosphorus diffusion time. There is some indication of a peak at about 50 minutes.
- Temperatures of 950° are detrimental.
- Heating prior to phosphorus diffusion is detrimental.

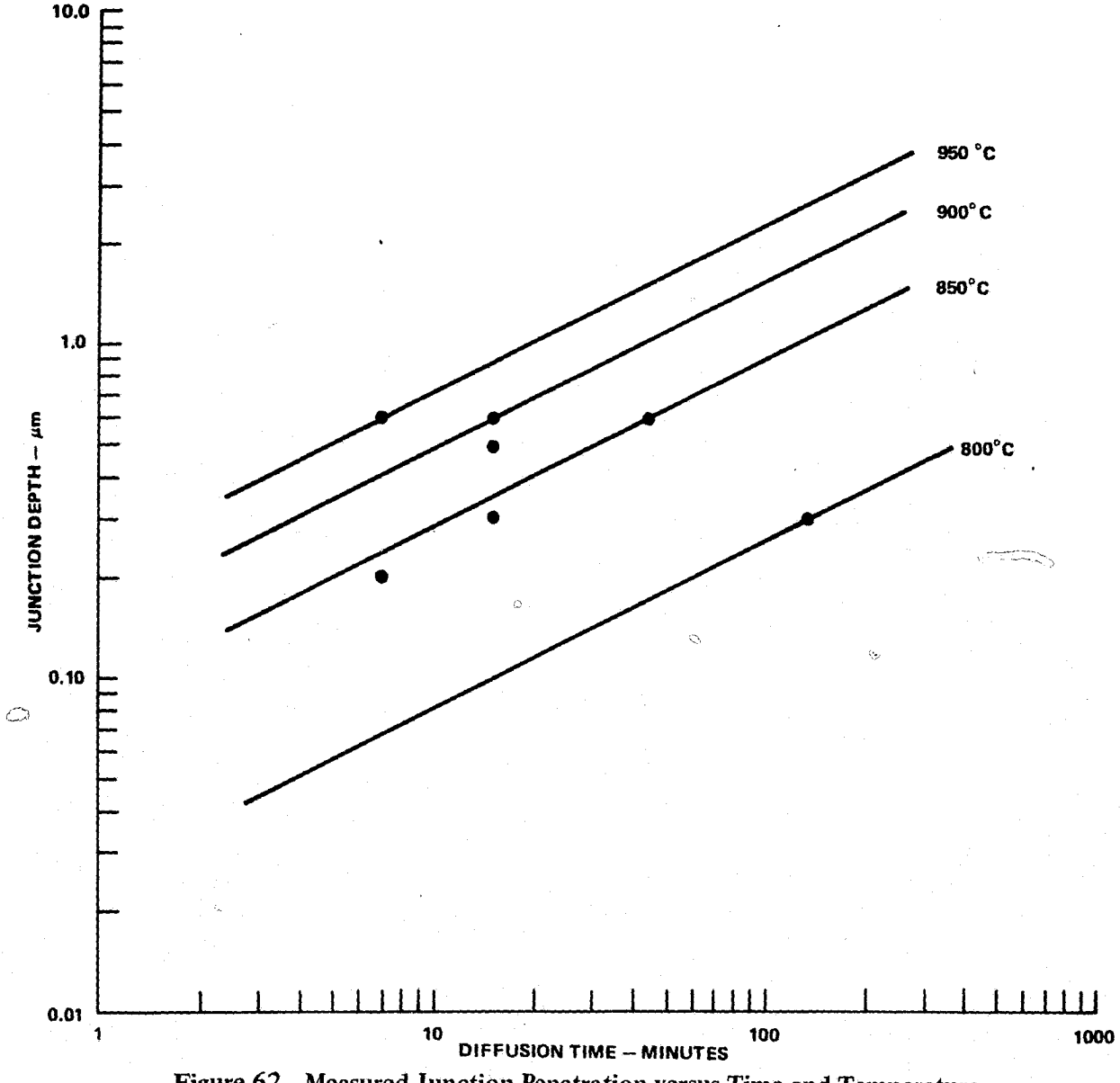


Figure 62. Measured Junction Penetration versus Time and Temperature for $POCl_3$ (100 cc/min)

Reverse recovery times measured for the junctions of the hexagonal cells are shown in Table 25. These values are approximately 3 times the lifetimes obtained from the constant I_{SC} technique.

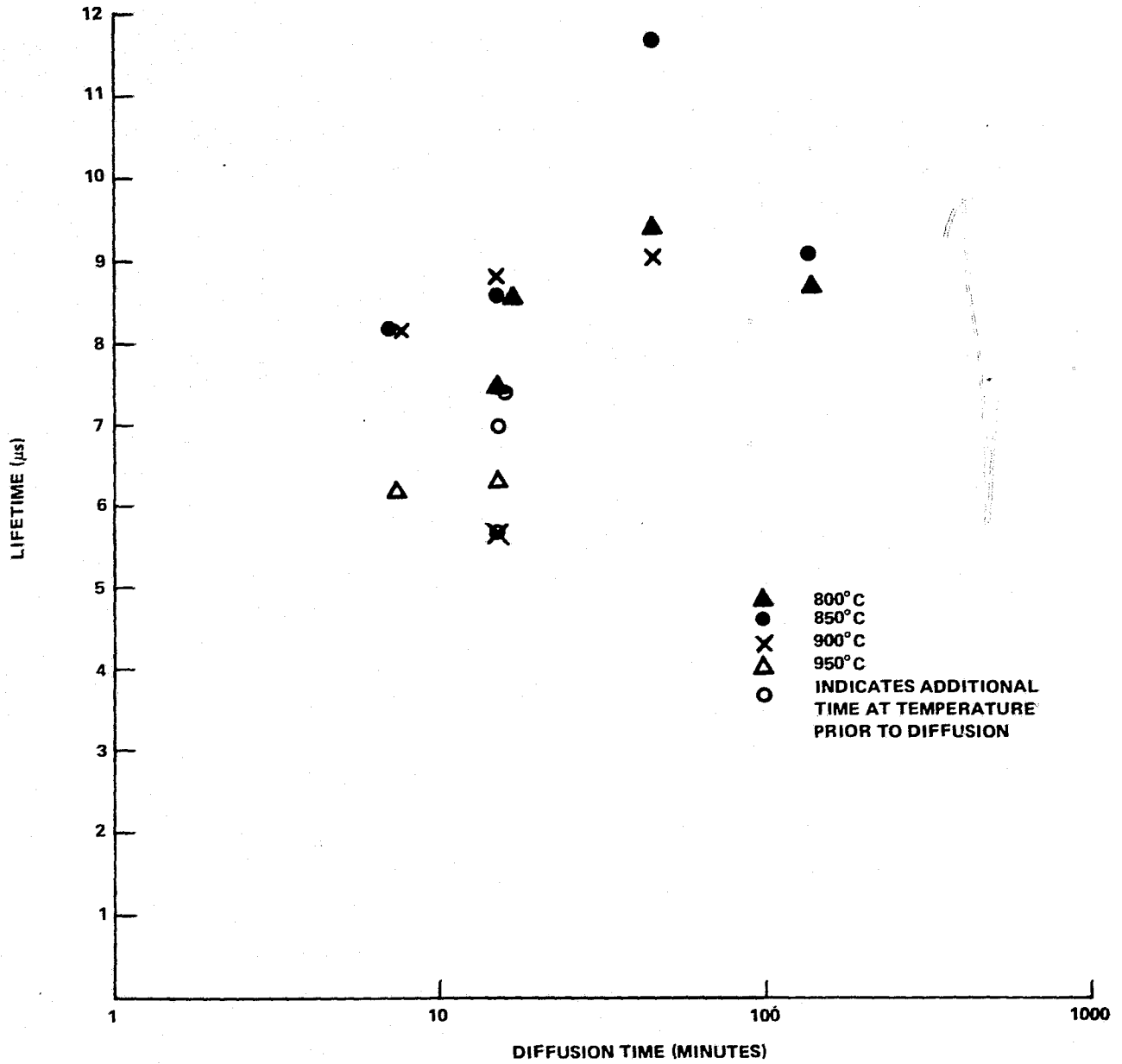


Figure 63. Base Lifetime as a Function of Diffusion Time and Temperature for Hexagonal Solar Cells

c. BASE LAYER LIFETIME

Base layer lifetime in the finished solar cell can be related to minority carrier diffusion length. Diffusion length must be sufficient to allow all carriers generated in the base material to be collected at the collecting junction. From Table 16 it is evident that carriers are generated at all depths in the solar cell, therefore effective collection length should be equal to or greater than the cell thickness. Collection lengths less than the cell thickness will result in significant loss of generated current, J_G to recombination. According to Fossum[6], typical resistivities employed in solar cell manufacture, 0.5 to 10 ohm-cm, exhibit diffusion lengths greater than or equal to cell thickness.

Control of the base layer lifetime is very complex. Many factors are involved including impurity levels in the silicon sheet material, particularly heavy metals, thermal history and defects. Relationships between these factors and base layer lifetime are not quantitatively understood. Therefore quantitative sensitivity correlations are not possible.

The impact of low base lifetime is very easy to observe however. As base lifetime falls below a critical level, J_{SC} degrades. The cause of this lowering of J_{SC} is the loss of carriers generated deep in the base of the solar cell.

Base lifetime can be monitored using the surface photo voltage technique or diode recovery techniques. For a fixed, controlled fabrication process, base lifetime should remain relatively constant. Therefore measurement of base lifetime at the end of the solar cell fabrication process should afford sufficient process control.

d. OTHER OBSERVATIONS

The above treatment assumes a relatively flat surface on the solar cell. In practice, high-efficiency solar cells will probably use textured surfaces to further reduce reflection losses. Quantitative treatment of the textured surface case is beyond the scope of this study but qualitative assessments are possible. All calculations involving depth into the cell are relative to a flat surface with normal incident solar flux. The case for a textured surface would treat the path of the absorbed light ray as the depth so that textured surface solar cells behave as though they are thicker than planar surface cells. Any nonabsorbed radiation that strikes the back of the cell can be reflected back through the cell giving a fractional increase in J_G.

Front surface recombination does not appear to be a significant factor since only $\approx$ 2% of J_G is generated in the first 10 nm. Less than 1% of the J_G is generated in the last 1 μm of a 250-μm cell so back surface recombination is even less of a factor.

M. 1982 FACTORY STUDY

A study was done to outline the requirements for a 1982 solar cell module factory with a target selling price of $2.00 per peak watt. A number of assumptions were made (or required) in this study. The key assumptions are given below:

1) Polycrystalline silicon costs $25/kg.

2) The factory will produce a single product.

3) No sales or marketing costs are incurred.

4) Delivery is at the factory.

5) Czochralski grown silicon will be used.

1. Design to Cost

The allowable costs for each major process element, silicon sheet, cell procesing, and module fabrication can be allocated, along with an allocation for profit and nonmanufacturing overhead. As discussed earlier, the cost allocations are engineering judgments and are meant as guidelines to evaluate each process element. Table 28 is the cost allocation for the $2.00 per watt factory.

Table 28. Cost Goals

	$/W
Silicon Sheet	0.60
Processing	0.35
Module Fabrication	0.40
Subtotal	1.35
Other Cost & Profit	0.65
Total	**2.00**

2. Module Design

The whole process must be designed around the design of the solar cell module. The size and shape of the silicon sheet and the cell process are integral parts of the final solar cell module. Various trade-offs must be made to arrive at the overall process. A key foundation for this study is the conclusion that high module efficiency, and consequently high cell efficiency, is a must. (The impact of module efficiency on module materials, glass and steel, is discussed later.)

High module efficiency is achieved by using high efficiency cells with high packing efficiency in the finished module. Since the module will be rectangular (interlocking irregular shapes were not considered), the highest packing efficiency can be achieved by using rectangular cells. Cz wafers are grown round and the largest rectangle that can be cut from a circle is a square. Therefore square cells were chosen. For maximum Si utilization, an oversized square is cut from the round wafers. The module is made up of any array of square wafers on a rectangular module. Either 7.62 cm or 10.16 cm diameter, Cz grown, crystals can be used.

The cell efficiency that can be forecast for a 1982 factory is 16% at AM1. This is not typical for today's manufacturing, but we feel that it is an achievable goal for high efficiency cell development within the allowable time frame.

Taking all losses into account, the 16% cell should yield a 14.6% module using square cells and a steel-glass module construction. The following analysis is based on the 1982 module.

3. Silicon Sheet

A major portion of the solar cell module manufacturing cost is related to the silicon sheet costs. Therefore, an aggressive, advanced technique was chosen to minimize the cost in this area. Two technologies that are still in development, semicontinuous crystal growth and multiblade slurry sawing, are used in the silicon sheet area. This part of the process is based on successful developments in these technologies.

Process costing for this part of the process in the 1982 factory was done for four cases. The assumptions underlying these four cases are shown in Table 29. Case I is the most conservative and Case IV is the most aggressive. The silicon sheet process flow with polycrystalline silicon at $25 per kg as the input is given in Figure 64. Also included in Figure 64 is the number of machines used at each operation and the yield at each operation for a 6×10^6 wafer per year operation.

Based on this 6×10^6 wafer per year unit, manufacturing costs were calculated for each of the four cases given in Table 29. Costs for crystal growth and del[illegible] slicing and shaping costs are given in Table 30 along with total wafer costs. The shaped wafer is a square 7.89 cm on a side (The squares have an 11.16-cm diagonal and were cut from a 10.16-cm circle, therefore each "square" is missing the four corners.), with an area of 61.27 cm^2. At an AM1 (100 mW/cm^2) efficiency of 16%, the peak output of one wafer is 0.980 watt. To convert from cost per wafer to cost per watt, divide the cost per wafer by 0.980. By comparison with Table 28, it can be seen that the manufacturing cost at this stage is very close to the design-to-cost goal.

Table 29. Silicon Sheet Cost Assumptions – 1982

CASE I

Crystal Growth	Slicing
Semicontinuous crystal puller	Slice + Kerf = 0.46 mm
3 Crystals at 84 cm each	28 cm Crystal segment sawed
Cost $200K each	Saw Cost $20K each
3 Pullers per operator	8 Saws per operator

CASE II

Crystal Growth	Slicing
Semicontinuous crystal puller	Slice + Kerf = 0.46 mm
3 Crystals at 84 cm each	42 cm Crystal segment sawed
Cost $200K each	Saw Cost $20K each
3 Pullers per operator	8 Saws per operator

CASE III

Crystal	Slicing
5 Crystals at 126 cm each	Same as Case I

CASE IV

Crystal	Slicing
5 Crystals at 126 cm each	Same as Case II

The encapsulated cell efficiency would be 14.6% AM1, giving 0.895 watt per wafer and the cost, not yielded through module fabrication, would be derived by dividing the wafer cost by 0.895.

The clean shaped wafers are taken to the cell processing area.

4. Solar Cell Processing

To achieve the target 16% cell efficiency, we propose to use an advanced cell structure, the tandem junction cell, TJC.[14] The cell processing is very similar to conventional solar cell processing with the exception of a collecting N^+ junction on the back, nonilluminated, side instead of a back surface field. Development is required to bring this solar cell structure to manufacturing readiness.

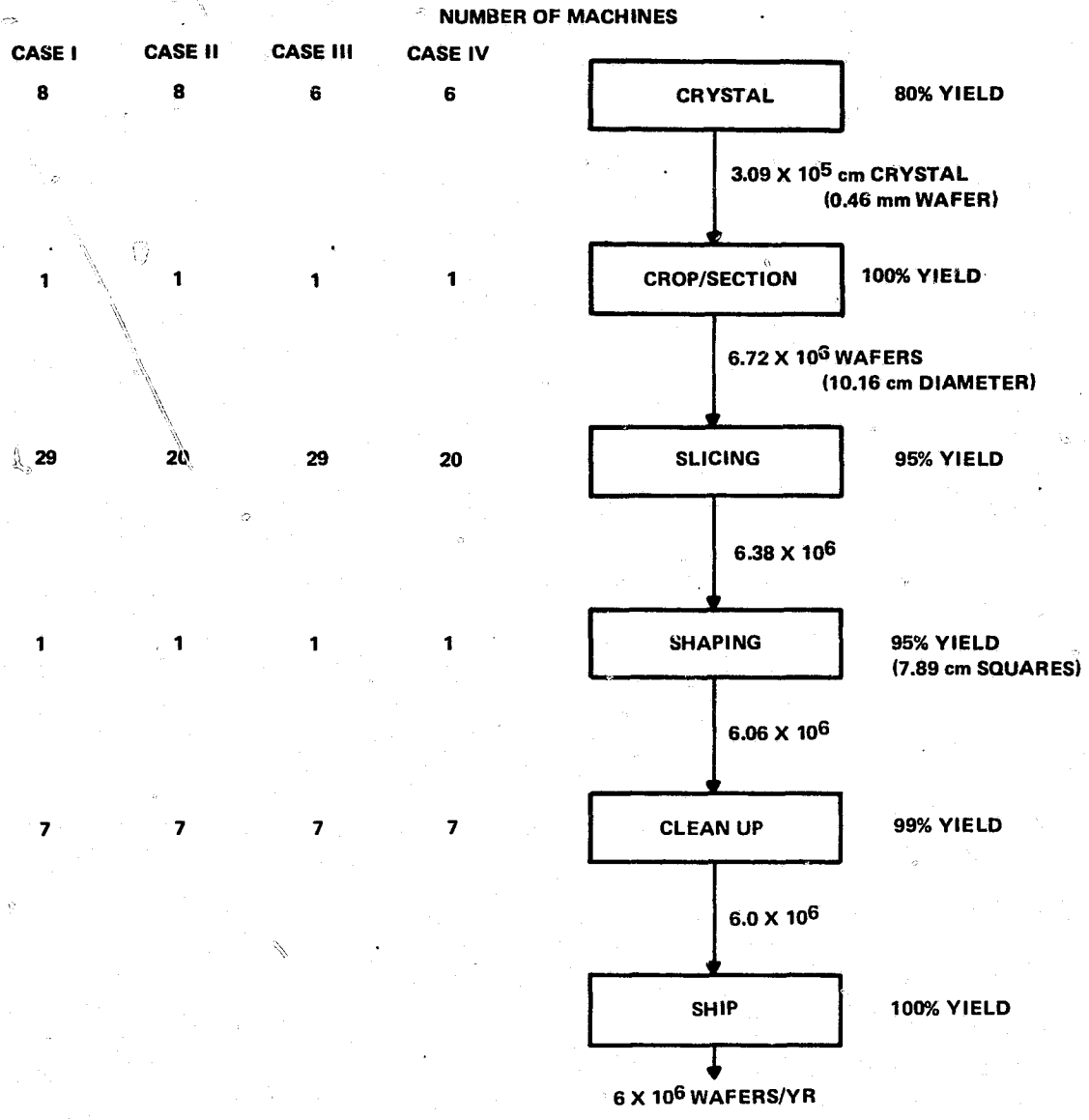


Figure 64. Silicon Sheet Process Flow – 1982 Plant

The solar cell process outline and process step costs derived from Table 15 by ratioing the efficiency (X 13.5/16) are given in Table 31 for the unencapsulated cells. Also included in Table 31 is the encapsulated efficiency step cost where the encapsulated efficiency is calculated to be 14.6% (9% loss in encapsulation). Mechanical and electrical test yields are also included. Add-on process step yielded costs are in the third column of the table. An add-on yielded cost based on the encapsulated efficiency would be $0.2155/W. By comparison with Table 28, the cell process cost appears very favorable. It must be remembered that yielded silicon sheet costs must be included. The costs in Table 31 assume a running factory and are not meant to be read as start-up costs. The process step costs were derived from earlier sections of this report. Process development is required before this process is factory ready. All process steps are in use in either the solar cell or the semiconductor industry.

Table 30. Silicon Sheet Cost Projection – 1982

	CASE I	CASE II	CASE III	CASE IV
Crystal Growth				
Furnaces	8	8	6	6
kg/wk	1092	1092	1092	1092
$/kg	49.44	49.39	42.91	42.85
Slicing				
Wafer/wk	115,385	115,385	115,385	115,385
$/Wafer	0.153	0.123	0.153	0.123
Si Sheet				
$/Wafer (Total)	0.621	0.591	0.559	0.529
Output	Square Wafer	7.89 cm on a side		

Table 31. Baseline Cell Process Cost – 1982

Process Step	Yield	16% Step Cost ($/W)	Add-On Yielded Cost ($/W)	Encapsulated Efficiency Step Cost ($/W)
Surface Preparation	0.99	0.0186	0.0188	0.0204
Spin-On As (Front)	0.99	0.0159	0.0350	0.0174
Deposit Plasma Oxide (Back)	0.99	0.0340	0.0697	0.0373
Plasma Etch (Back)	0.98	0.0183	0.0898	0.0201
Spin-On P (Back)	0.99	0.0159	0.1068	0.0174
Diffuse	0.99	0.0146	0.1226	0.0160
Open Metal Contacts (Plasma Etch, Back)	0.98	0.0183	0.1438	0.0201
Print Metal	0.98	0.0197	0.1668	0.0216
Test Cells	0.90	0.0100	0.1965	0.0110

The output of this phase of the manufacturing process is tested square cells with a textured surface (illuminated side) and a TJC structure ready for assembly into the module.

5. Module Fabrication

a. BASIC ASSUMPTION

Module size is based on JPL Drawing Number J10082854A which establishes an overall length of 47.88 inches and an overall width = 0.750 (N) –0.12 where "N" shall have an integer value from 13 to 64. A 6.16-cm cell combined with optimum spacing, border requirements and the above equation resulted in the 26.13 inch width.

Therefore, the basic assumptions used throughout this evaluation are as follows:

Module Size	26.13 inch X 47.88 inch (0.664 m X 1.215 m)
Rectangular Cell	6.16 cm
Cell Efficiency	16%
Module Efficiency	13%
Module Peak Output	105 watts
Work Day	16 hours
Work Week	6 days
Work Year	300 days

b. FORECAST OF THROUGHPUT

Tables 32 and 33 are matricies of module and selected component throughputs for a 10 MW facility with module efficiencies ranging from 10 to 16%. This data is plotted as a function of module efficiency in Figure 65.

A 10 MW annual manufacturing facility would ship 95,239 modules. Assuming an overall yield of 98.5%, 96,690 would be assembled annually.

A 19 X 10 cell matrix per module would require 18,464,580 cells assembled into 1,846,458 cell rows annually.

Table 32. Source Data for Table 33

Steel required for substrate

0.045 X 30.0 X 51.0 inches
2.5 X 4.25 feet = 10.625 ft^2
0.76 X 1.29 meters

Steel required for lockframe

0.045 X 1.5 X 162.0 inches
0.125 X 13.5 feet = 1.688 ft^2
4.115 meters

Total Steel/Module 12.3 ft^2

Pounds of Steel/Module (@2 lbs/ft^2) 24.6 lbs

Glass

Ordinary clear lime	2.51 lbs/ft^2
Water-white crystal No. 76	2.41 lbs/ft^2

Finished Module Size

26.13 X 47.88 inches
2.178 X 3.99 feet = 8.69 ft^2
0.664 X 1.216 meters = 0.807 m^2

$$\text{Module Efficiency} = \frac{\text{Module Power}}{\text{Module Area X 1000 W/m}^2}$$

A two-shift, 16-hour day, 6-day week, 300-day year would generate the following manufacturing schedule:

	Throughput per			
	Hour	**Day**	**Week**	**Month**
Cells	3,847	61,549	369,292	1,538,715
Cell Rows	384.68	6154.86	36,929.16	153,871.50
Modules	20.25	322.30	1,933.78	8,057.42

In subsequent discussion it will be shown that some of the relatively low throughputs described above will not warrant extensive capital investment. Subcontracting to outside vendors would be more economical.

Table 33. Annual Throughput for 10 Mw Facility

	Module Efficiency						
	10	11	12	13	14	15	16
Watt/Module	80.7	88.8	96.9	105.0	113.0	121.1	129.2
Modules/10 MW (shipped)	123,916.0	112,613.0	103,520.0	95,239.0	88,496.0	82,577.0	77,400.0
Modules/10 MW (98.5% Yield)	125,803.0	114,328.0	105,097.0	96,689.0	89,844.0	83,834.0	78,579.0
Steel							
Ft^2/Year	1,547,376.9	1,406,234.4	1,292,693.1	1,191,747.0	1,105,081.2	1,031,158.2	966,521.7
Lbs/Year	3,094,753.8	2,812,468.8	2,585,386.2	2,378,549.4	2,210,162.4	2,062,316.4	1,933,043.4
Glass							
Ft^2/Year	1,093,228.1	993,510.3	913,292.9	840,227.4	780,744.4	728,517.5	682,851.5
Pounds/Year							
Ordinary Clear Lime	2,744,002.5	2,493,710.9	2,292,365.2	2,108,970.8	1,959,668.3	1,828,578.8	1,713,957.3
Water-White Crystal	2,634,679.6	2,394,359.9	2,201,035.0	2,024,948.1	1,881,593.9	1,755,727.1	1,645,672.1
Modules/Week (50)	2,516.1	2,281.6	2,101.9	1,933.8	1,796.9	1,676.7	1,571.6
Modules/Day (300)	419.3	381.1	350.3	322.3	299.5	279.4	261.9
Modules/Hour (4800)	26.2	23.8	21.9	20.1	18.7	17.5	16.4
Modules/Week (50)	2,516.1	2,286.6	2,101.9	1,933.8	1,796.9	1,676.7	1,571.6
Modules/Day (250)	503.2	457.3	420.4	386.8	359.4	335.3	314.3
Modules/Hour (2000)	62.9	57.2	52.5	48.3	44.9	41.9	39.3

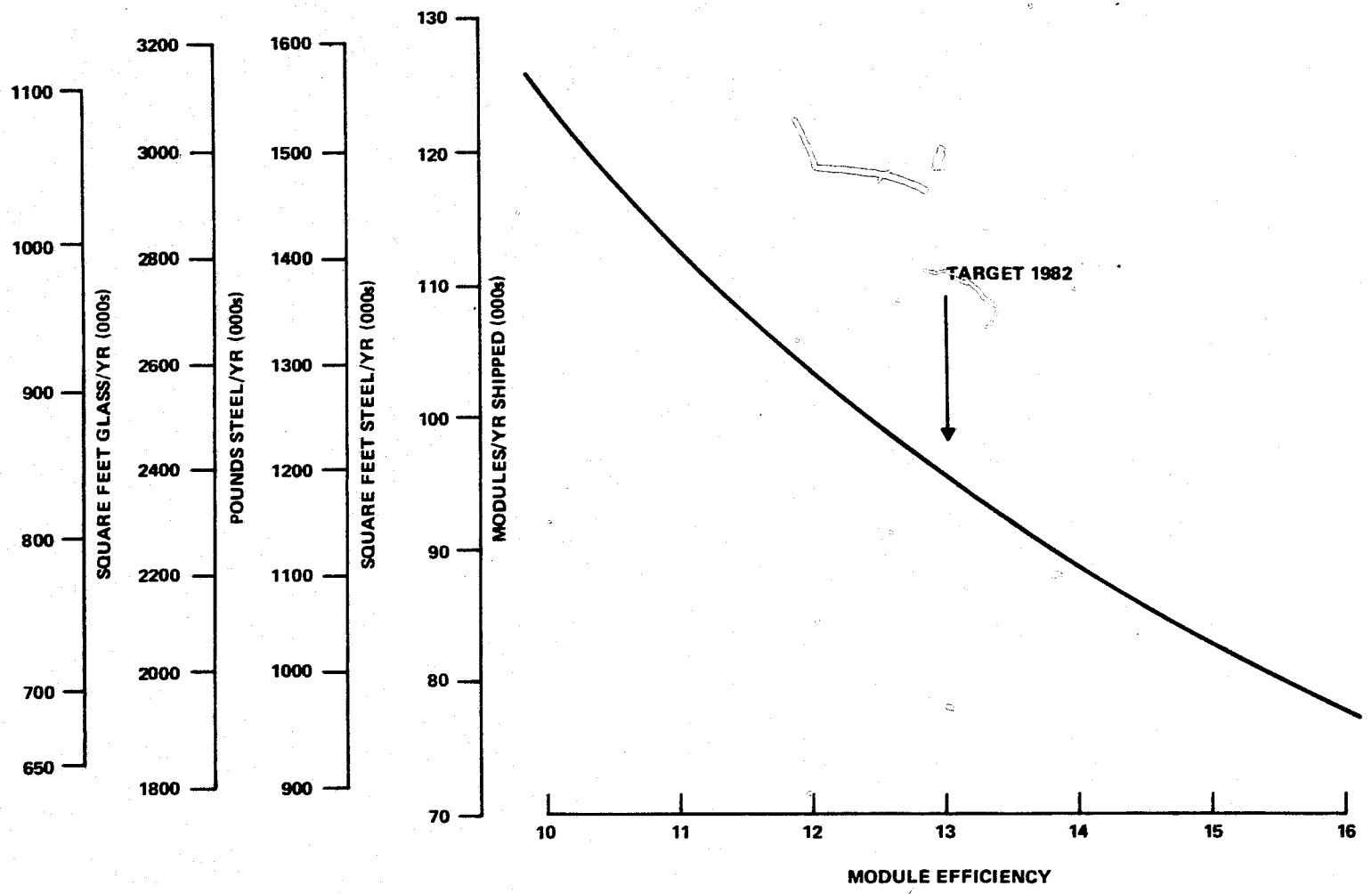


Figure 65. Material Usage of 1982 10-MW Module Facility

c. DESCRIPTION OF THE MANUFACTURING PROCESS

1. SUMMARY

Module assembly will consist of 11 separate components.

1)	Substrate – porcelainized steel	
2)	Lock Frame – porcelainized steel	
3)	Glass Cover	
4)	Silicone sealant	
5)	Silicon Cells	
6)	Front bus bar	Could also be solder clad
7)	Front solder preform	
8)	Back bus bar	Could also be solder clad
9)	Back solder preform	
10)	Adhesive	
11)	Connector lugs	

Figures 66 and 67 present the segmented process flow of all support function, and parts manufacturing, e.g., receiving inspection, metal forming, porcelainizing, and bus bar formation. Figure 68 shows the process flow of the actual assembly operation.

In the flow diagrams "circles" indicate an operation, "arrows" indicate transportation, "squares" indicate inspection, and "triangles" indicate storage.

Porcelainized steel has been chosen for the substrate and the lock frame because of its inherent strength and durability. A pinhole-free, acid resistant porcelain coating will protect the steel components for the 20-year life requirement. It has good demonstrated durability in outdoor environment, low per square meter material cost, good thermal conductivity as substrate material and the raw materials are available in large quantities. The good dielectric properties of the porcelain enamel permit direct mounting of the silicon solar cells on the substrate assuring good thermal contact and, consequently, good thermal dissipation through the substrate.

By having only one material system for all the structural parts offers definite advantages in the module assembly. Notably the same manufacturing equipment and processes can be used for all the structural components and also inventories are reduced.

Glass was selected as cover material because of its demonstrated durability against atmosphere deterioration, good availability and relatively low cost. The fragility of glass is of concern.

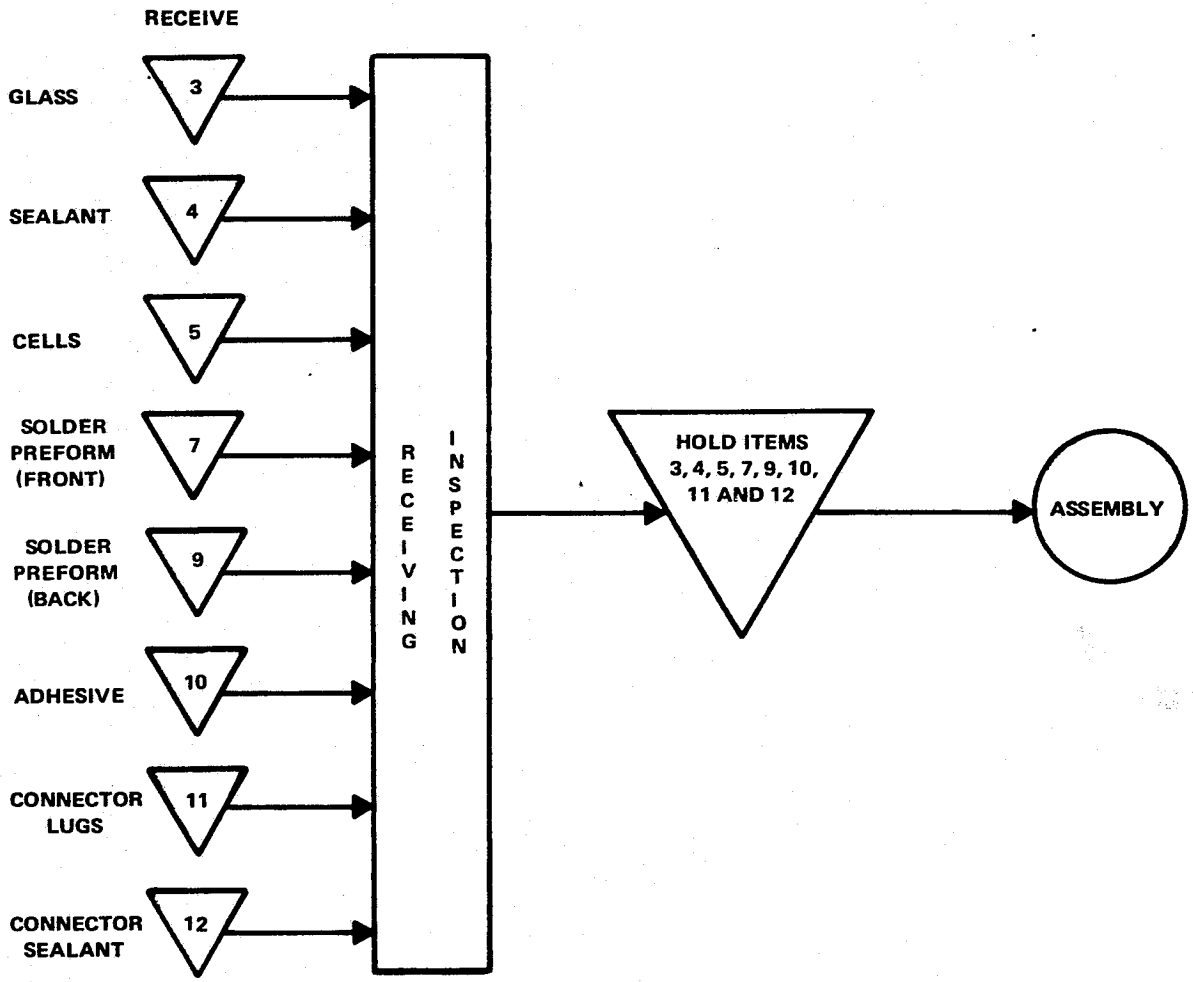


Figure 66. Segmented Process Flow – "Receiving Inspection"

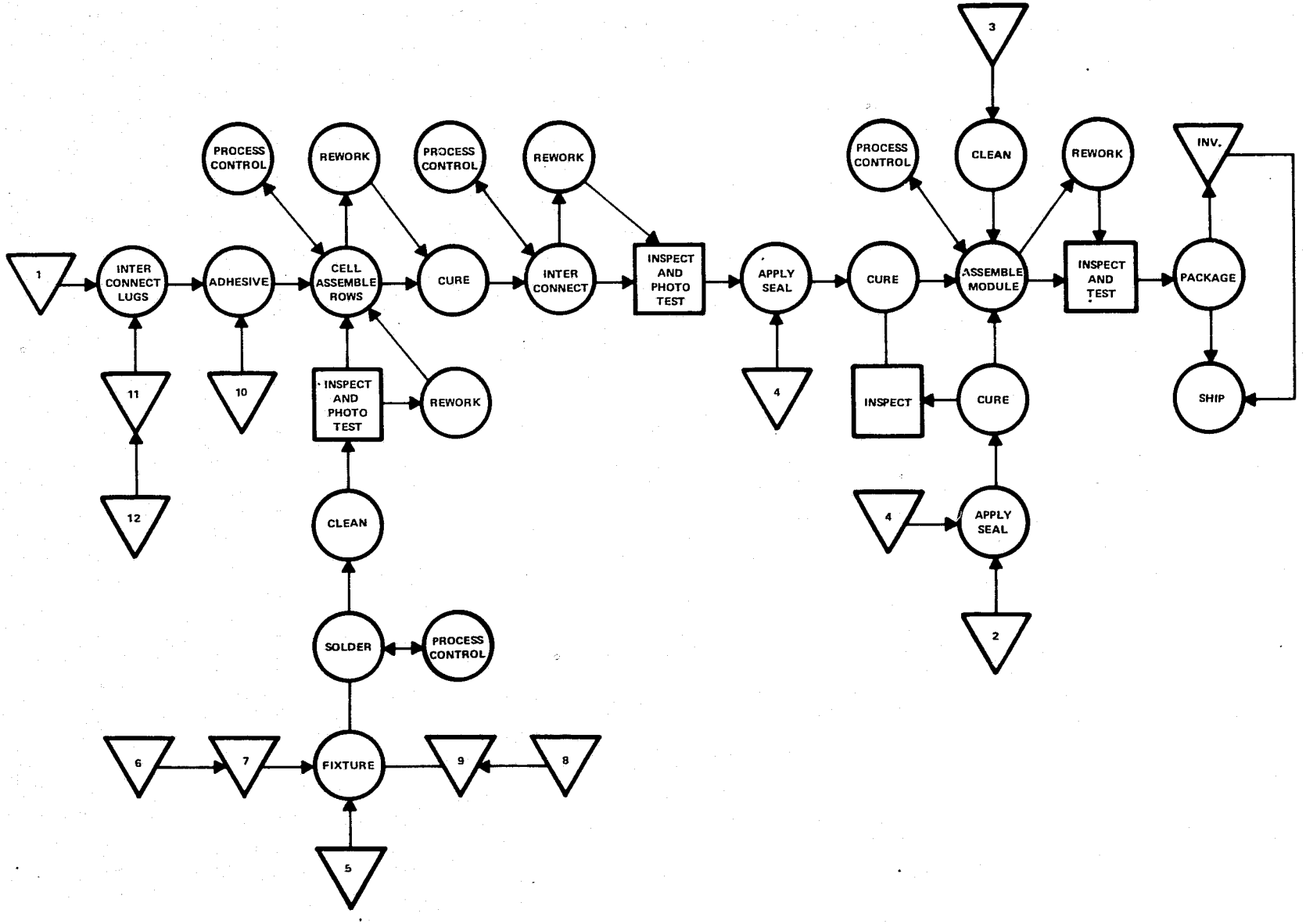


Figure 67. Segmented Process Flow — "Second Operations"

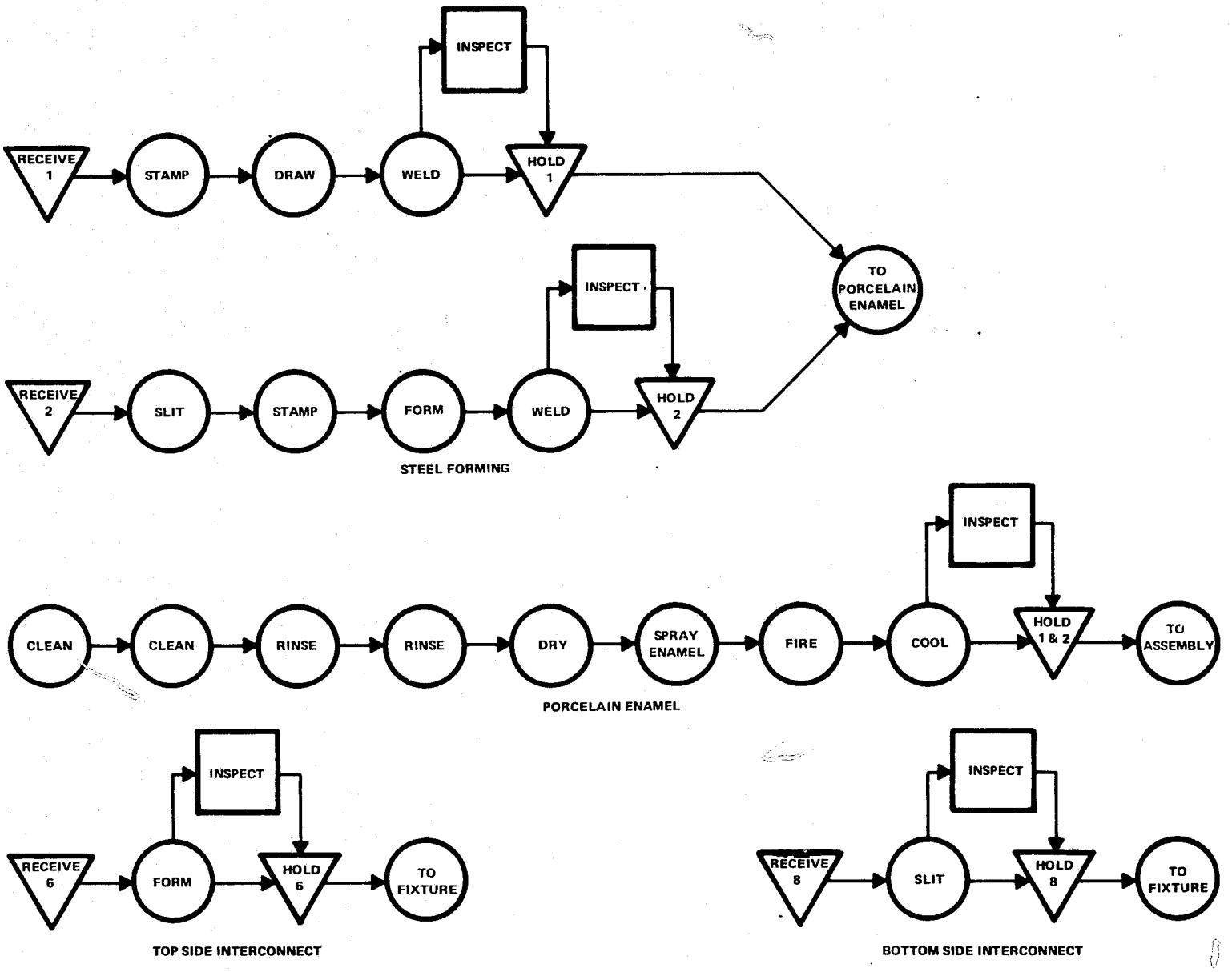


Figure 68. Segmented Process Flow – "Module Assembly"

Silicon rubber sealer strips, applied to and cured directly on the substrate and lock frame, are used to seal the collector from ambient atmosphere. Contacts through the substrate are also sealed using silicone rubber washers.

The conductors are soldered directly across the front and the back of the silicon solar cells. In both cases a good electrical conductivity is required to minimize the I^2R losses and the coefficient of thermal expansion of the conductor cannot differ too significantly from that of silicon, $\alpha_{Si} = 2.33 \times 10^{-6}$ cm/cm/°C. As an addition, conductor material should be easy to solder. None of the monolithic metals or alloys meet these requirements. However, composite metal technology can be used to manufacture material systems to meet the requirements. For this application the best choice, from the standpoint of manufacturability and cost, is copper clad Invar.

The front conductor should cause a minimum shadowing of the solar cell and offer a flat surface for soldering to the metallization pattern on the silicon solar cell. An equilateral triangle was selected because some of the incident radiation, blocked by the base of the triangular conductor can be recovered by reflection from the sides of the conductor to the cell surface.

The back conductor is also a copper clad Invar but of rectangular cross section. The conductor is tin-lead soldered to the back sides of the silicon solar cells.

2. *COMPONENTS*

a. *Substrate*

Steel for the substrate will be received in sheet form at 0.045 inch x 30 inches x 51 inches. In Figure 67 the steel for the substrate is shown at "receive" where it is inspected and then held until it is needed for the forming process. It is then transported to the stamping press and stamped to the correct dimensions for deep draw. This form includes rounded corners, holes for two Cannon plugs, holes for lock frame, and hanging holes for the porcelain enameling process. Stamping will be done on a commercially available press. Total cycle time for stamping one substrate preform is 15.4 seconds or 4.3 hours per thousand preforms. See Appendix A-1.

The preform is transported to the deep draw press, where it is drawn into a shallow box-like structure which provides unwelded corners, a boss periphery for mounting the glass cover, and recess grooves for additional support and for housing the bus bars for parallel connection of the silicon solar cells. Total cycle time for the deep drawing operation is 20.6 seconds per substrate or 7.7 hours per thousand substrates.

After deep drawing the substrate, it is transported to a welding area where separate gussets will be welded into each corner to provide additional support and to be used for mounting to a support frame. The welding cycle time is 4.39 minutes per substrate for 73.2 hours per thousand substrate. Completed substrate steel structure is transported to the porcelain enameling area. Figure 69 shows the substrate at each step of its process.

b. Lock Frame

Steel for the lock frame will be received in coil form at 0.045 inch x 24 inches wide. In Figure 67 the steel for the lock frame is shown at "receive" where it is inspected and then held until it is needed for lock frame manufacturing. The steel is transported to the slitting machine where the 24-inch wide coils weighing 9000 lbs are slit into sixteen 1-1/2 inch wide coils. The slitting of one coil will take 4 hours and requires 3 operators. Because one 9000-lb coil will yield 3000 lock frames, the labor content per thousand lock frames will be four hours. See Appendix A-2.

After slitting, the lock frame material is transported to press area where it is stamped into preform shape with corner notches and hanging holes for porcelain enameling. Subsequently each prestamped coil will be sheared into approximate lengths after corner notches and spring tabs are properly located and the strips are roll formed. Each 1-1/2 inch wide coil will yield approximately 190 lock frames and the labor content of the stamping, cutting and roll forming is 5.5 hours per thousand frames.

The stamped and form rolled strips are formed into a picture-frame-like lock frame with angled sides. The front and the back interfaces of the notched corners are welded. Forming time is 3.5 hours per thousand units and welding time is 13.3 hours per thousand units.

The frames are transported into the porcelain enameling area. Figure 70 shows the lock frame at each stage of its process.

c. Porcelain Enameling

To achieve 20-year lifetime, excellent corrosion resistance at varied environments is required. At the same time, low cost must be achieved. Of the various candidate materials considered, only steel with pinhole-free, and acid-resistant porcelain enamel surface has been demonstrated to possess the necessary durability.

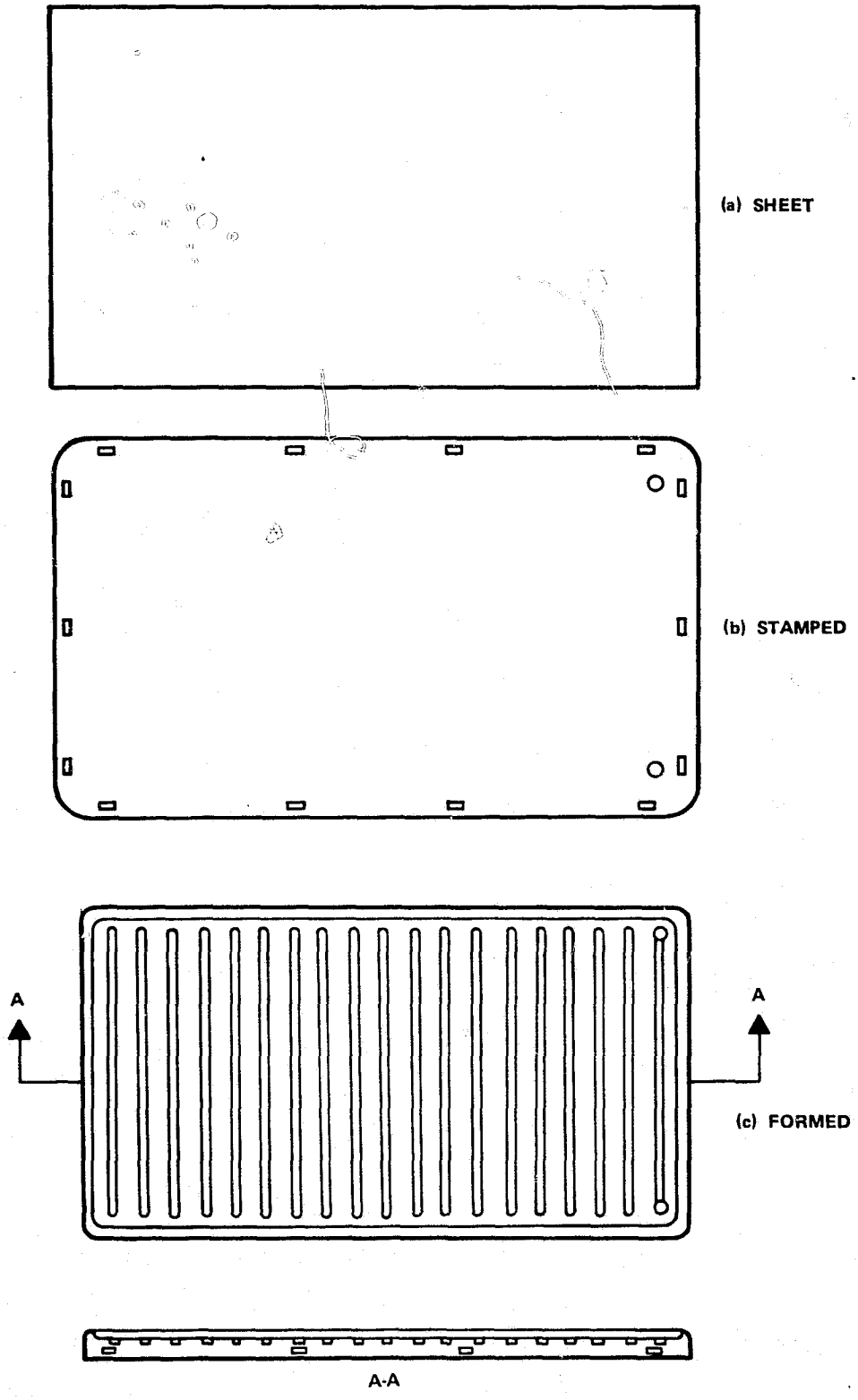
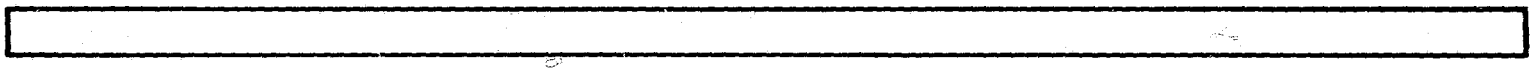
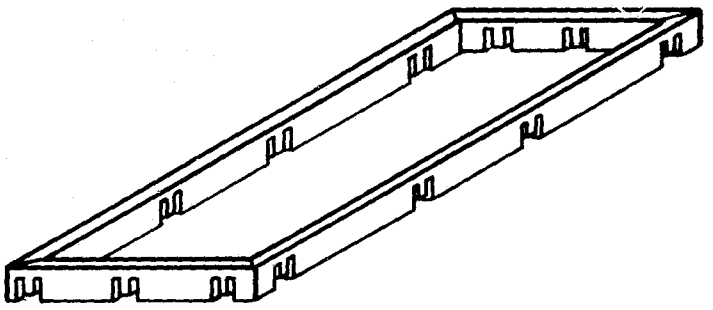


Figure 69. Substrate



(a) AS SLIT

(b) NOTCHED AND CUT TO LENGTH



(c) FORMED AND WELDED

Figure 70. Lock Frame

Both substrate and lock frame will be porcelain enameled. The porcelain enameling process consists of two cleaning operations, two rinsings, spraying of the enameling frit, firing and cooling. All the processes are in a continuous line. The residence times are 20 minutes for each of the cleaning operations, 3 minutes for each rinsing, 10 minutes for drying, 5 minutes for enamel frit spray, 4 minutes for firing and 10 minutes for cooling. The porcelain enamels, which will be used, are fused to the metal at temperatures ranging from 900°F to 1800°F to form the pinhole-free acid-resistant inorganic finish.

The enameling line start-up is approximately 1/2 hour with additional line preloading of approximately 75 minutes. Thereafter throughput will be one component per minute for 13.75 hours, followed by 1/2 hour shutdown. Assuming a 16-hour day, labor content would be 38.8 hours per thousand components, the same amount for each substrate and the lock frame. If an 8-hour day is assumed, the labor content jumps to 46.4 hours per thousand units. Reference Appendix A-3.

d. Module Cover

To achieve the required 20-year lifetime, again only glass has been demonstrated to possess the necessary durability and will be used as the module cover. The selected glass is a Water-White Crystal No. 76 (0.01% iron oxide) with the transmittance of 91%. It will be received in precut form to match the size required for the finished module.

e. Sealants

RTV Silicon Rubber will be used as the sealant. It will be applied to the periphery of the substrate and the lock frame by an automatic dispensing system.

f. Front and Back Bus Bars

Both the front and back bus bar will be manufactured from copper clad Invar to match, as nearly as possible, the coefficient of thermal expansion of the silicon solar cells. Copper clad Invar front and back side conductor stock would be purchased from an outside vendor such as Texas Instruments and formed in-house.

The front conductor, which is triangular in cross section, will be form-rolled or drawn through Turks head from copper clad Invar wire stock. The triangular bus bar is straightened and cut into length in the same operation. Subsequently they are bent and trimmed to correct length ready for cell row assembly.

The back conductor which is rectangular in cross section will be slit from a copper clad Invar strip to the proper width, straightened and cut to correct length for cell row assembly.

Depending on the manufacturing method selected, both the front and the back bus bar materials can be pretinned before soldering onto the silicon solar cells or separate solder preforms can be used in which case untinned copper clad Invar will be used for both of the conductors. Reference Appendix A-4.

g. Adhesives

Commercially available silicone adhesives will be used to attach the cell rows to the structure.

h. Connectors

Cannon connector plugs, which will be purchased from outside vendors, are used for module to module interconnection.

3. ASSEMBLY

The assembly of the solar cell module is divided into three parts: (1) Cell row assembly, (2) Cell array assembly, and (3) Module assembly.

a. Cell Row Assembly

The first assembly operation is the manufacturing of cell rows in which the silicon solar cells and the front and the back bus bars are soldered together to form cell row assembly with appropriate number of silicon solar cells. Cells, conductors, and if used, solder preforms, are positioned into a fixture which will correctly locate the silicon solar cells and the bus bars in relation to each other. They are firmly held into place for the soldering operation. For the handling of the cells air/vacuum tools are used to reduce breakage and handling costs. The cell row assemblies in the fixture are then batch processed through an HTC Phase IV vapor phase solder reflow unit (condensation soldering). After soldering, the cells rows which are left in the fixtures are inspected visually, then tested for electrical continuity and for photovoltaic performance. The accepted units, still in the fixtures are transported to the module assembly line. See Appendices A-5, A-6, and A-7.

b. Cell Array Assembly

The cell array assembly process flow, Figure 68, begins by removing a substrate from a transportation rack and placing it on the assembly conveyor. The Cannon plugs and the contact lugs are inserted into the substrate. See Appendix A-8.

The substrate is transported by the conveyor to the area where the cell row adhesive is applied to the substrate. Portion-Aire Model BV 100/115 built by Glenmarc or similar unit is used to automatically and uniformly disperse the adhesive for 19 cell rows. See Appendix A-9.

The adhesive is applied in narrow, parallel, strips about 1/4-inch wide and 0.030 apart onto the areas where silicon solar cells are bonded to the substrate. The application of adhesive in narrow strips is used to prevent the formation of closed air pockets under the silicon solar cells which could later, due to the thermal expansion of the enclosed air, cause mechanical stresses in the silicon solar cells and cell adhesive interface and possibly premature failure.

Conveyor belt will transport the substrate with applied adhesive to the solar cell array assembly station. The cell row assemblies are removed from the soldering fixture, positioned on the substrate and allowed to cure in place. See Appendix A-9.

The module is then indexed to the interconnect station. A multihead soldering unit is lowered over the cell array assembly on the substrate. Individual soldering heads are positioned on each interconnect and free-flow soldering accomplished. The interconnected silicon solar cell array on the substrate is transported to the inspection station where the terminals are contacted. A light source will illuminate the cell array and the output values are measured. Accepted arrays continue to the module assembly and defective arrays are sent to rework area. See Appendix A-10.

c. Module Assembly

The final intersection of the assembly line involves the module, the glass and the lock frame. In the first station of the final module assembly, RTV silicone rubber sealants are applied on the lock frame and on the module. For both the substrate with the solar cell array and the lock frame, Glenmarc Portion-Aire or similar equipment is used to dispense the sealant. On the module the sealant is dispensed along the top of the peripheral area, while on the lock frame, the sealant is dispensed on the inside of the front flange contacting the glass and to match the location of the sealant on substrate on the opposite side of the glass. In both cases the sealant is allowed to cure before final assembly. See Appendices A-11 and A-12.

The glass is placed onto the module sealant, the lock frame is placed on the top of the glass and the entire module assembly compressed until the lock tabs snap into place. See Appendix A-13.

Complete modules are passed through a final performance testing program prior to packaging.

Process control personnel monitor critical steps in the assembly for deviation from specification.

d. MANUFACTURING FACILITY

Manufacturing facility space requirements are outlined as follows:

Function	Area in ft^2
Receiving and Receiving Inventory	2000
Steel Forming	3000
Porcelain-Enamel	3000
Cell Row Assembly	1000
Module Assembly	3400
Finished inventory	1000
Packaging and Shipping	1000
Administration	1200
Testing and Inspection	500
Machine Shop	500
Housekeeping/Grounds	500
Total	**17,100**

Equipment requirements are outlined as follows:

Equipment	Cost
15 Ton Stamping Press	$ 30,000
75 Ton Forming Press	55,000
Slitting Line	250,000
Airco Heliarc Welder	2,000
Thompson Spot Welder	7,000
Porcelain-Enamel Line	675,000
HTC Phase IV Solderer	21,000
Turks Head	2,000
Adhesive and Sealant Dispensing Equipment (3 ea @ $2,500)	7,500
Miscellaneous Tooling, Specialty Items, Testing Equipment, and Office Furniture	250,000
Building	
17,100 ft^2 @ $40.00/$ft^2$	684.000

e. MANUFACTURING COSTS

The approach used to determine the manufacturing costs of the module is outlined as follows. Each stage in the manufacturing and assembly process has been broken down into discrete measurable steps in order to establish a base line estimate for labor hours per 1000 units. (See Appendices A-1 through A-13 and B).

The above data is then summarized in Appendix B to generate total estimated labor hours to manufacture 10 MW of modules.

The present cost of steel in sheet form is 20.55¢ /lb and in coil form is 19.5¢ /lb. The substrate weighs 21.25 pounds for a substrate cost of $4.37. The lock frame weighs 3.376 pounds for a cost of 66¢ . Water-white crystal glass cover would cost $3.84 (44¢ /$ft^2$). Twenty-five cubic centimeters of sealant would be required per module at a cost of 62¢ . One hundred cubic centimeters of adhesive, for cell row to substrate assembly would be required at a cost of $2.48 per module. There are 1.069 pounds each of triangular and rectangular bus bar required for each module at a cost of $3.82 and $3.05 respectively. Two ITT Cannon Plugs (35¢ each) are required per module for a total cost of 70¢.

The material costs are summarized as follows.

Item	Weight	Cost	$/W @ 105 W per module with 13% efficiency
Substrate	21.250	$ 4.37	$0.042
Lock Frame	3.376	0.66	0.006
Glass	20.943	3.84	0.037
Front Bus (Δ)	1.069	3.82	0.036
Back Bus (□)	1.069	3.05	0.029
Porcelain Frit	2.170	1.52	0.014
RTV Sealant	0.100	0.62	0.006
Adhesive	0.400	2.48	0.024
Connectors	0.100	0.70	0.007
Totals	**50.477**	**$21.06**	**$0.201**

Labor Costs as summarized from Appendix B are as follows.

Total Hours per 10 MW	128,199.6	
Hourly rate @ $5.00		$640,998.00
Benefits @ 17%		108,969.66
Miscellaneous Overhead @ 25%		160,249.50
Total Labor Content		**$910,217.16**
Total Dollars/Watt		**0.09**

Building and Equipment depreciation costs are summarized as follows.

Item	Total Cost	Annual Depreciation	$/Watt
Building	$ 684,000	$ 22,800	$0.002
**Equipment	1,299,500	259,900	0.026
Total	**$1,983,500**	**$282,700**	**$0.028**

*Building – 30-year straight line.

**Equipment – 10-year double declining.

Overhead costs based on 17,100 square feet are as follows.

	Annual
Occupancy @ $0.41/ft^2	$ 84,132
Electricity @ $.04/kWh	
500 kW for 4800	96,000
Lighting 1 watt/ft^2	3,284
Total Overhead	**$183,416**
Total Dollar/Watt	**$ 0.018**

Module costs can be summarized as follows.

Item	$/Watt
Module Material	0.201
Labor & Misc. Overhead	0.090
Depreciation	0.028
Factory Overhead	0.018
Total	**0.337**

f. SUMMARY

Analysis of the minimum low cost 1982 factory size is incomplete. Throughput, capital investment, and line balancing indicate that a minimum size of 25 to 30 MW/year is necessary. Throughput is low in the module assembly area and effective utilization of people and assets may dictate a buy rather than build decision for some of the module components, such as glass and porcelainized steel.

Assuming the events required for the 1982 factory take place, an overall cost projection can be made. Since none of the processing segments are defined exactly, a representative overall costing will be given.

Silicon sheet costs for the four cases cited above range from $0.699/W to $0.591/W (yielded). If we assume a typical cost of $0.65/W for the silicon sheet material, and a module fabrication cost of $0.337/W, we can calculate a yielded cumulative manufacturing cost as shown below.

	$/W
Silicon Sheet	0.65
Square Cells	1.074
Modules	1.433

The cost derived for finished module manufacturing costs compares favorably with the manufacturing subtotal in Table 28. This result encourages one to believe that the $2.00/W selling price goal in 1982 is feasible if an aggressive, goal oriented effort is made.

SECTION III
CONCLUSIONS

A number of detailed conclusions were reached during the course of this investigation. The generalized conclusions at this stage of the study are summarized in this section of the report.

1. **The design-to-cost concept** has been applied to the LSSA Project 1985 cost goal to allocate costs to the various elements in the fabrication of silicon solar cell modules. In order for the program to be 100% successful, the total manufacturing cost must be less than the selling price goal to allow a satisfactory profit margin, return on assets and cash flow. The exact differential depends on external factors, such as tax credits or government subsidies, available at the time of investment. The general principle is valid and useful even without an exact knowledge of these external factors.

2. **Solar cell and module modeling** is a useful tool in the evaluation of solar cell processes and module configurations. An understanding of the effects exerted by various device parameters on cell and module performance allows one to make more quantitative technical judgments.

3. **A new approach to solar cell metal pattern design** using minimum power losses has proven to be an extremely valuable tool in the design of optimized metallization patterns and in the evaluation of front-side metallization technologies. It has been shown that on large-area solar cells, fine-line (12-μm) definition offers very little performance advantage over coarse-line ($> 100\,\mu$m) definition. This conclusion was a significant factor in the choice of screen-printed metal for the baseline low-cost process.

4. **For rectangular solar cells,** limits can be established for maximum cell length and width. The limits are a function of allowable power loss and metal pattern configuration.

5. **For low-cost solar cell processing**, each process step must be capable of high throughput to minimize labor cost and depreciation, and materials costs must be kept to a minimum. Process steps that do not contribute in an additive fashion to the final product, such as cleaning or metal etching, should be avoided whenever possible.

6. **Metallization** is the most expensive of the cell process steps. Metallization costs are a key to cell process cost. Low cost options are screen printed metal and a patterned electroless plating technique, PIMDEP.

7. **Module fabrication** has been identified as a significant cost barrier in meeting the 1985 LSSA Project cost goal. The cost impact of the 20-year life goal is difficult to assess due to the limited data base on terrestrial operating systems. Over-design is probably required in this area. A "hermetic" module configuration has been proposed utilizing a glass superstrate and a porcelainized steel substrate.

8. **A baseline low-cost silicon solar cell process** is proposed along with two alternate versions. Two module configurations are proposed. All of the above use evolution of existing technology and do not require technology breakthroughs.

9. **This contract and other parallel contracts** under the LSSA Project have defined a number of areas that need immediate attention to maintain the thrust of the LSSA Project toward the 1985 cost and performance goals. Key areas related to Automated Array Assembly are contained in the following section of this report.

10. **Assuming silicon sheet costs** $\leq$ \$0.25 per watt and resulting cell efficiency $\geq$ 13.5% AM1, automation of existing evolving technology can drive solar cell module factory costs to $<$ \$1.00 per watt, provided a market exists to absorb the factory output.

11. **Device and parameter models** are very useful in determining the impact of process variables on cell performance.

12. **Process sensitivity analysis** shows that normal process control, typical to the semiconductor industry, is sufficient for most process steps.

13. **A selling price of \$2.00 per watt** in a 1982 factory appears feasible if a high-efficiency module (13%) can be achieved.

14. **The most efficient cell shape** for a high efficiency module is a regular rectangle. Starting with Czochralski grown silicon, a square cell is the preferred shape.

SECTION IV
RECOMMENDATIONS

The assessment of technology required to fabricate silicon solar cells for a low-cost high-volume factory leads to several key areas requiring more detailed investigation. These areas are outlined below.

A. HIGH-EFFICIENCY CELL DEVELOPMENT

All cell and module costs are directly tied to cell and module efficiency. Significant improvement in module costs can be achieved by improvements in cell efficiency. Improvements in cell structure or better control of material and cell parameters can pay major dividends in lower cost per watt. A realistic goal would be AM1 cell efficiency of 20% for a low-cost process.

B. LOW-COST PROCESS DEVELOPMENT

Some of the process steps included in the Low-Cost Baseline Process or in Alternates 1 and 2 need further development before the full process can be optimized. Individual process steps that need further development are printed metallization, photo impeded metal deposition (PIMDIP) and spin-on polymer dopant diffusion. The process step development needs to be part of an overall low-cost process development.

C. THIN-CELL DEVELOPMENT

A substantial cost savings can be achieved if the silicon sheet thickness can be reduced. The cost saving would be in the silicon sheet cost. Thin-cell development must be consistent with high cell efficiency and low-cost cell processing to achieve maximum cost benefit. Thin cells should not be developed if the cell efficiency is $<13.5\%$ AM1.

D. ALL BACK SIDE CONTACT METALLIZATION

Current solar cell technology resembles the state-of-the-art mesa diodes of the 1960 time frame with one contact on the top and the second contact on the bottom. Significant improvement in diode performance was achieved with the advent of planar diodes in the early 1960s. Similar technology applied to solar cells with the contacts on the nonilluminated back side could yield

substantial benefits in cost and performance. Module assembly would be simplified with the use of existing high-speed automatic bonding equipment, photocurrent generation would increase due to the elimination of shadowing losses and back side recombination and the surface dead layer could be reduced or eliminated. To achieve maximum benefits, so-called wraparound contacts are not acceptable, rather an entirely new structure is required. This area could yield a step function improvement in cost per watt at the module level and bring projected cost into line with design-to-cost goals.

E. LONG-LIFE MODULE DEVELOPMENT

Present solar cell modules featuring printed circuit board substrates and silicone or epoxy encapsulant do not appear to offer a high probability of achieving the 20-year life goal of the LSSA Project. A program is needed to develop and qualify a long-life module similar to the module proposed in this report.

These areas are recommended for further investigation in the immediate future as fruitful avenues of pursuit in the attainment of the LSSA Project goal.

SECTION V
REFERENCES

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SECTION VI
NEW TECHNOLOGY

The following new technology areas were disclosed during the course of this contract.

Proximity texturing is a maskless technique for texturing one side of a ⟨100⟩ Si wafer in dilute NaOH etchant while retaining a polish on the other side. The process is carried out by bringing a surface parallel to and in proximity to the ⟨100⟩ Si surface being textured. Spacings of the order of 1 mm are appropriate. When the aqueous NaOH etchant concentration is adjusted to a concentration range slightly greater than the normal range used for texture etching, the proximate surface texture etches while the reverse surface polish etches. No masking is required.

A New Solar Cell Structure called a Tandem Junction Cell (TJC) was disclosed during the period of this contract. The TJC features a collecting junction on the front and on the back of a solar cell. Additional collection from the backside increases J_{SC} by $>10\%$.

A New Solar Cell Design was generated during this contract that includes a number of test sites on the cell. These test sites can be used to perform in-line process control testing on various process steps in the solar cell process.

A Solar Cell Test Machine concept was developed during this contract. The test machine concept utilizes parallel testing of several cells at a time to achieve high-speed test rates that are compatible with low-cost automated module fabrication.

A Computer Program for Optimization of the Metal Pattern on Solar Cells was developed during this contract. The program computes optimum metal finger spacing to achieve minimum power loss and calculates the various fractional power losses for each loss factor.

APPENDIX A-1
LABOR CONTENT FOR SUBSTRATE

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
SUBSTRATE					
Stamp					
Pick up	1.8				
Turn/Load	1.8				
Position	1.8				
Hit Buttons	1.8				
Remove	1.8				
Inspect	1.8				
Stack/Rack	1.8				
Orient	1.8				
Press Cycle	1.0				
Total Cycle time	15.4		4.3	100%	4.3
Deep Draw					
Reach	1.8				
Turn/Load	1.8				
Hit Buttons	1.8				
Remove	1.8				
Inspect	1.8				
Stack/Rack	1.8				
Orient	1.8				
Press Cycle	15.0				
Total Cycle time	27.6		7.7	100%	7.7

APPENDIX A-1
LABOR CONTENT FOR SUBSTRATE (Continued)

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
Weld Gussets					
Reach Substrate	1.8				
Turn/Load	1.8				
Reach Gussets	1.8				
Pick up Four	1.8				
Turn to Load	1.8				
Position 1	1.8				
Weld 1A	30.0				
Weld 1B	30.0				
Position 2	1.8				
Weld 2A	30.0				
Weld 2B	30.0				
Position 3	1.8				
Weld 3A	30.0				
Weld 3B	30.0				
Position 4	1.8				
Weld 4A	30.0				
Weld 4B	30.0				
Remove	1.8				
Inspect	1.8				
Stack/Rack	1.8				
Orient	1.8				
Total Cycle Time	263.4		73.2	100%	73.2

APPENDIX A-2
LABOR CONTENT FOR LOCK FRAME

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
LOCK FRAME					
Slit (3000 pieces)					
Set Up		2.0			
Slitting Time		2.0			
Total Cycle Time		4.0			
Three People Required		12.0	4.0	100%	4.0
Shear to Length (190 pieces)					
Set Up		0.25			
Press Cycle					
End Form					
Corner Notch					
Total Press (15 seconds/piece)		0.80			
Total Cycle Time		1.05	5.4	100%	5.5
Form					
Pick Up Strip	1.8				
Turn to Load	1.8				
Fixture and Bend	9.0				
Total Cycle Time	12.6		3.5	100%	3.5
Weld Corners	55.0		15.3	100%	15.3

APPENDIX A-3
LABOR CONTENT FOR PORCELAIN

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
PORCELAIN					
16-Hour Day					
Line Start Up		0.50			
Line Preload		1.25			
Throughput @ 1/min.					
(825 units)		13.75			
Line Shutdown		0.50			
Multiplied by Two People					
Total Process Time (Substrate)		32.0	38.8	99.5	39.0
Total Process Time (Lock Frame)		32.0	38.8	99.5	39.0
8-Hour Day					
Line Start Up		0.50			
Line Preload		1.25			
Throughput @ 1/min.					
(345 units)		5.75			
Line Shutdown		0.50			
Multiplied by Two People					
Total Process Time (Substrate)		16.0	46.4	99.5	46.6
Total Process Time (Lock Frame)		16.0	46.4	99.5	46.6

APPENDIX A-4
LABOR CONTENT FOR BUS BAR FORMATION

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
BUS BAR					
Front (Δ)					
Set up Turks Head Run Time Straighten and cut to length			5.58	98	5.69
Load in solder basket	3.0				
Load onto wave solder	3.0		0.67	99	0.67
Unload wave solder	3.0				
Load degrease rack	3.0				
Degrease	6.0		1.67	100	1.67
BACK (▭)					
Set-up slitter and slit to width		104.0	1.08	98	1.10
Straighten and cut to length		435.0	4.50	98	4.59
Load in solder basket (5)	3.0				
Load onto wave solder	3.0				
Unload wave solder	3.0		0.67	99	0.67
Load degrease rack	3.0				
Degrease (100 Mod)	6.0		1.67	100	1.67

APPENDIX A-5
LABOR CONTENT FOR CELL ROW FIXTURING

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
BATCH					
Fixture Cell Rows					
Reach for and Position					
Back Bus	1.8				
Back Solder Pre.	2.0				
Cell No. 1	1.8				
Cell No. 2	1.8				
Cell No. 3	1.8				
Cell No. 4	1.8				
Cell No. 5	1.8				
Cell No. 6	1.8				
Cell No. 7	1.8				
Cell No. 8	1.8				
Cell No. 9	1.8				
Cell No. 10	1.8				
Front Solder Preforms	1.8				
Front Bus	1.8				
Secure Fixture	1.8				
Remove Loaded Fixture	1.8				
Turn to Solder Rack	1.8				
Load into Solder Rack	1.8				
Turn to and pick up					
New Fixture	1.8				
Orient	1.8				
Position New Fixture	1.8				
Total Cycle Time	38.0		10.6	98%	10.8

APPENDIX A-6
LABOR CONTENT FOR CELL ROW SOLDERING (BATCH)

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
BATCH					
Solder (15 Rows/Cy)					
Raise Solder Rack with Hoist	10.0				
Rotate Rack over Solder Unit	5.0				
Hit Button	1.8				
Rack Lowers	60.0				
Residence Time in Solder Unit	0.0				
Raise Rack from Solder Unit	60.0				
Rotate Solder Rack to Unload Area	5.0				
Lower Solder Rack	10.0				
Unload Solder Rack	10.0				
Place Rack in Holding Area	2.0				
Rotate Hoist to New Solder Rack	5.0				
Total Cycle Time	168.8				
Cycle Time per Row	11.2		3.1	98%	3.2

APPENDIX A-7
LABOR CONTENT FOR CELL ROW SOLDERING (CONTINUOUS)

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Automatic					
Solder					
Turn to Transfer Rack	1.8				
Remove Cell Row	1.8				
Turn to solder Conveyor	1.8				
Load onto Solder Conveyor	1.8				
Unload from Solder Conveyor	1.8				
Turn to Finish Rack	1.8				
Load onto Finish Rack	1.8				
Reorientate	1.8				
Total Cycle Time	14.4		4.0	98%	4.1

APPENDIX A-8
LABOR CONTENT FOR CONNECTOR LUGS

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Assemble Contact Lugs					
Turn to Supply Bins	1.8				
Reach for Lugs	1.8				
Reorient	1.8				
Set Lug No. 2	5.0				
Set Lug No. 2	5.0				
Turn to Supply Bin	1.8				
Reach for Cannon Lugs	1.8				
Reorient	1.8				
Set Pigtail No. 1	5.0				
Set Pigtail No. 2	5.0				
Release Substrate	1.8				
Index New Substrate	3.0				
Total Cycle Time	35.6		9.9	100%	9.9

APPENDIX A-9
LABOR CONTENT FOR CELL ROW ADHESIVE AND CELL ROW ASSEMBLY

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Assemble Cell Rows					
Apply Adhesive					
Reach for Substrate	1.8				
Turn to Load	1.8				
Load in Work Area	1.8				
Hit Buttons	1.8				
Dispense Cycle	15.0			Multihead Auto	
Reorient	1.8				
Total Cycle Time	24.0		6.7	100%	6.7
Apply Cell Rows					
Turn to Solder Rack	1.8				
Pick up Cell Row	1.8				
Turn to Substrate	1.8				
Place onto Substrate	1.8				
Position Cell Row	1.8				
Cycle Time/Cell Row	9.0				
Cycle Time/Module Equals 9.0 Times 19 Rows	171.0				
Release Module to Conveyor	1.8				
Total Cycle Time	172.8		48.0	99%	48.5

APPENDIX A-10
LABOR CONTENT FOR CELL ROW INTERCONNECT

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Interconnect Cell Rows					
Turn to substrate	1.8				
Reach	1.8				
Move/Position	3.0				
Hit Buttons	1.8				
Solder Cycle	5.0				
Inspect Cycle	5.0				
Release	1.8				
Reorient	1.8				
Total Cycle Time	22.0		6.1	99.5%	6.1

APPENDIX A-11
LABOR CONTENT FOR SUBSTRATE SEALANT

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Apply Sealant (1)					
Pick up Substrate	1.8				
Turn to Position	3.0				
Position and Lock	3.0				
Apply Sealant (Auto.)	41.8				
Remove Substrate	2.0				
Turn to Cure Rack	2.0				
Load on Cure Rack	2.0				
Reorient	1.8				
Total Cycle	57.4		15.9	100%	15.9
Cure					

APPENDIX A-12
LABOR CONTENT FOR LOCK FRAME SEALANT

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Apply Sealant (2)					
Turn to Lock Frames	1.8				
Reach for L. F.	1.8				
Reorient	3.0				
Position L. F.	1.8				
Hit Buttons	1.8				
Apply Sealant (Auto)	40.0				
Remove L. F.	1.8				
Turn to Cure Rack	1.8				
Load on Cure Rack	1.8				
Reorient	1.8				
Total Cycle Time	57.4		15.9	100%	15.9

APPENDIX A-13
LABOR CONTENT FOR MODULE ASSEMBLY

	Time in Seconds	Time in Hours	Estimated Hrs/1000	Yield	Actual Hrs/1000
ASSEMBLY					
Module					
Turn to Substrate	1.8				
Reach	1.8				
Index (Position)	3.0				
Turn to Glass	1.8				
Reach for Glass	1.8				
Reorient	1.8				
Position Glass	1.8				
Turn to L. F.	1.8				
Reach for L. F.	1.8				
Reorient	1.8				
Position L. F.	1.8				
Press Together (Auto)	10.0				
Release Module	1.8				
Load on Transfer Rack	3.0				
Reorient	1.8				
Total Cycle Time	37.6		10.4	98%	10.6

APPENDIX B
SUMMARIZED LABOR CONTENT FROM APPENDICES A-1 THRU A-13

Operation	Hrs/1000 Modules	Hrs/10 Mw
Stamp (1 person)	4.30	415.8
Draw (1)	7.70	744.5
Weld Substrate (1)	73.20	7077.6
Slit (3 people)	4.00	386.8
Shear (1)	5.50	531.8
Form (1)	3.50	338.4
Weld Lock Frame (1)	15.30	1479.3
Porcelain (2 people)	78.00	7541.7
Bus Bar Formation (front)	5.58	539.5
	0.67	64.8
	1.67	161.5
(back)	1.08	104.4
	4.50	435.1
	0.67	64.8
	1.67	161.5
Contact Lugs	9.9	957.2
Fixture Cell Rows (1)	201.4	19473.2
Solder Cell Rows (1)	58.9	5695.0
Assemble Cell Rows		
Adhesive (1)	6.7	647.8
Cell Rows (1)	48.5	4689.4
Cell Row Interconnect (1)	6.1	589.8
Substrate Sealant (1)	15.9	1537.4
Lock Frame Sealant (1)	15.9	1537.4
Module Assembly (1)	10.6	1024.9

APPENDIX B (Continued)

Operation	Hrs/10 Mw
Superintendent	4800.0
Forman	
Assembly	4800.0
Services	4800.0
Engineering (2)	9600.0
Quality Control (3)	14400.0
Purchasing, etc.	4800.0
Set Up Man	4800.0
Toolmaker	4800.0
Machinist	4800.0
Secretary	4800.0
Control Analyst	4800.0
Accounting Clerk	4800.0
Total Labor Hours	128,199.6