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A Quick Response Four Decade Logarithmic High-Voltage Stepping Supply

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A QUICK RESPONSE FOUR DECADE LOGARITHMIC HIGH-VOLTAGE STEPPING SUPPLY

Henry Doong
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ABSTRACT

This document describes an improved high-voltage stepping supply, Reference 1, for space instrumentation where low power consumption and fast settling time between steps are required. The supply was designed to drive the electrostatic analyzers in the High and Low Altitude Plasma Experiments aboard the Dynamic Explorers which are scheduled for launch in 1980.

The high-voltage stepping supply, utilizing an average power of 750 milliwatts, delivers a pair of mirror images with 64 level logarithmic outputs. It covers a four decade range of ±2500 to ±0.29 volts having an output stability of ±0.5 percent or ±20 millivolts for all line load and temperature variations. The supply provides a typical step settling time of 1 millisecond with 100 microseconds for the lower two decades.

The versatile design features of the high-voltage stepping supply provides a quick response staircase generator as described or a fixed voltage with the option to change levels as required over large dynamic ranges without circuit modifications. The concept can be implemented up to ±5000 volts. With these design features, the high-voltage stepping supply should find numerous applications where charged particle detection, electro-optical systems, and high voltage scientific instruments are used.

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TM 79547

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INTRODUCTION

The design of low power, high voltage supplies usually consists of an amplitude modulated high frequency tuned oscillator in conjunction with a voltage multiplier and filter to raise the available voltage to the desired output level. This type of circuit arrangement does not meet the design goals when a fast response time is required as the output voltage response time is prolonged by the time constant associated with the voltage multiplier-filter capacitor and load. To compensate for the fast response time, either or both the capacitor value and the load resistance must be reduced, but a reduction in resistance leads to a large increase in input power while a smaller capacitor value results in a large ripple voltage; or if operated at higher frequencies, the ripple voltage improves but the efficiency is reduced. To minimize the response time without increasing the input power or output ripple voltage, the high-voltage stepping supply uses an active high-voltage shunt regulator at the high-voltage output.

To meet the design goals of the four decade dynamic range, two innovative circuits are used. One circuit uses the 6 bit to 32 step decoder which requires only 12 scaling resistors rather than the 32 in a conventional design. The other circuit has two complementary amplifier channels with each channel producing one-half of the 64 step staircase waveform; each channel is "gated" on at the appropriate time to produce a complete staircase voltage at the output.

The high-voltage stepping supply is equipped with a self contained low voltage source for the internal circuits, an overload and over voltage protection circuit, and two output voltage monitor circuits. The supply, including the supply housing, weighs 1-1/2 pounds and occupies a volume of approximately 63-cubic inches.

SYSTEM DESCRIPTION

The stepping supply functional block diagram, Figure 1, consists of the following units.

- 6 bit to 32 step logarithmic staircase generator (two consecutive 32 steps per cycle)
- Reference voltage source
- Signal processor
- Oscillator, modulator, and parallel charge multipliers
- High voltage dc shunt regulators

OPERATION

SIX BIT TO 32 STEP LOGARITHMIC STAIRCASE GENERATOR

The 6 bit to 32-step logarithmic staircase generator, Figure 2, accepts the 6 bit binary input commands at the basic clock rate of 64 steps per second (15.6 ms step dwell time). Each bit is passed through a buffer stage (Q_1 thru Q_6) and an inverter logic IC-1 (CD4049A). The three most significant bits (MSB) interface with the multiplexer IC-2 (CD4051A). The other three least significant bits (LSB) are level shifted by Q_7, Q_8 and Q_9. Thus for the LSB, a logic "1" is zero volt and a logic "0" is -10 volts. The level shifters are necessary to interface with the multiplexer IC-3 (CD4051A) as the switches are connected to the negative potential.

The two multiplexers, IC-2 and IC-3, combined with amplifier A_1 and the 12 resistor matrix, constitute a multigain summing amplifier, with resistors R_f as the feedback resistor and R_{in} as the input resistor. Each switch in the multiplexers is selectively turned on by the 6 bit input code. Thus for any step, the amplifier A_1 output voltage E_1 can be written as:

$$E_1 = \frac{R_f}{R_{in}} = (V_r). \tag{1}$$

Where:

E_1 = the output voltage of A_1

R_f = feedback resistance selected by LSB code

R_{in} = input resistance selected by MSB code

V_r = reference voltage, 7.50 volts

The circuitry provides 32 logarithmically scaled voltage levels at the output E_1. Each level is determined by two discrete switch closures. The MSB code closes a discrete switch in IC-2 and the LSB code closes another discrete switch in IC-3. Accordingly, one scaling resistor of four is chosen for R_{in} and one scaling resistor of eight is chosen for R_f. The total number of combinations available is 32. Since the basic clock rate is 64 steps per second, the logarithmic staircase will be generated twice per second. The resistive scale factors are chosen to cover two decades of voltage over the 32 levels. Table 1 shows amplifier A_1 output E_1 vs input command code and the corresponding scaling resistors.

Table 1
Six Bit to 32 Step Voltage levels and Scaling Resistors Versus Command Code

No.	Code*	E_1	R_{in}	R_f	No.	Code*	E_1	R_{in}	R_f
1	X00000	-7.500	100K	100K°	17	X10000	-0.7500	1M	100K
2°	X00001	-6.495	100K	86.6K	18	X10001	-0.6495	1M	86.6K
3	X00010	-5.625	100K	75.0K	19	X10010	-0.5625	1M	75.0K
4	X00011	-4.872	100K	64.9K	20	X10011	-0.4872	1M	64.9K
5	X00100	-4.218	100K	56.2K	21	X10100	-0.4218	1M	56.2K
6	X00101	-3.654	100K	48.7K	22	X10101	-0.3654	1M	48.7K
7	X00110	-3.165	100K	42.2K	23	X10110	-0.3165	1M	42.2K
8	X00111	-2.739	100K	36.5K	24	X10111	-0.2739	1M	36.5K
9	X01000	-2.374	316K	100K	25	X11000	-0.2374	3.16M	100K
10	X01001	-2.056	316K	86.6K	26	X11001	-0.2056	3.16M	86.6K
11	X01010	-1.781	316K	75.0K	27	X11010	-0.1781	3.16M	75.0K
12	X01011	-1.542	316K	64.9K	28	X11011	-0.1542	3.16M	64.9K
13	X01100	-1.336	316K	56.2K	29	X11100	-0.1336	3.16M	56.2K
14	X01101	-1.157	316K	48.7K	30	X11101	-0.1157	3.16M	48.7K
15	X01110	-1.002	316K	42.2K	31	X11110	-0.1002	3.16M	42.2K
16	X01111	-0.8679	316K	36.5K	32	X11111	-0.0868	3.16M	36.5K

*"X" denotes a "don't care bit."

REFERENCE VOLTAGE SOURCE

The reference voltage V_r, Figure 2, for the staircase generator is obtained from two stable 6.8 volts, temperature-compensated zener diodes, D_1 and D_2. The field effect transistor FET (Q_{10}) is employed to furnish a constant current source to the two diodes. Resistors R_1 and R_2 scale the zener voltage to exactly 7.50 volts. Amplifier A_2 serves as the buffer for the low source impedance to the load.

SIGNAL PROCESSOR

The signal processor, Figure 3, has four basic functions.

1. to condition staircase waveform E_1 so that the proper polarity and format sequence are provided at V_p and V_n
2. to amplify and deliver a pair of mirror image staircase voltages at +LV and -LV
3. to compensate for the temperature and tracking error of each mirror image voltage
4. to alternately select each of the two amplifier channel voltages which produce $+V_o$ and $-V_o$ outputs.

As shown in Figures 2 and 3, the 32 level staircase E_1 waveform is applied to each of the two sets of amplifiers. One set, consists of two inverting unity gain amplifiers A_1 and A_2. When the 2^5 bit logic is "Zero," amplifiers A_1 and A_2 produce a pair of mirror image staircase voltages V_p and V_n, refer to Figure 4, to set the highest two decade voltage outputs in the first half cycle of the total staircase waveform. However, when the 2^5 bit logic is "One" during the second half cycle of the total staircase waveform, the voltage E_1 is blocked from going through the amplifiers. The voltage at V_p becomes slightly positive while the voltage at V_n becomes slightly negative.

V_p is used to dynamically control the positive shunt regulator to provide the regulation output $+V_o$ during this half cycle (steps 1-32). V_p is also compared with the feedback voltage from the multiplier stack output +HV. The difference is the error voltage and is amplified to control the +HV level via the modulator.

V_n, the mirror image of V_r, controls the negative shunt regulator output $-V_o$ during the same first half cycle to provide the regulated output $-V_o$.

The second amplifier set is used to provide the logarithmically scaled voltage levels during the second half cycle (step 33-64). It consists of amplifier A_3 (gain = -3.33) and amplifier A_4 (gain = -1) and a temperature compensation network R_1 - D_1, refer to Figure 3.

The staircase outputs, +LV from amplifier A_3 and the mirror image -LV from amplifier A_4, refer to Figure 4, are used directly as outputs $+V_o$ and $-V_o$ respectively during the second half cycle, (steps 33-64). Actually these outputs are connected to $+V_o$ and $-V_o$ by means of the high voltage steering diodes, D_{10} and D_{20}, refer to Figure 6. During the first half cycle (steps 1-32), when the highest two decades of output levels are regulated by the high voltage shunt regulators, both of these diodes (D_{10} and D_{20}) are reverse biased since $\pm$LV outputs never exceed $\pm V_o$.

During the second half cycle, the slight positive voltage on V_p is sufficient to cut off the parallel charge multipliers; therefore no voltage is generated at either +HV or -HV output terminals. This allows the two steering diodes D_{10} and D_{20} in Figure 6 to conduct, providing the lower two decade outputs to $+V_o$ and $-V_o$. The voltage drop across each diode is compensated by an equal offset diode (D_1) voltage (V_d) to the amplifier A_3 input in Figure 3. Diode D_1 is similar to the steering diodes, and resistor R_1 provides the necessary compensating current.

The equations for defining the outputs: V_p, V_n +LV and -LV in Figure 3 are:

First half cycle (steps 1-32)

$$V_p = (-1)\ (-1)\ E_1 = E_1 \tag{2}$$

$$V_n = (-1)\ E_1 \tag{3}$$

$$+LV = (-3.33)\ E_1 + (-1)\ (V_d) \tag{4}$$

$$-LV = (-1)\ (+LV) \tag{5}$$

Second half cycle (steps 33-64)

$$V_p = (-1)\ (-1)\ (\text{"1"}) = \text{positive voltage greater than 1 volt} \tag{6}$$

$$V_n = (-1)\ (\text{"1"}) = \text{negative voltage greater than 1 volt} \tag{7}$$

$$+LV = (-3.33)\ E_1 + (-1)\ (V_d) \tag{8}$$

$$-LV = (-1)\ (+LV) \tag{9}$$

Notes:

E_1 and V_d are always negative

("1") denotes 2^5 bit logic "One". It is always greater than E_1 in magnitude and positive.

Using -7.5 volts as the maximum voltage for E_1 (steps 1 or 33), the following voltages yield.

First half-cycle, step 1

(From eq. 2) V_p = -7.5 volts

(From eq. 3) V_n = +7.5 volts

(From eq. 4) +LV = 25 + 3 = 28 volts (assume V_d = -3 volts)

(From eq. 5) -LV = -28 volts

Second half-cycle, step 33

(From eq. 6) V_p = positive voltage greater than 1 volt

(From eq. 7) V_n = negative voltage greater than 1 volt

(From eq. 8) +LV = 25 + 3 = 28 volts (assume V_d = -3 volts)

(From eq. 9) -LV = -28 volts

OSCILLATOR

The 60 Khz sinewave oscillator, Figure 5, consists of transistors Q_1 and Q_2, inductor L_1, and transformer T_1, refer to Reference 2. The operating frequency is determined by the secondary inductance and shunt capacitance C_1. Inductor L_1 keeps the current through it fairly constant at all times, reducing sharp current spikes when the transistor is turned on and minimizing conducted radiated EMI to nearby circuits.

The peak primary voltage ($\pi/2$ times V_{cc}) is 57 percent higher than the standard Hartley or Colpitts oscillators. When V_{cc} equals 24 volts and the transformer T_1 step-up ratio is 3, the secondary peak output voltage of 226 volts is realized.

MODULATOR

The diode modulator is a full wave diode bridge (D_1 thru D_4), Figure 5. The bridge circuit is connected in series with transformer T_2 primary, with transistors Q_3 and Q_4 acting as the variable load across the bridge arms. Transistors Q_3 and Q_4 are in parallel to share the worst case load dissipation condition.

The oscillator output from the step up T_1 secondary winding is divided between the load and transformer T_2. The voltage across the secondary winding is again stepped up to produce about 1 kV peak-to-peak. Transformer T_2 is tuned to the same frequency as the oscillator frequency with capacitor C_2 so the minimum reactive load is reflected to the oscillator and modulator circuitry.

PARALLEL CHARGE MULTIPLIERS

The relatively high ac voltage (approx. 1000 Vpp) from transformer T_2 secondary is fed into two sets of multiplier stacks, Figure 5. One set generates a positive high-voltage staircase at +HV and the other set produces a negative-high voltage staircase at -HV. Each stack, composed of 6 diodes and 6 capacitors, is connected in a parallel-charge configuration rather than in a series-charge configuration as in the Cockcraft-Walton multiplier.

The parallel-charge configuration is more efficient when several voltage multiplier stages are used. The trade-off is the a.c. capacitor peak inverse voltage must be N-times larger in the N-th stage of the multiplier.

The positive high-voltage +HV and negative high-voltage -HV are the result of the rectified multiplier stack voltages. Their magnitude is dictated by the inputs to the summing amplifier A_1, Figure 5, namely the staircase waveform V_p and the fixed offset voltage. As each step advances, the staircase waveform at V_p immediately introduces an error signal to the amplifier A_1 input. The amplified error signal drives the base terminal of the two parallel transistors, Q_3 and Q_4, connected across the diode bridge. This drive signal determines the available collector to emitter resistance across the diode bridge. Since the oscillator signal is shared between the diode bridge and the primary winding of transformer T_2 only that portion across T_2 is stepped up and multiplied. The multiplier output voltage +HV adjusts accordingly until the feedback current through resistor R_f cancels the error signal that has been generated by the V_p staircase waveform.

Thus, summing amplifier A_1 combined with the diode modulator and the parallel charge multiplier, Figure 5, may be considered as an operational amplifier with a gain equal to:

$$+HV = -V_p \frac{R_f}{R_{in}} + (V_s) \frac{R_f}{R_b} \tag{10}$$

where

R_f = 110 M

R_{in} = 301 K

R_b = 3.3 M (offset input resistance)

V_s = 3 volts (offset voltage)

Therefore $+HV = -365.4\ V_p + 100$

As mentioned earlier V_p in step 1 is -7.50 volts, substituting this voltage in equation 10 yields +HV equal to 2840 volts. This is the maximum voltage developed at +HV, with the same negative voltage occurring simultaneously at the -HV terminal.

Normally, the +HV and -HV outputs can be used as the final output voltage for the external load if the step time is at least several times larger than the transient time. The transient time is the rise or fall time of the RC time constant of the multiplier stack used and is typically about 20 milliseconds. When the step time is small, as in this application (15.6 ms/step), several alternatives can be used to meet the requirement, for example.

Reduce the Load Resistance

Assuming that the equivalent capacitance of the multiplier stack is 1000pF, to obtain a time constant of 1 millisecond a 10^6 ohm resistor must be used from the +HV output to ground. The 10^6 ohm resistor will dissipate 6.25 watts of power at +HV when the +HV equals 2500 volts. A similar resistor must be used between the -HV output and ground which dissipates an additional 6.25 watts.

Decrease the Multiplier Capacitance

Assuming the load resistance is 10^8 ohms, to keep the power dissipation to a reasonable level for the same time constant of 1 millisecond it would require the equivalent capacitance on the multiplier to be no larger than 10 pF. A multiplier stack with such small capacitors in the chain would be inefficient with a large ripple voltage that may exceed the magnitude of the step voltage itself. Although the ripple voltage may be reduced if the oscillator frequency is near one MHz, but operating at this frequency would create many new problems such as: diode leakage in the multiplier, RF shielding, and excessive core loss in the transformer, etc.

Add an Active Circuit to the Load

By adding a dynamic dc shunt regulator to the load, the low resistance shunt would discharge the excessive charge during transition times but then would act as a very high resistance during the steady state condition. This shunt regulator is described in the following section.

HIGH-VOLTAGE DC SHUNT REGULATOR

The use of two shunt regulators, one to regulate the positive voltage output from +HV and the other to regulate the negative voltage output from -HV, are coupled through isolation resistors R_d as shown in Figure 6. The resistors allow the regulated outputs $+V_o$ and $-V_o$ to track the input waveform V_p faithfully with a fixed gain; Figure 7 shows the improvements to these waveforms. The transition time between steps of the +HV waveform is measured to be about 20 milliseconds. For high-level steps, the shunt regulator output $+V_o$ is less than 1 millisecond. For low-level steps, the transition time for both +LV and $+V_o$ are approximately 100 microseconds.

Operation of the D.' Shunt Regulator

Amplifier A_1, Figure 6, receives waveform V_p via input R_i connected between V_p and the virtual ground input. It also receives the stepping supply output $+V_o$ as a feedback signal via resistor R_2. The shunt regulator and amplifier A_1, when combined, have a negative overall gain determined by the ratio of R_2 to R_1. The voltage $+V_o$ is then

$$+V_o = -\frac{R_2}{R_1} V_p = -333\ V_p \qquad (11)$$

Compare equation 11 with equation 10; $(+HV) - (+V_o) = 0.1\ V_o + 100$ or the difference of 100 volts plus 10 percent of the output voltage. The difference is the drop across the resistor R_d which provides a margin of regulation for the shunt regulator.

Because of the relatively high maximum voltage (2500 volts) appearing at $+V_o$ and the limited breakdown voltage of available solid-state devices, the shunt regulator, Reference 3, is composed of 9 stages connected in a totem pole configuration. The NPN transistors (Q_1 to Q_9) are rated at 400 volts, and the zener diodes (D_1 to D_9) are rated at 300 volts. This arrangement permits the voltage $+V_o$ to be divided across the 9 transistors.

Each shunting zener diode limits the voltage across its companion collector to emitter junction to about 300 volts. The emitter and base of each transistor are connected by a separate resistor for shunting transistor leakage current in a conventional manner. All bases are coupled to amplifier A_1 output via separate high-voltage diodes (D_{11} to D_{19}) in series with current limiting resistors ($R_{\cdot}$ to R_{13}). These diodes are reverse biased whenever their connecting base-to-emitter junction resides at 300 volts or greater. Amplifier A_1 output can drive each base (Q_1 to Q_9), one at a time, into active linear conduction. If the base is overdriven, the transistor saturates and pulls the next series transistor into conduction.

The composite shunt regulator is variably driven into conduction by the output of amplifier A_1 to a voltage at terminal $+V_o$, refer to equation 11. Current conducts from +HV, through dropping resistor R_d, into the shunt regulator. This current at $+V_o$ passes through all zener diodes whose companion transistors are biased off. It then passes through the transistors to the -10 volt return. For discussion purposes, it is assumed that the zener diodes have a breakdown voltage of 300 volts and that the instantaneous voltage of $+V_o$ is 1400 volts. Starting from terminal $+V_o$, the first four zener diodes (D1 to D4) are in conduction and provide a voltage across diodes D1 to D4 of 1200 volts. The remaining diodes (D5 to D9) and the first four transistors (Q1 to Q4) are at cutoff. The conduction path then passes through the fifth until the ninth transistor (Q5 to Q9). Q5 is dynamically controlled by the output of amplifier A_1 so that it has a collector-emitter voltage drop of approximately 200 volts. Transistors Q6 to Q9 are saturated and have a voltage drop approaching zero volts producing the 1400 volts from terminal $+V_o$ to ground. The first four transistors (Q_1 to Q_4) are maintained at cutoff because the emitter voltage established by the first four zener diodes are higher than the small base voltage established by amplifier A_1.

Thus for any instantaneous voltage $+V_o$, not more than one of the transistors is dynamically controlled by amplifier A_1. All transistors above the controlled transistor are at cutoff and the transistors below the controlled transistor are

saturated. Each transistor assumes control in different adjoining 300-volt ranges, whereby transistor Q_1 dynamically controls $+V_o$ between zero and 300 volts, transistor Q_2 dynamically controls $+V_o$ between 300 volts and 600 volts, and so forth. The shunt regulator is returned to a -10 volt source rather than to ground in order to enable the low gain amplifier output +LV to pass through the steering diode D_{10} to the output $+V_o$, when $+V_o$ is less than 25 volts. As mentioned before, when the output $+V_o$ is between the range 2500 volts and 25 volts, it obtains its voltage from the parallel charge multiplier output +HV through the dropping resistor R_d. When it is in the 25 volt or less range, it obtains its voltage from the low gain amplifier output +LV through the steering diode D_{10}. The control for this process is a logic "OR" function. The inputs to the "OR" are +HV and +LV and the output is the $+V_o$ voltage. For the MSB range, a staircase voltage at E_1 (Figure 1) is amplified by a gain of -333 to become $+V_o$ by controlling the parallel charge multiplier voltage +HV and the dc shunt regulator gain. For the LSB range this amplification gain is only -3.33 by controlling the low-gain amplifier. Therefore, E_1 = -7.5 volts, $+V_o$ would be 2500 volts via the high channel and +25 volts via the low gain channel. The LSB range covers the second half cycle (steps 33 to 64) of the 64 step cycle. During this period, the $+V_o$ output is obtained via the low gain channel and is equal to:

$$+V_o = +LV - \text{steering diode drop} \qquad (12)$$

$$= 28 - 3 = 25 \text{ volts}.$$

Also during this period all the transistors in the shunt regulator are saturated on and the diode modulator is turned off, effectively blocking any voltage build up at +HV. This condition is created by the 2^5 bit that causes a slight positive voltage at V_p. The shunt regulator is dormant during this period with a passive load from $+V_o$ to -10 volts of 100 kilohms.

The negative voltage shunt regulator operates similar to the positive voltage shunt regulator. There are two additional circuits used in the negative voltage regulator to bring its voltage $-V_o$ exactly equal to, but opposite in polarity from the $+V_o$ voltage. One is the "BAL. ADJ." trimming resistor coupled to the input of the amplifier A_2 in Figure 6; this adjustment is for the high gain channel. The other is the low gain adjust (LGA) resistor network coupled to the input of amplifier A_4, Figure 3, to adjust for the low gain channel output. This slight difference in voltage between the two outputs is due to component tolerance error in each channel. A to be determined (TBD) capacitor across R_2 in the feedback loop of each shunt regulator is used to adjust for critical damping in the operational amplifier loop.

CONCLUSION

Although the high-voltage stepping supply described in this document pertains to step-down staircase voltages, a step-up staircase voltage may be constructed by using the same design principles. Other voltage combinations, such as having a step-up and step-down voltage supply, can also be obtained.

ACKNOWLEDGMENTS

The author wishes to thank Mr. John L. Westrom, GSFC Code 711, for helpful suggestions and comments and for the assistance of Mr. Kenneth M. Young, GSFC Code 711, who built and helped test the units; in addition, I wish to thank Mrs. Thelma M. Young for typing assistance.

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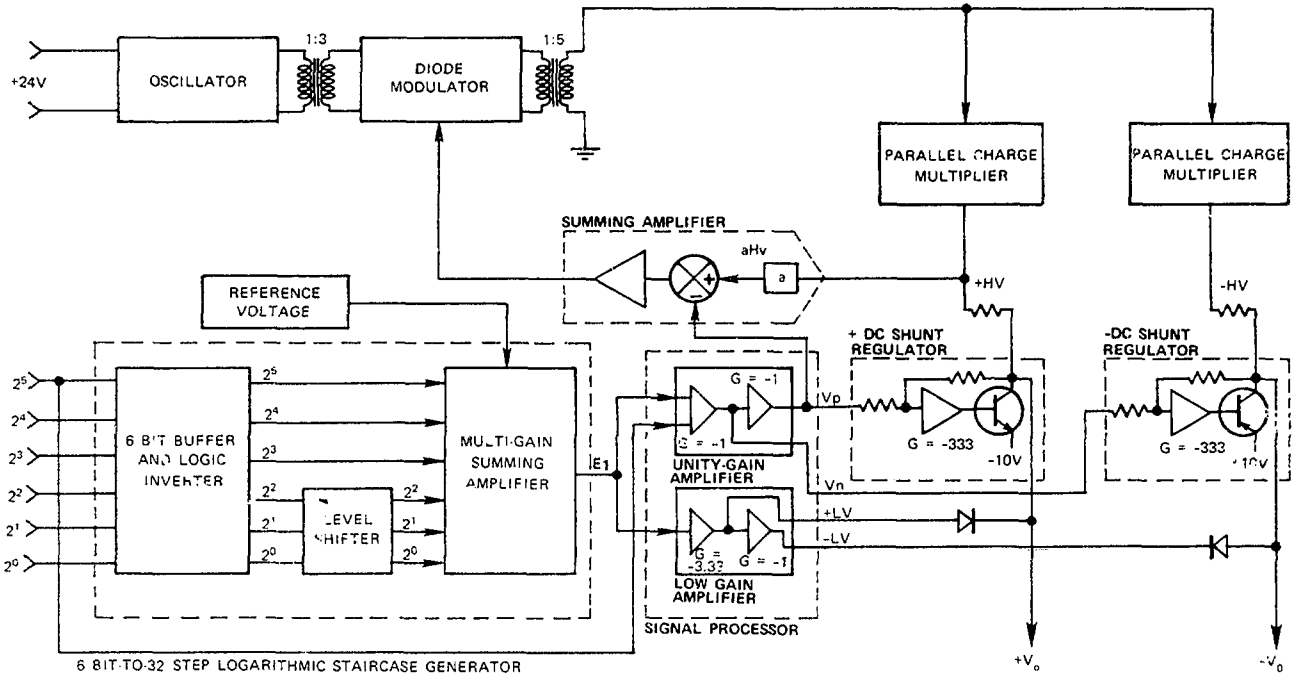

Figure 1. Stepping Supply Functional Diagram

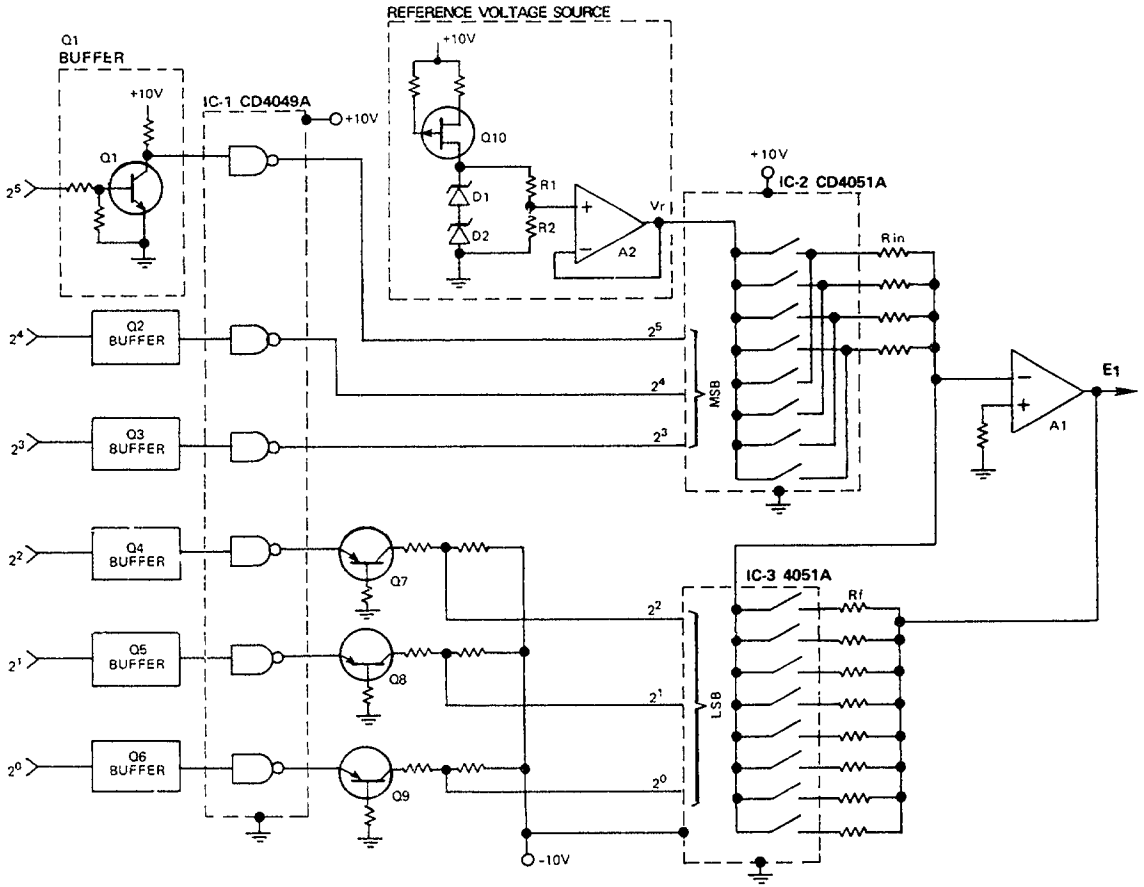

Figure 2. Six Bit to 32 Step Logarithmic Staircase Generator

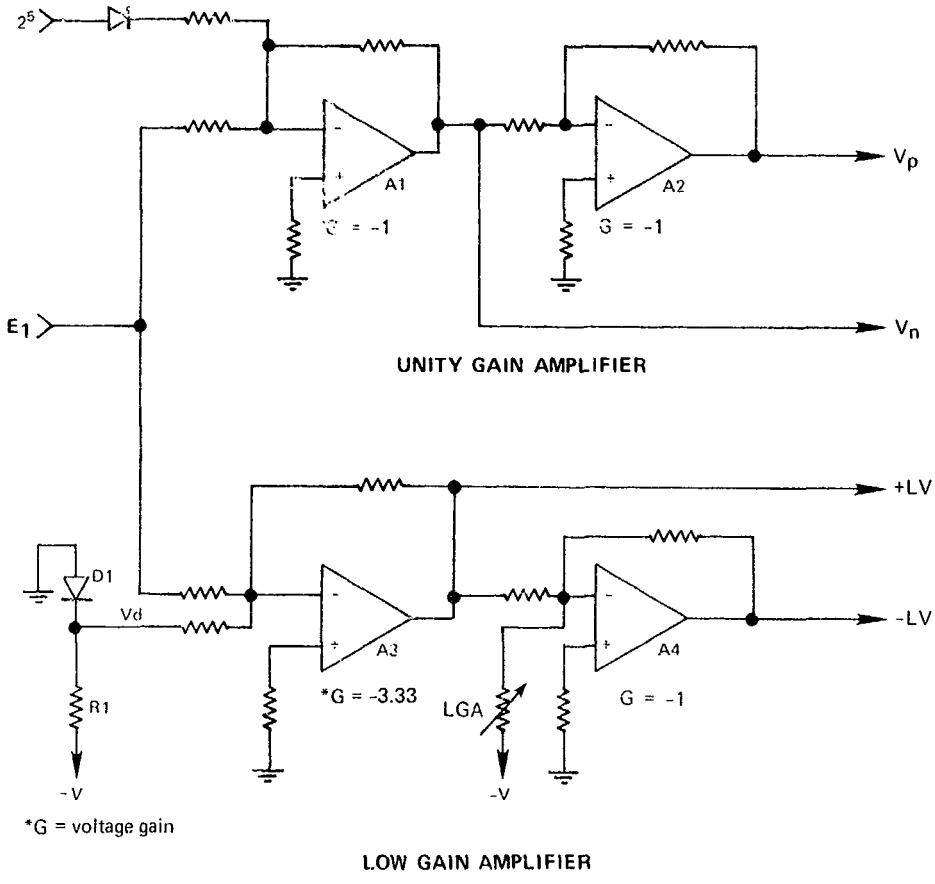

Figure 3. Signal Processor

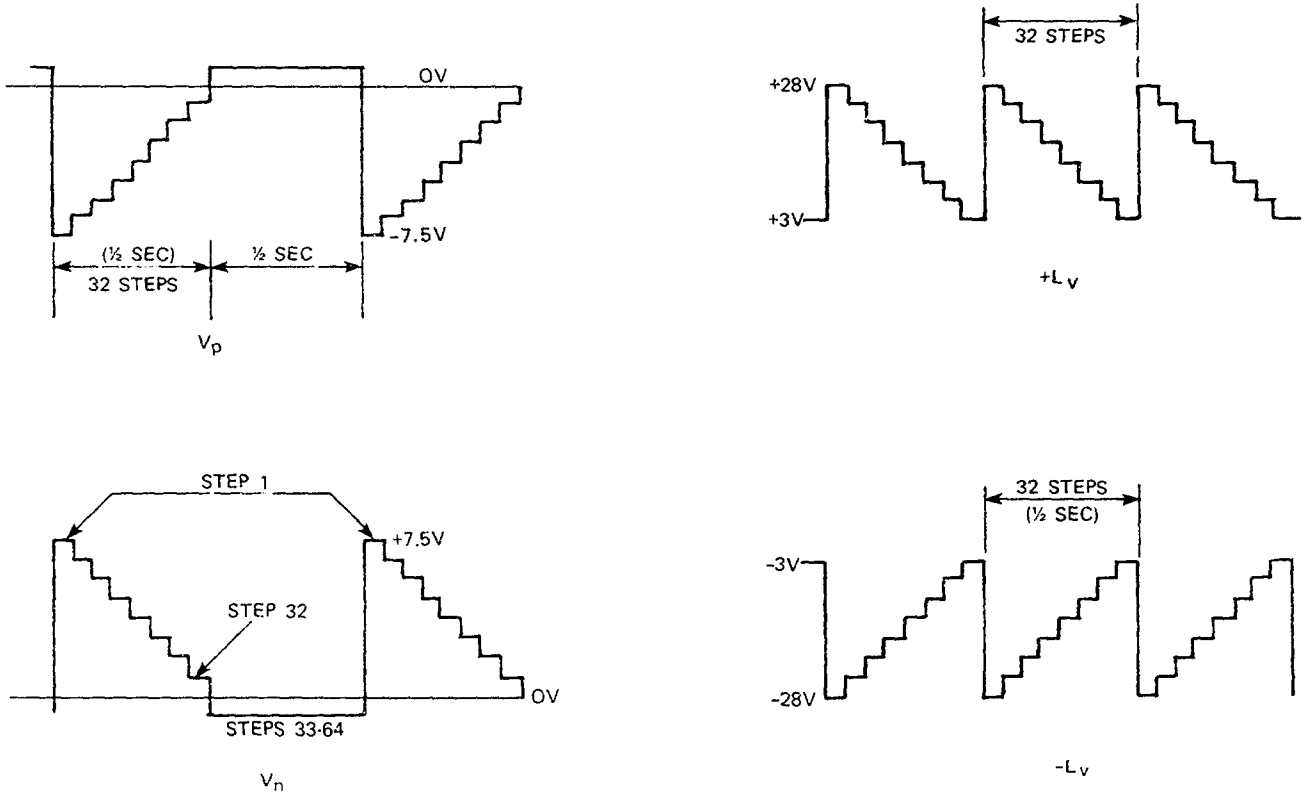

Figure 4. Signal Processor Output Waveforms

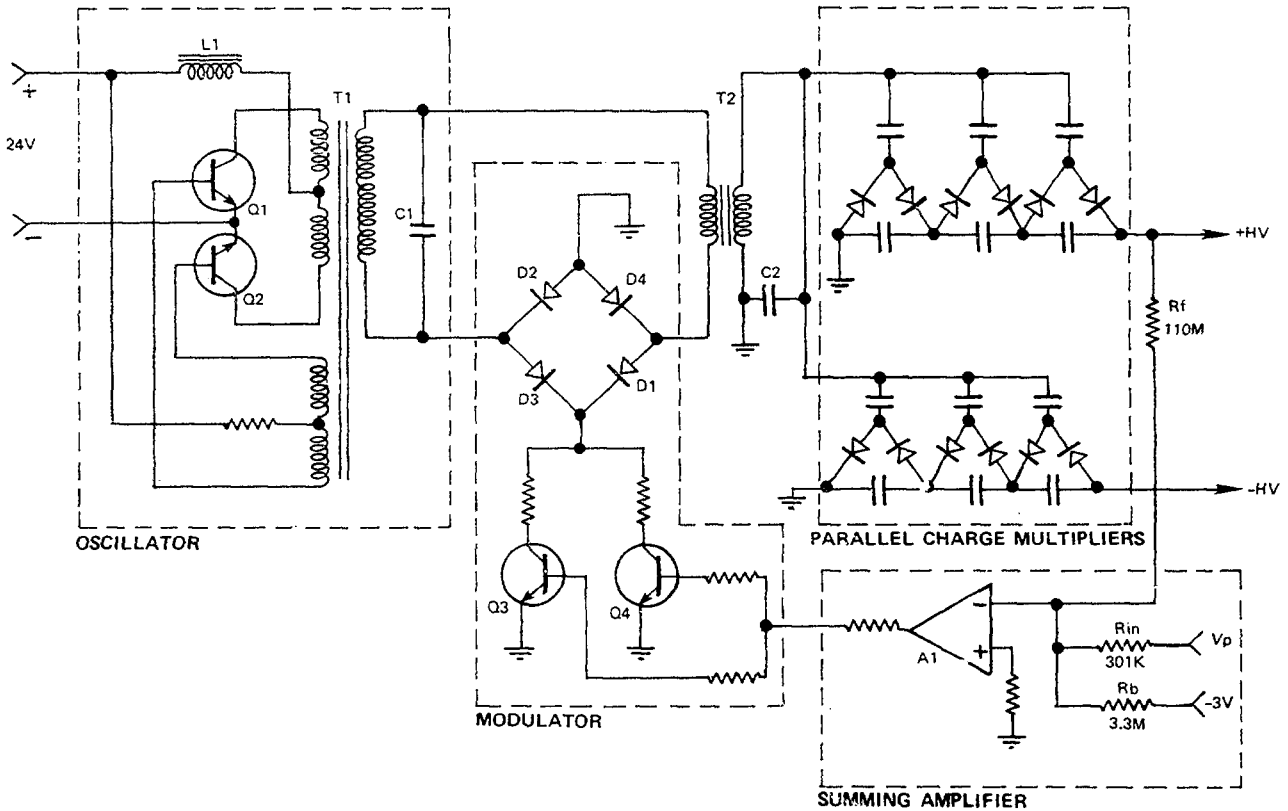

Figure 5. Oscillator, Modulator, and Parallel Charge Multipliers

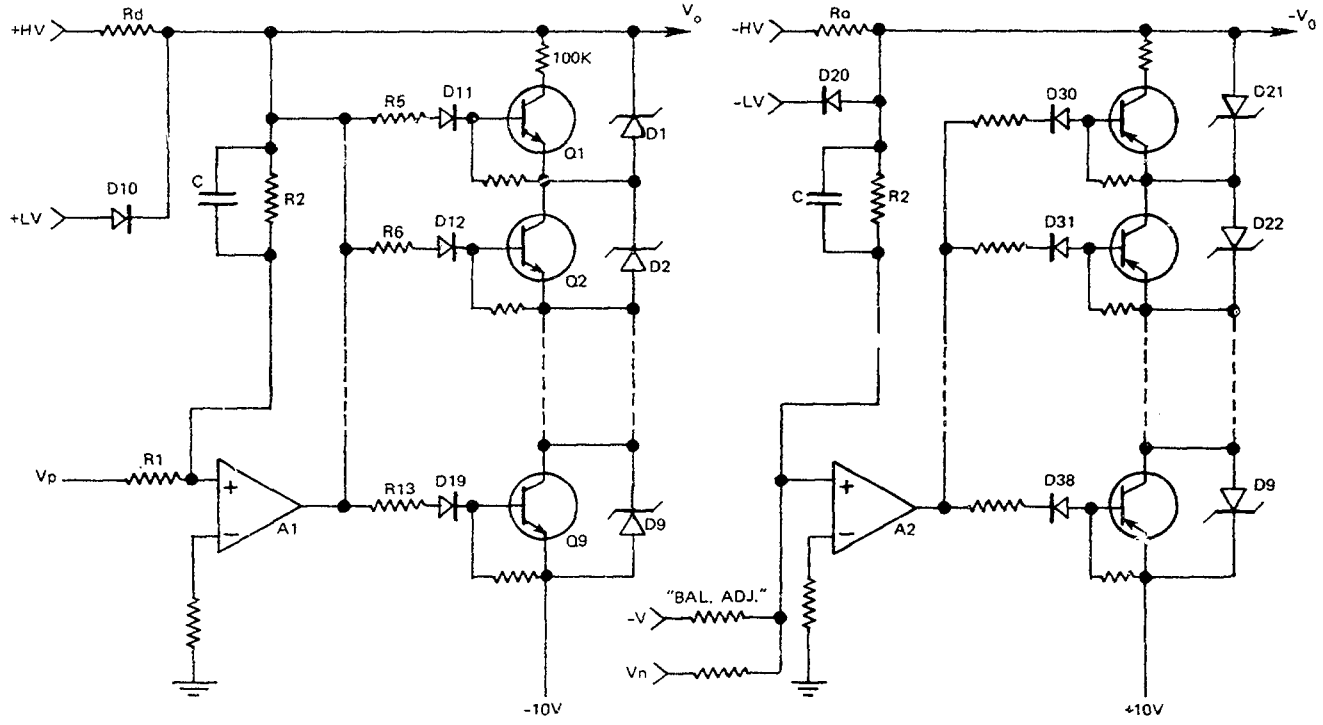

Figure 6. High-Voltage DC Shunt Regulators

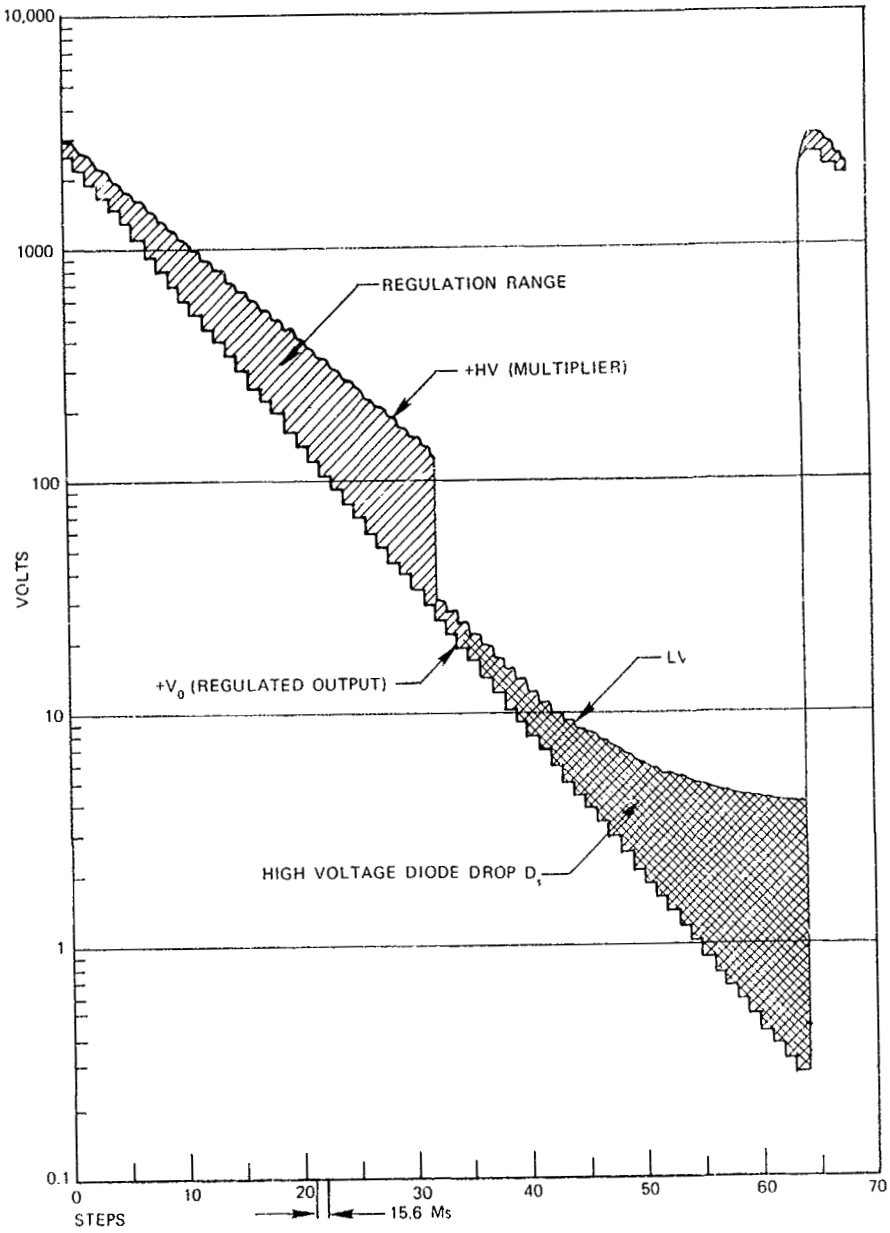

Figure 7. Multiplier, Low Level, and Regulated Outputs