CR-135358
TRW 31526.000

EXTENDED PERFORMANCE ELECTRIC PROPULSION POWER PROCESSOR DESIGN STUDY

FINAL REPORT

VOLUME II TECHNICAL SUMMARY

NOVEMBER 1977

by:

TRW DEFENSE AND SPACE SYSTEMS GROUP
POWER CONVERSION ELECTRONICS DEPARTMENT

Prepared For:

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
NASA LEWIS RESEARCH CENTER

CONTRACT NAS 3-20403

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Project Manager Robert J Frye, NASA Lewis Research Center, Cleveland, Ohio 44135

16 Abstract

Electric Propulsion Power Processor Technology has processed during the past decade to the point that it is considered ready for application During this study, several power processor design concepts were evaluated and compared Emphasis was placed on a 30cm Ion Thruster Power Processor with a Beam Power Rating Supply of 2 2KW to 10KW for the main propulsion power stage Extensions in power processor performance were defined and were designed in sufficient detail to determine efficiency, component weight, part count, reliability and thermal control

A detail design was performed on a microprocessor as the thyristor power processor controller A reliability analysis was performed to evaluate the effect of the control electronics redesign

A Preliminary electrical design, mechanical design and thermal analysis were performed on a 6KW power transformer for the beam supply

Bi-Mod mechanical, structural and thermal control configurations were evaluated for the power processor and preliminary estimates of mechanical weight were determined

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FORWARD

The work described herein was performed in the Power Conversion Electronics Department of the Electrical System Laboratory within the Space Systems Division of TRW Defense and Space Systems Group. This department is managed by Mr. Bert J. McComb. The work was funded under contract NAS 3-20403 and monitored by Mr. Robert Frye of the NASA Lewis Research Center. The key technical contributors were:

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Efren Mendez	Project Engineer for Mechanical Design and Power Magnetic Mechanical Design
Chuck Louie	Project Engineer for Digital Interface Unit Microprocessor
Bernie Shupack	Project Engineer for Thermal Control of Power Processor and Power Magnetics
Bob Heile	Project Engineer for Reliability
A. D. Schoenfeld	Technical and Project Review
M. G. Monegan	Mechanical and Thermal Design Review

SUMMARY

The primary objective of this study was to provide a data base for a program plan for the development of the ion propulsion power processor to support a Halley's Comet Rendezvous Mission. This data base was to include:

- Conceptual design and tradeoffs for an electric propulsion power processor with a power rating up to 10kW beam power.
- Identification of New Technology Requirements and potential savings and risks.
- Selection of a preferred Power Processor Configuration.
- Preliminary Electrical and Mechanical Design of the preferred configuration.
- Program plan for the electric propulsion power processor in support of a Halley Comet Rendezvous Mission.

A preferred configuration for the power processor was selected as a result of detailed analysis of the data base. A complete electrical design was performed for a 6kW and 2.2kW beam supply power processor based on a revised power processor requirement specification and updated electrical design for product improvement in the area of part count reduction, weight reduction and efficiency improvement.

A discussion is presented on the electrical redesign of control electronics and microprocessor for thruster operation. The beam power transformer design is presented with the thermal analysis. A preliminary reliability analysis was performed.

A presentation is made for a method to determine the power processor weight efficiency optimization tradeoff. The accuracy of the optimization is determined by the solar array power vs. weight constant and by the thermal control heat rejection system weight vs. loss constant.

A conceptual mechanical design was performed to identify the electrical, structural and thermal interfaces.

The following is a summary of the 6KW beam power processor design characteristics:

Electrical component weight	21.3KG
Electrical component losses	605W
Efficiency at nominal load	91.5%
Part count	2720
Mechanical packaging hardware weight	21.0KG
Volume	.107 cu meter

The following is a summary of the 2.2KW beam power processor design characteristics:

Electrical component weight	14.4KG
Electrical component loss	333W
Efficiency at nominal load	89.2%
Part count	2587
Mechanical packaging hardware weight	14 4KG
Volume	.073 cu meter

The designs were based on existing component technologies and therefore the technical risks were minimal and would not compromise the overall program schedule.

A detailed program plan schedule and cost estimate in support of the Halley Comet Rendezvous Mission are contained in Volume I, Executive Summary.

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1. INTRODUCTION

Solar electric propulsion is being viewed as matured, developed technology that can be applied to new high energy missions in the 1980 time frame with the Shuttle/IUS as the launch vehicle.

The Halley Comet Rendezvous Mission requires a major decrease in the ion drive systems specific mass currently projected for the 3KW, 30cm ion thruster as approximately 50KG/KW. This requirement necessitates a thrust system design which increases the output power to greater than 6KW.

Because of the increase in output power level, it is necessary to redesign the power processor. Contract NAS3-20403, "Extended Performance Electric Propulsion Power Processor Design Study," performed the necessary conceptual design and tradeoffs to identify the preferred power processor circuit configuration that meet the new requirements while at the same time reducing the specific mass KG/KW and improving the power processor efficiency and reliability.

This study program had three objectives. The first was to evaluate the power processor unit at higher beam supply power levels (from 2.2 to 10KW). The second was to evaluate revised requirements and alternate methods of implementation for the low power supplies of power processing unit; and the third was to develop a power processor plan to support a Hally Comet Rendezvous Mission. The outputs of the first two objectives are system approaches versus weight, efficiency, parts count, reliability, and component technology requirements.

The information obtained from this contracted effort was used in direct support of a Halley Comet Rendezvous Mission study completed in the summer of 1977 and other alternate electric propulsion missions being planned in the 1980 time period.

This report summarizes the results of a six month study to define the design, program plan and cost of the electric propulsion power processor for the Halley's Comet Mission Spacecraft

The following sections summarize the results of the design trade-off studies. After the selection and approval of the preferred configuration by NASA Lewis, a detailed electrical design, magnetic design and thermal control and conceptual mechanical packaging was performed.

An assessment of the technical risks is also presented.

2. DESIGN TRADEOFF STUDIES

The first task of the study program considered a spectrum of alternate power distribution systems, mechanization of the beam supply up to 10KW, mechanization of discharge supply, mechanization of the low voltage supplies and the method of controlling the power processors by means of central computer or localized microprocessor. The following sections present the results of the design tradeoff studies. A method to evaluation of the weight efficiency optimization is presented in Section 2.6. Section 3.0 Baseline Design presents the results of the detail design of the selected power processor configuration.

2.1 Power Distribution System

Two separate power distribution systems were studied·

a) A single 200-400VDC solar array split bus supplies all the power to the thrust subsystem and the mission module.

b) a 200-400VDC solar array split bus supplies power to beam and discharge supplies for the thrust subsystem and two separate 28VDC solar array buses supply power to the ion thruster low level outputs and the mission module.

The split or center tapped solar array bus reduces the space charge interaction with the solar array and allows the adaption of existing remote power controllers (solid state switchgear) to provide fault isolation in case of power processor failure. These remote power controllers must be used in both the positive and negative power lines and must open at the same time so that they will not be subjected to overvoltage stress.

Figures 2-1 and 2-2 present the basic block diagrams for these different power distribution systems. Table 2-I and 2-II summarizes the characteristics of the two different systems.

Figure 2-2 (200-400VDC bus and 28VDC bus) was the selected configuration since it would be more compatible with existing 28VDC hardware developed for other spacecraft programs. The high voltage DC was only used for the high power loads of the ion engine (beam and discharge supplies).

The selected configuration has the maximum reliability with use of solid state breakers to clear failed hardware and redundant 28VDC distribution buses.

Further development is required on the solid state breakers for the ion engine and for the thrust system controller hardware and software.

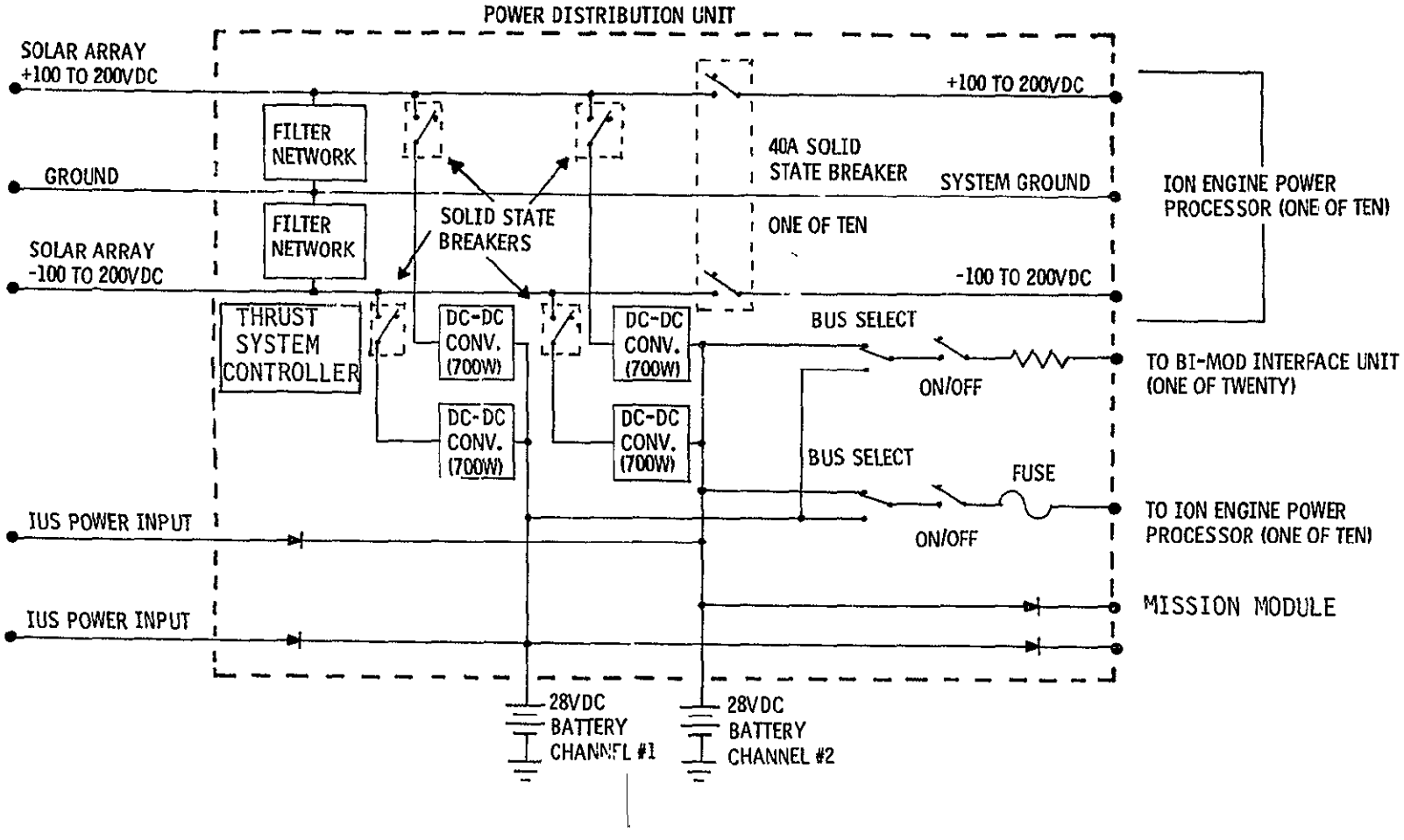


Figure 2-1. 200-400VDC Power Distribution System

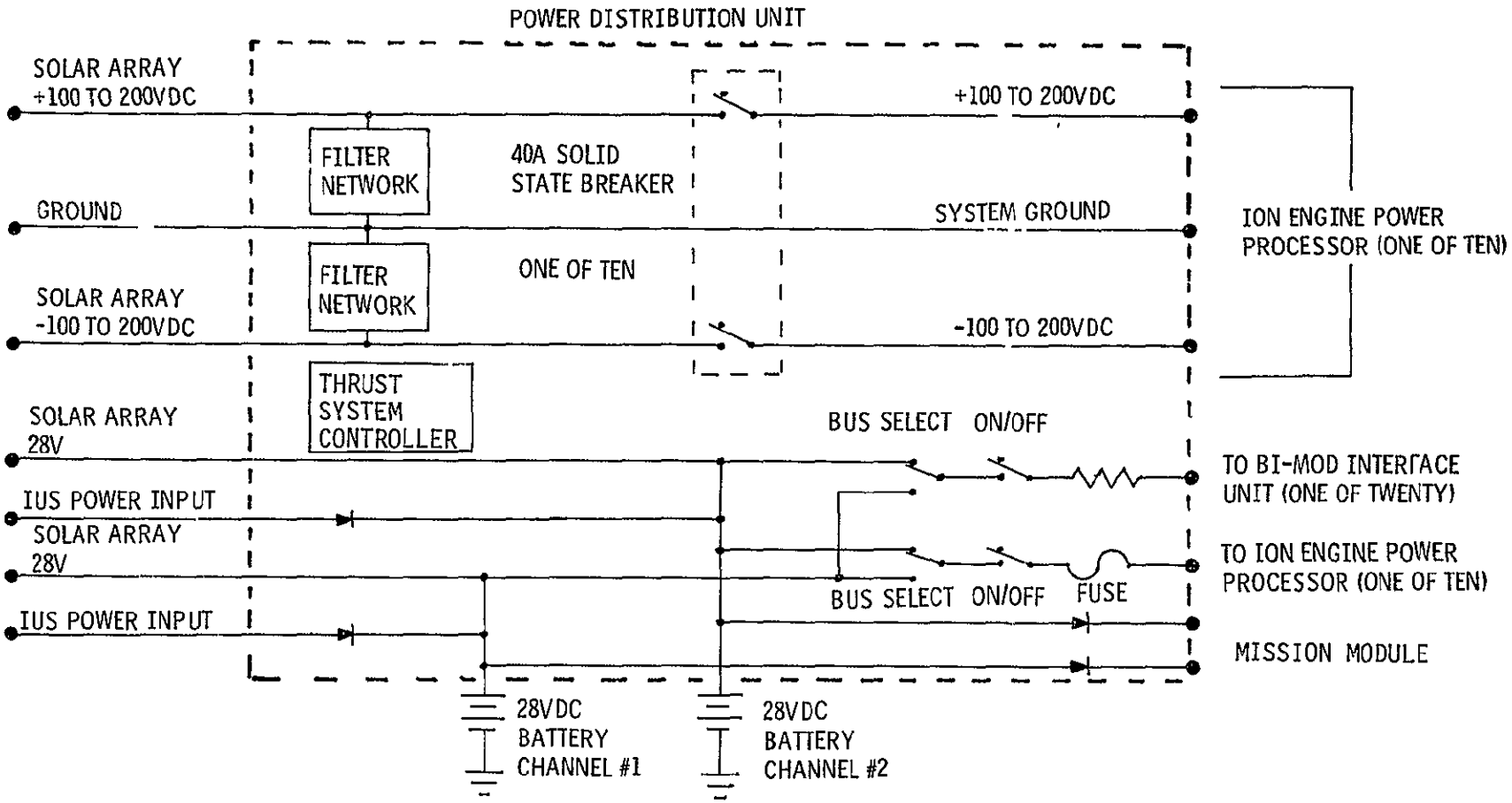


Figure 2-2. 200 to 400VDC and 28VDC Power Distribution System

Table 2-I. Summary of 200-400VDC Power Distribution System Characteristics

- Plus (+) and Minus (-) Solar Array Voltage Reduces
  a) Component stresses (Solid State Breaker)
  b) Space Charge Interaction
- Filter Network Controls Bus Impedance for EMC
- Thrust System Controller Perform all Power Control & Management (Max Power Tracking, Bi-Mod Control, Failure Analysis, Attitude Control, Thrust & Gimbal Angle).
- Solid State Breaker for Loads on ±100 to 200VDC Distribution Bus.
- Low Voltage DC Power Distribution for EMC Control and Ease of Integration of All Low Power Equipment.
- Redundant +28VDC Buses for Low Power Distribution:
  a) Interface with Mission Module
  b) Interface with IUS
  c) Interface with Bi-Mod
- Battery Supplies Transient Loads such as Startup and Fault Clearing.
- Plus (+) and Minus (-) DC-DC Converters Condition Power for 28VDC Bus (700W Rating to Carry Maximum Load if Required for Redundancy).
- On/Off Control, Bus Selection and Fault Clearing for 28VDC Loads.
- Compatible with IUS Power Bus.

Table 2-II. Summary of 200-400VDC and 28VDC Power Distribution System Characteristics

- Plus (+) and Minus (-) Solar Array Voltage Reduces:
  a) Component Stresses (Solid State Breaker)
  b) Space Charge Interaction
- Filter Network Controls Bus Impedance for EMC.
- Thrust System Controller Performs all Power Control & Management (Max Power Tracking Bi-Mod Control, Failure Analysis, Attitude Control, Thrust & Gimbal Angle).
- Solid State Breaker for Loads on ±100 to 200VDC Distribution Bus.
- Low Voltage DC Power Distribution for EMC Control and Ease of Integration of all Low Power Equipment
- Redundant +28VDC Buses for Low Power Distribution·
  a) Interface with Mission Module
  b) Interface with IUS
  c) Interface with Bi-Mod
- Battery Supplies Transient Loads such as Startup and Fault Clearing.
- On/Off Control, Bus Selection and Fault Clearing for 28VDC Loads.
- Compatible with IUS Power Bus.
- Isolated 28VDC Solar Array to Supply Low Level Electronic Loads.

2.2 Beam Supply Tradeoff Analysis

In order to obtain beam power levels up to 10KW with existing high power thyristors, different power stage mechanization and modulization had to be designed and anayzed.

The series resonant inverter power stage configurations selected for review included·

- Single full bridge — 6KW power rating
- 2 Channel full bridge — 10KW power rating
- 2 Channel half bridge — 6KW power rating
- 3 Channel half bridge — 10KW power rating
- 4 Channel half bridge — 10KW power rating

Figure 2-3 presents the schematic of the thyristor full bridge operating at maximum frequency of 20kHz.

Figure 2-4 presents the schematic of the thyristor half bridge operating at maximum frequency of 20kHz.

Table 2-III summarizes the design results of different power and power stage configurations The single full bridge (6KW rating) was the selected configuration due to its low component weight. The efficiency of all of the beam configurations remained above 93%.

The use of the thyristor series resonant inverter allows power growth with minimal impact on the weight loss and part count. With further development of the power thyristor from the 200A current capability to a 500A rating could easily allow the basic power stage to operate at about 20KW. The basic component limitations at this time is the power thyristor. Additional development of the power transformer may be needed to maintain adequate operating temperatures with the present thermal control techniques.

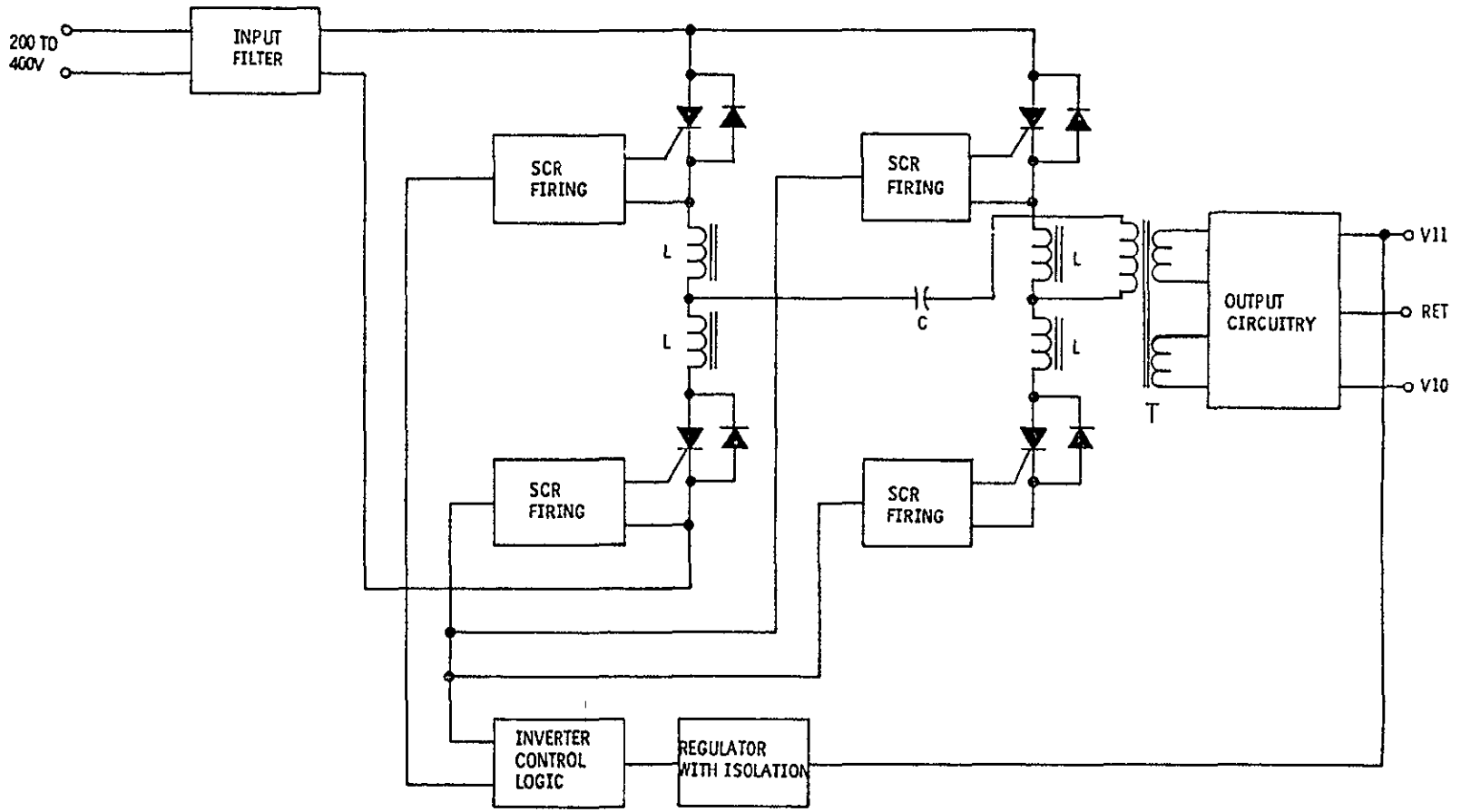


Figure 2-3. Schematic of the Thyristor Full Bridge Series Resonant Beam Inverter

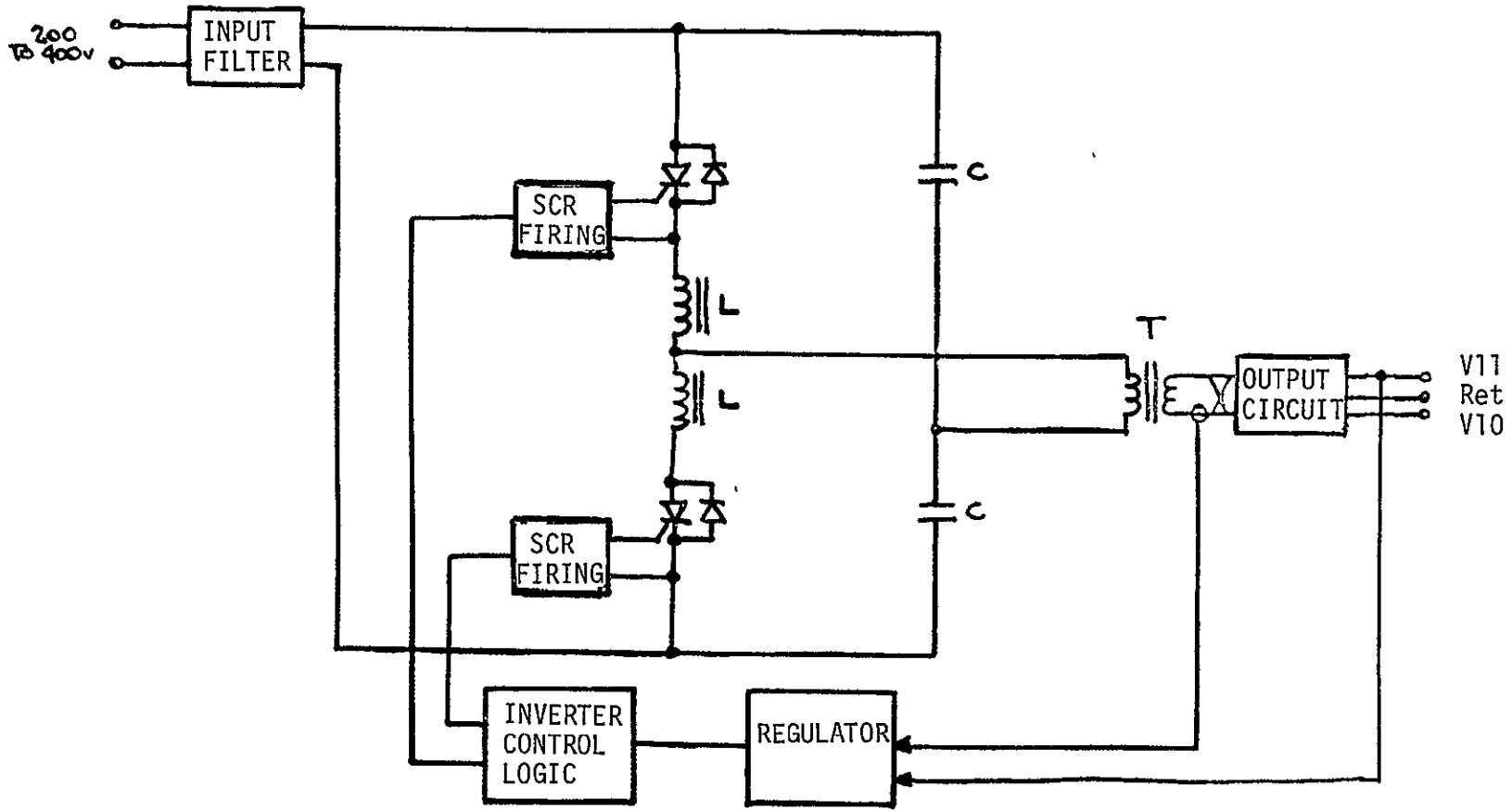


Figure 2-4. Schematic of the Thyristor Half Bridge Series Resonant Beam Inverter

Table 2-III Summary of Beam Supply Tradeoff Analysis

CONFIGURATION	MAXIMUM PWR RATING	COMPONENT WEIGHT (KG)	LOSS (WATTS) *	PART COUNT	POWER STAGE EFFIC. (%)
SINGLE FULL BRIDGE	6KW	9.4	440	521	93.6
2 CHANNEL FULL BRIDGE	10KW	16.0	743	910	93 5
2 CHANNEL HALF BRIDGE	6KW	11.4	478	740	93 1
3 CHANNEL HALF BRIDGE	10KW	18.1	770	1041	93 2
4 CHANNEL HALF BRIDGE	10KW	19.1	784	1352	93 2

*Losses include power stage and control losses

2.3 Discharge Supply Tradeoff Analysis

Due to the relatively lower power rating of the discharge supply (800W), new power conversion technology can be applied. The different configurations analyzed include the following:

- Thyristor 20kHz half bridge series resonant inverter
- Transistor 50kHz full bridge series resonant inverter

The half bridge configuration is similar to that shown in Figure 2-4 and uses the standard power thyristor.

Figure 2-5 presents the schematic of the transistorized 50kHz full bridge series resonant inverter which takes advantage of the faster switching and lower storage times of the power transistors.

Table 2-IV summarizes the design results of the two different configurations.

Due to the electrical component weight saving of about 1.1KG, the 50kHz full bridge transistorized series resonant inverter was selected as the preferred configuration.

There is a penalty in efficiency but when analyzed against the weight efficiency optimization discussed in section 2.6, the overall weight was lower.

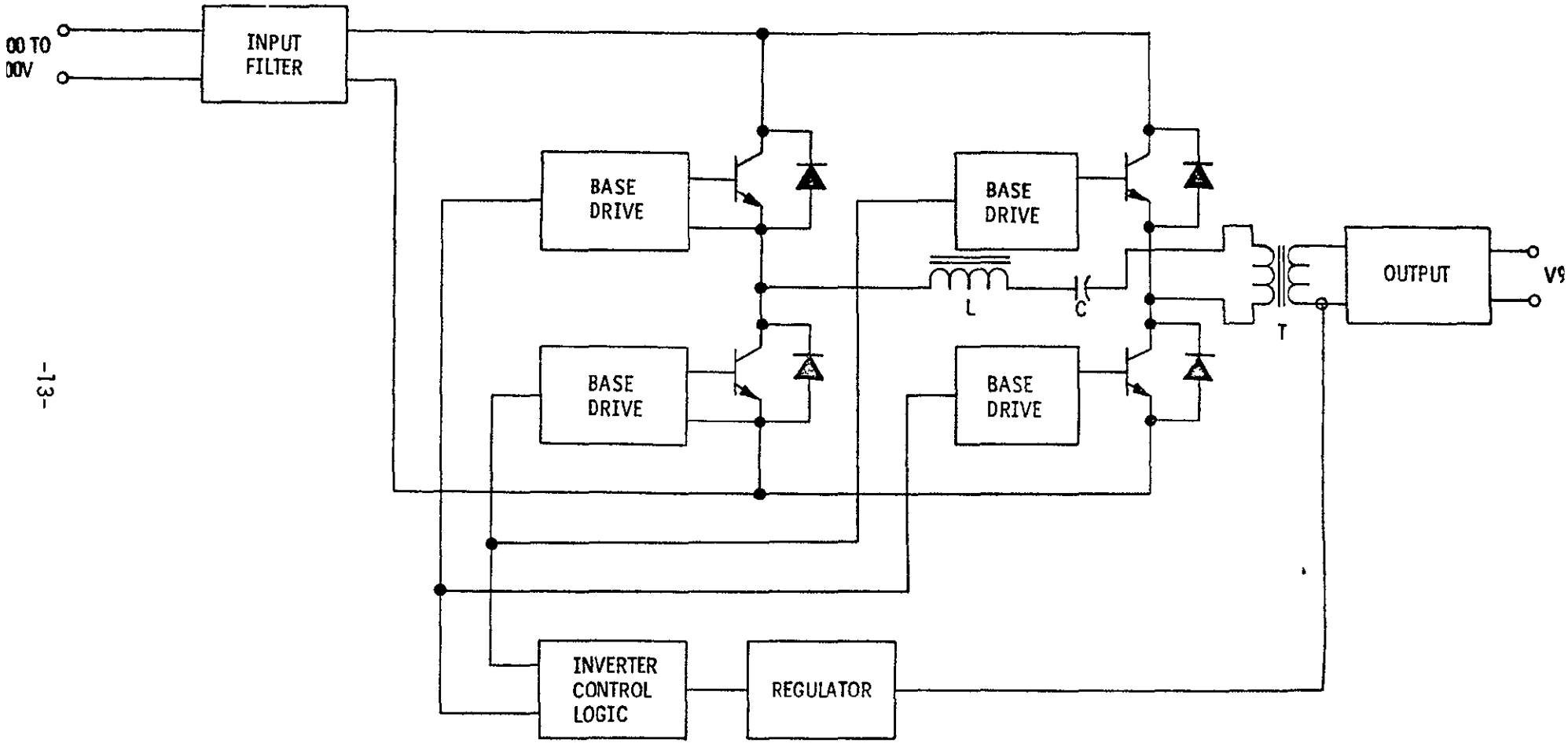


Figure 2-5. Schematic of Transistorized Bridge Series Resonant Discharge Inverter

Table 2-IV Summary of Discharge Supply Tradeoff Analysis

CONFIGURATION	MAXIMUM PWR RATING	COMPONENT WT. (KG)	LOSS AT 415W OUTPUT (W) *	PART COUNT	POWER STAGE EFFIC. (%)
THYRISTOR 20kHz HALF BRIDGE	815W	3.3	70.7	331	88.0
TRANSISTOR 50kHz FULL BRIDGE	815W	2.2	79.1	473	87 2

*Losses include power stage and control losses

2.4 Low Voltage Supplies Tradeoff Analysis

The low voltage supplies greatly affect the total power processor weight, losses and part count. Tradeoffs were performed on new power stage configurations, sharing of power functions between two thrusters in a Bi-Mod configuration and the application of latest integrated circuit technology.

The power electronics mechanization to satisfy the revised power processor requirements include:

- Transistor Half Bridge 50kHz Series Resonant Inverter (Figure 2-6)
- Transistor Half Bridge 50kHz Series Resonant Inverter to Operate Two Ion Thrusters in a Bi-Mod Configuration (Figure 2-7)
- Buck/Boost DC/DC Converter for Each Separate Output Load (Figure 2-8)

Table 2-V summarizes the characteristics of the low voltage supply configurations.

The dedicated Buck/Boost DC/DC Converter is the preferred configuration mainly since it has the highest overall efficiency in comparison with the other proposed configurations.

It also maintains the high efficiency over wide output power loading which are required when starting up a cold engine and when providing normal steady-state power to operate the ion engine control loops.

No potential advantage were identified in the Bi-Mod Configuration shown in Figure 2-7. It had a potential lower reliability where one series resonant inverter could fail two ion engines.

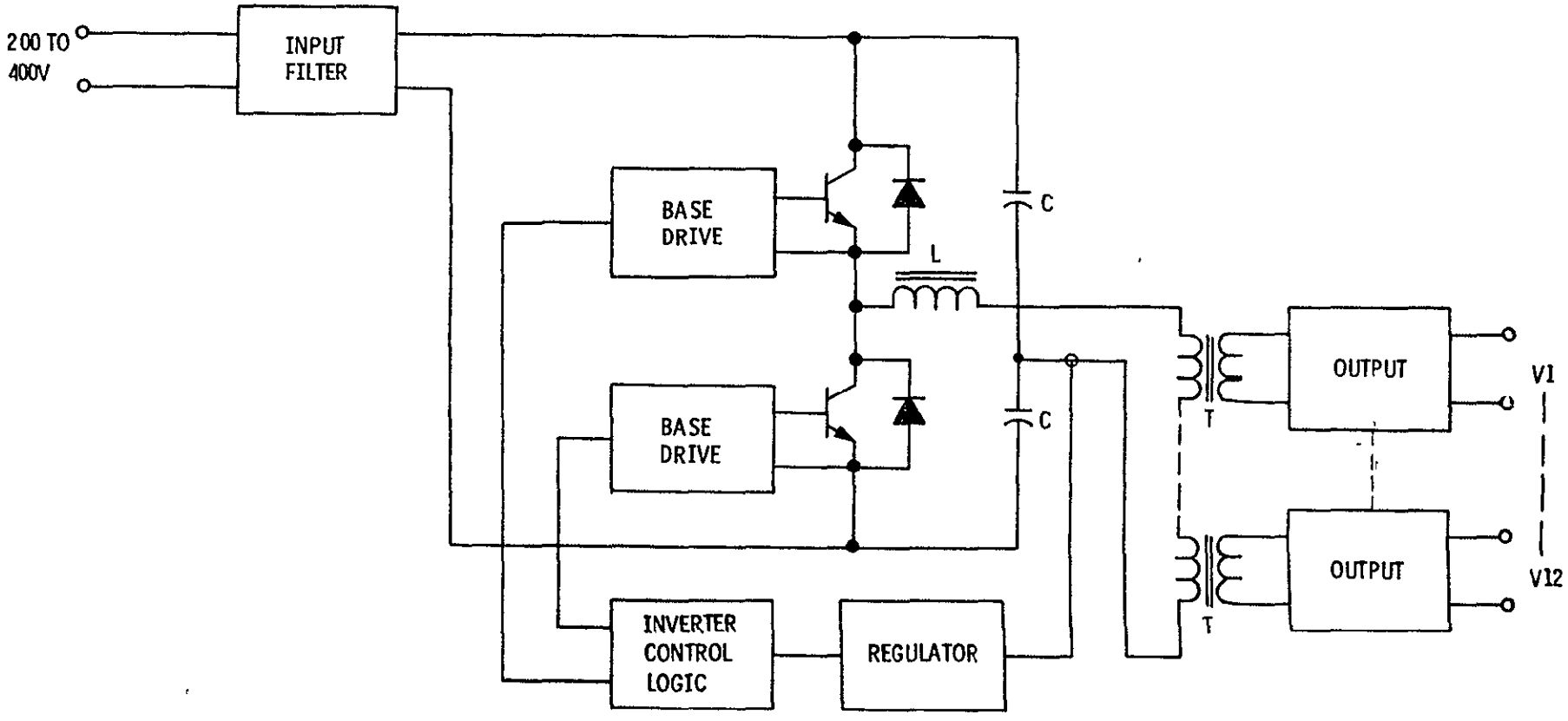


Figure 2-6. Schematic for Half Bridge 50kHz Series Resonant Inverter for the Low Voltage Supplies

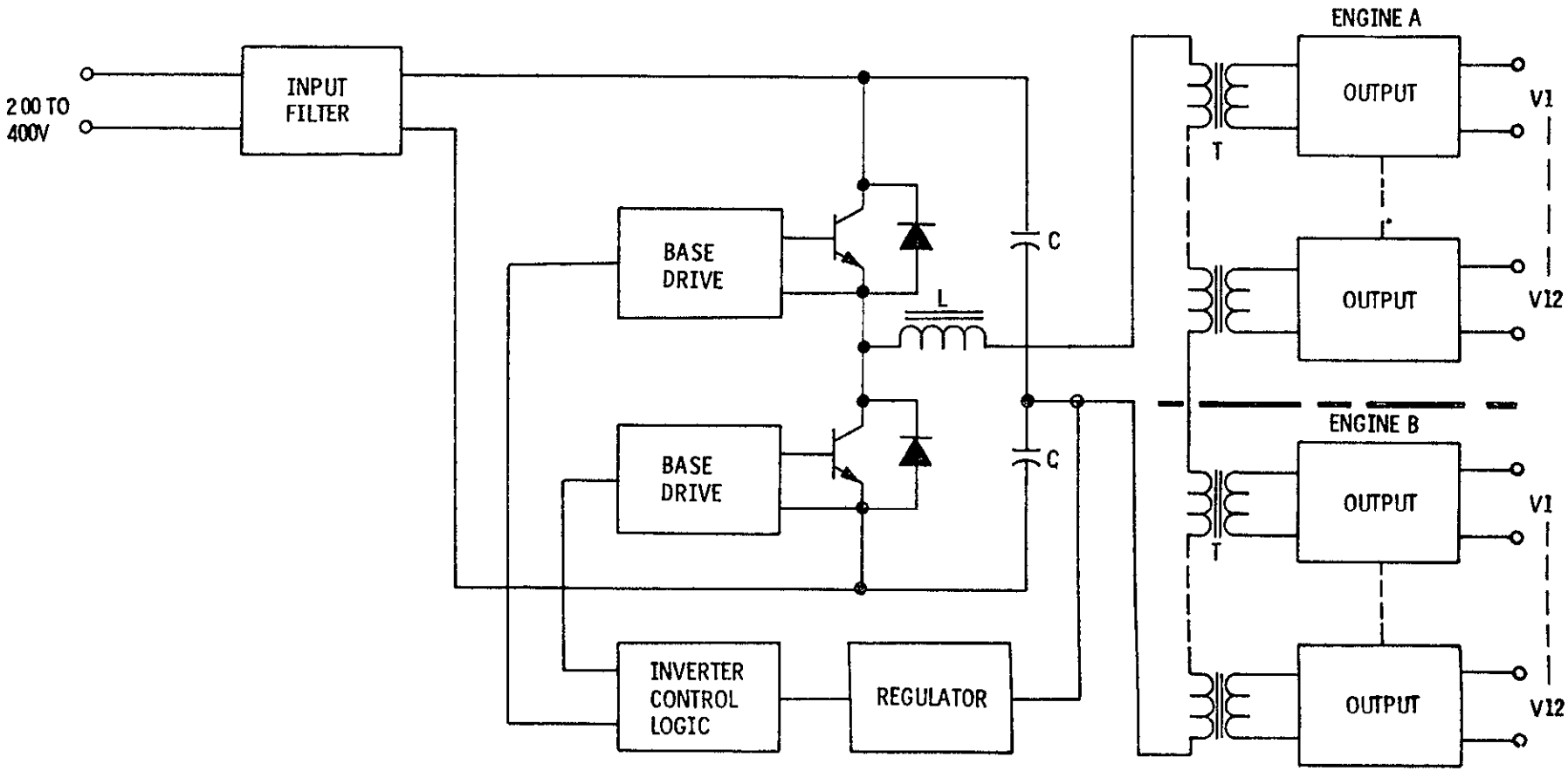


Figure 2-7. Schematic of Transistorized 50kHz Series Resonant Inverter Configurated to Supply Low Voltage Outputs for Two Thrusters in Bi-Mod Configuration

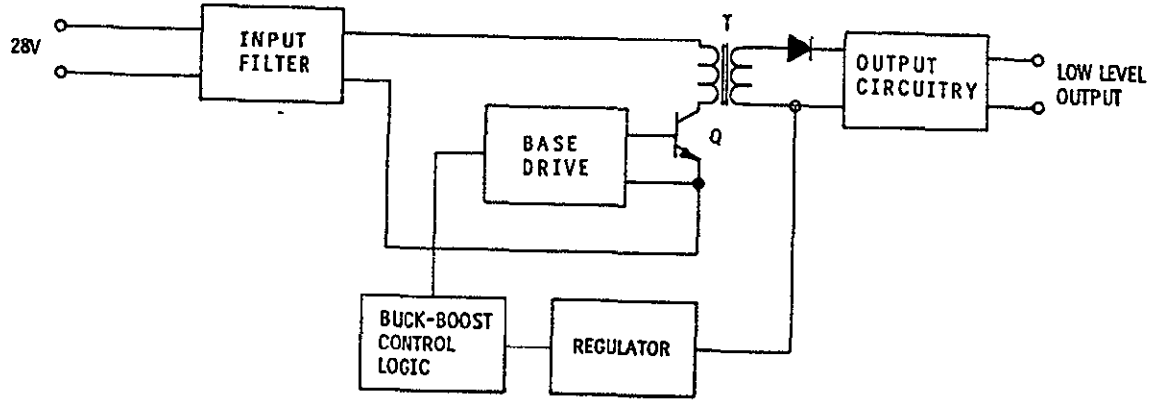


Figure 2-8. Schematic of Buck/Boost DC/DC Converter for Typical Low Voltage Supply

CONFIGURATION	MAXIMUM PWR RATING	COMPONENT WT. (KG)	LOSS AT 45W OUTPUT (W)*	PART COUNT	POWER STAGE EFFIC. (%)
Transistor Half Bridge Series Resonant Inverter	200W	2.7	65.8	1001	46.0
Transistor Half Bridge Series Resonant Inv. for Bi-Mod	250W	4.8	109.9(@90W)	1673 (2 Units)	48.9
Dedicated Buck/Boost DC-DC Converter	200W	2.6	25 6	1039	66.5

*Losses include power stage and control losses.

Table 2-V Summary Data for Low Voltage Supply Design Configurations

2.5 Power Processor Configuration Tradeoff

Two separate power processor configurations were mechanized to satisfy the requirements of the two power distribution system identified in Section 2.1.

These configurations include·

a) a single 200-400VDC solar array bus to supply all power (Figure 2-9).

b) 200-400VDC bus supplies power to high power loads, such as beam and discharge and a 28VDC solar array bus supplies power for the low level supply (Figure 2-10).

In Figure 2-9, three series resonant inverters process all of the 200-400VDC power to the ion engine. 28VDC power is used only for internal power processor control electronics and for microprocessor digital interface units. This configuration is very similar to the (2.7KW) Electrical Prototype Power Processor Unit developed under contract NAS3-19730.

In Figure 2-10, two series resonant inverters process the 200 to 400VDC power to beam and discharge functions of the ion engine. All the remaining low power controller used 28VDC power through dedicated DC-DC Converters.

Table 2-VI and VII summarizes the characteristics for the two power processor block diagrams, respectively.

The major function is listed with its part count, electrical component weight and losses for each major element.

- Beam inverter
- Discharge inverter
- Low voltage supplies
- Input filter
- Low level command, control and telemetry electronics.

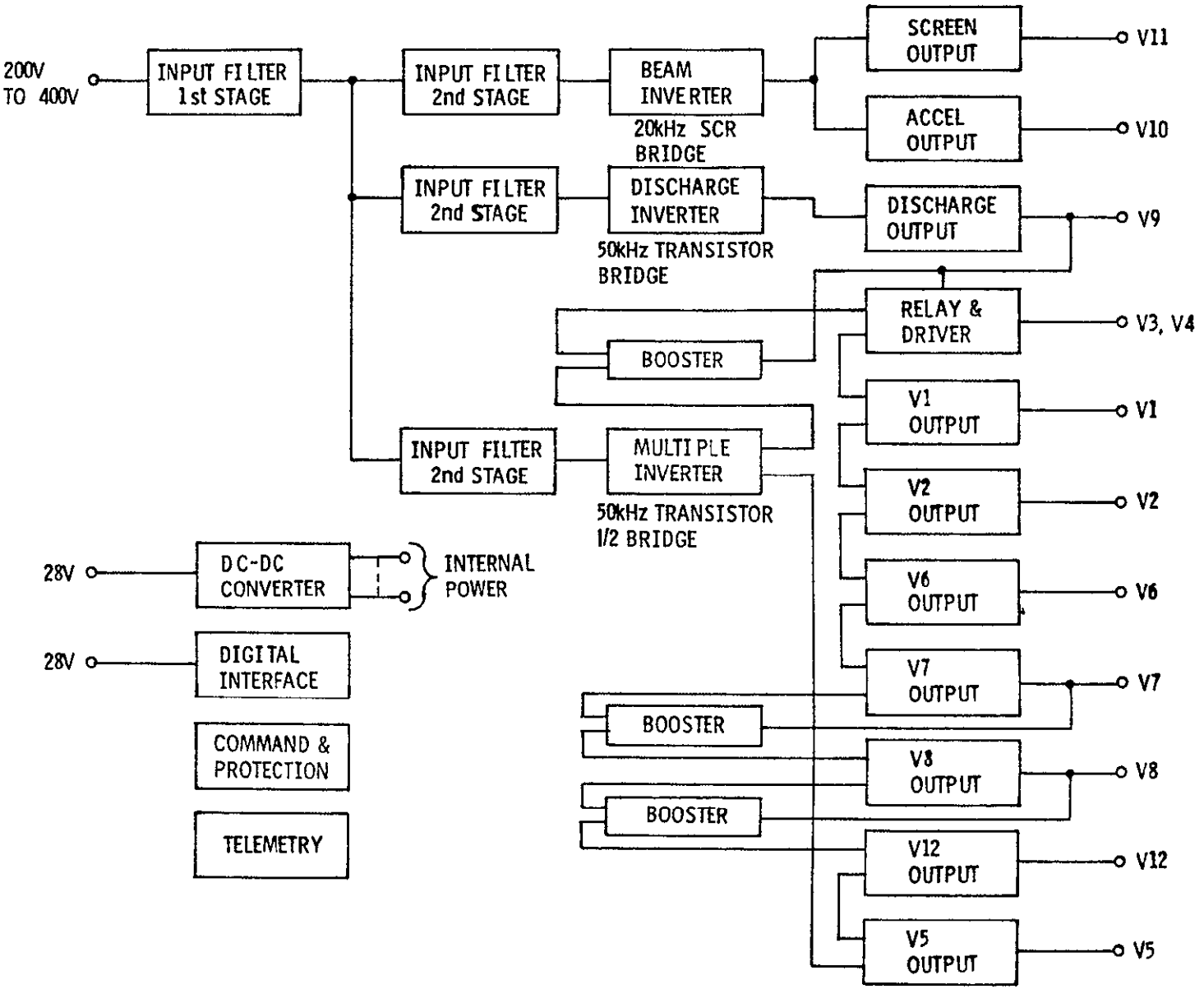


Figure 2-9. Power Processor Block Diagram

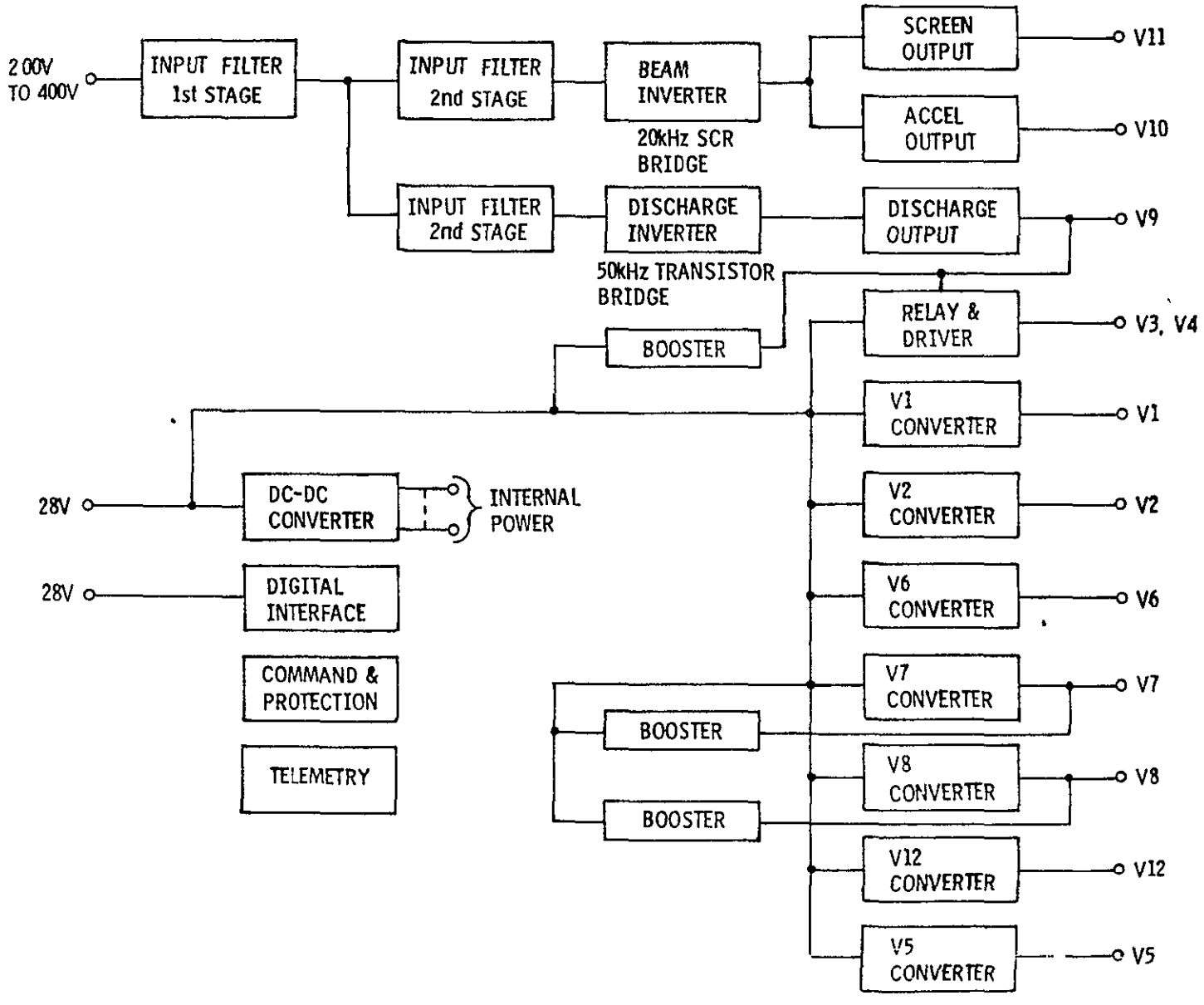


Figure 2-10. Power Processor Block Diagram (200 to 400V and 28V Solar Array Power Distribution)

Table 2-VI Power Processor Estimate - High Voltage System

		PART COUNT	WEIGHT (gms)	LOSSES (W)(2)	EFFIC.	
Beam Inverter (6000W)	Power Stage	81	8893.3	408.42	93.6%	(1)
	SCR Firing	152	165	23.6		
	Series Inverter Control	125	116.45	1.379		
	Regulator	92	120.75	2.121		
	Accelerator Regulator	71	107.5	4.021		
	Beam Total	521	9403.0	439.541		
Discharge Inverter (415W)	Power Stage	33	1639 35	60.64	87.3%	(1)
	Transistor Drive	218	288.6	16.0		
	Series Inverter Control	125	116.45	1 379		
	Regulator	97	131 8	1.082		
	Discharge Total	473	2176.2	79.101		
Low Voltage Supplies	Power Stage	10	207	15.50	46%	(1)
Multiple Inverter (45W)	Controls	319	362.3	10 202		
(Series Inverter)	Outputs - Power	146	1522.85	37.141		
	. Regulators	526	592 9	2 975		
	Multiple Total	1001	2685 05	65 818		
Input Filter		45	4410	20 60		
	Sub Totals	2040	18674 25	605.06	91.4%	
Telemetry		239	686 35	5 528		
Protection		235	186 3	3 00		
Command		52	181 6	2 57		
Interface Unit		91	454	.97		
28V Converter		122	611 8	16 46		
Output power ≅ 6460W	TOTALS	2779	20784.3	633 588	91 07%	

Notes (1) Power stage efficiency only.
(2) Losses at two amp beam current

Table 2-VII Power Processor Estimate - High & Low Voltage System

		PART COUNT	WEIGHT (gms)	LOSSES (W) (2)	EFFIC.
Beam Inverter (6000W)	Power Stage	81	8893.3	408 42	93 6% (1)
	SCR Firing	152	165	23 6	
	Series Inverter Control	125	116.45	1.379	
	Regulator	92	120.75	2.121	
	Accelerator Regulator	71	107 5	4 021	
	Beam Total	521	9403.0	439.541	
Discharge Inverter (415W)	Power Stage	33	1639 35	60.64	87.3% (1)
	Transistor Drive	218	288.6	16.0	
	Series Inverter Control	125	116 45	1.379	
	Regulator	97	131 8	1.082	
	Discharge Total	473	2176.2	79.101	
Low Voltage Supplies	Power Stage	336	1859.2	22.662	66 5% (1)
Multiple Outputs (45W) (Buck-Boost)	Controls	703	733 3	2.963	
	Multiple Total	1039	2592 5	25.625	
Input Filter		45	4385	20.6	
	Sub Totals	2078	18556.7	564 867	91 9 %
Telemetry		239	686 35	5.528	
Protection		235	186 3	3 00	
Command		52	181 6	2 57	
Interface Unit		91	454	.97	
28V Converter		122	611 8	16.46	
Output Power ≅ 6460W	TOTALS	2817	20676 75	593 395	91.6%

Notes: (1) Power Stage Efficiency Only.
(2) Losses at Two Amp Beam Current.

The Table 2-VII shows that Figure 2-10 has the slightly lower electrical component weight of about 110 grams and a higher efficiency of 0.5%. The real efficiency savings occur when the beam current is varied to 1/4 power level and difference between the low voltage supplies improves the overall efficiency. This will be further discussed in Section 3.5, Electrical Design.

2.6 Power Processor Weight-Efficiency Optimization

The optimization of a power processor design is dependent on the design of the spacecraft, basically the solar array and the thermal control system used to reject the heat loss generated by the power processor.

In the solar electric mission, the solar array power capability varies constantly during its mission due to the variation of the distance between the Sun and the spacecraft and makes the optimization more difficult.

Figure 2-11 shows the characteristic optimization curves where the power processor weight is plotted as a function of its losses. The summation of the weight for the power processor, the weight for the solar array due to losses and the weight of the thermal control system to radiate the internal losses is also plotted as a function of the power processor losses. The optimization point is where the power processor weight is equal to 1/2 of the total weight.

For the Halley's Comet Rendezvous mission, the following spacecraft characteristics were estimated·

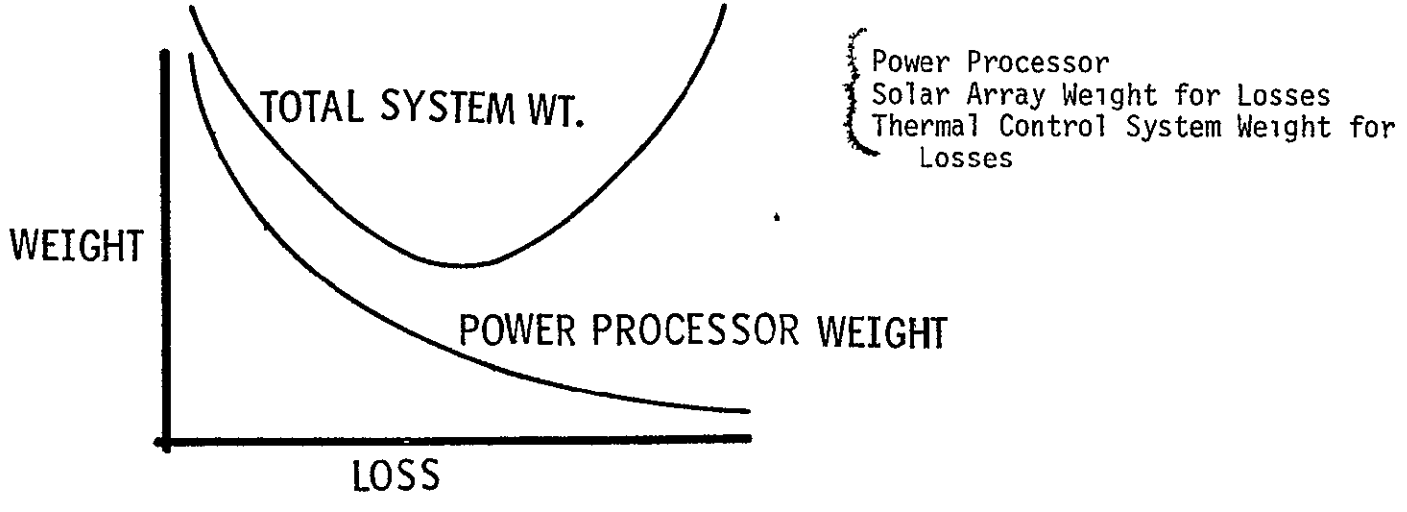
- Solar Array Density (Averaged overflight profile) $\frac{20KG}{KW}$
- Thermal Control System Density $\frac{28KG}{KW}$

The following is an estimate of the preferred power processor configuration design:

- Packaged Weight (2 times component weight) 40KG
- Power Processor Losses 593 Watts
- Solar Array Weight for Losses $\frac{20KG}{KW}$ x .593KW) = 11.8KG
- Thermal Control System Weight $\frac{28KG}{KW}$ x .593KW) = 16.6KG

The total power processor, solar array and thermal control system weight is 68.8KG and the ratio of power processor weight total is .587. This ratio is off the 0.5 point and shows that a different design could reduce the overall weight.

Figure 2-11. Power Processor Weight-Efficiency Optimization



The estimated optimum solution is:

Total weight	65KG
Power processor weight	32.5KG
Power processor losses	677W
Power processor efficiency	90.5%

A redesign of the magnetic components would easily provide these optimum characteristics and provide a thrust system weight savings of 3.8KG per ion thruster.

This example shows the optimization procedure and is dependent on the accuracy of the solar array density and the thermal control system density.

3 0 BASELINE DESIGN

After the review and approval of the preferred configuration by the NASA Project Office on 18 August 1977, a more detailed electrical and mechanical design of the power processor was performed for a beam power rating of 2.2KW and 6KW Both the electrical, mechanical and thermal interfaces were reviewed and incorporated into the preliminary design concept

3 1 Power Distribution System

Figure 3-1 illustrates the power distribution system selected by NASA Lewis that was used to establish the necessary electrical interfaces for detailed electrical design of power processor. Power from the high power solar array is supplied to the main power distribution unit at ±100 to ±200VDC Electromagnetic interference filters control the reflected AC noise that can be returned from the spacecraft load to the large solar array surfaces

Solid state DC breakers are used with each ion engine power processor to protect against any power line failure or failures in the power processor power electronics

The unregulated solar array bus also goes through separate solid state breakers to two redundant DC-DC converters that generate 28VDC @ 1500W output to supply the low voltage electronics of the ion engine power processor and to the spacecraft

By eliminating the DC-DC converter, and using a 28VDC solar array, the power processor design would still be compatible with the new power distribution system

Figure 3-2 illustrates the schematic of the 28V DC-DC converter It is a half bridge thyristor series resonant inverter operating at 20kHz Table 3-I summarizes the component weight, losses and part count for the electrical design Preliminary estimate of efficiency is 88% and should be constant for a load range of 25 to 100% during the expected mission flight profile

During launch, 28VDC power will be supplied directly from the shuttle interim upper stage (IUS) and provides necessary 28VDC power for the ion engine power processors and to the spacecraft.

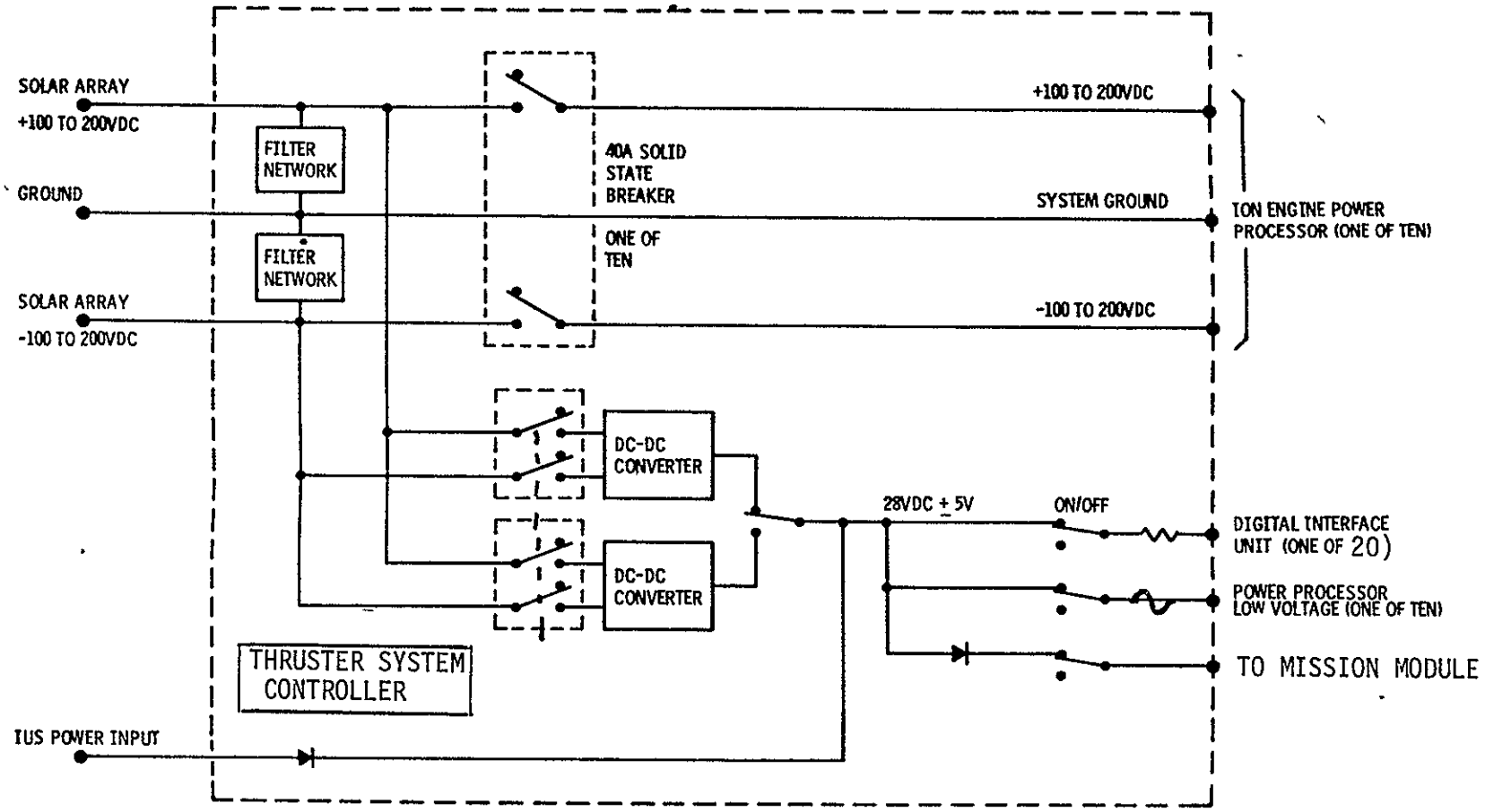


Figure 3-1. Power Distribution System Block Diagram

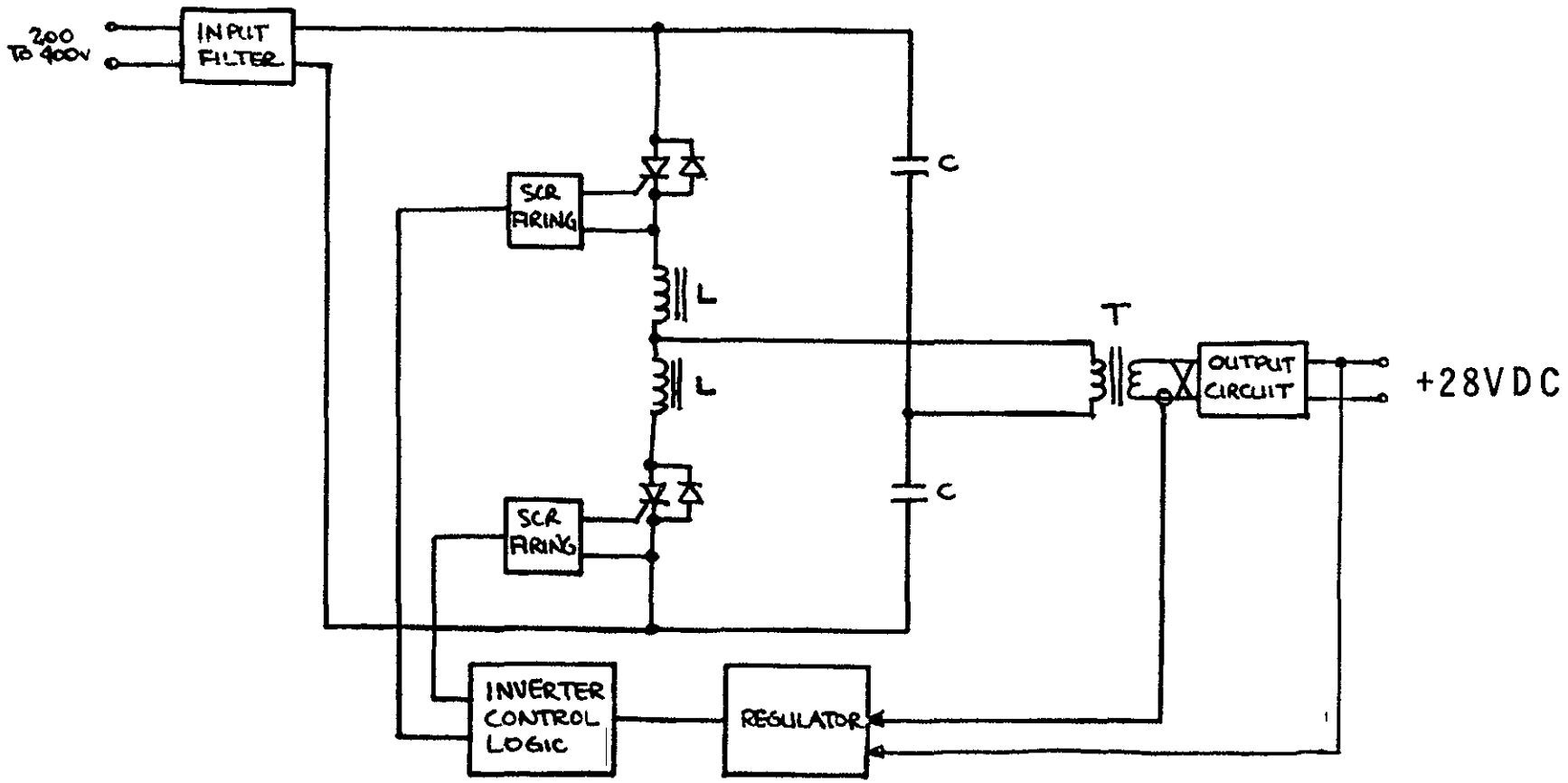


Figure 3-2. Schematic of DC-DC Converters Used to Generate 28VDC Power Bus

Table 3-I Summary of 28VDC Bus Converter (1.5KW Output Power Rating)

	COMP. WT. gms	LOSSES Watts	PART COUNT
Power Stage (Input Filter Series Inverter, Output Transformer Rectifier and Filter)	6677.3	186.601	55
SCR Firing	90.83	13.331	78
Series Inverter Control	76.83	.980	140
Regulator	82.44	.325	72
Bias Supply	314.41	2.714	91
	7241.81 gm	203.951 W	436

88% EFFIC

Continued system study is necessary to identify all of the interfaces to ensure a compatible electrical propulsion spacedraft with a Shuttle/IUS Launch Vehicle.

A redundant microprocessor thrust system controller performs all power control and management, Bi-Mod control, thrust control and failure analysis.

The features of this system configuration are:

- ±100 to ±200VDC supplies the high power loads
- 28VDC power distribution for EMC control and ease of integration of all low power equipment
- Interfaces with Bi-Mod, Mission Module, and IUS
- Filter networks control high power bus impedance for EMC control
- Solid state breakers provide the necessary protection and fault clearing of ±100 to ±200VDC for the power system
- Thrust system controls the flow of power and the operation of the ion engines
- On/Off control and fault clearing for 28VDC loads.

Both hardware and software development work are necessary for the power distribution unit in the following areas:

a) Power Distribution System
b) Thrust System Controller
c) Solid State Breakers
d) DC-DC Converter Line Regulators

3.2 Command System

The overall spacecraft command system must include the electric propulsion module and its power processor modules.

Figure 3-3 shows the basic block diagram for the command system and the inter-relationship of the spacecraft central computer, thrust system controller, located in the power distribution unit and electric propulsion Bi-Mod. The ring bus command line allows for open in the cabling and still allows total system operation.

With the use of microprocessors, most of the operational controls can be located at the Bi-Mod and we can limit the amount of data that must be transferred and processed by the thrust system controller and the spacecraft computer.

A reliability analyses should be performed on the proposed configuration to identify the level of redundancy that should be maintained in the command system.

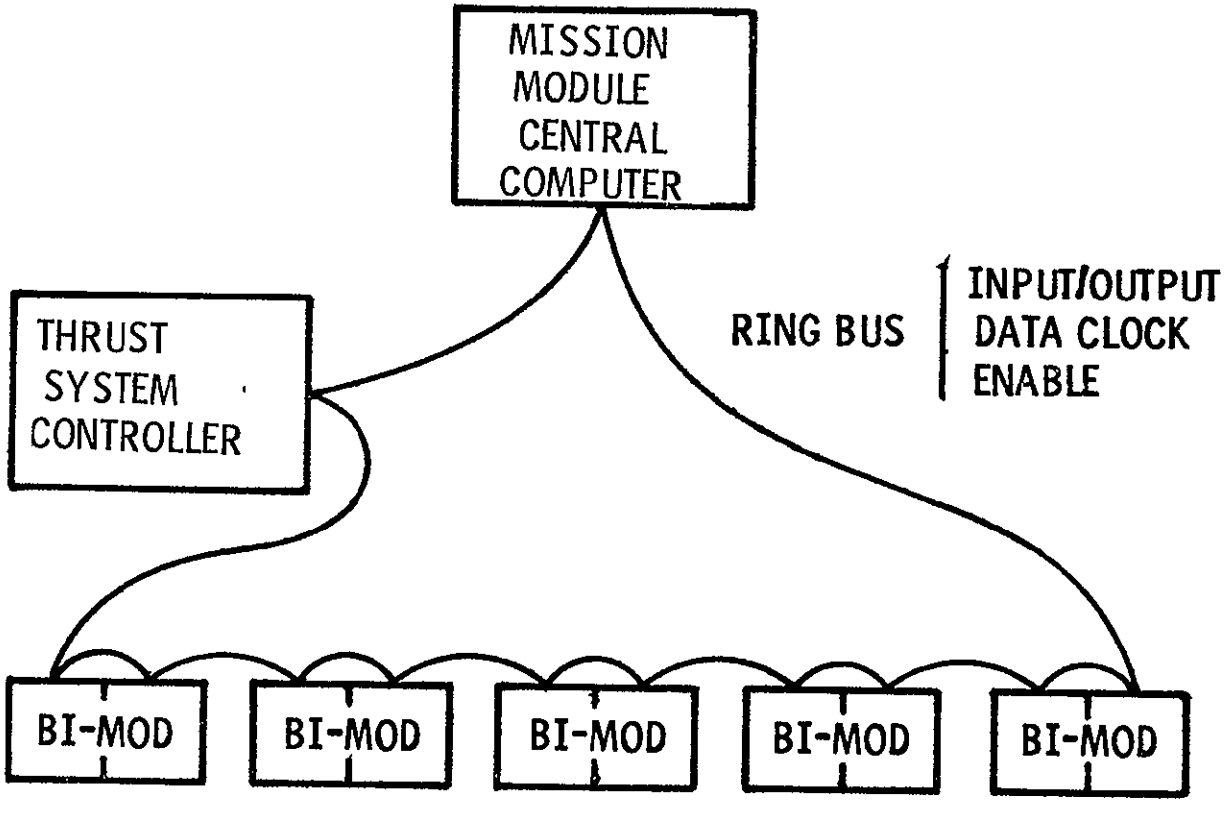


Figure 3-3. Command System Block Diagram

3.3 Bi-Mod Configuration

Figure 3-4 shows the block diagram for the electric propulsion Bi-Mod where two ion engines and two power processors form a complete mechanical subassembly. All of the electrical interfaces are illustrated in the diagram:

- Serial command data (high speed)
- 28VDC for microprocessor interface unit
- Low speed parallel command & data between the interface unit and the power processor for high noise immunity
- ±100V to ±200VDC solar array input to each power processor
- 28VDC for the low level power processor electronics
- Power processor output lines to the ion engine gimbals Gimbals controlled by Thrust System Controller.

Each power processor is dedicated to its own ion engine and there is no sharing of electric functions between the power processors.

The ion engines and power processors share only the mechanical structure and heat pipe/radiator assembly to affect a overall system weight saving.

Figure 3-5 shows the interfaces between the microprocessor digital interface unit and the two power processors. The input data to the microprocessor is high speed serial data. The outputs to the power processor are low speed parallel data lines which extra filtering can be added to provide high noise immunity for the power processor control electronics.

Table 3-II summarizes the features of this proposed digital system.

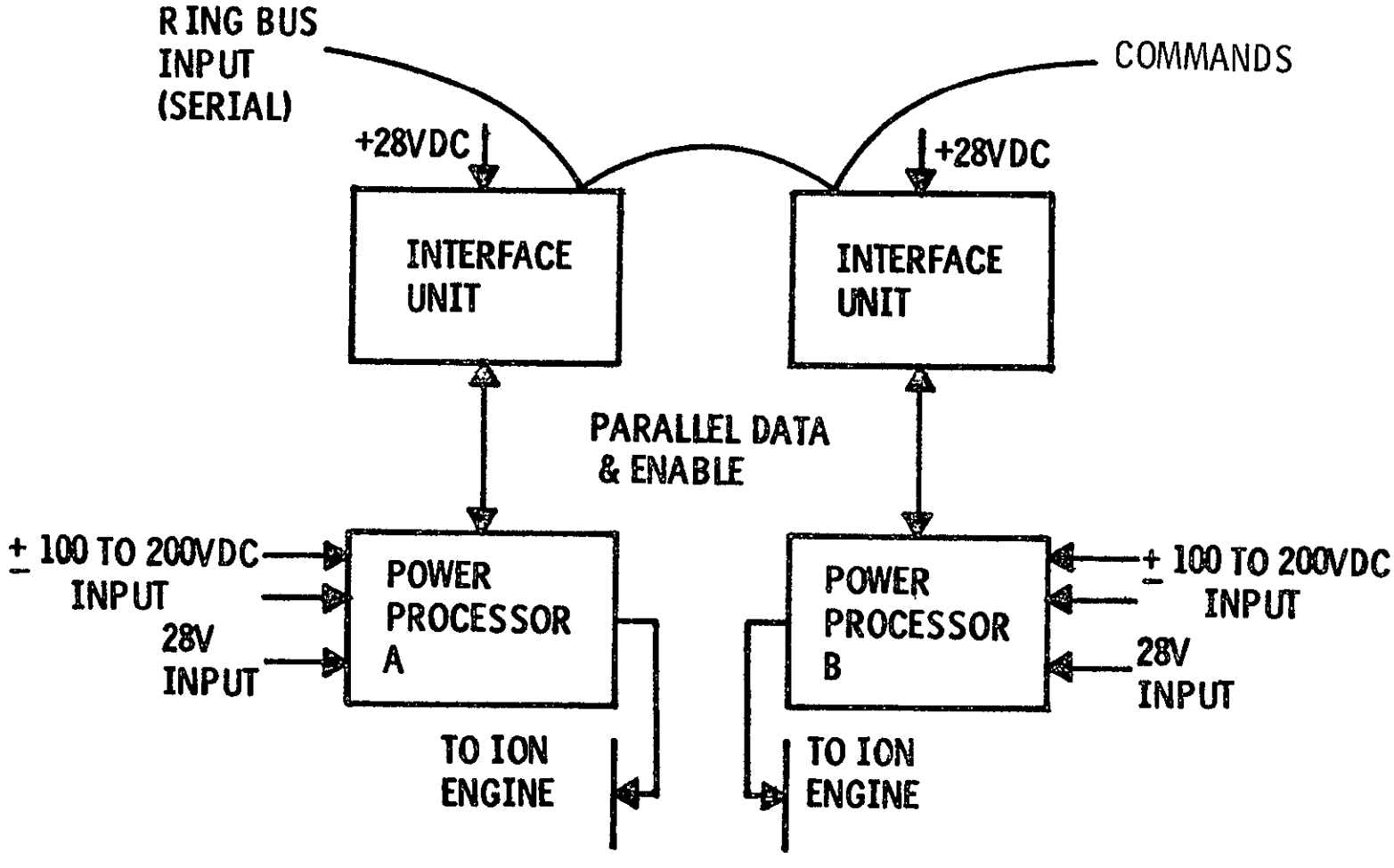


Figure 3-4. Bi-Mod Configuration Blodk Diagram

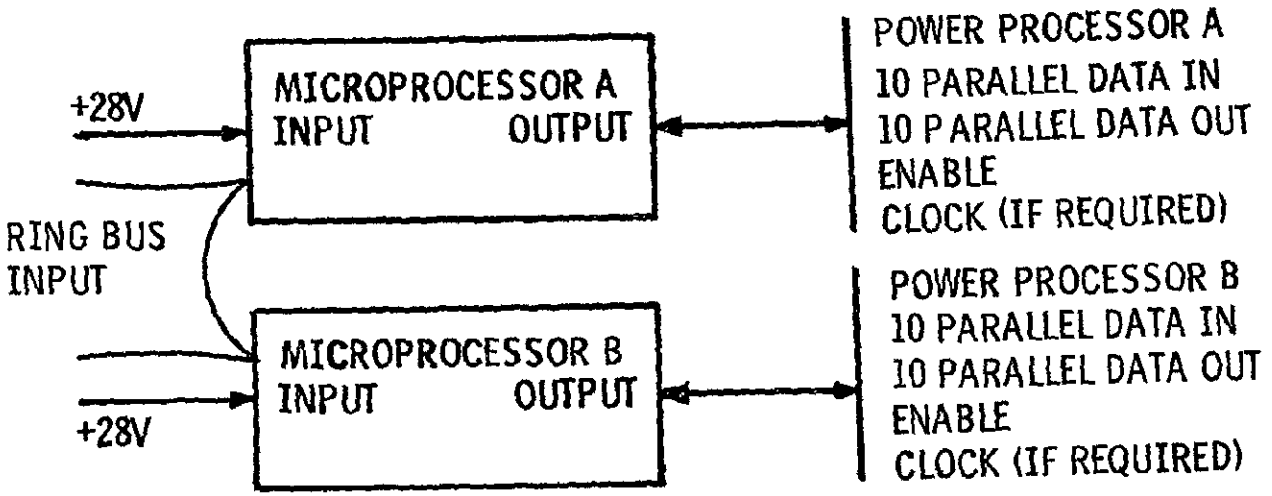


Figure 3-5 Bi-Mod Interface Unit Configuration

Table 3-II Features of Bi-Mod Interface Unit Configuration

- Separate Interface Unit (Microprocessor) for Each Ion Engine
- 28V Power can Turn On/Off Each Interface Unit
- All Output Lines Filtered
- 10 Parallel Outputs (3 for Address & 7 for Data)
- Optical Isolation for Input and Output
- High Speed Input Data/Low Speed Output Data

3.4 Power Processor Block Diagram

Figure 3-6 illustrates the basic block diagram for the Extended Performance Power Processor. The 200 to 400VDC bus supplies power through a common first stage input filter and separate 2nd stage input filters to the beam inverter and the discharge inverter, respectively.

28VDC supplies power to the low level outputs each with their own dedicated dc/dc converter that provides the necessary regulation, control and isolation for the different ion engine outputs.

A separated dc/dc converter supplies internal control logic power.

A microprocessor digital interface unit controls the total power processor through the command, protection and telemetry electronics:

- to startup an ion engine
- to throttle the ion engine thrust
- to change power processor set point to be compatible with ion engine thrust
- to recycle the outputs during ion engine arcs or overloads
- to provide an orderly shut-down of the ion engine

The discharge supply V9 is used during startup to supply power to V3 and V4 outputs and reduce the power processor part count.

Separate boosters are used for the V9, V7 and V8 outputs to initiate a discharge in the mercury plasma.

Figure 3-7 presents the grounding system designed into the power processor electronics to eliminate high ground loop currents that could damage the low level control electronics during ion engine overload or shorts.

Both optical coupling and transformer magnetic isolation are used to provide the necessary separation between.

Microprocessor Digital Interface Unit
PPU Signal Electronics
PPU Power Stage Electronics
Ion Engine

A separate ground return wire goes from each area to a single point ground located in the electric propulsion system interface module which connects the solar array and its drive system to the Bi-Mod mechanical assembly.

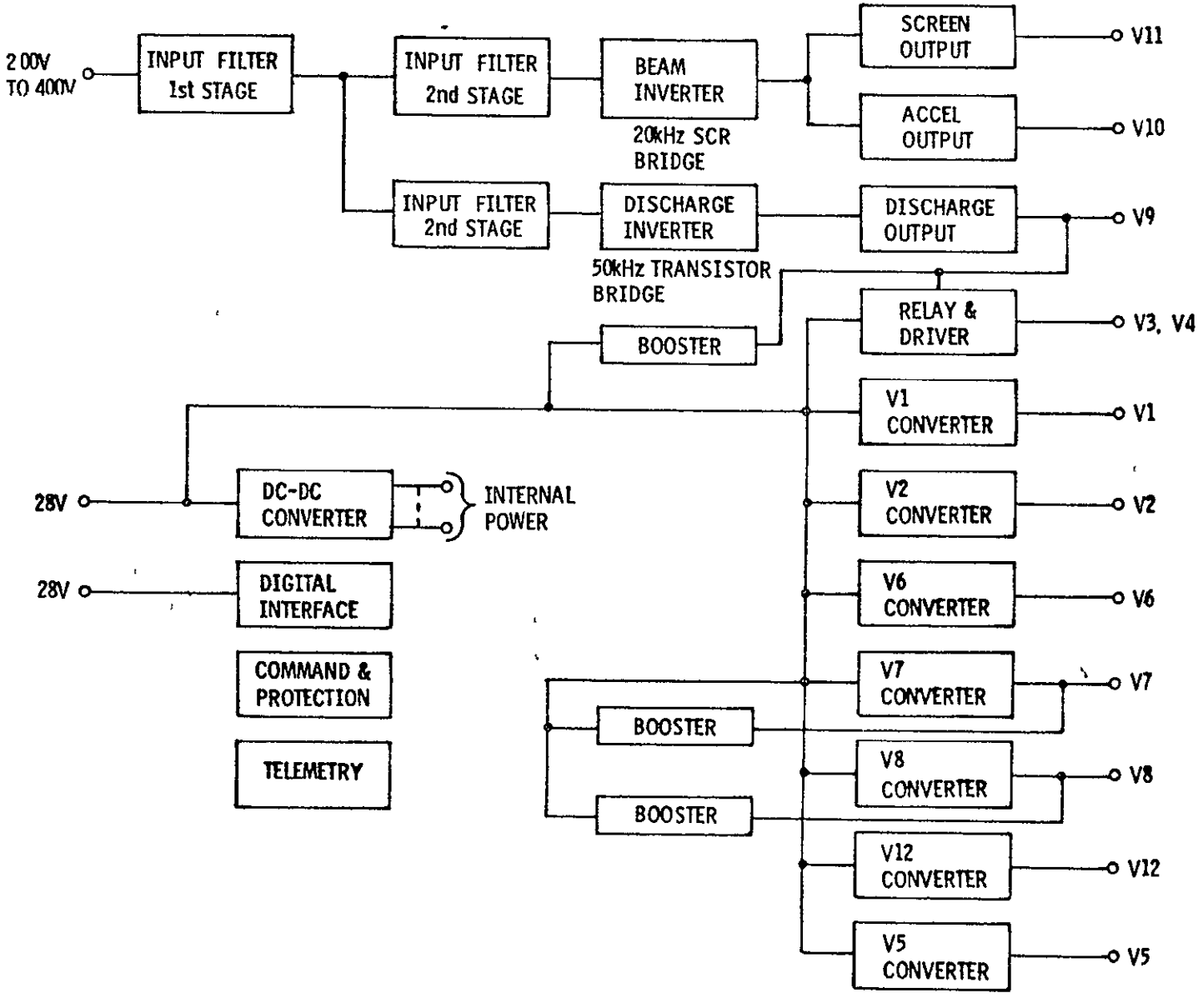


Figure 3-6. Electric Propulsion Power Processor Block Diagram

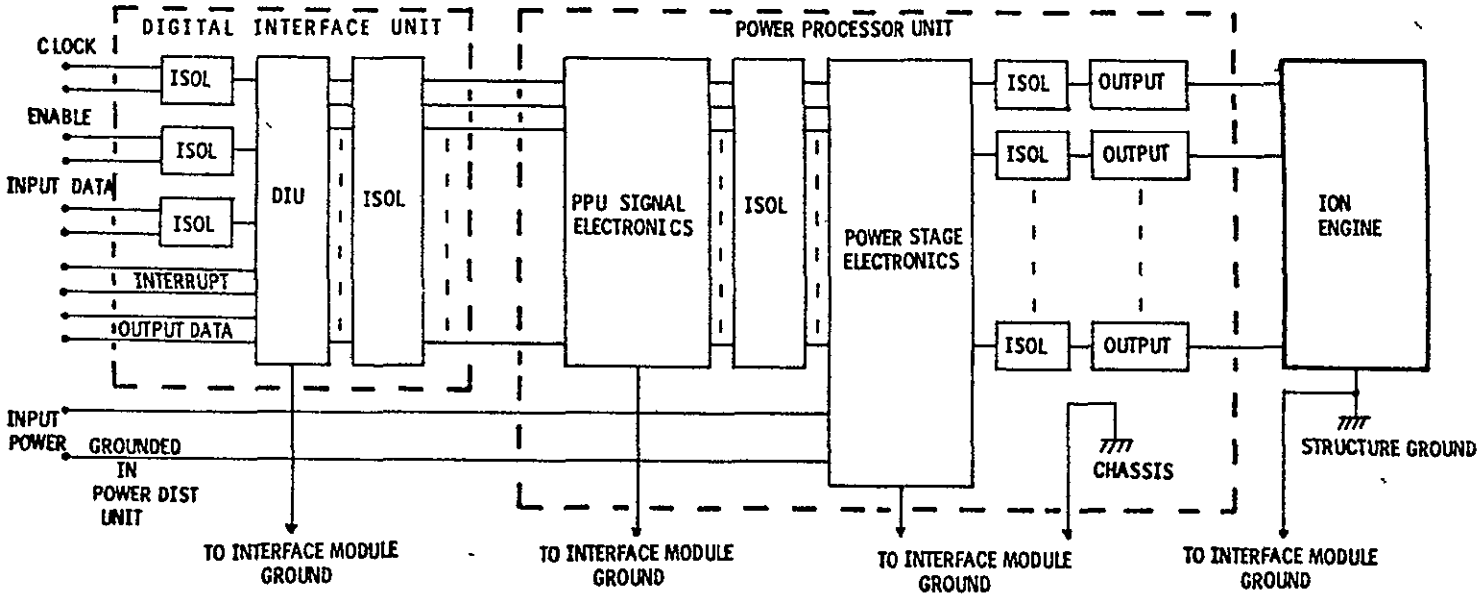


Figure 3-7. Power Processor Grounding System Block Diagram

This basic grounding system has been used on three other electric propulsion power processor breadboard designs and the Transmitter Experiment Package without any operational problems. This ground isolation technique does have a slight weight and loss penalty.

3.5 Electrical Design

A detailed electrical design was performed based on the power processor block diagram shown previously in Figure 3-6. Two different designs were performed in support of the following programs:

- Halley Comet Mission Power Processor with a 6KW Beam Supply
- Alternate Electric Propulsion Missions using a Power Processor with the Standard 2.2KW Beam Supply

3.5.1 Input Filter

Figure 3-8 shows the schematic for the input filter for the Halley Comet Power Processor. It includes a two stage L-C power filter. The first stage capacitor contains series resistance to provide the necessary damping for the high efficiency input filter during input power bus disturbances. Each output load such as the discharge inverter and beam inverter has its own 2nd stage inductor. The second stage capacitors are located near the switching semiconductor located at each inverter. Table 3-III summarizes the input filter design details. This filter design was scaled down for the Alternate Electric Propulsion Missions.

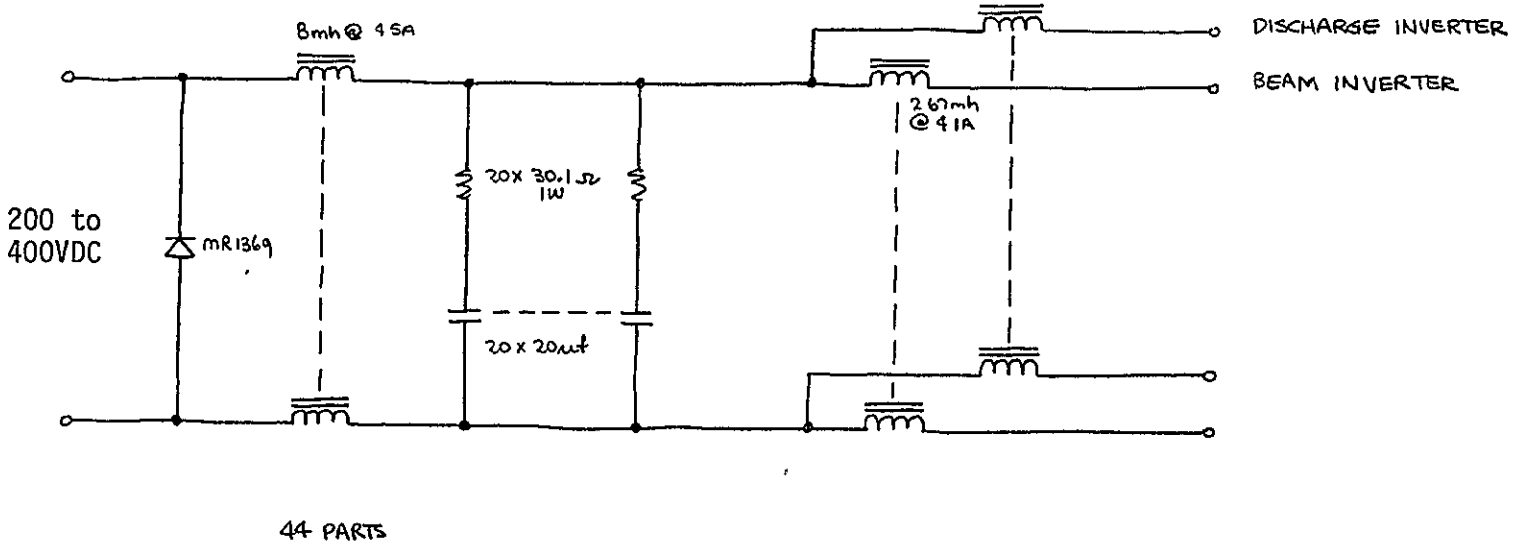


FIGURE 3-8 Input Filter

Table 3-III Design Summary - Input Filter (6KW)

	WEIGHT	LOSSES	PART COUNT
INDUCTOR - FIRST STAGE	1750	10.48	1
CAPACITORS - FIRST STAGE	1750	- -	20
INDUCTOR - SECOND STAGE-BEAM	750	9.67	1
INDUCTOR - SECOND STAGE-DISCHARGE	102	.83	1
RESISTORS	1	- -	20
DIODE	15.1	- -	1
	4368.1 gm	20.98W	44

3.5.2 Beam Supply

Figure 3-9 shows the schematic of the thyristor bridge inverter for a 3KV - 2A screen output. It includes four 9.5μh series resonant inductors and a single 2.15μF series resonant capacitor.

The power transformer feeds the main output power through a diode bridge and output filter capacitor composed of four 0.5μF capacitors. The output resistor network limits the peak surge currents that can flow through the output shorts.

A low power transformer is connected across the main power transformer output winding to develop the negative accelerator potential. The split of transformer reduced the winding and insulation complexity for the main power transformer.

Figure 3-10 is the schematic of thyristor firing network. The firing network provides both turn-on pulse for the thyristor gate-cathode and turn-off pulse to ensure the fast turn-off of the power thyristor.

Figure 3-11 is the redesign of the series resonant inverter control logic using T^2L digital logic. The basic operation and block diagram of the control logic is presented in NASA CR-134785 Power Processor for a 30cm Ion Thruster. The thyristor current signal going to zero determines the end of each power half cycle. The series capacitor voltage sensor protects the power stage from excessive capacitor voltage during transient operation

Figure 3-12 is the redesign of regulator control electronics using T^2L digital logic and low power operational amplifiers. It includes (1) the screen voltage regulator with ASDTIC feedback loop from the output filter capacitors and commands a method to adjust the output voltage level, (2) primary winding current regulator and (3) accelerator output current limit which protects during an output overload.

Table 3-IV presents the design summary for the 6 kW Beam Power Supply.

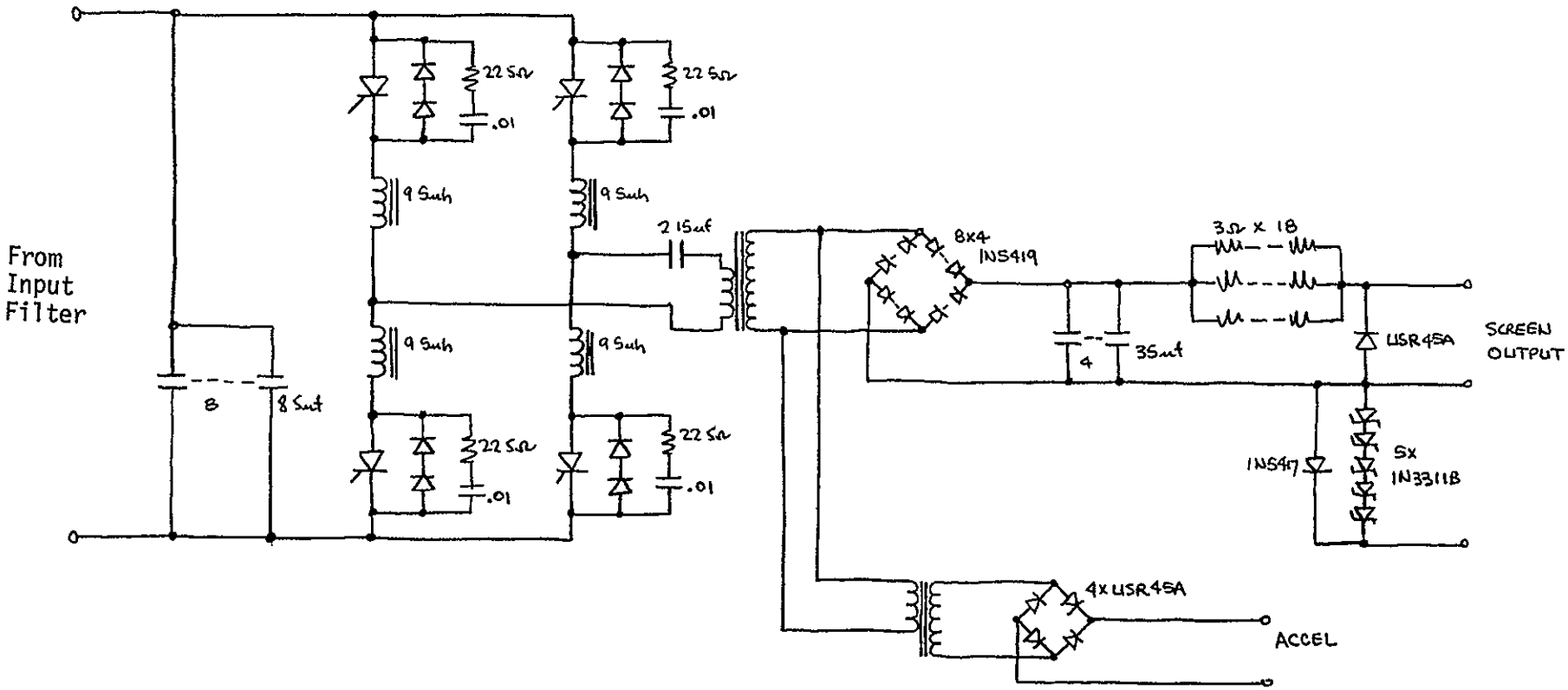


Figure 3-9 6KW Bridge Series Resonant Beam Inverter

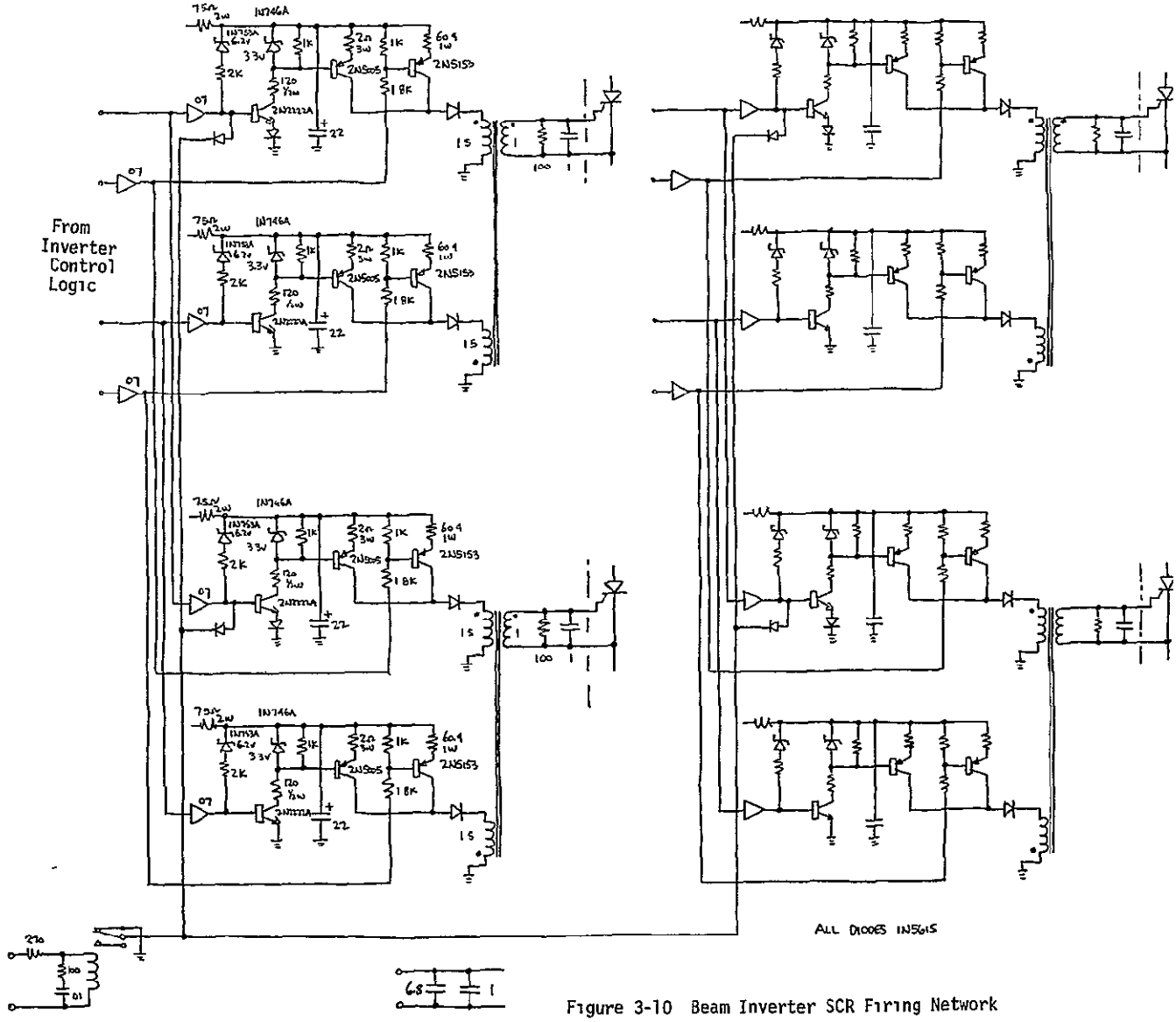


Figure 3-10 Beam Inverter SCR Firing Network

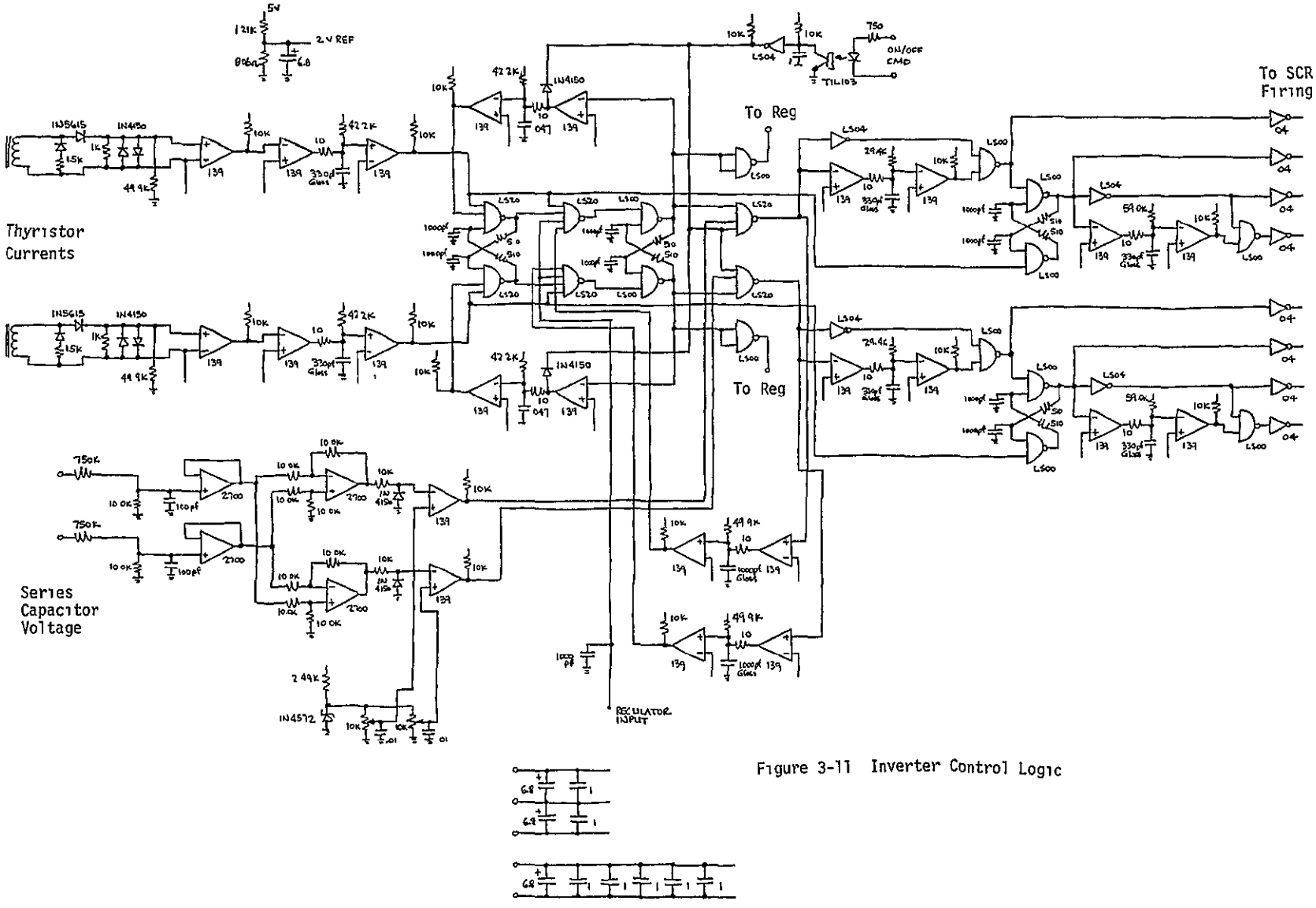


Figure 3-11 Inverter Control Logic

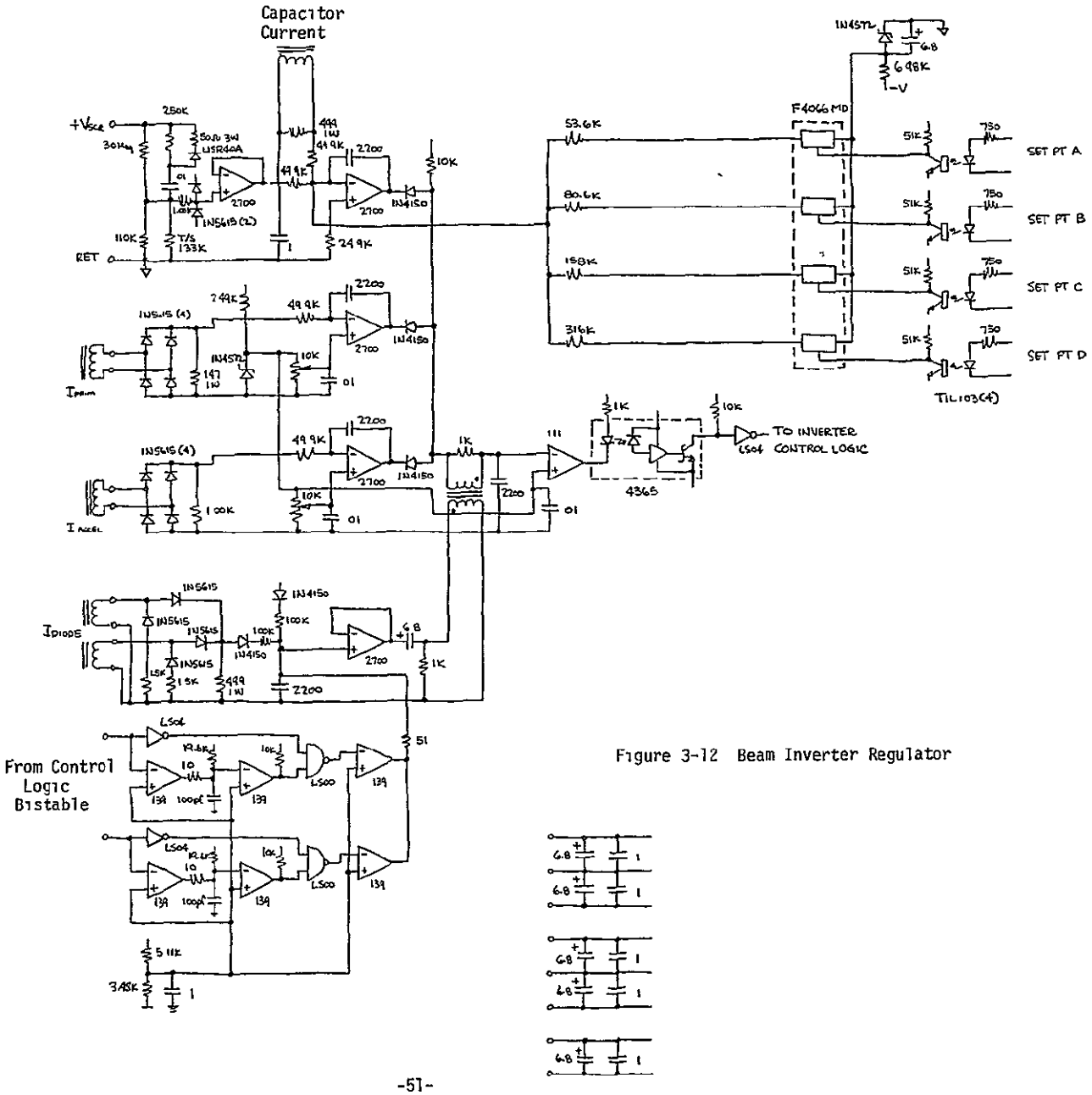


Figure 3-12 Beam Inverter Regulator

Table 3-IV Design Summary - Beam Inverter
SCR Bridge - 6KW

	Component Weight	Losses	Part Count
POWER STAGE	9388.1	408.6	106
SCR FIRING	173.85	26.251	148
SERIES INVERTER CONTROL	76.83	.980	140
REGULATOR	123.47	1.320	118
ACCELERATOR REGULATOR	89.78	2.104	50
	9852.03 gm	439.255W	562

3.5.3 Discharge Supply

Figure 3-13 presents the schematic for the discharge supply. It is a 50kHz transistor full bridge series resonant inverter. The series resonant inductor is 72μh and the series resonant capacitor is 0.14μF.

Figure 3-14 shows the schematic for the transistor drive network It includes proportional basedrive current and reverse turn-off current.

Figure 3-15 is the control logic for transistorized inverter. It is designed with T^2L digital logic and is very similar to beam inverter control logic shown in Figure 3-11, except that the interface with transistor drive network is changed.

Figure 3-16 is the discharge output regulation. It includes three regulation signals (1) maximum discharge output voltage (2) discharge current as a function of command reference, and (3) primary current limit for peak output power control.

Figure 3-17 is the schematic of the discharge booster circuit that is used to initiate the mercury arc in the discharge chamber during ion engine startup. The power stage used is a buck/boost converter.

Table 3-V summarizes the discharge supply characteristics.

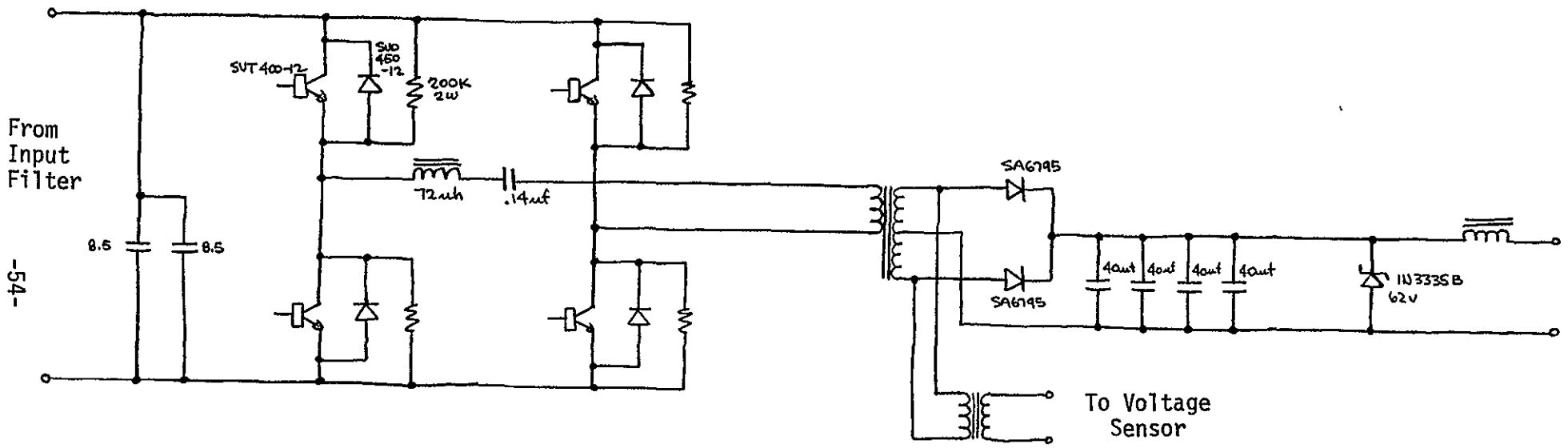
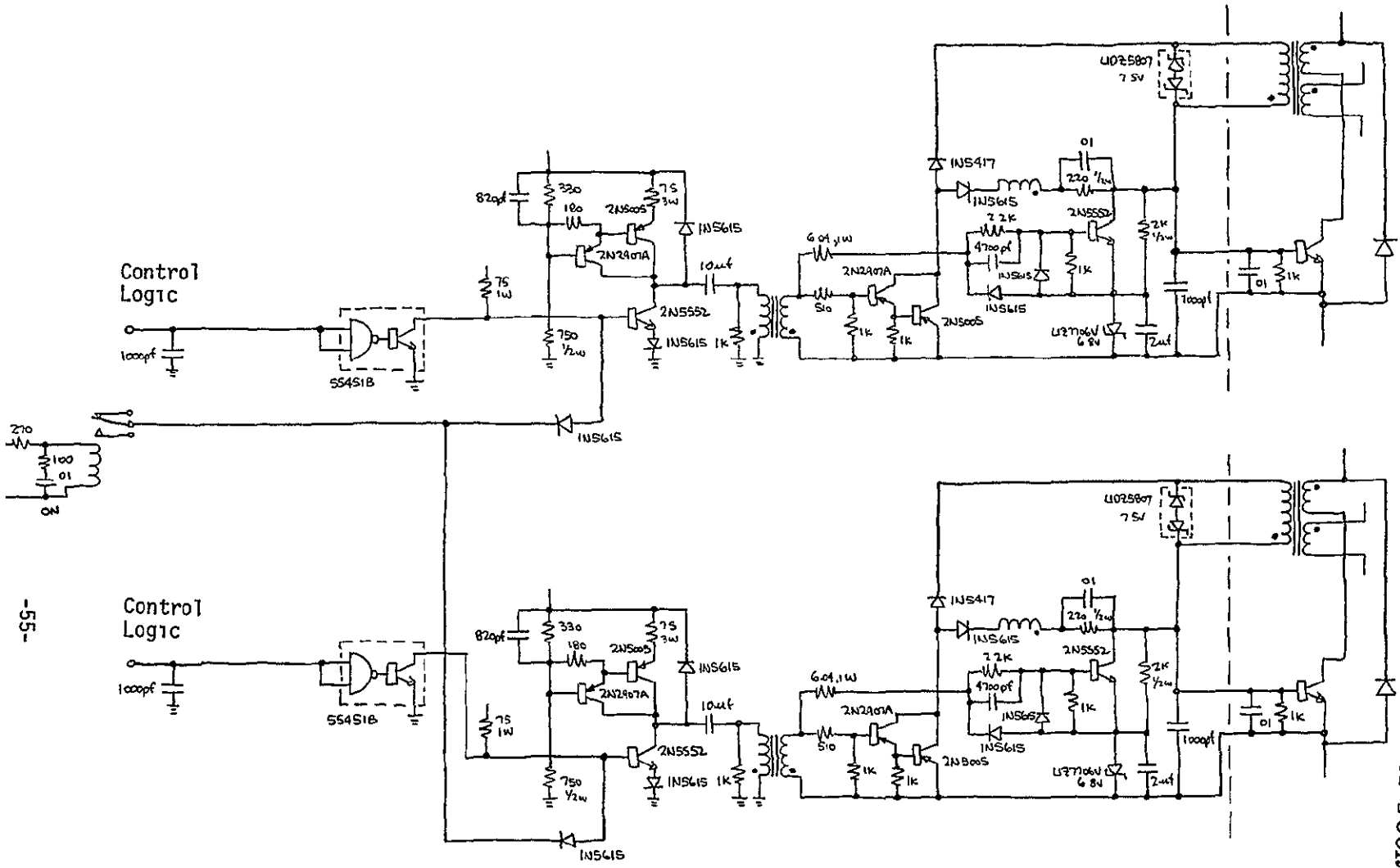


Figure 3-13 Discharge Inverter Power Stage
Transistor Bridge



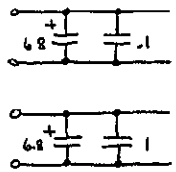


Figure 3-14 Discharge Inverter Transistor Drive Network

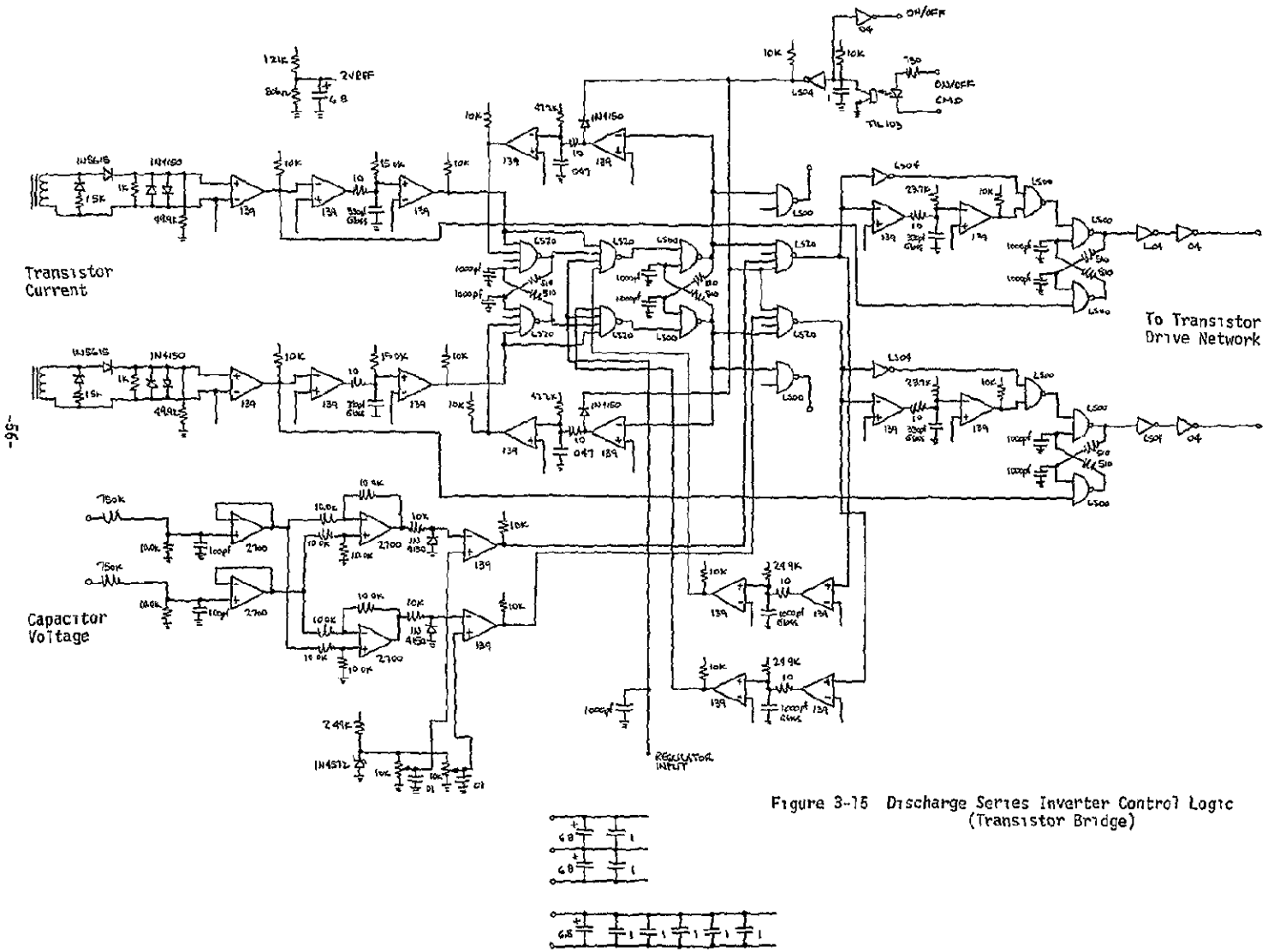


Figure 3-15 Discharge Series Inverter Control Logic (Transistor Bridge)

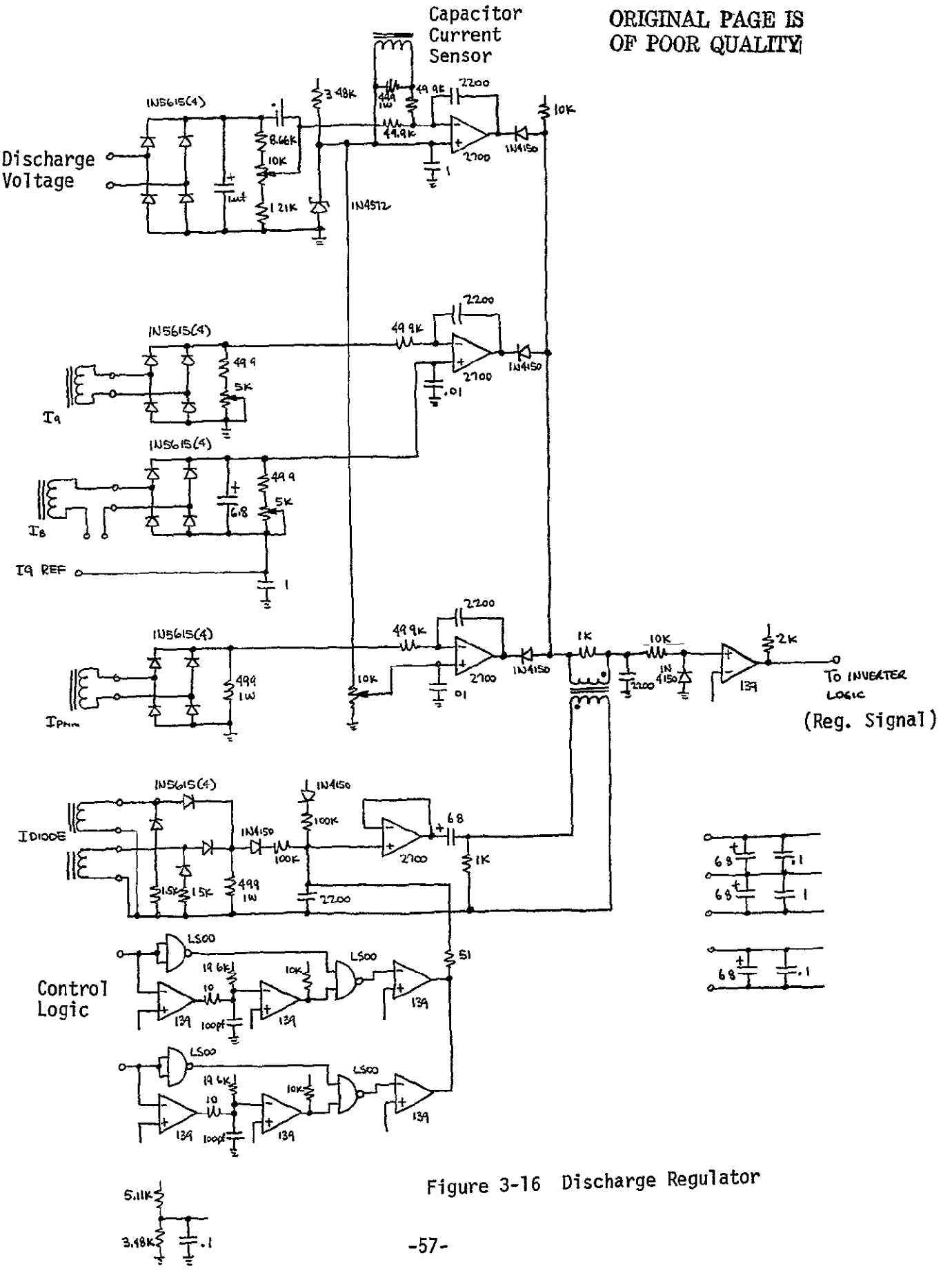


Figure 3-16 Discharge Regulator

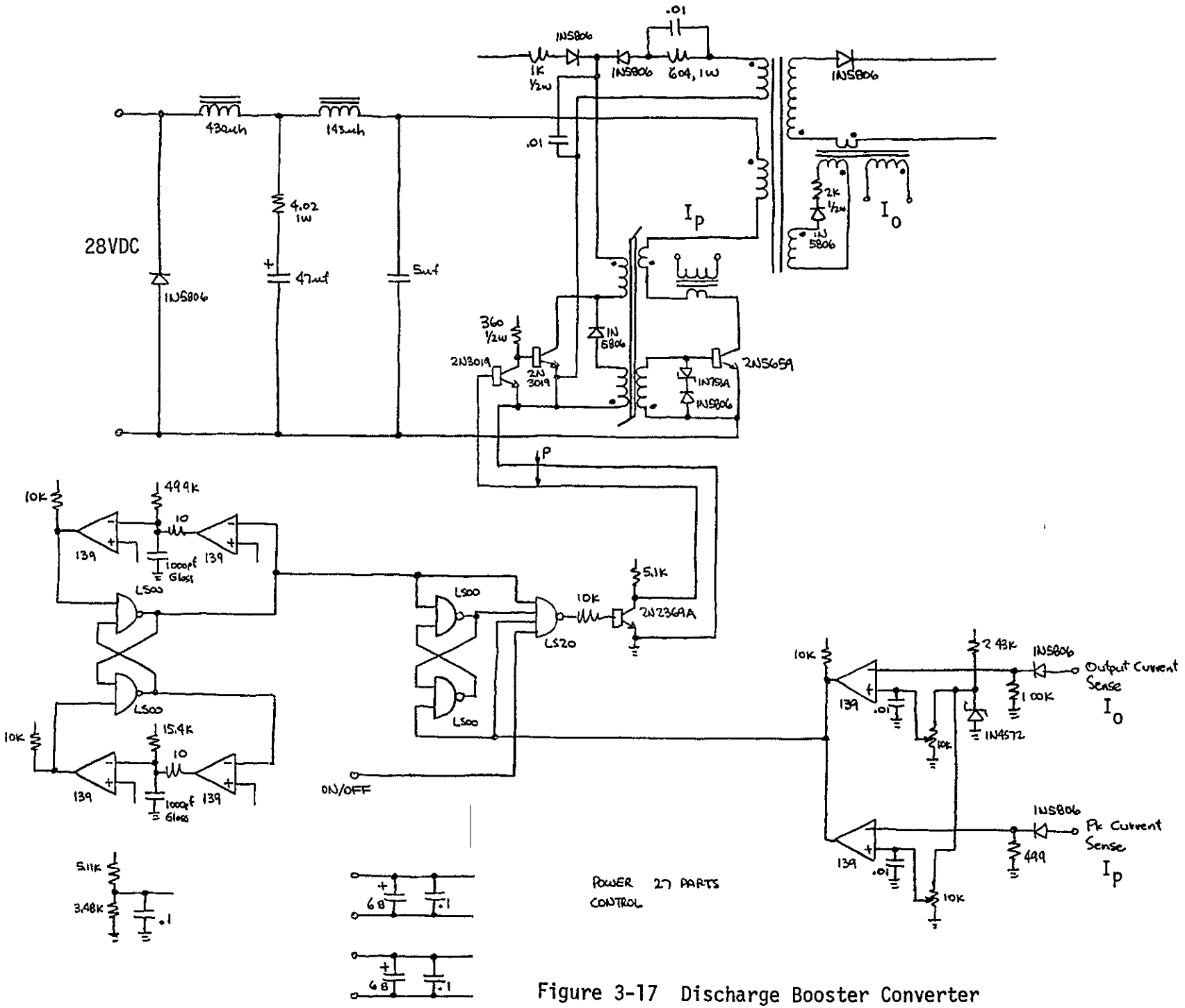


Figure 3-17 Discharge Booster Converter

Table 3-V Design Summary - Discharge Inverter
50kHz Transistor Bridge - 815W Max. (500W Nom)*

	WEIGHT	LOSSES *	PART COUNT
POWER STAGE	1493.6	77.54	28
TRANSISTOR DRIVE	243.17	16.990	167
SERIES INVERTER CONTROL	71.03	.924	130
REGULATOR	113.87	.493	97
BOOSTER	134.01	.783	59
	2055.68gm	96.73W	481

3.5.4 Low Voltage Supplies

The low voltage supplies include the following:

- V1
- V2
- V6
- V5
- V7 and Booster
- V8 and Booster
- V12
- Relay Driver

Auxiliary electronics necessary for the low voltage supplies include the clock which is a common timing unit for all supplies and ramp which is used for the output regulator stability. All low level control electronics use T^2L digital electronics and low power operational amplifiers to reduce the overall power drain necessary for the control electronics.

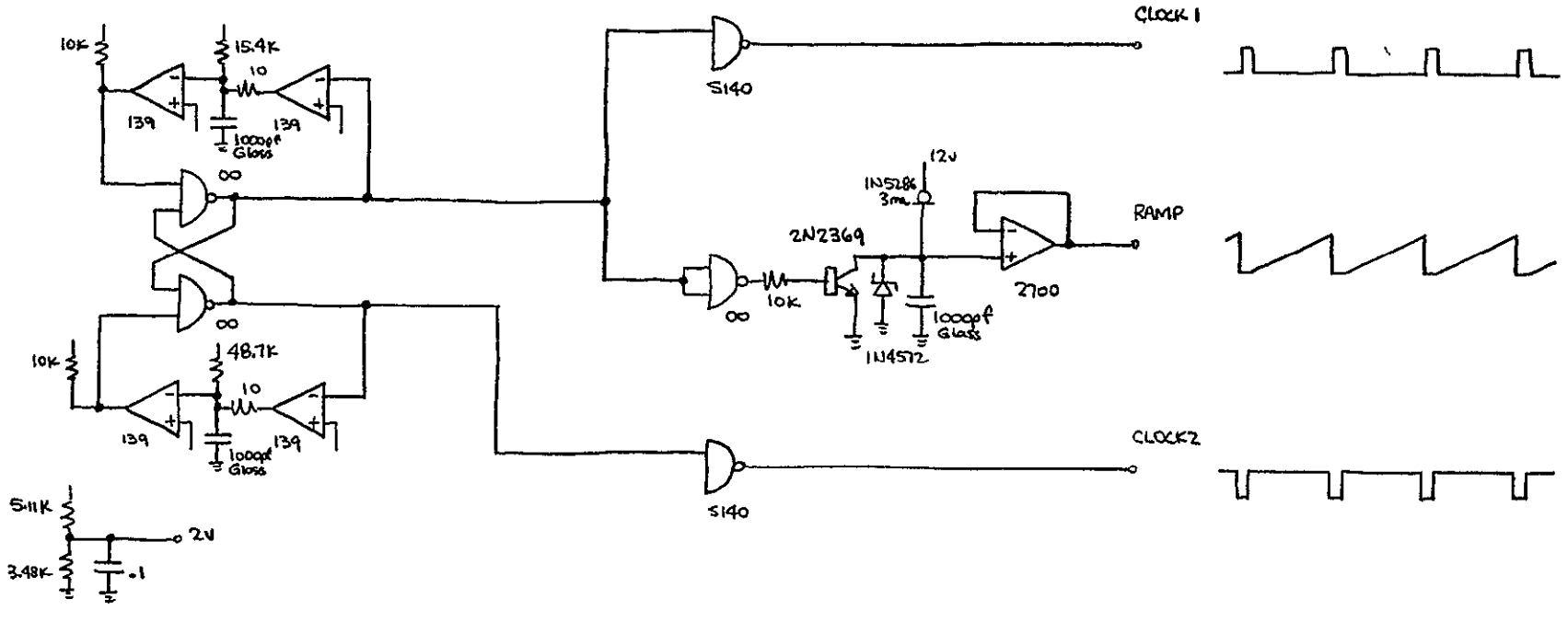
Figure 3-18 is the schematic of the master oscillator with a basic frequency of 25kHz and the ramp generator for output regulator stability.

Only two typical outputs will be presented in the following discussion. All power stages use the buck/boost DC-DC converter. Figure 3-19 is the schematic of the power stage for V1 main vaporizer supply. It contains a two stage input filter, energy recovery network to shape the power transistor switching characteristics, proportional basedrive control, peak current sensor and output overcurrent protection.

Figure 3-20 is the schematic of the V1 output regulator. It includes (1) maximum output voltage limiter, (2) overcurrent limiter and (3) main ion engine feedback loop that controls the vaporizing power as a function of the ion engine output beam current. The feedback loop includes all the necessary ion engine frequency compensation networks.

Figure 3-21 is the schematic of the V7 output and its high voltage booster which is used to initiate an arc during an ion engine startup. One buck boost circuit is used as the power stage and a second buck boost circuit is used as the high voltage booster.

Figure 3-22 is the schematic for both the output regulator and booster control electronics. The output regulator includes (1) maximum output voltage limiter and (2) output current regulator with commandable operational reference set points.



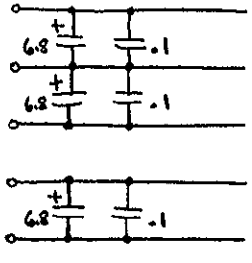


Figure 3-18 Multiple Buck Boost Converter
Master Oscillator & Ramp Generator

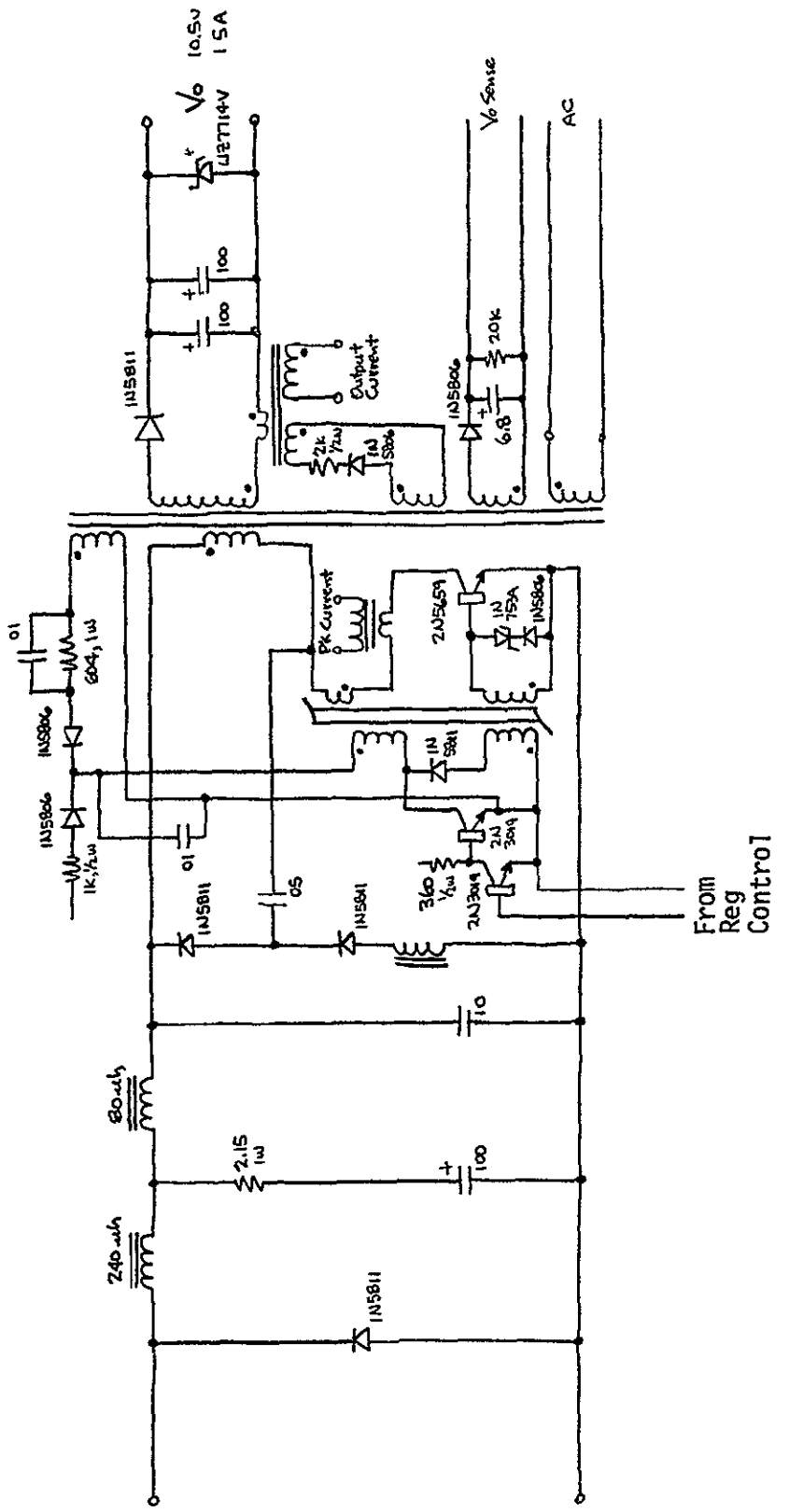


Figure 3-19 V1 Output

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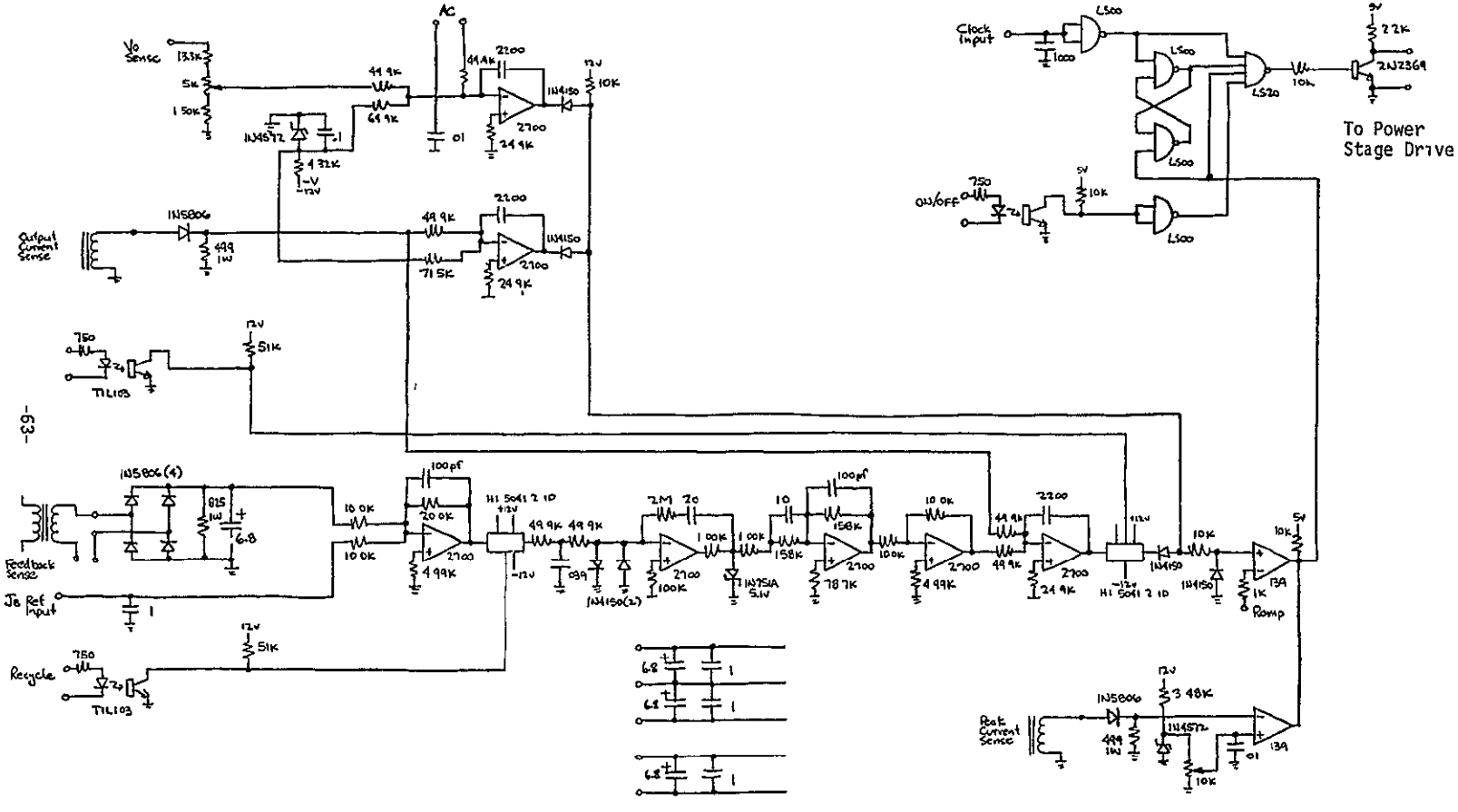

Figure 3-20 V1 Regulator

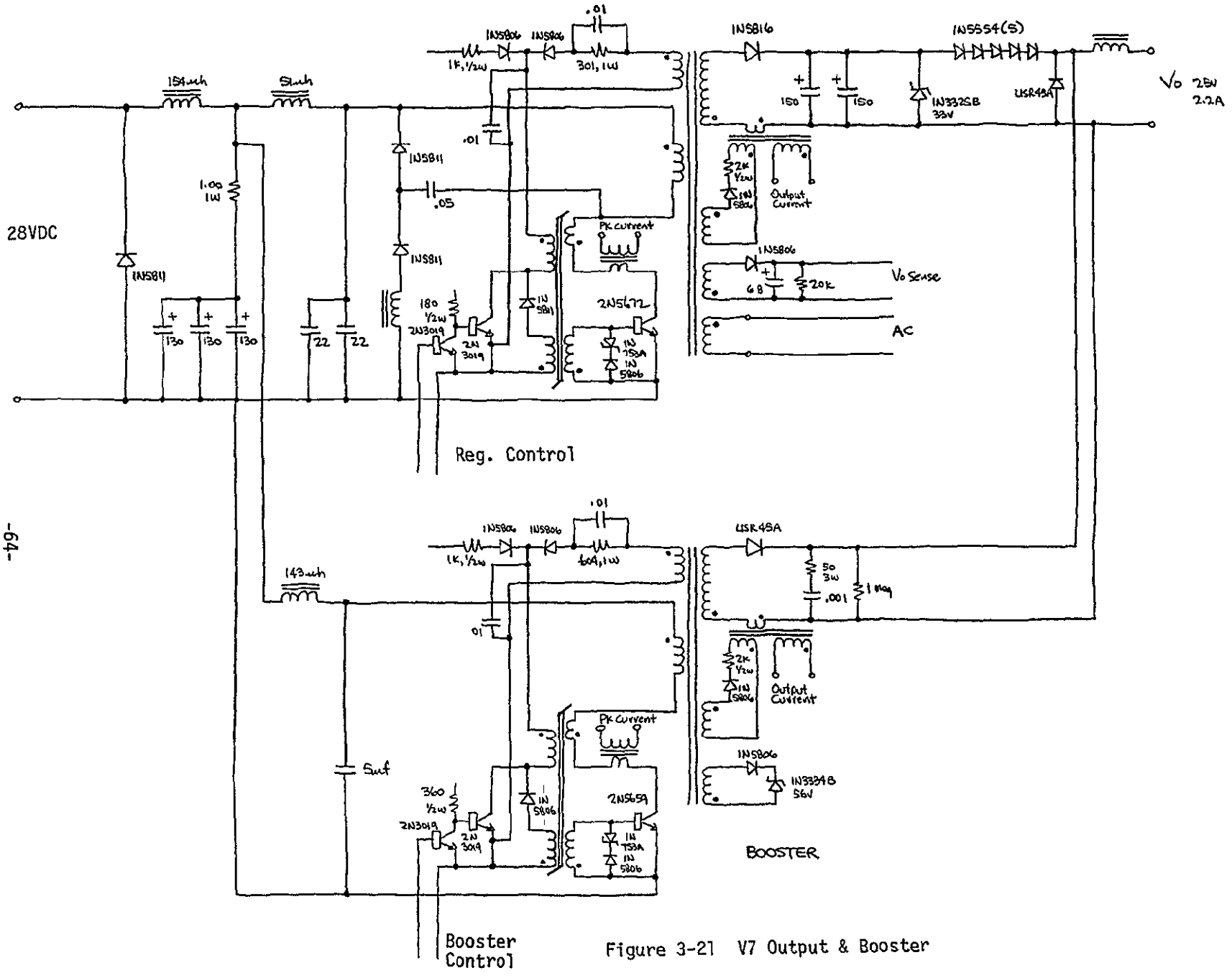

Figure 3-21 V7 Output & Booster

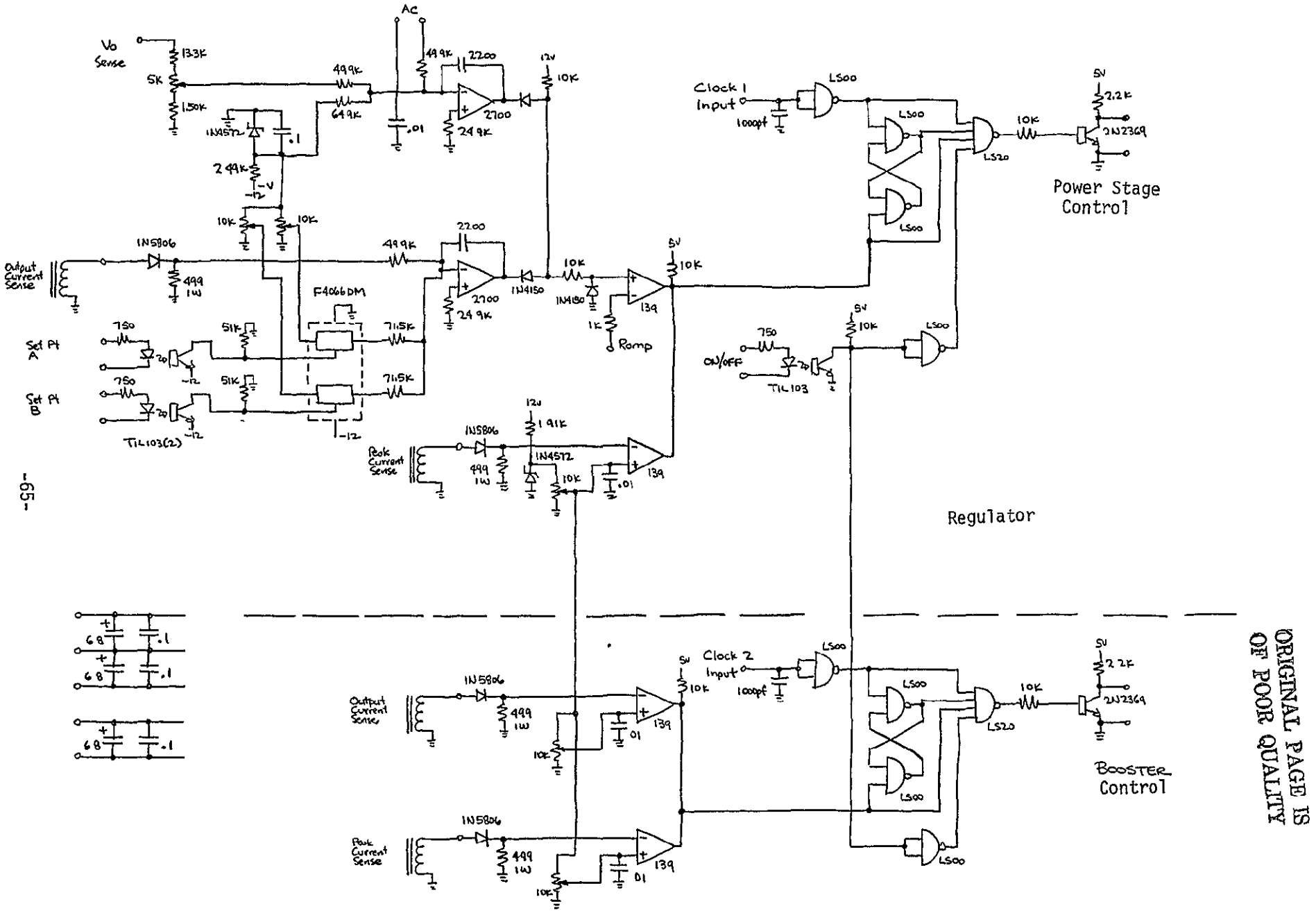

Figure 3-22 V7 Regulator

Figure 3-23 is the schematic for the relay driver that connects the V9 supply to the ion engine V3 and V4 outputs. These outputs are floating at 3KV and therefore the output power transformer has 3KW insulation between primary and secondary output power winding.

Table 3-VI summarizes the design data for all of the low voltage outputs. The design does not include any component or circuitry redundancy.

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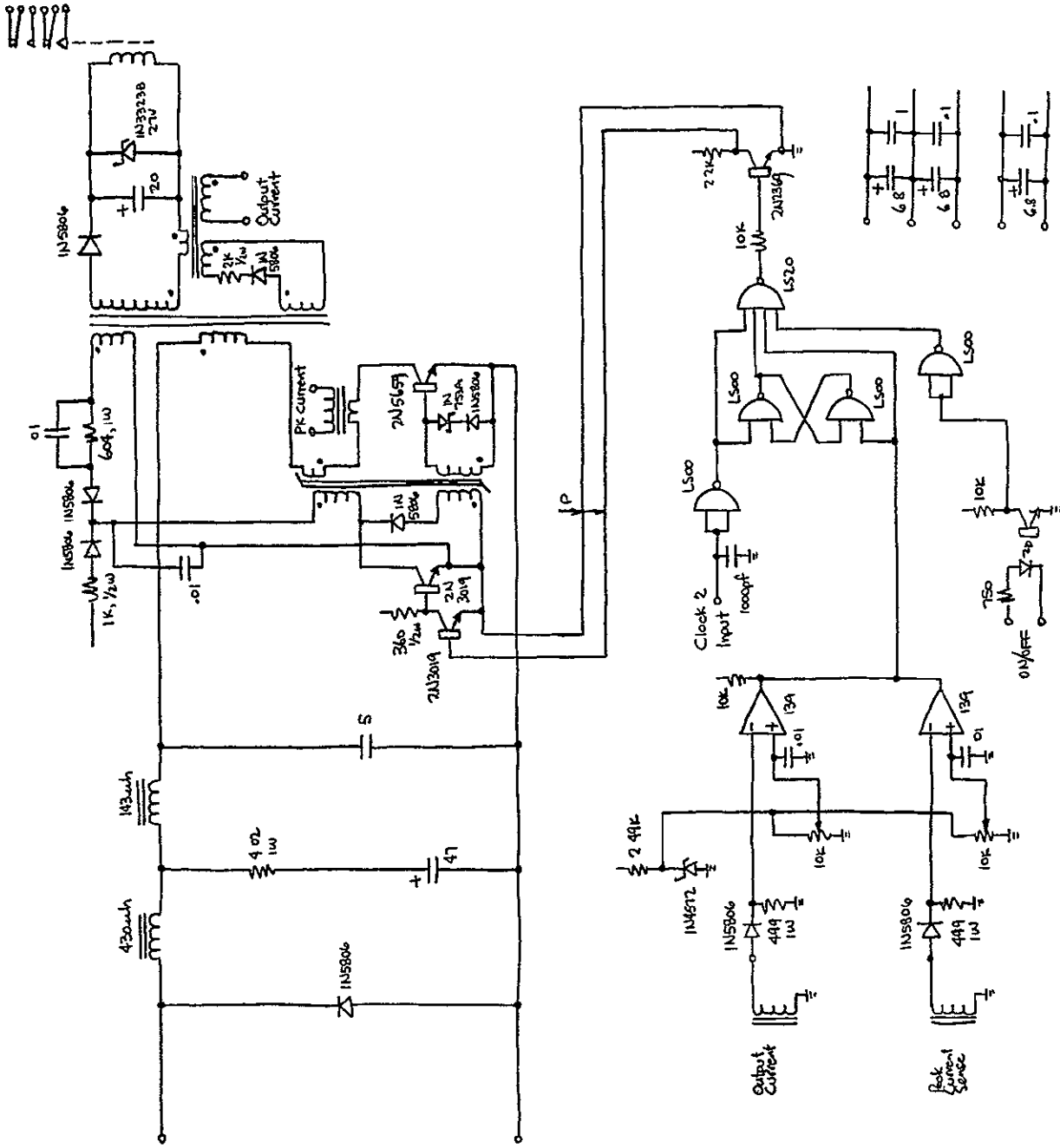


Figure 3-23 Relay Driver

Table 3-VI Design Summary - Low Level Outputs

SUPPLY	WEIGHT		LOSSES		PART COUNT	
	POWER	CONTROLS	POWER	CONTROLS	POWER	CONTROLS
V1	169.85	93.08	1.159	.424	34	100
V2	169.85	93.27	1.121	.667	34	105
V6	169.85	94.27	1.122	.599	34	109
V5	487.5	40 43	.300	.295	38	59
V7 and Booster	854.72	67.12	11.901	.387	69	77
V8 and Booster	271.47	61.62	3.438	.319	61	68
V12	208.5	37.39	2.658	.221	33	52
Relay Driver	163.49	28.42	2.864	182	27	28
Clock and Ramp.	- -	15.29	- -	.103	-	25
	2495.23	530.89	24.563	3.197	330	623
OUTPUT POWER ≈ 45W	3026.12gm		27.76W		953	

3.5 5 Telemetry

Critical power source, power processor and ion engine operating parameters are conditioned for transfer back to ground or spacecraft central computer.

Figure 3-24 is the schematic of a 2kHz squarewave or oscillator that feeds AC power to all of the telemetry monitoring circuits. Output series resistors limits the maximum power that can be drawn from the oscillator in case of a failure in the telemetry monitoring circuits.

Figure 3-25 shows the telemetry monitoring used for the beam supply It includes both voltage and current monitors. The voltage monitor uses a voltage divider and operational amplifier voltage follower, which generates an output current proportional to the operational input voltage. This output current controls a two core series connected saturable reactor amplifier.

The saturable reactor stage obeys the following control law: $N_c I_c = N_g I_g$, where $N_c I_c$ is the control ampere turns and $N_g I_g$ is the output gate ampere turns. This output current is rectified and filtered and a voltage is developed across the output resistor proportional to the input signal current.

The current monitor circuit uses just the series connected saturable reactor and its operation performance is the same as in the voltage monitor.

These saturable reactor circuits are excited at 2kHz because of the low output error (less 0.5% of full scale).

The input and output signals are isolated by means of the magnetic winding. The input signal can be at any ground or elevated at high voltage and the output can be common to telemetry command system ground.

Table 3-VII summarizes all the design data for all of the telemetry monitoring equipment in the power processor design.

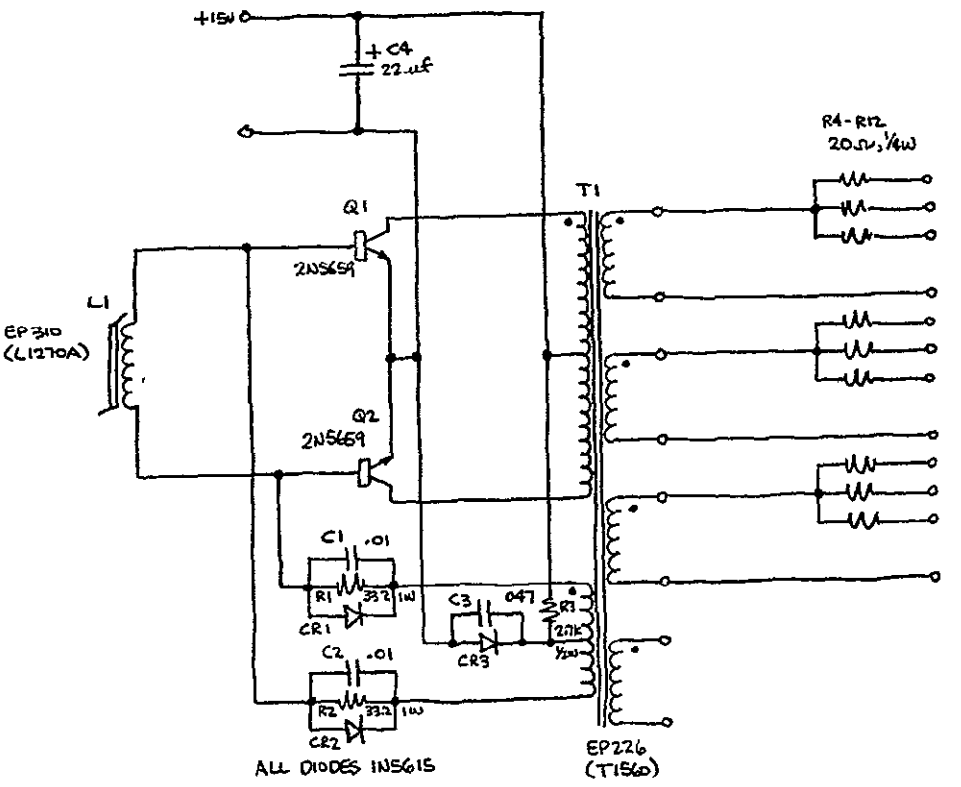


Figure 3-24 TLM Oscillator

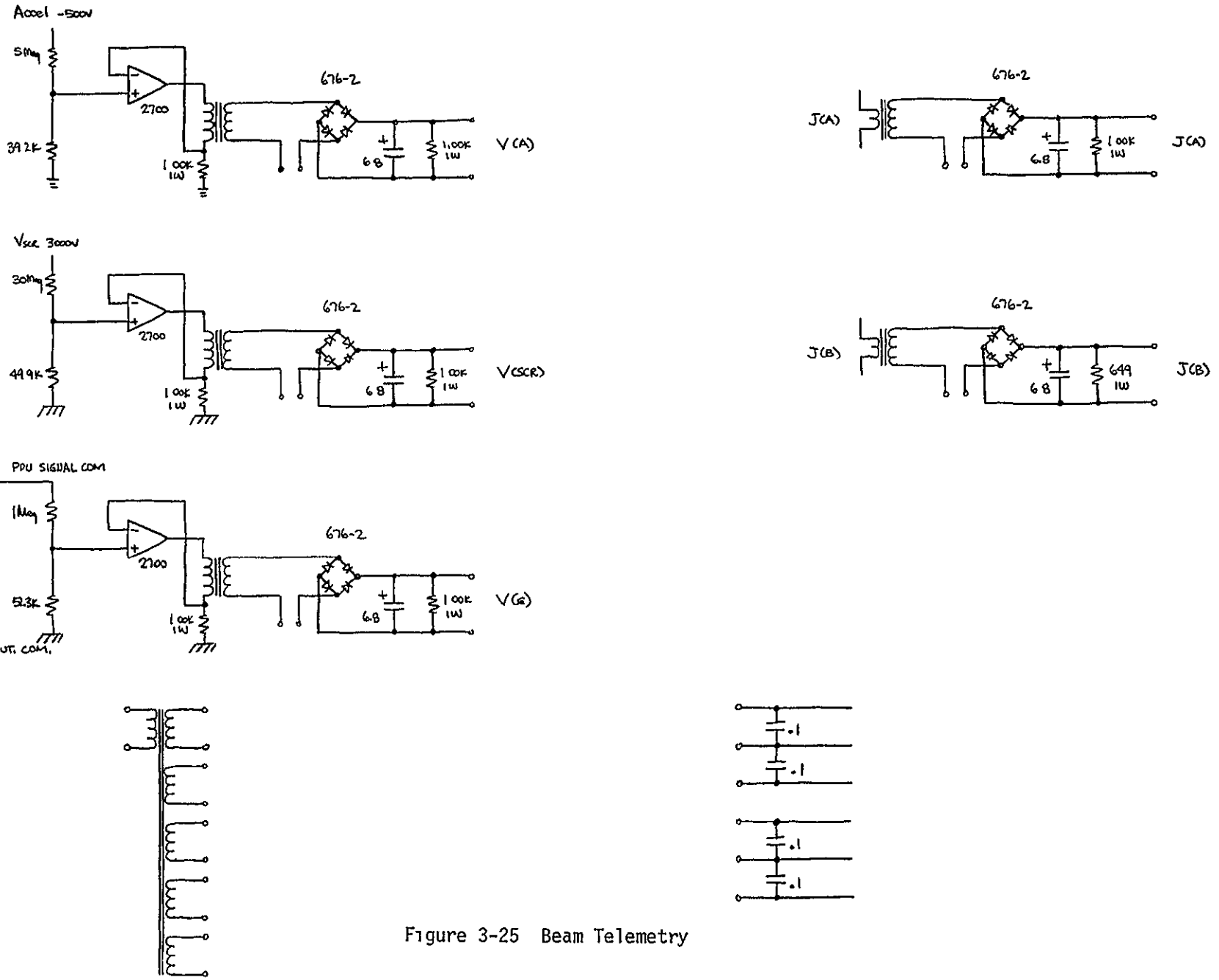


Figure 3-25 Beam Telemetry

Table 3-VII Design Summary - Telemetry

	COMPONENT WEIGHT	LOSSES	PART COUNT
TLM OSCILLATOR	66.35	1.760	23
INPUT TLM	69.17	.431	24
BEAM INVERTER TLM	135.24	.518	37
DISCHARGE INVERTER TLM	91.07	.627	20
LOW LEVEL TLM	327.1	.714	64
	688.93gm	4.05W	168

3.5.6 Command and Protection System

Figure 3-26 shows the block design for digital interface unit with its microprocessor and its relationship to the output commands to the PPU and digital response data from the PPU.

Figure 3-27 shows the proposed serial data format used for the basic design for PPU digital interface unit.

Figure 3-28 through 3-30 presents the schematics of the microprocessor digital interface unit using standard LSI microprocessor hardware.

Flow diagrams were generated for the following power processor functional operation to check memory capability of the microprocessor and to determine the extent of software necessary for the microprocessor:

- Power turn-on
- Initiate corrective action
- Recycle procedure
- Engine control loops
- Interrupt
- Power supply on/off control

Figures 3-31 through 3-35 are the schematics of the PPU command and protection system and its interface with the microprocessor.

Figure 3-31 decodes the type of command:

> Type 1, Telemetry measurement; Type 2, Discrete command set points; Type 3, Power supply outputs on/off; Type 4, Beam current reference, Type 5, Discharge current ref.; Type 6, Magnetic Baffle current ref. being sent to the PPU.

Figure 3-31 also contains the three analog references.

Figure 3-32 shows the circuitry for the output supplies turn-on and turn-off and the telemetry channel conditioning.

Figure 3-33 shows the generation of the power supplies operational set point references.

Figure 3-34 senses the critical power processor parameters and generates the interrupt signal to the microprocessor.

Figure 3-35 shows the schematic of the circuitry to ensure providing the necessary isolation between the microprocessor power ground and the separate grounds in the PPU.

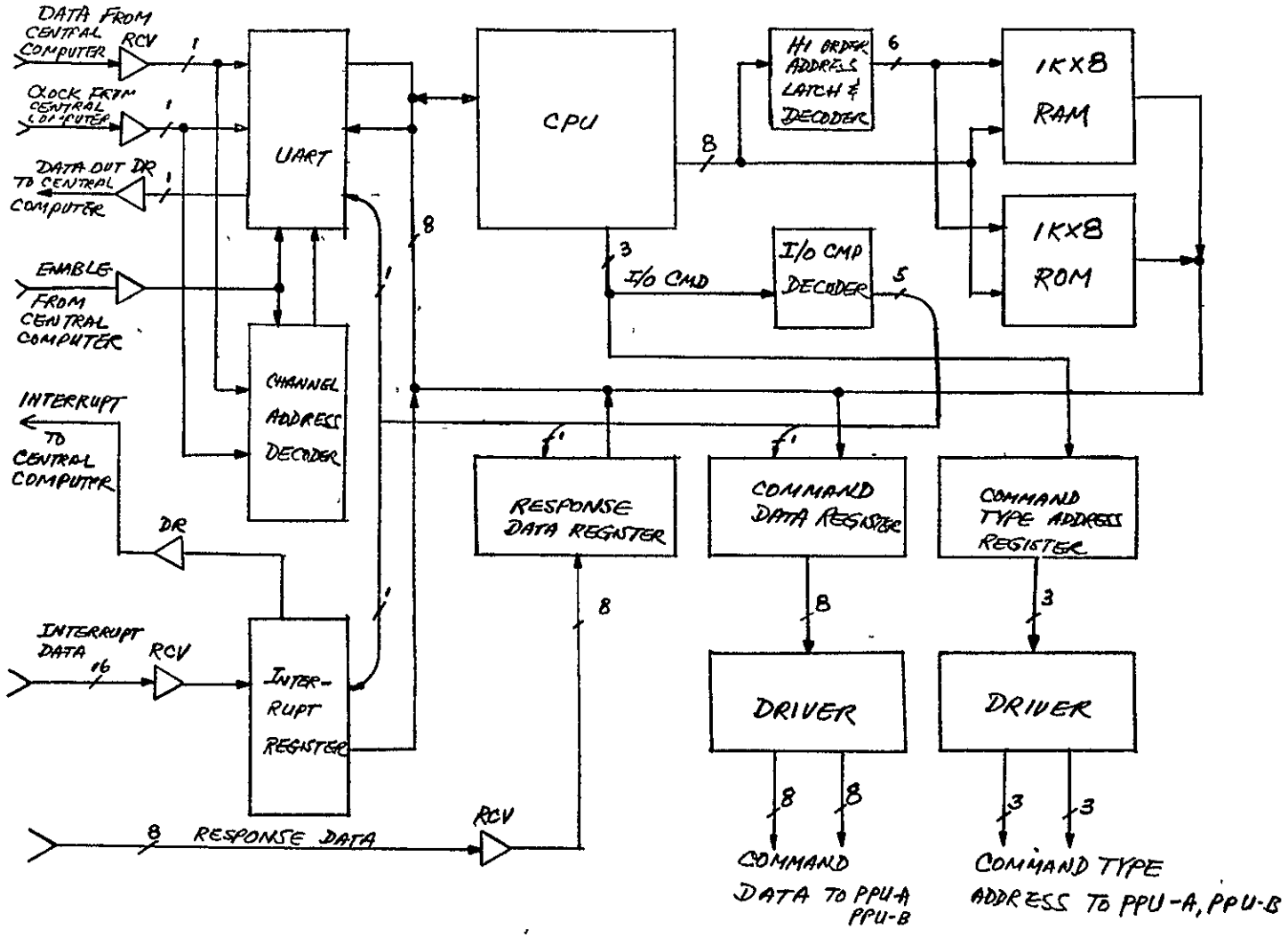
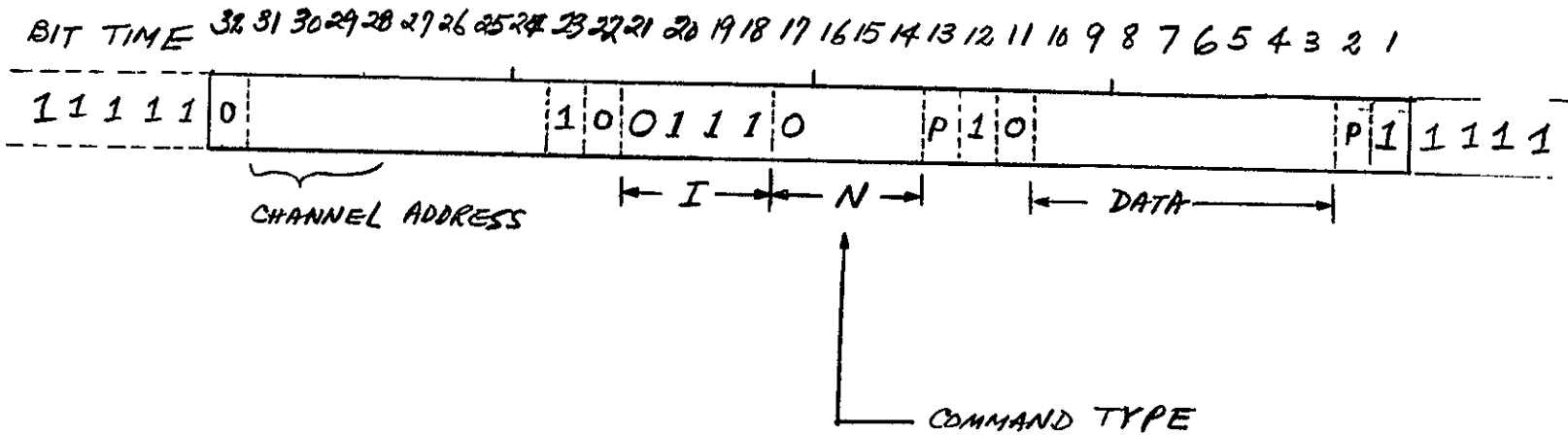


Figure 3-26 Digital Interface Unit - Block Diagram



where P = parity bit

Figure 3-27 External Command Format

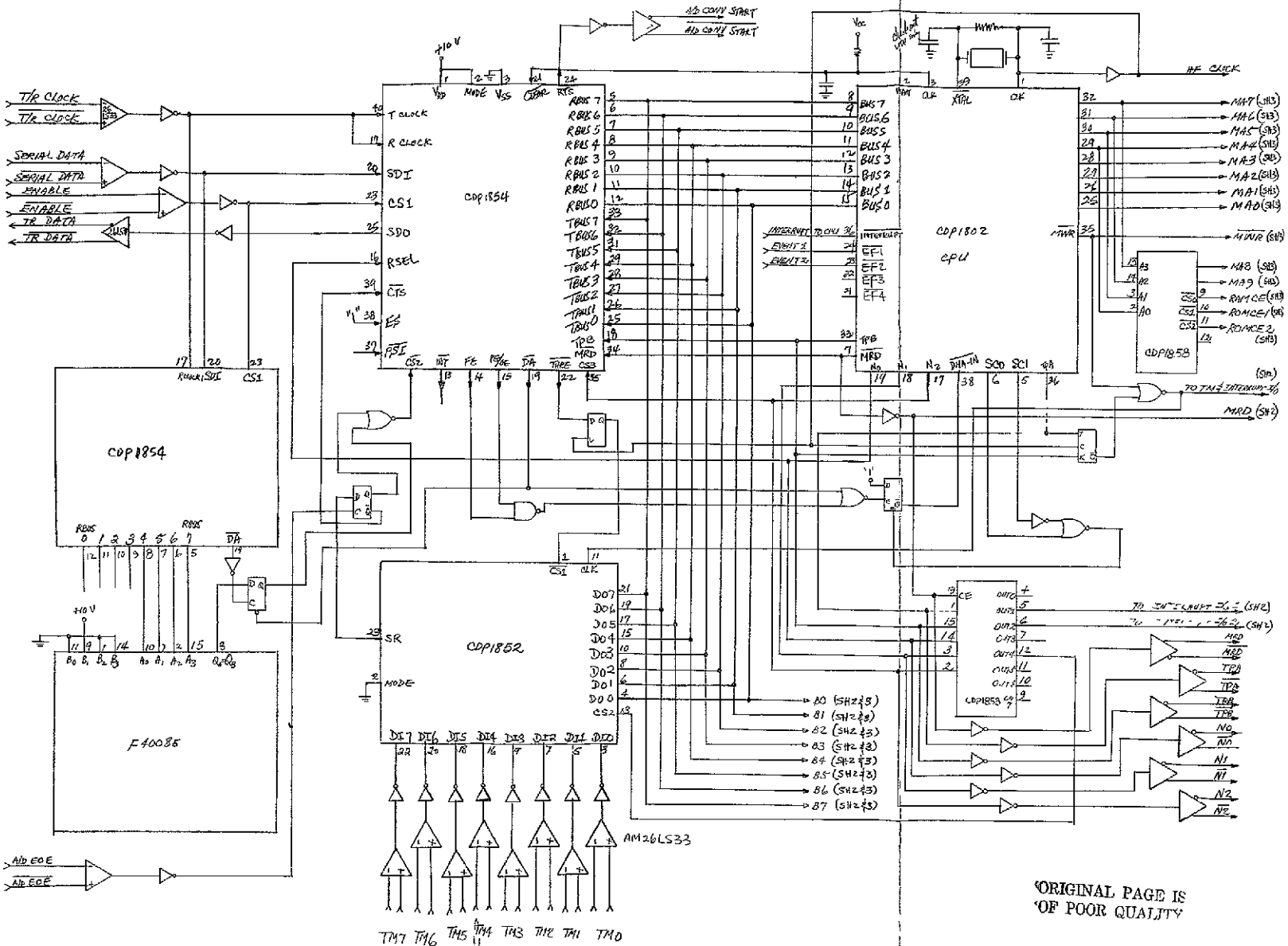


Figure 3-28 Digital Interface Unit

FOLDOUT FRAME 1

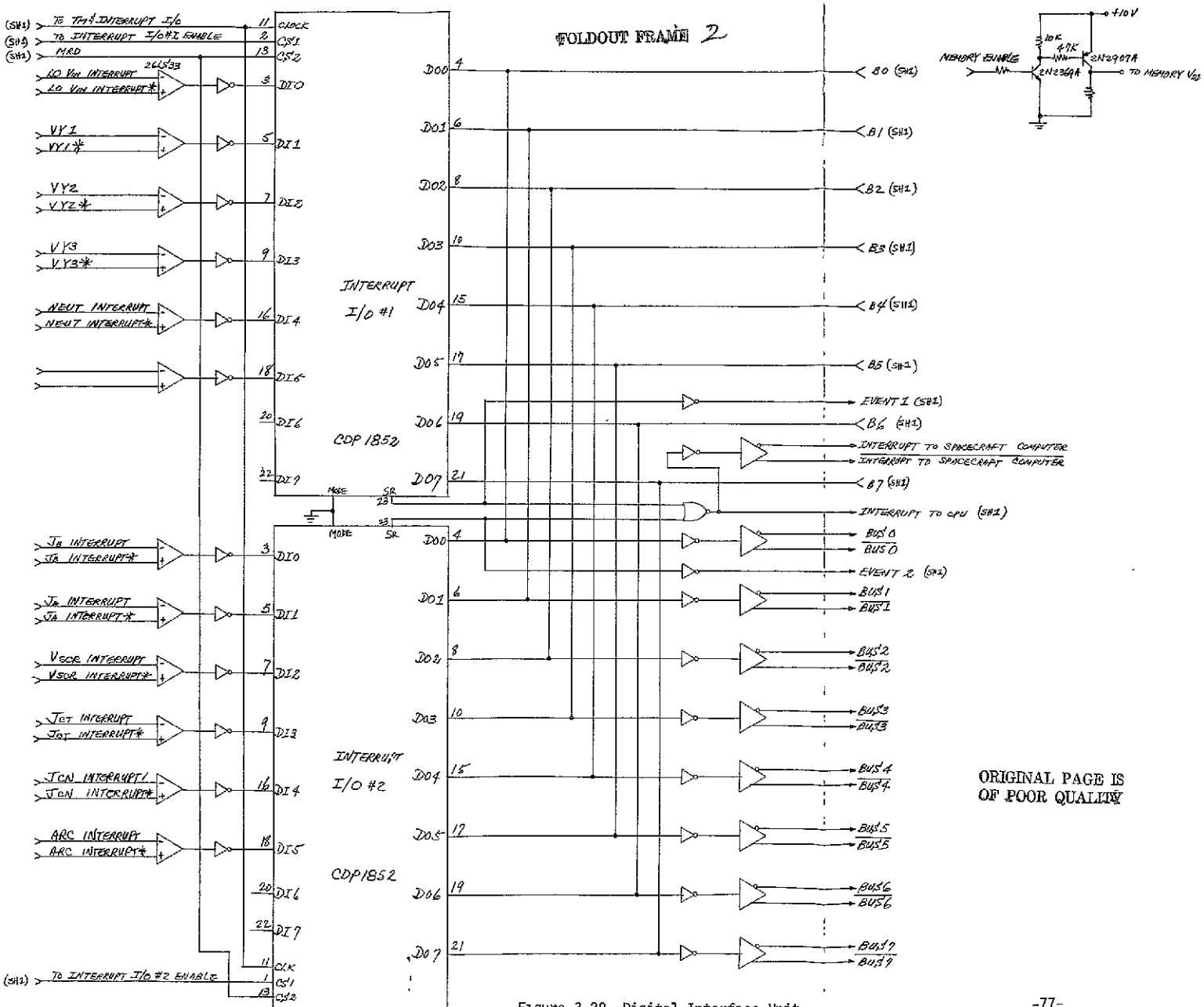


Figure 3-29 Digital Interface Unit

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FOLDOUT FRAME 1

FOLDOUT FRAME 2

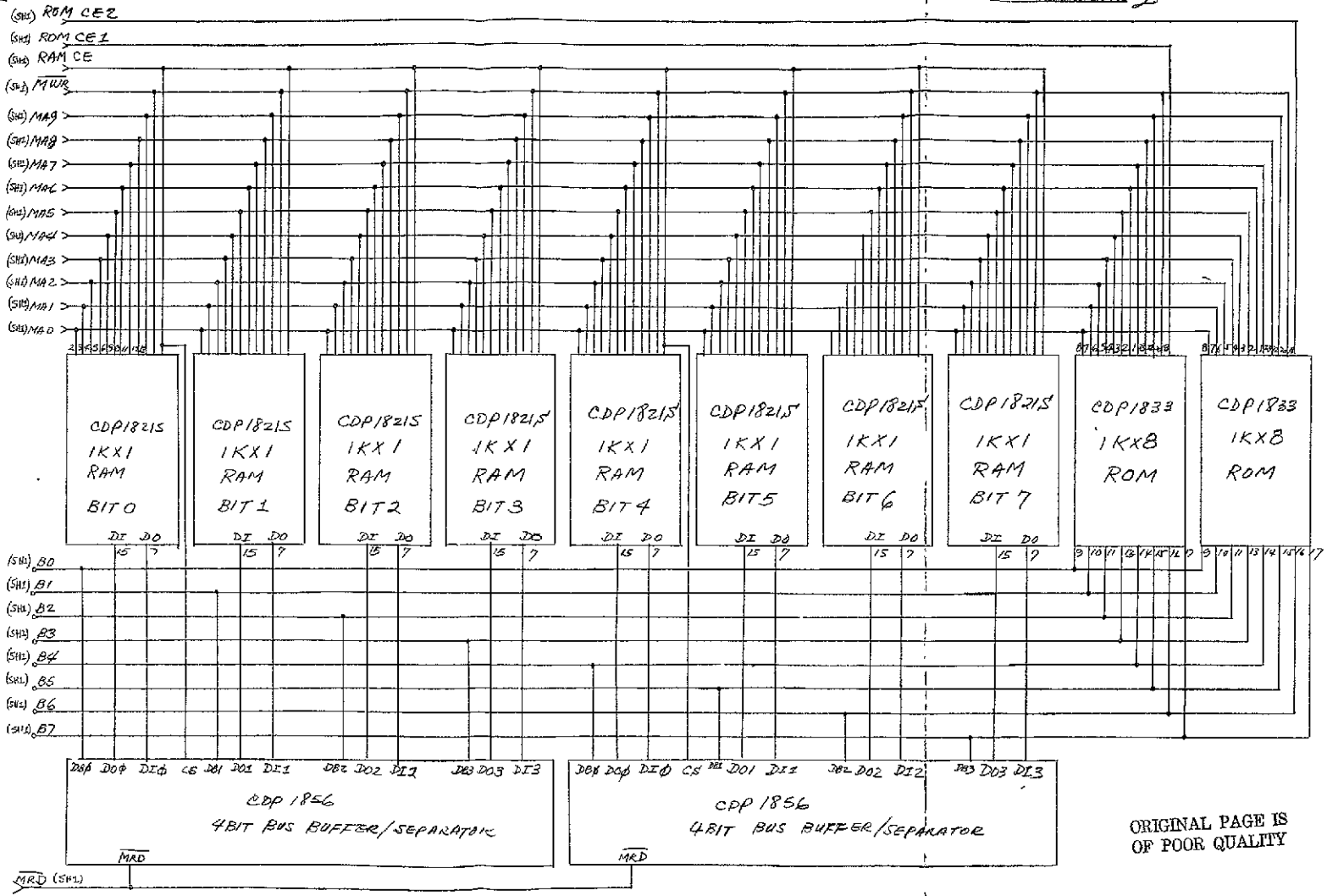

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Figure 3-30 Digital Interface Unit

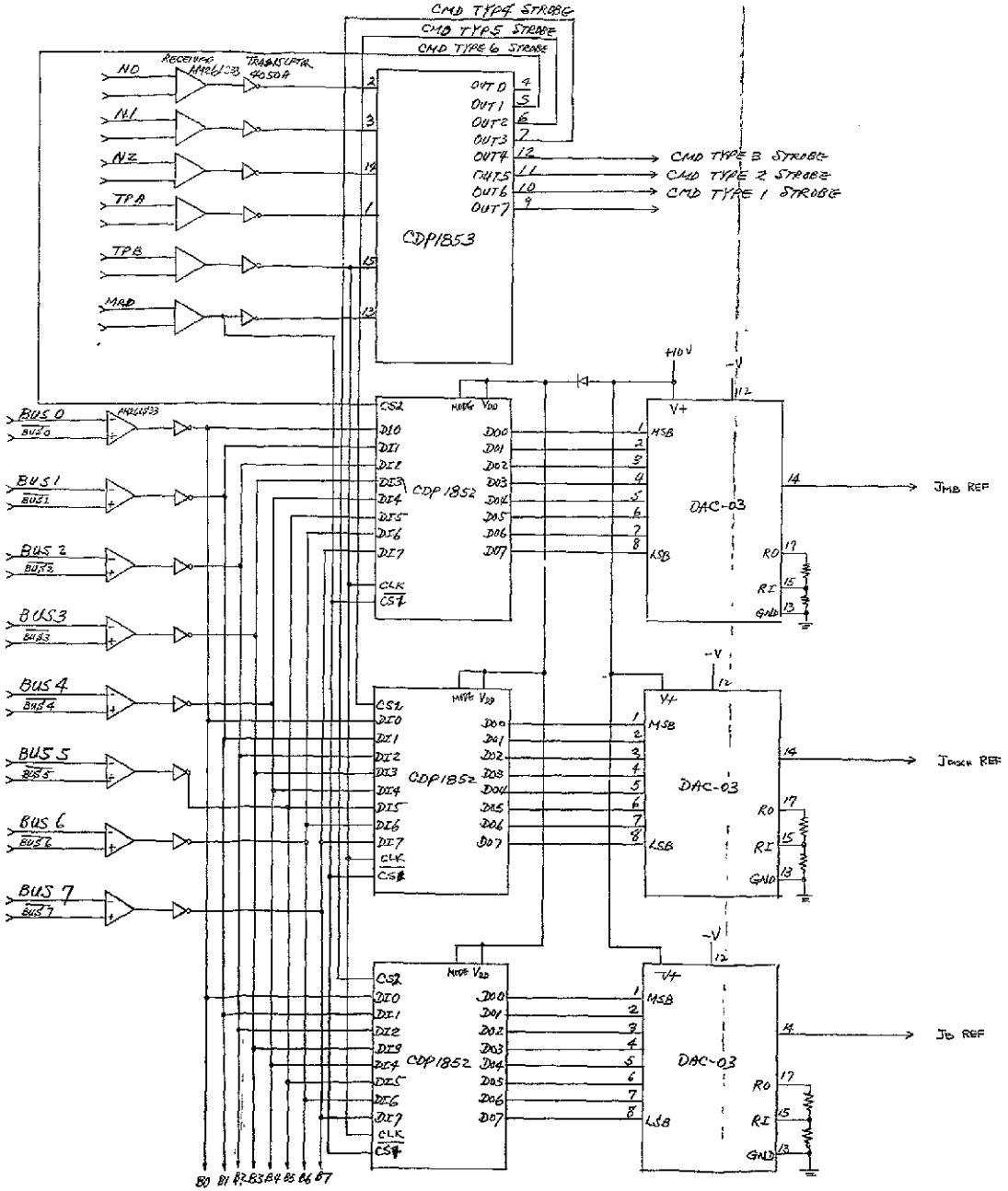


Figure 3-31 Command and Protection

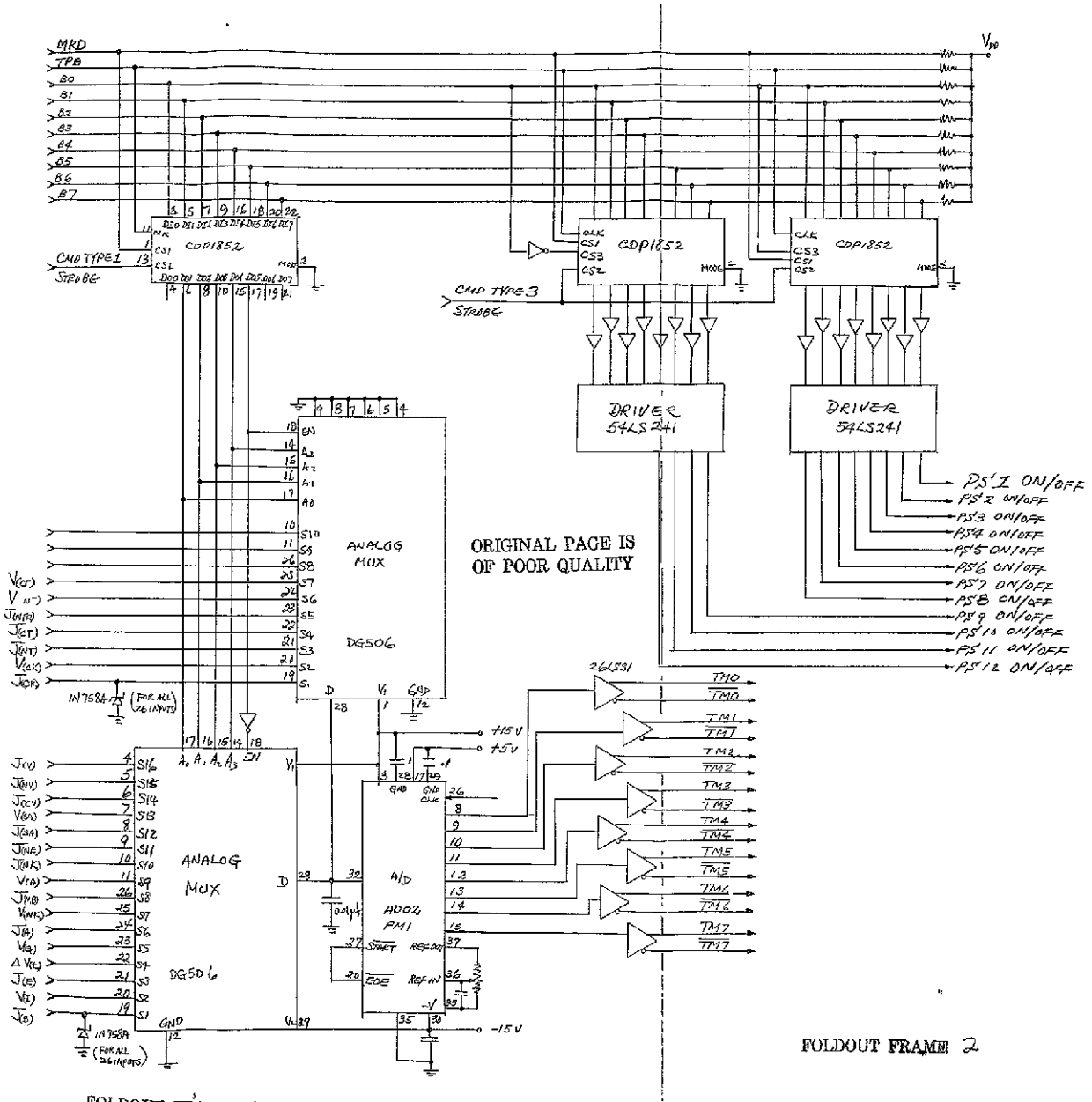


Figure 3-32 Command and Protection

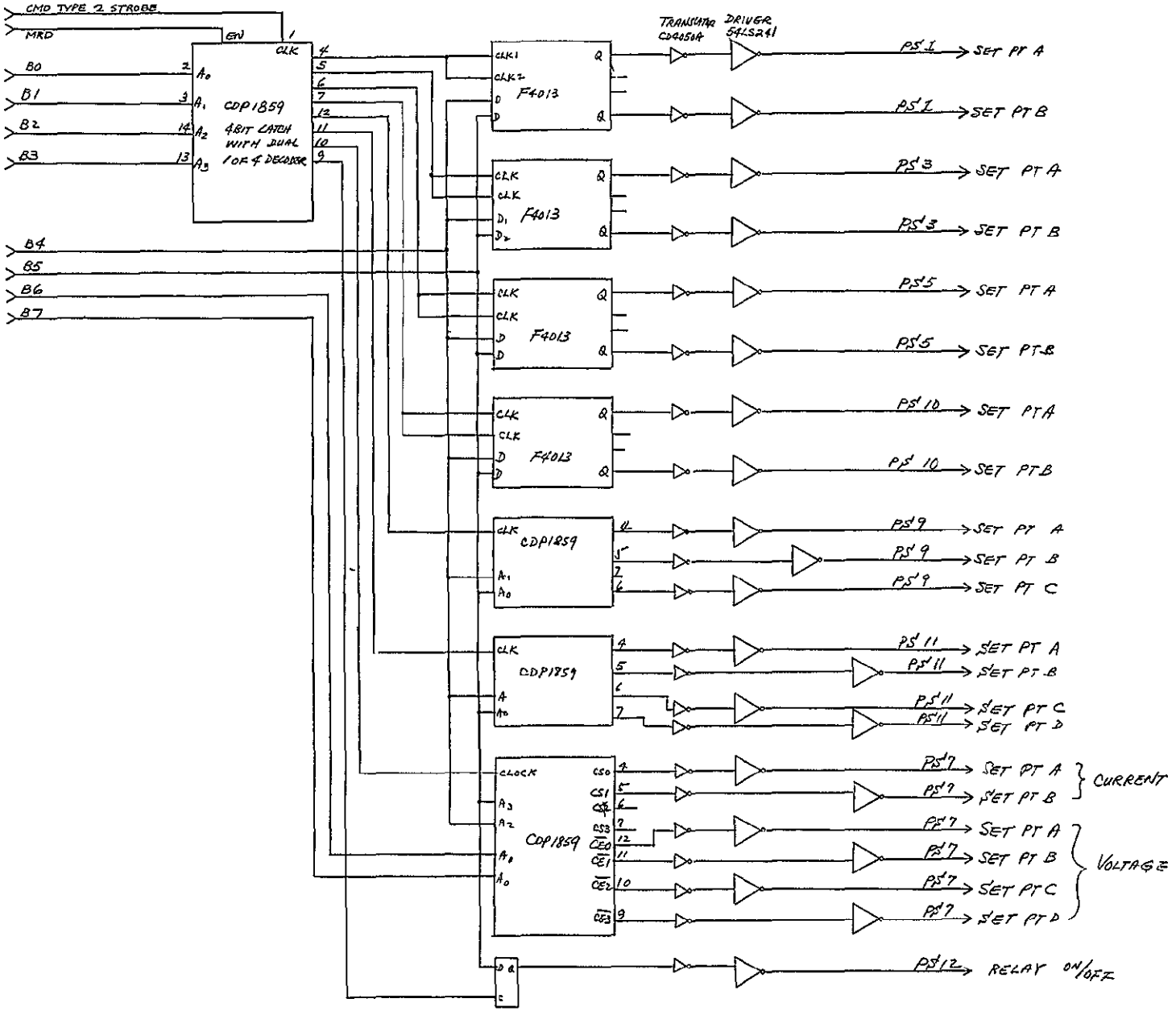


Figure 3-33 Command and Protection

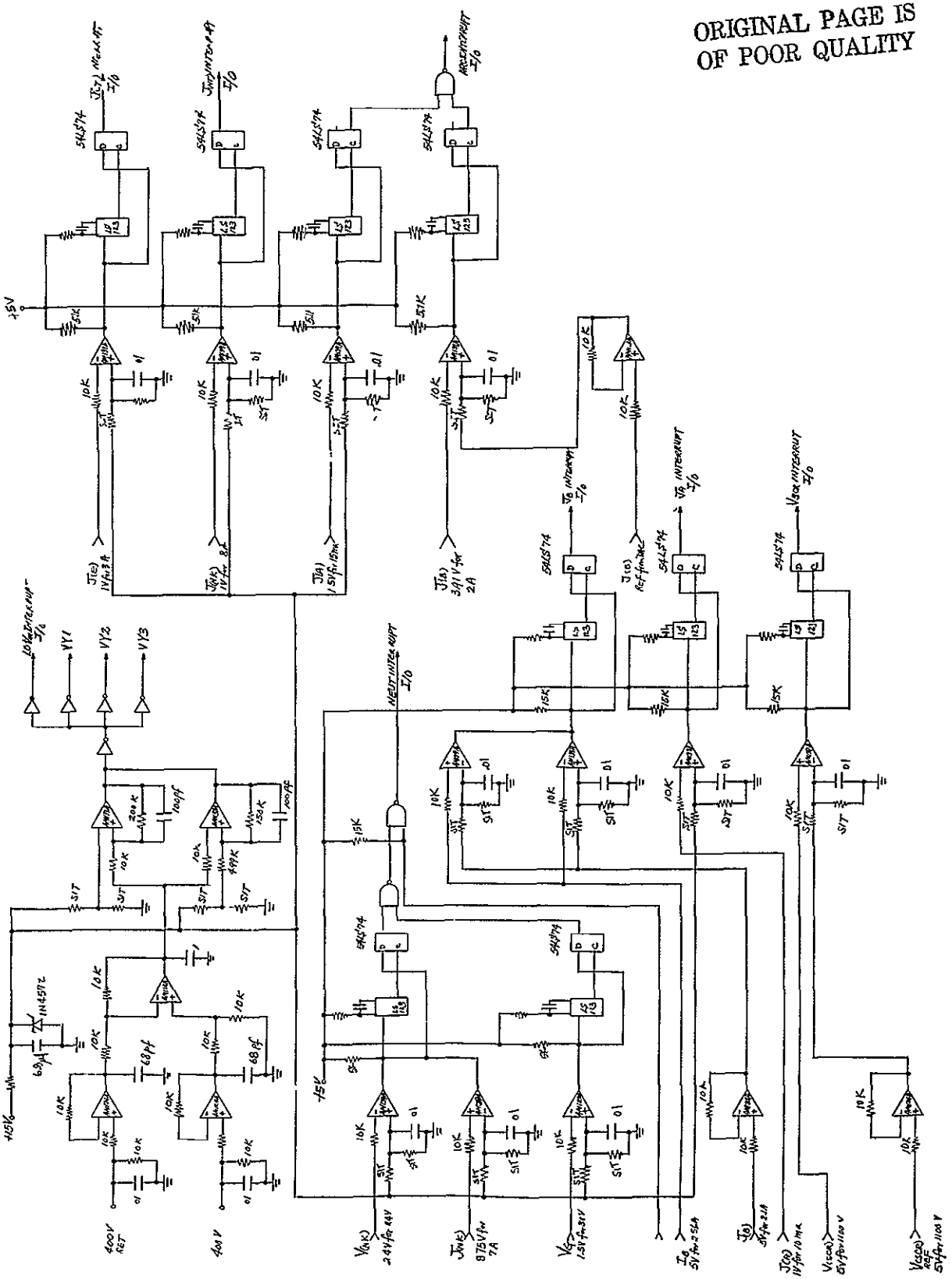


Figure 3-34 Command and Protection

C-2

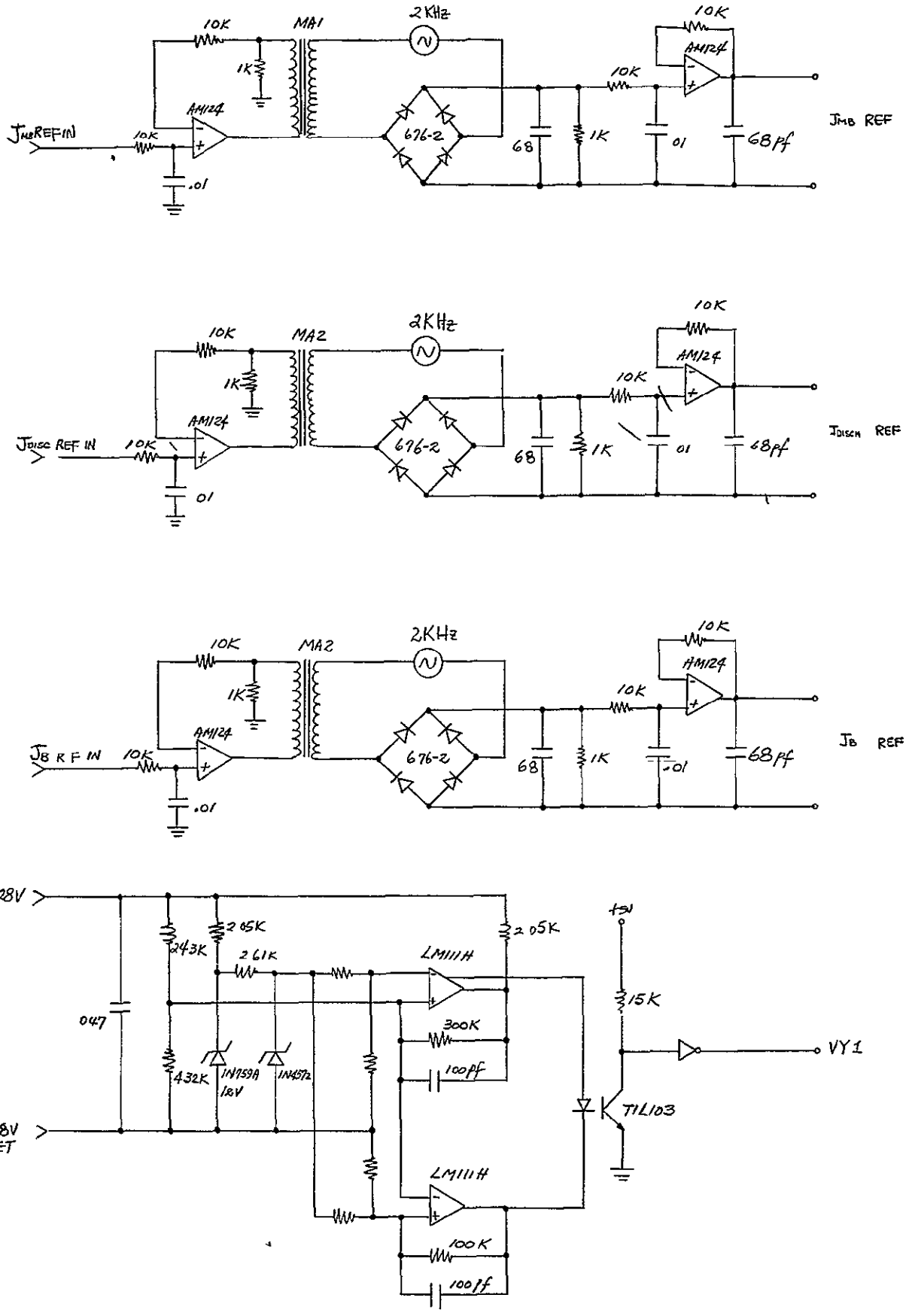


Figure 3-35 Command and Protection

The microprocessor simplified the design of the protection system since sequencing and timing of the power supplies are controlled directly by the microprocessor.

Table 3-VIII summarizes the design data for the microprocessor digital interface unit and the PPU Command and Protection System.

Table 3-VIII Design Summary - Digital Interface Unit, Command & Protection

	COMPONENT WEIGHT GRAMS	LOSSES WATTS	PART COUNT
DIGITAL INTERFACE	147.1	.973	92
COMMAND PROTECTION	243.0	3.479	224
TOTAL	490.1	4.452	316

3.5.7 Auxiliary Power Supplies

Two auxiliary power supplies are used in the proposed design (1) for the power processor control electronics and (2) for the interface unit.

These two power supplies are seperated to ensure keeping out unwanted noise transients in the microprocessor and also as a means of turning the microprocessor on and off in case a standby digital interface unit is added for redundancy.

Figure 3-36 is the DC-DC converter used for the PPU control electronics. It is supplied from the 28 VDC bus and supplied regulated output power to the different PPU electronics signal common, neutralizer common.

Figure 3-37 is the DC-DC converter supplied isolated regulated power to the microprocessor and it's associated electronics.

Table 3-IX summarizes the design data for these low power converters.

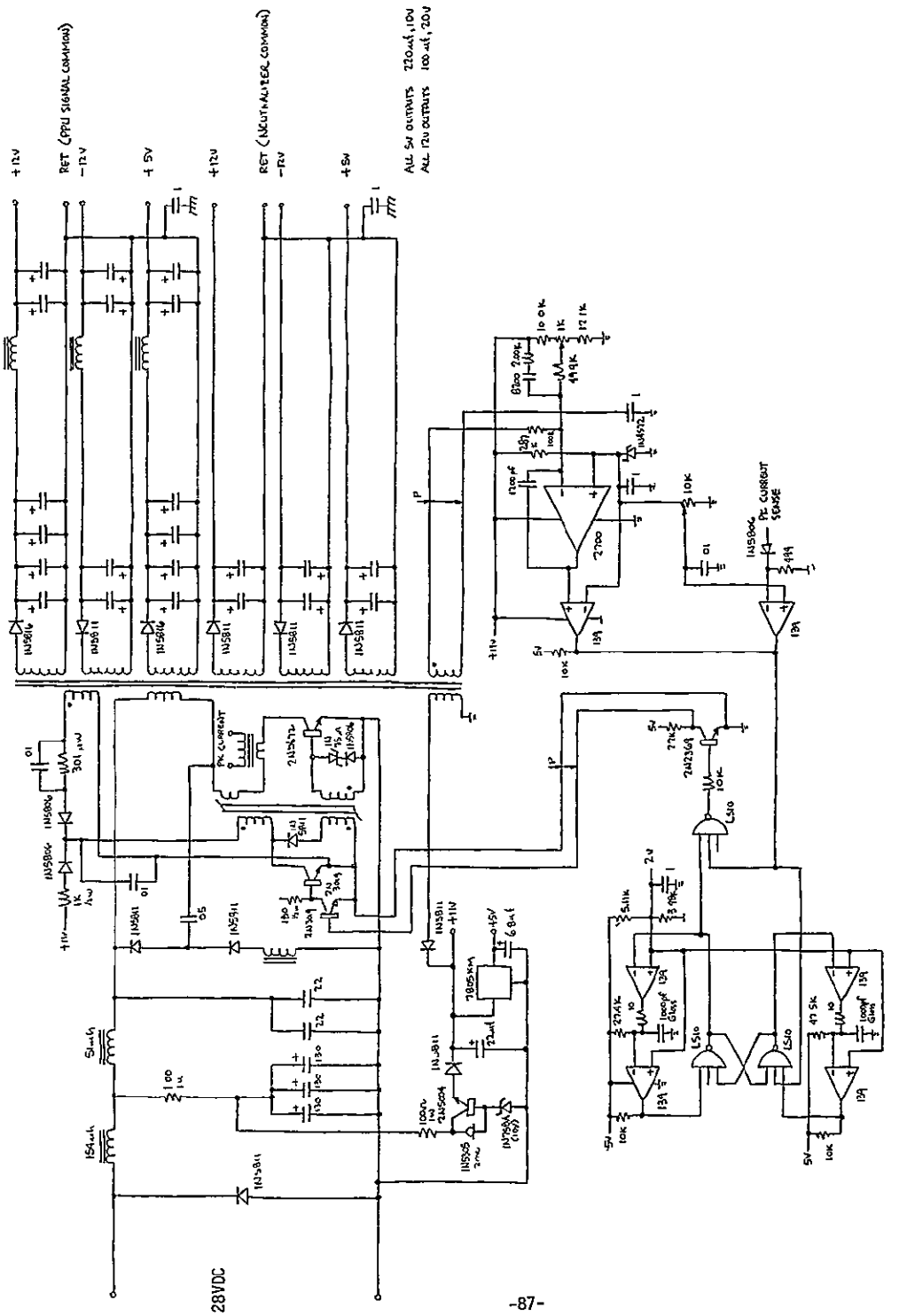


Figure 3-36 Auxiliary Converter

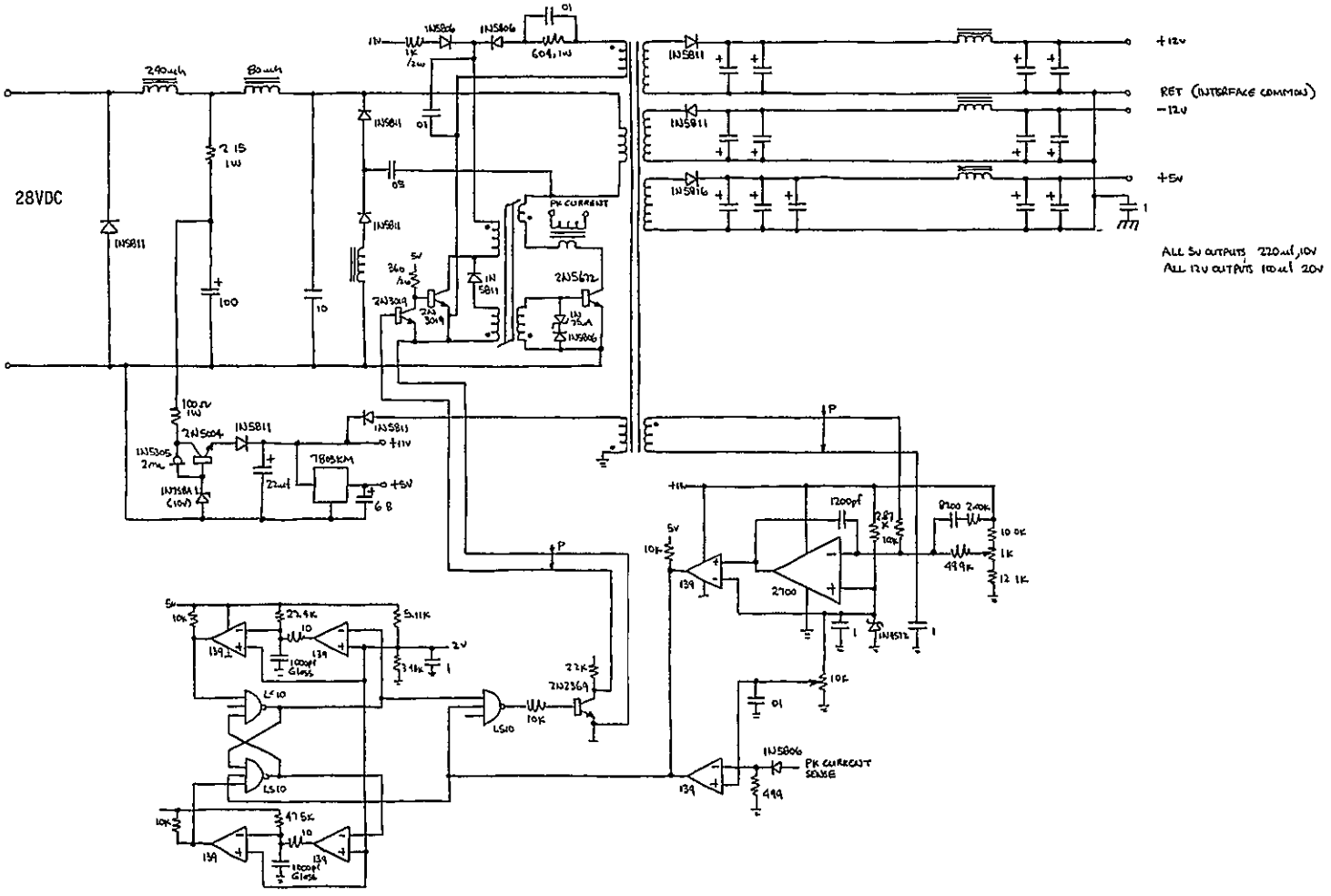


Figure 3-37 Interface Converter

Table 3-IX Design Summary and Auxiliary Converters

	COMPONENT WEIGHT GRAMS	LOSSES WATTS	PART COUNT
AUXILIARY CONVERTER	599.36	9.066	106
INTERFACE CONVERTER	309.36	2.864	90
TOTAL	908.72	11.930	196

3.5.8 Power Processor Design Summary

Table 3-X presents the data on the complete power processor electrical design based on a 6 KW Beam supply. This design is based on:

20KHZ thyristor full bridge series resonant inverters Beam supply

50KHZ transistor full bridge series resonant inverter Discharge supply

Dedicated DC-DC converters for the low power ion engine output

Microprocessor digital interface unit

Use of T^2L integrated circuits for all digital control electronics

Low power operational simplifiers

Table 3-XI presents the data on the complete power processor electrical design based on a 2.2 KW Beam supply. All above improvement have been incorporated except that a 20KHZ thyristor half bridge series resonant inverter beam supply is used for the 2.2KW output and the input filter had to be redesigned due to the lower total input power level.

Table 3-X Summary of Power Processor Characteristics (6KW Beam)

Output Power ≈ 6545W	PART COUNT	COMPONENT WEIGHT GMS	LOSSES WATTS	EFFICIENCY %
INPUT FILTER	44	4368 1	20.98	
Beam Inverter (6000W)				
Power Stage	106	9388 1	408 6	93.6%*
SCR Firing	148	173.85	26 251	
Series Inverter Control	140	76 83	980	
Regulator	118	123 47	1 320	
Accelerator Regulator	50	89 78	2.104	
Sub Total	562	9852 03	439.255	
Discharge Inverter (500W)				
Power Stage	28	1493.6	77 54	86 6%*
Transistor Drive	167	243 17	16.99	
Series Inverter Control	130	71.03	.924	
Regulator	97	113.87	.493	
Booster	59	134 01	783	
Sub Total	481	2055.68	96 73	
Low Level Outputs (45W)				
Power Stage	330	2495.23	24.563	64.7%*
Controls	623	530.89	3 197	
Sub Total	953	3026 12	27 76	
TELEMETRY	168	688.93	4 05	
DIGITAL INTERFACE	92	147.1	973	
COMMAND AND PROTECTION	224	243 05	3.479	
AUXILIARY CONVERTER	106	599.36	9.066	
INTERFACE CONVERTER	90	309 36	2.864	
Sub Total	680	1987 80	20 432	
TOTALS	2720	21289 73	605 157	91.5%

*Power Stage Efficiency

Table 3-XI Summary of Power Processor Characteristics (2.2KW Beam)

	PART COUNT	COMPONENT WEIGHT GMS	LOSSES WATTS	EFFICIENCY %
INPUT FILTER	32	2147	8.24	
Beam Inverter (2200W)				
Power Stage	59	4803.2	161.92	93 1%*
SCR Firing	74	87.0	13 1	
Series Inverter Control	140	76.83	980	
Regulator	118	123.47	1.320	
Accelerator Regulator	50	89.78	3.104	
Sub Total	441	5180.28	180.424	
Discharge Inverter (500W)				
Power Stage	28	1493 6	77.54	86.6%*
Transistor Drive	167	243 17	16.99	
Series Inverter Control	130	71.03	.924	
Regulator	97	113 87	.493	
Booster	59	134.01	.783	
Sub Total	481	2055.68	96.73	
Low Level Outputs (45W)				
Power Stage	330	2495.23	24.563	64.7%*
Controls	623	530.89	3.197	
Sub Total	953	3026.12	27.76	
Telemetry	168	688.93	4 05	
Digital Interface	92	147.1	.973	
Command & Protection	224	243 05	3 479	
Auxiliary Converter	106	599 36	9 066	
Interface Converter	90	309.36	2 864	
Sub Total	680	1987 8	20 432	
Totals	2587	14396.88	333.586	89.2%

*Power Stage Efficiency

3.6 Reliability Estimate

A preliminary reliability assessment was performed based on the detailed electrical schematics and parts list generated for the 6KW power processor.

Figure 3-38 presents the reliability block diagram for the Extended Performance Power Processor. The component temperature was estimated at 70°C. The failure rate for each power processor function has been identified in order to show where reliability improvement can be made without large weight or power loss penalties.

Comments on the results of this analysis and a discussion of the techniques applied are as follows:

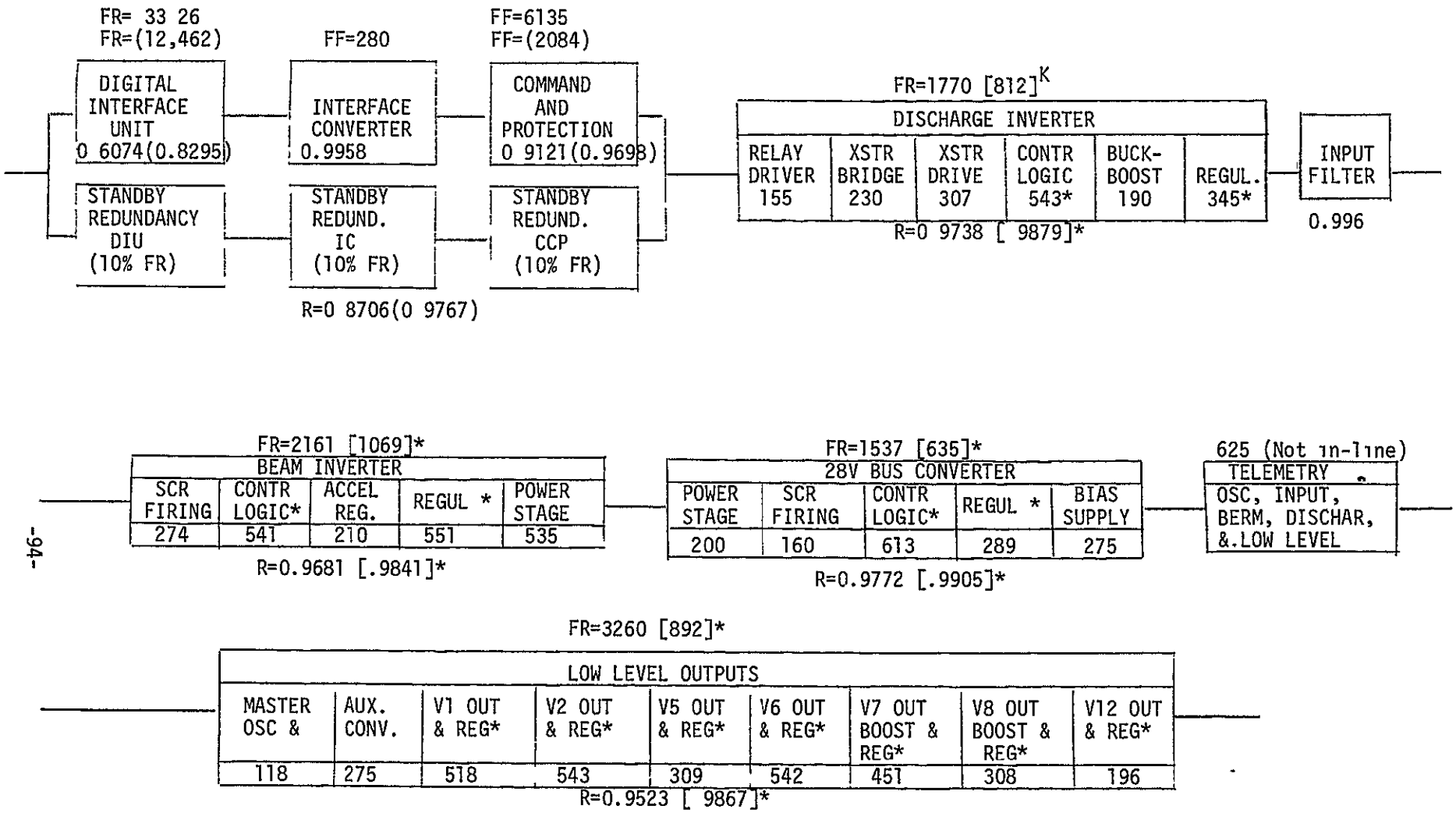
- The DIU, CIU, and C&P slices of the PPU were assessed in both a standby redundant and non-redundant configuration. Also, thermal isolation of these slices (to maintain a 55°C internal ambient rather than 70°C) was assessed as an option. For the best case, viz standby redundant DIU, CIU and C&P slices (thermally-isolated), the PPU reliability is 0.8769, which is somewhat less than the goal of 0.96 at 15,000 hours. Numerous mitigating factors, however, make the actual PPU reliability somewhat better than 0.8767. These factors are discussed in the next several bullets. (Schedule and budget considerations did not permit examination of these factors at this time.)

- All parts in all slices were counted in this assessment (excluding the Telemetry Slice which was treated as not in-line). Failure rate improvement would result from identifying un-used gates (e.g., in quad parts) and non-critical failure modes (e.g., opens in certain capacitors).

- Taking into account the duty cycle of certain parts (e.g., registers) would significantly improve failure rates.

- All semiconductors were assessed using calculated primary electrical stress levels (I or P) as well as the secondary stress levels (V) required by the MIL-HDBK-217B failure rate formulae. The maximum stress level encountered for a particular part type in any application was then used for all parts of that generic callout. Some failure rate improvement would result from using the actual stress level encountered for each individual part.

- MIL-HDBK-217B failure rates for LSI may be decreased in the near future as a prospective revision to the document is now being coordinated with Industry. It can be seen from the IC failure rates of Table 3-XI that the PPU failure rate total is heavily influenced by the IC failure rates.



NOTES: A) Failure rates shown are per billion hours
B) Failure rates in parenthesis assume slice is thermally isolated.
C) Standby unit is at 10% of operative failure rate while in standby mode.

* Majority voting used in the control and regulator electronics

Figure 3-38. PPU Reliability Block Diagram

- Two specific IC types (57 each HA2-2700 Op Amp and 36 each LM139D Quad Comparator) encompass 50% of the PPU failure rate in the non-redundant slices (i.e., other than the DIU, C&P, and CIU). Several factors might reduce the failure rates assigned to these two part types:

    1) Part manufacturer's failure rate data may be available that demonstrates lower failure rates than those calculated by MIL-HDBK-217B.

    2) The failure rates for these parts has been multiplied by a factor of (7) per MIL-HDBK-217B to account for the ambient temperature effect. A special heat sink might be designed for these parts, if this effect is determined to be realistic.

    3) For these parts, as well as for all IC's, a more accurate determination of junction temperatures (i.e , rise above the part ambient temps) may reveal lower junction temperatures than are specified by the ground-rules contained in the Notes to Table 2.1.5.4 of MIL-HDBK-217B.

- By the time this design materializes as hardware, failure rates for piece parts (and in particular CMOS) will generally be lower. It has been traditionally true that failure rates have tended to decline with time as the technology improves to combat the failure modes which surface.

- Failure rate totals for each slice are shown in Figure 3-38. These totals have been calculated by multiplying the quantity of each part type shown on the October 1977 Parts List for each slice of the PPU by the respective part failure rates listed in Tables 3-XIII through 3-XVII herein (and by adding a 3% factor for resistors and caps and using the failure rates listed in a subsequent bullet of this section for Magnetics). To reduce the volume of this report the numerous Parts List sheets showing this multiplication and addition have not been included herewith but are available in the TRW SSD Reliability files. Specific computational techniques employed for this assessment are discussed in the bullets which follow.

- Standby redundant DIU and C&P slices (and CIU) are assessed using a 10% standby failure rate factor.

- The 55°C thermal isolation temperature is based on maintaining an internal slice ambient that is only 5°C above the 50°C PPU baseplate. Non-thermally isolated slices would be 20° above the baseplate (or 70°C internal ambient).

- The September 1976 revision of MIL-HDBK-217B was used in the failure rate assessment.

- The failure rate for Resistors and Capacitors was not calculated on a part-by-part basis but was rather lumped in as an additional 3% to each slice's failure rate. This approximation was derived from the October 1976 assessment of a prior PPU configuration (IOC 7515.268) wherein the failure rate for all resistors and capacitors, as individually assessed, totalled 2.5% of the PPU failure rate. A failure rate total of 2.5% is, in reality, lost in the tolerance on the accuracy of the reliability prediction. The basic reason that the R&C failure rates are so small in that These parts are bought to ERMIL established failure rate levels (R,S) which result in a fractional multiplier in the MIL-HDBK-217B models.

- Magnetics in the PPU were assumed to be MIL-T-27, Class S (130°C rated) and operating in a 70°C ambient with a 20°C hot spot temp rise. These assumptions are based on TRW historical experience. Failure rates employed for Magnetics were:

	Failure Rate ($F/10^9$ hrs)
Low Power XFMR's	2
All chokes (since they're all power types) and high power XFMR's	6
Mag Amps	6
Current sensors	2
Relay	11

Note: Anything dissipating over 20mW was treated as "High Power."

- The single crystal used in the PPU was assessed at $200F/10^9$ hrs (per MIL-HDBK-217B).

- For all part types, the quality level factor (πQ) used in the MIL-HDBK-217B failure rate calculations was the best listed since TRW historically buys parts with the best possible screening and production heritage or screens the parts in-house to such a level

- The environmental factor (πE) employed was that for space flight.

Table 3-XIII

PPU IC FAILURE RATES

L = Linear
✓ = In DIU or C&P

(T_{amb} = 70°C, π_Q = 1, π_L = 1, π_E = 0.2)

( ) = 55°C ambient for DIU and C&P

	Description	IC Callout		No of GATES, XSTR'S, or BITS	π_P	π_T	C_1 0.97 for G 0.056 for M	C_2 0 46 0 02	λ
CMOS	RCA CPU	CDP 1802D	✓	842G & 256 bits	1.1	8.5 (3.1)			9653(3600)
CMOS	RAM (1Kx1)	CDP 1821SD	✓	1024 bits	1	8.5 (3.1)	0.13	0 049	1115 (413)
CMOS	ROM (1Kx8)	CDP 1833 or 1834D	✓	8196 bits	1	8.5 (3 1)	0 26	0.11	2232 (828)
CMOS	8 Bit I/O Port	CDP 1852D	✓	88G	1	8.5 (3 1)	0 0265	0.0195	226 (86)
CMOS	N-Bit Decoder	CDP 1853	✓	50G	1	8.5 (3.1)	0.018	0 016	156 (59)
CMOS	UART	CDP 1854D	✓	469G	1.1	8 5 (3 1)	0 17	0.095	1798(789)
CMOS	4 Bit Bus Buff/Separ.	CDP 1856 Bus Buffer	✓	20G	1	5 (1.7)	0.0098	0.011	51 (19)
		CDP 1858 4 Bit Latch w/1 of 4 DEC	✓	49G	1	8.5 (3.1)	0.0185	0.016	160 (60)
		CDP 1859 Ditto w/Dual DEC	✓	66G	1	8.5 (3 1)	0 022	0 018	191 (72)
CMOS	Quad 2 input nor	CD 4002	✓	2G	1	5	0 0021	0.0039	11 (5)
CMOS	Quad 2 input nand	CD 4011	✓	6G	1	5	0 0043	0.0074	23 (10)
CMOS	Dual F-F	CD 4013	✓	24G	1	5 (1 7)	0.011	0 012	57 (21)
CMOS	Dual F-F	CD 4027	✓	30G	1	5 (1.7)	0.013	0 013	67 (25)
CMOS	Translator (Hex Buff)	CD 4049	✓	6G	1	5	0.0043	0.0074	23 (9)
CMOS	Translator (Hex Buff)	CD 4050A	✓	6G	1	5	0 0043	0.0074	23 (9)
CMOS	1 of 16 Decoder	CD 4514		102G	1.1	8.5 (3.1)	0.030	0.020	285 (97)
CMOS	Dual 1 of 4 Decoder	CD 4556		34G	1	8 5 (3.1)	0.014	0.014	122 (46)

Table 3-XIII

PPU IC FAILURE RATES (Continued)

L = Linear
✓ = In DIU or C&P

(T_{amb} = 70°C, π_Q = 1, π_L = 1, π_E = 0.2)

( ) = 55°C ambient for DIU and C&P

	Description	IC Callout		No. of GATES, XSTR'S, or BITS	π_P	π_T	C_1	C_2	λ
L	Driver (Advanced Microdevices)	AM 26LS31	✓	98Q	1	7 (2.5)	0 0185	0.032	136 (53)
L	Receiver	AM 26LS33	✓	100Q	1	7 (2 5)	0.019	0 032	139 (54)
L	Dual Comparator	AM 119	✓	16Q	1	7 (2.5)	0 0046	0.012	35 (14)
L	Quad Op Amp	AM 124A	✓	52Q	1	7 (2.5)	0.011	0 023	82 (32)
L	Quad Comparator	AM 139A	✓	32Q	1	7 (2.5)	0 0079	0 017	59 (23)
	CMOS 16 Ch Analog Mux	DG 506 (Siliconix)	✓	124Q	1.1	18 (7)	0.0334	0 0224	667 (262)
L	8 bit D/A (PMI)	DAC 03	✓	76Q	1	7 (2.5)	0 015	0 028	91 (43)
L	Driver	DS 1688		36Q	1	7 (2.5)	0 0086	0.018	64 (25)
L	Receiver	DS 1690		96Q	1	7 (2.5)	0.018	0 032	132 (51)
	TTL (LP)	54LS00J		4G	1	1	0.0033	0 0064	4.6
	TTL (LP)	54LS04J		6G	1	1	0 0043	0 0074	5.6
	TTL (LP)	54LS10J		3G	1	1	0.0025	0 0057	5
	TTL (LP)	54LS20J		2G	1	1	0.0021	0 0050	3
	TTL (LP)	54LS74	✓	12G	1	1	0 0069	0.0095	9
	TTL (LP)	54LS123	✓	20G	1	1	0 0098	0.011	12
	TTL (LP)	54LS241	✓	10G	1	1	0.0061	0 0089	8
	Line Driver	SN54S140J		2G	1	1 25	0 0021	0 0050	3.6
	Hex Buff/Driver	SN5407J		6G	1	1 25	0 0043	0 0074	6.3
L	Dual Periph. Driver	SN55451B		10Q	1	7	0 0032	0.009	24

Table 3-XIII

PPU IC FAILURE RATES (Continued)

L = Linear
✓ = In DIU or G&P

(T_{amb} = 70°C, π_Q = 1, π_L = 1, π_E = 0 2)

( ) = 55°C for DIU and C&P

Description	IC Callout	No. of GATES, XSTR'S, or BITS	π_P	π_T	C_1	C_2	λ
(Harris) Analog Switch (CMOS)	H1-5040-2-10	3G	1	5	0.0025	0 0057	14
(Harris) Dual Analog Switch (CMOS)	H1-5041-2-10	6G	1	5	0.0043	0.0074	23
(TI) Opto Isolator	TIL 103	2Q	1	7	0 0016	0.0056	11
(FSC) Quad Switch (CMOS)	F4066	20Q	1	5	0 0055	0.013	30
8 bit Addr Latch (CMOS)	F4724	59G	1	8.5	0 0205	0 017	178
Dual F-F (CMOS)	F4013	24G	1	5	0.011	0 012	57
Op Amp (Harris)	HA2-2700	20Q	1	7	0.0055	0 013	41
Opt. Isol. (HP)	HP5082-4365	2G & 6Q = 14Q	1	7	0.0041	0 011	31
Quad Comparator (Nat'l)	LM139D	32Q	1	7	0.0079	0 017	59
L Compar.	LM111H	23Q	1	7	0 0062	0 015	46
(PMI) 8 bit A/D	AD02	220Q	1.1	18(7)	0.034	0 050	684(273)

Table XIV

$\pi_E = 1$, $\pi_Q = 0.2$

PPU XSTR'S

λ_p	% PWR	Callout	Type	π_A	π_R	π_C	$\frac{V_{CE\ APPL.}}{V_{CEO\ RAT.}}$	π_{S2}	λ_b	Power Rating
1.4	<10	2N2222A	Sm. Sign. Amp & Sw. NPN	1.5	1	1	40V rat <50%	0.64	7 5	1.8W at 25°C case 0 5W at 25° amb
1.4	<10	2N2369A	High Speed Sw. NPN	1.5	1	1	15V rat. <50%	0.64	7.5	0 36W at 25°C amb 0 68W at 100°C case
3	<10	2N2907A	Sm. Sign. Amp. PNP	1 5	1.5	1	60V rat. <50%	0 64	11	0 6W at 25°C amb. 3W at 25°C case
2	<10	2N3019	Sm. Sign GP Amp. NPN	1.5	1 5	1	80V rat <50%	0 64	7.5	0 8W at 25° amb. 5W at 25°C case
7	<10	2N5004	50W Power NPN	1.5	5	1	80V rat. <50%	0 64	7.5	58W at 25°C case
10.6	<10	2N5005	50W Power PNP	1.5	5	1	80V rat. <50%	0.64	11	58W at 25°C case
6	<10	2N5153	TI Power PNP	1 5	2	1	80V rat. 60%	0 88	11	12W at 25°C case 200°C max
4[A]	<10	2N5552	Unitr. Power Sw NPN	1.5	2	1	80V rat. 60%	0 88	7 5	15W at 100°C case 200°C max.
5[B]	<10	2N5659	Unitr. Power Sw. NPN	1 5	2.5	1	80V rat 60%	0.88	7 5	30W 100°C case 200°C max
10[C]	<10	2N5672	RCA Power Sw NPN	1.5	5	1	120V rat. 60%	0.88	7.5	105W at 70°C case 200°C max.
34	<10	SVT400-12	TRW H V. Power Sw NPN	1.5	5	1	400V rat. 100%	3.0	7.5	150W at 25°C case 200°C max
5[D]	<10	DTS723	DELCO H.V. Power NPN	1.5	2.5	1	1000 rat. 50%	0.64	10	50W at 75°C case 150°C max.

STRESS CORRECTION FACTORS (C_F)

A = 0.5 C = 0.7
B = 0.5 D = 0.5, T = 95°C

Table 3-XV

PPU Reliability Assessment

Group IV Diodes — Silicon GP

π_Q = 0.5
π_E = 1.0

λ_P	CF	Callout	Type	π_R	π_A	Rated V_R	Applied V_R	π_{S_2}	π_C	S	I_{O_P}	I_{max}
8	0.83 & T = 95°C	676-2 (Unitr.)	Full Wave Bridge	1	1.5	200V	20V	0.70	1	10%	15 ma	1A
2	0.8	1N5806 (Unitr.)	Power Rectifier	1.5	1.5	150V	75V	0.70	1	<10%	16 ma	2.5A
2	0.8	1N5811 (Unitr)	Power Rectifier	2	1.5	150V	75V	0.70	1	<10%	200 ma	6A
5	0 5	1N5816 (Unitr.)	Power Rectifier	4	1.5	150V	75V	0.70	1	<20%	4A	20A
35	0.83 & T = 95°C	USR45A (Unitr)	Power Rectifier	1	25	4500V	3500V	0.78	1	<10%	16 ma	250 ma
1	1	1N4150 (Fair)	Computer Diode	1	1.0	50V	30V	0.70	1	<10%	6 ma	200 ma
20	0.67 & T = 95°C	SA6795 (SEM)	Power Rectifiers	10	1.5	500V	350V	0.75	1	14%	7A	3A (S-S) 50A (pulse) (1 msec)
20	0.67 & T = 95°C	SA6796 (SEM)	Power Rectifiers	10	1.5	500V	350V	0.75	1	14%	7A	3A (S-S) 50A (pulse) (1 msec)
3	0.8	1N5553 (SEM)	Power Rectifiers	1.5	2.5	800V	500V	0.72	1	<10%	0	3A (S-S) 25A (pulse)
1	0.8	1N5715 (SEM)	Fast Recov. Rectif.	1	1 5	200V	50V	0.70	1	<10%	50 ma	1A (S-S) 6A (pulse)
1	0.8	1N5617 (SEM)	Fast Recov. Rectif.	1	1.5	400V	200V	0.70	1	<10%	10 ma	1A (S-S) 6A (pulse)
2	0.8	1N5417 (SEM)	Fast Recov. Rectif	1.5	1.5	200V	100V	0.70	1	<10%	200 ma	3A (S-S) 50A (pulse)
3	0.8	1N5419 (SEM)	Fast Recov Rectif.	1.5	1.5	500V	375V	0.78	1	30%	800 ma	3A (S-S) 50A (pulse)
11	0.85 & T = 95°C	SVD450-12 (TRW)	Power Diode	4	1 5	450V	425V	0.94	1	15%	1 3A	12A
4	0.33 & T = 95°C	MR1369 (Mot)	Power Diode	2	1.5	600V	425V	0 75	1	<10	0	6A (S-S) 35A (pulse)

Table XV

PPU Reliability Assessment (Continued)

Group IV Diodes — Silicon GP

λ_P	CF	Callout	Type	π_R	π_A	Rated V_R	Applied V_R	π_{S_2}	π_C	S	I_{O_P}	I_{max}
29	0.67 & T = 95°C	SCF S-2 (SEM)	Power Rectifier	10	1.5	200V	75V	0.70	1	35%	38W 35A	3A (S-S) 100A (pulse)
3	0.8	1N5554 (SEM)	Power Rectifier	2	1.5	1000V	600V	0.70	1	20%	1.3A	6A 25A (pulse)

Table 3-XVI

$\pi_E = 1$

$\pi_Q = 0.5$

PPU Reliability Assessment

Group V Diodes — Zener/Avalanche

λ_P	Callout	Type	π_A	I_Z or P Rating	I_Z or P Applied	S	C.F.
4	UDZ5807 (Unitr)	Power Zener (Two direction)	1.0	620 ma 5 w	400 mw	<10%	1
3	1N4572A (Mot)	T.C. Zener	1.5	62 ma 400 mw	18 mw	<10%	0.83
2	1N746A (Mot)	Zener	1.0	110 ma 400 mw	3 mw	<10%	0.83
2	1N751A (Mot)	Zener	1.0	70 ma 400 mw	0	<10%	0.83
2	1N753A (Mot)	Zener	1.0	60 ma 400 mw	18 mw	<10%	0.83
2	1N758A (Mot)	Zener	1.0	35 ma 400 mw	20 mw	<10%	0.83
2	UZ7707 (Unitr)	Power Zener	1.0	1250 ma 10 w	0	<10%	0.5
2	UZ7706 (Unitr)	Power Zener	1.0	1350 ma 10 w	0	<10%	0.5
2	UZ7712 (Unitr)	Power Zener	1.0	770 ma 10 w	0	<10%	0.5
2	UZ7714 (Unitr)	Power Zener	1.0	640 ma 10 w	0	<10%	0.5
2	UZ7720 (Unitr)	Power Zener	1 0	440 ma 10 w	0	<10%	0.5
2	1N3311B (Mot)	Power Zener	1.0	3600 ma 50 w	0	<10%	0.67
2	1N3320B (Mot)	Power Zener	1.0	1900 ma 50 w	0	<10%	0.67
2	1N3323B (Mot)	Power Zener	1.0	1500 ma 50 w	100 mw	<10%	0.67

Table 3-XVI

PPU Reliability Assessment (Continued)

Group V Diodes – Zener/Avalanche

λ_P	Callout	Type	π_A	I_Z or P Applied	I_Z or P Applied	S	C.F.
2	1N3325B (Mot)	Power Zener	1.0	1300 ma 50 w	0	<10%	0.67
2	1N3334B (Mot)	Power Zener	1.0	740 ma 50 w	100 mw	<10%	0.67
2	1N3335B (Mot)	Power Zener	1.0	660 ma 50 w	0	<10%	0.67
2	1N3350B (Mot)	Power Zener	1.0	200 ma 50 w	0	<10%	0.67
2	1N5305 (Mot)	Current Regulator (2 ma)	1.0	600 mw 100 v	36 mw	<10%	0.67
2	1N5286 (Mot)	Current Regulator (0 3 ma)	1.0	600 mw 100 v	3 mw	<10%	0.67
2	7805KM (Fairch)	5V Regulator (Power)	1.0	7.5 w 1500 ma	250 mw 50 ma	<10%	0.67

π_Q = 0.5

π_E = 1.0

Table 3-XVII

PPU Reliability Assessment

Group VI Diodes – Thyristors

λ_P	Callout	Type	π_R	Applied I	Rated I	S	CF
11	A348779 (Westing)	SCR	15	110A peak (70A avg)	200A RMS (125A half wave avg)	55%	0.67 and T = 120°C

Table 3-XVIII summarizes the present reliability prediction. Reliability improvement can be obtained by the following methods:

- Redundancy in digital interface unit and command protection electronics
- Redundancy in the low level electronics in the power processor
- Reduction of the control electronics temperature

Additional reliability improvement can be obtained by performing component screening and lower the basic component failure rate.

Table 3-XVIII PPU Reliability Assessment

		Reliability for 15,000 Hr.	
		No Redundancy	Standby Redundancy
Digital Interface Unit, Interface Converter, & Command and Protection Slices.	70°C Int. Amb.	0.5522	0.8706
	55°C Int. Amb.	0.8008	0.9767
Power Processor, Power & Control Electronics		No Redundancy	Majority Voting in Cont. Elect.
		0.8769	0.9498
Total Extended Performance Power Processor		0.7186	0.9277

3.7 Beam Power Transformer

Due to higher power rating (6KW) of the Beam Supply, a detailed electrical and mechanical design was performed on the beam power transformer. A thermal analysis was performed to check the thermal control aspects of the design.

A detailed electrical design was performed on the 6KW beam transformer, based on the 2.2KW beam transformer that was designed, fabricated and tested on Contract NAS3-19730 Electrical Prototype Power Processor Unit.

Table 3-XIX summarizes the electrical design details for the 2.2KW, 6KW and 10KW beam power transformers. The core material used in the design was 1/2 mil supermalloy.

Figure 3-39 shows the mechanical design of the 6KW beam transformer.

Table 3-XX summarizes the weight losses for the 6KW beam power transformer. 40% of the total weight was in the tape core, 28% of the weight was in the coil and the remaining 32% of the weight is for the mechanical mounting and transformer thermal control. By the use of more core material and less winding coil weight, the loss in the windings is minimized in order to reduce thermal control aspects of the design.

Figure 3-40 shows the exploded view of the 6KW beam transformer. It is composed of the following subassemblies:

- One piece mounting base
- Molded coils/core configuration
- End clamping plates

The low profile is used to reduce the thermal resistances to the baseplate and the cooling loop saddle.

The coil/core assembly is composed of two molded coils with the electrostatic shield extended outside of the coil by copper tabs. BeO spacers are placed between the coil and core to act as heat shunts to carry heat from the coil and core to outside mounting surfaces. These heat shunts reduce the winding hot spots.

Table 3-XIX

Beam Transformer Design Data

OUTPUT POWER	2KW	6KW	10KW
CONFIG.	1/2 BR	FB	FB
# NUMBER REACTORS	2	4	4
CORE DXEXFXG	.75X 438X2.375X1 000 2 USED	1 000X1.000X3.500X1.750	1.188X1.188X4 500X2.000
WT GMS	638g	1650g	2860g
LOSS	10 W	30 W	52 W
PRIMARY TURNS	16t (2L, 1 COIL)	12+12 1 (2 COILS)	16+16 t
WIRE	5X3X21X33	5X3X35X33	5X3X31X33
CURRENT	33 Arms	45 Arms	75 Arms
WEIGHT	208	525 gms	740 gms
DCR	6 3 mΩ	5.85 mΩ	8 2 mΩ
LOSS	6 9 W	11.9 W	46 1W
SECONDARY TURNS	204t	408t	950t
WIRE	32/33	32/33	32/33
CURRENT	2 7 Arms	2.7 Arms	2.7 Arms
WEIGHT	350	610 gms	1500
DCR	91 Ω	1.59 Ω	4.1Ω
LOSS	6.6 W	11 6W	29.9 W

Figure 3-39. Outline Drawing of 6KW Beam Transformer

Table 3-XX

Loss-Weight Estimate

	LOSS	WT	%
CORE	30	1650	40%
COILS	27	1165	28%
ESS	3		
BeO		270	
FRAME		300	
TERMS & BeO		100	32%
POTTING		500	
SCREWS & HDW.		40	
AUXILIARY TRANSFORMER		100	
	60W	4125 grams	

Figure 3-40. 6KW Beam Transformer - Exploded View

The primary power leads use lead sinks to further remove winding heat to the mounting base.

A detailed thermal analysis was performed on the 6KW beam power transformer. The computer analysis was based on the thermal model generated for the 2.2KW beam power transformer, developed under Contract NAS3-19730.

Figure 3-41 contains the results of the thermal analysis. P_{Power} loss is identified for the coil and core where the heat flow from the transformer is present to show the effectiveness of the thermal control technique. The temperatures for each transformer part is also presented based on a transformer heat sink of $50^{o}C$.

The maximum hot temperature was $76^{o}C$ in the secondary transformer winding. This temperature is below the maximum design hot spot limit of $85^{o}C$.

Due to the results of this thermal analysis, a transformer redesign should be made that would reduce transformer weight and have a hot spot temperature of $85^{o}C$. The present limitation of $85^{o}C$ is based on the polyurethane potting material used as the impregnation for the winding coils.

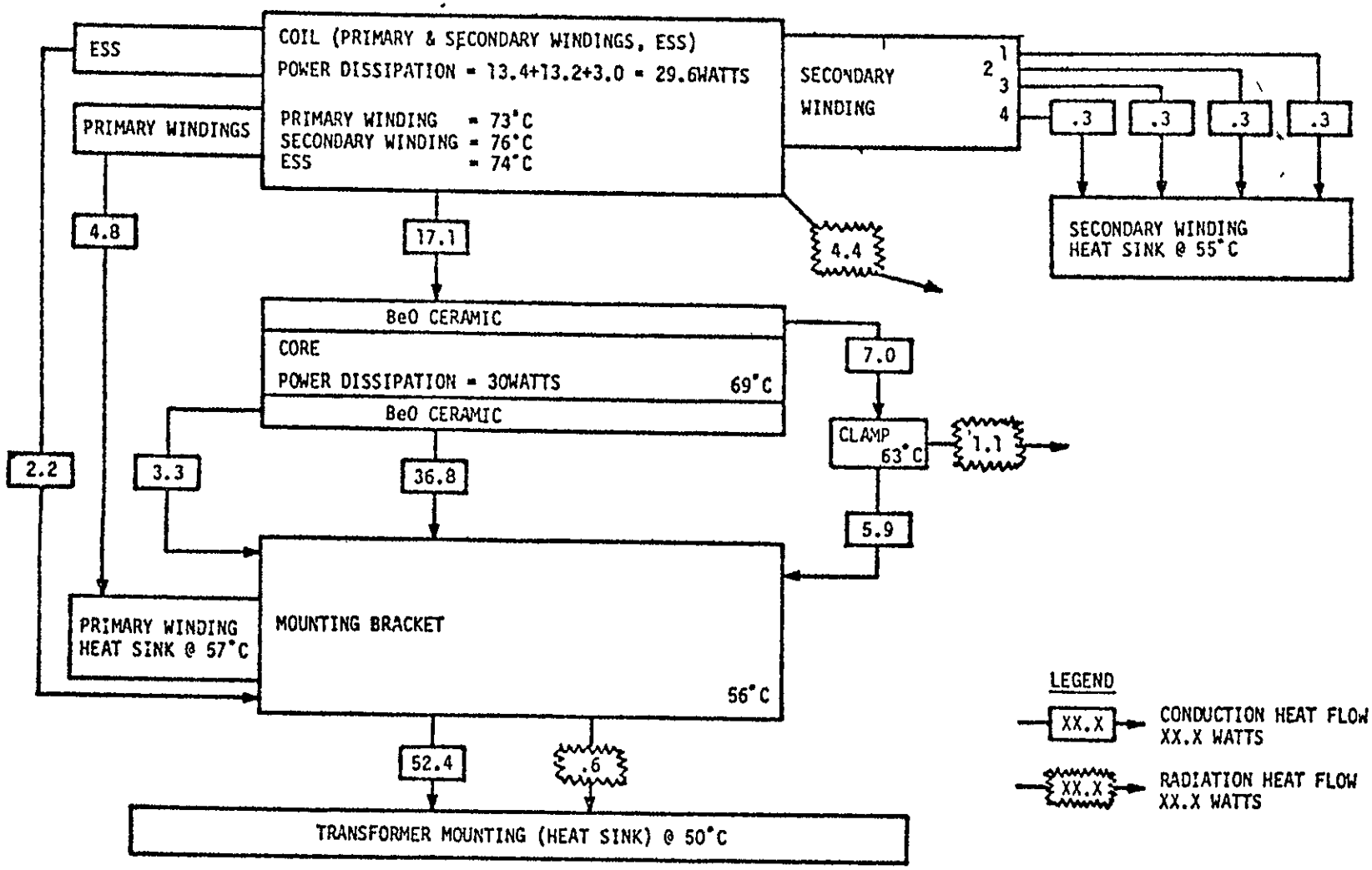


Figure 3-41. 6KW Beam Transformer Thermal Analysis Results

3.8 Beam Power Transformer Thermal Analysis

A thermal design study was undertaken for the purpose of analyzing the thermal design approach for the 6KW EPPP Beam Transformer. The purpose of the analysis was to predict transformer operating temperatures and to evaluate various passive thermal control design concepts.

The analysis of the transformer was conducted by developing a thermal model utilizing the SINDA Thermal Analyzer Program.

Although a thermal model had previously been developed for the analysis of the 2KW beam transformer (Ref. 3), a new thermal model was developed for the analysis of the 6KW beam transformer. The 6KW transformer model was then modified to simulate the 2KW transformer and a run was made to correlate these models. The correlation was good: Agreement of temperatures was within 1°C. The present thermal model of the 6KW transformer is fully documented in this report.

The present thermal model of the transformer was designed to be flexible to allow easy modification to allow analysis of other transformers of varying design, so long as the basic structuring is the same, i.e., symmetrical design with annular layers wrapped on a rectangular core.

3.8.1 Thermal Analysis Model

a) Pictorial Description of Thermal Model of 6KW Beam Transformer

The thermal model of the 6KW beam transformer is a model of a 1/4 symmetrical section of the entire transformer shown in Figure 3-42.

The thermal models of each element of the transformer are shown in Figures 3-43 thru 3-50. Included in these figures are the node numbers used in the thermal model (designated as .XXXX) and computer names of the physical dimensions as they are used in the calculations of the thermal parameters within the thermal model.

Figure 3-43 shows the thermal model of the transformer mounting bracket.

Figure 3-44 shows the thermal model of the transformer core.

Figure 3-45 shows the thermal model of the core and ceramic insulators.

Figure 3-46 shows the thermal model of the transformer coil.

Figure 3-47 shows the thermal model node numbering within a typical coil layer.

Figure 3-48 shows the thermal model of the electrostatic shield.

Figure 3-49 shows the thermal model of the heat conducting clamp connecting the core to the transformer bracket.

Figure 3-50 shows the thermal model of the primary winding heat sinking.

b) Power Dissipation

The total power dissipation of the 6KW beam transformer is 59.6W consisting of the following:

Primary winding	13.4W
Secondary windings	13.2W
Electrostatic shield	3.0W
Supermalloy core	30.0W
	59.6W

The power dissipation in the windings is considered to be constant. The total power is proportioned directly to the length of the windings including those external to the coil. The power dissipation in the electrostatic shield and core is considered to be evenly distributed over the volume.

c) Environmental Conditions

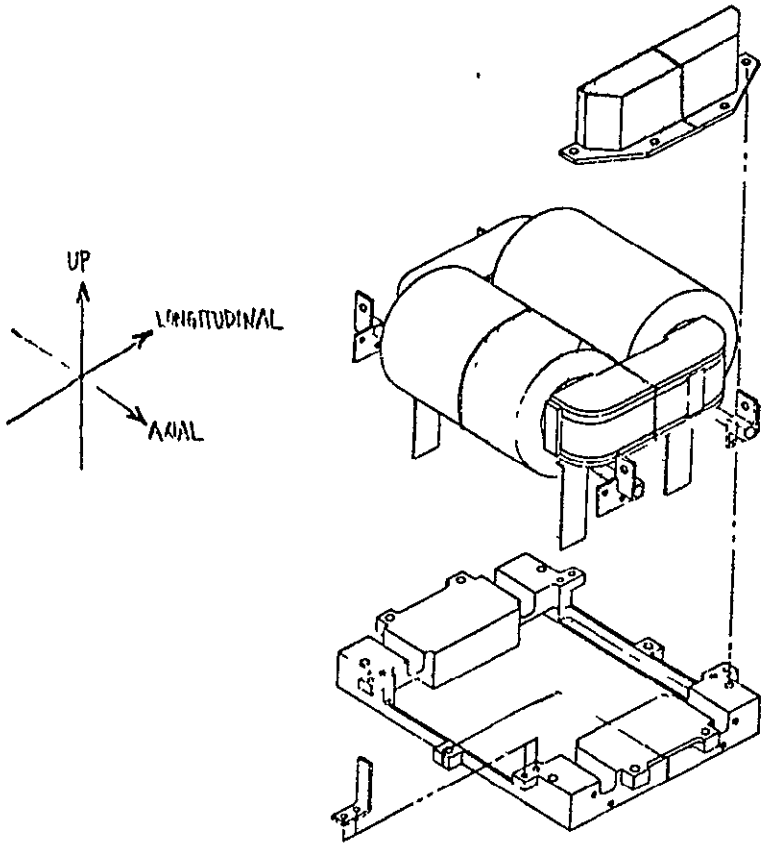
The transformer was assumed to be bolted to an isothermal heat sink at 50°C for heat conducted from the mounting bracket to the heat sink and for some radiation from the coil outer surface. The remainder of the surroundings was also assumed to be at 50°C for radiation from the outer surface of the coil. The transformer is assumed to be operating in a vacuum.

d) Thermal Properties of Materials

The following material properties were used in the analysis:

Material	Thermal Conductivity	
	BTU/hr-ft-F	Watt/in-C
Supermalloy Core		
Parallel to lamination	16.8	.738
Perpendicular to lamination	2.0	.088
Electrostatic shield primer	.11	.0048
OFHC copper	226.	9.93
Nomex insulation	.084	.00369
Polyeurethane potting	.084	.00369
Coil form	.084	.00369
6061-T6 aluminum	96.7	4.25
.995 pure beryllium oxide at 122°C	117.	5.14
Trucast bonding material (PR-4-2-6)	.42	.0185
.995 pure aluminum at 122°C	17.	.747

6KW BEAM TRANSFORMER - EXPLODED VIEW



¼ SYMMETRICAL SECTION MODELED SHOWN AS

FIGURE 3-42. THERMAL MODEL - 6 KW EPPP BEAM TRANSFORMER.

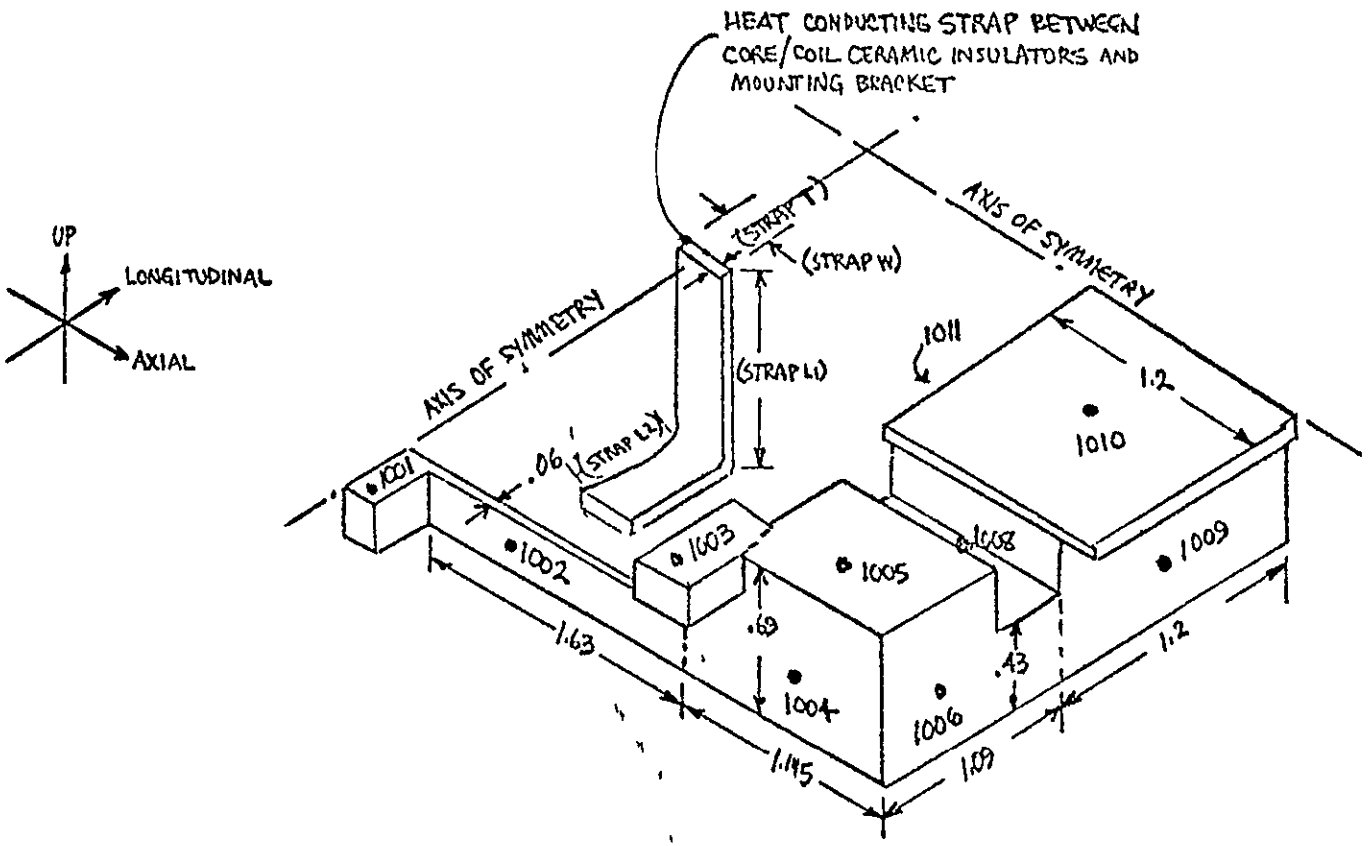
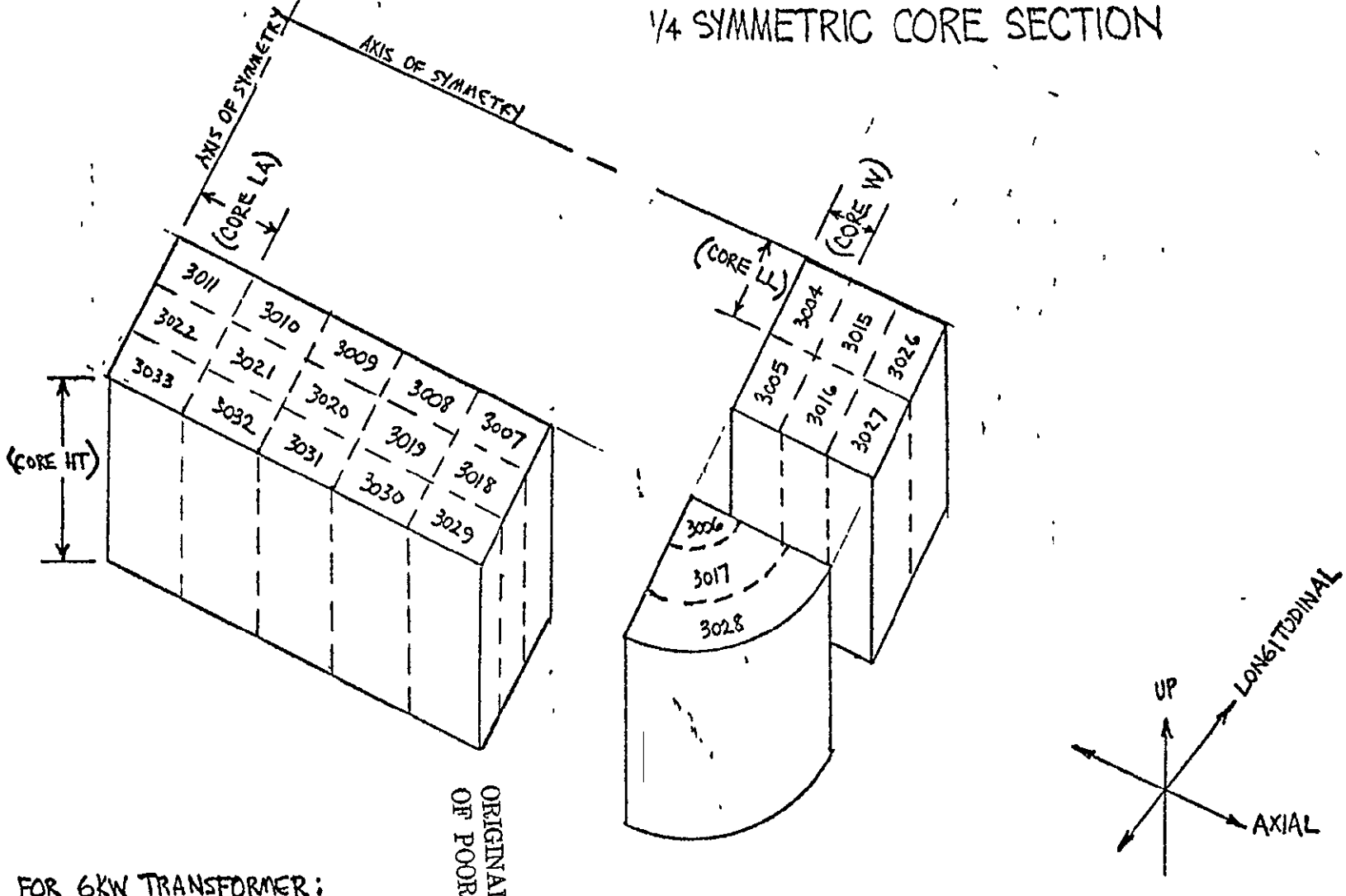


FIGURE 3-43. THERMAL MODEL - TRANSFORMER MOUNTING BRACKET

FIGURE 3-44. THERMAL MODEL I . . .

1/4 SYMMETRIC CORE SECTION



FOR 6KW TRANSFORMER:

CORE Ht = 1.0

CORE W = .3333

CORE LA = .35

CORE LL = .5

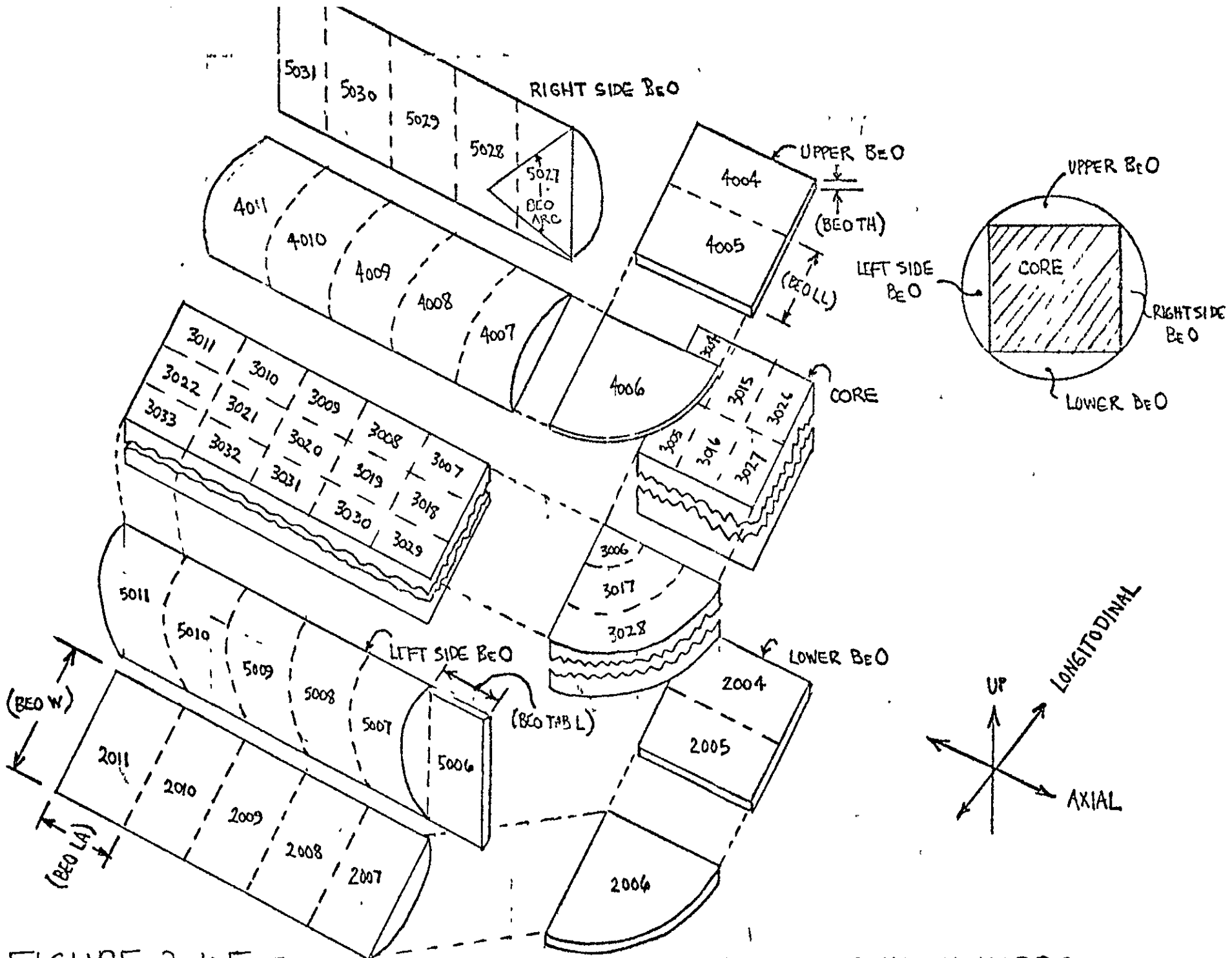


FIGURE 3-45. THERMAL MODEL - CORE AND CERAMIC INSULATORS

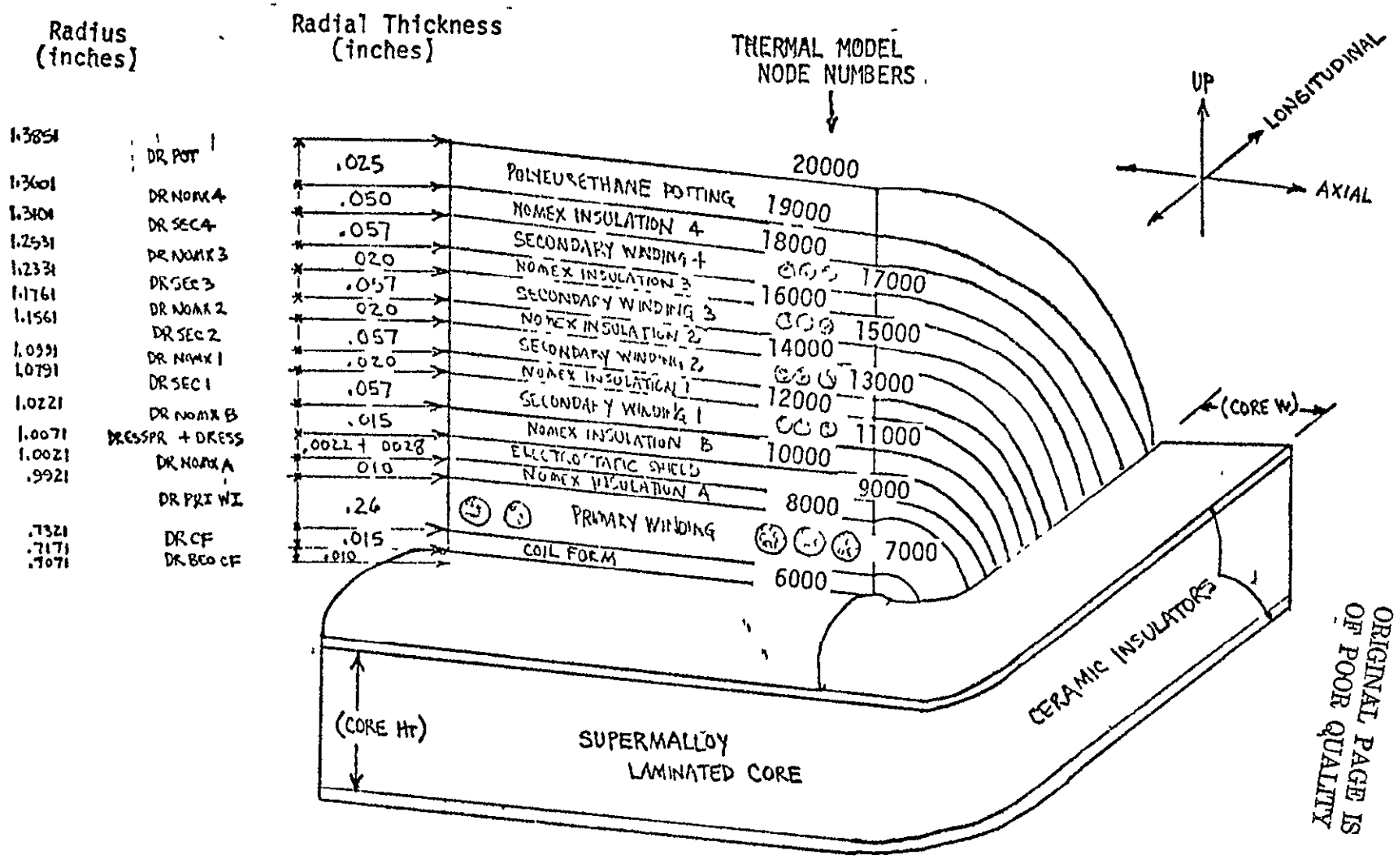
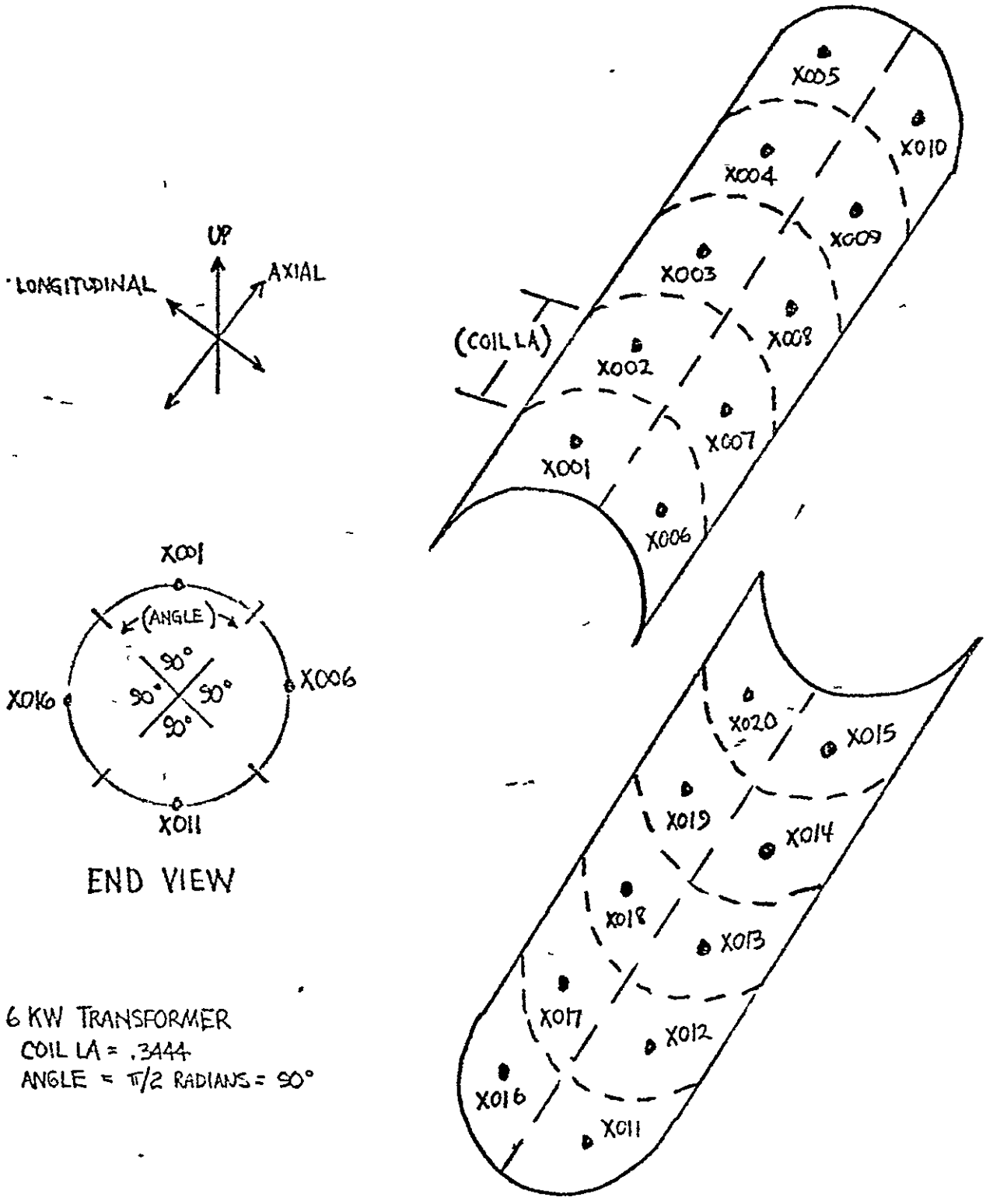


FIGURE 3-46. THERMAL MODEL - TRANSFORMER COIL



FOR 6 KW TRANSFORMER
COIL LA = .3444
ANGLE = $\pi/2$ RADIANS = 90°

FIGURE 3-47. THERMAL MODEL - TYPICAL COIL LAYER

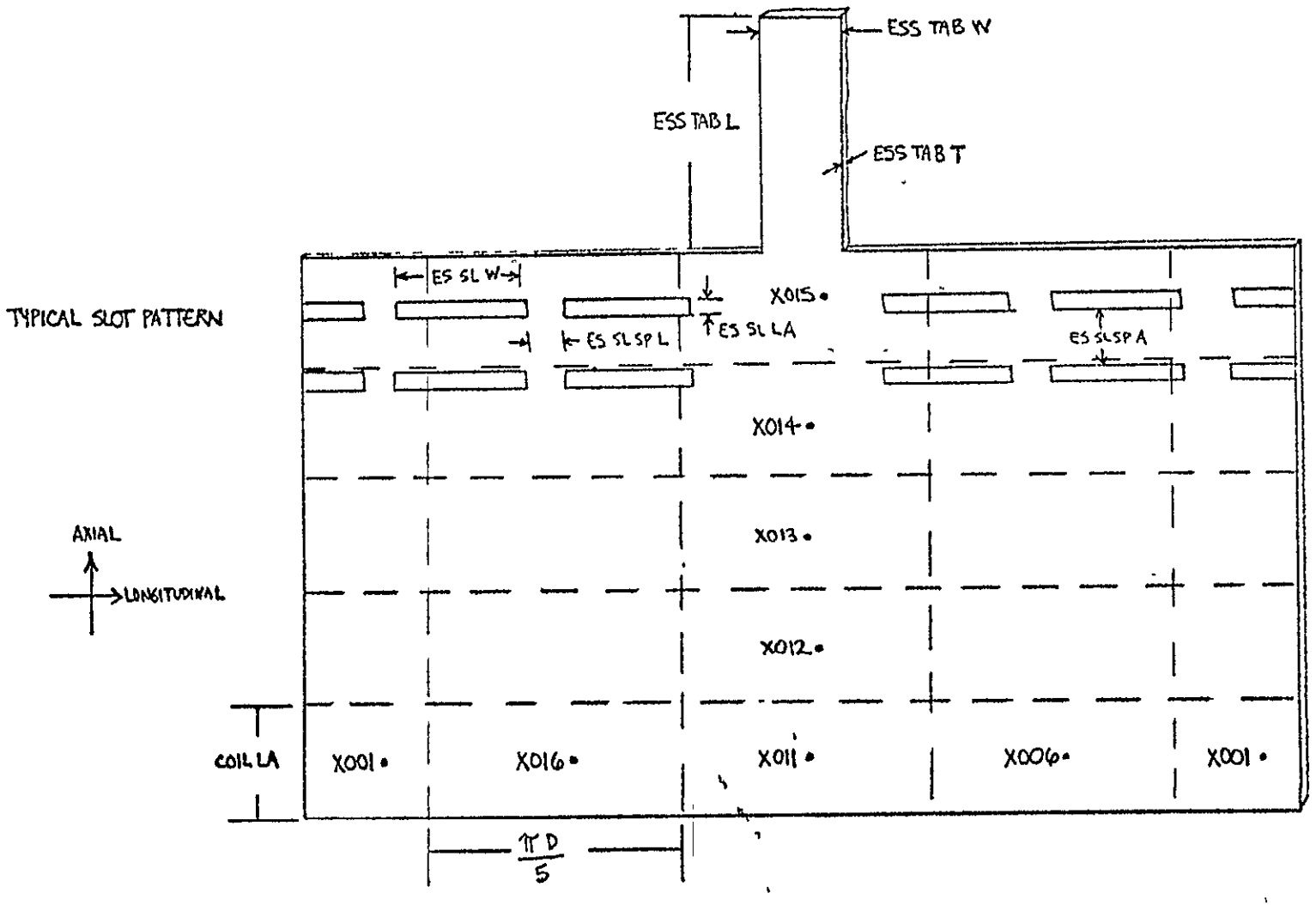
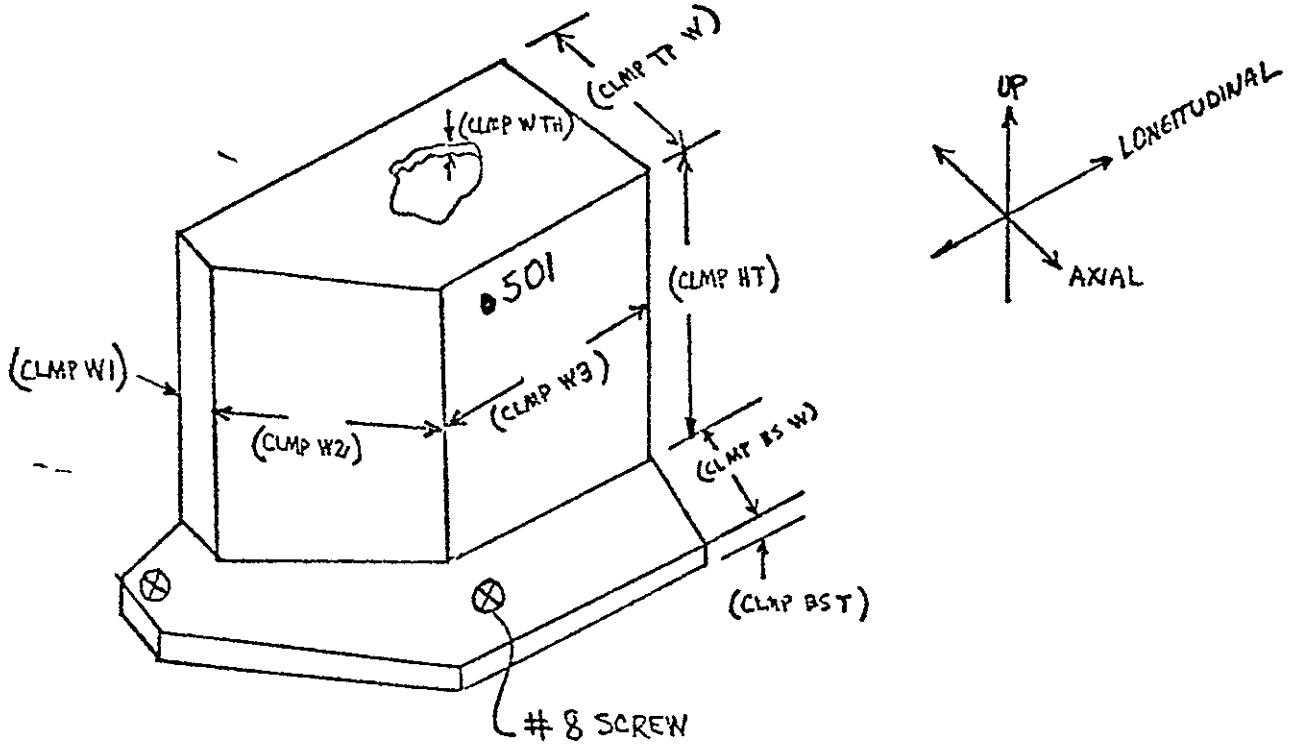


FIGURE 3-48 HERMAL MODEL - ELECTROSTATIC SHIELD



For 6KW Transformer

CLMP TP W = .65
CLMP HT = 1.18
CLMP W1 = .20
CLMP W2 = .80
CLMP W3 = 1.425
CLMP BS W = .35
CLMP BS T = .10
CLMP W TH = .06

FIGURE 3-49. THERMAL MODEL - HEAT CONDUCTING CLAMP CONNECTING CORE TO TRANSFORMER BRACKET

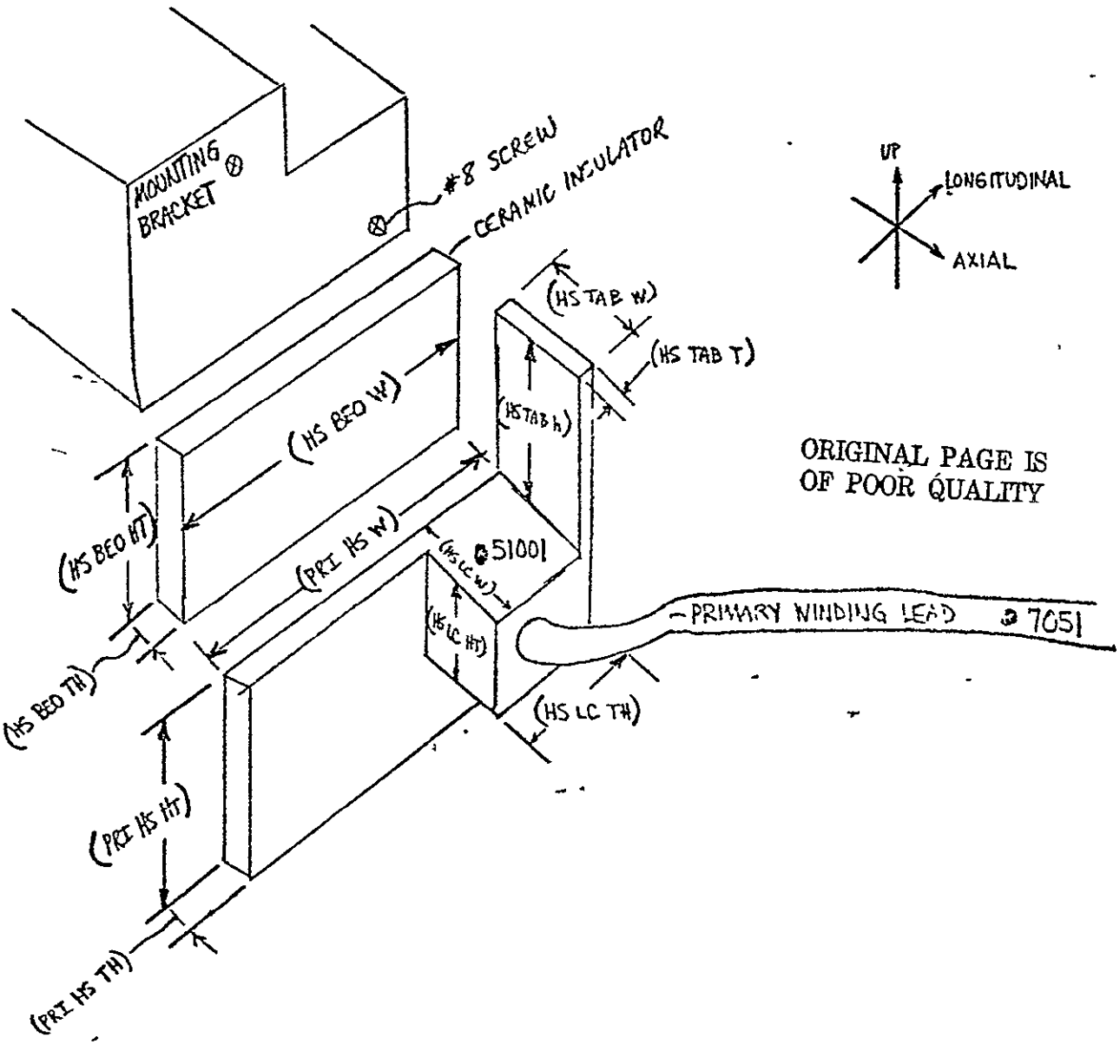


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FIGURE 3-50. THERMAL MODEL - PRIMARY WINDING : HEAT SINKING

The emissivity of the coil outer surface is 0.85
The emissivity of the mounting bracket is 0.90 (flat black paint)
The emissivity of the heat conducting damp is 0.90 (flat black paint)

e) Present Condition of Thermal Model

The thermal model of the 6KW transformer for use with the SINDA Thermal Analyzer program is maintained by the writer in the form of a deck of punched cards.

3.8.2 Thermal Analysis

a) Results

The results of the thermal analysis are presented in Figures 3-51 thru 3-56. These figures show the operating temperatures and the heat flow map for the transformer.

Figures 3-51, Transformer Heat Flow and 3-52. Coil Winding Heat Flow show the data for the 6KW transformer design with beryllium oxide ceramic insulators between coil form and core.

Figures 3-53, Transformer Heat Flow and 3-54, Coil Winding Heat Flow show the data for the 6KW transformer design with alumina ceramic insulators between coil form and core.

Figures 3-55, Transformer Heat Flow and 3-56, Coil Winding Heat Flow show the data for the 2KW transformer showing the comparison of the data utilizing the current thermal model and that from the previously developed thermal model.

6 KW ELECTRIC PROPULSION POWER PROCESSOR TRANSFORMER HEAT FLOW DIAGRAM

TOTAL TRANSFORMER POWER DISSIPATION = 59.6 WATTS

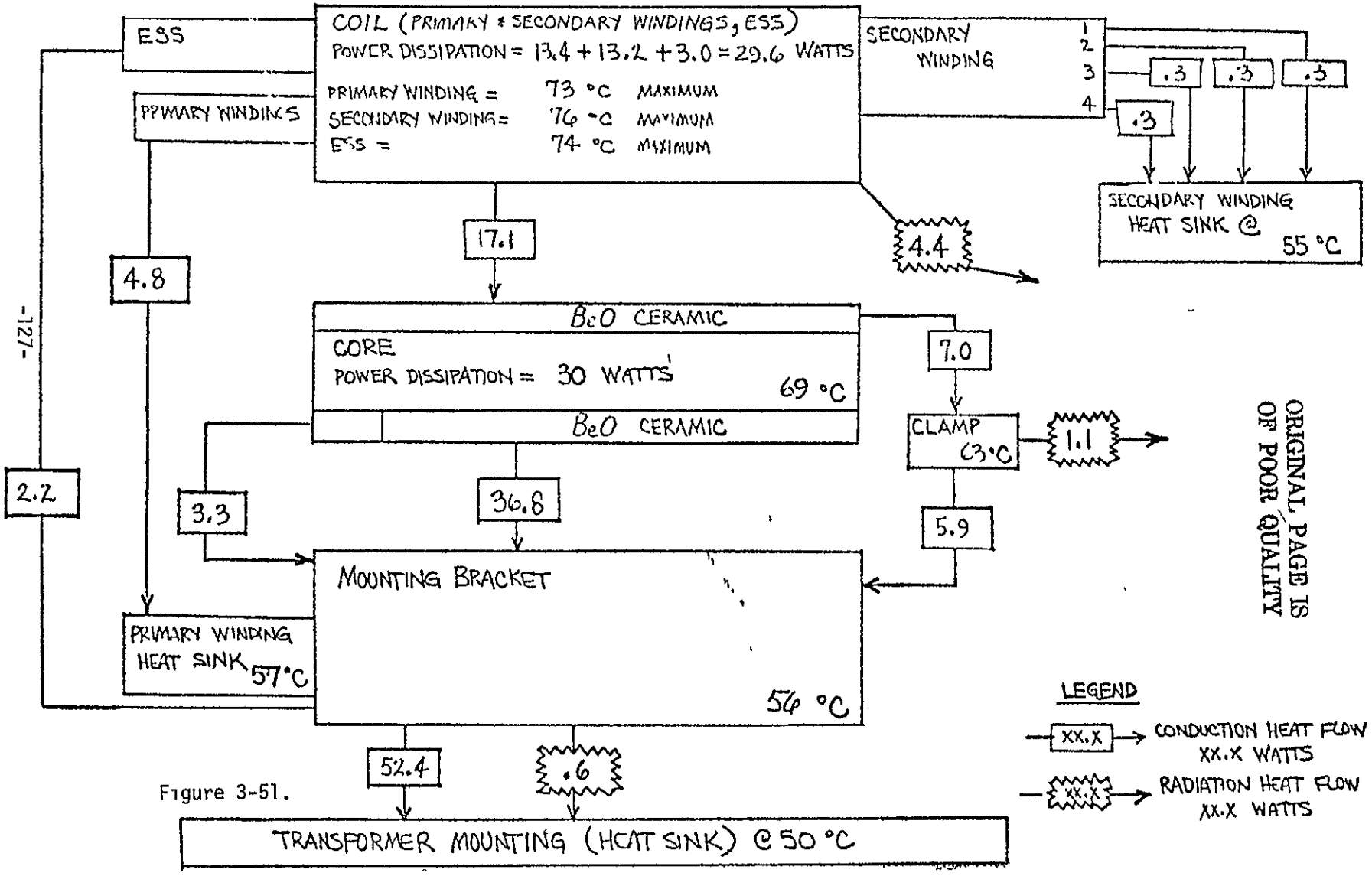
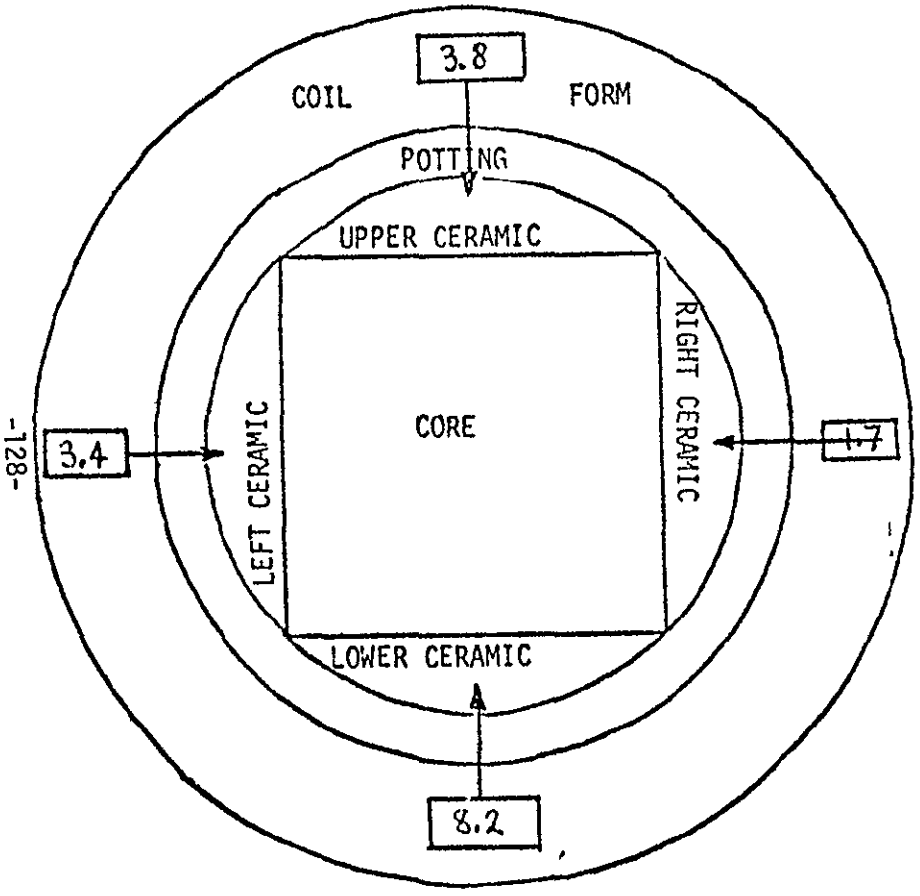


Figure 3-51.



TOTAL HEAT FLOW: 17.1 WATTS

Into UPPER Ceramic	3.8	watts (22% of total)
Into RIGHT Ceramic	1.7	watts (10 % of total)
Into LOWER Ceramic	8.2	watts (48 % of total)
Into LEFT Ceramic	3.4	watts (20 % of total)

FIGURE 3-52. HEAT FLOW MAP - COIL TO CERAMIC INSULATORS (Beryllium Oxide Ceramic)

6 KW ELECTRIC PROPULSION POWER PROCESSOR TRANSFORMER HEAT FLOW DIAGRAM

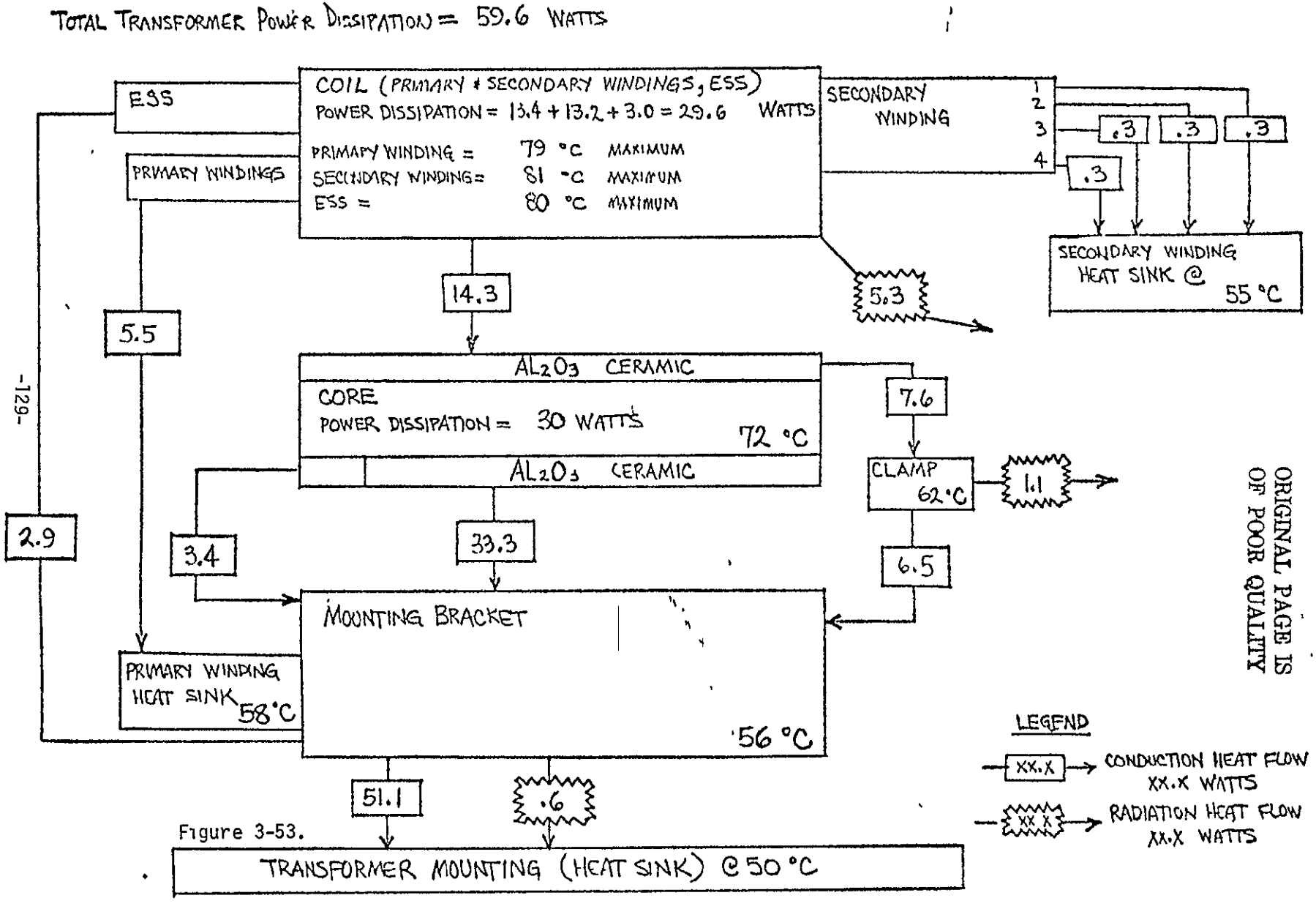
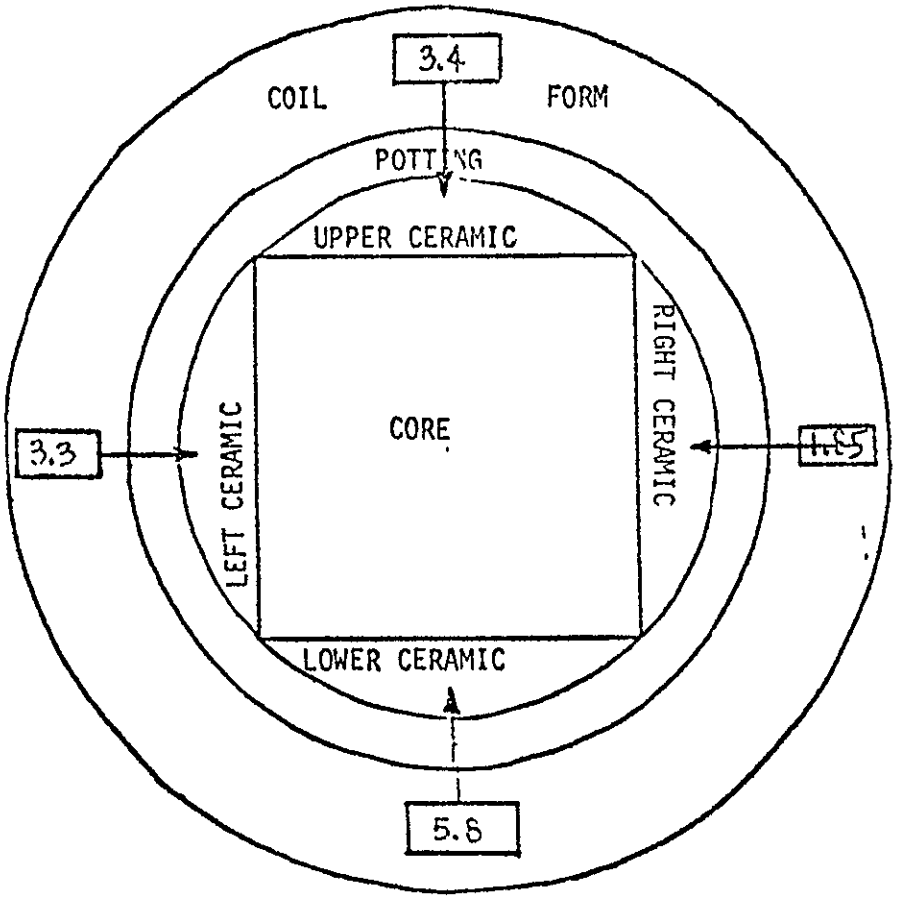


Figure 3-53.



TOTAL HEAT FLOW: 14.35 WATTS

Into UPPER Ceramic	3.4	watts	(24 % of total)
Into RIGHT Ceramic	1.85	watts	(13 % of total)
Into LOWER Ceramic	5.8	watts	(40 % of total)
Into LEFT Ceramic	3.3	watts	(23 % of total)

FIGURE 3-54. HEAT FLOW MAP - COIL TO CERAMIC INSULATORS (Alumina Ceramic)

2 KW ELECTRIC PROPULSION POWER PROCESSOR TRANSFORMER HEAT FLOW DIAGRAM

TOTAL TRANSFORMER POWER DISSIPATION = 26.9 WATTS (26.8)

VALUES IN (—) ARE FROM THERMAL MODEL PER REF (3) and REPORTED IN REFERENCE (1)

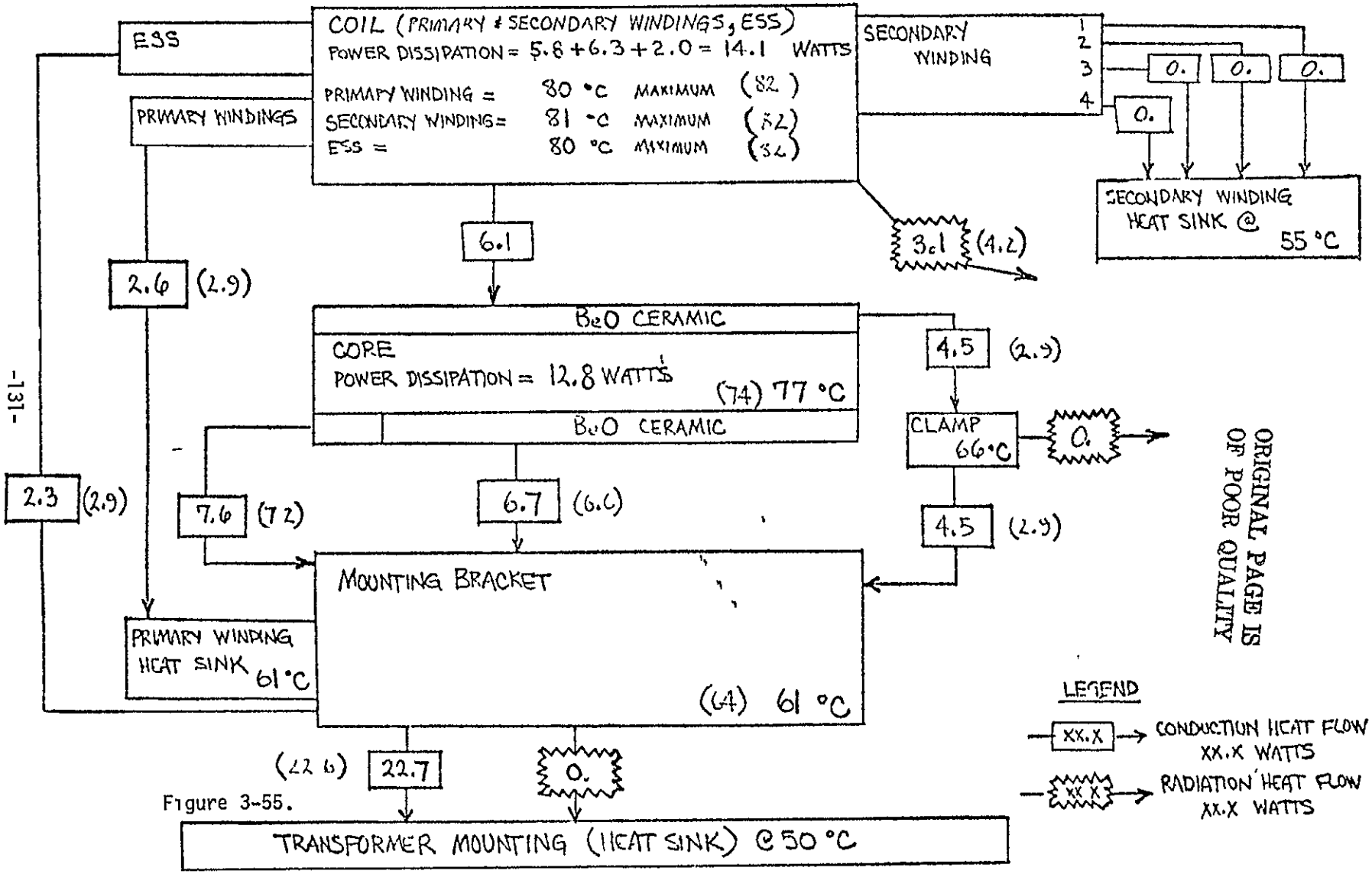
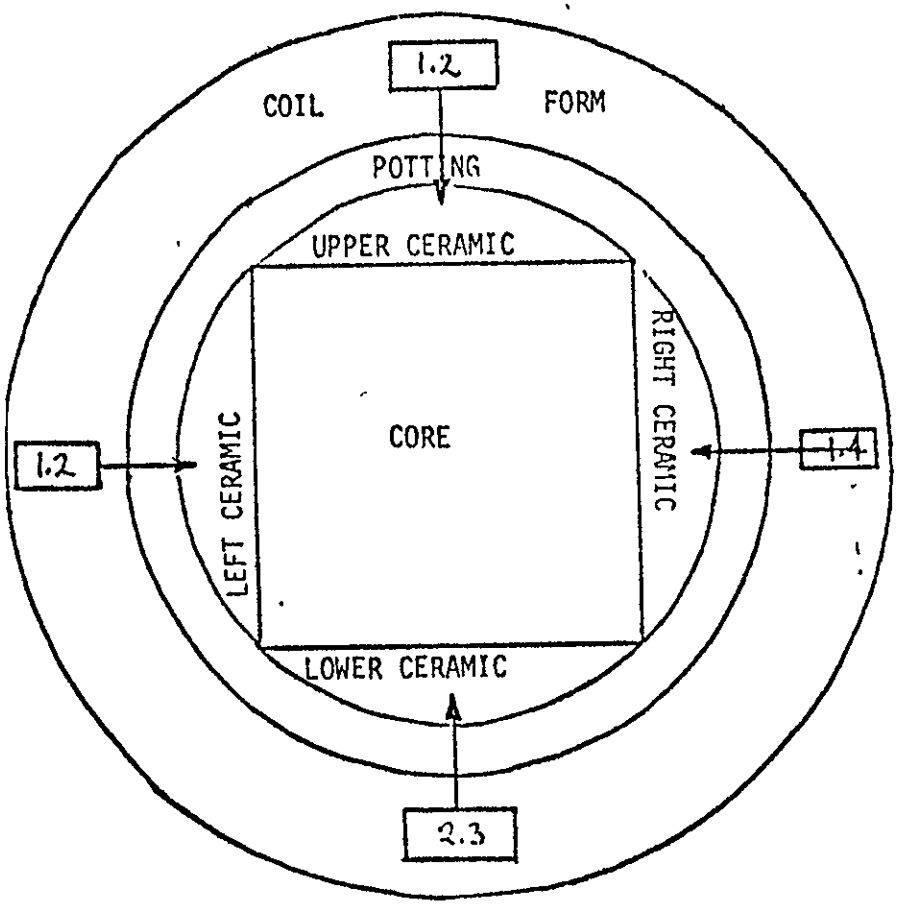


Figure 3-55.



TOTAL HEAT FLOW: 6.1 WATTS

Into UPPER Ceramic	1.2	watts	(20 % of total)
Into RIGHT Ceramic	1.4	watts	(23 % of total)
Into LOWER Ceramic	2.3	watts	(38 % of total)
Into LEFT Ceramic	1.2	watts	(20 % of total)

FIGURE 3-56. HEAT FLOW MAP - COIL TO CERAMIC INSULATORS (2KW)

3.8.3 Conclusions and Recommendations

While there is a significant advantages in the utilization of a good heat conducting material in the interface between the coil form and core its attachment to the mounting bracket to provide a low resistance heat flow path to the heat sink, the efficiency of this material is not directly proportional to the thermal conductivity of the material.

As can be seen from the comparison between the design incorporating the high purity beryllium oxide (thermal conductivity = 117 BTU/hr-ft-F [15.1W/in-C]) and the design incorporating alumina (thermal conductivity = 17 BTU/hr-ft-F [.75W/in-C]) to enhance heat transfer from coil and core to mounting bracket, the difference in maximum transformer hot spot is only 5°C. Even with the alumina, the maximum temperature is 81°C whereas the design goal is to achieve a maximum temperature of less than 85°C hot spot.

Based upon the present physical size of the transformer and its internal losses, there does not appear to be a sufficiently strong rationale to utilize the beryllium oxide when the alumina will be satisfactory. It is recommended that the alumina be used in this present configuration.

3.8.4 References

(1) Extended Performance Electric Propulsion Power Processor Design Study - Conceptual Design Review
4 August 1977, Contract NAS3-20403

(2) NASA Technical Memorandum NASA TM X-3473, Mass Study for Modular Approach to a Solar Electric Propulsion Module
NASA Lewis Research Center
Authors: Sharp, Cake, Oglebay, and Shaker
March 1977

(3) IOC 76.6821.5.4-1 dated 27 January 1976, Subject: EPP Thermal Analysis - CDR Inputs from C. T. Schumann to J. Biess.

3.9 Conceptual Mechanical Design

The structural and thermal interfaces were reviewed in order to be compatible with Bi-Mod power processor configuration. The power processor electrical design was also analyzed to determine the optimum modularization.

Figure 3-57 presents the mechanical packaging concept for a side-by-side power processor configuration. Figure 3-58 shows the interface module structure which is connected to the platform/evaporator heat saddle with its radiator panels. The two separate power processors are connected to the base of the evaporator saddle.

The power processor is divided up into three separate modules that can be individually tested. The modules are divided up into the following functions:

- Input filter, interface unit & low voltage outputs
- Beam supply & high voltage outputs
- Discharge supply & high voltage outputs

The cabling harness is recessed into the side of the power processor and is accessible through a cover plate.

The top of the evaporator saddle is available for other electronic hardware necessary for the interface module operation.

Table 3-XXI highlights the packaging concept featured for the power processor. This packaging concept is applicable to both the 6KW & 2.2KW beam supply designs.

Figure 3-58 presents an estimate of the 6KW power processor physical dimensions and volume, and is compatible with the proposed side of the platform/evaporator saddle.

Figure 3-59 presents an estimate of the 2.2KW power processor physical dimensions and volume.

Figure 3-60 illustrates the size of a typical 6KW beam module, location of large heat producing components and cutoff for the inter-connecting connectors and cable harness. With this location of the cable harness, the module can be easily removed for maintenance and testing.

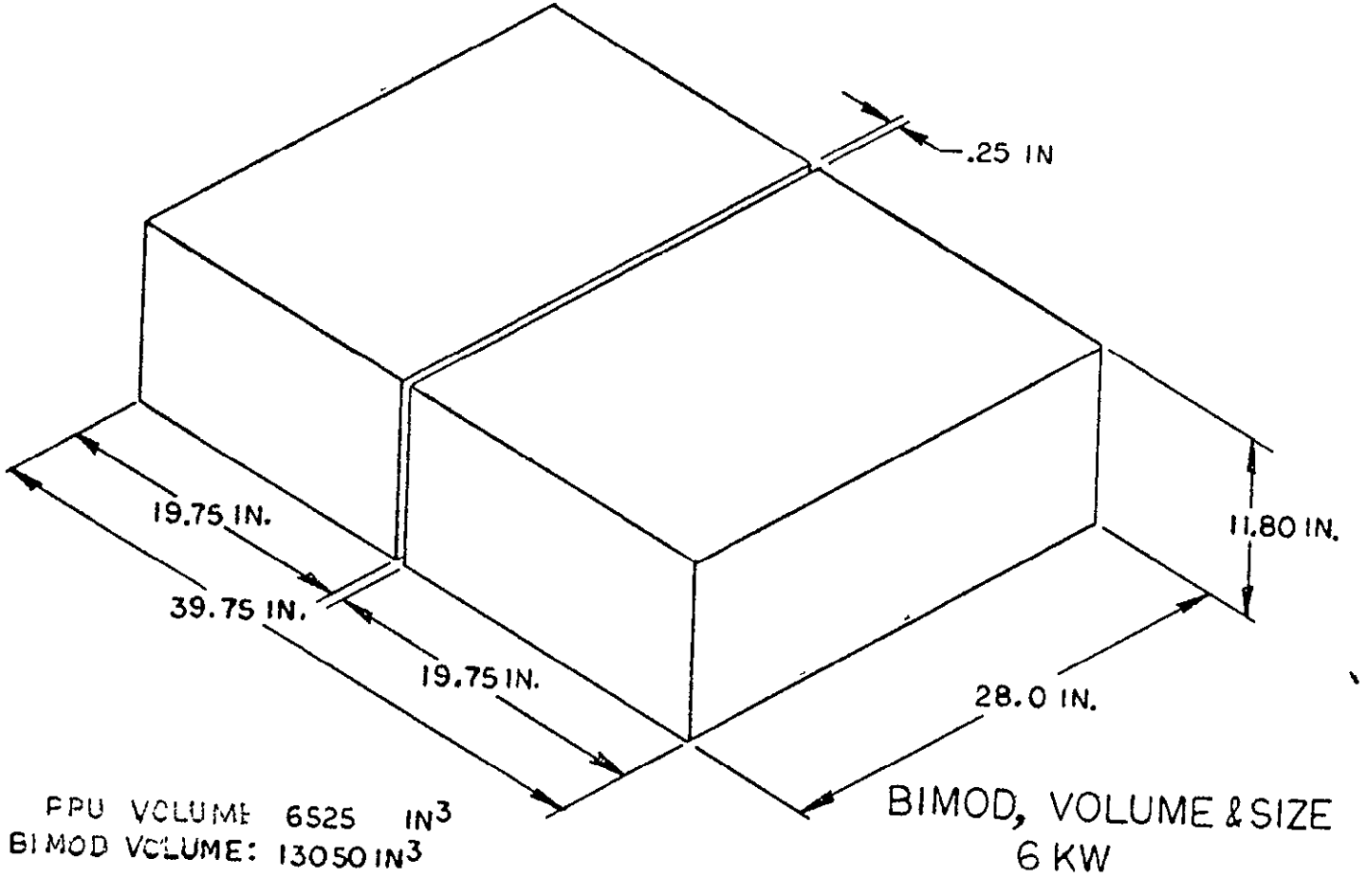


Figure 3-57 Size and Volume Estimate for 6KW Beam Supply Power Processor

Table 3-XXI Features of Bi-Mod Power Processor Conceptual Mechanical Configuration

- Power processor circuit packaged in three individually removeable modules.
- PPU enclosure consists of two (2) side walls, two (2) end walls and a top cover.
- Modules are screw fastened to the side panels, top cover, and finally to the platform/evaporator.
- Wire harness is internal to and captive to the PPU enclosure.
- Module connecting plugs are accessible thru covered ports in the side panels.
- External connectors (input/output and interface control) are located on the end panel facing the heat pipe radiators.

BIMOD, MECHANICAL/STRUCTURAL CONFIGURATION–
EXPLODED VIEW

Figure 3-58 Bi-Mod Power Processor Conceptual Mechanical Configuration

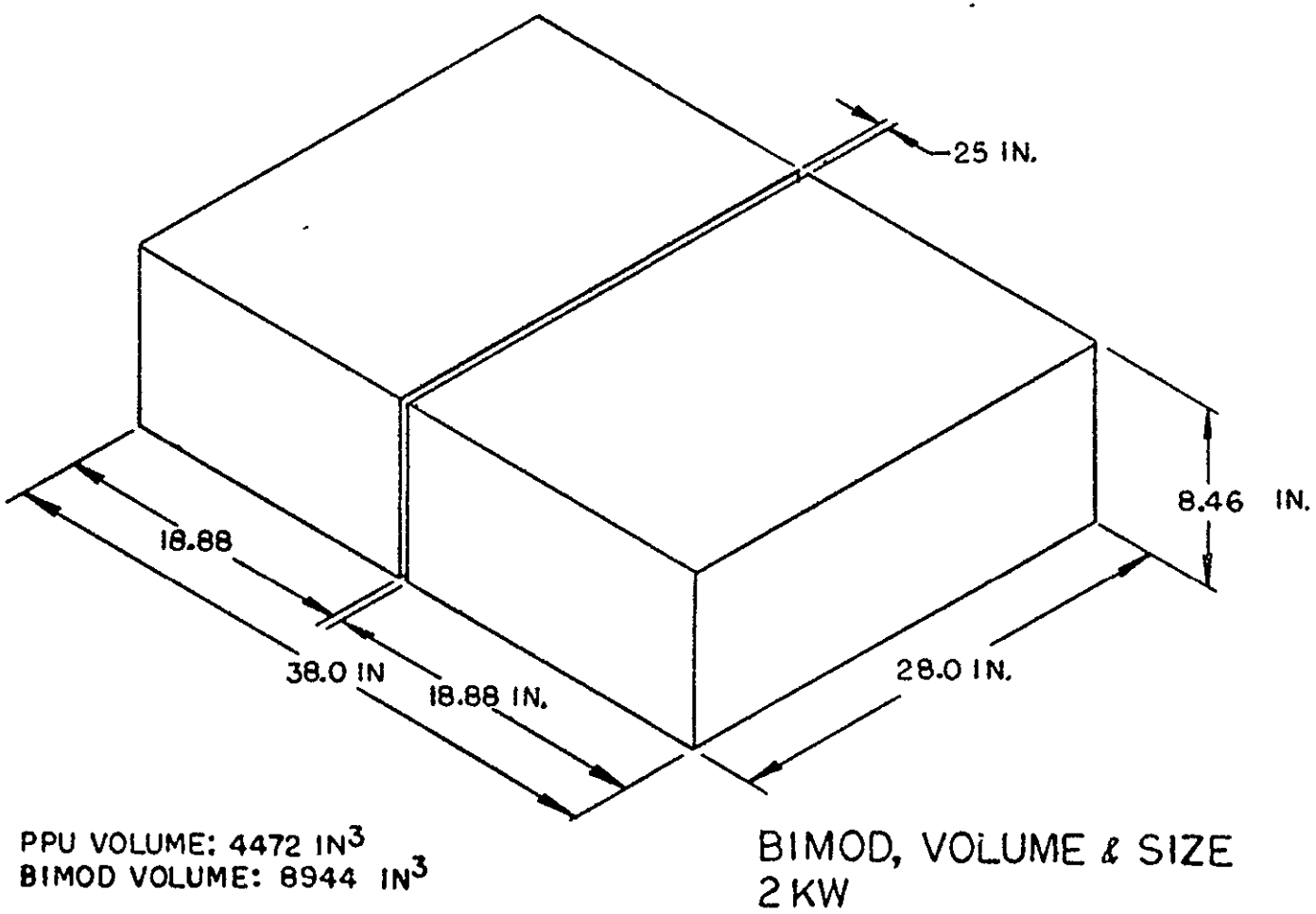


Figure 3-59 Size and Volume of 2.2KW Beam Supply Power Processor

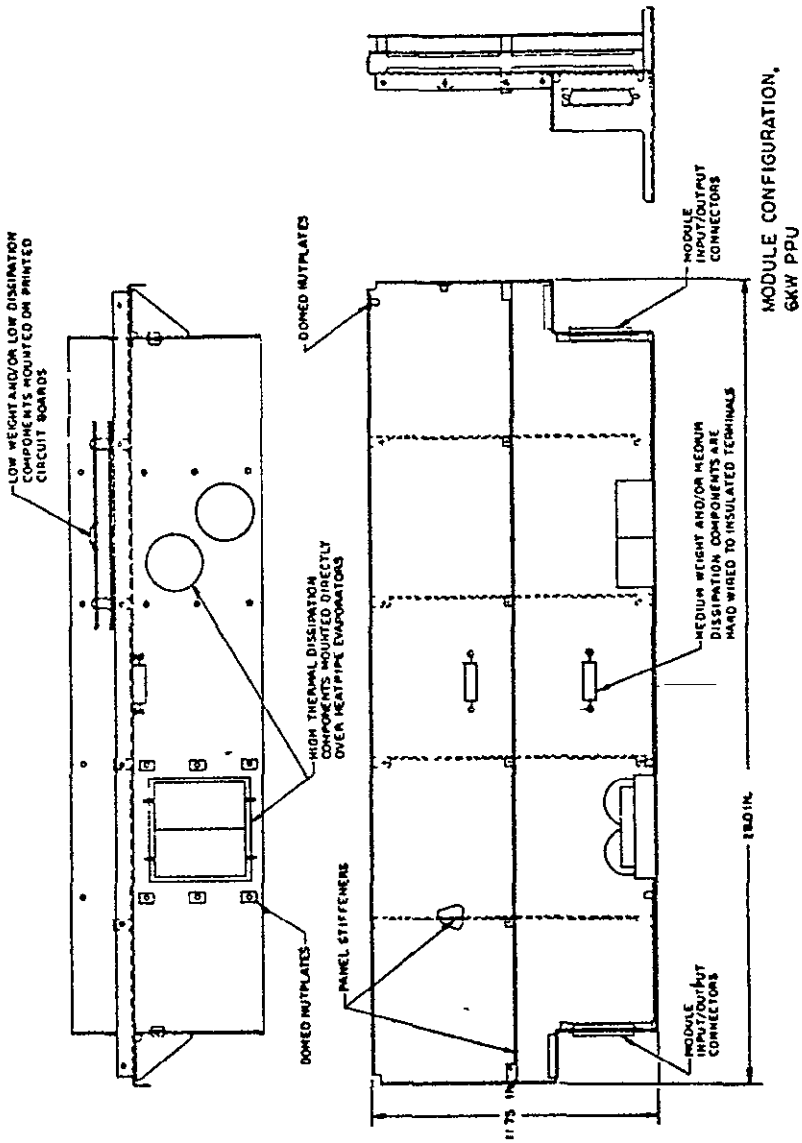


Figure 3-60 Proposed Module Subassembly

Table 3-XXII Mechanical Weight Estimate - 6KW Beam Power Processor

	LBS	GMS
Panel, Side	1.17	531.2
Panel, Side	1.17	531.2
Panel, End	1.76	799.04
Panel, End	1.76	799.04
Cover, Top	3.30	1498.2
Printed Ckt. Bds.	7.40	3359.6
Board Frames	3.00	1362.0
Modules	12.49	5670.4
Screws	3.39	1539.06
Nutplates	.75	340.5
Spacers	1.82	826.2
Wiring	4.00	1816.0
Connectors	1.40	635.6
Conformal Coat	1.11	503.9
Bonding & Potting	.75	340.5
Misc. Brackets & Insulators	1.00	454.0
	46.27	21006.4

Based upon the proposed packaging concepts, Tables 3-XXII and 3-XXIII present the mechanical hardware weight estimates for both the 6KW and 2.2KW power processors respectively.

Table 3-XXIII Mechanical Weight Estimate - 2.2KW Beam Power Processor

	LBS	GMS
Panel, Side	.80	363.9
Panel, Side	.80	363.9
Panel, End	1.20	547.34
Panel, End	1.20	547.34
Cover, Top	2.26	1026.27
Printed Ckt. Bds.	5.07	2301.33
Board Frames	2.05	932.97
Modules	8.55	3884.22
Screws	2.32	1054.26
Nutplates	.51	233.24
Spacers	1.25	565.95
Wiring	2.74	1243.96
Connectors	.96	435.39
Conformal Coat	.76	345.17
Bonding & Potting	.51	233.24
Misc. Brackets & Insulators	.68	311.
Total	31.7	14389.4

4.0 RISK ASSESSMENT

The design technical risks have been minimized due to the past development of the series resonant inverter circuit and the demonstrated operational reliability of three power processor breadboards.

- Thermal Vacuum Breadboard Contract NAS3-14383.
- New Technology Breadboard Power Processor Contract NAS3-18924.
- Electrical Prototype Power Processor Unit Contract NAS3-19730.

Present redesign activities further address component and circuit design techniques that can further reduce component weight, reduce losses and reduce overall component part count. By reducing part count, the unit production costs will also be reduced.

Risks can be identified in two basic areas; critical technologies and potential problems.

4.1 Critical Technologies

The electric propulsion technology is extending the state-of-the-art for high power processing technologies for space flight applications. For low weight, high efficiency and high reliability power processing equipment, new power semiconductors and power magnetics technology application must be used.

The following critical technologies have been identified:

- High speed, low loss power thyristors for the beam series resonant inverter.
- High speed, low loss power transistors for the discharge series resonant inverter.
- High voltage, high power beam transformer and power magnetics.

In order to maintain the low weight estimates for the power processor, it is necessary that component manufacturers continue to further improve and develop manufacturing lines that can produce the required high reliability power semiconductors.

Magnetic components are a major weight element for the power processor. Design techniques need to be improved in order to reduce magnetic component weight and provide the necessary thermal control for high reliability operation.

4.2 Potential Problem Areas

In order to obtain a flight power processor design that is ready for the future electric propulsion missions, it is necessary that a realistic schedule be adopted with timely funding of the different design, development, qualification and manufacturing phases.

Additional high power components development and qualification must be funded in support of the basic power processor schedule in order that timely high reliable component delivery will meet the power processor manufacturing schedule.

5.0 CONCLUSIONS

This study program has demonstrated that the electric propulsion power processor technology is capable of performing the planned electric propulsion mission applications. The program plan also demonstrates the capability of meeting the critical launch dates proposed for the Halley's Comet Mission.

In the event that the Halley Comet Rendezvous Program is not funded, alternate technology readiness programs can be initiated. The program includes the following:

a) Engineering/Qualification Model

b) Product Improvement Tasks

- 6KW Beam Supply
- 50kHz Discharge Supply
- Low Voltage Output Supplies
- Microporcessor Digital Interface Unit
- Component Improvement
  1) Beam power transformer
  2) Transformer potting material
  3) Transformer thermal control techniques
- Structural Thermal Mockup

The relative funding of each program is quite different with the product improvement cost being a lower cost compared to an Engineering/ Qualification Model.

The product improvement tasks ensures that the future Engineering/Qualification could be designed, fabricated and tested with minimum technical problems and would meet the contracted schedule and funding allotment.

The sequential funding of the two programs would be a cost effective approach where there is no immediate launch date that must be met.

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