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MODELING AND ANALYSIS OF POWER PROCESSING SYSTEMS (MAPPS)

(Initial Phase II)

FINAL REPORT

by

Yuan Yu, Fred C. Lee, Herb Wangenheim, Dan Warren

December 22, 1977

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Lewis Research Center
on
Contract NAS3-19690

to

TRW DEFENSE AND SPACE SYSTEMS
Power Conversion Electronics Department

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FOREWARD

This program was sponsored under Contract NAS3-19690, from the National Aeronautics and Space Administration, for the support and technical interface, we would like to acknowledge Mr. J.E. Triner of the Lewis Research Center, the NASA Project Manager.

Out appreciation also goes to Messrs. P.A. Thollot and F.F. Terdan of Lewis Research Center, and Messrs. A.D. Schoenfeld and B.J. McComb of TRW Defense and Space Systems, who realized the need for such a program, and lent support for its initiation as well as its completion.

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SUMMARY

The Phase-I MAPPS program started in 1973, amidst a growing concern on the need for and the lack of such a program. Being of a long-range nature, the MAPPS is currently at the conclusion of its initial Phase II.

The primary program effort focused on the formulation and implementation of various modeling, analysis, design, and optimization methodologies for power processing equipment and systems. The effort can be divided into four major categories:

- Control-dependent performance modeling and analysis.
- Control circuit design.
- Power circuit design and optimization.
- System configuration study and performance simulation.

The methodologies associated with each category were elaborated, so that a user with the proper background can proceed to follow the description and adapt the methodology to solve problems at hand. In addition to this tutorial fulfillment, those program efforts with general appeals to a multiple of perspective users were reduced into application-oriented subprograms, thus fulfilling as well the utility goal of the MAPPS program.

The program thus provided the engineering tools for conducting an analytically-based, cost-effective design of power processors, effecting ultimately the performance improvements and the cost savings for future NASA/military power processing development programs.

1. DEFINITION OF COMMONLY-USED TERMS

Certain modeling and analysis terminologies are defined here to avoid later ambiguity, as they are frequently used throughout the report:

Components: Electronic parts such as magnetics, capacitors, semiconductors, etc.

Circuit: A combination of electronic components to perform given functions. Examples are input filters, feedback amplifiers, etc.

Equipment: A collection of circuit functions to achieve certain specified input/output compatibilities. Examples are line regulators, dc-to-dc converters. A power processing equipment can be divided into the power circuit and the control circuit; the former processes the power flow from input to output, while the latter controls the power flow.

System: A combination of multiple equipment aimed to fulfill certain power processing requirements in a given application.

Performance: Steady state or transient behavior of an equipment or system. There are two general performance categories: the control-dependent performance and the power-dependent performance.

The control-dependent performances are those closely related to the control-circuit design for a given power circuit. They include:

- Stability of control loop
- Attenuation of source sinusoidal disturbances (audiosusceptibility)
- Response to load sinusoidal disturbances (output impedance)
- Response to step line disturbances
- Response to step load disturbances

The power-dependent performances are those closely related to the power-circuit design for a given control scheme. They include:

- Source EMI
- Output Ripple
- Input/output power and voltage levels
- Weight
- Loss

Design: Conceive a scheme for the equipment or system to meet a given set of performance requirements.

Modeling: Provide an adoptable representation of an equipment or system to facilitate performance evaluation or design implementation.

Simulation: To portray the time-domain performance of a given design. Its utility becomes most significant when multiple non-linearities render analysis impractical.

Design Optimization: To design the equipment or system and concurrently minimizing a defined quantity such as weight, loss, or a performance criterion.

2. INTRODUCTION

Electronic power processing is a complex field encompassing power and control electronics, magnetics, semiconductors, and nonlinear feedback control. However, due to the industry's preoccupation with hardware production, the technology development has been hampered by a lack of vigorous and cost-effective modeling, analysis, simulation, and design optimization techniques. Consequently, heavy reliance on empirical and intuitive methods as well as breadboard trial and error has been necessary in power processing development. Needless to say, such inadequacies inevitably lead to penalties in performance, reliability, weight/efficiency, and cost. In view of the following factors:

(1) The forthcoming use of considerably higher levels of power in future power processors,

(2) The prevailing trend of equipment standardization which must rely on analysis-based design and predictable performance,

(3) The ever-increasing sensitivity to equipment development cost,

the empirical and trial approaches will become increasingly impractical. The need for a power processing modeling and analysis program thus cannot be over-emphasized. The overall objective of such a program, then, is to provide the useful engineering tools to reduce the design, analysis/simulation, and design optimization time, and consequently the development time and cost, in achieving the required performances for power processing equipment and systems.

To fulfill such an objective, a program entitled "Modeling and Analysis of Power Processing System (MAPPS)", was initiated in 1973. Phase I of the program addressed the formulation of a methodology for the MAPPS approaches [1]. Subsequently, the program entered Phase II in 1975. Since then, certain selected approaches have been implemented through computer-based design, analysis, and optimization subprograms. To provide the basic coordination of various subprograms, the framework of an expandable Data Management Program is also completed. Being of long range nature, the program is currently at the conclusion of the initial Phase II.

Since the inception of the MAPPS program, TRW Defense and Space Systems Group has been working in unison with Dr. R.D. Middlebrook of the California Institute of Technology in a joint industry-university program effort. Sponsored by a subcontract from TRW to CalTech and supported by Dr. Cuk of CalTech, Dr. Middlebrook's major contribution has been in the modeling of various nonlinear dc-to-dc converter power stages based on a unified state-space averaging technique. Details of the modeling and the significant results obtained by CalTech are published separately in a companion NASA Contractor Report, NASA CR-135174.

This report volume, NASA CR-135173, summarized the analytical/numerical details of modeling, analysis, simulation, and optimization techniques pertaining to the conception of all subprograms generated at TRW in the MAPPS program. The report also contains narrative of softwares constituting the basic Data Management Program. For conciseness and clarity, certain minute details in mathematical derivations and computer programming are reserved for presentation in the Appendices at the end of the report. Prior to the conclusion, the report also includes an overview of MAPPS' present capability and its future expectation, supplemented by a follow-on program outline for the immediate next phase.

3. INTRODUCTION TO MAJOR MAPPS SUBPROGRAMS

Engineering tools on power processing design, analysis/simulation and optimization are provided in five major MAPPS subprograms, designated as the following:

- Performance Analysis Subprogram
- Control Design Subprogram
- Design Optimization Subprogram
- System Analysis Subprogram
- Component Library Subprogram

3.1 PERFORMANCE ANALYSIS SUBPROGRAM (PAS)

The utility of the PAS is to allow one to predict, for a given equipment design, all control-dependent performance characteristics listed in Section 1. A major difficulty in such analytical predictions lies in the nonlinear operation inherent in the power stage of all switching regulators. Generally there may be as many as three time intervals within each cycle of switching operation: the power transistor on-time interval during which the output inductor MMF ascends, the off-time interval during which the MMF descends, and if the descending MMF diminishes to zero, the rest of the off time interval when the MMF stays essentially at zero before the next cycle is initiated. Even though the power stage is linear for each time interval, the combination of all different linear circuits for the purpose of analyzing a complete cycle of switching-regulator operation becomes a complicated piecewise-linear analysis problem.

As stated in Section 1, the performances closeley associated with the analysis and simulation are stability, audiosusceptibility, output impedance, and large-signal step transient responses. Except when dealing with the last performance category, the nature of all other disturbances is that the regulator can be regarded as a time-invarient system without a significant loss in analytical accuracy. In other words, the nonlinear system can be linearized about its equilibrium state to obtain a linear analytical model for small-signal performance evaluations. For the last category concerning transient response, the generally varying duty cycle subsequent to a step line and load change represents a time-varying nonlinear system. For a proactical, higher-order system, its performance evaluation is invariably limited to tactics closely identified with simulation techniques.

Basic approaches for conducting performance analysis/simulation differ primarily in their methods of linearizing the nonlinear operation. They are classified as follows:

(1) Discrete Time Domain Anlaysis

Since a switching regulator inherently contains an analog-to-discrete time conversion, it is only natural that the regulator can be more accurately analyzed through the discrete time-domain equations in vector form. Newton's iteration is then used to reach the regulator equilibrium state. The system is then linearized about this equilibrium state to arrive at a linear, small-signal discrete time model. The entire closed-loop regulator is thus modeled as a single entity rather than separating it into different control blocks. The stability is studied by examining the eigenvalues of the linearized system. The analysis can be extended, through z-transform, to determine frequency-related performance characteristics such as audiosusceptibility. The modeling and analysis approach makes extensive use of digital computers, thus making automation in regulator analysis possible. The application of this approach to switching regulator was performed at TRW.[2,3]

(2) Impulse Function Frequency Domain Analysis

The approach is capable of describing accurately a nonlinear system under periodical structural changes. It is based on the fact that when a regulator is subjected to a small disturbance, its duty cycle is perturbed. Such a perturbed duty cycle signal can be regarded as an impulse train when the perturbation is vanishingly small. Through mathematical manipulation, a linearized discrete impulse response function is then generated for the nonlinear power stage in closed form at the discrete sampling instant. By neglecting the minute details of the waveforms between samples and studying only the macroscopic performance, an equivalent continuous linear impulse response is then obtained for the power stage. This approach was originated from the University of Toulouse, France and the European Space Agency [4,5], and supplemented by TRW [6].

(3) Average Time Domain Analysis

As far as the nonlinear power stage is concerned, the average time-domain approach also starts with the exact time-domain description. However, instead of treating the complete regulator as a single entity as the aforedescribed discrete time-domain approach, the average method divides the regulator into separate functional blocks and treats them as individual analytical entities. In general, these entities include the power stage, the analog signal processor for error detection and amplification, and the digital signal processor for converting the amplified analog error to discrete-time interval. Based on a practical assumption that the regulator-output switching ripple is small, the model then averages the exact state-space description of the respective power stages corresponding to distinct time intervals over a single period of operation. The culmination of the averaging process is an equivalent linear circuit power-stage representation about a quiescent operating point. The power stage model is then combined with the linear analog signal processor and the linearized digital signal processor (usually through describing function technique) to perform the small-signal analysis for a complete regulator. Infused by an earlier topological deduction [7], the evaluation of the averaging approach has been the contribution of CalTech [8,9].

(4) Discrete Time Domain Simulation

The previously described methods are applicable only to small-signal analysis. The reason for such restrictions stems from the fact that the system modeling is linearized about the equilibrium state for a given operating duty cycle. When a large disturbance is introduced, the duty cycle varies during the entire transient until a new equilibrium is reached. The time-variant operation thus renders the aforedescribed small-signal analysis powerless. In addition, other nonlinearities, such as those provided by protection circuits and saturation effects of the amplifier or magnetics, often are significant during large-signal transients. For example, all these nonlinearities are present during the regulator start-up process. A separate simulation task is thus needed.

The simulation is based on the discrete time domain model previously described. The technique utilizes the recurrent discrete time-domain analytical expressions, and propagates the recurrence through Fortran computation of state transition matrices and predetermined threshold boundary conditions. This simulation approach has been practiced frequently at TRW [2].

Techniques for all four approaches were well established in the MAPPS program. Their respective utility for a given application depends on the analysis objective, the desired accuracy, the control circuit type, the nature of the disturbance, and perhaps more influential than most, the analyst's own modeling preferrence. Detailed discussion on each approach, supplemented by specific analysis examples, will be given in this report.

3.2. CONTROL DESIGN SUBPROGRAM (CDS)

As stated previously, a power processing equipment is composed of of a power circuit handling the power flow and a control circuit regulating the power flow. A regulator's static and dynamic performances are effected, to a large extent, by the quality of its control circuit. The control design is thus instrumental in determining those external characteristics that are previously classified as control dependent.

For a given power circuit design, different control designs manifest themselves in various schemes of analog and digital signal processors. For most regulators, the design of the power stage and the digital signal processor is dictated by requirements other than control-dependent performances. For example, input/output isolation and source/load voltage compatibility frequently determine the power-stage selection, while the requirements of frequency constraint and the EMC consideration quite often impose the need for a constant-frequency digital signal processor. Consequently, the analog-signal processor generally holds the most leverage in determining the quality of the regulator control circuit.

The function of the Control Design Subprogram, therefore, is to utilize the power stage and the digital signal processor conceived elsewhere and to determine the design of the analog-signal processor in order to meet a set of specified control-dependent performance requirements. By necessity, the creation of such subprograms must rely on certain well-defined amplification and compensation configurations central to the design of analog signal processors. In the MAPPS program, analog signal processors of the following two categories are considered:

- Conventional Single-Loop Control
- Advanced Multiple-Loop Control [10,11]

Examples of control circuit design are demonstrated.

3.3 DESIGN OPTIMIZATION SUBPROGRAMS (DOS)

Unlike the previous two control-circuit oriented subprograms, the DOS concerns itself primarily with the power circuit. In a power converter, the number of variables to be designed invariably exceeds that of the constraints linking the variables to various performance requirements. Consequently, after the design constraints are defined, there exists virtually an infinite set of design solutions. The essence of the design optimization, therefore, is to pinpoint a set of design variables to meet all given constraints, and concurrently to achieve the optimization of a specific converter characteristic deemed particularly desirable. The characteristic can be the converter weight, loss, or any other physically-realizable entity. One of the unique features of the design optimization is that the converter switching frequency becomes a parameter to be designed through the optimization process, which is different from most other approaches in which the switching frequency is predetermined either intuitively or empirically.

Continued rapid growth by applied optimization as a scientific discipline has been fostered by the application of optimization theory and the high-speed computer developments. In converter design, it follows naturally that the key in implementing the optimization approach rests on the availability of suitable mathematical and computer techniques. A general optimization technique is the method of Lagrange Multipliers [12]. When applied to simple converter problems, the method usually yields closed-form optimized solutions. Several applications applied to the optimum inductor and transformer designs were demonstrated in this program.

Most larger problems arising from practical converter applications are sufficiently complicated to defy closed-form solutions. To identify an optimum design, one has to resort to nonlinear programming algorithms which provide fast convengence to optimum numerical solutions from an educated guess of an initial set of input design parameters. The "nonlinear" programming, as opposed to the well-developed "linear" programming, arises from the fact that most converter applications involving energy storage are simply based on formulations of highly nonlinear design constraints and optimization criteria. The principles and practices to effect convengence vary with each nonlinear programming. Methods based on penalty function [13] and general gredient [14] are among the more popular ones. In this program, the Sequential Unconstrained Minimization Technique (SUMT) based on the penalty-function approach was used, and optimization up to a complete step-down switching-regulator power circuit was demonstrated. [15,16]

3.4 SYSTEM ANALYSIS SUBPROGRAM (SAS)

The SAS's represent extensions of the aforedescribed PAS's and DOS's from the equipment to the system level. The SAS's rely on DOS techniques as the basic tool for identifying the optimum system configuration, and on PAS techniques to address the dynamic system performances under large-signal disturbances. An obvious constraint in pursuing the SAS is the awesome analytical/numerical effort generally required to analyze or design a system of even only moderate complexity. The progresses of SAS thus must be geared to those already made in the more fundamental DOS's and PAS's.

In this report, two examples of reasonable complexity were successfully demonstrated: one dealing with the weight optimization of a source-converter system, the other dealing with the dynamic response of a 12th order switching-regulator-inverter system. However, one must not let such limited success obscure the proper perspective - a truly useful SAS capable of allowing a more "scientific" system configuration design/analysis by minimizing the need for subjective bias from the system and equipment designers is still in its infancy. Long-range effort of considerably more intensity will be needed before truly prevalent SAS's can be developed for practical system analysis and design.

3.5 COMPONENT LIBRARY SUBPROGRAM (CLS)

The CLS, when completed, represents the arrays of useful data that are sufficient to completely characterize the rating and the behavior of various types of components commonly used in equipment design. The data is to be stored according to the following basic categories:

- Resistors: Carbon, Film, Wire-Wound, Precision
- Capacitors: Foil and Solid Tantalum, Ceramic
- Cores: Linear, square-loop, ferrite
- Diodes: Power, Signal, HV, Schottky
- Transistors: Power Switching, General Purpose
- Conductors: Solid, Litz
- IC's: Digital, Analog

In this report, components in the first three categories are partially comprised and stored. The structure of the data set was also implemented to facilitate random inquiries and to assume efficient retrieval, updating, and delete.

3.6 DATA MANAGEMENT PROGRAMS (DMP)

The DMP provides the needed coordination between the various subprograms and the users. In the designing the DMP, three critical considerations were observed:

- Ease of use
- Ease of modification and internal flexibility
- Portability from one computer host system to another

By observing these considerations in the DMP design, the user's effort may be concentrated on the analysis/design/optimization problem at hand, rather than on the administrative details of invoking the MAPPS system capabilities.

The normal use of the MAPPS involves interactive conversation between the MAPPS System and the user. The user begins by signing on and requests the MAPPS system be loaded and executed. A conversation then begins between the user and an executive routine through which the user instructs the system to attach certain external files and to perform specific analytic functions. Upon completion of the input cycle, the DMP will proceed to execute and satisfy the user's requests.

The user will be able to invoke various subprograms of analysis, design, and optimization. If intermediate results require a decision by the user, interactive conversation will again take place. During the course of an interactive session, the user may display results, store results, or retrieve previously stored results from the component library or the data base. The coordinated data management system is accomplished through the development of appropriate control and communication routines.

3.7 CONCLUSION TO SECTION 3

In this section, the major power processing subprograms and the data management program coordinating these subprograms were briefly discussed. From the foregoing descriptions, the MAPPS system present or future capabilities include the following major categories:

- Switching regulator control-dependent performance analysis through the Performance Analysis Subprogram.
- Basic control-circuit design to meet control-dependent performance requirements through the Control Design Subprogram.
- Detailed optimum power circuit design to meet given power-dependent performance requirements through the Design Optimization Subprogram.
- Identification of optimum systems configuration and large-signal system disturbance propagation through the System Analysis Subprogram.
- Retrieve best-fit components per user's instruction through the Component Library Subprogram.
- Coordinate between various subprograms and the user through a Data Management Program, aimed primarily for ease of use.

Each of these categories will be discussed in detail in the following sections.

4. PERFORMANCE ANALYSIS SUBPROGRAMS (PAS)

4.1 GENERAL DESCRIPTION

In this section, the approach and the scope of the analytical tasks are described. From the utility viewpoint, the PAS is regarded as both application and tutorial. The application aspect will be fulfilled by the creation of analysis and simulation subprograms based on certain preselected power/control circuit configurations. However, due to the large converter varieties of different power and control schemes, the function of the MAPPS program in terms of performance analysis/simulation must also be sufficiently tutorial so that a prospective beneficiary of the MAPPS program can follow the analytical methodology established in the PAS, and adapt the necessary analysis procedures to his specific applications.

The discussion starts with the nonlinear operation in switching regulators, to be followed by the description of different methodologies of linearization. Analysis methods including discrete time domain, impulse function frequency domain, and average time domain, are presented, and specific examples are given to illustrate each method. In addition, the discrete time domain analysis is extended to perform the discrete time domain simulation. Future PAS emphasis and expectation are also advanced.

4.2 NONLINEAR SWITCHING REGULATORS

4.2.1 Switching Regulator Block-Diagram Representation

To facilitate discussion, switching regulators can be characterized by the three basic functions shown in Figure 1: the power stage, the analog signal processor, and the digital signal processor. The power stage processes the power from input to output. The three basic power stages are shown here as buck, boost, and buck boost. They can operate either in continuous or discontinuous inductor current conduction modes. The analog-signal and digital-signal processors combine to regulate the power flow from input to output. An analog signal is derived from the power stage output, which is processed to deliver a discrete-time interval at the digital-signal processor output to achieve the required on-off control of the power switch in the power stage. The discrete-time voltage or current pulses thus generated are averaged by a low pass filter in the power stage to restore an analog signal at the power stage output, thus completing the switching-regulator control loop.

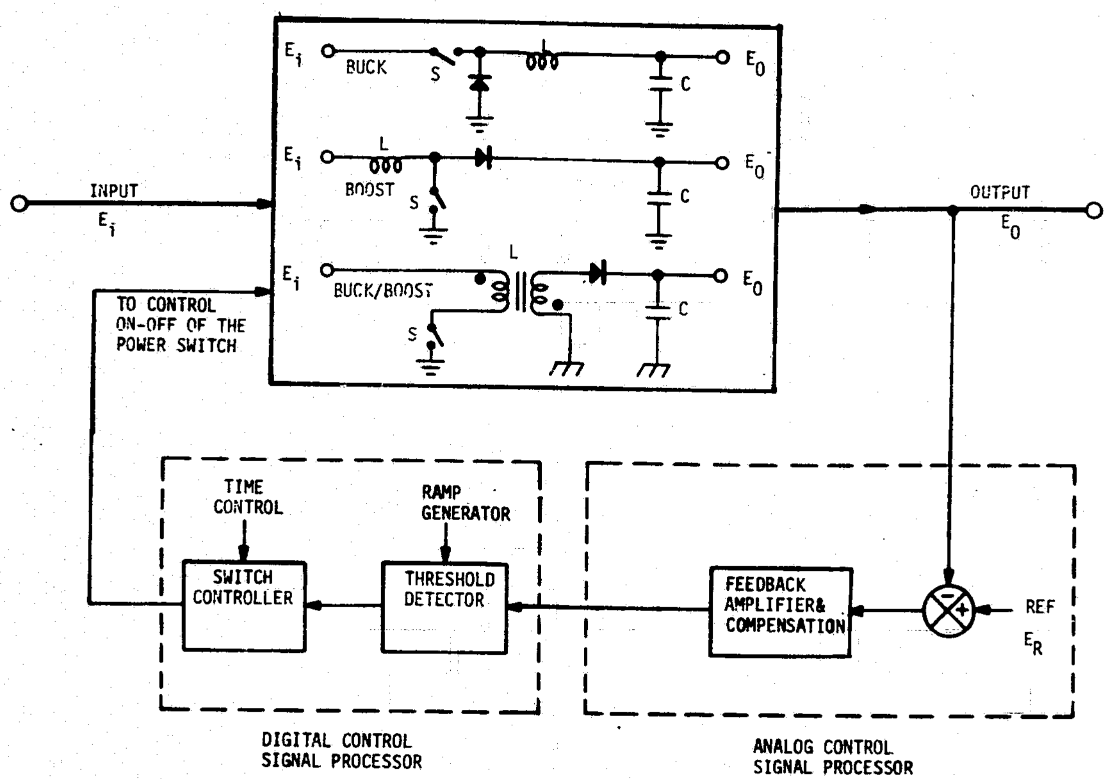


Figure 1 A Switching Regulator Basic Functional Block Diagram

4.2.2 Nonlinearities in Switching Regulators

4.2.2.1 Basic Nonlinearity in the Power Stage

Continuous and discontinuous conductions are sketched in Figure 2, using the buck-boost power stage as an example. In Figure 2(A) for continuous conduction, the MMF ascends in the input winding during T_{on} when the power switch is ON and the diode is OFF, and descends in the output winding when the power switch is OFF and the diode is ON. The MMF thus never vanishes in the output inductor. In Figure 2(B) for discontinuous conduction, the MMF ascends during T_{ON} in the input winding starting from zero MMF at the beginning of T_{ON}, and descends during T_{F1} in the output winding, reaching zero MMF at the end of T_{F1}. An additional time T_{F2} exists when both the power switch and the diode are OFF, during which the MMF remains zero in both input/output windings, and the load current is supplied by the output filter capacitor.

From the foregoing description, topologies of the buck-boost power stage correspond to T_{ON}, T_{F1}, and T_{F2} are illustrated in Figure 3. The figures make it clear that, even though the power stage is linear for each time interval, the combination of all different linear circuits for the purpose of modeling a complete cycle of switching-regulator operation becomes a piecewise-linear nonlinear analysis problem.

4.2.2.2 Basic Nonlinearity in the Analog- and Digital-Signal Processors

To characterize how a disturbance is propagated in the analog-signal-to-discrete-time-conversion, one is interested in how the duty-cycle variation d(t) of the power switch is being effected by a small sinusoidal disturbance derived from the processed error at the analog-signal processor output. Obviously, if one seeks the complete analytical transfer function of such a disturbance propagation, the function would have to include components not only of the disturbance frequency, but also its higher harmonics as well as the beat frequencies of the disturbance frequency and the regulator switching frequency. Thus a single frequency input results in an output of multiple frequencies - an inherent characteristic of nonlinear circuit operation.

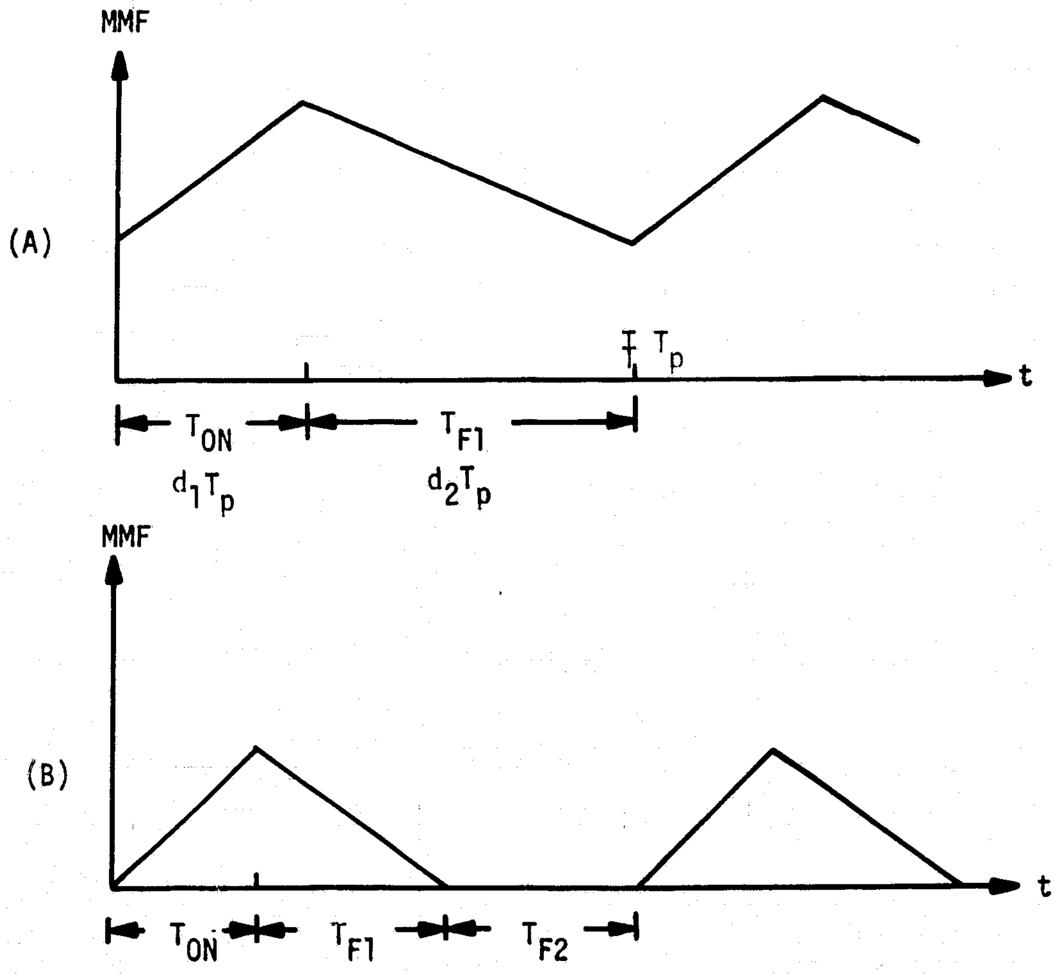


Figure 2 (A) Continuous and (B) Discontinuous Conduction Operations

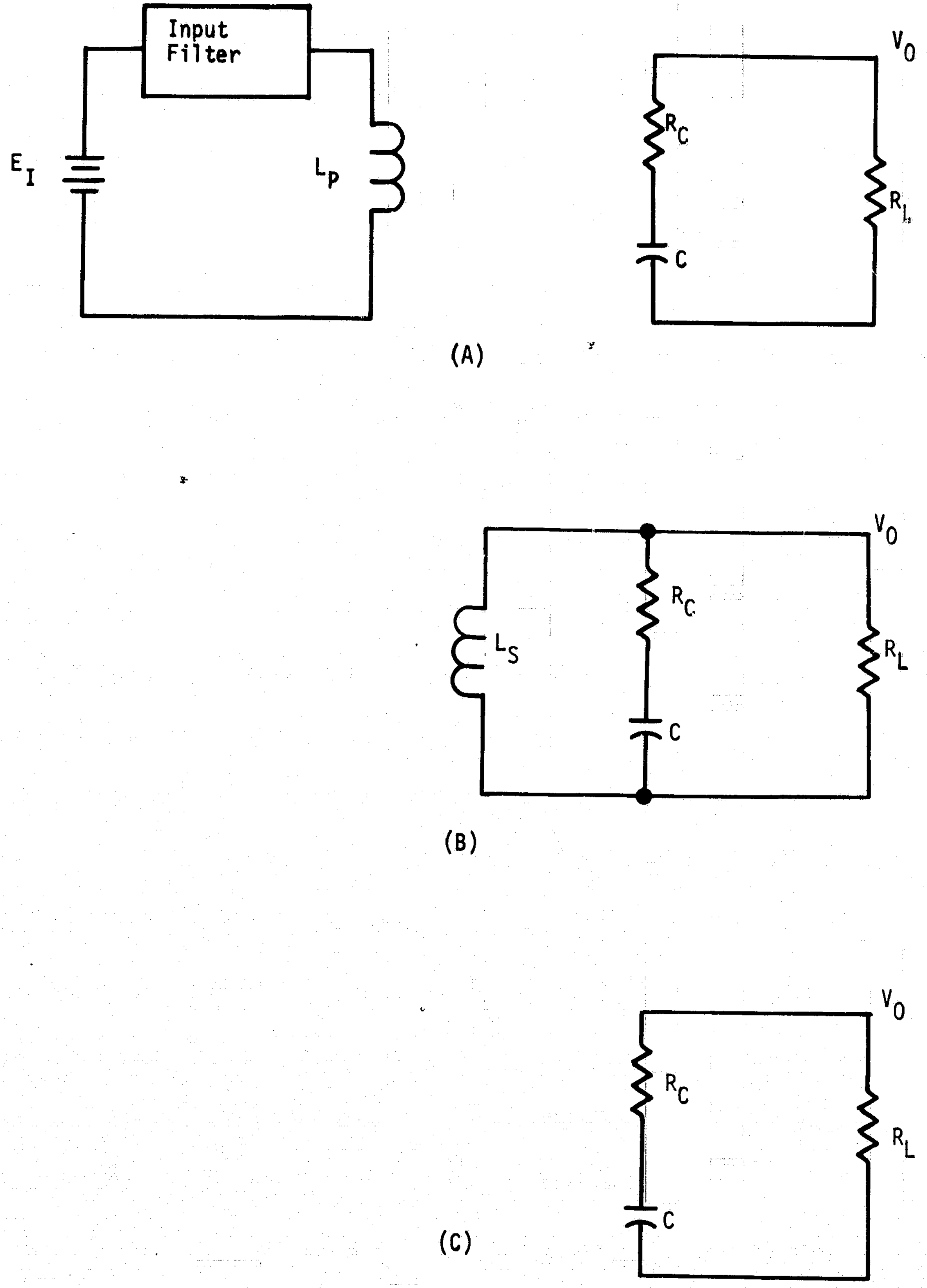


Figure 3 Buck Boost Converter Topology During: (A)T_{ON} (B)T_{F1} (C)T_{F2}

4.2.2.3 Other Significant Nonlinearities and Analytical Complications

In addition to the inherent nonlinearities previously described in the basic power stages and signal processors, other nonlinearities and complications include the following:

(1) The Effect of Input Filter

The complication provided by the input filter can be vividly demonstrated by Figure 3. Being an integral part of the power stage during T_{ON} in Figure 3(A), its presence vanishes in either Figure 3(B) or Figure 3(C), causing complications in the modeling of a linearized power stage for analysis purpose.

(2) Nonlinearities during Dynamic Operations

Certain nonlinearities ignored in the analysis of small-signal disturbance propagation become highly significant when a large-signal disturbance is introduced. They include filter inductor nonlinear flux-MMF relations, error-amplifier saturation, and the control asserted by certain protection circuits (e.g., peak current limiting) that are functional only during severe transient operations. For example, these nonlinearities are all present during the regulator start-up.

Having identified all major nonlinearities, the different methodologies of treating these nonlinearities, which result in different analysis/simulation approaches, will be discussed next.

4.3 LINEARIZATION METHODOLOGY

In this section, the analytical basis fundamental to all methodologies is presented. Methodologies resulting from different approximations made in the linearization process are then described. A concise comparison of all methodologies is provided.

4.3.1 Common Analytical Basis for All Methodologies

A common starting point for switching-regulator analysis is the identification of a state vector $\underline{X}$ and an input vector $\underline{U}$. The (nxl) vector $\underline{X}$ contains all the system state variables, while the (mxl) vector $\underline{U}$ is associated with regulator input voltage, the reference, the saturation drop of semiconductors, etc. For continuous conduction shown in Figure 2(A), the system representation is:

$$\dot{\underline{X}} = F1\ \underline{X} + G1\ \underline{U} \qquad \text{during } T_{ON} \tag{1}$$

$$\dot{\underline{X}} = F2\ \underline{X} + G2\ \underline{U} \qquad \text{during } T_{F1} \tag{2}$$

The (nxn) matrices F1 and F2 and the (Nxm) matrices G1 and G2 are constant matrices composed of various circuit and input parameters. In discontinuous-conduction operation an additional equation:

$$\dot{\underline{X}} = F3\ \underline{X} + G3\ \underline{U} \qquad \text{during } T_{F2} \tag{3}$$

is added to complete the system representation. The state trajectory during one switching period of propagation is illustrated in Figure 4, where the time instants at which switching action occur in steady-state operation are:

t_k, t_{k+1}, t_{k+2} : The initiation of T_{ON} interval
t_1^k, t_1^{k+1}, t_1^{k+2} : The initiation of T_{F1} interval
t_2^k, t_2^{k+1}, t_2^{k+2} : The initiation of T_{F2} interval

Each of the linear systems of equations (1) to (3) admits a closed form solution of the form:

$$\underline{X}(t_1^k) = \underline{X}(t_k+T_{ON}^k) = \phi 1\ (T_{ON}^k)\ \underline{X}(t_k) + D1(T_{ON}^k)\ \underline{U} \tag{4}$$

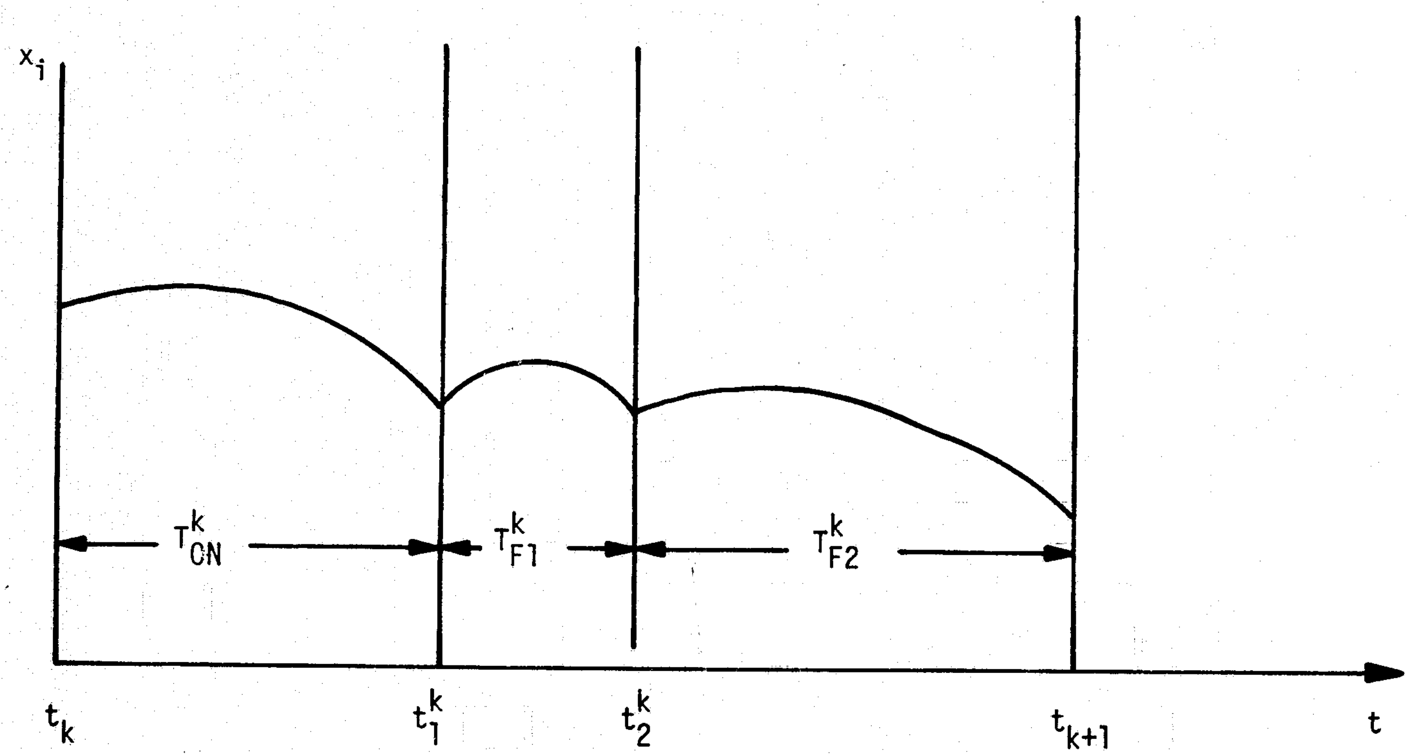


Figure 4 State Trajectory of One Switching Period of Operation

$$\underline{X}(t_2^k) = \underline{X}(t_1^k+T_{F1}^k) = \phi 2(T_{F1}^k)\ \underline{X}(T_1^k) + D2(T_{F1}^k)\ \underline{U} \tag{5}$$

$$\underline{X}(t_{k+1}) = \underline{X}(t_2^k+T_{F2}^k) = \phi 3(T_{F2}^k)\ \underline{X}(T_2^k) + D3(T_{F2}^k)\ \underline{U} \tag{6}$$

where

$$\phi i(T) = e^{FiT}, \qquad i = 1, 2, 3 \tag{7}$$

$$Di(T) = e^{FiT}\ [\ \int_0^T e^{-FiS}\ dS\ ]Gi, \qquad i = 1, 2, 3 \tag{8}$$

The discrete state transition equation for the converter in a complete switching cycle can be obtained by combining the state transition equation expressed by eqs. (4) to (6) as:

$$\underline{X}(t_{k+1}) = \phi\ \underline{X}\ (t_k) + D\ \underline{U} \tag{9}$$

where t_k and t_{k+1} correspond to time instants at the beginning of the k*th* and the (k+1)*th* cycle respectively. Combining the state transition equations for the continuous-conduction operation, the ϕ and D matrices in eq. (9) become:

$$\phi = \phi 2(T_{F1}^k)\ \phi 1(T_{ON}^k) \tag{10}$$

$$D = \phi 2(T_{F1}^k)\ D1(T_{ON}^k) + D2(T_{F1}^k) \tag{11}$$

For the discontinuous-conduction operation,

$$\phi = \phi 3(T_{F2}^k)\ \phi 2(T_{F1}^k)\ \phi 1(T_{ON}^k) \tag{12}$$

$$D = \phi 3(T_{F2}^k)\ \phi 2(T_{F1}^k)\ D1(T_{ON}^k) + \phi 3(T_{F2}^k)\ D2(T_{F1}^k) + D3(T_{F2}^k) \tag{13}$$

Time intervals T_{ON}^{k}, T_{F1}^{k}, and T_{F2}^{k} are determined through threshold conditions. For continuous operation, the two threshold conditions needed to determine T_{ON}^{k} and T_{F1}^{k} are the control-loop error and the implemented duty-cycle control method, which can be respectively expressed as:

$$\xi_1 \left[\underline{X}(T_k),\ T_{ON}^{k},\ T_{F1}^{k} \right] = 0 \tag{14}$$

$$\xi_2 \left[\underline{X}(t_k),\ T_{ON}^{k},\ T_{F1}^{k} \right] = 0 \tag{15}$$

In discontinuous operation, a third condition is added which detects the time instant at which the inductor MMF is reduced to zero:

$$\xi_1 \left[\underline{X}(T_k),\ T_{ON}^{k},\ T_{F1}^{k},\ T_{F2}^{k} \right] = 0 \tag{16}$$

$$\xi_2 \left[\underline{X}(t_k),\ T_{ON}^{k},\ T_{F1}^{k},\ T_{F2}^{k} \right] = 0 \tag{17}$$

$$\xi_3 \left[\underline{X}(t_k),\ T_{ON}^{k},\ T_{F1}^{k},\ T_{F2}^{k} \right] = 0 \tag{18}$$

Equations (9) to (18) thus represent exactly the nonlinear switching regulator system. Starting with an initial state, the equations can be used to compute recursively the state vector $\underline{X}$ for all succeeding time instants exactly without any approximation.

Notice that in this analysis method, the complete switching-regulator power and control circuits are treated as a single entity in the formulation of equations (1) to (3). There is no deliberate division among the power stage, the analog- and the digital-signal processors.

Direct application of this exact analytical basis for time-domain simulation is rather straight forward from a theoretical viewpoint. However, the numerical complexity involved and the need for a more readily-defined means of assessing the various control-dependent performances such as stability and audiosusceptibility have provided the impetus for many methods of linearization and approximation to branch out from this common basis. These methods are described next.

4.3.2 Discrete Time Domain Analysis Description

The discrete time domain analysis starts essentially with the common analytical basis described in the previous section. The entire regulator is treated as a single entity. Subsequent to the formulation of equation (9) and all the attendant threshold conditions, the following steps are followed to facilitate the control-dependent performance evaluation:

(1) Numerically Seek the Equilibrium State:

In steady state, eq. (9) can be written as:

$$\underline{X}^* = \Phi \underline{X}^* + D\underline{U} \tag{19}$$

The Φ and D matrices can be computed for a given T_{ON}, T_{F1}, and T_{F2}. Using the initial approximations for T_{ON}, T_{F1}, and T_{F2} obtained from given system input/output conditions (19), and substituting them into eqs. (9) to (18) as appropriate, an approximate steady state $\underline{X}^*$ is obtained. Using $\underline{X}^*$ as an initial setting, Newton's iteration method is employed to solve for the equilibrium state, during which eqs. (9) to (18) are computed continuously in the iteration process until a certain specified state-matching condition is satisfied. For example, the condition can be defined such that:

$$\sqrt{\sum_{i=1}^{n} [x_i (t_{k+1}) - x_i (t_k)]^2} < \varepsilon \tag{20}$$

when ε is an arbitrarily small number.

(2) Linearize the Discrete Time System

Equation (9) is nonlinear because the matrix Φ is a function of the time intervals T_{ON}^k, T_{F1}^k, and T_{F2}^k, which are all functions of the system state $\underline{X}(t_k)$ by virtue of the attendant threshold condition (14) to (18). The nonlinear equation is rewritten as:

$$\underline{X}(t_{k+1}) = f [\underline{X}(t_k), \underline{U} , T_{ON}, T_{F1}, T_{F2}] \tag{21}$$

For a constant $\underline{U}$, equation (21) is linearized about $\underline{X}^*$ as:

$$\delta\underline{X}(t_{k+1}) = \left.\frac{\partial f}{\partial \underline{X}}\right|_{\underline{X}^*} \delta \underline{X} (t_k) \tag{22}$$

where

$$\Psi = \left.\frac{\partial f}{\partial \underline{X}}\right|_{\underline{X}^*} \tag{23}$$

is a (nmn) matrix. The partial differentiation $\partial f/\partial \underline{X}$ can be performed analytically if the problem is simple. Otherwise, it must be computed numerically through the difference quotients.

(3) Stability Analysis

Once the matrix Ψ is conceived for the linearized system, its eigenvalues are evaluated. The linearized system, as represented by eq. (22), is stable if and only if all the eigenvalues of Ψ are absolutely less then unity,

$$|\lambda_i| < 1 \qquad i = 1, \cdots n \tag{24}$$

Changes of eigenvalues as a function of system parameters can be plotted in the complex Z-plane. Locations of eigenvalues in the Z-plane indicate not only the stability but also the system transient behavior, i.e., damping and rapidity of response.

(4) Audio Susceptibility Analysis

The audiosusceptibility analysis deals with how a small sinusoidal disturbance of the dc supply voltage E_i affects the regulated output voltage E_o. The audiosusceptibility of the regulator is, in essence, the regulator's closed-loop input-to-output transfer function. If E_i becomes time-varying, but sufficiently slow so that the input voltage can be considered essentially constant over a switching period, then eq. (21) can be linearized about the previously-defined equilibrium state $\underline{X}^*$ and the nominal dc input voltage E_I as:

$$\delta\underline{X}(t_{k+1}) = \Psi\delta\,\underline{X}(t_k) + \Gamma\,\delta\,e_i(t_k) \tag{25}$$

where

$$\Gamma = \frac{\partial f}{\partial e_i}\bigg|_{X^*,\,E_I} \tag{26}$$

and

$$\delta e_i(t_k) = E_i(t_k) - E_i \tag{27}$$

that is, the time varying $E_i(t)$ now contains a dc component E_I plus a small ac component $\delta e_i(t)$. The output voltage E_o can be expressed as

$$E_o(t_k) = C\, \underline{X}(t_k) \tag{28}$$

where C is a constant (1xn) row matrix. Applying Z-transform to eq. (25), one has:

$$\delta \underline{X}(Z) = (IZ - \Psi)^{-1}\, \Gamma\, \delta\, e_i(Z) \tag{29}$$

The frequency-domain audiosusceptibility transfer function can be derived after replacing Z by $e^{j\omega T_p}$ and combining eqs. (28) and (29),

$$G(jw) = \frac{\delta e_o(jw)/E_o}{\delta e_i(jw)/E_I} = \frac{E_I}{E_o}\,\frac{\delta e_o(jw)}{\delta \underline{x}(jw)}\,\frac{\delta \underline{x}(jw)}{\delta e_i}$$

$$= \frac{E_I}{E_o}\, C\,(Ie^{j\omega T_p} - \psi)^{-1}\Gamma \tag{30}$$

4.3.3 Impulse-Function Analysis Description

In this analysis, the three general control blocks shown in Figure 1 are treated as three separate entities. During one cycle of switching operations as illustrated in Figure 2(B), the regulator power stage can be represented by equations (1) to (3) of the previous section, namely:

$$\underline{X} = F1\, \underline{X} + G1\, \underline{U} \quad \text{during } T_{F1} \tag{31}$$

$$\underline{X} = F2\, \underline{X} + G2\, \underline{U} \quad \text{during } T_{F2} \tag{32}$$

$$\underline{X} = F3\, \underline{X} + G3\, \underline{U} \quad \text{during } T_{ON} \tag{33}$$

The difference between equations (31) to (33) and equations (1) to (3) of the previous section is that the F's, the G's and the X now only contain power stage parameters. When the regulator is subjected to a small disturbance, the duty-cycle signal d(t) is modified as $d(t)+\Delta d(t)$, shown as Figure 5. Such a perturbed duty-cycle signal can be idealized as an impulse trains when the perturbation is vanishingly small.

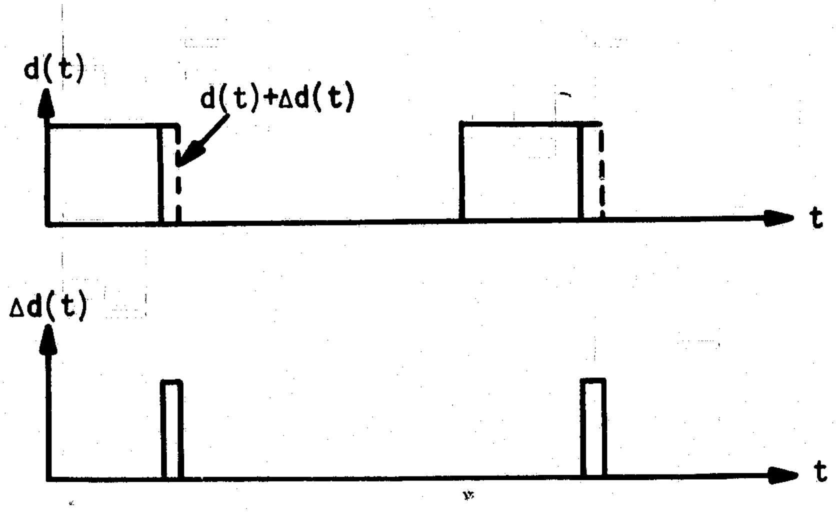


Figure 5 Perturbation of Duty Cycle d(t)

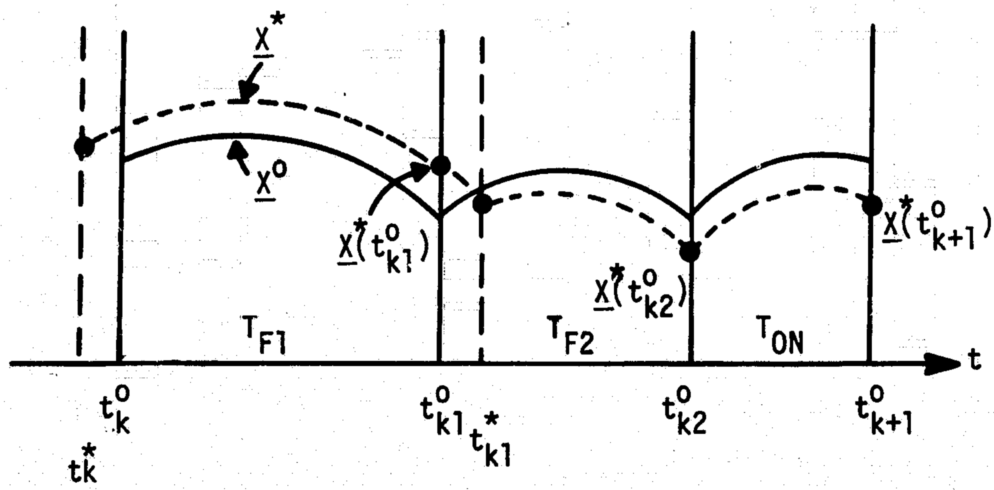


Figure 6 State Trajectories for steady state and for small perturbation

A linearized discrete impulse response, which characterizes the small-signal behavior of the power stage about its equilibrium state, can be obtained if the output-voltage perturbation $\Delta V_o(t_{k+n})$ due to a $\Delta d(t_k)$ at the Kth cycle can be computed after n cycles of operation. The sampling rate is the switching frequency $1/T_p$. Analytically, one wishes to express the discrete impulse response $g(nT_p)$ in a closed form as power-stage circuit parameters and operating conditions:

$$g(nT_p) = \frac{\Delta V_o(t_{k+n})}{\Delta t_k} \tag{34}$$

Let the state trajectories for steady state and perturbed state be illustrated in Figure 6 as solid and dotted curve respectively. The instants of switching are denoted by a superscript "o" for the steady state, and by a superscript "*" for perturbed state. For a small duty-cycle perturbation at Kth cycle from t_k^o to t_k^*, the perturbed state after one cycle of propagation is $\underline{X}^*(t_{K+1}^o)$. Using the closed-form solution of equations (31) to (33) which are similarly in form to those expressed in equations (4) to (6) of the previous section, one can then express $\underline{X}^*(t_{k+1}^o)$ in terms of the t_k^*. Since the output voltage V_o can be expressed as:

$$V_o = C\,\underline{X} \tag{35}$$

When C is a constant row matrix, the $g(nT_p)$ in equation (34) can be obtained through the following vector differentiation

$$g(nT_p) = \frac{C\,d\underline{X}^*(t_{k+n}^o)}{dt_k^*} \tag{36}$$

Equation (36) can be shown to be the following:

$$g(nT_p) = C\Phi^n(T_p)\,B \tag{37}$$

were

$$B = (F3-F1)\,\underline{X}^o(t_k^o) + (G3-G1)\,\underline{U} \tag{38}$$

Equation (37) thus characterizes the small-signal behavior of the regulator power stage exactly at the sampling instants following a duty-cycle perturbation $\Delta d(t)$.

To forsake the details between samples, an equivalent continuous linear impulse response g(t) can be obtained simply by substituting $t = nT_p$ in equation (34).

Such a transform is made plausible by the low-pass filter inherent in most regulator power stages. The continuous linear response g(t) thus characterizes the small-signal, low-frequency behavior of the regulator, up to one-half of the switching frequency. Once g(t) is obtained, the corresponding frequency-domain transfer function G(s) follows.

The key to this linearization method is therefore, equation (34), which linearizes the nonlinear system by considering a samll-signal disturbance about its equilibrium state, thus allowing the exact portrayal of the regulator's small-signal behavior at the discrete sampling instant. The simplification based on a much shorter switching period in relation to the output-filter time constant is then invoked to extend the response from discrete to continuous.

The foregoing presentation summarizes the essence of the impulse-response frequency-domain analysis for the power-stage linearization. Details of mathematical manipulations and matrix formulations for both continuous and discontinuous conduction operations will be presented later.

The power-stage frequency-domain transfer function G(s) is then complemented by the linear transfer function of the analog signal processor and the describing function of the digital-signal processor. The entire regulator is represented in block-diagram form, from which the regulator's control-dependent performances can be analyzed.

4.3.4 Average Time Domain Analysis Description

The objective of averaging is to make a continuous system model out of the piecewise-linear discrete system. There exists various averaging techniques combining the piece-wise linear switching intervals. One is the "circuit-averaging approach [7, 17], in which equivalent circuits of switched power stages operating in the continuous conduction mode are derived based on the effect of the duty cycle d(t) and [1-d(t)] on the power stage parameters. Other methods consist in generating the perturbation of the average current injected into the output circuit. In conjunction with the output-circuit transfer function, the disturbance in the output voltage caused by a corresponding disturbance in the average current is then obtained [18,19].

While the circuit-averaging method relies more on equivalence of circuit topology rather than analysis, it nevertheless provides not only the duty-cycle-to-output-voltage transfer function as does the current averaging method, but it also provides the converter input-to-output-voltage transfer function, which is essential in evaluating the behavior of disturbance propagation involving the regulator input. Such important behaviors include the audiosusceptibility and the effect of input filter on the stability and other control-dependent performances.

To retain this advantage of enabling these dual transfer functions and to provide a unified analytical basis for both continuous and discontinuous-conduction operations, the "state-space averaging" method was advanced by Caltech investigators, sponsored by a subcontract from TRW [8,9,20]. Details of this method are published in a companion report volume, NASA CR-135172.

Similar to the previous approach described in Section 4.3.3, the method treats the power stage as an entity by iteself, in addition to the analog and digital-equal processors. The analysis starts with the formulation of basic equations (31), (32), (33) and (35), which contains only power-stage parameters.

The objective of state-space averaging is to replace the state-space description of the piece-wise linear switched intervals of the switching cycle T_p by a single state-space description which represents approximately the behavior of the regulator across the entire period T_p. Using the continuous conduction case for example, equations (31) and (33) are averaged by summing the equation for intervals T_{on} and T_{F1} multiplied by d_1 and d_2 respectively, when the d's are identified in Figure 2 (A). The basic averaged state-space model over a single period T_p becomes:

$$\underline{\dot{X}} = (d_1F_1 + d_2F_2)\ \underline{X} + (d_1G_1 + d_2G_2)\ \underline{U} \qquad (39)$$

$$\underline{\Psi} = (d_1C_1 + d_2C_2)\ \underline{X} \qquad (40)$$

Justification of this approximation is provided in Referene [8], i.e., it corresponds to that of approximation of the fundamental matrix $e^{At}=1+At+\ldots$ by its first-order linear term. It also coincides with the fact that the output-filter resonant frequency is much lower than the switching frequency.

Once equations (39) and (40) are obtained, either analytical or circuit averaging can be carried out to realize the averaged model. The analytical realization starts by assuming d_1 and d_2 to be constant such that $d_1 = D$ and $d_2 = D' = 1-D$, then the following linear system holds:

$$\underline{X} = F\underline{X} + G\,\underline{U} \tag{41}$$

$$\underline{\Psi} = C\,\underline{X} \tag{42}$$

where

$$\left.\begin{aligned} F &= d_1F_1 + d_2F_2 \\ G &= d_1G_1 + d_2G_2 \\ C &= d_1C_1 + d_2C_2 \end{aligned}\right\} \tag{43}$$

Perturbations $u = U + \hat{u}$ is then introduced to the linear system represented by equations (41) and (42) to cause $x = X + \hat{x}$ and $Y = \Psi + \hat{y}$. Separation of the ac transfer function from the steady-state dc component gives:

$$\hat{x} = F\,\hat{x} + G\,\hat{u} \tag{44}$$

$$\hat{y} = C\,\hat{x} \tag{45}$$

The line voltage transfer function thus becomes:

$$\frac{\hat{y}\,(s)}{\hat{u}\,(s)} = C\,(sI - F)^{-1}\,G \tag{46}$$

The time-varying duty-cycle is then expressed as $d = D + \hat{d}$, with the corresponding perturbation $x = X + \hat{x}$, $y = Y + \hat{y}$, and $u = U + \hat{u}$. Substituting these variations into equations (39) and (40), and making the approximations that $\hat{u}/U \ll 1$, $\hat{d}/D \ll 1$, $\hat{x}/X \ll 1$, one has the following models:

dc model:
$$\underline{X} = -F^{-1}G\,\underline{U}\ , \quad \underline{\Psi} = -cA^{-1}G\,\underline{U} \tag{47}$$

ac model:
$$\begin{aligned} \hat{x} &= F\,\hat{x} + G\,\hat{U} + [(F_1 - F_2)\,\underline{X} + (G_1 - G_2)\,\underline{U}]\,\hat{d} \\ \hat{y} &= C\,\hat{x} + (C_1 - C_2)\,\underline{X}\,\hat{d} \end{aligned} \tag{48}$$

It is demonstrated [8,9] that through Laplace transform, these equations can be used to arrive at a common Canonical Model for all switching regulators.

The model offers a powerful design tool, as the input filters or other linear circuits are easily incorporated with the model and various control-dependent performances of different converters are readily compared. Expressed slightly different than the original form [8,9], the canonical dual-input (line and control) transfer function model for the buck, boost, and the two-winding buck-boost power stages are given in Figure 7. With the dual input from line and control disturbance properly defined, it is rather straight forward to incorporate the source variation as well as the control signal perturbation from the output of the digital signal processor to conduct the control-dependent performance analysis.

With the power stage modelled and with the linear analog signal processor routinely analyzed, the digital signal processor remains as the only non-linear block. Consistent with the low-pass nature of the output filter in relation to the switching frequency, the digital-signal processor is linearized through the describing-function technique. The technique is briefly discussed next.

Assuming the input to the digital signal processor is:

$$V_A\,(t) = A\,\mathrm{Sin}\,\omega t \tag{49}$$

and then output of the digital signal processor, d(t), can be expressed by its Fourier series:

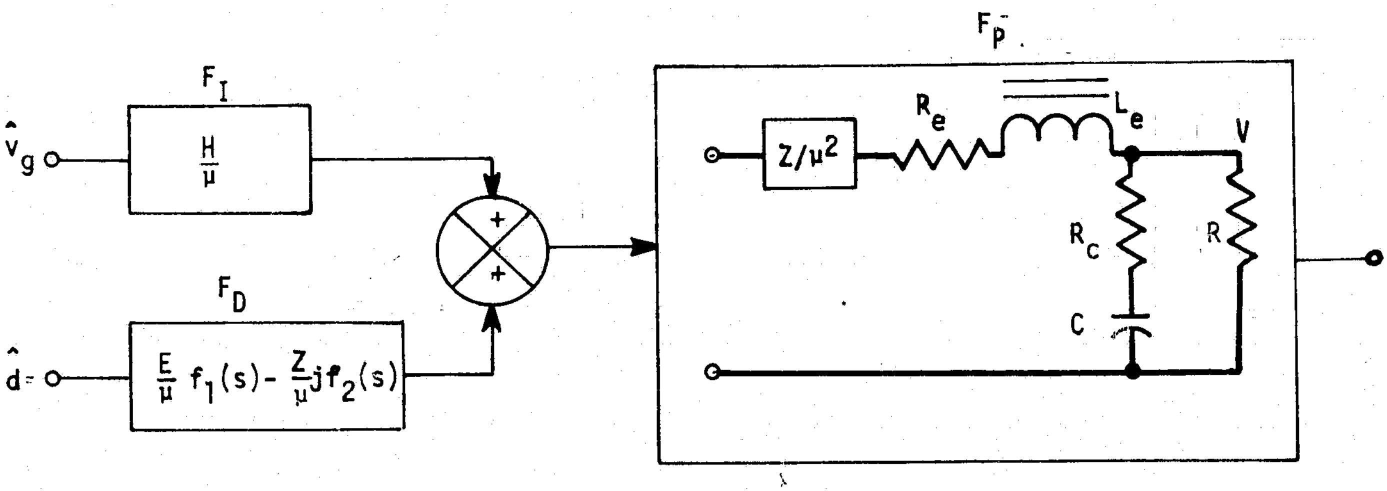
$$d(t) = D + a_1 \mathrm{Sin}\,\omega t + b_1 \mathrm{Cos}\,\omega t + \ldots \tag{50}$$

By definition, the describing function of the digital signal processor is:

$$F_M = \frac{\sqrt{a_1^{\,2}+b_1^{\,2}}}{A}\; e^{-j\tan^{-1}(b_1/a_1)} \tag{51}$$

Thus, by neglecting the higher harmonics of d(t) and seeking only its fundamental component, the non-linear digital signal processor is represented by a linear describing function, with gain $(a_1^{\,2}+b_1^{\,2})^{0.5}$ and phase $\tan^{-1}(b_1/a_1)$.

The representation can be combined with the canonical power-stage model and the linear analog signal processor to characterize the behavior of a complete switching regulator.



TYPE	M(D)	E	$f_1(S)$	J	$f_2(S)$	L_e	R_e	Z	H
BUCK	$\frac{1}{D}$	$\frac{V}{D^2}$	1	$\frac{V}{R}$	1	L	R_s	Z_F	H_F
BOOST	1-D	V	$1-S\frac{L_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$	$\frac{R_s}{(1-D)^2}$	Z_F	H_F
TWO WINDING BUCK BOOST	$\frac{1-D}{D}$	$\frac{V}{D^2}$	$1-D\frac{R_e+SL_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$	$\frac{R_s}{(1-D)^2}$	$\left(\frac{N_s}{N_p}\right)^2 Z_F$	$\frac{N_s}{N_p} H_F$

D = Duty Cycle
V = Output Voltage
L = Output Inductor
N_p = Primary Turns
N_s = Secondary Turns

R = Output Load Resistance
R_s = Inductor Winding Resistance
Z_F = Output Impedance of Input Filter
H_F = Input Filter Forward Transfer Function

Figure 7 Dual input transfer function for three basic power stages.

4.3.5 Discrete Time Domain Simulation Description

Switching regulator linear models derived from the afore-described techniqeus are applicable to small-signal analysis only. The reason for such a restriction stems from the fact that both the power stage and the digital signal processor are linearized about the system equilibrium state for a given fixed duty cycle $d(t) = D$. When a large-signal disturbance is introduced, either through a large step change in line or in load, the duty cycle varies during the entire transient until the new equilibrium state is reached. The time-variant duty cycle renders the small-signal models powerless.

Another restriction on the previously described techniques is that they cannot handle the transition between the continuous and discontinuous conduction in a given analytical effort. However, a large signal transient (e.g. a step load change) often can cause the pre-and post-transient states to be in different conduction modes. Such a transition again renders the small-signal model powerless.

In addition, other control input signals such as those provided by the peak current sensor, the saturation effect of the power stage inductors as well as the analog-signal-processor operational amplifier, may play important roles in large signal transients. Such non-linearifies, in a higher-order time-varying practical regulator system, can only be effectively taken into account through computer simulation.

There are many established simulation programs based on either topology input (ECAP, SCETPRE, SPICE) or block input (CSMP). Although it may not be necessarily evident from the user's viewpoint, these programs are based directly on the time-domain equations that are generated either from the input topology by the computer, or by the user. Consequently, the exact discrete time-domain system equations, presented previously in equations (1) to (18) prior to any linearization effort, serve conveniently as the natural basis for conducting the discrete time-domain simulation. An advantage of employing these formulated equations for simulation is its cost-effectiveness due to the following reasons:

1) The state transition is already formulated in matrices form thus saving computer compilation time.

2) For each switched interval within one operating cycle, the system is linear. Thus, a large fraction of the time period (including unity) can be specified as the step interval of calculation during steady-state or transient operations. Otherwise, because of the low system damping and the switching discontinuity, very small integration steps may be needed.

3) In certain simple cases, the constant state transition matrices Φ and D can be evaluated in closed form, thus, allowing the steady-state to be converged to much more rapidly.

Consequently, based on equations (4), (5) and (6), the system state can be propagated by the state transition matrix $\Phi 1(T)$ and the input matrix D1(T) until the time period $T_{ON}{}^{k}$ has elapsed due to the threshold condition (14), where $T < T_{ON}{}^{k}$ is the time period used in each computation. Subsequently, a new state transition matrix $\Phi 2(T)$ and input matrix D2(T) are employed to propagate the system state. If the system operation dictates a zero-conduction interval, matrices $\Phi 3(T)$ and D3(T) are invoked until the $T_{on}{}^{k}$ of the next cycle starts. If discontinuous conduction is not encountered, $\Phi 3$ and D3 are by-passed, and from $\Phi 2$ and D2 the system propagates back to $\Phi 1$ and D1. It is through this propagation that long-duration transient and steady-state operations are simulated.

4.3.6 Methodology Comparisons

Having presented the major analysis/simulation methodologies, a summary comparison is in order. These methods all start with the piecewise linear state-space system formulation and their closed-form solution in terms of state transition and input matrices. They differ only by the means through which the linearization of the nonlinear system is achieved.

In the discrete time domain analysis, the system equilibrium state is numerically evaluated and linearization about the equilibrium is achieved by performing the partial differentiation $\partial f/\partial \underline{X}$ numerically (or analytically for simple problems), where the function "f" relates $\underline{X}(t_{k+1})$ to $\underline{X}(t_k)$ in the equilibrium state. The linearization treats the complete switching regulator as a single entity. For most practical applications, a digital computer is used to carry out the detailed numerical analysis.

In the impulse-response analysis, the nonlinear power stage is linearized about its equilibrium state by idealizing a perturbed duty-cycle signal Δt_k as an impulse train, and by calculating the corresponding output-voltage perturbation $\Delta V_o\ (t_{k+n})$. The linearized power stage model, $g(nt_o)$ characterizes the small-signal behavior of the regulator exactly at the discrete sampling instant at a sampling rate $1/T_p$. Assuming the system response is much slower than the sampling rate, the continuous time-domain is achieved simply by letting $nT_p = t$, from which the frequency domain transfer function $G(s)$ follows through $s = j\omega t$. A closed-form $d(t)$- to-ΔV_o power-stage transfer function is thus obtained by invoking a simplifying assumption at the end of a complicated derivation. Additional frequency-domain transfer functions are needed for the analog and digital signal processors to facilitate the complete regulator control-loop analysis.

In the average time-domain analysis, the simplifying assumption for the power stage is made at the outset of the derivation. An averaged state-space representation for a complete switching period T_p is formulated by simply summing the state-space representation of the individual switched interval T_i properly weighed by the corresponding time ratio T_i/T_p. Linearization is accomplished through simple perturbation of the averaged representation. Small-signal power-stage models can be obtained either in analytical form or in circuit form. Again, transfer functions for analog and digital-signal processors are needed to complete the control-loop modeling and analysis.

No linearization is needed in the discrete time-domain simulation, as the disturbance in the nonlinear system is allowed to simply propagate through the state-transition matrices corresponding to one switched interval until a specific threshold condition for that interval is reached, upon which the disturbance propagates to the next switched interval of different state-transition matrices.

A concise comparison of the merits and limitations for each of these analytical approaches is given in Table 1. These approaches, along with analysis examples, will be presented next.

Table 1: Merits and Limitations of Analytical Approaches

ANALYTICAL APPROACH	MERITS	LIMITATIONS
DISCRETE TIME DOMAIN ANALYSIS	• Most accurate small-signal stability analysis • Can treat both conductions in a single computer subprogram • No need to separate a regulator into functional blocks. • Leads directly to discrete time domain simulation.	• Basically a numerical approach. No closed-form insight can be gained. • A circuit topology change would require new equation formulation. • No convenient test verification (e.g., Bode Plot) for stability analysis.
IMPULSE RESPONSE ANALYSIS	• Seem to provide a more accurate power-stage transfer function at high frequencies (>10% of switching frequency) than the average time-domain analysis.	• Need to separate regulator into functional blocks. • Closed-form power-stage representation does not incorporate input filter easily. • No input line disturbance transfer function is available.
AVERAGE TIME DOMAIN ANALYSIS	• Gain insight readily to enhance control loop design. • Performance analysis skill resides in most designers. • More cost-effective for complex system with multiple outputs. • Provide both line and control transfer functions thus allowing the power stage model to be incorporated in a larger system.	• Analytical results lose accuracy beyond 15-20% of switching frequency. May not be entirely satisfactory for multiple-loop regulators with high bandwidth. • Need to separate a regulator into functional blocks, thus necessitating the derivation of describing function for digital-signal processors.
DISCRETE TIME DOMAIN SIMULATION	• The only approach that can handle large-signal disturbance such as regulator start-up and sudden line/load changes	• Simulation effort gains no insight when not supported by analysis.

4.4 DISCRETE TIME DOMAIN ANALYSIS AND EXAMPLES

In this section, a step-by-step analytical procedure for performing the discrete time domain analysis is first outlined. Several examples are given as applications of this procedure. The examples are designed to demonstrate the merits and limitations of this particular analytical approach.

4.4.1 Step-by-Step Analytical Procedure

The following five basic steps are involved with the discrete-time domain stability analysis:

Step 1: State space system representation
Step 2: Nonlinear discrete state transition representation
Step 3: Solution of equilibrium state
Step 4: Linearization about equilibrium
Step 5: Eigenvalue stability analysis.

Additionally, audiosusceptibility analysis can be performed by Z-transform, of the linearized time-varying system and by replacing Z with jwT_p where T_p is the time interval of one switching period.

4.4.2 Example 1 Stability Analysis of a Multiple-Loop Controlled Buck Regulator Operating in Continuous Conduction Mode with a Constant T_{ON} Duty Cycle Control

A buck regulator with input E_i and output E_o is shown in Figure 8. The power circuit of the regulator consists of power transistor Q, power diode D, inductor L and its winding resistance R_L, Capacitor C and its ESR R_5, and load resistance R. The control circuit employs three feedback control loops. Loop I senses the converter output voltage and compares it with reference E_R to generate a dc error. Loop II sensing the ac voltage across the inductor [10,11] serves two functions. In addition to generating an ac error signal which combines with the dc error to serve as the composite small-signal amplifier input, it also produces a large-signal triangular ramp by integrating the steady state rectangular inductor voltage. This ramp, upon intersecting the threshold level E_T, actuates the Digital Signal Processor (DSP), which in turn controls the on-off of power switch Q. In this example, the control is such that the on time T_{ON} is fixed. Loop III containing capacitor C2 is needed to improve the dynamic response of the regulator.

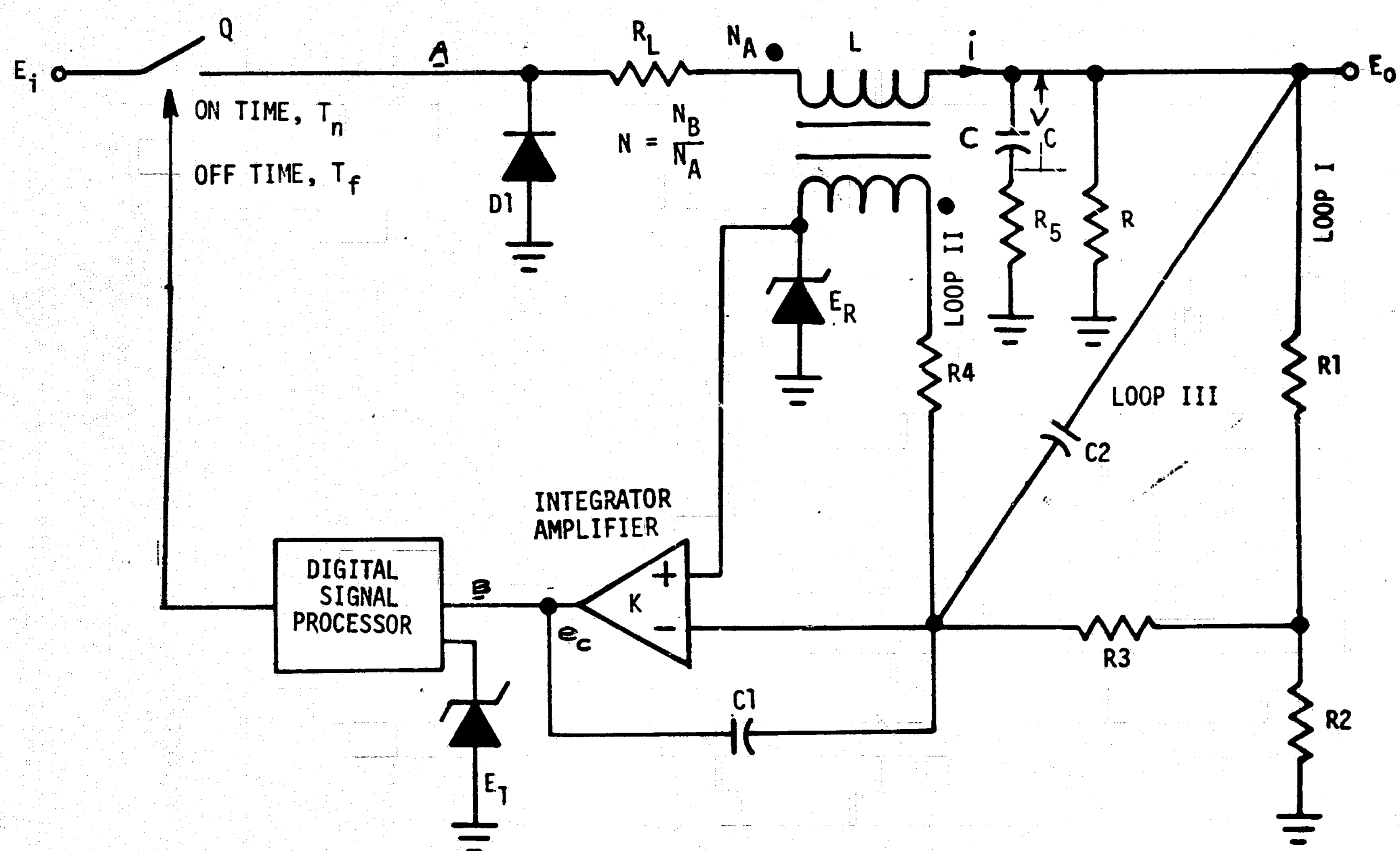


Figure 8 A Multiple-Loop Buck Regulator

4.4.2.1 State Space System Representation

It is apparent from Figure 8 that the system has three states: the output voltage e_o, the inductor current i, and the output voltage e_c of the integrator amplifier.

$$\frac{di}{dt} = \frac{1}{L_o} (e_i - e_o - R_o i) \tag{52}$$

$$e_o = R_5 \left(i - \frac{e_o}{R_L}\right) + v_c \tag{53}$$

$$\frac{dV_c}{dt} = \frac{i}{C_o} - \frac{e_o}{R_L C_o} \tag{54}$$

Differentiating e_o in equation (53) and substituting (52) and (54) into (53) yields

$$\frac{de_o}{dt} = e_o \left[- \frac{1}{C_o(R_5+R_L)} - \frac{R_5 R_L}{L_o(R_5+R_L)}\right] + i \left[\frac{R_L}{C_o(R_5+R_L)} - \frac{R_o R_5 R_L}{L_o(R_5+R_L)}\right] + e_i \left[\frac{R_5 R_L}{L_o(R_5+R_L)}\right] \tag{55}$$

The input voltage e_i is defined as

$$e_i = \begin{cases} E_i \text{ during } T_{on} \\ E_o \text{ during } T_{off} \end{cases} \tag{56}$$

The integrator amplifier output voltage e_c is:

$$e_c = K_d E_R + \int_{t_o}^{t} \left[\frac{K_d}{R_3 C_1} (E_R - e_o) - \frac{n}{R_4 C_1} (e_i - e_o) - \frac{C_2}{C_1} \dot{e}_o\right] dt \tag{57}$$

Thus,

$$\dot{e}_c = \left(\frac{n}{R_4 C_1} - \frac{K_d}{R_3 C_1}\right) e_o - \frac{C_2}{C_1} \dot{e}_o + \frac{K_d}{R_3 C_1} E_R - \frac{n}{R_4 C_1} e_i \tag{58}$$

Substituting (55) into (58), and defining

$$x_1 = e_o, \qquad x_2 = i, \qquad x_3 = e_c \tag{59}$$

One has

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \end{bmatrix} = \begin{bmatrix} f_{11} & f_{12} & 0 \\ f_{21} & f_{22} & 0 \\ f_{31} & f_{32} & 0 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} + \begin{bmatrix} g_{11} & 0 \\ g_{21} & 0 \\ g_{31} & g_{32} \end{bmatrix} \begin{bmatrix} e_i \\ E_R \end{bmatrix} \tag{60}$$

$$f_{11} = \frac{1}{C_o(R_5+R_L)} = \frac{R_5R_L}{L_o(R_5+R_L)}$$

$$f_{12} = \frac{R_L}{C_o(R_5+R_L)} = \frac{R_oR_5R_L}{L_o(R_5+R_L)}$$

$$f_{21} = -\frac{1}{L_o}, \quad f_{22} = \frac{R_o}{L_o} \tag{61}$$

$$f_{31} = \frac{n}{R_4C_1} - \frac{K_d}{R_3C_1} + \frac{C_2}{C_1C_o(R_5+R_L)} + \frac{C_2R_5R_L}{C_1L_o(R_5+R_L)}$$

$$f_{32} = \frac{C_2R_oR_5R_L}{C_1L_o(R_5+R_L)} - \frac{R_LC_2}{C_1C_o(R_5+R_L)}$$

$$g_{11} = \frac{R_5R_L}{L_o(R_5+R_L)}, \quad g_{21} = \frac{1}{L_o}$$

$$g_{31} = -\frac{n}{R_4C_1} - \frac{C_2R_5R_L}{C_1L_o(R_5+R_L)} \tag{62}$$

$$g_{32} = \frac{K_d}{R_3C_1}$$

Let

$$\underline{u} = \begin{bmatrix} e_i \\ E_R \end{bmatrix} \tag{63}$$

Equation (60) can now be written in compact form as:

$$\dot{X} = F\,\underline{X} + G\,\underline{u} \tag{64}$$

where F and G are the respective matrices in (60). This equation is the state-space system representation of the regulator shown in Figure 8.

4.4.2.2 Nonlinear Discrete State Transition Representation

The solution to (64) is given by:

$$\underline{x}(t) = e^{(t-t_o)F}\ \underline{x}(t_o) + \int_{t_o}^{t} e^{(t-\tau)F}\ G\ \underline{u}\ (\tau)d\tau \tag{65}$$

Or, since $\underline{u}$ is piecewise constant,

$$\underline{x}(t_k+T) = e^{FT}\ \underline{x}(t_k) + e^{FT}\ [\int_{o}^{T} e^{-FS}dS]\ G\ \underline{u}\ (t_k) \tag{66}$$

where $\qquad o \leq T < t_{k+1} - t_k$

$$\underline{u}(t) = \underline{u}(t_k) = \text{constant},\ t_k \leq t < t_{k+1}$$

Define the following matrices:

$$\left.\begin{aligned} \Phi(T) &= e^{FT} \\ D(T) &= e^{FT}\int_{o}^{T} e^{-FS}dS\ \ G \end{aligned}\right\} \tag{67}$$

Equation (66) becomes

$$\underline{x}(t_k+T) = \Phi(T)\ \underline{x}(t_k) + D(T)\ \underline{u}(t_k) \tag{68}$$

The value of $\underline{u}(t_k)$ depends on the state of the switch Q at time t_k^+. Note that matrices Φ and D are only functions of the time step T whose maximum permissible value is either T_{on} or T_{off}, depending on the state of the switch at t_k^+.

Defining

$$\underline{u}_o = \begin{bmatrix} o \\ E_R \end{bmatrix} \quad \text{and} \quad \underline{u}_1 = \begin{bmatrix} E_i \\ E_R \end{bmatrix} \tag{69}$$

It follows from (68) that

$$x(t_{k+1}) = \Phi(T_{on})\ \Phi(T^k_{off})\ \underline{x}(t_k) + \Phi(T_{on})\ D(T^k_{off})\ \underline{u}_o + D(T_{on})\ \underline{u}_1 \tag{70}$$

where T^k_{off} is a function of $\underline{x}(t_k)$ described implicitly by the threshold condition:

$$E_T = \phi_{31}(T^k_{off})\ x_1(t_k) + \phi_{32}(T^k_{off})\ x_2(t_k) + x_3(t_k) + d_{32}(T^k_{off})E_R \tag{71}$$

Note that given any initial state $\underline{x}(t_o)$, equations (70) and (71) can be used to compute recursively the state vector $\underline{x}(t_k)$ for all future time instances t_k. Note that this discrete state transition representation is nonlinear, due to the dependence of T^k_{off} on the state $\underline{x}(t_k)$ via (71).

4.4.2.3 Solution of Equilibrium State

The approximate solution is employed as an initial set toward solving for the exact state through Newton's iteration method. The approxmate time intervals, T_{on} and T_{off}, can be easily determined through regulator volt-second balance in the output inductor and the input/output energy equilibrium [21]. In the approximate steady state, equation (70) can be written as

$$\tilde{\underline{x}}^* = \Phi\ \tilde{\underline{x}}^* + D(\underline{u}) \tag{72}$$

where the Φ and D matrices can be computed for a given set of T_{on} and T_{off}. If the matrix $(I - \Phi)$ is non-singular, equation (72) alone is sufficient to solve for:

$$\tilde{\underline{x}}^* = (I - \Phi)^{-1} D\ \underline{u} \tag{73}$$

However, $(I - \Phi)$ is singular in many cases, and eqs. (71) and (72) are required to solve for $\underline{\tilde{x}}^*$. With this $\underline{\tilde{x}}^*$ as the initial setting, equations (71) and (72) are iterately computed until a certain specified matching condition is met. The condition can be defined as

$$\sqrt{\sum_{i=1}^{n} [\, x_i(t_{k+1}) - x_i(t_k) \,]^2} < \varepsilon \tag{74}$$

or

$$|\, x_i(t_{k+1}) = x_i(t_k) \,| < \varepsilon \tag{75}$$

where ε is an arbitrarily small positive number.

4.4.2.4 Linearization About Equilibrium

Regarding stability of the discrete time nonlinear system, one may consider two approaches: (1) Determine stability-in-the-large, and (2) Determine stability of the equilibrium solution. Attempts of relating stability-in-the -large to the contraction mapping/fixed point theorem [22] to solving eqs. (70) and (71) were unsuccessful, so had attempts of using the second method of Liapunov [23, 24]. Establishing the stability-in-the-large is therefore reserved as an effort for digital simulation. Of more importance at the moment is to establish stability of the equilibrium solution, which will be accomplished by linearization about the equilibrium state $\underline{x}^*$. Let

$$\delta\, \underline{x}(t_k) = \underline{x}(t_k) - \underline{x}^* \text{ and } E_i = E_i^* = \text{constant}, \tag{76}$$

then,

$$\delta\, \underline{x}(t_{k+1}) = \Psi\, \delta\, \underline{x}(t_k) \tag{77}$$

where

$$\Psi = \Phi(T_{on}) \frac{\delta}{\delta \underline{x}} [\, \Phi(T^k_{off})\, \underline{x}(t_k) + D(T^k_{off})\, \underline{u}_o \,] \Big|_{\underline{x}^*} \tag{78}$$

The above partial derivative is computed numerically by using different quotients. Let

$$\underline{f} = \Phi\ (T_{off}^{k})\ \underline{x}\ (t_k) + D(T_{off}^{k})\ \underline{u}_o \tag{79}$$

Then,

$$\left.\frac{\partial \underline{f}}{\partial \underline{x}}\right|_{\underline{x}^*} = \begin{bmatrix} \dfrac{f_1(x_1^* + \Delta x_1) - f_1(x_1^*)}{\Delta x_1} & \cdots & \dfrac{f_1(x_3^* + \Delta x_3) - f_1(x_3^*)}{\Delta x_3} \\ \vdots & & \vdots \\ \dfrac{f_3(x_1^* + \Delta x_1) - f_3(x_1^*)}{\Delta x_3} & \cdots & \dfrac{f_3(x_3^* + \Delta x_3) - f_3(x_3^*)}{\Delta x_3} \end{bmatrix} \tag{80}$$

The increments Δx_j were taken as 1% of the value of x_j, i.e.,

$$\Delta x_i = 0.01\ |\ x_j^*\ | \tag{81}$$

4.4.2.5 Eigenvalue Stability Analysis

The system is stable if all eigenvalues λ_i of Ψ in eq. (78) are absolutely less than unity. The eigenvalues are evaluated by a digital computer, and changes in the eigenvalues as a function of system parameters can be plotted in a complex plane. The eigenvalues correspond to the roots of the system. Existing relationships between root locations inside the unit circle and corresponding system response times and damping are well known from Z-transform analysis of linear discrete time system. [25,26]

For nominal regulator parameters as listed in Table 2, one expects to obtain three real and positive eigenvalues less than unity, since it is known from the actual regulator breadboard tests that the system was stable, and that the transient decay after a disturbance nonoscillatorily. Computer results ascertained the stability, where the three eigenvalues obtained are shown as follows:

Table 2 Nominal Regulator Parameters

Symbol	Parameter	Units	Value
E_i	Supply Voltage	volts	30
E_R	Reference (Desired Output) Voltage	volts	20
E_T	Integrator Threshold	volts	8
R_o	Inductor Series Resistance	ohms	0.015
R_1	Part of Output Voltage Divider	ohms	28.7K
R_2	Part of Output Voltage Divider	ohms	13.5K
R_3	Op-amp DC Input Resistor	ohms	10K
R_4	Op-amp AC Input Resistor	ohms	100K
R_5	Series-Equivalent Resistance of C_o	ohms	0.077
R_L	Load	ohms	10.
C_o	Output Filter Capacitor	μF	300
C_1	Op-amp Feedback Capacitor	pF	2200
C_2	Lead Compensation Capacitor	μF	0.022
L_o	Output Filter Inductor/Transformer	μH	250
n	Transformer Turns Rate n_2/n_1	--	0.65
T_{ON}	On Time	μs	30

$$\lambda_1 = 4.1176E-01 + j0$$

$$\lambda_2 = 9.5654E-01 + j0$$

$$\lambda_3 = 1.9027E-15 + j0$$

Note that λ_3 is for all practical purposes equal to zero. This is because the incremental voltage δe_c can be shown to be essentially a linear combination of δi and δe_o. The zero eigenvalue should, therefore, cause no concern, as it is clearly less than unity.

Since the objective of this example is to demonstrate the basic analytical steps from state-space system formulation to eigenvalue stability analysis, other related analytical topics developed in the MAPPS program for the regulator shown in Figure 8 are not presented here. These topics include the following:

- The analytical determination of Φ and D matrices in closed-form.
- The root loci of the linearized system as a function of key system parameters.
- The calculation of audio susceptibility analysis through Z-transform.
- The transient behavior caused by supply-voltage step changes.

Analytical presentation on these topics can be found in Appendix A [2], which becomes an integral part of this report.

4.4.3 Example 2 - Stability and Audiosusceptibility of a Boost Regulator Operating in Discontinuous Conduction Mode.

In this example, the same analytical procedure illustrated in Example 1 is applied to a different power circuit (boost regulator) operating in a different conduction mode (discontinuous), thus helping to demonstrate the unified nature of the discrete time-domain analysis. The analysis and the significant results are elaborated in Appendix B, which becomes an integral part of this report.

An interesting note concerning the stability result is that one eigenvalue is equal to zero for discontinuous-conduction operation. The zero eigenvalue indicates that the order of the system is reduced by one, which confirms findings elsewhere [5, 6]. The phenomenon can also be explained from a circuit viewpoint. The inductor current is always reduced to zero after a small perturbation; it therefore, can no longer constitute a state variable since its secondary condition is no longer free.

An audiosusceptibility analysis is also performed in this example. The performance is found to be a function of the regulator loading; it improves as the load becomes lighter. This phenomenon is quite different from the continuous-conduction operation, where the audio performance is essentially independent of the load.

4.4.4 Example 3 - A Buck Regulator Discrete Time-Domain Analysis Subprogram Containing Both Continuous and Discontinuous Conduction Modes.

Either through light-load operation or through design intent, the discontinuous-conduction is generally an inevitable mode of operation. It is thus desirable to have an analytical approach, through which a composite computer program can be developed to incorporate both continuous and discontinuous conductions. The objective can be achieved through the afore-described discrete time-domain analysis. The objective of this example is to demonstrate the practicality and the utility of such a program.

4.4.4.1 Continuous Conduction Mode Analysis

Using the analytical procedure outlined previously, analysis of a constant-frequency buck regulator operating in continuous conduction is given in Appendix C.

The regulator used for analysis is the sameone shown in Figure 8, except that for this example a constant-frequency instead of constant-T_{on} duty cycle control is used. The nominal circuit parameters are identical to those given in Table 2, with a constant period of 30 microseconds.

4.4.4.2 Discontinuous Conduction Mode Analysis

Analysis of discontinuous conduction mode is presented in Appendix D for the same circuit operating at lighter load condition.

4.4.4.3 A Composite Computer Program

A computer program, "MBUCK", combining the composite analysis presented in Appendices C and D is generated. The complete program listing is given in Appendix E.

For a given line and load condition, the main program first detects the inductor-current conduction mode. The appropriate subroutine for the operating mode is then entered for numerical computations. The following features of this program are noted:

- The program is able to handle automatically the transition between the two operating modes due to a large step load transients.
- The program numerically identifies the "jump" phenomenon frequently observed in regulator breadboard performance when an unstable constant-frequency continuous-conduction operation (when duty cycle is above 0.5) suddenly becomes stable when a line/load change results in a discontinuous conduction. Numerically, the phenomenon manifests itself by a sudden change of one eigenvalue from $|\lambda|>1$ to $\lambda=o$.
- The audio susceptibility and line transients can also be analyzed for both operating modes.

4.4.4.4 Define Users Interface Requirements

The philosophy here is to make the program "easy to use" by minimizing the necessary knowledge a user needs to know to run the program, and at the same time, maintaining the programming flexibility. The user interface is therefore the conversational type presented in "Question and "Answer" form. A sample of the conversation types is presented here:

```
          [ GET,MBUCK
          [ RUNX,I=MBUCK
          [ LGO
(1)        ENTER"STOP"TO DISCONTINUE PAS,OTHERWISE "NO"
          ? N
(2)        DO YOU WANT TO CHANGE "PARAM"? (Y OR N)
          ? N
(3)        DO YOU WANT TO CHANGE "COMP"? (Y OR N)
          ? N
(4)        DO YOU WANT NAMELIST? (Y OR N)
          ? N
(5)        DO YOU WANT STABILITY ANALYSIS? (Y OR N)
          ? N
(6)        DO YOU WANT ROOT LOCUS ANALYSIS? (Y OR N)
          ? N
(7)        DO YOU WANT AUDIO ANALYSIS? (Y,N)
          ? N
(8)        DO YOU WANT TRANSIENT ANALYSIS? (Y,N)
```

Statement (1) enables the user to continuously perform the analysis of the "MBUCK" program. Statement (2) allows a user to input various circuit parameter values or change certain values used in the previous run. The user also has the option to change computational parameters in Statement (3), such as certain convergence error or maximum number of iterations to achieve a convergent solution. In Statement (4), a user can ask a list of all the parameter values entered into or stored in the Statements (2) and (3). Statements (5) through (8) allow a user to access various performance analyses such as stability, root-locus, audiosusceptibility and transient response. The user can respond to these questions simply by typing Y for Yes and N for No.

4.4.5 Summary Remarks on Discrete Time-Domain Analysis

The foregoing examples have deomonstrated certain inherent merits and limitations concerning the discrete time-domain analysis:

- For a given design, it provides the most accurate small-signal stability analysis through eigenvalue calculations.

- The root loci of eignevalues as a function of a certain control parameter give a vivid account of the dependence

- Of stability on that parameter, although the numerical parametric display can seldom match the insight gained through analyticall-6 derived closed-form relationships.

- By treating the complete regulator as a single entity, it is particularly applicable for high-bandwidth multiple-loop controlled regulators in which the power stage, the analog signal processor, and the digital signal processor are intimately related without distinct functional divisions.

- It treats both inductor-current conduction modes readily in a single analysis program. However, a design change, particularly a change involving the addition or re-orientation of a state variable, would reqire the reform of the entire non-linear system formulation. Consequently, it is perhaps best suited for regulators where the design has been standardized.

- It leads directly into a cost-effective discrete-time domain simulation, which can handle the stability-in-the-large.

4.5 IMPULSE-FUNCTION ANALYSIS AND EXAMPLES

As described previously in Section 4.3.3, impulse-function techniques can be employed to derive accurate models for buck, boost, and buck-boost regulator power stages operating in continuous and discontinuous inductor-current conductions. In this section, a discontinuous-conduction buck regulator power stage is used to demonstrate the methodology of the impulse-function analysis, from which the analysis is generalized to include all three power stages in both modes of operation. A numerical example is then given for a complete regulator including analog- and digital-signal processors as separate entities. Summary remarks are made to conclude the section.

4.5.1 Example 1 - Discontinuous-Conduction Buck Regulator Power Stage Modeling Based on Impulse-Function Analysis

Three circuit topologies are presented in each operating cycle. Figure 9(A) to 9(C) correspond to the T_{ON}, T_{F1} and T_{F2} interval, respectively. A duty cycle control signal d(t) and the corresponding input voltage $V_{D(t)}$ to the output filter are shown in Figure 10(A) and 10(B). Each T_{ON} is initiated by a constant-frequency clock, and the signal d(t) only controls the time interval T_{ON}. Note that $V_D(t)$ during T_{F2} is the time-dependent output voltage v_o, which is not treated as a constant in the time-domain analysis.

The buck regulator power stage has two state variables, i_L and v_C. During T_{F1}^k,

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -\dfrac{R_5R_L}{L_o(R_5+R_L)} & -\dfrac{R_L}{L_o(R_5+R_L)} \\ -\dfrac{R_L}{C_o(R_5+R_L)} & -\dfrac{1}{C_o(R_5+R_L)} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

$$\triangleq \begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \qquad (82)$$

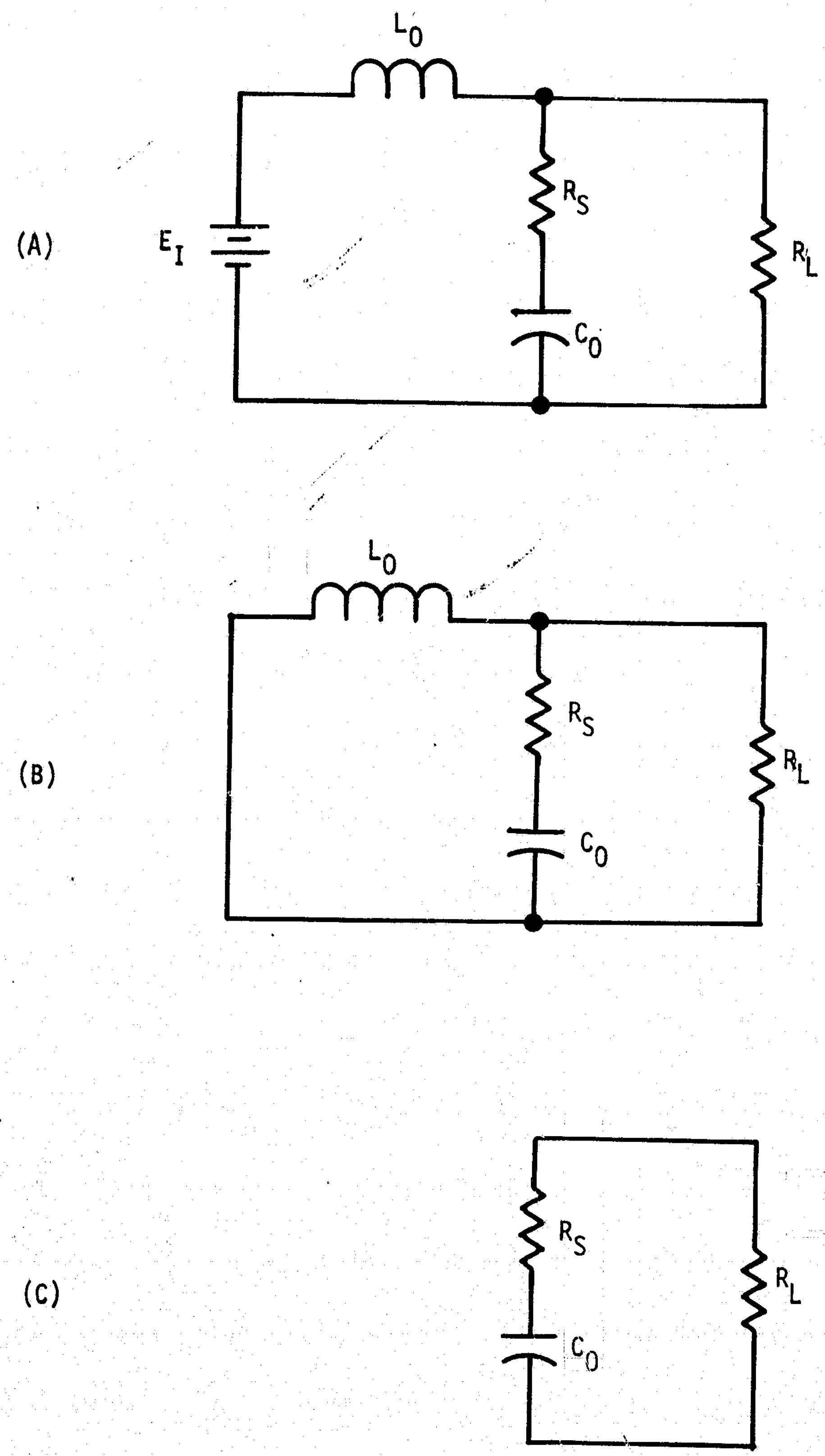


Figure 9   Power Stage Topology during (A) T_{ON}, (B) T_{F1}, and (C) T_{F2}.

During T_{F2}^{k}

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C_o(R_S+R_L)} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \tag{83}$$

During T_{ON}^{k}

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \end{bmatrix} = \begin{bmatrix} -\frac{R_S R_L}{L_o(R_S+R_L)} & -\frac{R_L}{L_o(R_S+R_L)} \\ \frac{R_L}{C_o(R_S+R_L)} & -\frac{1}{C_o(R_S+R_L)} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_o} \\ 0 \end{bmatrix} E_I \tag{84}$$

Equations (82) to (84) are represented by (85) to (87), respectively for matrix representation.

$$\underline{\dot{X}} = F1\ \underline{X} \tag{85}$$

$$\underline{\dot{X}} = F2\ \underline{X} \tag{86}$$

$$\underline{\dot{X}} = F3\ \underline{X} + G3\ E_I \tag{87}$$

where $F1 \equiv F3 \triangleq F$

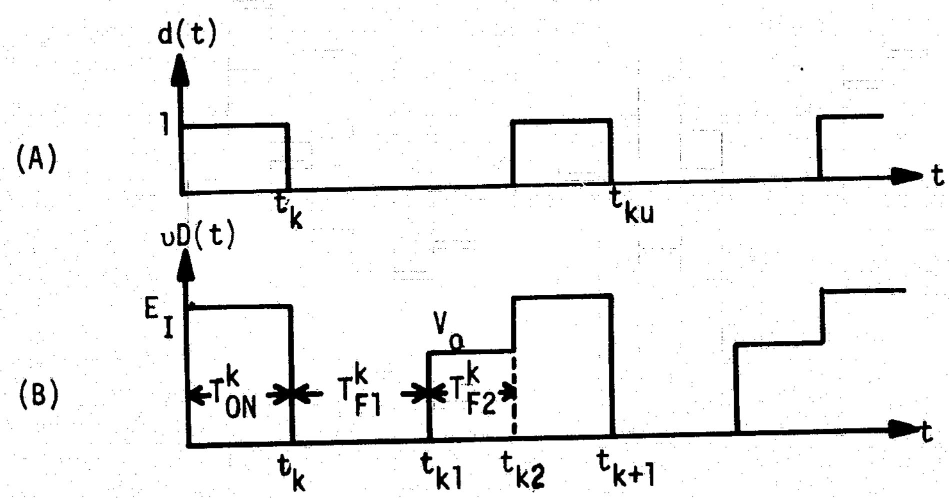


Figure 10 Duty Cycle Signal and Voltage Applied to Output Filter

Consider the small signal behavior of the converter about its equilibrium state is the same as a linear system. When the converter is subjected to a small disturbance, the duty cycle signal d(t) is modified as $d(t)+\Delta d(t)$ shown in Figure 5. Such a perturbed duty cycle signal can be idealized as a impulse train when the perturbation is sufficiently small. Since the small signal behavior of the converter is considered linear, the discrete impulse response of the linear system is equivalent to that of the continuous system. The discrete-time-domain model for the power stage can be derived if the state of the system subjected to a small perturbation at the end of T_{on}^{k} can be computed after n cycles of propagation. This concept can be elaborated by the state trajectories, shown in Figure 6. The superscripts "o" and "*" represent the steady state and the perturbed state, respectively. For a small disturbance at t_k^*, the perturbed state after one cycle of propagation is represented as $\underline{X}(t_{k+1}^{1})$.

The first step toward developing the discrete-time-domain model is to find:

$$\frac{d\underline{X}(t_{k+1}^{o})}{d\, t_k^*} \triangleq g(\cdot) \tag{88}$$

To do so, the solution of the piecewise-linear system equations (85) to (87) are given as the following:

$$\underline{X}^*(t_{k1}^{o}) = \Phi 1(t_{k1}^{o} - t_k^*)\, \underline{X}^*(t^*_k) \tag{89}$$

$$\underline{X}^*(t_{k2}^{o}) = \Phi 2(t_{k2}^{o} - t_{k1}^*)\, \underline{X}^*(t_{k1}^*) \tag{90}$$

$$\begin{aligned}\underline{X}^*(t_{k+1}^{o}) &= \Phi 3(t_{k+1}^{o}) - t_{k2}^*)\, \underline{X}^*(t_{k2}^*) \\ &+ \Phi 3(t_{k+1}^{o}) \int_{t_{k2}^*}^{t_{k+1}^{o}} \Phi 3(-S)dS\ G3\ E_i \end{aligned} \tag{91}$$

where Φi for i = 1, 2, 3 are the state transition matrices. Applying the chain rule, equation (88) can be written as:

$$\frac{dX^*(t^o_{k+1})}{dt^*_k} = \frac{d\underline{X}^*(t^o_{k+1})}{dX^*(t^o_{k2})} \quad \frac{d\underline{X}^*(t^o_{k2})}{d\underline{X}^*(t^o_{k1})} \quad \frac{d\underline{X}^*(t^o_{k1})}{dt^*_k} \tag{92}$$

Equation (92) can be computed by performing each individual differentiation. The result is presented here.

$$\frac{dX^*(t^o_{k+1})}{dt^*_k} = \Phi 3(T^o_{ON})\ \Phi 2(T^o_{F2})\ [1+(F1-F2)\underline{X}(t^o_{k1})\ \frac{-C1}{C1F1\underline{X}^*(t^o_{k1})}\ ]$$
$$\Phi 1(T^o_{F1})\ G_3E_I \tag{93}$$

The condition which determines the time instant t^*_{k1} is when the inductor current X_1 reduces to zero. i.e.,

$$C1\ \underline{X}(t^*_{k1}) = 0$$

where

$$C1 = [1 \quad 0]$$

The following expression can be simplified.

$$1+(F1-F2)\ \underline{X}\ (t^o_{k1})\ \frac{-C1}{C1F1\ \underline{X}^*(t_{k1})} = 1-(F1-F2)\begin{bmatrix} o \\ V_o \end{bmatrix} C1/C1\, F1\ \begin{bmatrix} o \\ V_o \end{bmatrix}$$

$$= \begin{bmatrix} o & o \\ o & 1 \end{bmatrix} \tag{94}$$

Equation (93) then becomes

$$\frac{dX^*(t^o_{k+1})}{d\,t^*_k} = \Phi 3(T^o_{ON})\ \Phi 2(T^o_{F2}) \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \Phi 1(T_{F1})\ G3E_I \tag{95}$$

The transition matrices $\Phi 3(T_{ON})$, $\Phi 2(T_{F2})$ and $\Phi 1(T_{F1})$ are computed.

Let

$$\Phi(T_p) \triangleq \Phi 3(T^o_{ON})\ \Phi 2(T^o_{F2}) \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \Phi 1(T^o_{F1})$$

$$= e^{f_{22}T^o_{F2} - \alpha(T^o_{ON}+T^o_{F1})} \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix}$$

$$\triangleq e^{-a\ T_p} \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \tag{96}$$

where

$$\phi_{11} = \frac{f_{12}\ f_{21}}{\omega^2}\ \sin \omega T_{ON} \sin \omega T_{F1}$$

$$\phi_{12} = \frac{f_{12}}{\omega} \sin \omega T^o_{ON}\ \left(\frac{\alpha+f_{22}}{\omega} \sin \omega T^o_{F1} + \cos \omega T^o_{F1}\right)$$

$$\phi_{21} = \left(\frac{\alpha+f_{22}}{\omega} \sin \omega T^o_{ON} + \cos \omega T^o_{ON}\right) \frac{f_{21}}{\omega} \sin \omega T^o_{F1}$$

$$\phi_{22} = \left(\frac{\alpha+f_{22}}{\omega} \sin \omega T^o_{ON} + \cos \omega T^o_{ON}\right)\left(\frac{\alpha+f_{22}}{\omega} \sin \omega T^o_{F1} + \cos \omega T^o_{F1}\right)$$

and

$$a = -f_{22} \frac{T^o_{F2}}{T_p} + \alpha(T^o_{ON}+T^o_{F1})/T_p$$

The eigenvalues of the matrix shown in (96) are computed

$$\lambda_{1,2} = -\frac{\phi_{11}+\phi_{22}}{2} \pm j\sqrt{\phi_{11}\phi_{22}-\phi_{12}\phi_{21}-(\phi_{11}+\phi_{22})^2/4}$$

However, due to the nature of the problem

$$\phi_{11}\phi_{22}-\phi_{12}\phi_{21} \equiv 0 \tag{97}$$

Therefore,

$$\lambda_{1,2} = 0, -(\phi_{11}+\phi_{22})$$

This is a very interesting finding...It says that the power stage in discontinuous operation behaves as a first order system even though there exists two energy storage elements.

The perturbed state after n cycles of propagation can be expressed as

$$\frac{d\underline{X}^*(t^o_{k+n})}{dt^*_k} = \frac{d\underline{X}^*(t^o_{k+n})}{dX^*(t^o_{k+n-1})} \cdot \cdot \cdot \frac{d\underline{X}^*(t^o_{k+2})}{d\underline{X}^*(t^o_{k+1})} \frac{dX^*(t^o_{k+1})}{dt^*_k} \tag{98}$$

Since:

$$\frac{dX^*(t^o_{k+n})}{dX^*(t^o_{k+n-1})} = \phi 3(T^o_{ON})\ \phi 2(T^o_{F2}) \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \phi 1(T^o_{F1}) \tag{99}$$

Employing (95) and (99), equation (98) can be reduced to:

$$\frac{d\underline{X}^*(t^o_{k+n})}{dt^*_k} = \phi(T_p)^n\ G_3\ E_I \tag{100}$$

It can be shown that:

$$\phi(T_p)^n = e^{-anT_p}\ (\phi_{11}+\phi_{22})^{n-1} \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \tag{101}$$

Since

$$v_o = C\,\underline{X}$$

where $$C \triangleq [C_{11}\ C_{12}] = \begin{bmatrix} \dfrac{R_S\,R_L}{R_S+R_L} & \dfrac{R_L}{R_S+R_L} \end{bmatrix} \tag{102}$$

The impulse response of the linearized discrete system can be represented by

$$g(nT_p) \triangleq \frac{\Delta v_o(t^o_{k+n})}{\Delta t^*_k} = C\,\Phi(T_p)^n\,G_3\,E_I$$

$$= \frac{C_{11}\Phi_{11}+C_{12}\Phi_{21}}{\Phi_{11}+\Phi_{22}}\,\frac{E_I}{L_o}\,e^{[-a+\frac{1}{T_p}\ln(\Phi_{11}+\Phi_{22})]nT_p} \tag{103}$$

In order to approximate the above discrete linear system by a continuous linear system one can substitute t = nT into (103).

$$g_p(t) = \frac{C_{11}\Phi_{11}+C_{12}\Phi_{21}}{\Phi_{11}+\Phi_{22}}\,\frac{E_I}{L_o}\,e^{-[a-\frac{1}{T_p}\ln(\Phi_{11}+\Phi_{22})]t}$$

$$\triangleq G\,e^{-a't} \tag{104}$$

where

$$G = \frac{R_L}{R_S+R_L}\,\frac{E_I}{L_o}\,\frac{-R_S\sin\omega T^o_{ON}\,\sin\omega T^o_{F1}+\sqrt{\frac{L_o}{C_o}}\cos(\omega T^o_{ON}-\theta)\sin\omega T^o_{F1}}{-\sin\omega T^o_{ON}\,\sin\omega T^o_{F1}+\cos(\omega T^o_{ON}-\theta)\cos(\omega T^o_{F1}-\theta)} \tag{105}$$

$$a' = \left[\frac{+1}{C_o} - \frac{1}{2}\left(\frac{1}{C_o} - \frac{R_S R_L}{L_o}\right)\frac{T^o_{ON}+T^o_{F1}}{T_p}\right]\frac{1}{R_S+R_L}$$

$$-\frac{1}{T_p}\ln\frac{1}{\omega^2}\left(\frac{R_L}{R_L+R_S}\right)^2\frac{1}{L_oC_o}\left[-\sin\omega T^o_{ON}\,\sin\omega T^o_{F1} + \cos(\omega T^o_{ON}-\Theta)\cos(\omega T^o_{F1}-\Theta)\right] \tag{106}$$

$$\Theta = \tan^{-1}\frac{1}{2\omega}\,\frac{1}{R_S+R_L}\left(-\frac{1}{C_o}+\frac{R_S\,R_L}{L_o}\right) \tag{107}$$

$$\omega = \frac{1}{R_S+R_L}\sqrt{\frac{R_L^2}{L_oC_o} - \frac{1}{4}\left(\frac{R_SR_L}{L_o} - \frac{1}{C_o}\right)^2} \tag{108}$$

Taking Laplace Transformation of the linear system (104), the frequency-domain transfer function becomes:

$$G_p(S) = \frac{(G/a')}{1+S(1/a')} \tag{109}$$

where G and a' functions of the switching frequency, the steady state T_{on}^{o} and T_{F1}^{o}, the input voltage, and practically all power-stage circuit parameters. Despite the physical presence of both L and C, the power stage behaves as a single-order system, with varying gain and phase.

4.5.2 Impulse-Function Analysis Extended to Other Power Stages With Continuous and Discontinuous Conduction Modes

The analysis outlined in the previous section is extended to include the three most-commonly used converter power stages: the buck, the boost, and the buck-boost, operating with either continuous or discontinuous conduction. The duty-cycle-to-output-voltage discrete time domain models are then transformed into frequency-domain transfer functions representing the small-signal low-frequency characteristics of the regulators. The analytical details of this effort is presented in Appendix F. Conclusions of the significant importance include the following:

- All three regulator power stages behave as first-order systems in discontinuous conduction, as contrary to second-order system in condinuous conduction. The transition between the two operating modes is abrupt.
- In discontinuous conduction, the gain and the corner frequency are both functions of the input voltage, the load, all power stage parameters, the switching frequency, and the on-off time intervals. In continuous conduction, however, the gain is only related to the input voltage and the duty cycle, and the corner frequency is dominated by the duty cycle and the output filter.

- The continuous-conduction boost and buck-boost regulators have only one conditional zero in the right half plane, which is a function of the switching period. This is different from results previously obtained through "circuit averaging" [7], where each of the two regulators has a positive zero that is independent of the switching period.
- The gain and phase of the power-stage transfer function differ significantly from those obtained through the "averaging" model. Experimental data are closer to the impulse-function analytical result than the "averaging" counterpart.

4.5.3 Example of a Complete Buck Regulator Analysis

A buck regulator, shown in Figure 11, is designed to operate in the continuous conduction under normal-to-heavy load and in the discontinuous conduction under light load. The regulator output is compared with a reference voltage E_R, the error signal is then sent through a lead-lag compensation network and an amplifier, both represented by G_c. The frequency domain model of the converter is shown in Figure 12.

The transfer function G_c thus represents that of the analog signal processor, its characteristic is:

$$G_c = 193.3 \frac{(1+jf/20)(1+jf/1225)}{(1+jf/0.3)(1+jf/3263)} \tag{110}$$

The digital signal processor, as illustrated in Figure 13, compares the error signal $v_e(t)$ with a fixed ramp A(t), where

$$A(t) = A_o(t-nT_s),\ nT_s \leq t \leq (n+1)T_s \tag{111}$$

where $A_o = 6.25 \times 10^4$ volts per second is the slope of the ramp. The output of the digital signal processor is a unity pulse train, with its pulse duration governed by

$$\begin{aligned} d(t) &= 1 \quad \text{if} \quad A(t) \leq V_e(t) \\ &= 0 \quad \text{if} \quad A(t) \geq V_e(t) \end{aligned}$$

The digital signal processor has been characterized by the describing

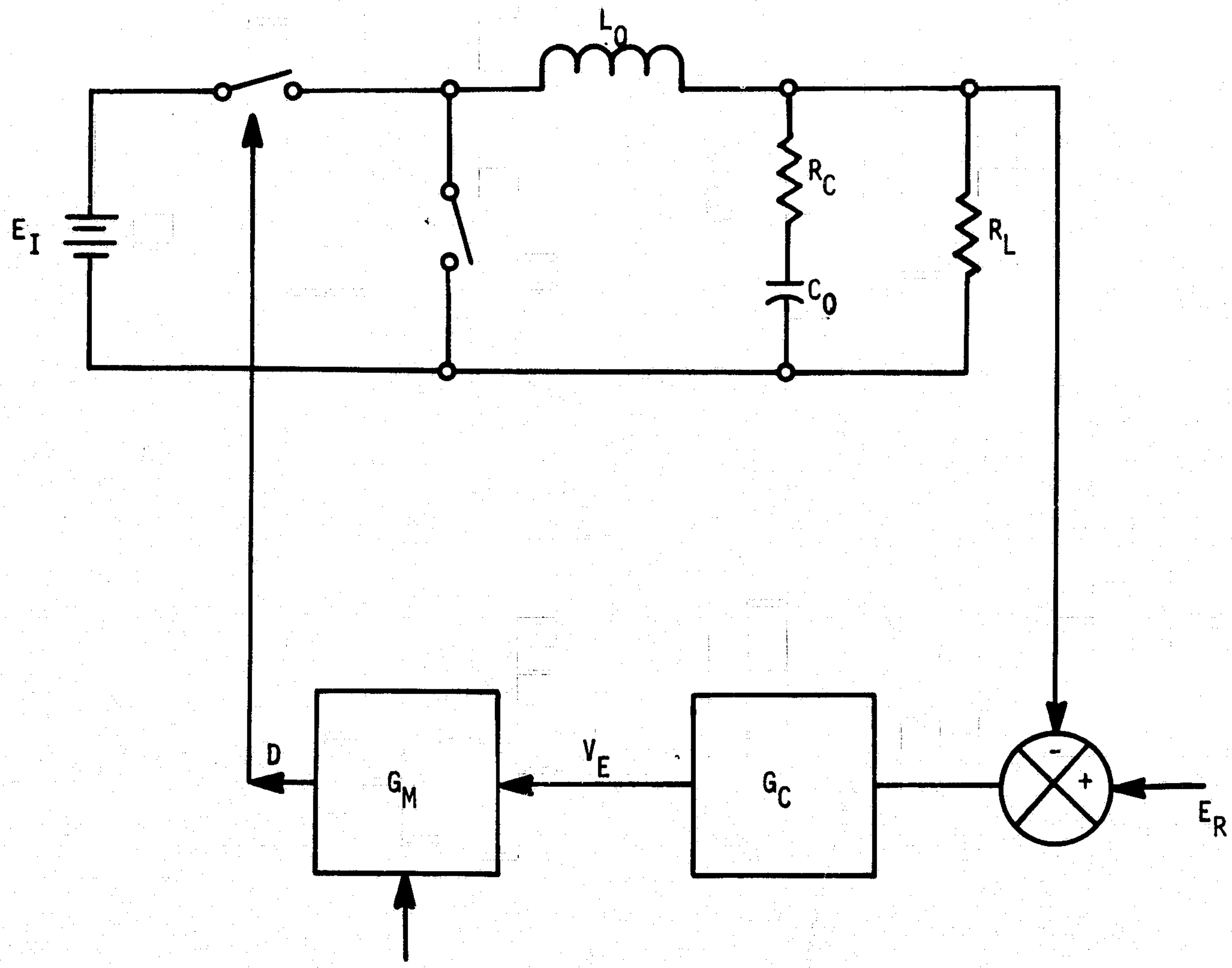


Figure 11 A Buck Regulator

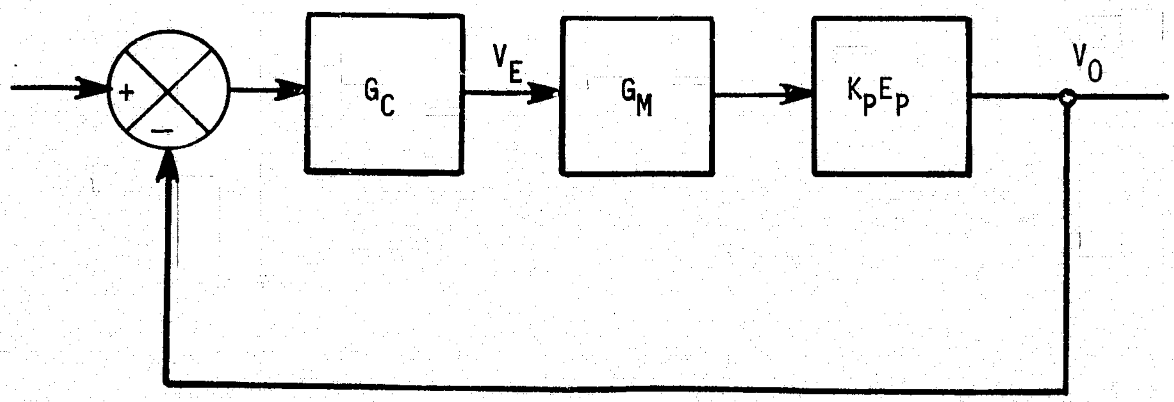


Figure 12 Simplified Control Block Diagram For Figure 11

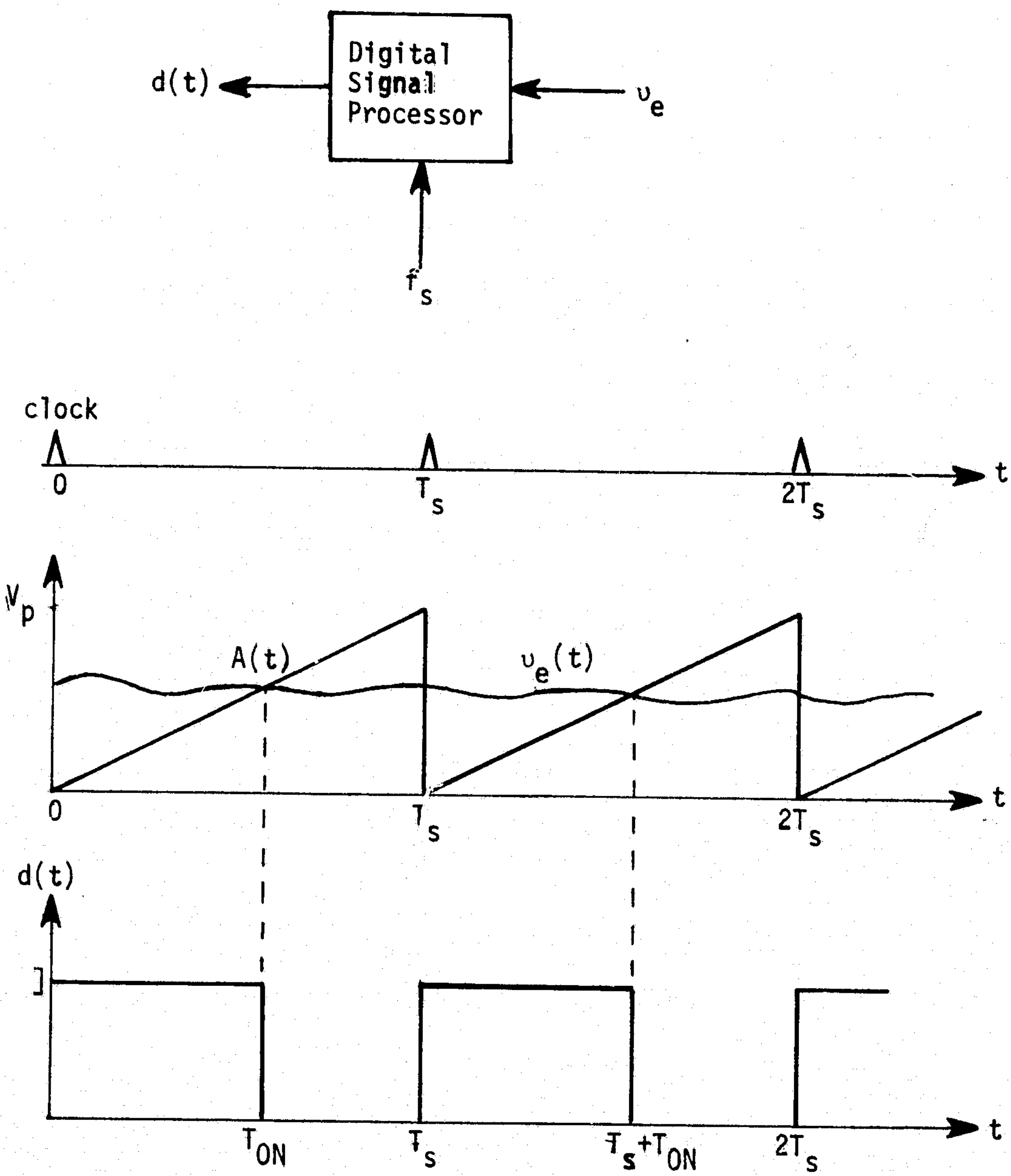


Figure 13 Implementation of the Digital Signal Processor

function in Reference [7], and is found to be:

$$K_M = \frac{1}{V_p} \tag{112}$$

Due to the circuit implementation, there is a delay τ_d from the signal d(t) to the power switch. For convenience, this delay is included as part of the digital-signal-processor characteristic. The transfer function of the entire digital signal processor is therefore represented as

$$G_M = \frac{1}{V_p} e^{jw\tau_d} \tag{113}$$

The power stage transfer function for a continuous-conduction buck regulator has been derived in Appendix E as:

$$G_p(s) = E_I \frac{1 + \tau_a S}{\frac{S^2}{\omega_N^2} + 2\,\xi \frac{S}{\omega_N} + 1} \tag{114}$$

where

$$\tau_a = R_S C_o$$

$$\omega_N = \sqrt{\frac{R_L}{R_L + R_S}}$$

$$\xi = \frac{1}{2} \left(1 + \frac{R_S R_L C_o}{C_o}\right) \sqrt{\frac{L_o}{C_o R_L (R_S R_L)}}$$

The power stage transfer function for a discontinuous-conduction buck regulator has been derived previously in equation (109).

The combination of equations (109), (110), and (113) thus protrays the entire regulator in discontinuous-conduction operation, while that of (114), (110), and (113) protrays the same regulator in continuous-conduction.

The circuit parameters for the power stage are: $L_o = 1mH$, $C_o = 455\mu F$, $R_C = 0.034$ ohms, $T_S = 50\mu s$, $E_I = 40V$. The time delay τ_d is $8\mu s$. The load resistance R_L is taken as 6.7 ohms and 150 ohms for the continuous- and discontinuous-conduction, respectively.

Figure 14 shows the Bode plot of the regulator in continuous-conduction. The second-order effect of the output filter is apparent. Excellent agreements exist between analytical and experimental results.

Figure 15 shows the Bode plot of the regulator in discontinuous-conduction, from which the first-order effect of the output filter is verified. The first-order corner frequency is a function of all power-stage parameters, the load, and the T_{on} and T_{F1} intervals. The ESR of capacitor C_o, is noted here for its significant effect on determining the low-frequency corner (< 10Hz) of the first-order system. This is in contrast to the second-order system in continuous-conduction operation, where the effect of ESR only becomes significant in high-frequency range (> 5kHz).

Also observed in Figure 15 is the fact that the phase lag is at most 90° and the corner frequency is usually low. Therefore, only a gain compensation of the error amplifier is needed to improve the transient response for the inherently-stable system.

Furthermore, the analysis has predicted an abrupt reduction of system order when the inductor-current conduction emerges from continuous to discontinuous. This prediction was verified by measuring the open-loop crossover frequency of the regulator with a gradually diminishing load. As shown in Table 3, the crossover frequency remains essentially unchanged as long as continuous conduction is maintained. When the load is reduced to about 90 to 100 ohms, the regulator begins to operate in between the two conduction modes affected by the disturbance of the small signals injected for measurement purpose. A very significant reduction of the crossover frequency can be seen when the load is between 90 and 100 ohms. Further decrease in load only results in a gradual reduction of the crossover frequency.

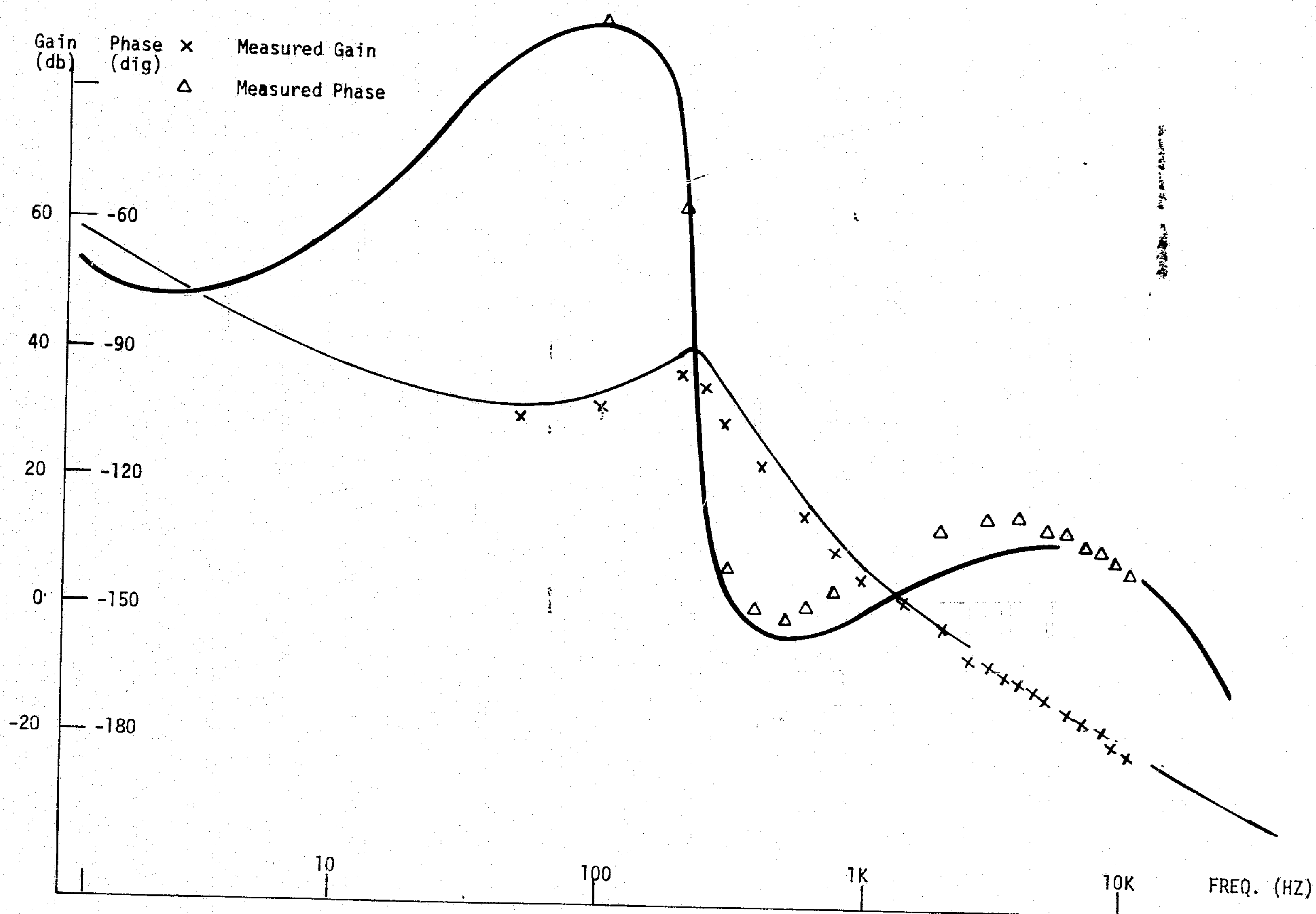


Figure 14 Continuous Conduction Bode Plot

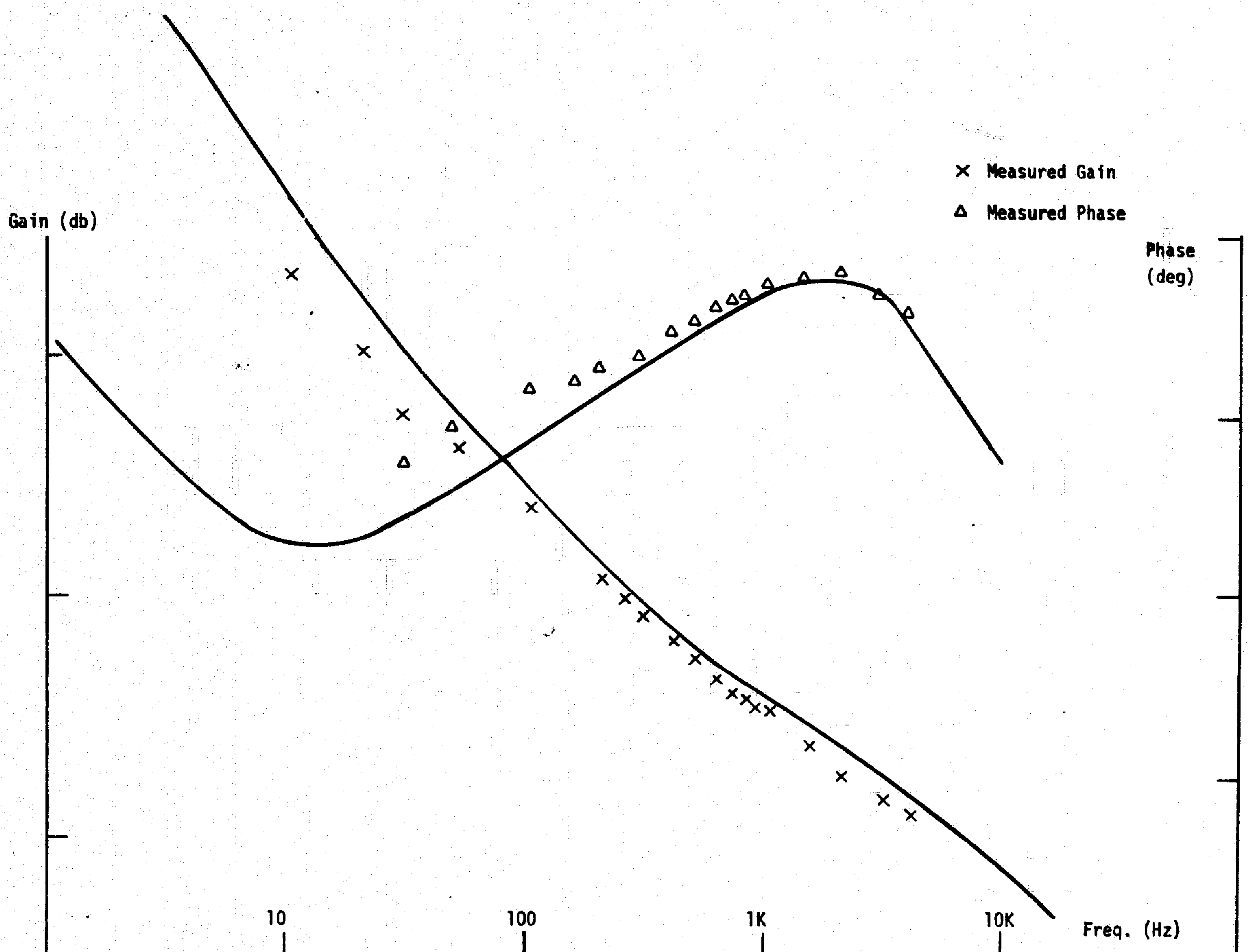


Figure 15 Discontinuous Conduction Bode Plot

Table 3

Open-Loop Crossover Frequency as a Function of Load Resistance

Load Resistance (Ohms)	10-70	80	90	100	110	120	130
Crossover Frequency (Hz)	1650	1600	1450	450	250	215	205

4.5.4 Summary Remarks on Impulse Function Analysis

The foregoing presentation and example have demonstrated the following points regarding the impulse-function analysis:

(1) The power-stage closed-form representations suitable for frequency-domain stability analysis are obtained from very complicated modeling; the simplifying assumption of a much slower system response in relation to the sampling rate is being applied only at the last step of derivation.

(2) Starting with a highly complex mathematical manipulation without approximation, the derivation does not include the input filter due to the formidable analytical task involved. Its utility to analyzing the stability of a practical regulator with input filter is therefore inhibited.

(3) The impulse-function formulation for duty-cycle perturbation cannot be followed for the small-signal perturbation in the input line. There is thus no input-to-output transfer function for the line disturbance.

4.6 AVERAGE TIME DOMAIN ANALYSIS AND EXAMPLES

As stated in Section 4.3.4, the objective of averaging is to make a continuous model out of the piecewise-linear discrete system. Through the approximation of the matrix $e^{At} = I + At + \cdots$ by its first-order linear term, linear system representation shown in equations (41) to (43) are obtained at the outset of the analysis. The basic feature of a switching regulator, that the output ripple is always negligibly small compared to the dc average output, is therefore properly utilized at the beginning for reducing the complexity in the power-stage analysis. Due to this simplification, the standard perturbation processes are applicable to both the duty-cycle control signal and the line input signal, thus enabling the derivation of the dual-input transfer function for the power stage. The culmination of this derivation is an equivalent linear circuit valid for small-signal line and control variations superimposed upon a dc operating point. The equivalent circuit is a canonical model containing the essential properties of any given switching regulator.

The average time-domain analysis is developed at CalTech, which represents the university part of the MAPPS joint industry-university team. Details of the analysis and the significant results are presented in NASA CR-135174, which is a separate but companion volume to this report, NASA CR-135173. No elaboration about the method itself is therefore needed here. Instead, certain application aspects of the average time domain analysis are addressed. Starting with the control-block formation of the dual-input transfer function, its application to a single-loop controlled buck regulator is given as an example.

4.6.1 Power Stage Dual-Input Transfer Function

The power stage transfer function, including an input filter, will be analyzed by using a dual-input describing function based on the averaging technique presented previously. The dual inputs presented to the power stage are two external forcing functions: the source voltage v_g and the duty-cycle control signal d(t) derived from the digital signal processors.

The canonical power-stage model for the buck, the boost, and the buck-boost regulators, as originally derived in Reference 8 for continuous conduction mode (See Appendix I), is reproduced in Figure 10 for convenience. Let

H_F = forward gain of the input filter from its input to output,
Z_F = output impedance of the input filter.

The canonical model including the input filter can be developed through the self-explanatory sequence depicted in Figure 17(A) to (C). Notice the duty-cycle perturbation $\hat{d}$ and the input-line perturbation $\hat{v}_g$ are properly separated in Figure 17 (C), in which:

$$\left.\begin{aligned} Z &= Z_F \\ H &= H_F \end{aligned}\right\} \text{ for buck and boost regulators}$$

and

$$\left.\begin{aligned} Z &= (N_s/N_p)^2 Z_F \\ H &= (N_s/N_p) H_V \end{aligned}\right\} \begin{array}{l}\text{For two-winding buck-boost regulator with primary} \\ \text{winding } N_P \text{ and secondary winding } N_S.\end{array}$$

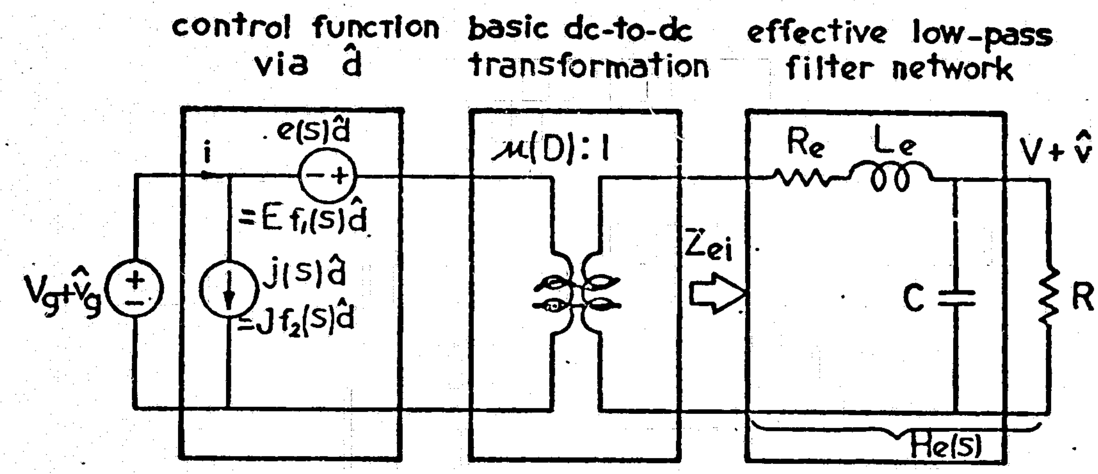
From Figure 17 (C), the canonical dual-input transfer function model for all three regulator power stages in continuous-conduction mode can be obtained, and was presented previously as Figure 7. In the following examples, this model is used for the stability analysis of a single-loop controlled buck regulator.

4.6.2 Single-Loop Controlled Buck Regulator Stability Analysis

The buck regulator used previously in Section 4.5.3 to demonstrate the impulse function analysis is again used here, with the exception that a two-stage input filter is added. The control blocks of the regulator is shown in Figure 18. The dual-input describing-function representation of the regulator is given in Figure 19(A). Based on this diagram, the open-loop transfer function of the regulator can be calculated as:

$$G(s) = F_P G_A G_C G_D \tag{115}$$

The calculated result is given in Figure 19(B). The accuracy of the model is supported by measurement correlations, also shown in Figure 19(B).



type	$\mu(D)$	E	$f_1(s)$	J	$f_2(s)$	L_e
buck	$\frac{1}{D}$	$\frac{V}{D^2}$	1	$\frac{V}{R}$	1	L
boost	$1-D$	V	$1-s\frac{L_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$
buck-boost	$\frac{1-D}{D}$	$\frac{-V}{D^2}$	$1-s\frac{DL_e}{R}$	$\frac{-V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$

Figure 16 Canonical Circuit Models for Three Basic Power Stages

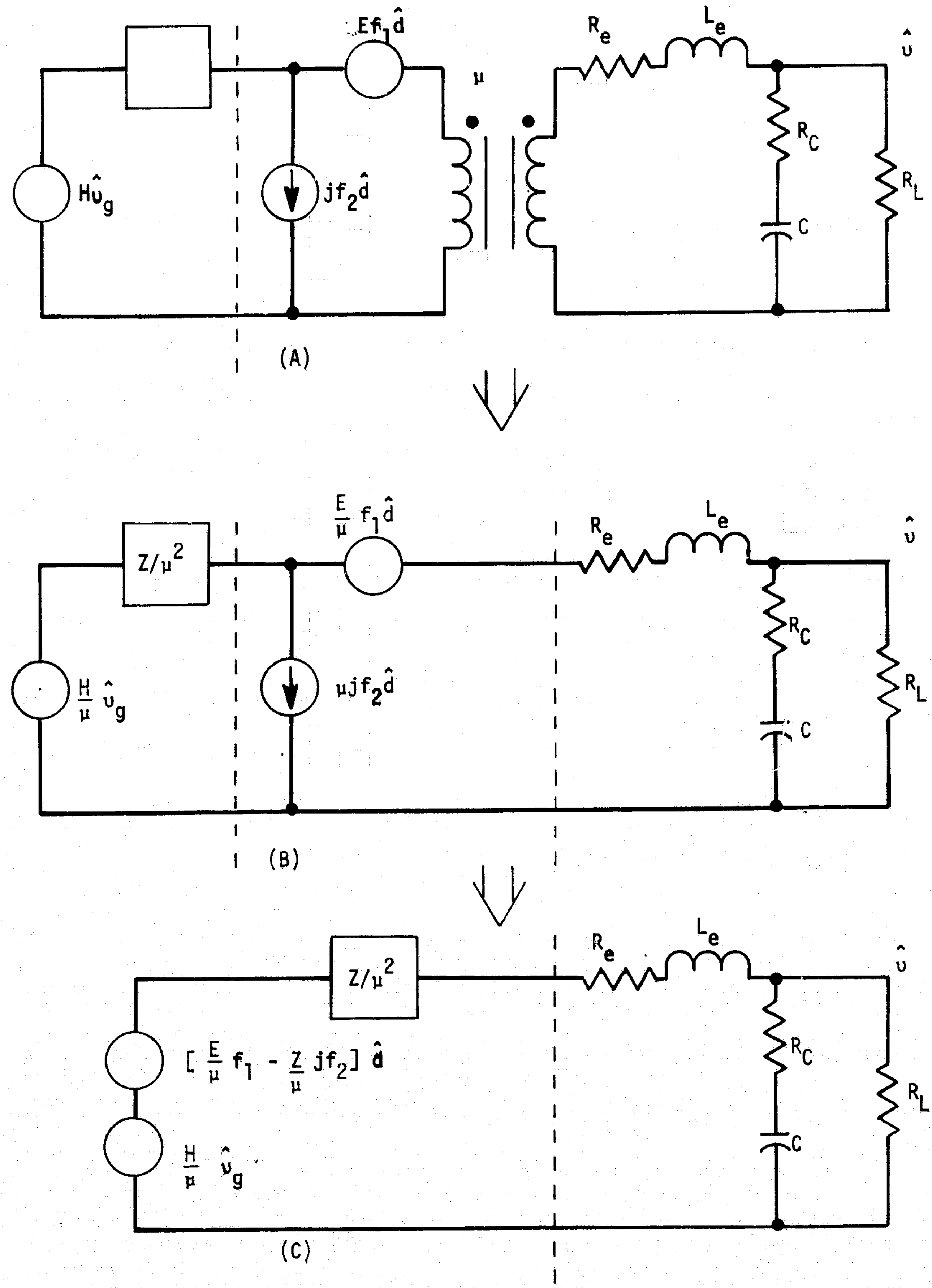


Figure 17 Canonical Model with Input Filter

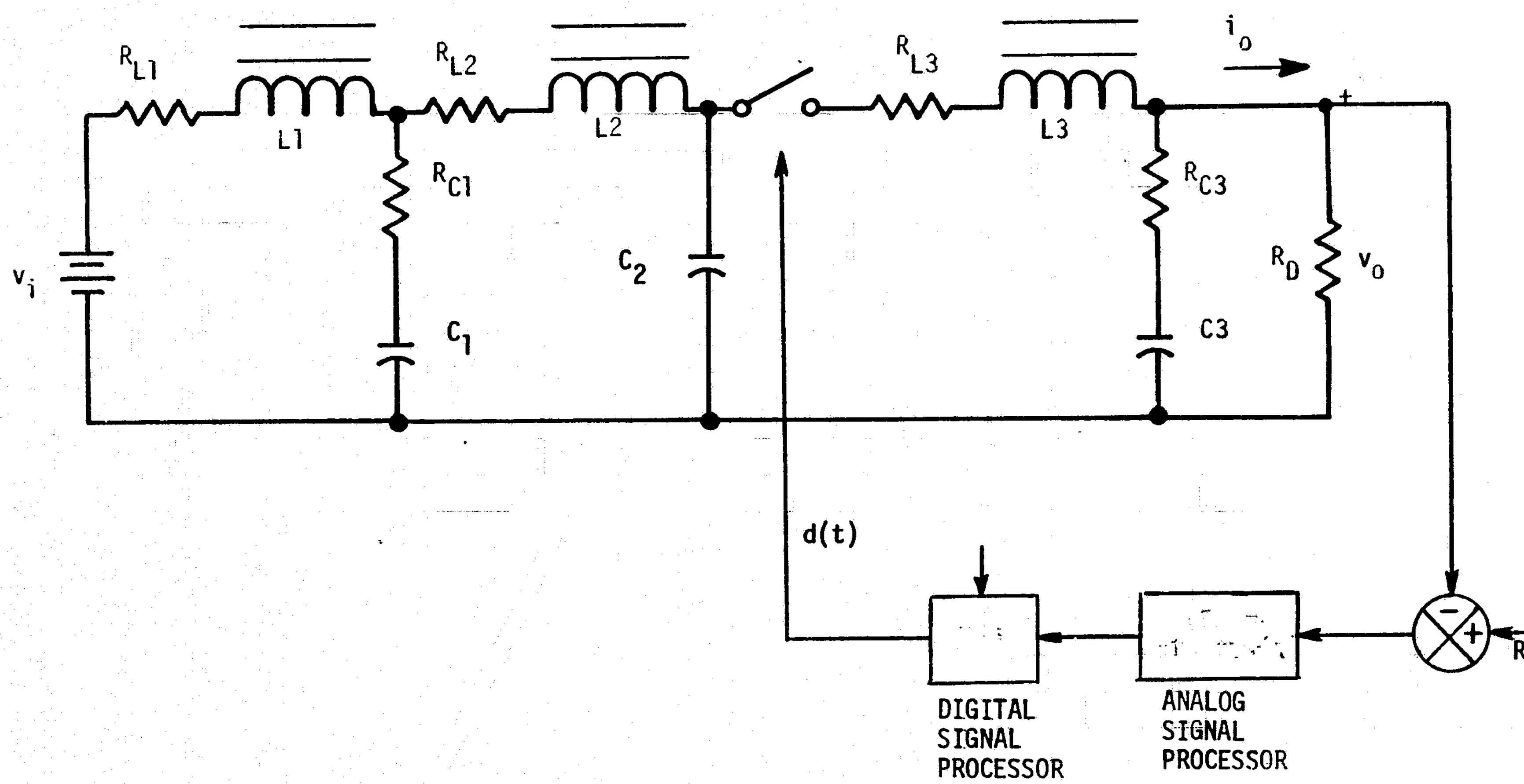
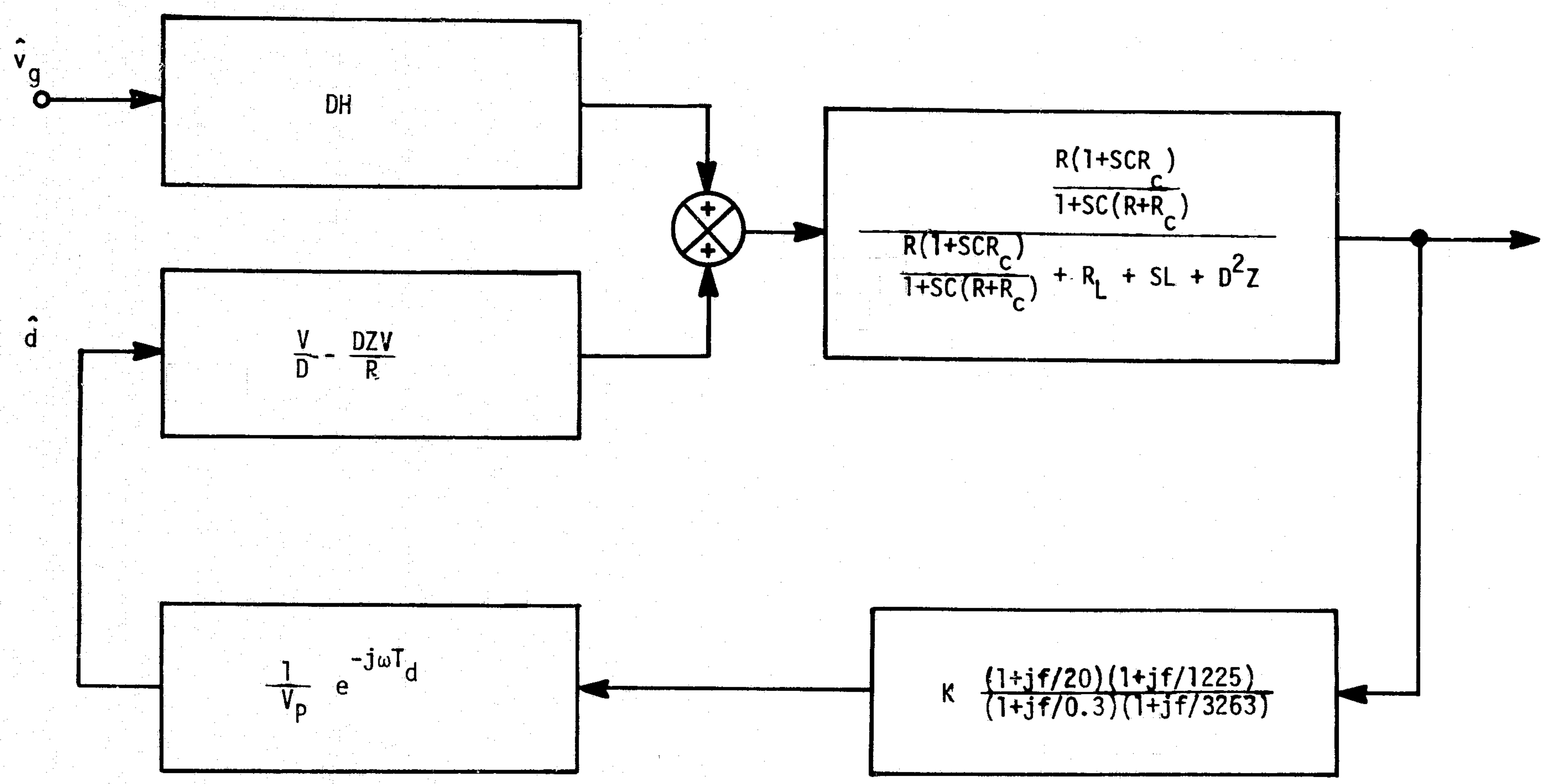


Figure 18 Single-Loop Controlled Buck Regulator with an Input Filter



H : Forward Gain of Input Filter,

D : Duty Cycle

Z : Output Impedance of Input Filter

K : Amplifier DC Gain

Figure 19(A) Dual-Input Describing Function Representation of the Regulator

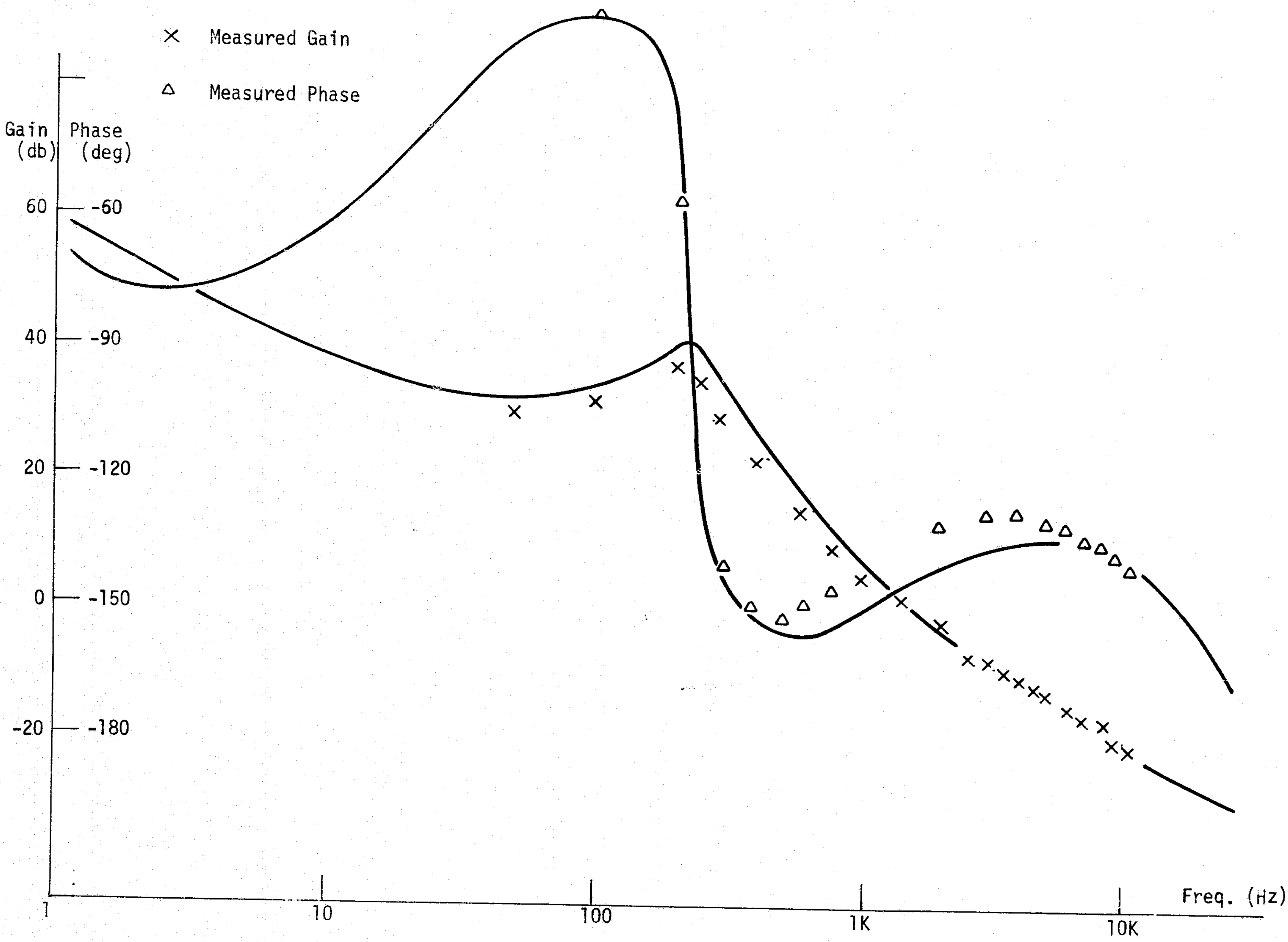


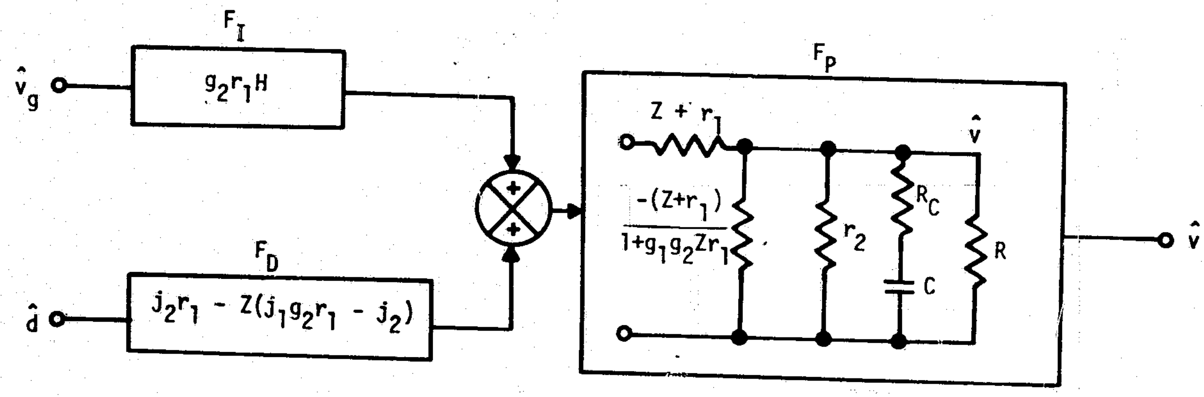
Figure 19(B) Analytical and Measured Data

4.6.3 Discontinuous Conduction Operation

The state-space and circuit averaging methods presented for the continuous-conduction case can be modified to account for the discontinuous operation. The differences are not only that, now there are three different configurations within each switching period, but also that instantaneous inductor current is restricted in its behavior. As shown in Figure 2(B), it starts at zero at the beginning of the switching period, and falls to zero again sometime before the period has expired.

Like the continuous conduction, the culmination of the discontinuous-conduction modeling is again a canonical circuit model for three basic power stages, whose fixed topology is of course different. Modeling details and significant results are provided by Reference [9] , which is included in this report as Appendix J. As in the continuous conduction case, the work has been performed by CalTech.

Using a slightly-modified block-diagram format in relation to that given in Reference [9] , the dual-input transfer functions for basic power stages operating in discontinuous conduction are given in Figure 20. In conjunction with its continuous-conduction counterpart shown previously in Figure 7, they provide powerful tools for conducting regulator analysis for most-commonly used power stages including line-disturbance propagations and input-filter effects on the regulator loop performances.



TYPE	j_1	r_1	g_1	j_2	r_2	g_2	Z	H
Buck	$\frac{2V}{R}\sqrt{\frac{1-M}{K}}$	$\frac{1-M}{M^2}$	$\frac{M^2}{1-M}\ \frac{1}{M}$	$\frac{2V}{RM}\sqrt{\frac{1-M}{K}}$	$(1-M)R$	$\frac{M(2-M)}{1-M}\ \frac{1}{R}$	Z_F	H_F
Boost	$\frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}$	$\frac{M-1}{M^3}R$	$\frac{M}{M-1}\ \frac{1}{R}$	$\frac{2V}{R\sqrt{KM(M-1)}}$	$\frac{M-1}{M}R$	$\frac{M(2M-1)}{M-1}\ \frac{1}{R}$	Z_F	H_F
Buck-Boost	$\frac{2\ V}{R\sqrt{K}}$	$\frac{R}{M^2}$	0	$\frac{2\ V}{R\sqrt{K}\,M}$	R	$\frac{2M}{R}$	Z_F	H_F
Two-* Winding Buck-Boost	$\frac{2\ V}{R\sqrt{K}}$	$\frac{R}{M^2}$	0	$\frac{2\ V}{R\sqrt{K}\ M}$	R	$\frac{2M}{R}$	$\left(\frac{N_S}{N_P}\right)^2 Z_F$	$\frac{N_S}{N_P}\ H_F$

* $M = V_0/(\frac{N_S}{N_P})V_I$, $K = \frac{2L_S}{RT_S}$

Figure 20 Dual Input Transfer Function for Discontinuous Conduction Operation

4.6.4 Summary Remarks on the Average Time-Domain Analysis

Several observations can be made from this example:

(1) From Figure 19, the audiosusceptibility performance can be derived as:

$$\frac{\hat{V}_v}{\hat{V}_g} = \frac{F_I\,F_P}{1 + F_A F_D F_P} \tag{116}$$

Calculated audiosusceptibility based on equation (116) was found to be in very good agreement with the corresponding measurement.

(2) For the buck regulator, the block F_D in Figure 19 can be shown to be:

$$F_D = I_o D\ (\ -Z_F\ )\ \frac{V_I}{I_o D} \tag{117}$$

A necessary condition to avoid system instability due to the input-filter interaction is to maintain F_D positive. In other words, the output impedance of the input filter, Z_F, should always be smaller than the small-signal negative impedance, (V_I/I_oD), of the regulator.

(3) The duty-cycly D is present in blocks F_P,F_D, and F_I. Consequently, the corner frequency and the damping exhibited by the Bode plot should be affected the line input voltage that determines D for a regulated output voltage. This observation was verified both analytically as experimentally.

(4) Different input-and output-filter configurations, including multiple regulator outputs each with its own complex output filter, can be easily incorporated into the dual input block diagram of Figure 19. While the example deals with continuous-conduction only, the canonical dual-input transfer function model can be extended to the discontinuous-conduction as well. The model is therefore a powerfül tool for conducting the control-dependent performance analysis of all switching-regulators.

4.7. DISCRETE TIME DOMAIN SIMULATION AND EXAMPLES

Since the small-signal analytical techniques previously described are no longer applicable for large-signal analysis, and yet the large-signal performance is often a vital part of the hardware design requirement, the significance of the discrete time domain simulation becomes self-evident.

The most-often encountered simulation effort involves step line transient, step load transient, and regulator/converter starting. Specifically, large-signal simulation applies when one of the following conditions arises:

- The large input-filter oscillation as a result of large step line or load change would cause a slowly-varying voltage at the input of the power stage. The consequent slow-varying duty cycle controlled by the loop to maintain output-voltage regulation requires the large signal analysis.

- Large step line/load changes may result in two differenct inductor-current conduction modes for the pre- and post-transient steady state.

- During converter starting and sudden output fault, the protection circuit becomes effective and the operation amplifier experiences saturation.

Two simulation examples, all based on the propagation through exact discrete time-domain system representations presented previously in equations (1) to (18), are given to illustrate the particular simulation approach undertaken in the MAPPS program. The first example simulate a buck-regulator transient response due to a step line change. The objective here is to show that for certain low-order regulator systems, the state transition matrix Φ (T) and the input matrix D (T) may be derived in closed-form, thus greatly improving the cost-effectiveness of the computer simulation. The second example simulate the start-up of a boost regulator, during which power-transistor peak-current limiting and operational-amplifier saturation are inevitably encountered.

4.7.1. Example 1, Step line-change Response of a Buck Regulator

The continuous-conduction buck regulator circuit to be simulated has been given in Figure 8. The duty-cycle control is assumed to be constant - T_{ON}. The state vector $\underline{X}$, the input vector $\underline{U}$, the F and G matrices, and matrices Φ (T) and the D (T), have all been identified previously in Section 4.4 as Equations (59) to (68). The analytical determination of the Φ and D matrices is achieved through the application of the Cayley-Hamilton theorem. [27] Details of the derivation can be found at the end of Appendix A.

Note that with T = Constant in Φ (T) and D (T), Φ (T) and D (T) become constant matrices which need be computed only once. This can be done for the regulator "on" period with $T = T_{ON}$ (or integer submultiples of T_{ON} if data points in-between are desired). Defining

$$\Phi\,(T_{ON}) = \Phi_N = \text{Constant,} \tag{118}$$

$$D\,(T_{ON}) = D_N = \text{Constant} \tag{119}$$

equation (68) becomes

$$\underline{X}\,(t_k + T_{ON}) = \Phi_N\,\underline{X}\,(t_k) + D_N\,\underline{U}\,(t_k) \tag{120}$$

Off time T_{OFF} is generally not constant, being a variable determined by the control-signal error. Using the closed-form expressions for Φ (T) and D (T), T_{OFF} can be solved for implicity or by linearization about a nominal value. If the nominal value of T_{OFF} is denoted by

$$T_{OFF}^{*} = \text{nominal } T_{OFF}$$

then, just as before, one can define and precompute the constant matrices

$$\Phi\,(T_{OFF}^{*}) = \Phi_F = \text{constant,}\quad D\,(T_{OFF}^{*}) = D_F = \text{constant}$$

which may then be used in equation (68) for partial state propagation during the "off" period. The application of these observations will speed up digital computation considerably. The time step T can be specified as a fraction (including unity) of the constant T_{ON} and the nominal T_{OFF}^{*} periods.

Thus, using the closed-form solution of Φ and D, the three system states e_o, i, and e_c, can be propagated by constant state transition matrices until either the fixed, known T_{ON} has elapsed, or, with the switch off, until the unknown T_{OFF} has been transgressed. In the latter case, after exceeding the specified threshold, iterative linearization on the propagation time T, which appears as a parameter in the expression for the closed-form solution, is used to determine the exact time when e_c has reached the threshold.

A flow chart of the simulation program is given in Appendix H. The program, written in FORTRAN IV, was exercised with several runs, one of which is included here as Figure 21. The figure illustrates the output-voltage response to a step voltage change at the regulator input from 30V to 40V for a load resistance of 10 ohms. The simulated response was found in excellent agreement with laboratory test data. The simulated run time is 3.5 milliseconds, and the number of data points per each switched period is five (5). The central processor time used for this simulation is only 17.9 seconds, which vividly demonstrates the cost-effectiveness rendered by the use of closed-form solutions. For most runs, the cost of plotting exceeds the central processor cost of running the simulation. A rule of thumb is that most runs, inclusive plotting and time-share terminal usage, will cost about $1.50 per run.

4.7.2 Example 2 Start-up Transient of a Boost Regulator

A boost regulator with input voltage E_I and load R_L is shown in Figure 22. Two switches, S1 and S2, represent the power transistor and power diode, respectively. The state variables of the system are:

v_c = voltage across output capacitor C_o.

i = current through energy-storage inductor L_o.

e_R = voltage at the junction of compensation network R5-C2

e_C = the integrator-amplifier output voltage.

Output Response to a Step Input Voltage Change (30-40V)

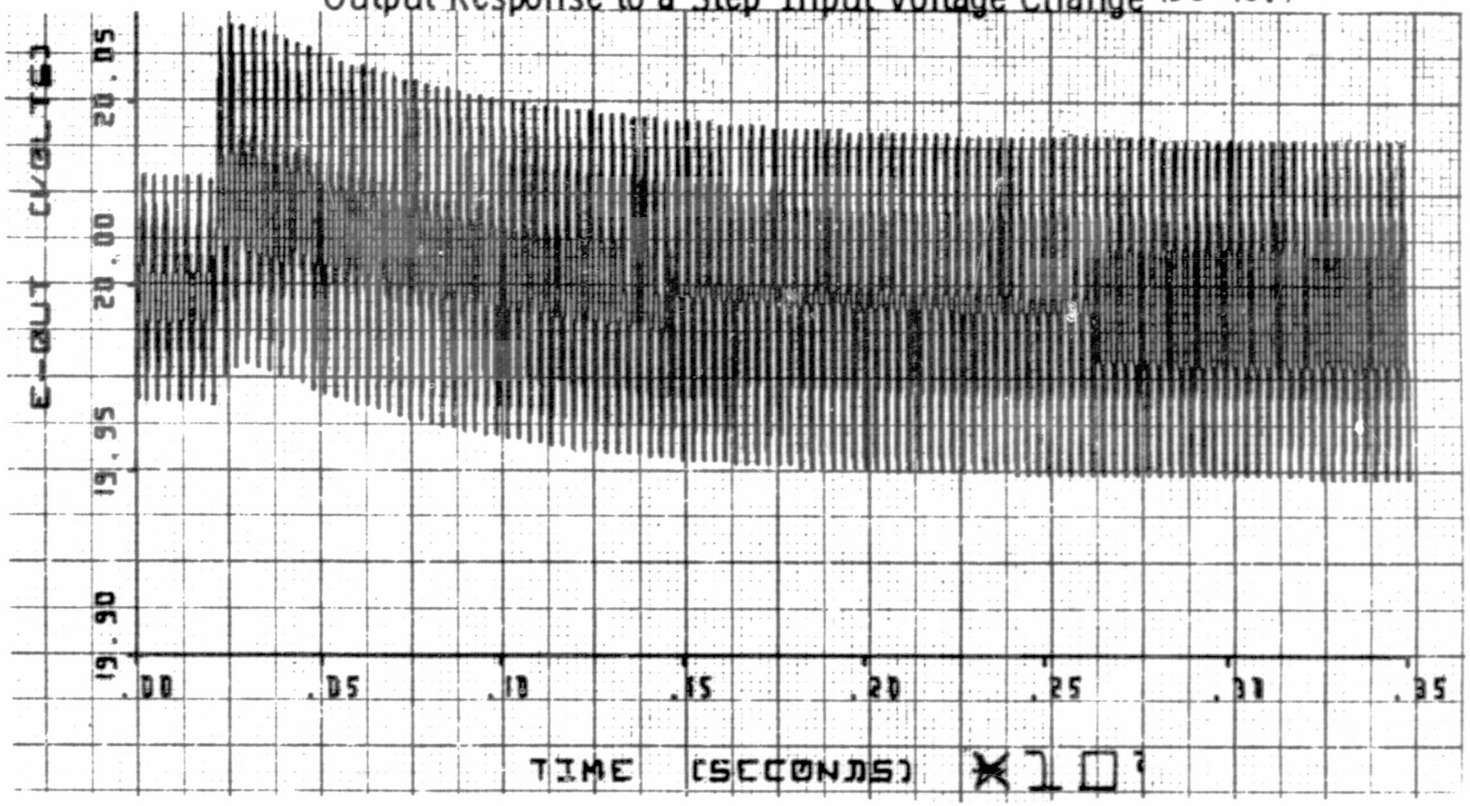


Figure 21 Sample of Buck Regulator Simulation Run

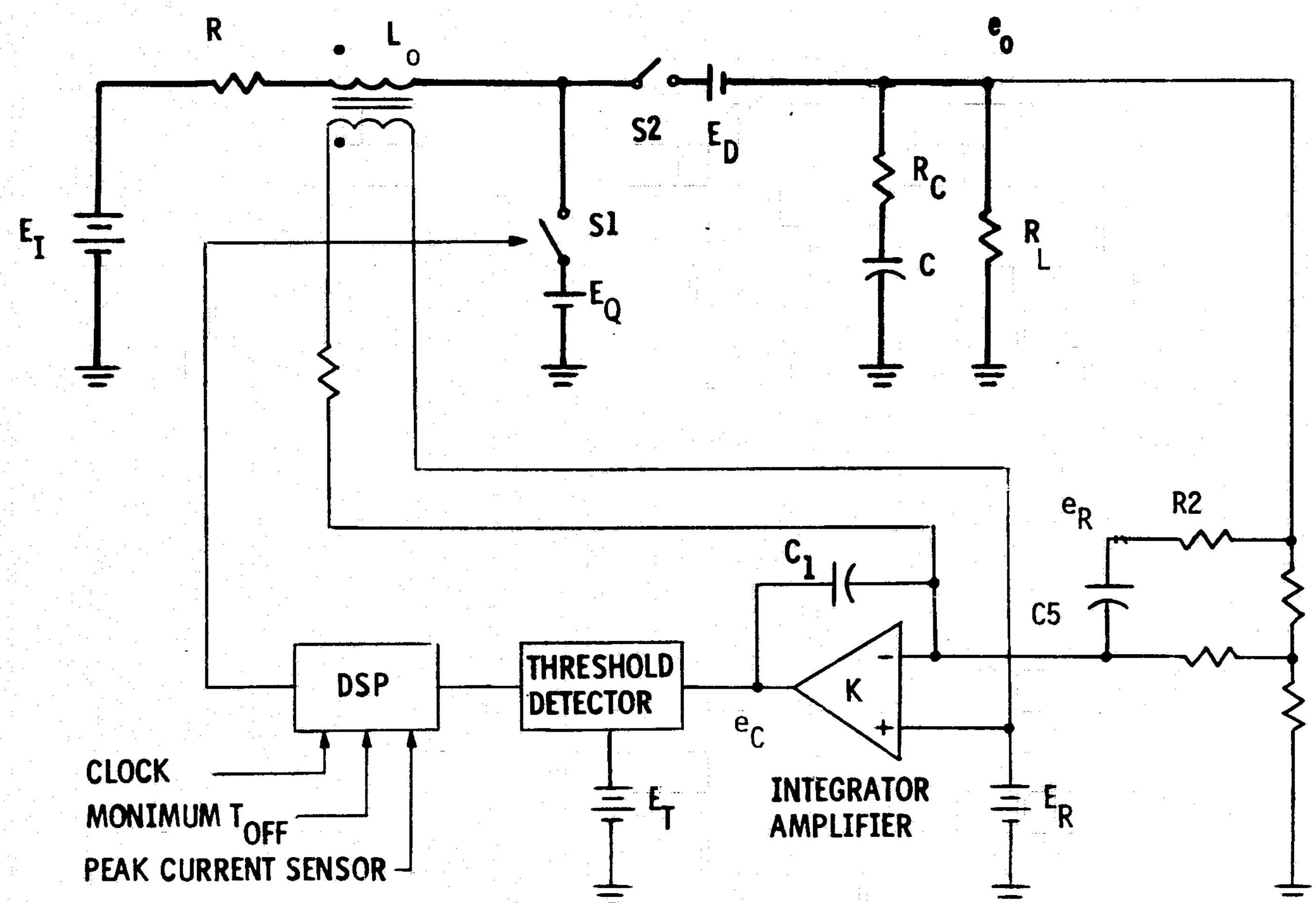


Figure 22 A Multiple-Loop [illegible]olled Boost Regulator

Three possible modes of operation are illustrated in Figure 23. They are:

(1) The power transistor is ON, and the diode is OFF. This interval has been designated previously as T_{ON}.

(2) The power transistor is OFF, and the diode is ON. This interval has been designated as T_{F1}.

(3) Both the transistor and the diode are OFF. This interval has been designated as T_{F2}.

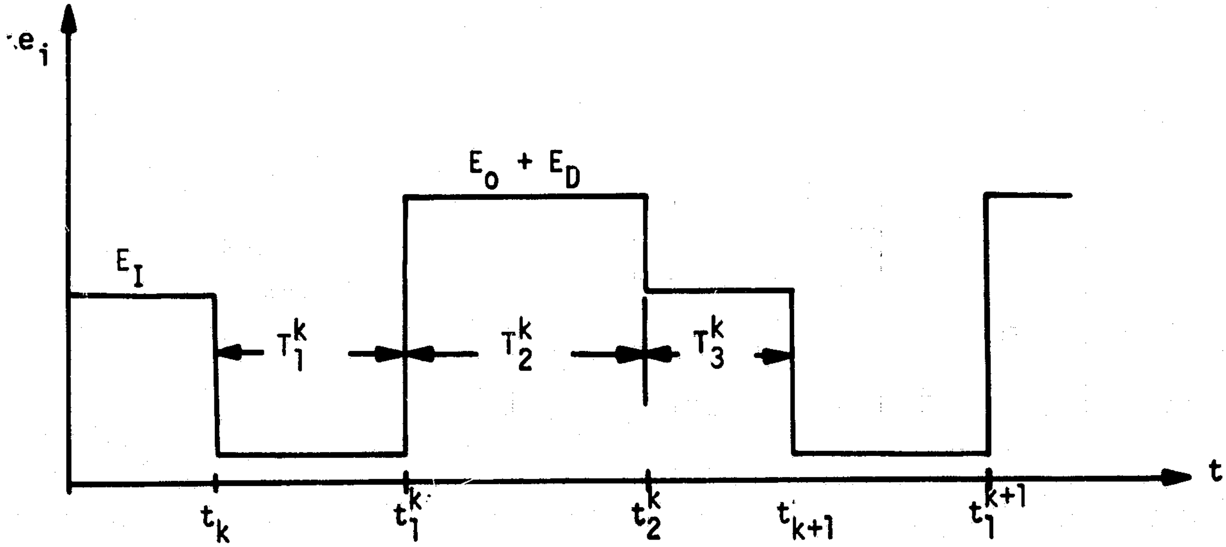
The continuous-conduction case includes only the first two operating modes, while the discontinuous-conduction includes all three modes. The system in this example is designed to operate in discontinuous conduction during steady state. However, during transients excursions into the continuous conduction are possible. Each of these intervals admits the following closed-form solutions:

$$\underline{X}\,(t_1^k) = \underline{X}\,(t_k + T_1^k) = \Phi_1(T_1^k)\,\underline{X}\,(t_k) + D_1(T_1^k)\,\underline{U} \tag{121}$$

$$\underline{X}\,(t_2^k) = \underline{X}\,(t_1^k + T_2^k) = \Phi_2(T_2^k)\,\underline{X}\,(t_1^k) + D_2(T_2^k)\,\underline{U} \tag{122}$$

$$\underline{X}\,(t_{k+1}) = \underline{X}\,(t_2^k + T_3^k) = \Phi_3(T_3^k)\,\underline{X}\,(t_2^k) + D_3(T_3^k)\,\underline{U} \tag{123}$$

where Φ and D have been identified in equation (67), and the various time intervals and time instances are defined in Figure 23. The time interval T_1^k is a function of the system state $\underline{X}\,(t_k)$, the threshold condition, or the peak current limiter. The time interval T_2^k is a function of the system state $\underline{X}\,(t_1^k)$, the inductor current, or the period T_p of regulator switching. The time interval T_3^k is the difference between T_p and $(T_1^k + T_2^k)$. Details concerning the Φ and D matrices in Equations (121) to (123) are presented in Appendix G.



$t_K \leq t < t_1^K$	Power transistor ON Diode OFF Continuous inductor current
$t_1^K \leq t < t_2^K$	Power transistor OFF Diode ON Continuous inductor current
$t_2^K \leq t < t_{K+1}$	Power transistor OFF Diode OFF Zero inductor current

Figure 23 Possible Modes of Boost Regulator Operation

Digital simulation of the regulator is based on equations (121) to (123). The step T in each computation is specified as a fraction of the steady-state values of the corresponding time intervals T_i, i = 1,2,3. Thus, using the closed-form solutions, the system state can be propagated by $\Phi_1(T)$ and $D_1(T)$ until the time period T_1^k has elapsed due to one of the aforementioned threshold boundries. Subsequently, $\Phi_2(T)$ and $D_2(T)$ are used to continue the propagation. If the inductor current vanishes prior to the end of one switching period, $\Phi_3(T)$ and $D_3(T)$ are invoked until the end of the clock period, and the system engages in discontinuous-conduction operation. However, if the switching period elapses before a zero inductor current is reached, continuous-conduction prevails, and $\Phi_3(T)$ and $D_3(T)$ will not be introduced.

The flow chart and the computer program are not included here for conciseness. The program was exercised with several runs. Two runs, one for step load transient response, the other for regulator command-on start up, are presented here.

Figure 24 illustrates the output-voltage transient during a step change of load from 50 ohms to 25 ohms. An undershoot of 0.25V is observed, which recovers to its nominal output in about 3 milli-seconds. The response is found in good agreement with the test result.

Figure 25 shows the inductor-current transient during the regulator startup. Upon commanded on, the current rises to the pre-set peak current limit, followed by an off time interval which lasts the rest of the switching period. The peak-current limiting operation persists for two more cycles before entering a continuous conduction mode when the rising output voltage causes the inductor current to diminish more during T_{F1} than to rise during T_{ON}. The current eventually reaches the discontinuous conduction as dictated by the intended steady-state operation. Again, excellent agreement was obtained between the simulation and the actual hardware performance.

4.7.3 Summary Remarks on Time-Domain Simulation

The utility of time-domain simulation lies in its unique capability to handle multiple nonlinearities arising from the propagation of large-signal disturbances. While there exist many different topological and/or block-oriented simulation approaches, the particular discrete time-domain formulation used in the MAPPS program, as illustrated in the examples given, is inherently basic to all the seemingly-different simulation programs such as ECAP, SCEPTRE, SPICE, CSMP, etc. Consequently, instead of making the simulation program so generalized as to conciliate with the convenience of a great many of perspective users, thus making the program inevitably cost ineffective, the particular approach used in the MAPPS program and embodied in these examples utilizes the inherent piecewise linearity and threshold boundry of a switching regulator, and conceives an approach specifically adapted to the cyclic nature of the switching regulators. Compared with other more generalized approach, the cost-effectiveness of the simulation is improved, often more than an order of magnitude. This cost-effectiveness is expected to enhance the utility of the simulation, particularly for more complicated, higher-order regulator systems.

Since different regulator circuits have different topologies, duty-cycle control laws, and operating constraints during transients, the simulation is best suited for, although not limited to, regulator circuits for which the designs have been fairly well standardized.

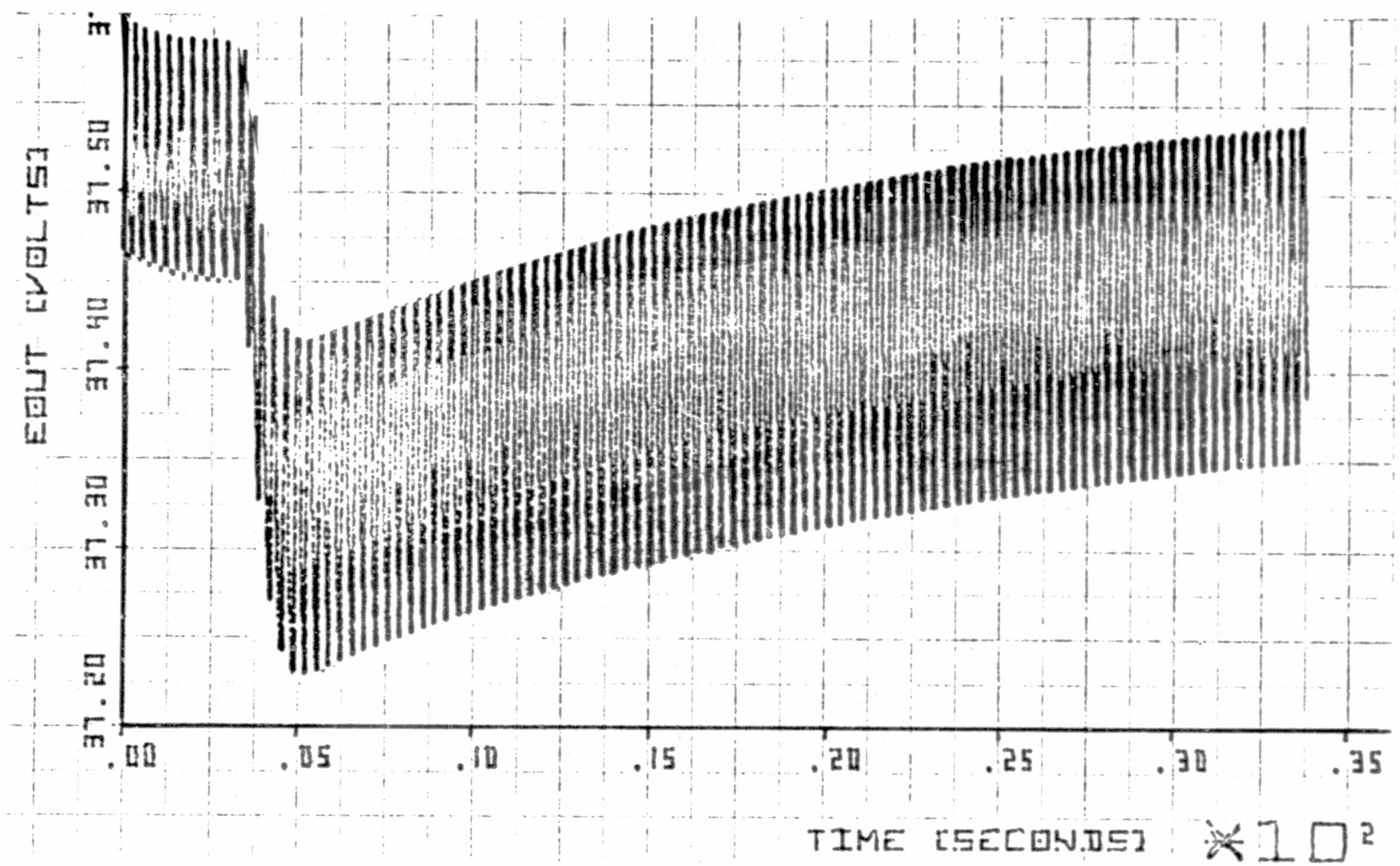


Figure 24 Simulated Output Voltage Response for a Step Load Change

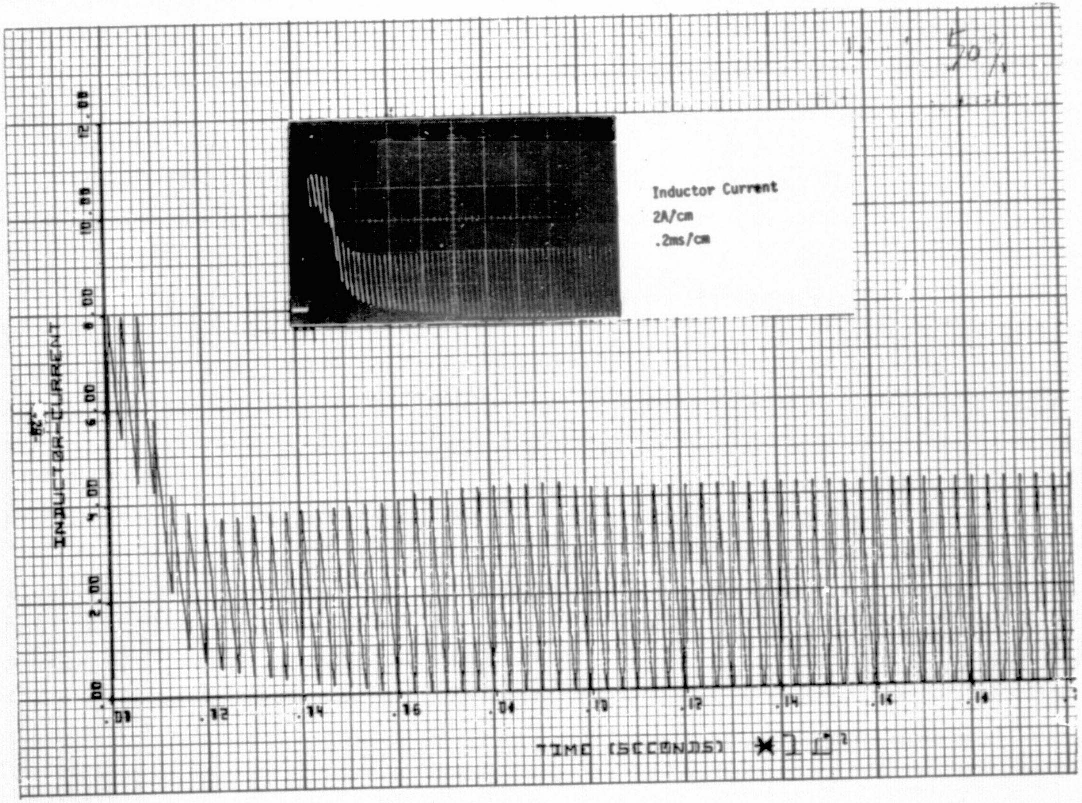


Figure 25 Simulated and Observed Regulator Start-up Transient

4.8 SUMMARY, FUTURE EMPHASIS AND EXPECTATION

In Section 4, the nonlinearities in the switching regulators were identified, from which the various analytical methods based on different linearization techniques were advanced. The discussion centers on four major analysis/simulation categories:

- Discrete time domain analysis
- Impulse function analysis
- Average time domain analysis
- Discrete time domain simulation

Merits and limitations of these approaches were pointed out, and illustrated by analysis/simulation examples as practical.

Being the most accurate method for assessing the small-signal stability, emphasis on the discrete time-domain analysis will be continued in the future. The intent will be to create three subprograms, one for each of the three basic power stages (buck,boost, and buck-boost). Each subprogram will include both continuous- and discontinuous-conduction operations as well as the various duty-cycle control schemes including constant frequency. The multiple-loop control circuit described in certain previous examples will be used in the subprogram due to its standardization appeal. In conducting the analysis, special attention will be paid to describing clearly the formulation of analytical procedure and the details of achieving cost-effective computer iteration, so that any user with a proper background can follow the step-by-step description, and adapt the analysis to the circuit of his own choice.

Although minor differences do exist, the impulse-function analysis and the average time domain analysis both provide the basic power-stage duty-cycle-to-regulator-output transfer function. However, by retaining in the analysis the discrete nature of the regulator until essentially the very last analytical step, the impulse-function analysis, thus, does not concern itself with the small-signal line-to-output-voltage perturbation.

The average time-domain analysis, on the other hand, forsakes the discrete nature of the regulator almost at the outset of the analysis, and therefore manages to address both the duty-cycle-to-output and line-to-output perturbations.

Since the input-filter-regulator interaction and the audiosusceptibility performance are of great significance to regulator designers, future emphasis is inclined toward the averaging approach. Other incentives for the continued pursuit of the average approach include the following:

- Being essentially a linear circuit analysis, the approach is applicable to many designers whose background may not be sufficient to perform, or even to comprehend, the more mathematically sophisticated discrete approach.

- By treating the complete regulator as a single entity, the discrete approach is most suitable to perform an accurate analysis of a regulator with a standardized power- and control-circuit configuration. While standardization is a goal to be diligently pursued by government/industrial concerns, the degree to which designs will be standardized, and the ultimate standardized configuration, are not clear at the present time. For the time being, the average time domain analysis can accomodate more readily the numerous varieties of analog signal processors than its discrete counterpart.

- For higher-order regulators (e.g., those with multiple outputs, each having complex loadings), the average approach is more cost-effective in terms of the required computer time in conducting the control-dependent performance analysis.

The discrete-time domain simulation is a natural product of discrete time domain analysis. The analytical involvement is straightforward, and the major effort is to implement the computer iteration routine for cost effectiveness. Performance simulation undoubtedly will continue for different regulators. However, advancements from modeling as the analysis viewpoint will probably be somewhat confined.

5. CONTROL DESIGN SUBPROGRAM

In the previous section, various methods of conducting performance analysis were discussed. However, one cannot help but to note that, before subjecting the design to the analysis, one must have a design first. Preferrably, the design should be based on certain well-conceived design guidelines, from which the ensuing design can more or less be expected to achieve a given level of control-dependent performances. After all, the primary function of a power-processing engineer is to design in accordance with a given set of performance requirement, and it will be far more effective if the designer can proceed with the design confidently, knowing what performances can be expected from the design rather than having to rely on the results of the performance analysis to guide major design iterations. Since a regulator's static and dynamic performances are effected primarily by the quality of its control circuit, the essence of the Control Design Subprogram is to perform an "analytically-based" design that will enable the regulator to meet the specified control-dependent performances.

As stated previously, a regulator control circuit is composed of an analog signal processor and a digital signal processor. The digital signal processor prescribes the scheme of duty-cycle control of the power switch. Different duty-cycle control schemes do provide different regulator performance characteristics. However, their impacts are generally not of a major proportion. Furthermore, the design of digital signal processors is often dictated by requirements such as frequency synchronization and EMC considerations, which are only remotely related to the feedback control. Consequently, the other half of a regulator control circuit, the analog signal processor, invariably holds the key in determining the quality of the regulator feedback loop, which is instrumental in determining the regulator external characteristics such as stability, audiosusceptibility, output impedance, and step line/load transient response. The specific function of the Control Design Subprogram, therefore, is to determine the design of the analog signal processor, based on a preselected amplification and compensation configuration, in order to meet a given set of performance requirements.

5.1 CONTROL DESIGN APPROACH

To gain more insight to enhance the initial parameter design, approximate design equations and circuit characterizations expressed in closed form are obviously preferred even though their accuracy may not match the precise numerical calculations performed by a digital computer. The average time-domain analysis previously discussed thus becomes the leading candidate on which the control design can be based.

The given power stage is characterized by a continuous small-signal average model, taking full advantage of the much lower ouput-filter resonant frequency in relation to the converter switching frequency. Describing function techniques are used to derive the gain/phase transfer function of the digital signal processors. The analog signal processor to be designed presents no particular difficulty for analysis, as only linear circuit small-signal analysis is involved.

It should be noted that essentially the same approach is being taken in another NASA-sponsored TRW program under Contract NAS3-20102: "Application Handbook for a Standardized Control Module for Dc-Dc Converters", in which the aforedescribed approach is used to analyze the multiple-loop controlled regulators and to conceive design guidelines which enable the user to design readily the control parameters in order to meet a given set of performance specifications. In fact, selected outputs of the Application Handbook will be integrated into the MAPPS structure as Control Design Subprograms during the next program phase.

5.2 A GENERALIZED CONTROL BLOCK DIAGRAM, SINGLE VS. MULTIPLE-LOOP CONTROLLED REGULATORS

A generalized control block diagram was shown in Figure 1. The three basic power stages, the buck, the boost, and the buck boost, can operate in either continuous or discontinuous-conduction.

Depending on the digital-signal processor mechanization, different forms of duty-cycle control of the power switch are possible. These forms include constant frequency, constant on time, constant off time, bistable trigger, and variable frequency based on variable on time and off time. While the digital-signal-processor implementations proposed and in use today may appear numerous, they can always be reduced into two basic ingrediants: a threshold level and a ramp function. The intersection of these two ingredients initiates the switching action of the duty-cycle control. In single-loop controlled switching regulators, the ramp or the threshold is derived from the output of the analog signal processor, which, in turn, derives its input from sensing the regulated quantity at the output of the power stage. However, in certain more recent multiple-loop control developments [11,28], incentive in achieving a much-improved stability performance has resulted in an extra loop sensing an additional state variable associated with the power stage. In this implementation, the needed ramp is obtained from processing a steady-state switching waveform inherent within the output filter.

The analog-signal processor processes the amplification and compensation of the analog signal(s) sensed from the power stage. The processor presents no particular analytical difficulty, as only linear circuits are involved and merely small-signal analysis is intended. However, since it holds the most leverage in determining the control-dependent performances, it naturally becomes the target of the Control Design Subprogram using the average time domain approach. In the following discussion, both single- and multiple-loop analog signal processors will be addressed.

Due to the presence of a second-order low-frequency output filter, the utilization of a high-gain and wide-bandwidth amplifier for good static and dynamic regulations usually results in an increasing risk of instability. While the stability can be enhanced through various second-order pole-zero cancellation techniques, the cancellation becomes grossly ineffective in the face of cumulative component changes due to tolerances, environments, and aging. More importantly, external reactive loading which is generally not fully defined in the regulator development stage, may completely destroy the elaborate pole-zero cancellation conceived for a resistive load which is often assumed during the regulator development.

With the existing pole-zero cancellation eneffective against component and loading changes, compensation of the second-order filter should ideally be achieved adaptively, i.e., any change is met with a corresponding change in the compensation such that an effective pole-zero cancellation is automatically maintained. Intuitively, such an achievement must involve the sensing and processing of inductor voltage or capacitor current associated with the output filter. No adaptive compensation of the second-order filter is conceivable without utilizing its state variables for control purposes.

This sensing, which is additional to the error sensed from the regulated quantity, is unique to the multiple-loop control.

Before presenting examples of single- and multiple-loop analog signal processor designs, two clarifications are needed:

(1) The Control Design Subprogram was not part of the original work plan for the MAPPS program. It was added during the course of the program amidst a growing inclination, on the part of both TRW and NASA, that the MAPPS objective could not be well served with only Performance Analysis Subprograms, and that the MAPPS utility would be diminished unless some control design subprograms could also be included. This inclusion was achieved at no attendent cost/schedule adjustment. Consequently, one would view the subprograms conceived here only as a prelude to a more intensive effort in the future.

(2) The Control Design Subprogram, for the time being, does not perform the optimum control-circuit synthesis. Rather, the intention here is to take a fixed analog-signal-processor circuit topology, and to perform the detailed design of circuit parameters to meet a given set of control-dependent performances.

Having made these clarifications, two control design examples are provided to illustrate the existing effort on the Control Design Subprogram.

5.3 CONTROL DESIGN FOR A SINGLE-LOOP ANALOG SIGNAL PROCESSOR

In the regulator shown in Figure 26(A), the buck power stage, the digital-signal processor, and the switching frequency are assumed given. The objective here is to perform the design for the analog-signal-processor block, G_c to achieve the following regulator control-dependent performances.

(1) A crossover frequency at about one-tenth of the switching frequency
(2) A phase margin of Φ_c deg. at the crossover
(3) A given dc gain

The control block diagram of the regulator is shown in Figure 26(B), from which the following steps of the analog-signal processor design procedures can be presented.

5.3.1. Step-by-Step Design Procedures

Step 1: Provide Bode plot for the given power stage and digital signal processor

For the given example, the describing funtion K_M of the digital signal processor is a constant gain without phase delay, and the power stage $K_P F_P$, is of second-order. As an example, 20 log $K_M K_P F_P$ is shown asymptotically as curve (1) in Figure 27. The power-stage transfer function $F_P(s)$ is expressed as:

$$F_P(s) = (1 + S\tau_c)/[1 + \xi(S/\omega_N) + (S/\omega_N)^2] \quad (124)$$

Here τ_c is generally associated with Λ output capacitors, while ξ and $(\omega_N/2\pi)$ are the damping factor and the natural resonant frequency of the output filter. At the intended crossover, the phase margin of $K_M K_P F_P$ is designated Φ_c.

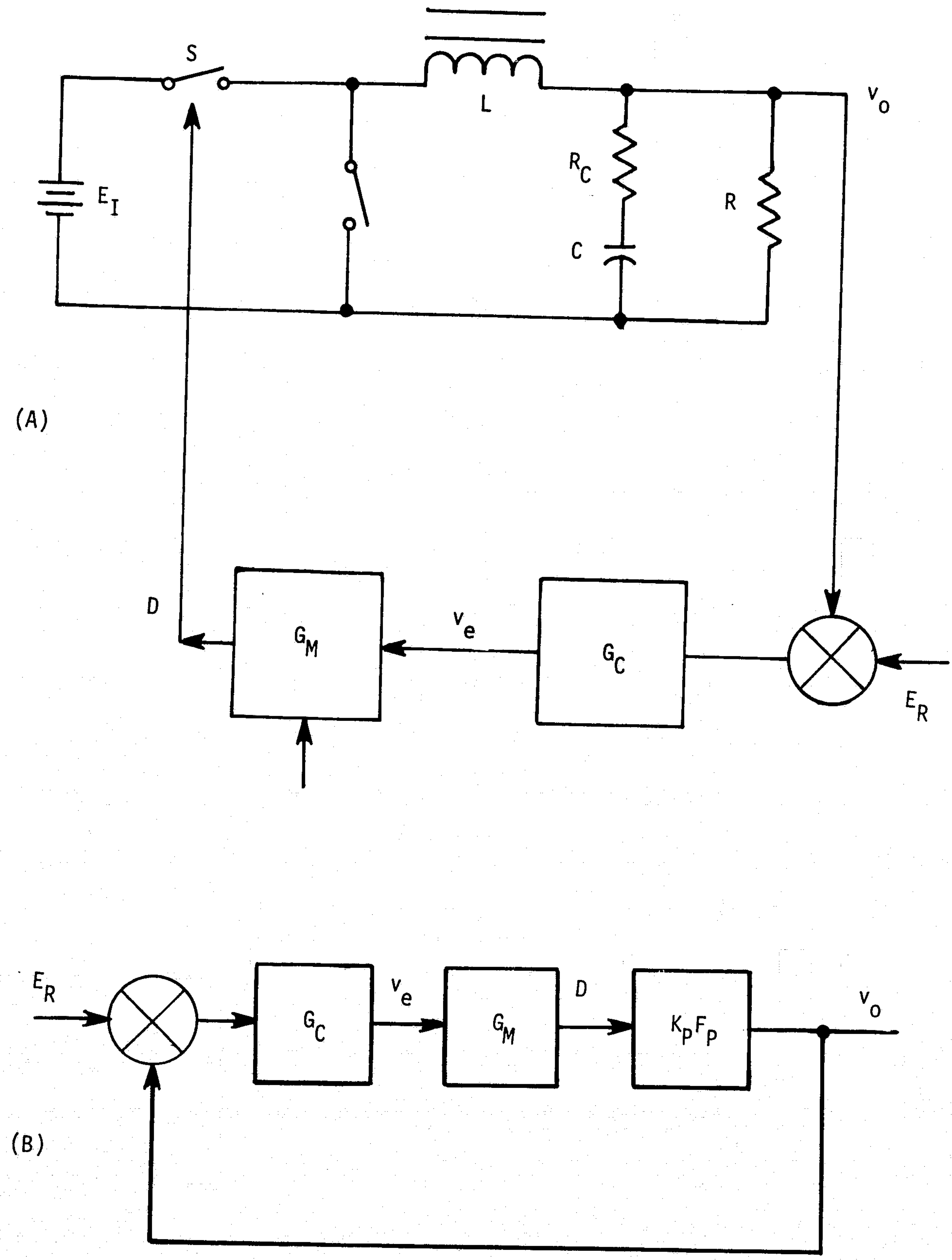


Figure 26(A) Buck Regulator and (B) Control Block Diagram

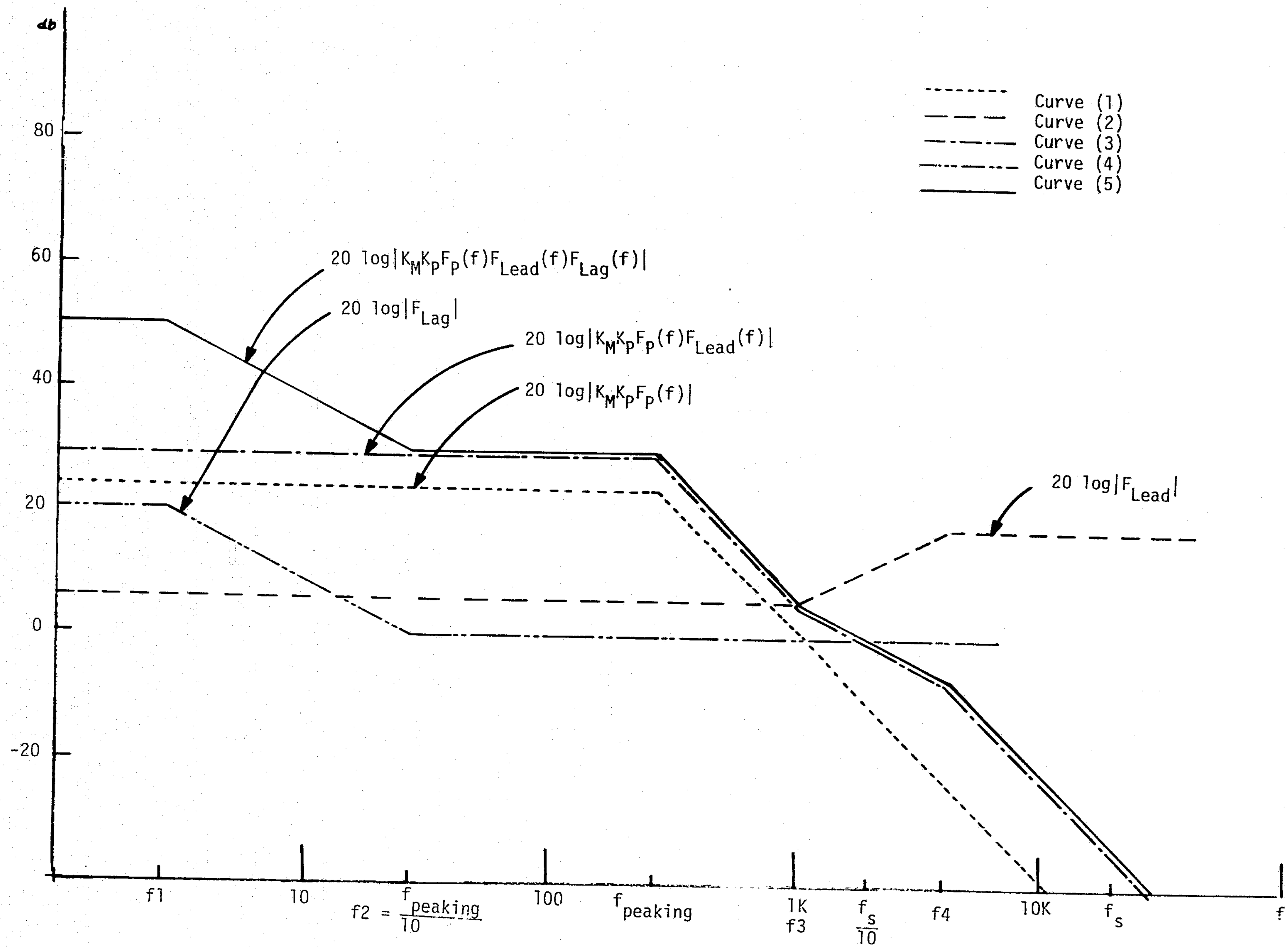


Figure 27. Asymptotic Plot for Control Design

Step 2: <u>Determine the need for a lead network</u>

From curve (1), the crossover is about 1KHz, with very poor phase margin. A lead netwrok is therefore needed to raise the crossover frequency from 1KHz to $0.1f_s$ = 2KHz, with attendant phase-margin improvement. The lead compensation normally has the transfer function of the form:

$$F_{lead} = K_{lead} \frac{1 + jf/f_3}{1 + jf/f_4} \tag{125}$$

The maximum phase-lead occurs at:

$$f_M = (f_3 f_4)^{0.5} \tag{126}$$

and is equal to:

$$\Phi_M = 90° - 2 \tan^{-1}(f_3/f_4)^{0.5} \tag{127}$$

Normally, one should design the maximum lead-phase at the crossover frequency. The three unknowns, namely, f_3, f_4, and K_{lead}, should then satisfy the following three equations in order to meet the specified phase-margin requirement, Φ_X, at f_c.

$$(f_3 f_4)^{0.5} = 0.1f_s \tag{128}$$

$$90 + \Phi_c - 2 \tan^{-1}(f_3/f_4)^{0.5} \geq \Phi_X \text{ deg.} \tag{129}$$

where Φ_c obtained from Step 1. The lead-network dc gain, K_{lead}, has to satisfy the following equation in order to get the desireable crossover that has a maximum phase lead:

$$K_{lead} = \log^{-1}\left[\frac{1}{100} \frac{f_s}{f_3} - \log |K_M K_P K_P (f_3)| \right] \tag{130}$$

Step 3: Check dc gain

The dc gain of $K_M K_p K_{lead}$ is compared with the given dc gain requirement, K_{dc} to see if $K_M K_p K_{lead} \geq K_{dc}$ is met.

Step 4: Determine the need for a lag network

If the above inequality is not satisfied, a lag network is needed to increase the system dc gain. The lag-network transfer function normally has the form:

$$F_{lag} = \frac{f_2}{f_1} \frac{1 + jf/f_2}{1 + jf/f_1} \tag{131}$$

The frequency f_2 should be designed sufficiently low so as not to increase the system phase lag. A reasonable f_2 would be one tenth of the filter natural frequency, $f_N = (\omega_N/2\pi)$.

Once f_2 is determined, the corner frequency f_1 can be derived in conjunction of K_{dc}. Let

$$f_2 = 0.1\ f_N\ (1-2\xi^2)^{0.5} \tag{132}$$

$$K_M K_p K_{lead}\ (f_2/f_1) \geq K_{dc} \tag{133}$$

From (132) and (133), f_1 can be determined as:

$$f_1 \leq f_2\ \frac{K_M K_p K_{lead}}{K_{dc}} \tag{134}$$

Step 5: Complete the design of lead-lag compensation network

Here,

$$G_c = K\ \frac{1+jf/f_2}{1+jf/f_1} \cdot \frac{1+jf/f_3}{1+jf/f_4} \tag{135}$$

where

$$f_3 = 0.1\ f_s\ \tan\frac{90+\Phi_c-\Phi_x}{2} \tag{136}$$

$$f_4 = 0.1\ f_s\ (\tan \frac{90+\Phi_c-\Phi_x}{2})^{-1} \tag{137}$$

$$K_{lead} = \log^{-1}[(0.01\ f_s/f_3) - \log|K_M K_p F_p|_{at\ f_3}] \tag{138}$$

$$f_2 = 0.1\ f_N\ (1-2\xi^2)^{0.5} \tag{139}$$

$$f_1 \leq 0.1\ f_N\ (K_M K_p K_{lead}/K_{dc})\ (1-2\xi^2)^{0.5} \tag{140}$$

$$K = K_{lead}\ (f_2/f_1) \tag{141}$$

Step 6: Numerical design

From the known power stage, digital signal processor, and the switching frequency, the values for K and f_1 to f_4 in equation (135) can be numerically determined.

Step 7: Design of network parameters

Once the transfer function G_c in equation (135) is numerically determined, the actual networks to implement the calculated G_c can vary. Figure 28 shows a fairly-universal lead-lag compensation network, where C1 and C2 serve as lead and lag capacitor, respectively. Since their corner frequencies are widely apart, a practical approximation can be made to simplify the network synthesis by assuming that the lead capacitor C1 is open in the low-frequency range, as that the lag capacitor C2 is short in the high frequency range. By so doing, it becomes rather straightforward to relate the design of transfer function G_c to the network parameters shown in Figure 28. The end result is demonstrated in the following subprogram.

5.3.2 Control Design Subprogram

In this subprogram. The regulator shown in Figure 26 has the following parameters: L = 1mH, E_i = 25 to 50V, C = 455μF, E_o = 20V, R_s = 0.068 ohms, R_L = 6.7 ohms, and f_s = 20KHz. The design requirements are to have a crossover frequency of 2KHz, a phase margin of 45 deg., and a room-temperature dc regulation of 0.1%.

The design equations and lead-lag synthesis discussed in the previous section have been programmed into the control design subprogram. Upon logging in, the user will be presented with a summary of all the parameter inputs. Upon user's instruction, the subprogram will proceed to perform the design analysis, from which the unknowns K_1, f_1,f_2,f_3, and f_4 in equation (135) are identified, and the RC networks in the analog-signal processor properly designed. To verify that the design indeed meets the specified requirements, the user has the option of requesting an analysis of the regulator open-loop frequency response based on the finished design. A computer printout illustrating these features is given in Figure 29.

Notice that the computer cost of all the design-synthesis-analysis performed for this example is only $ .81, a negligible amount when compared to hours and perhaps days of engineering time that otherwise may be required to accomplish the same.

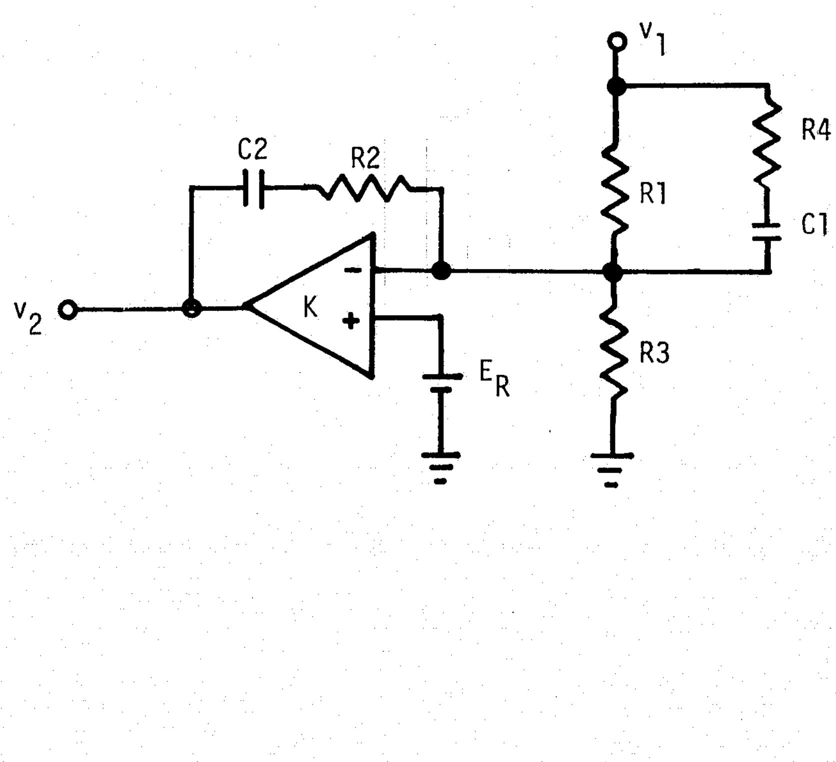


Figure 28 A Commonly-Used Lead-Lag Network

```
/ GET,CDS1
/ RUNX,I=CDS1
/ LGO
 ENTER"STOP" TO DISCONTINUE CDS, OTHERWISE "NO"
? N
 DO YOU WANT TO CHANGE"PARAM"?(Y OR N)
? Y
 THE "PARAM" VALUES WERE:
 $PARAM
 EIMIN    = 2.5E+01,
 EIMAX    = 5.0E+01,
 ED       = 2.0E+01,
 PD       = 6.0E+01,
 REG      = 1.0E-03,
 L        = 1.0E-03,
 C        = 4.55E-04,
 RS       = 6.8E-02,
 FS       = 2.0E+04,
 FX       = 2.0E+03,
 THETX    = 4.0E+01,
 $END
  $PARAM
? L=1.E-3,,$
 DO YOU WANT DESIGN ANALYSIS?(Y OR N)
? Y
 TRANSFER FUNCTION OF COMPENSATION NETWORK
 K= 66
 F1= 8.944230139E-01   F2= 2.286042696E+01   F3= 1.273162526E+03
3.141782702E+03
 DESIGN SYNTHESIS OF COMP. NETWORK
 R1= 4.181E+03   R2= 1.079649358E+04   R3= 3.090304348E+05   R4=
 2.848675502E+03
 C1= 1.778283506E-09   C2= 6.448416143E-07
 MINIMUM OP.AMP.GAIN= 1.147826087E+02
 DO YOU WANT BODE ANALYSIS?(Y,N)
? Y
```

```
 DO YOU WANT TO CHANGE FREQUENCY RANGE?(Y,N)
? Y
 ENTER INITIAL VALUE(THETA0)
? 0.
 ENTER INCREMENTAL VALUE(DELTHET)
? 5.
 ENTER FINAL VALUE(THETAF)
? 180.
  THETA   FREQ (HZ)    DBEL     MAG          PHASE
   5.00  2.7778E+02   36.61  6.7663E+01     49.28
  10.00  5.5556E+02   18.54  8.4524E+00     26.56
  15.00  8.3333E+02   11.26  3.6558E+00     31.24
  20.00  1.1111E+03    6.73  2.1693E+00     36.22
  25.00  1.3889E+03    3.49  1.4942E+00     40.41
  30.00  1.6667E+03     .99  1.1206E+00     43.80
  35.00  1.9444E+03   -1.04  8.8706E-01     46.57
  40.00  2.2222E+03   -2.75  7.2849E-01     48.86
  45.00  2.5000E+03   -4.23  6.1442E-01     50.82
  50.00  2.7778E+03   -5.53  5.2879E-01     52.52
  55.00  3.0556E+03   -6.70  4.6241E-01     54.03
  60.00  3.3333E+03   -7.75  4.0963E-01     55.41
  65.00  3.6111E+03   -8.71  3.6682E-01     56.67
  70.00  3.8889E+03   -9.59  3.3150E-01     57.84
  75.00  4.1667E+03  -10.40  3.0195E-01     58.94
  80.00  4.4444E+03  -11.15  2.7693E-01     59.98
  85.00  4.7222E+03  -11.85  2.5551E-01     60.96
  90.00  5.0000E+03  -12.50  2.3701E-01     61.88
  95.00  5.2778E+03  -13.12  2.2090E-01     62.76
 100.00  5.5556E+03  -13.69  2.0676E-01     63.60
 105.00  5.8333E+03  -14.23  1.9427E-01     64.40
 110.00  6.1111E+03  -14.74  1.8316E-01     65.15
 115.00  6.3889E+03  -15.23  1.7322E-01     65.88
 120.00  6.6667E+03  -15.69  1.6430E-01     66.56
 125.00  6.9444E+03  -16.12  1.5623E-01     67.22
 130.00  7.2222E+03  -16.54  1.4892E-01     67.85
 135.00  7.5000E+03  -16.94  1.4226E-01     68.45
 140.00  7.7778E+03  -17.32  1.3616E-01     69.02
 145.00  8.0556E+03  -17.68  1.3057E-01     69.56
 150.00  8.3333E+03  -18.03  1.2543E-01     70.09
 155.00  8.6111E+03  -18.37  1.2067E-01     70.59
 160.00  8.8889E+03  -18.69  1.1627E-01     71.06
 165.00  9.1667E+03  -19.00  1.1219E-01     71.52
 170.00  9.4444E+03  -19.30  1.0837E-01     71.96
 175.00  9.7222E+03  -19.59  1.0482E-01     72.38
 180.00  1.0000E+04  -19.87  1.0149E-01     72.78
 ENTER"STOP" TO DISCONTINUE CDS, OTHERWISE "NO"
? STOP
/ COST
LTIM      3.000 MIN.          .50
CPU       1.837 SEC.          .07
MUCM       .068 MW-S.         .09
DISK      5.246 KPRU.         .15
TOTAL                         .81
```

Figure 29   A Sample Printout of Control Design Subprogram.

5.4 CONTROL DESIGN FOR A MULTIPLE-LOOP ANALOG SIGNAL PROCESSOR

In this example, a particular multiple-loop analog-signal processor feature concerning the adaptive compensation of the output-filter change is examined. The most often used frequency-domain representation is through Bode plot of the open-loop transfer function. In a conventional single-loop system, the transfer function is the same regardless of the location at which an analyst chooses to mentally or physically open the loop. This freedom no longer holds for a multiple-loop controlled system. Opening the loop at different locations generally calls for different interpretation of analytical results. It is entirely possible for a multiple-loop design to exhibit essentially a -6db/octave slope when the open-loop transfer function is analyzed at a certain location, while concurrently the transfer function viewing from another location would suggest a highly-oscillatory system. In a multiple-loop design, one must therefore be careful in the selection and the interpretation of the loop opening.

5.4.1 A Multiple-Loop Controlled Buck Regulator

The buck regulator was shown in Figure 8. Input voltage E_i, power switch Q, diode D, inductor L with winding resistance R_L, capacitor C with an equivalent series resistance R_C, and load R_0, constitute the basic buck regulator. For clarity, no input filter is included in the power stage. The reason for choosing the buck regulator is also for clarity. Since the primary objective here is to identify the adaptive compensation of the analog-signal processor, the buck regulator serves the purpose with the least analytical complication, as its equivalent output filter is known to be independent of the operating duty cycle.

5.4.2 A Multiple-Loop Controlled Buck Regulator Block Diagram

From the small-signal viewpoint, the power processor shown in Figure 8 can be separated into three parts shown in Figure 30A, B, and C. Starting at point A of Figure 8 and tracing clockwise, the output filter and load is illustrated in Figure 30A. Voltages e_1 and e_2 represent the filter output voltage and the inductor voltage respectively, which are source signals for loop I and II. These two voltages are applied to the integrator amplifier as depicted in Figure 28B, resulting in an integrator-amplifier output voltage e_B. A sinusoidal voltage perturbation of unity peak amplitude at point B will cause a corresponding pulse train at point A, with identical pluse amplitude E_i and on-time T_n, but with varying intervals for off-time T_f. The pulse train contains a fundamental component with peak amplitude K_p and with a frequency identical to that of the sinusoidal perturbation. The factor K_p is defined as the gain from B to A clockwise. The graphical representation of the aforedescribed mechanism is shown in Figure 30C.

In Figure 30A, it can be shown that,

$$F_1(s) = \frac{e_1}{e_A} = \frac{\left(\frac{R}{R+R_L}\right)(1+SR_cC)}{1+S\left(\frac{R}{R+R_L}\right)\left[\left(R_L+R_c+\frac{R_LR_c}{R}\right)C+\frac{L}{R}\right]+S^2LC\left(\frac{R+R_c}{R+R_L}\right)} \tag{142}$$

$$F_2(s) = \frac{e_2}{e_A} = \frac{SNL\,[1+SC\,(R+R_c)]}{(R_L+R)\left\{1+\frac{SR}{R+R_L}\left[\left(R_L+R_c+\frac{R_LR_c}{R}\right)C+\frac{L}{R}\right]+S^2LC\left(\frac{R+R_c}{R+R_L}\right)\right\}} \tag{143}$$

In Figure 30B, output e_B of the integrator is related to e_1 and e_2 by:

$$\frac{ge_1-e_g-e_r}{R_3} + SC_1\,(e_B-e_g-e_r) + \frac{e_1-e_g-e_r}{R_5+\frac{1}{SC_2}} + \frac{e_2-e_g-e_r}{R_4} = 0 \tag{144}$$

Also, e_B is related to e_g by amplifier gain K,

$$-Ke_g = e_B \tag{145}$$

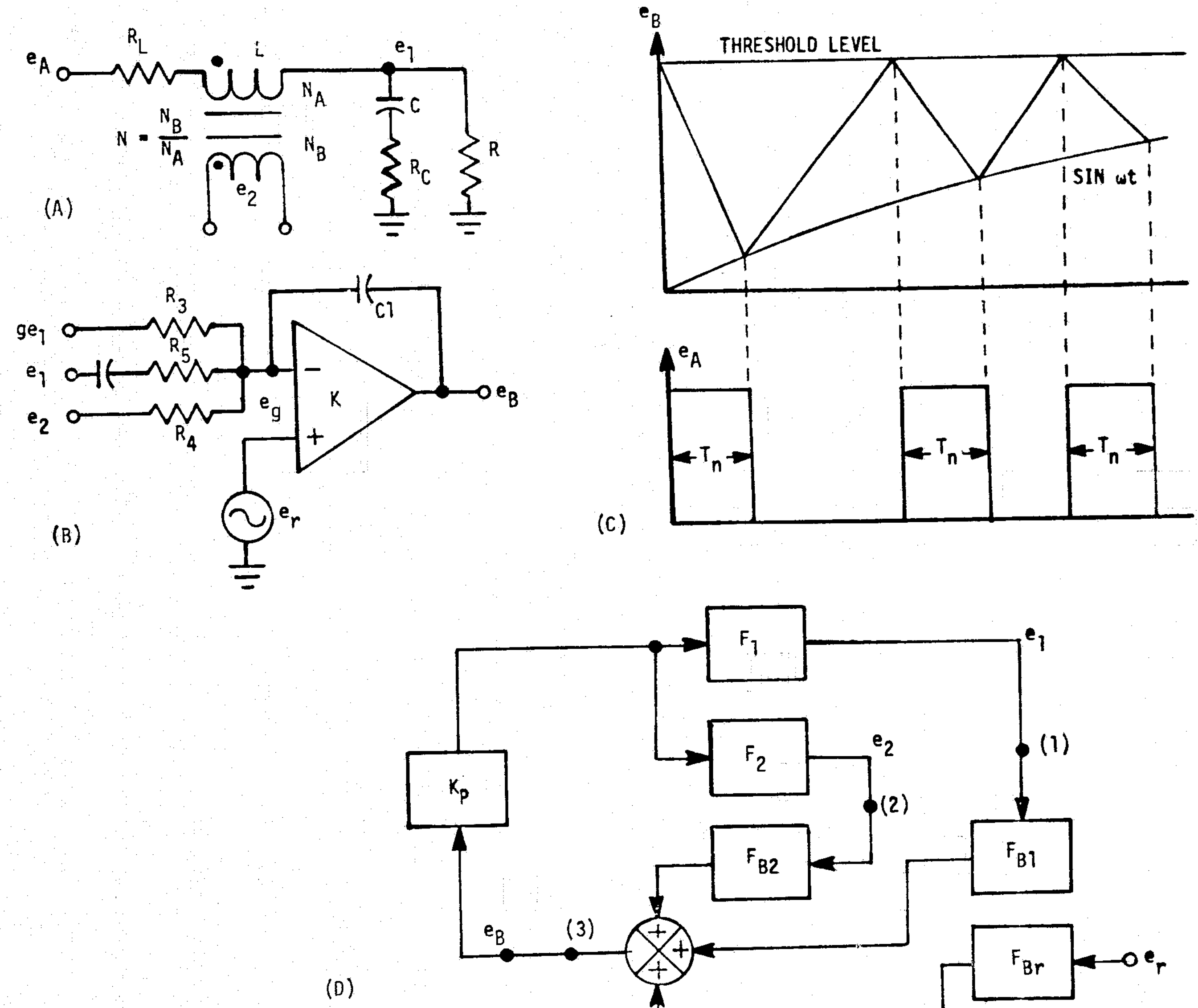


Figure 30   Small-Signal Equivalent Circuit for a Multiple-Loop Buck Regulator

Combining (144) and (145) to eliminate e_g, one has

$$e_1 \left(\frac{SC_2}{1+SC_2R_5} + \frac{g}{R_3}\right) + \frac{e_2}{R_4} - e_R\left(\frac{1}{R_3} + SC_1 + \frac{SC_2}{1+SC_2R_5} + \frac{1}{R_4}\right)$$

$$= - \; e_B \left[\frac{1}{KR_3} + SC_1 + \frac{SC_1}{K} + \frac{SC_2}{K(1+SC_2R_3)} + \frac{1}{KR_4}\right] \tag{146}$$

Let F_{Br}, F_{B1}, and F_{B2} to represent $\partial e_B/\partial e_r$, $\partial e_B/\partial e_1$, and $\partial e_B/\partial e_2$, respectively,

$$F_{Br} = \frac{\frac{1}{R_3} + SC_1 + \frac{SC_2}{1+SC_2R_5} + \frac{1}{R_4}}{\frac{1}{K}\left(\frac{SC_2}{1+SC_2R_5} + \frac{1}{R_3} + \frac{1}{R_4} + SC_1\right) + SC_1} \tag{147}$$

$$F_{B1} = - \frac{\frac{SC_2}{1+SC_2R_5} + \frac{g}{R_3}}{\frac{1}{K}\left(\frac{SC_2}{1+SC_2R_5} + \frac{1}{R_3} + \frac{1}{R_4} + SC_1\right) + SC_1} \tag{148}$$

$$F_{B2} = - \frac{\frac{1}{R_4}}{\frac{1}{K}\left(\frac{SC_2}{1+SC_2R_5} + \frac{1}{R_3} + \frac{1}{R_4} + SC_1\right) + SC_1} \tag{149}$$

Having identified the contribution of e_1, e_2, and e_r to e_B, the power processor control can be represented by the block diagram shown in Figure 28D. The five frequency-dependent blocks F_1, F_2, F_{B1}, F_{B2}, and F_{Br}, are expressed in (142), (143), (147), (148), and (149). The block K_p relates the integrator output to the voltage pulse train at the input of output filter, i.e., the pulses across free-wheeling diode D in Figure 30. The content of K_p will be analyzed in Appendix K.

Reference [11] identified point (3) in Fig. 30D as the proper breaking point for stability study, then, upon making the following reasonable assumptions

$$K >> 1$$

$$(1 + K)\, C_1 >> C_2$$

$$R >> R_L$$

$$R >> R_c$$

and substituting (142), (143), (148), and (149) into (147), one obtains:

$$\frac{de_B}{de_A} = \frac{\left(\frac{-KgR_4}{R_3+R_4}\right)\left\{(1+SR_cC)[1+SC_2(R_5+\frac{R_3}{g})] + S(1+SCR)(1+SC_2R_5)\,\frac{NR_3L}{gR_4R}\right\}}{\left\{1+S[(R_L+R_c)C + \frac{L}{R}] + S^2LC\right\}(1+SC_2R_5)(1+S\,\frac{KC_1R_3R_4}{R_3+R_4})} \tag{150}$$

Equation (150) can reveal the autocompensation of the LC parameters if for the time being one regards C_2 as negligibly small. Then, equation (150) is reduced to:

$$\frac{de_B}{de_A} = \frac{-\frac{KgR_4}{R_3+R_4}\left\{1 + S(R_cC + \frac{NR_3L}{gR_4R}) + S^2\,\frac{NR_3LC}{gR_4}\right\}}{\left\{1 + S[(R_c+R_L)\,C + \frac{L}{R}] + S^2LC\right\}(1 + S\,\frac{KC_1R_3R_4}{R_3+R_4})} \tag{151}$$

One can note from equation (151) that if the factor (NR_3/gR_4) is designed so that

$$\frac{NR_3}{gR_4} = 1, \tag{152}$$

then, equation (151) is further simplified to

$$\frac{de_B}{de_A} = \frac{-\frac{KgR_4}{R_3+R_4}\,[\,1 + S\,(R_cC + \frac{L}{R}) + S^2LC\,]}{(1+S\,\frac{KC_1R_3R_4}{R_3+R_4})\left\{1 + S\,[(R_c+R_L)\,C + \frac{L}{R}\,] + S^2LC\right\}} \tag{153}$$

From equation (153), the adaptive compensation of LC becomes clear, as both the numerator and denominator contain the S^2LC term. Both L and C can therefore vary extensively without materially effecting the open-loop transfer function. Consequently, in most designs where a unity (NR_3/GR_4) is observed, the (de_B/de_A) from A to B clockwise consists ideally a gain of $KGR_4/(R_3+R_4)$ and a first-order corner frequency $(R_3+R_4)/2\pi KC,R_3R_4$.

It is also noted that equation (153) only represents the transfer function from point A clockwise to point B. To complete the loop, the characteristics K_p from B clockwise to A must be derived.

The discussion thus comples the stability aspect of the particular multiple-loop control with emphasis on the adaptive compensation of the output-filter parameters. The contribution of the additional ac loop is apparent from equation (151), if one diminishes its effect by letting N approach zero.

It is also noted that equation (153) is based on an assumption of a negligibly small C2 in equation (150). In reality, C2 is not negligibly small, and it tends to detract somewhat the control from achieving the intended adaptive compensation. For a more detailed discussion, the reader is referred to reference [11].

As previously stated, this multiple-loop concept and its design, analysis, and application are currently the subjects of another NASA program, NAS3-20102. This example, therefore, only attempts to show one particular aspect of its control-related design. Upon completing NAS3-20102, the results obtained therein will be incorporated into the MAPPS as Control Design Subprogram for the multiple-loop control.

5.5 FUTURE EMPHASES

Future emphases on the Control Design Subprograms are expected to include the following:

- To treat all three basic power stages including the input filter, and to integrate the given power stage and digital signal processor with certain commonly-used single-loop analog-signal processor implementations, an example of which was given in Section 5.3.

- To include other small-signal control-dependent performance requirements such as sudiosusceptibility.

- To incorporate the work performed under NAS3-20102 for the aforementioned multiple-loop control into the MAPPS system.

6. DESIGN OPTIMIZATION SUBPROGRAMS

The design of a regulator converter generally involves four ingredients, shown in Figure 31(A). First, a set of performance requirements, $r=(r_1 \ldots r_n)$, is given to guide the design. Second, there are design constants, $k=(k_1 \ldots k_h)$, which are known to a designer either through manufacturer specifications, common sense, or designer's own experience. The objective of the design is to identify numerically all the design variables $x=(x_1 \ldots x_n)$, which are the unknowns prior to the initiation of the design. Performance requirements, design constants, and design variables, are related together through design constraints $g_j(x,k,r)=0$. The constraints include analytical and/or empirical relations that must be satisfied compositely by the other three aforementioned ingredients.

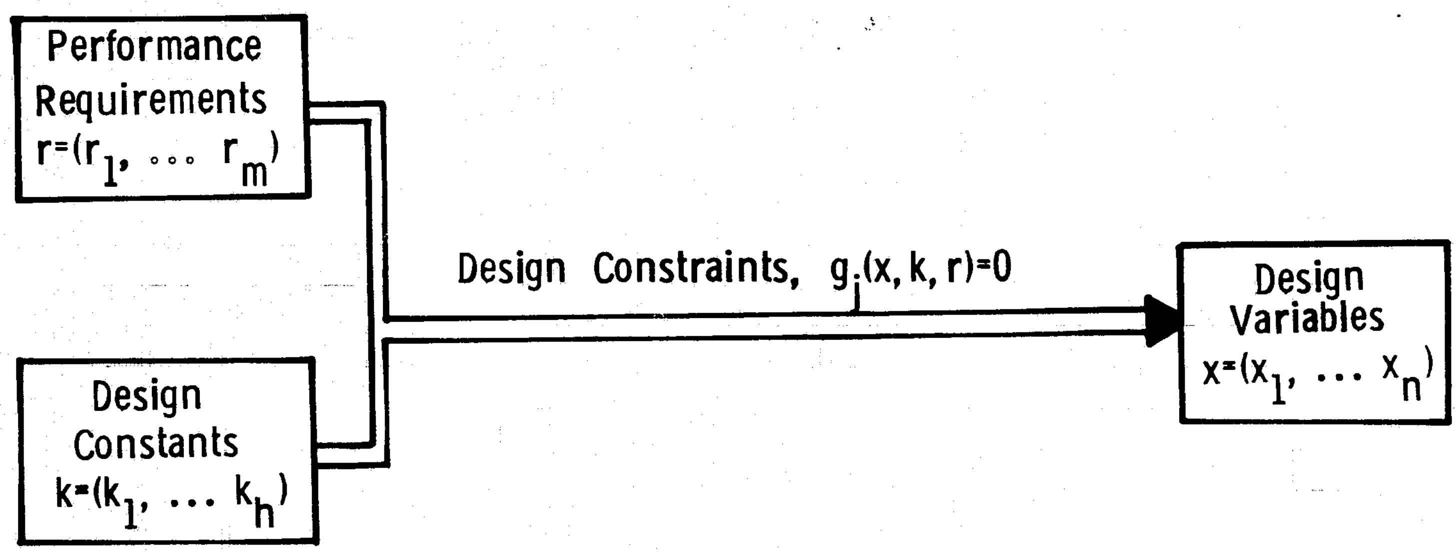
A common characteristic of the regulator-converter design is that the number of design variables $(x_1 \ldots x_n)$ exceeds that of the constraints $g_j(x,k,r)=0$. Consequently, there exists infinite sets of $x_1 \ldots x_n)$ to satisfy $g_j=0$, due to the inequality $n>j$. The fact that there usually exists multiple regulator-converter design alternatives all satisfying the same set of performance requirements only serves to underscore the projection of such in inequality.

Design optimization is illustrated in Figure 31(B). Comparing with Figure 31(A), an optimization criterion as a function of design variable x's and design constants k's is added to the entire design process. The essence of the design optimization, therefore, is to pinpoint a set of design variables to meet all constraints $g_j=0$ and requirements r, and concurrently, optimizes a certain converter characteristic, $f(x,k)$, deemed particularly desirable. The characteristic can be the converter weight, loss, or any other physically realizable entity associated with a converter.

In this section, a general design optimization methodology is outlined, and a practical design optimization approach is adopted. The approach is implemented through techniques involving the Lagrange Multipliers and the Nonlinear Programming, each supplemented by practical optimization applications. Improvements needed to further the course of design optimization are also related.

6.1 STATE-OF-THE-ART DESIGN APPROACH

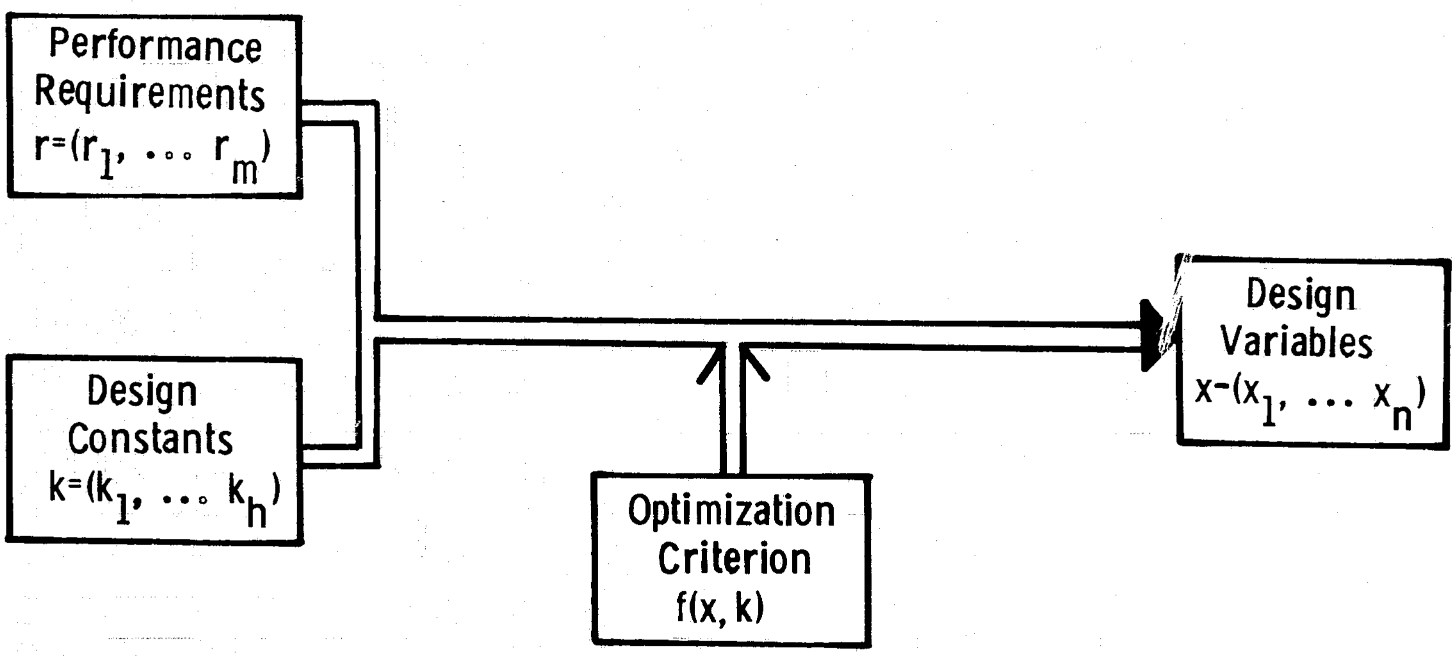
Before venturing into more detailed design optimization aspects it is perhaps worthwhile to review the satate-of-the-art in power converter design. It contains the following major sequences:



$\therefore\ n > j.$

$\therefore$ Infinite sets of $(x_1, \ldots x_n)$ to satisfy $g_j=0$

Figure 31(A) Design Ingredients



Design Optimization Objective: To pinpoint the single set of $(x_1 \ldots x_n)$ that satisfies $g_j=0$, and optimizes $f(x, k)$.

Figure 31(B) Design Optimization Ingredients

1) The designer obtains all specified converter requirements prescribed by someone presumably knowledgeable. Based on the nature of these requirements, the the designer selects a basic power-circuit configuration.

   Buck
   Boost
   Buck Boost
   Serie, Inverter
   Parallel Inverter, etc.

2) The designer's previous experience and occasionally a given specified performance requirement are called upon to elect from the control-circuit configurations that include:

   Constant frequency, variable on/off time
   Constant on time, variable off time
   Constant off time, variable on time
   Constant hysteresis, bang-bang control
   Variable frequency, variable on/off time

3) The designer then starts the power-circuit design by empirically or intuitively picking a power-converter switching frequency. Along with the power-dependent performance requirements listed in Section 1, the designer proceeds to obtain semi-conductor choices, input/output filter parameters, and design details of transformer and inductors. Based on a designer's often-profusely-arbitrary subjective judgement, crude weight-loss analysis is made, with occasional feeble attempt for piecemeal weight on loss optimization. The same process is repeated for different switching frequencies before completing a preliminary power circuit design. Despite the time-consuming iterations, optimization of the overall power circuit is seldom achieved.

4) Due to non-linearities in the power stage and in the digital signal processor, the design of the control circuit for a given power circuit to meet the control-dependent performance requirements is presently beyond the capability of the majority of the converter designers. Compliance with requirements is usually achieved by "bench design" of breadboard-component parameters, and assured through elaborate testing.

Against this background, one major thrust of this MAPPS program is in the area of control-related modeling, analysis and design, as has been presented in sections 4 and 5.

Undoubtedly, these efforts will be advanced in the future to form the basis of analytically-based design guidelines which, when complemented with standardization of control-dircuit configurations, will culminate in a complete control-circuit design meeting all performance requirements. For the time being, however, the preponderant regulator-converter designs are by no means analytically based.

6.2 A GENERAL DESIGN OPTIMIZATION METHODOLOGY

Simply stated, the design optimization task is to minimize and objective function $f(x,k)$, subjected to design constraints $g_j(x,k,r) = 0$.

Here, $x = (x_1, x_2, \ldots x_n)^T$ is a n-dimensional vector representing power and control circuit parameters to be designed. Examples of x are values of R, L, and C, the switching frequency, and the design details of magnetic components including core area, mean core length, permeability, wire size, number of turns, and turns ratio of multiple-winding magnetics.

The k's represent various constants related to component characteristics. Examples include winding and core densities, winding resistivity, window fill factor of the core, winding pitch factor (i.e., the ratio of the mean length of one-turn winding to the core circumference), transistor and diode conduction and switching characteristics, core-loss parameters, intended maximum operating flux density of given magnetics, and ESR as well as energy-storage characteristics of filter capacitors.

The r's are performance requirements to be met by the optimum design. Power-dependent requirements include input/output voltages, output power, maximum weight, minimum efficiency, source EMI, and maximum output ripple. Control-dependent requirements include regulator stability, minimum audio-susceptibility rejection, and maximum output impedance.

The function $f(x,k)$ represents the converter optimization criterion. Examples include the total weight, the total loss, the figure of merit of a specific design, a particular control-oriented performance, or any selected design quantity such as reliability and cost. The criterion generally can be expressed as a function of the x's and the k's.

Equations $g_j(x,k,r) = 0$ represent a total of "j" constraints. Examples of these equations include the relationship of an efficiency requirement to the sum of copper loss, core loss, semiconductor conduction and switching losses, and the loss in the capacitor ESR, the relationship of source EMI to the input-filter design parameters, the switching frequency, and the input/output voltage and current levels.

Equations $g_j = 0$ allow all performance requirements "r" and all component constants "k" to be integrated into governing the design of all variables "x". Consequently, solutions acquired for equations $g_j = 0$ to minimize the objective function f(x,k) would represent a detailed optimum design, down to the component level, in accordance with the performance requirements and the optimization criterion specified.

Thus, a general design optimization methodology is to analytically portray $g_j = 0$ for all control-dependent and power-dependent performance requirements. In conjunction with the defined optimization criterion f(x,k), computer techniques are then applied to seek out the x's that would satisfy $g_j = 0$ and concurrently minimize f(x,k).

Comparing this methodology to the present state-of-the-art design, the following notes can be made:

1) Both tasks start by obtaining requirements and selecting basic power- and control circuit configurations.

2) The switching frequency, which is fundamental to the power-circuit design, is selected in the general optimization methodology consistent with the optimization criterion. Unlike the state-of-the-art piecemeal design, the methodology acquires all design variables, including those prescribing detailed magnetics design, in an inclusive manner. Interdependences between various variables in different converter functions (e.g., input filter and output filter) are thus inherently preserved.

3) The methodology would eliminate the need for excessive "bench design" of control-circuit variables. It will also reduce the role of converter testing to that of verification only, rather than its current role of being the major vehicle through which compatibility between converter requirements and capabilities can be demonstrated.

6.3 A PRACTICAL DESIGN OPTIMIZATION APPROACH

While the aforedescribed general methodology represents the ultimate in converter design, its actual implementation is presently not without major difficulties. To begin with, it is realized that the well-developed computer linear programming techniques are inapplicable to converter optimization due to the nonlinear nature of the converter problems involved. As a result, the key to a successful design optimization of a complicated converter is to secure a nonlinear programming algorithm that enables optimum numerical solutions to be reached, with fast convergence, from an initial guess of the solutions.

Since the effectiveness of any nonlinear programming technique is invariably affected by the global and local properties of the multi-dimensional design problem, the unfortunate consequence is that there is no uniformly good method on which an algorithm can be based to handle optimization problems as complicated as those involved with the design of a complete regulator-converter. Naturally, the likelihood of securing an applicable nonlinear programming routine improves as the number, the non-linearity, and the complexity of the nonlinear constraints diminish.

Some of the most nonlinear and complex constraints are those describing the control-dependent performance requirements. Stability, audiosusceptibility, and output-impedance characteristics involve all power- and control-circuit RLC parameters as well as the converter switching frequency. Furthermore, the characteristics themselves are frequency dependent via s-transform or z-transform, thus compounding the complexity of the control-dependent performance design constraints. Based on experiences gained to date on the application of various nonlinear programming routines, the chance for a successful inclusion of all control-dependent performance constraints in an overall power-converter design optimization is extremely slim in the foreseeable future.

To realize a practical approach within the demonstrated capability of non-linear programming, one is, for the time being, forced to forsake the control-circuits, and to concentrate instead on the design optimization of the converter power circuit. The scope of the optimization criteria is reduced to include only those related to power-dependent performance characteristics, such as weight and losses.

Admittedly, the practical approach is less meritorious in relation to the general methodology. However, its utility is still significant for the following reasons:

- The prevailing trend toward converters designed for higher power places increasing emphasis on loss and weight optimizations.
- Sensitivity to program cost and space/military equipment standardization encourages analysis-based designs to reduce weight, loss, and cost penalties resulting from suboptimum designs and developments.
- For a given power- and control-circuit configuration, converter design experience has indicated that, once the power-circuit parameters are properly designed, generally it is possible to design compatible converter control-circuit parameters to meet stability and other control-dependent performance requirements.

Thus, while the inclusion of control-dependent constraints in an overall converter design optimization represents an increase in the optimization effort, it is not likely to alter the weight-loss optimization results obtained from considering power-circuit related constraints alone. The results obtained from power-circuit optimization are, therefore, both practical and meaningful.

- Comparing to the number of control-circuit configurations proposed and in use to date, there are relatively few commonly-used power-circuit configurations. The utility of the power circuit design optimization is thus widespread and well-defined.

Consequently, given the limited nonlinear-programming capability currently demonstrable, a practical and useful design optimization approach can be formulated, which consists of the following two major steps:

1) Design the power-circuit parameters to achieve the weight-loss optimization of a given power circuit configuration that will meet all power-dependent performance requirements.
2) Based on the power circuit parameters thus obtained, guidelines to design detailed control-circuit parameters to meet specified control-dependent performance requirements are then used to fulfill the design of a complete power converter. This step does not involve the use of a nonlinear programming routine. Design guidelines for control-circuit parameters will be conceived analytically based on the Control Design Subprogram currently in progress, and should become practical in the near future.

At present, the generation of design guidelines mentioned in step (2) appears to be the likely major thrust of near-term power-converter modeling and analysis. Undoubtedly, many significant contributions are forthcoming from industry/university/government research effort, both here and abroad. The emphasis of the design optimization here is placed on step (1). It is hoped that the work reported here will provide the needed complement for results emerging from the step (2) effort. Together they are expected to shape the standardized power-converter design approach in the foreseeable future.

In the following sections, the methodology implementation of the step (1) design optimization is discussed.

6.4 IMPLEMENTATION OF DESIGN OPTIMIZATION

Continued rapid growth by applied optimization as a scientific discipline has been fostered by the application of optimization theory and the high-speed computer developments. In power converter design, it follows naturally that the key in implementing the design optimization rests on the availability of suitable mathematical and computer techniques.

6.4.1 A General Mathematical Approach Based on Lagrange Multiples

Quite amenable to generalization, optimization theory in terms of Lagrange Multipliers [12] provides a practical method in seeking an extremum for the objective function f(x, k), subjecting to a total of "j" constraints.

$$g_j\ (x,k,r) = 0,\ x = (x_1,x_2\ ---\ x_n)^T \tag{154}$$

The method forms a function F, where

$$F = f + \sum h_j g_j \tag{155}$$

Here, the h_j's are Lagrange Multipliers independent of x's. For "F" to have an extremum, the requirement is

$$\frac{\partial F}{\partial X_i} = 0,\ i = 1,2,---n \tag{156}$$

From $g_j = 0$ and $\partial F/\partial X_i = 0$, a total of (j+n) equations are available to solve n variables and "j" Lagrange Multipliers. Applications of this method to simple converter optimization problems occasionally yield analytical optimum solutions [15]. However, when the problem transcends the simple component level, the method becomes impractical in yielding the optimum design in closed form.

6.4.2 Nonlinear Programming Techniques

Most larger problems arising from practical power converter applications are sufficiently complicated to defy closed-form solutions. To identify numerically an optimum design, one has to resort to nonlinear programming algorithms to provide fast convergence to opimum solutions from a reasonable set of input parameters. From the numerous existing methods of nonlinear programming, two popular ones were selected to test their utilities in power converter optimization: the method of reduced gredient [14], and the method of penalty functions [13]. The particular codes used to implement these two approaches are, respectively, the Generalized Reduced Gredient (GRE) and the Sequential Unconstrained Minimization Technique (SUMT) [13,29]. The effectiveness of each code depends greatly on the global and local properties of the particular multi-dimensional problem to which the method is applied. The dependency makes it difficult to compare objectively the general merits of different algorithms. Based solely on our application experience to date, both codes handle simple-to-moderately-simple optimization problems equally well. However, the SUMT code seems to have been most effective in achieving convergence for complex and highly nonlinear converter optimization problems.

At this juncture, a note is in order to clarify the meaning of the penalty function. A penalty function is one, which, when added to the original objective function f(x,k) to form a penalized objective function $f_p(x,k)$, will detract from achieving a minimum objective when an associated constraint within $g_j(x,k,r)=0$ is not satisfied. The particular penalty function used in the SUMT code is the quadratic for of g_j, which gives:

$$f_p = f + c \sum_{1}^{j} [g_j]^2 \qquad (157)$$

Here, c is the weighting coefficient when a minimum of f_p is desired. It is apparent from this equation that the constrained minimum of f(x,k) subjected to constraints $g_j=0$ is identical to the unconstrained minimum of $f_p(x,k)$ when 'c' approaches infinity. The SUMT code thus accomodates the initial "c", the conditions under which "c" is to be increased, and the criterion of bypassing the increasing "c" when the intended minimization has run its course.

6.5 APPLICATION EXAMPLES BASED ON THE METHOD OF LAGRANGE MULTIPLIERS

6.5.1 Inductor Design Optimization

In this example, a simple inductor design optimization is used to illustrate the application of the Lagrange Multipliers. Quite often in actual inductor design, the designer wishes to identify a core to achieve a certain inductance and to accomodate all windings for which the conductor size of each turn has been predetermined empirically or intuitively on a circular-mil-per ampere basis. In this case, one is not interested in an optimum design strictly from an overall weight-loss viewpoint. All that is wanted is the selection of a core that is just right; it is neither too small to accomodate physically all the windings nor is it too large to cause an excessive surplus in its electromagnetic capability in relation to that demanded by the specific inductor application.

In this example, the following design parameters are needed:

Known Constants "k"

- A_c: Predetermined cross-sectional area of one-turn conductor
- B_s: Saturation flux density of the core
- D_c: Conductor Density
- D_i: Iron core density
- F_c: Ratio of one-turn conductor average length to core circumference
- F_w: The proportion of core window actually occupied by the conductor when the window is filled.

Given Requirements "r"

- L: Inductance needed
- I_p: Peak current in the inductor winding

Unknown Variables "x"

- A: Core sectional area
- N: Number of turns
- Z: Mean length of core
- μ: Permeability of core

Constraint Equations "g_j"

Two constraints are used to formulate the design. First, all magnetic core flux capability is utilized:

$$B_S NA - LI_P = 0 \tag{158}$$

Next, all window area of the core is occupied:

$$(NA_c/\Pi F_N)^{1/2} - (Z/2\Pi) + (A^{1/2}/2) = 0 \tag{159}$$

In deriving (159), a core with a square sectional area A is assumed so that the circumference of the core becomes $4A^{0.5}$.

Objective Function "f(x,k)"

In this example, one wishes to minimize the inductor weight W, which can be expressed as:

$$W = f(x,k) = \text{conductor weight} + \text{core weight}$$
$$= 4F_c D_c A_c NA^{0.5} + D_i AZ \tag{160}$$

Having formulated the problem,it is recalled that the task here is to find solutions for the x's so that W of equation (160) is minimized, and concurrently equation (158) and (159) are satisfied.

Substituting x_1 for $A^{0.5}$, x_2 for $N^{0.5}$, and x_3 for Z, equations (146) to (148) become, respectively,

$$g_1(x,k,r) = B_s\, x_2^{\,2}\, x_1^{\,2} - LI_p = 0 \tag{161}$$

$$g_2(x,k,r) = (A_c/\Pi F_W)^{0.5} x_2 - (x_3/2\Pi) + (x_1/2) = 0 \tag{162}$$

$$f(x,k) = 4F_c D_c A_c x_2^{\,2} x_1 + D_i x_1^{\,2} x_3 \tag{163}$$

$$F = 4F_cD_cA_cX_2^2x_1 + D_ix_1^2x_3 - h_1(B_sx_2^2x_1^2 - LI_p)$$

$$-h_2[(A_c/\pi F_W)^{0.5}x_2 - (x_3/2\pi) + x_1/2] \tag{164}$$

$$\frac{\partial F}{\partial X_1} = 4F_cD_cA_cX_2^2 + 2D_iX_1X_3 - 2h_1B_sX_2^2X_1 - h_2/2 = 0 \tag{165}$$

$$\frac{\partial F}{\partial X_2} = 8F_cD_cA_cX_1X_2 - 2h_1B_sX_2X_1^2 - h_2(A_c/\pi F_W)^{05} = 0 \tag{166}$$

$$\frac{\partial F}{\partial X_3} = D_iX_1^2 + h_2/2\pi = 0 \tag{167}$$

From the five equations (161), (162), (165), (166), and (167), the five unknowns X_1 to X_3 and h_1 to h_2 can be solved. Solution of h_1 and h_2 are irrelevant to the inductor design. The relevant ones are:

$$A = X_1^2 = \left(\frac{1}{3}\right)\left(\frac{LI_pA_c}{B_s\pi F_W}\right)^{0.5} S \tag{168}$$

$$N = X_2^2 = 3\left(\frac{LI_p\pi F_W}{A_cB_s}\right)^{0.5} S^{-1} \tag{169}$$

$$Z = X_3 = (2\sqrt{3}\pi)\left(\frac{LI_pA_c}{B_s\pi F_W}\right)^{1/4}\left(S^{-1/2} + \frac{S^{1/2}}{6}\right) \tag{170}$$

where

$$S = \left(1 + \frac{RF_cF_WD_c}{D_i}\right)^{1/2} - 1 \tag{171}$$

From these equations, the permeability and the weight of the inductor can be derived as:

$$\mu = (2\pi/\sqrt{3})\left(\frac{B_s}{I_p}\right)^{-5/4}\left(\frac{A_c}{\pi F_W}\right)^{3/4} L^{-1/4} S\left(S^{-1/2} + \frac{S^{1/2}}{6}\right) \tag{172}$$

$$W = (2\pi D_c/\sqrt{3})\left(\frac{LI_pA_c}{\pi B_sF_W}\right)^{3/4} S^{-1/2}\left[6F_cF_W + \frac{D_i}{D_c}\left(S + \frac{S^2}{6}\right)\right] \tag{173}$$

Equations (168) to (172) illustrate the particular set of A, N, Z, and μ that will produce a minimum-weight inductor with inductance L, peak winding current I_p, conductor cross-sectional area A_c, saturation flux density B_s, winding factor F_W, pitch factor F_c, and densities D_c and D_i for the conductor and the core, respectively. In these equations, A is in square meter, Z is in meter, W is in kilograms, and μ is in Weber/Ampere-Turn-Meter. To converter the permeability into gauss/oersted, equation (172) is divided by a factor $4\pi x 10^{-7}$. Notice that if LI_p is being replaced by VS, the volt-second content of the core, then the aforedescribed equations are perfectly applicable to designing transformers using rectangular-loop core materials. When used that way, naturally eq. (172) for permeability is neither applicable nor needed for rectangular-BH-loop cores.

To demonstrate the utility of these equations, the following constants are assumed for the molypermalloy-powder-core inductor:

$$F_W = 0.4$$

$$F_c = 2.0$$

$$B_s = 0.35 \text{ Weber/meter}^2$$

$$D_c = 8900 \text{ kg/m}^3$$

$$D_i = 7800 \text{ kg/m}^3$$

Using these constants and making the conversions to the more familiar engineering units, then, with L expressed in microhenries, I_p in Amperes, and A_c in circular mils, eqs. (168) to (173) become:

$$A = 2.8\text{x}10^{-4} (LI_pA_c)^{1/2} \quad \text{cm}^2 \tag{174}$$

$$N = 103 (LI_p/A_c)^{1/2} \quad \text{turns} \tag{175}$$

$$Z = 0.18 (LI_pA_c)^{1/4} \quad \text{cm} \tag{176}$$

$$\mu = 6.1 I_p^{-5/4} L^{-1/4} A_c^{3/4} \quad \text{Gauss/Oersted} \tag{177}$$

$$W = 0.001 (LI_pA_c)^{3/4} \quad \text{grams} \tag{178}$$

Notice that once L, I_p, and A_c are known from requirements specified, the inductor weight is determined from eq. (178) without the need for actually designing the inductor.

6.5.2 Other Design Optimization Examples Using Lagrange Multipliers

Following similar procedures outlined in Section 5.5.1, for an inductor, closed-form optimum solutions were obtained for the following designs:

- Optimum-weight inductor or transformer, with the loss in the magnetics given as a constraint.
- Optimum-loss inductor or transformer, with the weight of the magnetics given as a constraint.

6.5.2.1 Optimum Weight Design for a Given Loss

This example deals with the design of an inductor to be used in an input filter carrying a direct current, and therefore incurring negligible iron losses. The allowed copper loss for the inductor is given as a constraint.

Known Constants "k"

P = Copper loss allowed

ρ = Conductor resistivity

B_s, D_c, D_i, F_c, and F_W are the same as the previous example.

Given Requirements "V"

I_p = Maximum direct current in the inductor winding

L = Inductance needed at I_p

Unknown Variables "X"

A_c = The conductor size is now unknown

A, N, Z, and μ are identical to the previous example.

Constraint Equations "g_j"

The copper loss of the inductor is:

$$P - (4I_{dc}^2 \rho F_c NA^{0.5}/A_c) = 0 \tag{179}$$

The other two constrains are identical to eqs. (158) and (159).

Objective Function "f(x,k)"

To optimize the weight, the weight equation is identical to eq. (160).

Based on these formulations, mathematical manipulations produce the following closed-form solutions:

$$A = 16\left(\frac{\rho\, D_c F_c^4}{B_s^2 \pi D_i}\right)^{2/5} \left(\frac{I_P^4\, L^2}{P}\right)^{2/5} S^{-4/5} \tag{180}$$

$$N = (1/16)\left(\frac{\pi^2\, D_i^{\,2}}{D_c^{\,2} B_s P^2\, F_c^8}\right)^{1/5} \left(\frac{L_P^{\,2}}{I_P^{\,3}}\right)^{1/5} S^{4/5} \tag{181}$$

$$Z = T\left(\frac{I_P^{\,4} L^2}{\rho}\right)^{1/5} \tag{182}$$

$$A_c = \left(\frac{\pi D_i F_c \rho^4}{D_c\, B_s^{\,3}}\right)^{1/5} \left(\frac{I_P^{\,11} L^3}{P^4}\right)^{1/5} \tag{183}$$

$$\mu = 16\left(\frac{D_c B_s^{\,3} \rho F_c^{\,4}}{\pi D_i}\right)^{2/5} \left(\frac{I_P^{\,2} L}{P^3}\right)^{1/5} S^{-4/5}\, T \tag{184}$$

$$W = \left[\left(\frac{\pi^2 D_i^{\,2} D_c^{\,3} \rho^3 F_c^{\,2}}{B_s^{\,6}}\right)^{1/5} S^{4/5} + 16\left(\frac{\rho F_c^{\,4} D_c D_i^{\,1/5}}{B_s^{\,2} \pi}\right)^{2/5} S^{-4/5}\, T\right] \left(\frac{L^6\, I_P^{\,12}}{P^3}\right)^{1/5} \tag{185}$$

where

$$S = \left(\frac{D_i F_c}{D_c F_N}\right)^{1/2} + \left(\frac{D_i F_c}{D_c F_W} + 96 F_c^{\,2}\right)^{1/2} \tag{186}$$

$$T = \frac{1}{2}\left(\frac{\pi^8 D_i^{\,3} \rho}{F_W^{\,5} D_c^{\,3} B_s^{\,4} F_c^{\,7}}\right)^{1/10} S^{3/5} + 4\left(\frac{\rho \pi^4 F_c^{\,4} D_c}{B_s^{\,2} D_i}\right)^{1/5} S^{-2/5} \tag{187}$$

Several significant characteristics exposed by these equations are:

(1) For a given core material, the minimum weight expressed in eq. (185) can be directly calculated from the given L, I_p, and loss limit P, without attending to the design details of the inductor. This feature should find great utility in parametric weight-loss trade-off analysis.

(2) Equation (185) prescribes one, and only one, optimum weight design for a given loss. Varying the conductor-to-core proportion in an alternate design would only result in a heavier inductor.

Again using powder core as an example, for which the following parameters are assigned:

$$B_s = 0.35 \quad W/m^2 , \qquad D_c = 8900 \text{ kg/m}^3$$

$$F_W = 0.42 , \qquad \rho = 1.724 \times 10^{-8} \text{ ohm-meter}$$

$$F_c = 1.9 , \qquad D_i = 7800 \text{ kg/m}^3$$

Substituting these parameters into (180) to (187), and making necessary engineering-unit conversions, one has:

$$A = 0.00076 \left(\frac{I_p^4 L^2}{P} \right)^{2/5} \quad \text{cm}^2 \tag{188}$$

$$N = 37.6 \left(\frac{LP^2}{I_p^3} \right)^{1/5} \quad \text{turns} \tag{189}$$

$$Z = 0.21 \left(\frac{I_p^4 L^2}{P} \right)^{1/5} \quad \text{cm} \tag{190}$$

$$Ac = 2.68 \left(\frac{I_p^{11} L^3}{P^4} \right)^{1/5} \quad \text{cir. mils} \tag{191}$$

$$\mu = 15.6 \left(\frac{I_p^2 L}{P^3} \right)^{1/5} \quad \text{gauss/oersted} \tag{192}$$

$$W = 0.0022 \left(\frac{I_p^{12} L^6}{P^3} \right)^{1/5} \quad \text{grams} \tag{193}$$

In these equations, I_p is in amperes, L is in microhenries, and P is in Watts.

6.5.2.2 Optimum-Weight Design for a Given Weight

In addition to the two constraints shown as eqs. (158) and (159) concerning the flux capability and the full window, a third constraint is the weight limit W, where

$$W - 4F_cD_cN\,A_c\,A^{1/2} - D_iAZ = 0 \tag{194}$$

The objective function to be optimized is the loss P,

$$P = 4I_p{}^2\rho\,F_cN\,A^{1/2} / A_c \tag{195}$$

Performing similar manipulations as the last example, the following closed-form solutions can be obtained:

$$A = W^{3/2}\,M^{-2} \tag{196}$$

$$N = (1/B_s)\left(\frac{LI_p}{W^{2/3}}\right)M^2 \tag{197}$$

$$A_c = \left(\frac{B_sF_W}{25D_i{}^2\pi}\right)(2M - 5\pi D_iM^{-2})^2\left(\frac{W^{4/3}}{LI_p}\right) \tag{198}$$

$$Z = (1/D_i)\left[M^2 - (S/40)(2M-5\pi D_iM^{-2})^2\right]W^{1/3} \tag{199}$$

$$\mu = \left(\frac{B_s{}^2}{D_i}\right)\left[1 - \left(\frac{S}{10}\right)\left(1 - \frac{16F_cD_cF_W}{D_iS}\right)^2\right]\frac{W}{I_p{}^2L} \tag{200}$$

$$P = \left(\frac{25\rho\pi F_cD_i{}^2}{B_s{}^2F_WM}\right)\left(\frac{1}{1 - \frac{16F_cD_cF_W}{D_iS}}\right)^2\left(\frac{L^2I_p{}^4}{W^{5/3}}\right) \tag{201}$$

where

$$M = \left(\frac{5\pi D_i{}^2S}{32F_cD_cF_W}\right)^{1/3} \tag{202}$$

$$S = 1 + \frac{16F_cF_WD_c}{D_i} \pm \left(1 + \frac{96F_cD_cF_W}{D_i}\right)^{1/2} \tag{203}$$

Notice the "$\pm$" sign in eq. (203). Only that which produces positive Z, P, and μ will be chosen. Again using the powder core for example with identical numerical values for B_s, F_W, F_c, D_c, D_i, and ρ specified for the previous example, one can obtain the following concise design equations:

$$A = 0.045 \quad W^{2/3} \quad \text{cm}^2 \tag{204}$$

$$N = 0.635 \left(\frac{LI_p}{W^{2/3}} \right) \quad \text{turns} \tag{205}$$

$$Z = 1.617 \quad W^{1/3} \quad \text{cm} \tag{206}$$

$$\mu = 7100 \left(\frac{W}{I_p^2 L} \right) \quad \text{gauss/oersted} \tag{207}$$

$$P = 4.12 \times 10^{-5} \left(\frac{L^2 I_p^4}{W^{5/3}} \right) \text{watts} \tag{208}$$

$$Ac = 8881 \left(\frac{W^{4/3}}{LI_p} \right) \quad \text{cir. mils} \tag{209}$$

Here, L is in microhenries, I_p is in amperes, and W is in grams. Notice that from eqs. (204) and (206) with D_i = 7.8 grams/cm^3,

$$D_i AZ = 0.57W \tag{210}$$

Thus, for an optimum-loss inductor, the core weight ($D_i AZ$) should be about 57 percent of the total inductor weight.

6.5.3. Design Optimization Subprograms Based on Closed-Form Solutions

While the examples given indeed provide the closed-form optimum design, calculations of core dimensions, conductor sizes, weight, etc. still are rather tiresome when different core and conductor materials are involved. Consequently, the three sets of general closed-form solutions for the three previous examples in terms of $D_c, D_i, F_c, F_w, \rho, B_s, I_p, L, P$, and W are implemented respectively into three user-oriented computer subprograms, completed with user instruction, input request, input summary printout, and the optimum design results.

For example, upon executing the subprogram concerning optimum weight inductor design for a given loss, the computer will print out the following user instructions:

```
[ RUNX,I=INDOS2,6
 THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN
 OPTIMUM WEIGHT INDUCTOR DESIGN FOR A GIVEN LOSS.
 TO USERS: PLEASE READ THE FOLLOWING STATEMENTS
    CAREFULLY BEFORE EXECUTING THE PROGRAM.
 THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:
    DC  : CONDUCTOR DENSITY IN GRAMS/CUBIC CM.
          IF NOT GIVEN BY THE USER, DC IS SET
          AT 8.9 BY DEFAULT.
    DI  : CORE DENSITY IN GRAMS/CUBIC CM.
          IF NOT GIVEN BY THE USER, DI IS SET
          AT 7.8 BY DEFAULT.
    FC  : RATIO OF AVERAGE ONE TURN LENGTH TO THE
          CORE CIRCUMFERENCE.
          IF NOT GIVEN,FC IS SET AT 2. BY DEFAULT.
    FW  : RATIO OF CONDUCTOR AREA TO WINDOW AREA.
          IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.
    RHO : CONDUCTOR RESISTIVITY IN OHM-METER. IF
          NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT.
    P   : DESIGNED POWER LOSS IN WATTS.
    BS  : MAXIMUM FLUX DENSITY IN KILOGAUSSES.
    IP  : PEAK INDUCTOR CURRENT IN AMPERES.
    L   : DESGNED INDUCTANCE IN MICROHENRIES.
 PLEASE GIVE INPUT DATA FOR L,IP,BS,AND P BELOW.
 PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,
    FC,FW,AND RHO IF ANY OF DEFAULTED SETTINGS IS
    NOT DESIRED.
 NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
 FOR ANSWERS AT THE END OF THE RUN,
 A IS CORE AREA, Z IS MEAN CORE LENGTH,
 N IS NUMBER OF TURNS, U IS PERMEABILITY,
 AZ IS PRODUCT OF A AND Z,AC IS CONDUCTOR AREA PER
 TURN,W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN P.
```

Subsequently, the computer requests input data from the user with regard to $D_c, D_i, F_c, F_w, \rho, P, B_s, I_p$, and L. For the first five parameters, the inherent values set by the subprogram are 8.9 g/cm^3, 7.8 g/cm^3, 2.0, 0.4, and 1.724×10^{-8} ohm-meter, respectively, representing the commonly-used copper density, core density, pitch factor, fill factor, and copper resistivity. These values can be supplanted by a user's own design numbers. However, if no user inputs with regard to these parameters are received, the subprogram will acknowledge user's default by utilizing the inherently-set values. The power loss P, peak current I_p, and the inductance L at I_p are, of course, individually assigned by the user for specific applications.

In this example, the user needs a 200-μH inductor carrying a peak current I_p of 4.5 amperes and utilizing a flux density B_s of 3.5 kilogauss (e.g., a powder core). The loss allowed by the user is 0.699 watts. For D_c, D_i, F_c, F_w, and ρ, the user defaults the input; those set inherently by the subprogram will be used. The user thus responds to the computer input request by typing the following:

```
 $B
? L=200.,IP=4.5,BS=3.5,P=0.6991$
```

Upon completing the input data, the computer will print a summary of assigned input parameters including the defaulted ones:

```
$B
DC        = 8.9,
DI        = 7.8,
FC        = 2.0,
FW        = 4.0E-01,
RHO       = 1.724E-08,
P         = 6.991E-01,
BS        = 3.5,
IP        = 4.5,
L         = 2.0E+02,
```

The optimum design values are then computed by the subprogram and delivered as outputs:

```
A = 6.939E-01      SQUARE CENTIMETERS
Z = 6.391E+00      CENTIMETERS
N = 3.661E+01      TURNS
U = 1.094E+02      GAUSS/OERSTED
AZ= 4.435E+00      CUBIC CENTIMETER
AC= 2.419E+03      CIRCULAR MIL
W = 6.085E+01      GRAMS
```

Based on the calculated A,Z,μ, and A_C, a compatible design using the commercially-available components is either core 55930 of Magnetics, Inc., or core A930157-2 of Arnold Engineering, with a wire size of #17 AWG. Such a design guarantees a loss limt around 0.7W as specified. From the printout, the total inductor core-and-winding weight is about 61 grams.

The cost for this design session is \$0.51. This compares favorably to hours of laborious and suboptimum design iterations needed by an experienced designer using the long-hand approach.

Similar subprograms are conceived for the other two examples previously described. Details regarding these user-oriented subprograms are shown in Appendix L, in which the computer input program and a sample run are included for each of the following design optimization:

INDOS 1: Optimum-weight inductor with wire size predetermined.
INDOS 2: Optimum-weight inductor with a given loss constraint.
INDOS 3: Optimum-loss inductor with a given weight constraint.

6.6 APPLICATION EXAMPLES BASED ON NONLINEAR PROGRAMMING TECHNIQUES

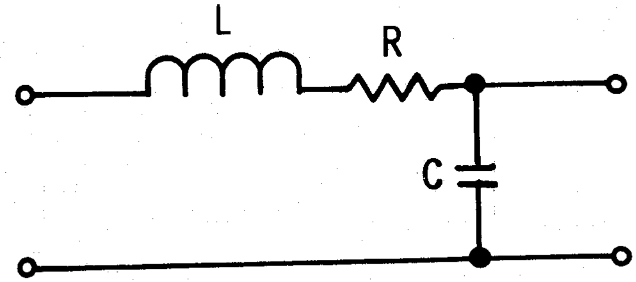
6.6.1 Input Filter Design Optimization

The optimum-weight designs for two different input-filter configurations are compared. A conventional LC filter is shown in Figure 32(A), where R is the winding resistance of L. Another configuration, shown in Figure 32(B), is a two-stage filter [30], in which R1 and R2 are winding resistances of L1 and L2, R3 is the lumped sum of ESR of C1 and a much higher external resistance added in series with C1, and C2 is a high-quality capacitor (e.g., polycarbonate type) with a negligible ESR. The advantage of the two-stage filter from a performance viewpoint is that while a high efficiency can be maintained as C2 handles most of the switching current, the resonant peaking of the entire filter is being controlled by the external resistance R3 in the first stage. The resistance incurs negligible losses, as negligible current flows in C1 during normal operations.

The known constraints, given requirements, unknown variables, constraint equations, and the objective function are formulated for both filters. Being a much more complicated problem, closed-form solutions for the two-stage filter are unattainable.

Parameters L1, L2, C1, R1, R2, and R3 along with the design of magnetics, are therefore numerically determined by invoking the SUMT nonlinear programming routine. Detailed formulations and significant numerical results can be found in Appendix M. One aspect worth noting here is the higher optimum weight of the two-stage filter in relation to its single-stage counterpart when they are designed to meet identical peaking, attenuation, and efficiency requirements. For given attenuation requirement, the weight difference will increase with a lower allowance on either the resonant peaking or the power loss.

(A)



(B)

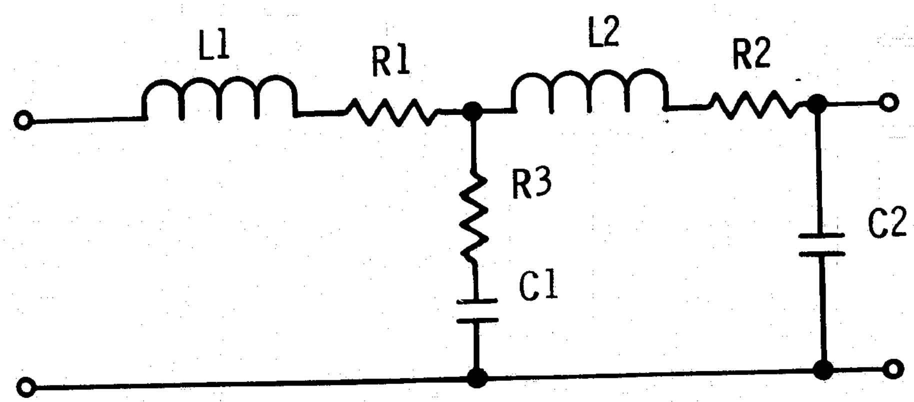


Figure 32 Single and Two-STage Input Filters

6.6.2 Design Optimization of a Complete Converter Power Circuit

This example deals with optimization on a vastly-expanded scale - an optimimum weight design for a complete buck converter power circuit shown in Figure 33, which includes a two-stage input filter. (See Appendix P).

Here, R1 to R3 are winding resistances of L1 to L3, respectively. The input filter is composed of L1-C1-R4-L2-C2, with L3-C3 being the output filter, and RC being the ESR of C3. Counting in addition the area A, turns N, length Z, and conductor area AC required to completely define each inductor, and including the switching frequency F, a total of twenty-three variables are involved. These variables, along with design constraints that include efficiency, source current ripple, output voltage ripple, input filter resonance, full utilization of inductor window areas, and no inductor saturation, are presented in Table 4. Most constraints are complicated nonlinear functions of the aforementioned variables; the most complicated one being equation (1) of Table 4, which includes copper losses, semiconductor conduction losses, capacitor dissipations, and frequency-dependent core losses and semiconductor switching lesses. The objective of the optimum design is to solve for all variables, with the intent to satisfy each constraint, and concurrently minimize the optimization criterion - the total weight of copper, iron, and the capacitors. Notice in particular the switching frequency is not a pre-set value; its optimum selection is an integral part of the total converter design.

The known constants, given requirements, unknown variables, constraint equations, and the objective function for these problems are presented next.

6.6.2.1 Known Constants

The following known constants are assumed:

F_{ci}: Pitch factor for L_i, where i=1,2,3

F_{wi}: Winding factor for L_i, where i=1,2,3

ρ: Common resistivity for L_i, where i=1,2,3

D_{ii}: Core density for L_i, where i=1,2,3

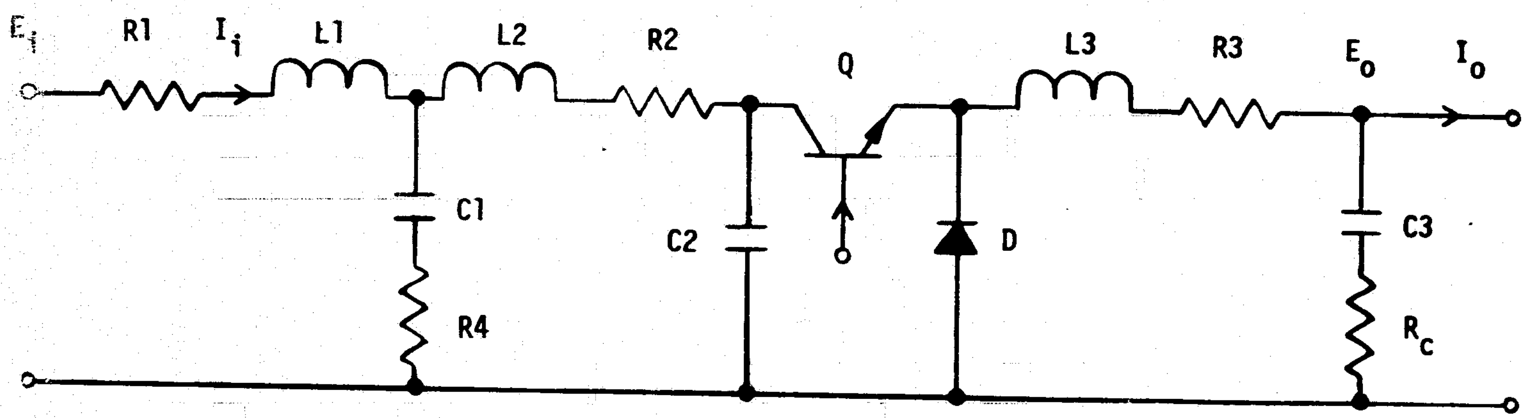


Figure 33 A Buck Converter Power Stage with a Two-Stage Input Filter

Table 4. Design Optimization Summary

Variables \ Components		L1	L2	L3	R1	R2	R3	R4	C1	C2	C3	F
A	Core Cross-sectional area	X	X	X								
N	Number of turns	X	X	X								
AC	Area per turn of conductor	X	X	X								
Z	Mean length of core	X	X	X								
L	Inductance needed	X	X	X								
R	Winding & external resistance				X	X	X	X				
C	Capacitance needed								X	X	X	
F	Switching frequency											X

Requirements	Constraints	
P_o = Output power e = Minimum efficiency required E_i = Input voltage range	$P_o(1-e)/e$ = (input filter loss) +(transistor and diode losses) +(output filter loss)	(1)
S = Frequency-dependent source ripple	$S = f_1(L1, L2, L3, C1, C2, R4, F, P_o, E_i, E_o)$	(2)
E_o = Output voltage		
r = Output ripple	$r = f_2(L3, C3, RC, F, E_i, E_o)$	(3)
P_e = Maximum input-filter resonant peaking	$P_e = f_3(C1, C2, L1, L2, R4)$	(4)
Full window	$f_4(ACk, Nk, Zk, Ak) = 0, \quad k=1,2,3$	(5,6,7)
No inductor saturation	$f_5(Nk, Ak, Lk, P_o, E_i) = 0, \quad k=1,2,3$	(8,9,10)

Optimization Criterion

Weight W = Iron weight + Copper weight + capacitor weight

$$= f_7[\Sigma(Ak \cdot Zk)] + f_8(\Sigma Ck \cdot Nk \cdot Ak) + f_9(\Sigma Ck)$$

D_{ci}: Conductor density for L_i, where i=1,2,3

B_{si}: Saturation flux density for L_i, where i=1,2,3

D_{cpi}: Weight per microfarad for C_i, where i=1,2,3

V_{st}: Collector-emitter drop when Q conducts

V_{be}: Base-emitter forward drop of Q

T_{sr}: Transistor switching rise time

T_{sf}: Transistor switching fall time

V_d: Forward diode drop

T_{nd}: Diode turn-on time

T_{fd}: Diode turn-off time

T_{re}: Diode recovery time

$O_e(F)$: Frequency-dependent core-loss factor for inductor L3, which processes a larger ac flux.

6.6.2.2 <u>Given Requirements</u>

The given requirements are the following:

PE: Input filter resonant peaking limit

P_o: Output power

E_i: Input voltage

E_o: Output voltage

s(F): Frequency-dependent source conducted interference

r_i: Output ripple

Sufficient core window

No magnetics saturation

6.6.2.3 Unknown Variables

The unknown variables $x = (x_1 \ldots x_n)^T$ are the following:

R_i: dc resistance for L_i, i=1,2,3

L1,L2,C1,C2

R4,L3,C3: Input/output filter parameters

A_i: Cross-sectional areas of inductors L_i, i=1,2,3

Z_i: Mean length of inductors L_i, i=1,2,3

N_i: Number of turns for L_i, i=1,2,3

A_{ci}: Winding areas per turn for L_i, i=1,2,3

F: Switching frequency

6.6.2.4 Objective Function

The objective function f(x,k) in this example is the total iron, copper, capacitor, and semiconductor weight. Since the semiconductor weight can be considered as fixed, the function f(x,k) becomes:

$$f(x,k) = \text{core weight} + \text{winding weight} + \text{capacitor weight}$$

$$= \Sigma\, D_{ii} A_i Z_i + 4 \Sigma D_{ci} A_i^{0.5}\, F_{ci} N_i A_{ci} + \Sigma D_{cpi} C_i,$$

$$i = 1,\ 2,\ \&\ 3 \qquad (211)$$

6.6.2.5 Constraint Equations

The constraints $g_j(x,k,r) = 0$ include the following expressions:

Loss Constraint-

In this constraint, the sum of all component losses should not exceed the total losses allowed by the minimum efficiency requirement, or,

$$P_{if} + P_t + P_d = P_{ofi} + P_{dc} \leq P_o\ (1-e)/e \tag{212}$$

P_{if} = input filter copper loss

$$= 4 \left(\frac{P_o}{eE_i}\right)^2 \rho \left(\frac{F_{c1}N_1A_1^{0.5}}{A_{c1}} + \frac{F_{c2}N_2A_2^{0.5}}{A_{c2}}\right) \tag{213}$$

P_t = Transistor conduction loss

+ base drive loss based on a forced Bets of 10

+ turn-on switching loss

+ turn-off switching loss

$$= \frac{PV_{st}}{E_i} + \frac{0.1\ P_oV_{be}}{E_i} + \frac{E_iT_{sr}F}{6}\left[\frac{P_o}{E_o} - \frac{(E_i-E_o)E_o}{2L_3E_iF}\right] + \frac{E_iT_{sf}F}{6}\left[\frac{P_o}{E_o} - \frac{(E_i-E_o)E_o}{2L_3E_iF}\right] \tag{214}$$

P_d = Diode conduction loss

+ turn-off and recovery loss

+ turn-on loss

$$= \frac{(E_i-E_o)P_oV_d}{E_oE_i}$$

$$+ \frac{E_iF(T_{fd}+3T_{re})}{12}\left[\frac{P_o}{E_o} - \frac{(E_i-E_o)E_o}{2L_3E_iF}\right]$$

$$+ \frac{E_iF\ T_{nd}}{12}\left[\frac{P_o}{E_o} + \frac{(E_i-E_o)E_o}{2L_3E_iF}\right] \tag{215}$$

P_{ofi} = Output-filter inductor core loss

+ output-filter inductor copper loss

$$= \frac{80E_o\ (E_i-E_o)Z_3\ 0_e\ (F)}{N_3E_i}$$

$$+ \frac{4\rho F_{c3}N_3A_3{}^{0.5}}{A_{c3}}\left[\frac{P_o}{E_o}{}^2 + \frac{(E_i-E_o)E_o}{RL_3E_iF}\right]^2 \tag{216}$$

P_{oc} = Output filter ESR losses

$$= \frac{1}{12}\left[\frac{(E_1-E_o)}{12L_3E_iF}\right]^2 R_o \tag{217}$$

Notice the dependence of these losses on the switching frequency F in equations (214) to (217). This includes the core loss expressed in (216), where $0_e(F)$ relates the width of the inductor flux-vs-ampere-turn loop to frequency F.

Source EMI Constraint

The frequency-dependent source EMI requirement has a constant peak-current allowance of "S" amperes when the frequency is below 2kHz, and decreases logarithmically from 2kHz on. The input filter must be designed so that:

$$\text{Required attenuation at switching frequency F} \leqq \frac{\text{EMI Requirement at F}}{\text{Fundamental switching current}}$$

Analytically, this relation becomes:

$$\frac{1}{\frac{L_2C_2}{L_1C_1}\left(2\Pi F\, L_1^{1/2}\, C_1^{1/2}\right)^3 \frac{1}{D} - \frac{C_2}{C_1}\left(2\Pi F\, L_1^{1/2}\, C_1^{1/2}\right)^2}$$

$$\leq \frac{\dfrac{S}{[1 + (\frac{F}{2000})^2]^{1/2}}}{(A^2 + B^2)^{1/2}} \qquad (218)$$

where:

$$A = \frac{2P_o}{\Pi E_o} \text{ Sin } \frac{\Pi E_o}{E_i} \qquad (219)$$

$$B = \frac{(E_i - E_o)E_o}{L_3 F \Pi E_i} \text{ Cos } \left(\frac{\Pi E_o}{E_i} - \frac{S_{in}(\Pi E_o/E_i)}{\Pi E_o/E_i}\right) \qquad (220)$$

$$D = R_4 \left(\frac{C_1}{L_1}\right)^{0.5} \qquad (221)$$

Other Input Filter Design Constraints

In addition to source EMI, other critical design aspects of an input filter include its forward resonant peaking and its output impedance, as they are improtant in determining the audiosusceptibility performance and the control-loop stability of the regulator. While these filter characteristics normally are not included in the regulator specification sheet, the includsion of the self-imposed resonance and impedance characteristic becomes highly desirable in order to ensure that the optimum-weight power circuit design will be compatible with its companion control circuit. In this example, the requirement "PE" concerning the resonant peaking limit is imposed as a design constraint:

$$(PE)_1^2 \leq \frac{1 + \frac{R_4{}^2 C_1}{L_1}}{\left(\frac{C_2}{C_1}\right)^2 + \frac{R_4{}^2 C_1}{L_1}\left(1 - \frac{C_2}{C_1} - \frac{L_2 C_2}{L_1 C_1}\right)^2} \qquad (222)$$

Output Ripple Constraint

The output ripple should be smaller than the corresponding requirement specified:

$$r_i \geqq \frac{1}{8L_3C_3}\left(1 - \frac{E_o}{E_i}\right)\left[\left(\frac{1}{F}\right)^2 + \frac{4C_3^{\,2}\,R_c^{\,2}\,E_i^{\,2}}{E_o(E_i - E_o)}\right] \tag{223}$$

Window Area Constraints

All inductor windings must be accommodated within the physical confine of the available core window, taking into account the proper winding factor F_W. Thus, for inductors L_1 to L_3,

$$\left(\frac{N_i A_{ci}}{\pi F_{Wi}}\right)^{1/2} - \frac{Z_i}{2\pi} + \frac{A_i^{\,1/2}}{2} = 0, \; i = 1, 2, 3 \qquad \begin{matrix}(224)\\(225)\\(226)\end{matrix}$$

Operating Flux Density Constraints

The inductors must not be operated beyond the intended flux density levels. In this example, the intended levels are taken as the saturation level B_{si}. Since L1 and L2 only conduct direct current,

$$N_i A_i - \frac{L_i P_o}{eE_i B_{si}} = 0, \qquad i = 1, 2 \qquad \begin{matrix}(227)\\(228)\end{matrix}$$

Inductor L3 processes both dc and ac components,

$$N_3 A_3 - \frac{L_3}{B_{s3}}\left(\frac{P_o}{E_o} + \frac{(E_i - E_o)E_o}{ZL_3E_iF}\right) = 0 \tag{229}$$

Having defined all constants, requirements, variables, objective functions, and constraints, the goal of this design example is to solve all variables to satisfy each constraints specified in eqs. (212) to (229), and concurrently to minimize the quantity specified in eq. (211).

Obviously, a problem of this complexity is not amendable to closed-form solutions. The SUMT code is used to seek optimum solutions numerically. The program listing, containing mostly constraints and their first and second derivatives with respect to variables within the constraints, is given in Appendix N.

Numerically, the following numbers are set to represent a practical converter:

P_o = Output power ≈ 100w

e = 0.92 at highest E_i at room temperature

E_i = 20V to 40V

E_o = 15V

F_{ci} = 1.9

F_{wi} = 0.4

$\rho = 1.724 \times 10^{-8}$ ohmmeter

V_{ST} = 0.25V at 8A

V_{be} = 0.8V

$T_{sr} = 0.15 \times 10^{-6}$ sec

$T_{sf} = 0.2 \times 10^{-6}$ sec

V_D = 0.9V at 8A

$T_{nd} = 0.03 \times 10^{-6}$ sec

$T_{fd} = 0.05 \times 10^{-6}$ sec

$T_{re} = 0.03 \times 10^{-6}$ sec

$(PE)_1 = 2.0$

$(PE)_2 = 0.333$

$B_{si} = 0.4$ Weber/meter^2

$O_e(F) = 0.7F^{0.5}$

$r_i = 0.01$

$R_C = 0.4$ ohms ($T = -30°C$)

$D_{ii} = 7800$ kg/m^3

$D_{Ci} = 8900$ kg/m^3

$K_{CP1} = 210$ kg/farad

$K_{CP2} = 1100$ kg/farad

$K_{C3} = 72$ kg/farad

Two sets of optimum design results are illustrated in Table 5. The difference between them is that design #1 assumes a three-times higher ESR for the output-filter capacitor and a five-times more stringent source EMI requirement than those of design #2. In each design, all RLC parameters, the switching frequency, the design details of all magnetics, and the minimum weight, are collectively achieved in a single computer run which yields a minimum component-weight design.

Table 5. Optimum Converter Component Weight

VARIABLES		DESIGN #1 (R_c= 0.3Ω, S= 0.1A)	DESIGN #2 (R_c= 0.1Ω, S= 0.5A)
Z1	(cm)	5.10	3.11
A1	(cm^2)	0.438	0.161
N1	(turns)	40	21
AC1	(mm^2)	0.775	0.519
Z2	(cm)	3.86	2.35
A2	(cm^2)	0.251	0.092
N2	(turns)	22	12
AC2	(mm^2)	0.756	0.507
Z3	(cm)	7.84	5.20
A3	(cm^2)	0.694	0.235
N3	(turns)	56	36
AC3	(mm^2)	1.9	1.21
L1	(μH)	253	53.7
L2	(μH)	84	17.9
L3	(μH)	192	53.5
C1	(μH)	89.5	47
C2	(μH)	30.8	10
C3	(μH)	710	325
R1	(mΩ)	41.5	20.9
R2	(mΩ)	17.9	9.1
R3	(mΩ)	25.3	18.3
R4	(Ω)	2.97	0.94
F	(kHz)	22.0	43.9
W	(grams)	239.5	78.1

Notice the impact of ESR and source EMI on the two data columns of Table 5. For the same loss constraints every parameter of Design #2 is smaller than its counterpart of Design #1. The only exception is the analytically-determined optimum switching frequency, where the 43.9 KHz for Design #2 is almost twice that of the Design #1. As a result, the combined magnetics and capacitor weight of Design #2 is barely one-third of that for Design #1.

Prior to concluding this example, the following SUMT application experiences are stated.

- Being primarily a research tool not specifically designed for power converter optimizations, a user generally needs to experiment with SUMT to realize its capabilities as well as its limitations.
- To save computation time, the number of variables should be reduced to a minimum by combining all interdependent ones.
- Numerically, the g_j's vary over a very wide range. To avoid conditions where certain g_j's in the equation for $f_p(x,k)$ may be so large as to obscure the effects of the rest of the g_j's, each g_j must be properly scaled to insure that the effect of violating a given constraint is of the same order of magnitude as that of violating any other constraint.
- Depending on the problem involved, the initial set of guesses for optimum solutions can be very important in determining the rate of convergence. The SUMT used in various converter-optimization applications tended to perform well in the presence of good starting guesses of variables for constraints whose global and local properties are "well behaved". On the other hand, the guarantee that is "almost always converges" is not inherent in SUMT, nor is it expected from other algorithms in the forseeable future. This difficulty is the single most critical area when design optimizations via nonlinear programming techniques are attempted.

6.7 NEEDED IMPROVEMENTS ON DESIGN OPTIMIZATION

While a practical design optimization approach has been successfully demonstrated to solve specific complex problems, it is not the intention of this report to paint an over-simplified picture concerning power converter design optimization in general.

To start with, one must realize that an optimization is generally associated with physical phenomena. Thus, the design optimization is of practical value only when there exists an accurate understanding of the physical principles and mathematical models upon which the design constraints and the design constants all depend. Since weight and loss generally are used as power-converter optimization criteria, knowledge of power-device weight-loss characteristics is thus a prerequisite to a successful optimization. Of these characteristics, the more important ones are:

- The accurate core-loss data as a function of the switching frequency and the asymmetrical rectangular-waveform excitation.
- The "effective resistance" of magnetic windings in high-frequency, high-current applications.
- An acceptable semiconductor switching-loss profile for power transistors and diodes in a given magnetics-semiconductor power-circuit configuration, and the likely impacts exerted by the commonly-used means of energy recovery of switching losses.

These characteristics, at the present time, are insufficiently defined. Considering that they are needed in the day-to-day design effort without any excursion into the realm of optimization, better understanding of component behavior must be regarded as a necessity that is long overdue. Without further knowledge of these characteristics, the selection of the optimum switching frequency, which is the most important parameter in power converter design and weight-loss tradeoff, will continue to be determined empirically. Since the optimization results are as accurate as the participating design constants and constraints, the design optimization approach thus brings into sharp focus the pressing need for knowledge of these characteristics.

Furthermore, since most practical power converter optimization problems are sufficiently complicated to defy closed-form solutions, the availability of powerful and fast-convergent nonlinear programming algorithms is indispensable. However, no general-purpose algorithms can be expected to cope with specialized nonlinear power converter problems. Consequently, the development of dedicated computer optimization routines for a given class of power converters will likely become a highly specialized yet essential research area.

6.8 CONCLUSIONS AND FUTURE EMPHASIS

A practical power converter design optimization approach is proposed, and its implementation is discussed. Through practical engineering design examples, the approach is demonstrated to greatly facilitate several endeavors heretofore regarded as difficult or unattainable:

(1) It allows a cost-effective optimum design for a power component or a complete power converter, down to the component level. The design includes the identification of the optimum switching frequency and detailed magnetics design parameters. Not only meeting all power-dependent performance requirements, the optimization of either the weight, the loss, or any other realizable entity of a power converter can be achieved.

(2) The design takes into account the interdependent nature of the various functions within a power converter (e.g., the impact of output-filter parameters on the input-filter design). The total computer cost for a complete power circuit design is within the \$20-to-\$40 range, which compares favorably with days of suboptimum, piecemeal, hand-iterated design effort. Savings in both design and development cost are thus achieved.

(3) It provides a fast and accurate weight-loss trade-off as well as a means for ready assessment of the impact of a given requirement or a particular component characteristic on an optimum design.

(4) It can assist the power system designer to conceive the optimum system configuration and the proper converter specifications to achieve an overall optimum system, thus setting the stage for a more "scientific" design approach without relying heavily on subjective judgements.

Proper fostering for power-converter design optimization takes the form of accurate device characterizations and dedicated programming developments. These needed improvements are briefly outlined.

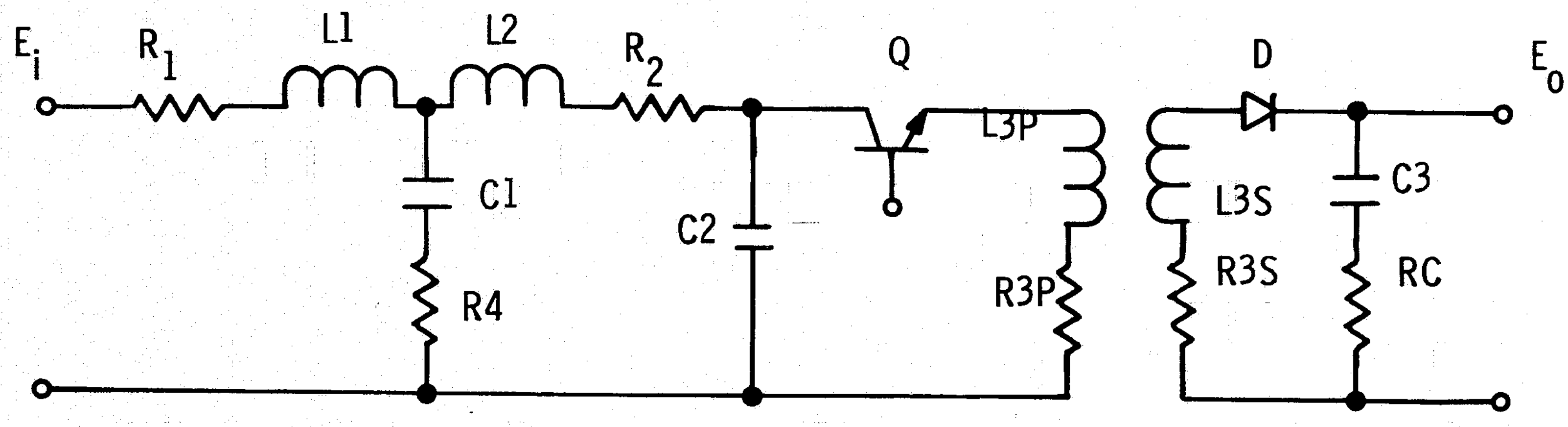
The importance of identifying an optimum design among all designs is underscored by the fact that, all other performances being equal, the design that is best in a specified sense is the one that usually prevails. However, being extremely hardware oriented and forever engrossed with necessary evils such as "schedule" and "cost", a converter designer often considers the design tasks successfully fulfilled even though the design itself may be, knowingly or unwittingly, quite "suboptimum". With the advent of high-speed computers and improved algorithms, applied optimization has become increasingly popular in all engineering disciplines. It is for the promotion of this trend in the field of power converter design that the optimization effort reported here is dedicated.

Future emphasis of the design optimization will focus on two efforts:

(1) To find a means to "normalize" the various constraints such that each constraint is properly weighted and evenly penalized. In this way, placing particularly-severe penalties to certain constraints can be avoided, and convergences of all constraints become attainable.

(2) Based on improved normalization, design optimization will be performed for the buck-boost and boost power circuits shown in Figure 34(A) and (B). Design equations relating variables to requirements will be generated in a manner similar to those used in this report for the buck converter.

Having gained valuable experiences, the confidence level of successfully fulfilling these emphases is high. It is expected that the resulting subprograms will be widely utilized in the design of the three most commonly used power converter configurations.



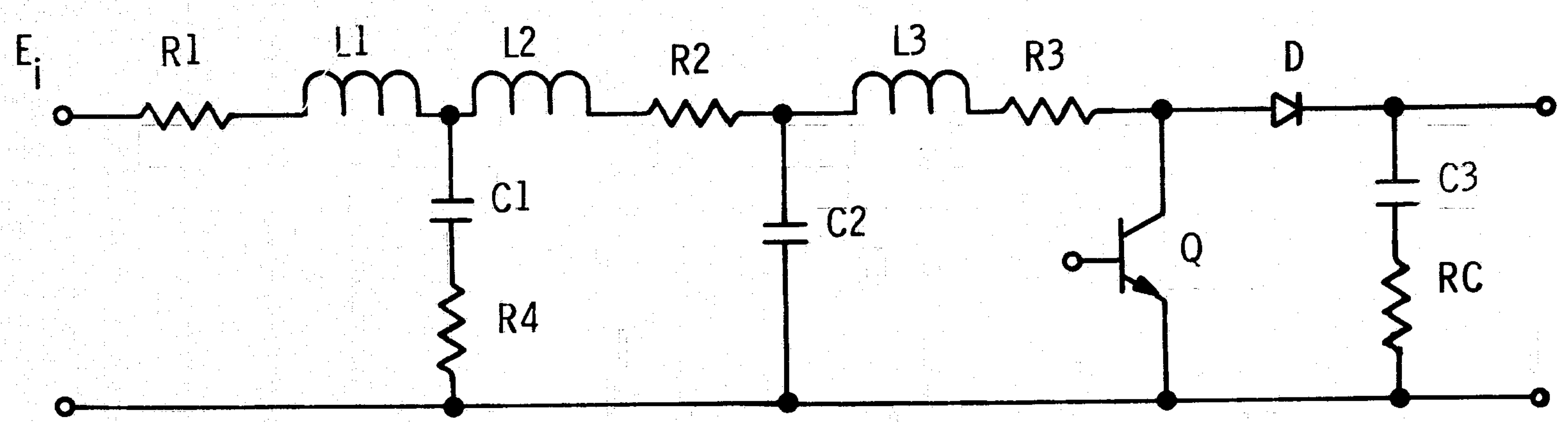
UNKNOWNS:

R1, R2, R3P, R3S, R4
L1, L2, L3P, L3S
C1, C2, C3
N1, Z1, A1, AC1 (For L1)
N2, Z2, A2, AC2 (For L2)
N3P, N3S, Z3, A3, AC3P, AC3S (For L3)
Switching Frequency F
N: turns, Z: core length,
A: core area, AC: winding size

OPTIMIZATION CRITERION:

Minimize the Sum of:
- Core Weight
- Winding Weight
- Capacitor Weight
- Heat Sink Weight

Figure 34(A) Design Optimization for Buck Boost Converter



UNKNOWNS:

R1, R2, R3, R4
L1, L2, L3
C1, C2, C3
N1, Z1, A1, AC1
N2, Z2, A2, AC2
N3, Z3, A3, AC3
Switching Frequency F

OPTIMIZATION CRITERION:

Minimize the sum of:

- Core Weight
- Winding Weight
- Capacitor Weight
- Heat Sink Weight

Figure 34(B) Design Optimization for Boost Power Converter

7. SYSTEM ANALYSIS SUBPROGRAM (SAS)

The system Analysis Subprogram is intended to extend the design optimization and performance analysis from the equipment level to the system level, thus providing power processing engineer with design and tradeoff tools. The subprogram categories thus include system configuration design and system performance (dynamic intra-system interactions), which represent, respectively, the extension of DOS and PAS.

A complete system configuration study is, by nature, quite complex. It involves at least the following considerations.

Optimum criterion: Cost, weight, reliability

Design considerations: Payload, environment, operating cycle, & life requirements

Special load equipment

Power source and energy storage

Power distribution

A system engineer is responsible for the definition and information collection regarding the first three items. The last two items, in conjunction with the power processing equipment, are the basic constituents of the systems analysis subprogram.

As stated previously, an overriding constraint in conducting the system analysis is the prohibitive complexity and therefore, the attendent modeling and analysis cost including that of the computation time. By necessity, then, the SAS effort must follow closely those involved in DOS and PAS so that merely an extension of the established techniques instead of the generation of new dedicated techniques is needed.

For this reason, the system analysis conducted in this MAPPS phase is composed of the following two efforts:

(1) The extension of design optimization subprogram to the configuration design of a source-line regulator system.

(2) The extension of performance analysis subprogram to the cost-effective simulation of a 12th order power processing system.

7.1 DESIGN OPTIMIZATION OF SOURCE-LINE-REGULATOR SYSTEM

In this example, the buck power converter shown in Figure 33 is integrated with a solar-array battery source of a known power density (kilogram/watt). The converter mechanical packaging weight is also included in the overall design optimization. Since the converter loss is supplied from the power source, and since the converter packaging weight (heat sink included) increases with the converter losses, for a given output power it follows that the combined source-and-mechanical-package weight becomes heavier if more converter loss is allowed. On the other hand, experience also indicates that the total converter component weight (magnetics and capacitors) tends to diminish with more allowable losses. Consequently, for a given output power as well as a given source density and packaging density, there must exist an optimum converter efficiency at which the combined system weight including power source, converter packaging, and converter component, is at its minimum. The objective is to identify numerically such an optimum efficiency. The minimum efficiency requirement "e" used previously in Section 6 for component weight optimization only thus is no longer a design constraint. Instead, the efficiency becomes an unknown variable in this design.

Comparing this example to that of Section 6, the difference formation of design variables, design constants, performance requirements, and the objective function are as follows:

- Efficiency "e" becomes a variable in addition to the twenty-three variables listed in Section 6.

- Two more design constants, KS and KH, for source and packaging densities respectively (in kilograms per watt), are added to the twenty-eight constants.

- Efficiency "e" is no longer a performance requirement. All other requirements in Section 6, however, remain applicable to this example.

- The loss constraint used in Section 6 is eliminated. The sum of all losses, i.e., the quantity

$$\Sigma P = P_{if} + P_t + P_d + P_{ofi} + P_{oc}$$

is being used in this example as part of the new objective function. All other constraints remain effective in this example.

- The new objective function for this example is:

$$\begin{aligned} W &= \text{Core Weight} + \text{Winding Weight} \\ &\quad + \text{Capacitor Weight} + \text{Source Weight} \\ &\quad + \text{Packaging Weight} \\ &= \Sigma\, D_{ii} A_i Z_i + 4\,\Sigma\, D_{ci} A_i^{0.5} F_{ci} N_i A_{ci} \\ &\quad + \Sigma\, D_{cpi} C_i + (P_o + \Sigma P)\,(K_s) \\ &\quad + (\Sigma P)\,(k_h) \quad , i = 1,2,3 \end{aligned} \tag{230}$$

Since ΣP has been shown previously in Section 6 to be a function of multiple factors:

$$\Sigma P = f(N_i, A_i, A_{ci}, L_3, Z_3, F, R_c),\ i = 1,2,3 \tag{231}$$

it can be seen that, after all variables are numerically identified by the SUMT processing, the term (ΣP) can be calculated to reveal the particular converter efficiency that will produce a minimum combined source-converter weight.

The SUMT program listing is given as Appendix O. Numerical values for constants, requirements, and formulation of constraints are identical to those used in Design #1 of Section 6. Two sets of optimum design results for minimum system weight are illustrated. in Table 7. The difference between them is the different source density "k_s" and packaging density "k_h" assumed. Several impacts exerted by different K_s's and k_h's are noted:

- As expected, a decrease in kg/w of source and package densities allows more loss in Design #2 to achieve an optimum-weight system. The system

Table 7. Optimum Source-Converter System

VARIABLES		DESIGN #1 (k_s = 65 g/w, k_h = 65 g/w)	DESIGN #2 (k_s = 16.3 g/w, k_h = 325 g/w)
Z1	(cm)	4.98	4.63
A1	(cm^2)	0.413	0.360
N1	(turns)	25	35
ACI	(mm^2)	1.13	0.70
Z2	(cm)	3.79	3.53
A2	(cm^2)	0.238	0.207
N2	(turns)	14	20
AC2	(mm^2)	1.133	0.701
Z3	(cm)	7.87	6.87
A3	(cm^2)	0.395	0.53
N3	(turns)	43	40
AC3	(mm^2)	2.6	1.68
L1	(μH)	154	188
L2	(μH)	51	62.7
L3	(μH)	101	126
C1	(μH)	133	108
C2	(μH)	19	15
C3	(μH)	1346	1075
R1	(mΩ)	18.3	39
R2	(mΩ)	8.1	17
R3	(mΩ)	13.5	22.5
R4	(Ω)	0.81	0.99
F	(kHz)	22.1	22.2
W	(kg)	7.56	2.17
EFF.	(%)	94.12	93.60

efficiency is reduced from 94.1% of Design #1 to 93.6% of Design #2. The 94.1%, incidentally, represents nearly the maximum possible efficiency consistent with the various design constants specified.

- For a four-to-one reduction in source density, the optimum efficiency only decreases from the approximate maximum limit by 0.5%. Since the realistic source density (including source and source conditioning) currently available is in the proximity of that used in Design #1, it is not surprising that the system designer has currently placed the highest emphasis on maximizing the converter efficiency.

7.2 DYNAMIC PERFORMANCE ANALYSIS OF A 12TH ORDER REGULATOR SYSTEM

The emphasis of this example is to address the dynamic aspect of the system performances, particularly those involving hard nonlinearities. Obviously, the most effective tool is system simulation based on propagation of the recurrent time domain state equations described in Section 4. A boost regulator-inverter system used in the NASA HEAO program, containing an equivalent of twelve state variables, is used for this effort. The objective here is to demonstrate the feasibility of simulating a large nonlinear system employing state-space techniques.

The system contains a fourth-order input filter, a fourth-order power stage including a second-stage LC filter, a second-order load simulating the outputs of a square-wave parallel inverter, and a control circuit containing two energy-storage elements. The simplified schematic of such a system is show in Figure 35.

Differential equations of the power-stage configuration are represented by equations (232) to (241). Two dummy variables, e_i and i_D, are introduced to represent the nonlinear characteristics of the system. The differential equations for the control loop are described by equations (242) to (244).

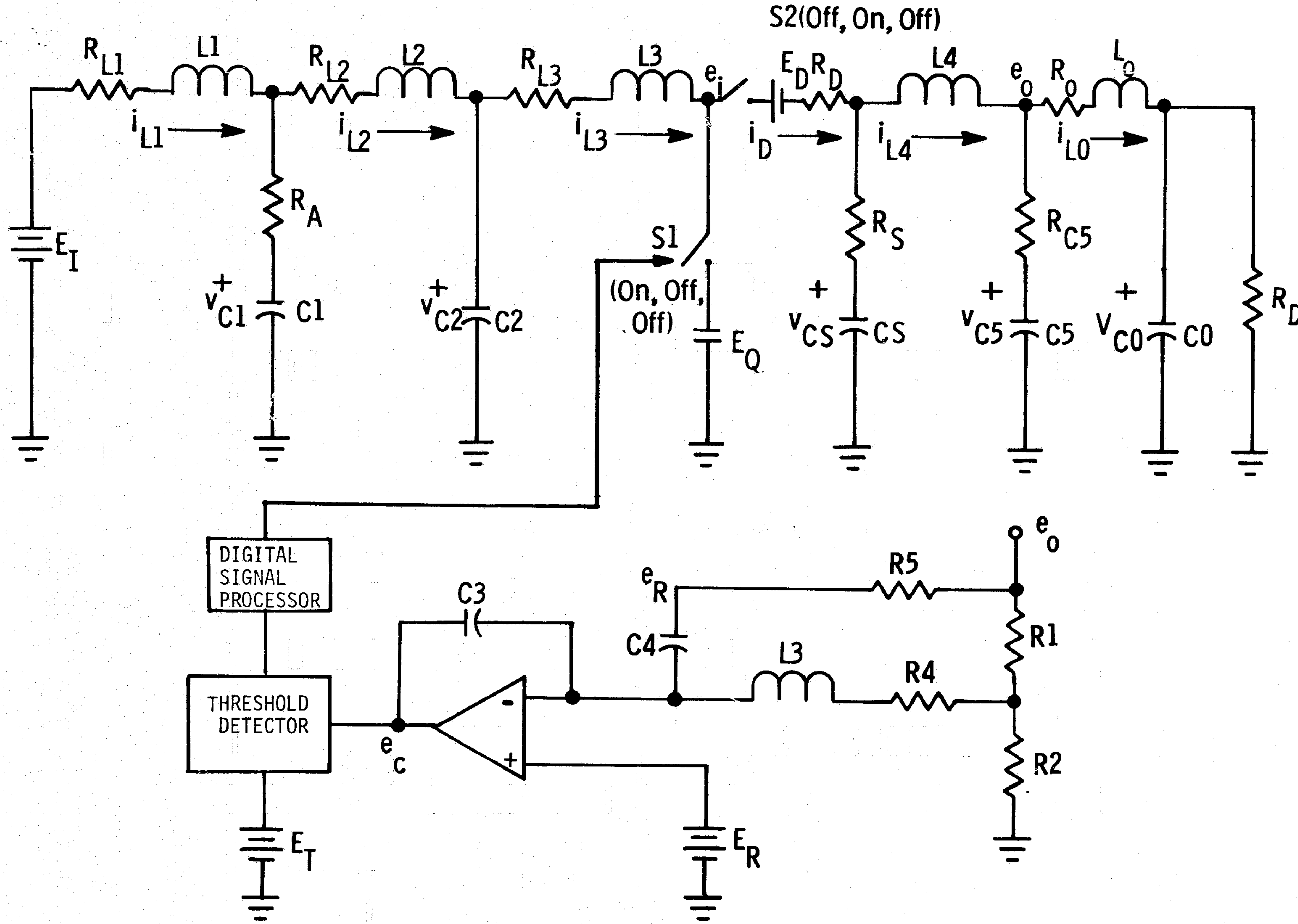


Figure 35 A Simplified 12-th Order System

Input Filter

$$\frac{di_{L1}}{dt} = \frac{1}{L_1} \left[E_I - R_{L1} i_{L1} - R_A (i_{L1} - i_{L2}) - V_{C1} \right] \tag{232}$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1} (i_{L1} - i_{L2}) \tag{233}$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2} \left[V_{C1} + R_A (i_{L1} - i_{L2}) - R_{L2} i_{L2} - V_{C2} \right] \tag{234}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2} (i_{L2} - i_{L3}) \tag{235}$$

Energy Storage Inductor

$$\frac{di_{L3}}{dt} = \frac{1}{L3} (V_{C2} - R_{L3} i_{L3} - e_i) \tag{236}$$

Output Filter

$$\frac{dV_{CS}}{dt} = \frac{1}{C_S} (i_D - i_{L4}) \tag{237}$$

$$\begin{aligned}
\frac{di_{L4}}{dt} &= \frac{1}{L4} \quad R_X (i_D - i_{L4}) + v_{CS} - R_{L4} i_{L4} - R_{C5} C_5 v_{C5} \\
&= \frac{R_S}{L_4} i_D - \frac{R_S + R_{L4}}{L_4} i_{L4} + \frac{V_{CS}}{L_4} - \frac{R_{C5}}{L_4} (i_{L4} - i_{L0}) - \frac{1}{L_4} v_{C5} \\
&= \frac{R_S}{L_4} i_D - \frac{1}{L_4} (R_S + R_{L4} + R_{C5}) i_{L4} + \frac{v_{CS}}{L_4} - \frac{1}{L_4} v_{C5} + \frac{R_{C5}}{L_4} i_{L0}
\end{aligned} \tag{238}$$

$$\frac{dv_{C5}}{dt} = \frac{1}{C_5} (i_{L4} - i_{L0}) \tag{239}$$

Simulated Converter Load

$$\frac{di_{L0}}{dt} = \frac{1}{L_0} \; v_{C5} + \frac{R_{C5}}{L_0} (i_{L4} - i_{L0}) - \frac{R_0}{L_0} i_{L0} - \frac{v_{C0}}{L_0} \tag{240}$$

$$\frac{dv_{C0}}{dt} = \frac{1}{C_0} (i_{L0} - \frac{1}{R_L} v_{C0}) \tag{241}$$

In deriving the differential equation for the control loop, Figure the following assumptions are made:

1. The integrator is operating in its linear region.
2. The control circuit has an insignificant load effect.

The first assumption is always true even during the transient step change of the input voltage or the step change of the load. The second assumption holds true in normal-load operation. For open-load operation, the result deviates slightly but still within reasonable accuracy. The differential equations for the control loop are:

$$\begin{aligned}\frac{de_c}{dt} = &- \frac{n}{C_3R_X} v_{C2} - \frac{n\, R_{L3}}{C_3R_X} i_{L3} \\ &- \frac{R_{C5}}{C_3} (\frac{R_2}{R_1 + R_2} \frac{1}{R_X} + \frac{1}{R_5}) (i_{L4} - i_{L0}) \\ &- (\frac{R_2}{R_1 + R_2} \frac{1}{R_X} + \frac{1}{R_5}) \frac{1}{C_3} v_{C5} + \frac{1}{C_3R_5} e_R \\ &+ \frac{n}{C_3R_X} e_i + \frac{E_R}{C_3R_X}\end{aligned} \tag{242}$$

where $R_X \triangleq (R_1R_2 + R_1R_4 + R_2R_4) / (R_1 + R_2)$

$$\frac{de_R}{dt} = \frac{R_{C5}}{C_4R_5} i_{L4} - \frac{R_{C5}}{C_4R_5} i_{LO} + \frac{1}{C_4R_5} v_{C5} - \frac{1}{C_4R_5} e_R \tag{243}$$

The output voltage is:

$$e_O = R_{C5} (i_{L4} - i_{LO}) + v_{C5} \tag{244}$$

For the three distinct operation intervals: T_{ON}, T_{F1}, and T_{F2}, the dummy variables e_i and i_D are assigned different variables. For detailed information, please refer to [3]. The differential equations (232) through (243) can be written into differential-difference equations each corresponding to a specified time interval, i.e., t_{ON} or t_{OFF}. The differential-difference equations are shown in the following pages. The state variables are defined below:

$i_{L1} \triangleq x_1$ | $i_{L4} \triangleq x_7$
$v_{C1} \triangleq x_2$ | $v_{C5} \triangleq x_8$
$i_{L2} \triangleq x_3$ | $i_{LO} \triangleq x_9$
$v_{C2} \triangleq x_4$ | $v_{CO} \triangleq x_{10}$
$i_{L3} \triangleq x_5$ | $e_R \triangleq x_{11}$
$v_{C_S} \triangleq x_6$ | $e_C \triangleq x_{12}$

(1) During T_{ON},

$$i_D = 0$$

$$e_i = E_Q$$

$$\dot{X}_1 = -(R_{L1} + R_A) X_1/L_1 - X_2/L_2 + R_A X_3/L_1 + E_I/L_1$$

$$\dot{X}_2 = X_1/C_1 - X_3/C_1$$

$$\dot{X}_3 = R_A X_1/L_2 = X_2/L_2 - (R_A + R_{L2}) X_3/L_2 - X_4/L_2$$

$$\dot{X}_4 = X_3/C_2 - X_5/C_1$$

$$\dot{X}_5 = X_4/L_3 - R_{L3} X_5/L_3 - E_Q/L_3$$

$$\dot{X}_6 = - X_7/C_5$$

$$\dot{X}_7 = X_6/L_4 - (R_S+R_{C5}+R_{L4}) X_7/L_4 - X_8/L_4 + R_{C5} X_9/L_4$$

$$\dot{X}_8 = X_7/C_5 - X_9/C_5$$

$$\dot{X}_9 = R_{C5} X_7/L_0 + X_8/L_0 - (R_{C5} + R_0) X_9/L_0 - X_{10}/L_0$$

$$\dot{X}_{10} = X_9/C_0 - X_{10}/(c_o R_L)$$

$$\dot{X}_{11} = R_{C5} X_7/(C_4 R_5) + X_8/(C_4 R_5) - R_{c5} X_9/(C_4 R_5) - X_{11}/(C_4 R_5)$$

$$\dot{x}_{12} = -n x_4/(C_3 R_x) - n R_{L3} x_5/(C_3 R_x) - R_{C5} x_7 \left(\frac{R_2 R_x}{R_1+R_2} + \frac{1}{R_s} \right) /C_3$$
$$- \left(\frac{R_2}{R_1+R_2} \frac{1}{R_x} + \frac{1}{R_5} \right) x_8/C_3 + R_{C5} \left(\frac{R_2}{R_1+R_2} \frac{1}{R_x} + \frac{1}{R_5} \right) x_9/C_3$$
$$+ x_{11}/(C_3 R_5) + E_R/(C_3 R_x) + n E_Q/(C_3 R_x)$$

(2) During T_{F2},

$$i_D = i_{L3}$$

$$e_i = (R_s+R_D)i_{L3} - R_s i_{L4} = v_{Cs} + E_D$$

$$\dot{x}_1 = -(R_4+R_A)x_1/L_1 - x_2/L_2 + R_A x_3/L_1 + E_2/L_1$$

$$\dot{x}_2 = x_1/C_1 - x_3/C_1$$

$$\dot{x}_3 = R_A x_1/L_2 + x_2/L_2 - (R_A+R_{L2})x_3/L_2 - x_4/L_2$$

$$\dot{x}_4 = x_3/C_2 - x_5/C_2$$

$$\dot{x}_5 = x_4/L_3 - (R_{L3}+R_s+R_D)x_5/L_3 - x_6/L_3 + R_s x_7/L_3 - E_D/L_3$$

$$\dot{x}_6 = x_5/C_s - x_7/C_s$$

$$\dot{x}_7 = R_x x_5/L_4 + x_6/L_4 - (R_s+R_{L4}+R_{C5})x_7/L_4 - x_8/L_4 + R_{C5}x_9/L_4$$

$$\dot{x}_8 = x_7/C_5 - x_9/C_5$$

$$\dot{x}_9 = R_{C5}x_7/L_o + x_8/L_o - (R_{C5}+R_o)x_9/L_o - x_{10}/L_o$$

$$\dot{x}_{10} = x_9/C_o - x_{10}/(C_o R_L)$$

$$\dot{x}_{11} = R_{C5}x_7/(C_4R_5) + x_8/(C_4R_5) - R_{C5}x_9/(C_4R_5) - x_{11}/(C_4R_5)$$

$$\dot{x}_{12} = - nx_4/(C_3R_x) - n(R_{L3} - R_s - R_D)x_5/(C_3R_x) + n\, x_6/(C_3R_x)$$
$$- \left[\frac{nR_3}{C_3R_x} + \frac{R_{C5}}{C_3}\left(\frac{R_2}{R_1+R_2}\ \frac{1}{R_x} + \frac{1}{R_5}\right)\right] x_7.$$
$$- \frac{1}{C_3}\left(\frac{R_2}{R_1+R_2}\ \frac{1}{R_x} + \frac{1}{R_5}\right) x_8 = R_{C5}\left(\frac{R_2}{R_1+R_2}\ \frac{1}{R_x} + \frac{1}{R_5}\right)x_9/C_3$$
$$+ x_{11}/(C_3R_5) + E_R/(C_3\, R_x) + n\, E_D/(C_3R_x)$$

(3) During T_{F2},

$$i_{L3} = i_D = 0$$

$$e_D = x_4$$

$$\dot{x}_1 = -(R_{L1}+R_A)x_1/L_1 - x_2/L_1 + R_A x_3/L_1 + E_2/L_1$$

$$\dot{x}_2 = x_1/C_1 - x_3/C_1$$

$$\dot{x}_3 = R_A x_1/L_2 + x_2/L_2 - (R_{L2}+R_A)x_3/L_2 - x_4/L_2$$

$$\dot{x}_4 = x_3/C_2$$

$$\dot{x}_5 = 0$$

$$\dot{x}_6 = -x_7/C_s$$

$$\dot{x}_7 = x_6/L_4 - (R_s + R_{L4} + R_{C5})x_7/L_4 - x_8/L_4 - R_{C5}\, x_9/L_4$$

$$\dot{x}_8 = x_7/C_5 - x_9/C_5$$

$$\dot{x}_9 = R_{C5}\, x_7/L_o + x_8/L_o - (R_{C5}+R_o)x_9/L_o - x_{10}/L_o$$

$$\dot{x}_{10} = x_9/C_o - x_{10}/(C_o R_L)$$

$$\dot{x}_{11} = R_{C5}\, x_7/(C_4R_5) + x_8/(C_4R_5) - R_{C5}x_9/(C_4R_5) - x_{11}/(C_4R_5)$$

$$\dot{x}_{12} = R_{C5}\left(\frac{R_2}{R_1+R_2}\;\frac{1}{R_x} + \frac{1}{R_5}\right)x_7/C_3 - \left(\frac{R_2}{R_1+R_2}\;\frac{1}{R_x} + \frac{1}{R_5}\right)x_9/C_3$$
$$+ R_{C5}\left(\frac{R_2}{R_1+R_2}\;\frac{1}{R_x} + \frac{1}{R_5}\right)x_9/C_3 + x_{11}/(C_3R_5)$$
$$+ E_R/(C_3R_x).$$

The differential-difference equations presented above can be written in the compact form

$$\dot{\underline{X}} = F1\ \underline{X} + G1\ \underline{U} \qquad \text{during } T_{ON} \tag{245}$$

$$\dot{\underline{X}} = F2\ \underline{X} + G2\ \underline{U} \qquad \text{during } T_{F1} \tag{246}$$

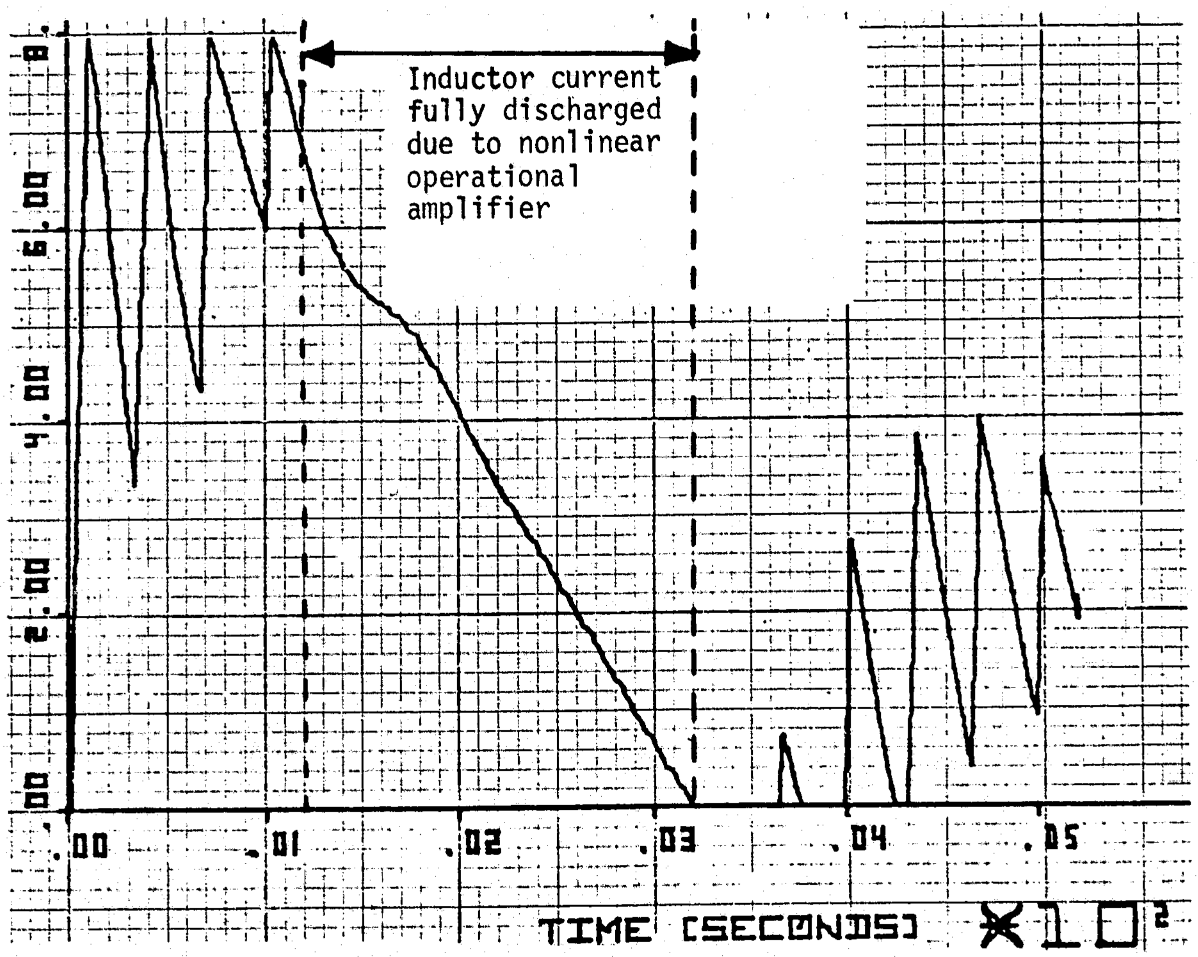
$$\dot{\underline{X}} = F3\ \underline{X} + G3\ \underline{U} \qquad \text{during } T_{F2} \tag{247}$$

and
$$e_o = R_{C5}\ X_7 + X_8 - R_{C5}\ X_9 \tag{248}$$

Equations (245), (246), and (247) admit closed-form solutions given as equations (121), (122), and (123) in Section 4.7. Digital simulation of the 12th order sysem based on equations (121) to (123) is then achieved in the same manner described previously in Section 4.7. For clarity, the detailed computer program is not included here.

Two sample simulation runs are shown in Figure 36 (A) and (B), illustrating the converter output voltage and energy-storage inductor current, respectively, following a regulator command-on. Of particular interest is the discharge of inductor current in (B) due to nonlinearity in the operational amplifier. The phenomenon was also observed in the regulator breadboard tests, thus lending credibility to the accuracy of the discrete time-domain simulation approach. The total cost for both runs is less than \$10.00.

(A) Converter Output Voltage



(B) Inductor Current

Figure 36. Simulation Runs for Regulator Start-up
(A) Output Voltage, (B) Inductor Current

7.3 CONCLUSION AND FUTURE EMPHASES

The effort documented in this section has demonstrated the feasibility of extending the performance analysis and design optimization for the equipment to the system level.

The following aspects of system analysis will be emphasized in the future:

- Configuration study of source-battery-charger-discharger system and power distribution units.
- Configuration study and anlysis of:

  Centralized vs. decentralized system
  dc vs. ac distribution system
  dedicated system (e.g., electric propulsion)

The basic tools for conducting these studies have been partially established. To what extent these studies can be realized depends on the intensity of the support, which would likely rely heavily on NASA's planned missions in the future.

8. COMPONENT LIBRARY SUBPROGRAMS

The component Library Subprograms (CLS) consist of the arrays of useful data for commonly-used components. The following CLS aspects are included in the discussion here:

- Functional relationship with other subprograms
- Types and characteristics of components to be stored
- Needed component characteristics study
- Component library structures
- Component libraries implemented.

8.1 FUNCTIONAL RELATIONSHIP WITH OTHER SUBPROGRAMS.

For CLS to be useful, it has to be organized and structured as to make all the data relating to any given component readily available to all other subprograms. When interrogated as to the existence of a single or a collection of data for a given component, it will produce the required information readily and in a format compatible with the requirement of the individual subprogram.

Specifically, the CLS relates to the other subprograms through the following functional requirements:

(1) The CLS shall provide the DOS, through prescribed search criteria, a list of best fit components, each with the closest match of ratings and characteristics in relation to those identified by the DOS as the optimum design. Since the equipment specifications processed by the DOS generally include both input-current ripple and output-voltage ripple, and since these performances vary greatly with the component initial tolerance and environmental temperature (primarily due to changes in C and ESR), the optimum design generated by the DOS using such equipment specifications as design constraints must therefore consult the CLS for the worst-case component characteristics to ensure design integrity under all conditions.

(2) The CLS shall provide the PAS with both nominal and worst-case component characteristics to allow the PAS to obtain the following:

- Nominal performance characteristics that are easily substantiated through hardware testing under nominal, room-temperature conditions.

- Worst-case performance characteristics to ensure compatibility between equipment requirements and capabilities.

8.2. TYPES AND CHARACTERISTICS OF COMPONENTS

8.2.1 Component Types

Component types include the following basic categories:

• Resistors:	Carbon, Film Wire-Wound, Precision
• Capacitors:	Tantalum (Foil and Solid), Film, Ceramic, High Voltage
• Diodes:	General Purpose, High Currents, High Voltage, Low Voltage Schottky.
• Transistors:	General Purpose, Power Switching
• Cores:	Square Loop, Linear, Ferrite.
• Conductors:	Solid, Litz
• IC's	Digital, Analog, HTL, TTL, MOS

8.2.2 Component Characteristics

For each component category, the groups of data residing in a component data bank are comprised of sets. Each set defines a given component. Each set in turn is made up of subsets, the elements of each subset describing some pertinent property of the component in that set. For example, the diode group in the component data bank may consist of 40 sets, representing 40 difference diodes. A given diode set would be comprised of a generic number subset, failure rate subset, voltage rating subset, etc. The subsets are listed as the following four major component categories:

- Resistors

  Available resistance

  Tolerance

  Temperature coefficient

  Power rating

  Unit weight as a function of power level

  Failure rate

  Cost

- Capacitors

  Available capacitance

  Tolerance

  DC voltage rating

  RMS current rating

  Nominal and worst-case ESR with temperature

  Case size

  Unit weight

  Failure rate

  Cost

- Transistors

  Generic number

  V_{CE} with a 10:1 base drive (nominal and min/max).

  Switching time and storage time

  Safe peak dissipation

  Voltage rating

  Current rating

  Power rating and derating with temperature

  Unit weight

  Failure rate

  Cost

- Magnetics

  Loss
  Cross-sectional area
  Mean length of magnetic path
  Permeability
  Core configuration
  Window area
  Saturation flux density
  Weight
  Cost

8.3 NEEDED COMPONENT CHARACTERISTICS STUDY

The major component characteristics needed to be addresses to those of magnetics, semiconductors, and capacitors.

<u>Magnetics</u>

The overriding preoccupation in most magnetics design aiming for a given set of performance specifications is to achieve either a minimum loss for a given weight, or a minimum weight for a given loss. Immediately, the following concerns can be raised:

(1) Is there an accurate model for core loss under asymmetrical squarewave excitation, as a function of frequency and flux-density excursion for different core materials?

(2) Is there a thorough understanding on the eddy current loss in the copper wire caused by flux linkage in the wire, particularly in high frequency, high current operations? Under what conditions is the use of Litz wire mandatory to effect loss reduction?

(3) Can one determine the adequate amount of "fly-back energy" of a square-loop core that is indispensible in sustaining oscillation in so many timing and drive applications, and yet has so frequently been glossed over in terms of "circuit descriptions".

Since power magnetics represent a major portion of the total equipment weight and significant percentage of the total equipment loss, and since there are still vast unknowns concerning their design and operation (particularly acute in view of the future high power, high frequency equipment), it is recommended that a major effort dedicated to magnetics be expanded to include the following items of interest:

- To collect, either through analysis, or more effectively through experiment, the pertinent core and copper loss data. The variables should include core materials, core and coil configurations, including Litz wire, and excitation waveforms, frequencies, and flux excursions.

- To develop an analytical model for high-frequency transformers and inductors to gain better understanding in all switching and incidental transient phenomena.

- To address certain commonly-encountered power processing phenomena closely related to the magnetics design, such as the use of "flyback energy" to sustain oscillation, the excessive voltage spike in magnetic-semi-conductor hybrid circuits, and the "effective inductance" which is smaller than the designed value due to the manifestation of small ac core losses as a resistance shunting the inductor.

Semiconductors

From strictly the component viewpoint, the single semiconductor modeling and analysis concern is the future trend of high power. Accompanied by the adequate protection and derating requirement, the high power demand could conceivably exceed the voltage and/or current capabilities of transistors. Silicon-controlled rectifiers are presently available with single chip (wafer) at ratings of 1000V 110A rms, and 5μs turn-off. They undoubtedly can, with the help of the proper power circuit design, be utilized to their advantages in a great many future high power, high frequency applications. The tools for the weight, reliability, performance and cost tradeoffs between the equipment using these two types of power switches shall be developed.

Capacitors

Capacitors are important in the analysis and modeling effort due to their impact on: (1) the output ripple caused mostly by the equivalent series resistance (ESR) within the capacitor, (2) the stability of the PPE control system through the capacitance or the ESR change with the ambient temperature, and (3) the damping effect contributed by the ESR to an LC filter, which may have unwittingly prevented many detrimental oscillations in past or existing equipment. These effects needed to be reflected.

8.4 COMPONENT LIBRARY STRUCTURES

Library data structures are expected to be stored upon on-line random access devices such as disc and drum files, (without random access devices, only sequential files such as those recorded on magnetic tape would need to be considered). The three basic forms of library structure are considered:

(1) Sequential Structures. Members of such a structure can only be read in order and thus to read the tenth element in sequence, it is necessary to read over the intervening nine members. This is a simple structure to implement and very conservative in the amount of space needed to contain the structure. Non-sequential retrieval and updating of isolated members tend to be slow operations and copying of the entire structure is often needed. A variation of a structure having a single sequence is introduced by having a (usually) brief index of pointers to members within the sequence. These index pointers can then be used to directly locate points within the structure from which sequential operation can then proceed.

(2) Indexed Structures. Members of this type of structure are located through the use of a key (e.g., a component part number) which is associated, in an index, with the location in the structure of the member(s) having that key value. This index, directory, or records, augment the data itself and permit immediate retrieval of items for

which index keys have been estabished. Such structures are very attractive where rapid resonses to random inquiries are needed. While the construction of the structure and selection of index parameters represent a certain amount of effort, it is considered worthwhile in view of the potential advantages particularly suited for power processing component library applications. A great many variations of this class of structure have been developed, and some will warrant consideration.

(3) Calculated Structures. Members of this form of structure are retrieved through the calculation of pointer values which are used to directly locate the member. (Hashing is frequently used to describe this procedure). No auxiliary directories are needed but a problem does exist since calculated values cannot normally be guaranteed to be unique. Thus, the calculated location of two different component parts might be identical with the result that some form of overflow chaining must be provided.

This discussion is brief, but should serve to emphasize the factors to be considered in the important process of future file design. It is noted that data structures are often of a hybrid form and that those features best suited for each library will be used.

At present, when a designer sets out to identify a component suitable for his application, he normally does so by first identifying a few most critical component characteristics. For example, the voltage rating, the current rating, and the saturation drop are generally major concerns in the selections of power transistors to be used in efficient switching regulators. Candidates preselected to fulfill these requirements are then evaluated for other secondary characteristics such as switching speed (although the preferential role of saturation drop and switching speed is often interchangeable), unit weight, case configuration, or cost, from which the final component is made.

The computer search routine, being a replica of the designer's methodology, should follow essentially the same pattern to avoid being detracted from the numerous minor component characteristics. Consequently, a rapid search and retrieval must be accomplished by indexing those few characteristics in which the designer is keenly interested. This indexing will be referred to as the major index. Only after the identification of those components exhibiting the needed key characteristics can further evaluation of details become practical. This evaluation can be achieved through a second set of indexing (minor index) of the remaining secondary characteristics, or, perhaps more efficiently, for an on-line user, by simply printing out the key and secondary characteristics of all components stored under the particular major index. In the later cases, the user then makes his on-line decision of his final selection of component(s).

8.5 COMPONENT LIBRARIES COMPILED

Data bases for the following component categories have been compiled:

- Foil tantalum capacitors
- Polycarbonate capacitor
- Wire-wound power resistors
- Conductor Sizes
- Powder Cores

Samples of the compilations are given in Appendix Q. The user's retrieval for these component libraries is discussed in Section 9, concerning the Data Management Program.

8.6 CONCLUSION TO SECTION 8

In this section, the component's functional relationship with other subprograms, their types and characteristics, the needed component study areas, the library structures and the libraries compiled, are discussed. To no one's surprise, complete component characterization and fully-automated component retrieval for various modeling and analysis subprograms are costly endeavors beyond the means of the current MAPPS program. In the future, a limited component-library implementation and component retrieval based on user's on-line decision making, rather than automatic processing, may be a more practical initial step.

9. MAPPS DATA MANAGEMENT PROGRAM

The objective of this document is to present the design of a computer based system for the Modeling and Analysis of Power Processing Systems (MAPPS). The MAPPS System is designed for use by the Designer/Analyst of Power Processing Systems. The purpose of the system is to provide efficient analytic tools to facilitate the design, modeling, and analysis of Power Processing Systems and their components. The procedure is to collect and/or build these tools in the form of computer programs and to integrate them into a coordinated data processing system.

The various analytic functions (MAPPS Major System Functions) incorporated now and in the future into the MAPPS System will be maintained as distinct modules with distinct responsibilities. MAPPS major system functions are exemplified by such major modules as Design Optimization (DOS), Performance Analysis (PAS), Systems Analysis (SAS), Component Library Subprogram (CLS) and the Data Base Manager (DBM). (Please note the trailing "S" in all the above acronyms stands for "Subprogram".) The integration of the various modules into a coordinated processing system will be accomplished by developing appropriate control and communication routines. An Executive User Interface (EUI) routine will provide the user the means for selecting specific processes for execution. An Executive module will carry out subprogram load requests and memory space allocation as well as input/output file linkage requests. Subprogram User Interface (SUI) routines will provide the means for user interaction with the system. One SUI will exist for each analytic subprogram integrated into the MAPPS System. Each SUI is capable of handling all of the communications relative to its respective subprogram.

In addition to several analytic subprograms there will be a Data Base Manager subprogram under control of the MAPPS Executive. The Data Base Manager (DBM) will respond to, and perform all, Data Base access requests generated during any and all execution of MAPPS System analytic routines. The basic operations performed by the DBM on the MAPPS System Data Base include STORE, MODIFY and RETRIEVE.

The Executive, Subprogram User Interface routines, the DBM and the Analytic Subprograms comprise the MAPPS System. The MAPPS System operates in the environment of a host computer operating system in either a timesharing or a batch mode. The host system is expected to provide a number of general purpose functions needed for enhancing the operation of the MAPPS System which will not be duplicated within the MAPPS System initially implemented. Such general purpose functions not included in earlier MAPPS configurations include external file management, text editing, program compilation/assembly and the numerous other functions normally available in a reasonably comprehensive computer operating system.

The normal use of the MAPPS System is projected to involve interactive communication between the system and the Designer/Analyst; however, batch use of the MAPPS system will also be available. The design of the MAPPS System takes into account the desire to utilize it on many different host computer systems. The design also seeks to make the interaction with the Designer/Analyst (User) as easy as possible. Ideally the user's effort may be concentrated on the problem at hand rather than on the administrative details of invoking the MAPPS System capabilities.

9.1 USE OF THE MAPPS SYSTEM

The MAPPS System will operate in one of two operating modes: interactive (timesharing) or batch. The ability to use either mode is predominantly dependent upon the capabilities of the host computer. At TRW Systems both modes will be available to the user.

In the interactive mode the use of the MAPPS System begins by signing on to the computer timesharing system. The Designer/Analyst (user) requests that the MAPPS System be loaded and executed in the conventional program load and execute manner. A conversation then begins between the user and an executive routine through which the user instructs the system to attach certain external files and to perform specific analytic and/or data base manipulation functions. Upon completion of the input cycle, the MAPPS System will proceed to execute and satisfy the user's requests. If intermediate results require a decision by the user, interactive conversation will again take place. During the course of a interactive session the user may display results, permanently or temporarily store results, or retrieve previously stored results from the data base. Interactive performance of several MAPPS System functions is expected to become common practice.

Batch mode use of the system is expected to take place generally whenever the host computer operating system does not support timesharing terminals. Also, on those occasions when execution of a particular function is expected to take a long time or generate extensive output, the user may wish to select batch mode operation. On such occasions it will be essential to thoroughly analyze the situation in order to insure the completeness and soundness of the input parameters and decisions. During execution in the batch mode there is not an opportunity for the user to alter the course of the process from the inputs originally submitted.

9.2 DESIGN REQUIREMENTS

Of all the requirements imposed on the MAPPS System design, five general categories stand out as the most imposing or critical requirements. The success of the MAPPS System development effort is greatly dependent upon the system's ease of use, flexibility and ease of modification, portability, interactive/batch operation, and fault protection features.

9.2.1 Ease of Use

The MAPPS System must be easy for the Designer/Analyst to use and should not require extensive knowledge of computer systems or programming. The operations which support the computerized functions performed for the user should be as transparent to him as is feasible within cost-effectiveness constraints. The system should allow for the user's depth of knowledge of the system by extending aid to the inexperienced user while permitting the knowledgeable user to take procedural shortcuts. The MAPPS System should also be relatively easy to maintain from the system programmer's point of view so that minimal effort in that area is needed.

9.2.2 Flexibility and Ease of Modification

The MAPPS System must be easily modified or expanded without excessive impact on the entire system. It is foreseen that a number of additional MAPPS System functions will be added to the system after the initial operational capability is provided. These additions should be taken into account early in the design process to allow their smooth integration into the system at later dates.

9.2.3 Portability

It is a requirement that the MAPPS System produced in the Phase II effort be "portable". This means the system will be designed so that a minimum conversion effort is required to move it from one computer hardware operating environment to another. It should be understood that a completely portable program in this sense is not totally realizable. While total portability is not attainable, the adjustments required to tailor the system to a new operating environment should be minimal.

9.2.4 Interactive/Batch Operation

Normal use of the MAPPS System is expected to be interactive between the Designer/Analyst and the system via timesharing terminals. At the user's option, the MAPPS System may also be used in a batch mode.

9.2.5 Fault Protection

The MAPPS System must have a reasonable ability to protect itself against failures which could be catastrophic to system data bases and other system generated output. When unable to completely recover, it will become important for the system to issue messages to aid in diagnosing the problem.

9.3 DESIGN TECHNIQUES

A high-quality software product (as the MAPPS System is intended to be) is readable, reliable, easy to extend functionally, and easy to maintain. The use of modularization, hierarchical program design, closed logic structures, and the sound principles of structured programming will contribute to these ends.

9.3.1 Modularization

Related functions (clerical, analytic, etc.) are collected into groups or modules with suitable interface logic to insure the integration of these modules into a coordinated processing system. Modularization facilitates design and maintenance activities by isolating dissimilar activities from one another. Often times it becomes necessary to implement program overlay loading techniques in order to fit software into the physical constraints of the host computer hardware system. The appropriate use of the modular design greatly facilitates implementing overlay loading.

9.3.2 Hierarchical Program Design

This technique is a part of the currently fashionable top-down design approach which begins at the highest system level, defines major functions, and then works downward until the lowest level of functions have been defined. We use a "top-down bias" approach which generally proceeds in a top-down manner with the addition of periodic assessments of potential problems at lower levels in the hierarchy. This can take the form of evaluating high-risk components, establishing common or reusable components. and minimizing machine dependence.

9.3.3 Closed Logic Structure

This technique uses subroutines and programs that have one entry and one exit point in a hierarchical manner. These structures are utilized in a calling-called relationship that resolves ultimately to one module at the highest level coordinating and controlling the actions of all those subordinate to it. This ties in well with the hierarchy mentioned above and with the concept of system modularization. This too tends to make both design and maintenance easier due to increased understandability of the resulting code.

9.3.4 Structured Programming

Structured programming is a set of principles established to assist software developers in producing programs that are readable, reliable, easy to expand and easy to maintain. Since these are also prime considerations in the development of the MAPPS System, it seems natural to make use of these principles in its development. Two qualifications are necessary, however. There is not general agreement in the industry as to the individual application of these principles and so an interpretation of these guidelines will be made. Also, significant portions of the MAPPS System are in the form of existing programs which may or may not be structured. It is not anticipated that restructuring such programs is a part of this effort. Newly created modules on the other hand will have structured programming principles applied to them.

9.3.5 Use of a High-Level Programming Language

Using a high-level programming language to code the MAPPS System is a requirement if portability is to be reasonably achieved. In selecting the programming language to be used in coding the MAPPS System, the following factors were considered:

- The language should be a standardized, high-level programming language.
- Compilers should be available on as wide a range of computer systems as possible.
- Differences in the language from one computer system environment to another should be small and well defined.
- The language should support extensive mathematical operations such as will be required by the MAPPS Subprograms.
- The language should be in widespread use.

- If possible, a body of programming and debugging aids should be available and operational.

The language that most closely fits these requirements is FORTRAN.

FORTRAN has a Standards Committee and a standard form of the language implemented on many different computer systems. Conversions from one environment to another have been accomplished and the potential problem areas are fairly well known.

FORTRAN (FORmula TRANslation) lends itself particularly to mathematical programming. The language is in use in a vast number of installations and a great number of known and operational programming/debugging aids exist for it.

One possible "soft" area of FORTRAN is in the handling of command and control data which is better handled by assembly language code. Efficiency may indicate the use of assembly language in certain routines of the MAPPS System. However, it is our intention to strive to use FORTRAN exclusively.

9.4 MAPPS SYSTEM MAJOR COMPONENTS

The MAPPS System consists of a number of computer programs and subprograms organized into modules. These modules each have a position in the operations hierarchy of MAPPS in accordance with certain communication requirements. The advantage of a modular organization will become apparent whenever additions or modifications to the MAPPS System are required. It will also ease if not actually make possible, the implementation of the MAPPS System on some computer configurations where it may become necessary to use program overlay techniques because of size limitation. Figure 37 illustrates the modular architecture of the MAPPS System. Dotted lines show separation of the major functions into modules. Level numbers are included to illustrate the potential computer loading overlay hierarchy of the various modules. Modules with like numbers cannot execute simultaneously if the use of overlays becomes necessary. Modules with like numbers roll in and out of the execution area on demand by the MAPPS Executive program. A discussion of the basic functions and features of each module follows below.

9.4.1 Host Computer Operating System

Level 0 is the host computer operating system. At TRW this system is commonly referred to as TRW/TSS. This system is supported on a complex of CDC 6000 and Cyber series computers. "MACE" is the basic operation system and "EDITOR" is an interactive text editing system. Both provide unique and powerful capabilities expected to support the resident portion of the MAPPS System.

Because attributes of timesharing systems are generalized, users going from one timesharing system to another find a number of

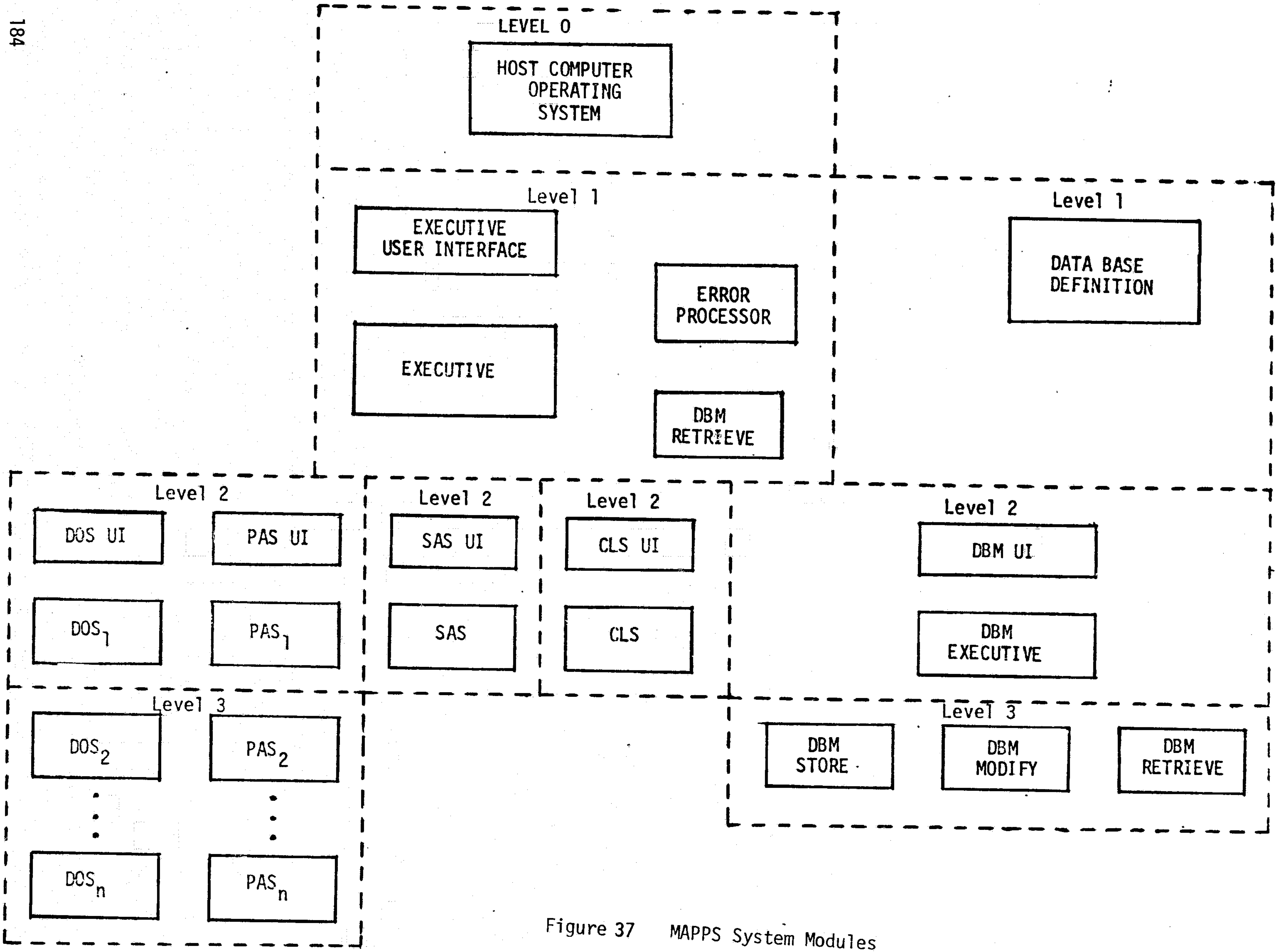


Figure 37 MAPPS System Modules

capabilities to be fairly uniform, although specific details and interactions may differ considerably. The following features are generally available to most timesharing computer systems:

- Security (restricted user access)
- System Use Accounting
- Checkpoint/Restart (system backup)
- On-Line and Batch User Access Modes
- Local and Permanent File Handling
- Editing Capability
- Higher Level Language Compilers (FORTRAN)
- Assemblers (host machine native language)
- Subroutine Library
- System Utility Library

The design of the MAPPS System will utilize these features as resident in the host computer system and not attempt to incorporate them in the MAPPS System itself. This prevents expenditures due to "reinventing the wheel" accumulating during the initial stages of the MAPPS Systems development. Some adjustments for the differences in host system capabilities may be necessary for implementation of the MAPPS System on a particular timesharing system, but the adjustment effort will be far less than if such features were actually part of the MAPPS Software.

9.4.2 MAPPS Executive Level

Level 1 is the primary level of the MAPPS System. Two distinct modules having separate functions reside at the primary level. One module consists of the Executive User Interface, the MAPPS System Executive, the Error Processor and the Data Base Manager Retrieve subroutine, and is oriented toward the execution of the analytic processes. The other module, Data Base Definition, is strictly concerned with initializing the system data base descriptions.

9.4.2.1 Executive User Interface

The Executive User Interface (EUI) provides the interactive and batch user with the means of invoking MAPPS analytic processes. The EUI provides for the communication to the system of essential administrative facts which activate the analytic processes. The EUI is the first point of contact the user has with the system.

9.4.2.2 MAPPS System Executive

The MAPPS System Executive controls subordinate module execution sequencing and maintains process integrity between successive execution of lower level (Level 2) analytic modules and/or the Data Base Manager. The Executive handles administration of operations for the rest of the various MAPPS System levels and invokes the Error Processor when appropriate.

9.4.2.3 Error Processor

If invoked, it is the primary function of the Error Processor (EP) to salvage wherever possible portions of the current effort. The EP is concerned with providing the interactive and batch MAPPS System user with suitable means to recover from input, output, and execution errors. In no way is the EP concerned with recovery from failures of the host computer.

9.4.2.4 Data Base Manager Retrieve

A copy of the Data Base Manager (DBM) Retrieve routine is shown residing at the Executive level in order to emphasize its availability to all execution levels of the MAPPS System. This feature is of particular importance whenever module overlaying becomes necessary to execute the system. The DBM Retrieve routine provides the means for acquiring information from the data bases.

9.4.2.5 Data Base Definition

The Data Base Definition (DBD) module exists solely for the purpose of defining data base files. It accepts user descriptions of file content and format, translates such information into data base language, and creates the internal mechanisms for storing information in the data base. The DBD program is maintained and executed independently of the MAPPS analytic system. The DBD program's use on Power Processing Master files will be limited to personnel with specific authority.

9.4.3 Operating Level

The secondary level (Level 2) of the MAPPS System is the actual operations level of the system. This is the working level where all of the analytic and the bulk of the data management activities are performed. The secondary level is comprised of Subprogram User Interfaces, analytic subprograms, and the Data Base Manager. Since it is probable that overlay loading of the analytic modules will be required in order to execute the MAPPS System, particular care must be exercised in the assignment of functions to the various modules at the secondary level.

9.4.3.1 Subprogram User Interface

The purpose of the Subprogram User Interface (SUI) is to provide the communication linkage between the user, the analysis programs, and the Data Base Manager. There will be at least one SUI for each Level 2 module of the MAPPS System. The extent of the functions performed by the SUI's will depend upon the purpose and activities of the respective module they service. Generally speaking, each SUI will have the task of assembling command, control and input parameters required for subprogram execution initiating subprogram execution, and validating successful completion of subprogram reiteration and for STORE, MODIFY, RETRIEVE functions of the Data Base Manager. Each SUI will invoke execution of the Error Processor as required.

9.4.3.2 Subprogram

The subprogram is the "work horse" of the MAPPS System. There are two basic categories of subprograms. One category includes all of the power processing related subprograms. The other category consists exclusively of data management related subprograms. The data management functions are discussed in separate paragraphs of this document. The power processing subprograms include those currently identified such as the following:

Design Optimization Subprogram,
Performance Analysis Subprogram,
Component Library Subprogram,
System Analysis Subprogram,

and those not identified, but which will undoubtedly warrant integration into the system as they are developed.

9.4.3.3 Data Base Manager User Interface

The Data Base Manager User Interface (DBMUI) performs the functions for the DBM that an SUI performs for a subprogram. It is this module that allows a user of the MAPPS System to interact directly with the Data Base Management Function, and hence the data base files, without invoking action from an analysis subprogram.

9.4.3.4 Data Base Manager Executive

The DBM Executive is tasked with the selection and execution of the subordinate data base functions such as Store, Modify, and Retrieve. It performs a security check for the function based on the origin of the request and the user identification. Failure to pass the check will cause a rejection of the request. If the check is positive, the Executive resolves the request into individual data base functions and sets those events in motion. Successful completion of requests results in the return of control as well as relevant information back to the module originating the request.

9.5 SYSTEM COMMUNICATION

The procedure proposed herein for communicating information within the MAPPS System supports the goal to maintain ease of modification and internal flexibility. It greatly facilitates error recovery procedures. It represents one of the built-in forces to promote programming convention standards and easily fits into the MAPPS concept of modularity.

There are two levels of communication each of which requires individual treatment. The first involves communication of command/control information and the second involves communication of data. Command/control information is used in the proper execution and internal sequencing of MAPPS System modules. Data is taken to be any information not used in command/control communication and which has computational implications in some aspect of a MAPPS System function (i.e., a MAPPS Subprogram).

The bulk of the communication between the various MAPPS System modules during execution will be through common memory areas. Since the programming language is to be FORTRAN, all reference to common areas is in the context of FORTRAN COMMON blocks.

Two kinds of common areas are each associated with Command/Control communication and Data communication. Command/control information passes primarily through Executive Common and Error Common, while Data communication deals with User Storage Common and DBM Common. Each of these common areas will be described in terms of its architecture, implementation, and its use.

9.5.1 Command/Control Communication

Figure 38 illustrates the command/control communication path for the entire MAPPS System. The basic media for communication of command/control information is expected to be FORTRAN Labelled Common blocks. The information expected to be transmitted through these Common blocks pertains to

- invoking execution of the various programs and subprograms
- relaying data storage area pointers
- maintaining error recovery and backtrace logic maps

and in general performing any other administrative and housekeeping chores required to insure system integrity during execution.

9.5.1.1 Executive Common Architecture

Executive Common (EXCOM) in a FORTRAN Labelled Common Block of memory cells having the principal function of providing a controlled and centralized vehicle for communicating command/control information. It is intended that EXCOM will be used to retain all information pertinent to I/O unit assignments, program and subprogram execution sequencing, error flags, common storage pointers and other information critical to proper execution of MAPPS.

Executive Common will be declared and initialized in the MAPPS Executive and will be available to all programs and subprograms in the system (Figure 39). During execution EXCOM will remain resident in memory and with the exception of certain cells will remain unchanged.

The MAPPS Executive will be responsible for monitoring the contents of EXCOM to insure its continual integrity and to invoke correct responses to subprogram requests and error conditions. It will be the responsibility of the subprogram programmer to use the executive common area; the content of which will evolve as MAPPS evolves.

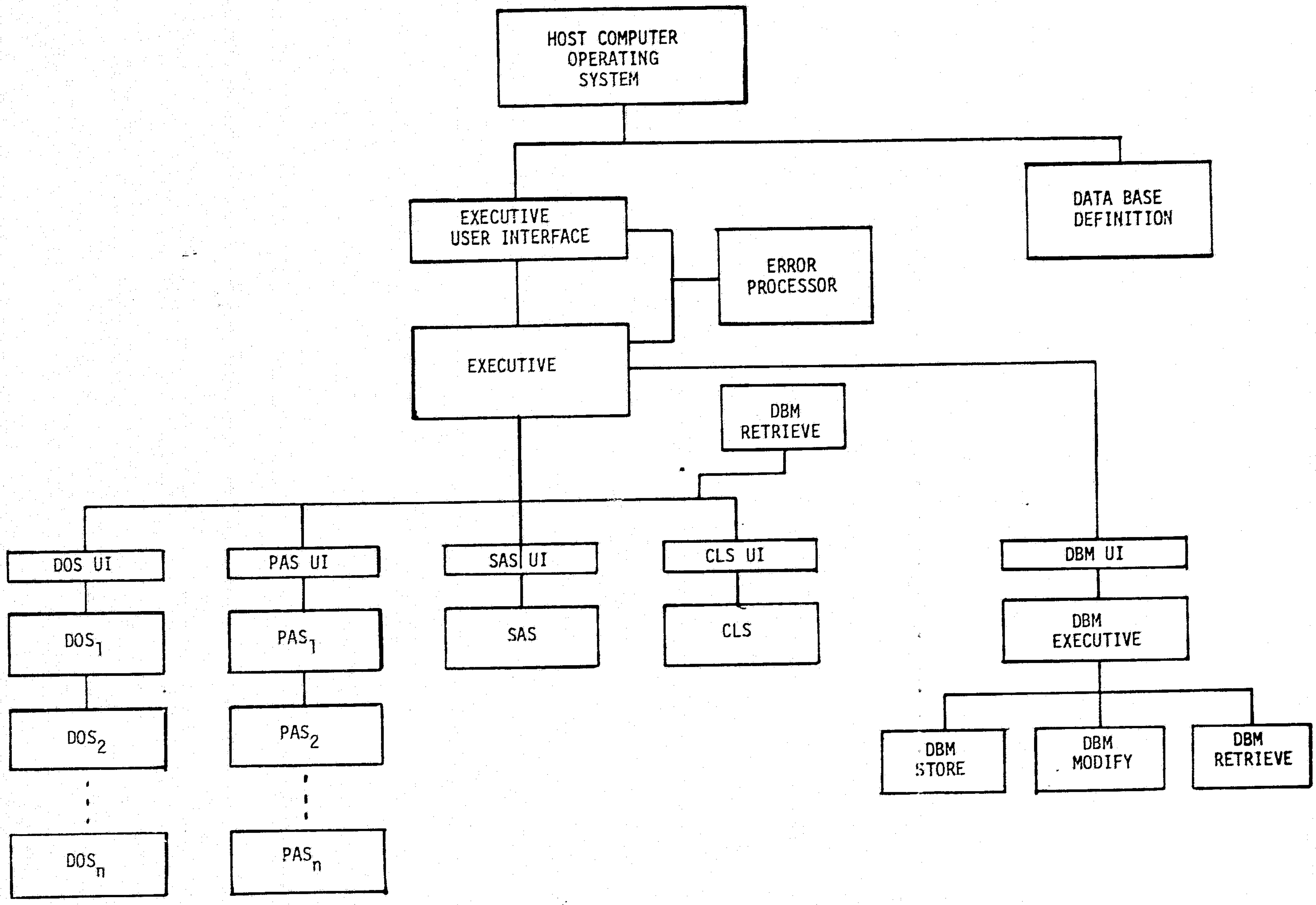


Figure 38 MAPPS Command and Control Communication

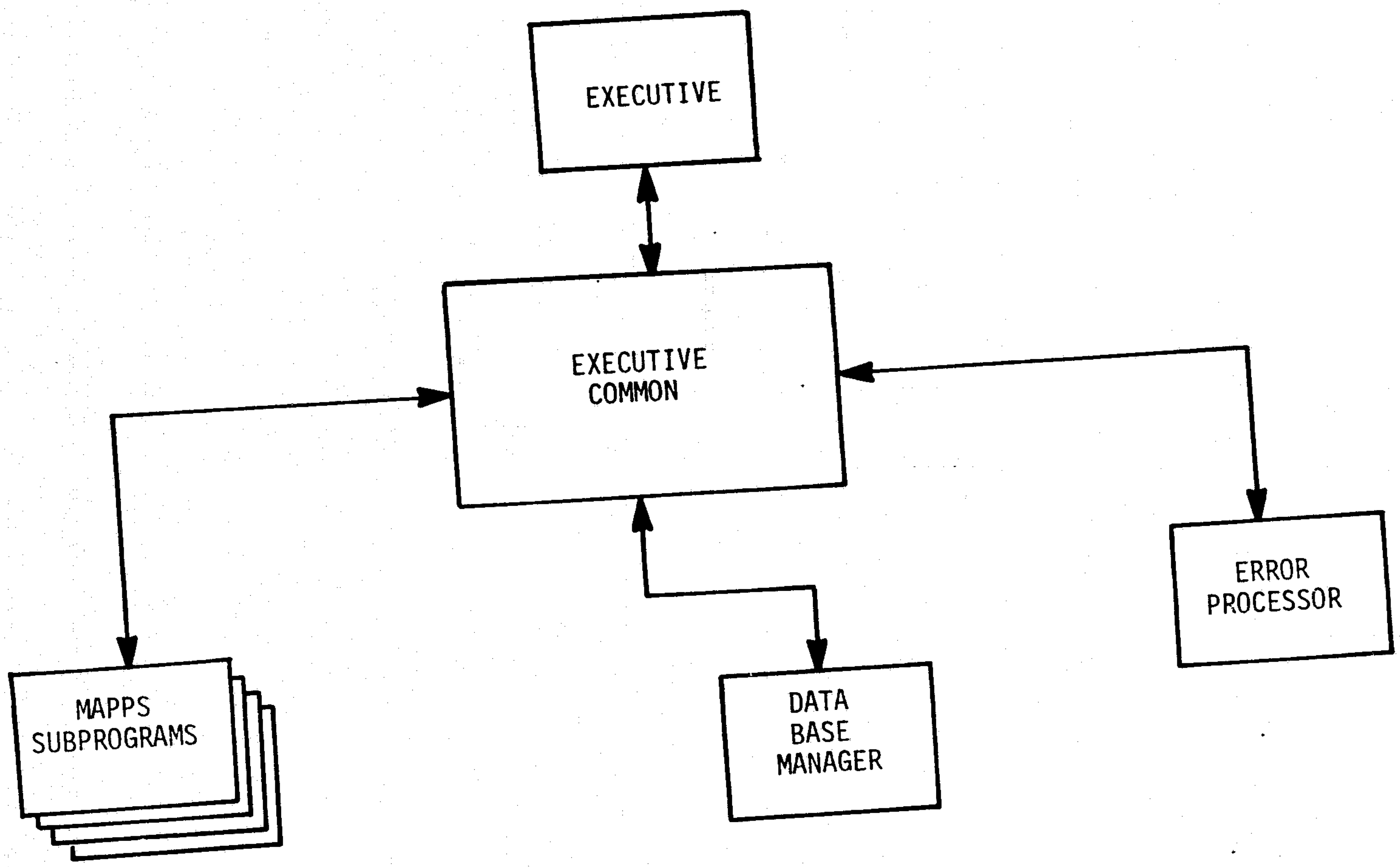


Figure 39 MAPPS Executive Common Communication

9.5.1.2 Error Common Architecture

The Error Processor (EP) uses areas in EXCOM to analyze the nature of a linkage error. However, it seems probable that in the course of dealing with errors, the EP will require some as yet undetermined additional data area to keep intermediate results before either resuming the session or terminating it.

The error common area requirements cannot be defined at this time but will develop as the detailed design of the EP unfolds. Initial reference to the Error Common will be in the DP, limiting its use to times when the EP itself is executing. It should be recognized that the EP will also use areas from EXCOM and User Storage Common to determine proper action and/or report the contents of data areas.

The Error Common Data Area will be used by the EP (Figure 40) for intermediate data access requirements in the course of analyzing and attempting to correct linkage errors within the MAPPS System. It is not anticipated that these items will have value beyond an individual execution of the Error Processor.

9.5.2 <u>Data Communication</u>

Figure41 is an illustration of the data flow paths between the data bases, the DBM, and the subprograms. In the illustration the "Intermediate Storage" refers to magnetic tape, disc and/or memory. Particular attention should be given to the types of data access available at each execution level. The limitation to retrieval only at the lower program levels is due primarily to the potential use of an overlay structure. Note that the Executive User Interface and the MAPPS Executive do not participate directly in the movement of data.

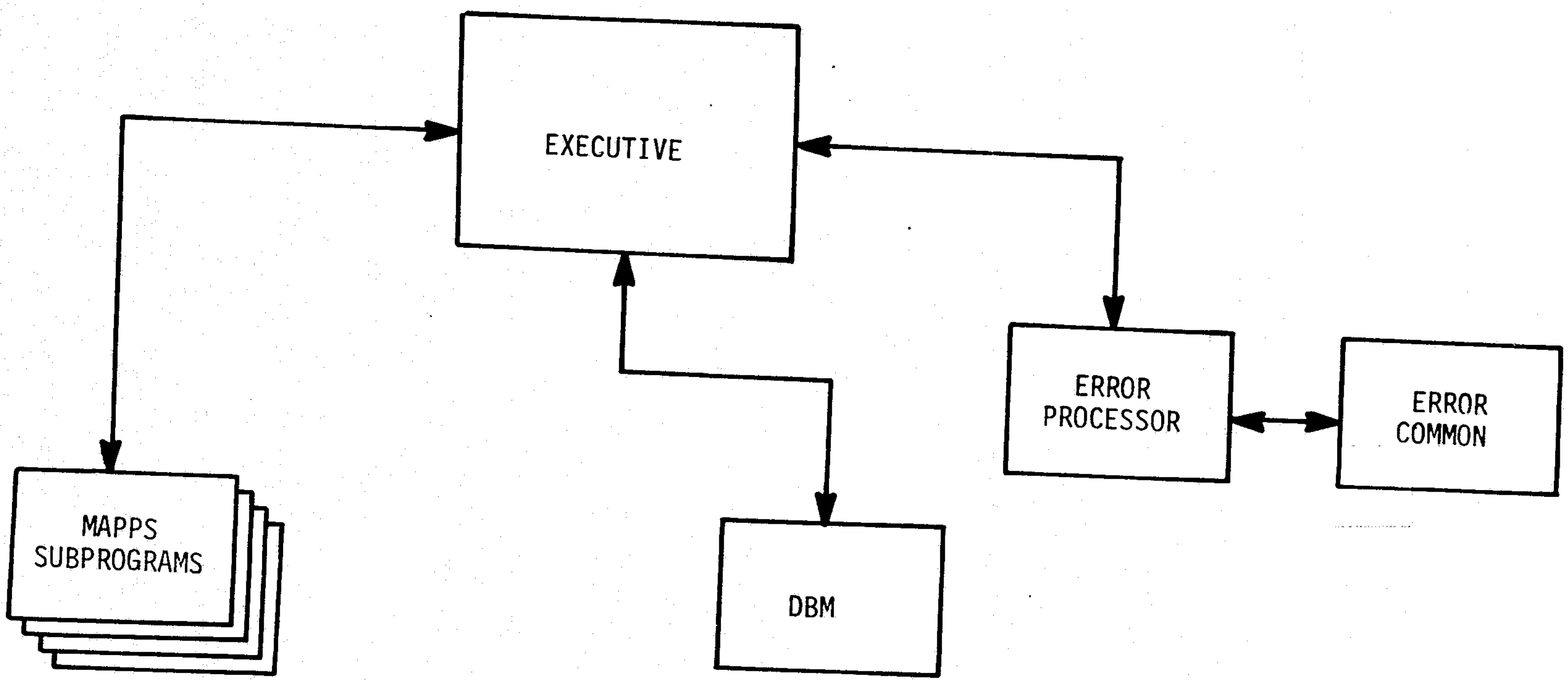


Figure 40 MAPPS Error Communication

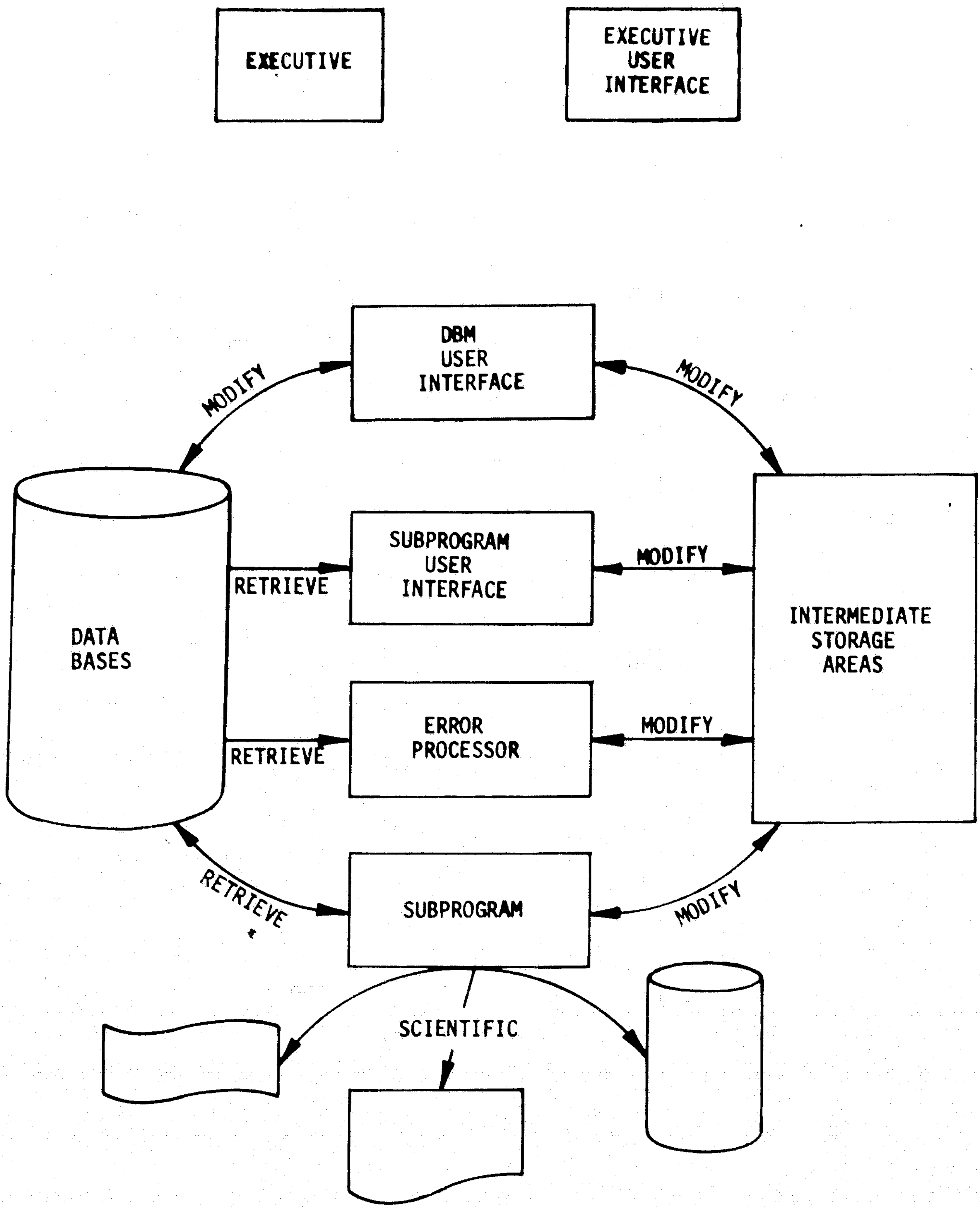


Figure 41 MAPPS Data Communication

9.5.2.1 User Storage Common Architecture

The User Storage Common area is designed to provide for the communication of analytic data throughout the MAPPS System. Two interdependent memory buffers constitute User Storage Common. One buffer is a directory of descriptive information about the second buffer which contains data values. The directory buffer will contain the data elements stored in strict accordance with the directory descriptors. Data elements may be single value or multivalue arrays and they may be in any legal FORTRAN format (integer, floating point, Hollerith, etc.).

Initial reference to User Storage Common will be in the MAPPS Executive. This insures its integrity and availability during all levels of MAPPS System execution. Of special importance is its availability during execution of error recovery procedures.

It will be the responsibility of the subprogram programmer to define the contents of User Storage Common. He must provide symbolic names, data element formats, space allocations (arrays) and the intended method of accessing the common area in the subprogram. It will also be his responsibility to code the subprogram with its own mechanism for accesses to the common area. Each Subprogram User Interface will be correspondingly modified to the subprogram programmer specifications. Actual definition of the directory buffer will occur in the respective Subprogram User Interfaces.

It is currently intended that a single User Storage Common Block be designated for use by all subprograms of the MAPPS System. Therefore, it will become essential to coordinate the element definitions with each and every subprogram accessing User Storage Common.

Since the User Storage Common is initially referenced in the MAPPS Executive and since it resides in memory, input/output access to it is available to all MAPPS System programs (Figure 42). It should be noted that only one User Storage Common area is contemplated and therefore coordination between subprogram requirements is mandatory. This approach is taken in order to facilitate communication between subprograms and to facilitate error recovery, as well as to minimize the demand for execution memory.

There are two methods available for accessing the common areas. Data accessing with directory reference is termed Variable Location. Data accessing without directory reference is termed Fixed Location. For reasons which will become apparent, the directory will exist and be maintained in either case.

Variable Location access requires scanning the directory, performing an element name match, and where a match occurs computing the location (i.e., subscript) of the corresponding data element in the data buffer. Fixed location access involves direct access to the data buffer with precoded subscripts. Use of the variable location scheme enhances flexibility while fractionally increasing execution time. Use of the fixed location scheme narrows flexibility, fractionally reduces execution time, and increases program modification effort.

User Storage Common may be filled with information in a variety of ways. In the subprograms it will be up to the respective programmer to determine the best approach. In the Subprogram User Interface three options will be available to the interactive user. The interactive user may request it be filled from a Data Base record which

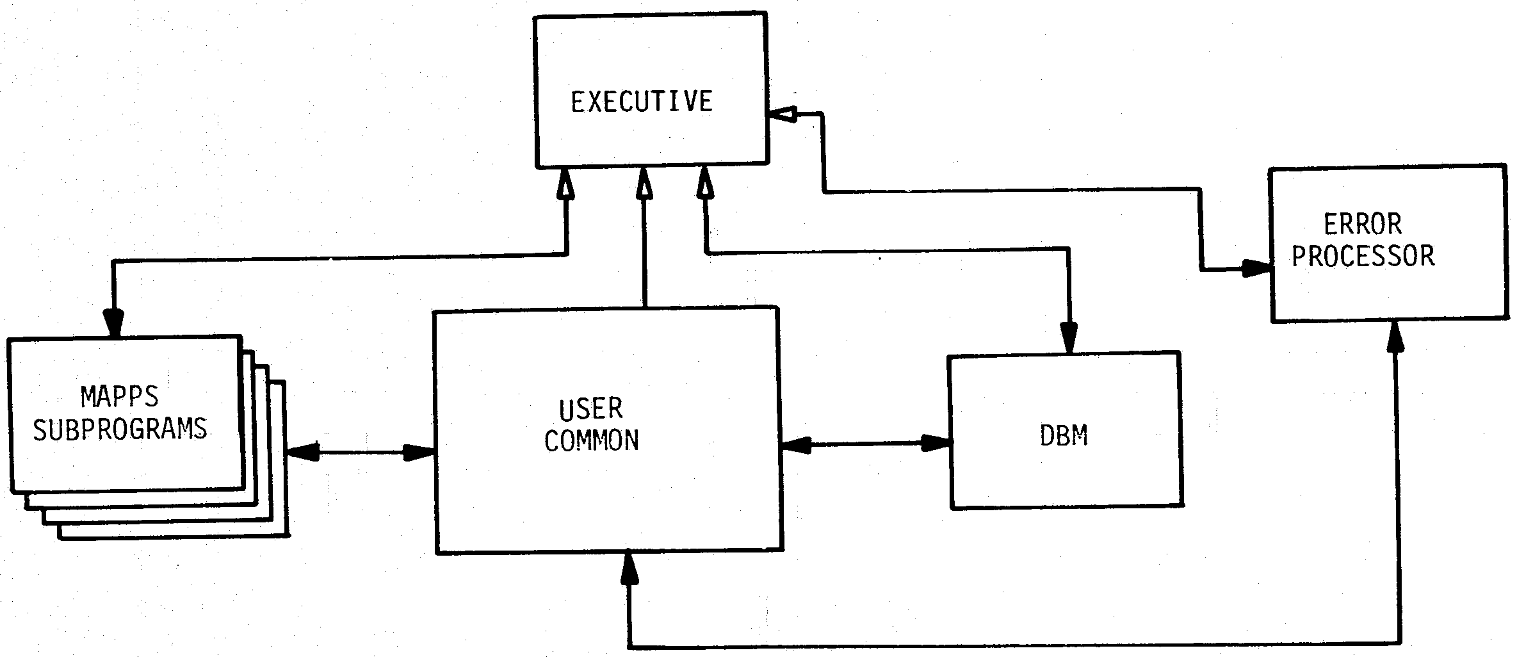


Figure 42 MAPPS User Common Communication

had been previously stored in a data base. He may also fill User Storage Common element by element through the terminal. He may also load a Data Base record and then modify specific elements.

The batch user will have two options for filling User Storage Common. He may load a Data Base Record or load an input record. In either case the information must be complete before execution of the subprogram or an involuntary termination could occur.

9.5.2.2 Data Base Management Common Architecture

Communication between other MAPPS System modules and the DBM takes place through the Data Base Management Common Data Area (DBMCOM). This area contains the various parameters needed for the RETRIEVE, MODIFY and STORE functions of the DBM as well as the data resulting from whatever DBM function was performed.

A number of parameters are required to gain full use of the DBM. These include items describing the data base file involved, its dictionary or schema descriptors and a number of other parameters which are shown in Appendix S.

DBMCOM is defined in all modules of the MAPPS System to afford all of them the ability to communicate with the MAPPS data base via the DBM module.

The MAPPS DBM module performs three basic functions: STORE, MODIFY and RETRIEVE. Such functions are available to other MAPPS System modules through a Data Base Action Request (DBAR).

The Executive handles the transfer to the DBM which validates the parameters in the DBMCOM. The DBM performs the DBM function, puts whatever output is generated in the

DBMCOM, and sets the Data Base Function Completion Code. Control then passes back through the Executive to the module which generated the request. (Figure 43)

The module then establishes where to begin processing and checks the Data Base Function Completion Code. Assuming a successful completion, the module now continues processing with the output generated by the DBM. (If an error does exist, the DP is invoked.)

It should be noted that the STORE and MODIFY functions result in the overhead of rolling out the requesting module, rolling in and out the DBM, and then rolling the requesting module back in. The RETRIEVE function (in a specific retrieval) is available to a requesting module without such overlay overhead as the RETRIEVE module is present at the Executive level and therefore does not require rolling in and out to satisfy the RETRIEVE function.

The above does not preclude storing or modification from any subprogram; it simply requires more overhead to perform these functions indirectly.

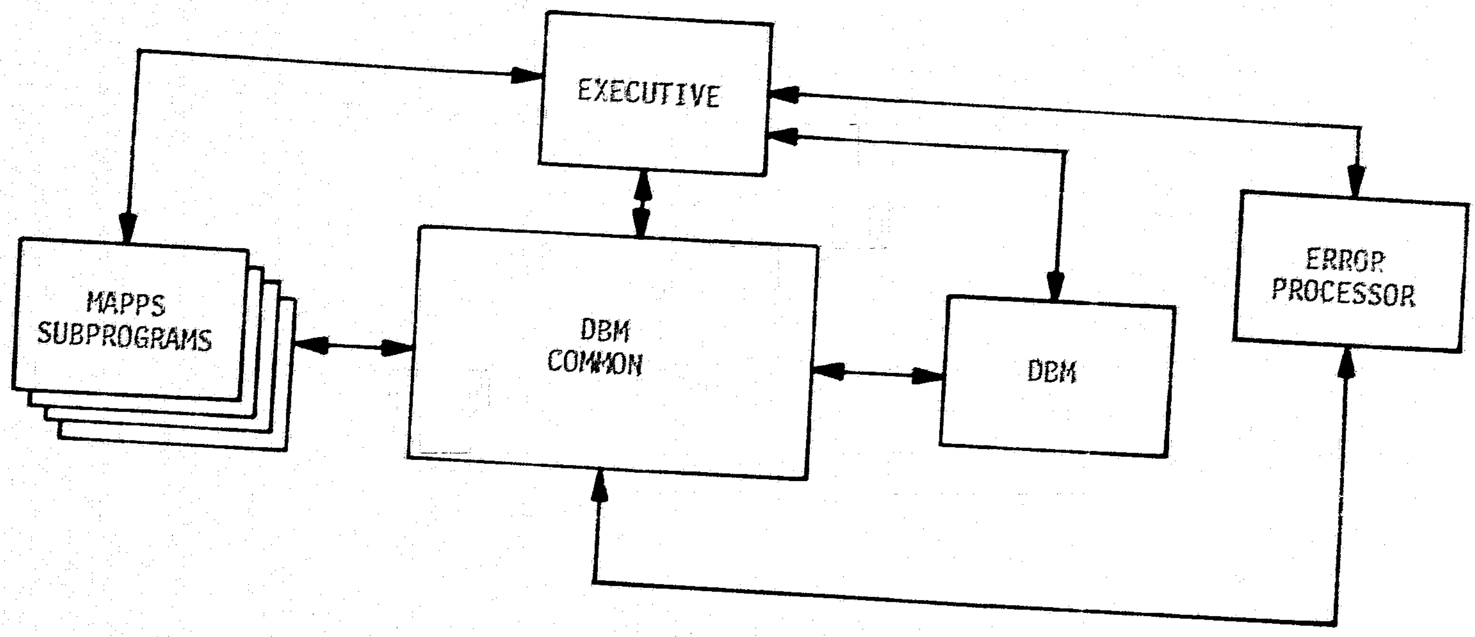


Figure 43 MAPPS DBM Common Communication

9.6 THE DATA BASE MANAGER

It is the primary function of the Data Base Manager (DBM) to provide the mechanism for the retention, maintenance, and retrieval of information pertinent to the MAPPS System. The DBM resides in the MAPPS System as a subprogram at the secondary level (Figure 37). Entrance of the DBM into the execution stream is accomplished directly by the MAPPS Executive and indirectly (through the executive) by the other subprograms of the system.

There are three activities performed on the MAPPS System Data Base by the Data Base Manager. These activities are performed by the three subroutines STORE, MODIFY, and RETRIEVE. STORE is a write function. Through the STORE routine, the DBM transports new data to existing data base files. MODIFY operations involve reading and writing. All DBM requests to change or delete information already contained in the data base are handled by the MODIFY routine. RETRIEVE is a read only operation. Requests for information contained in the data base are interpreted by the DBM executive, translated into retrieval language, and subsequently processed by the RETRIEVE routine.

9.6.1 Origins of DBM Request

Figure 41 illustrates the relationship between the MAPPS Subprogram levels and the DBM functions directly operable from those levels. The DBM can receive STORE, MODIFY, and RETRIEVE requests (direct or indirect) from the DBM User Interface, a Subprogram User Interface, a Subprogram, and the Error Processor. The MAPPS Executive and the Executive User Interface are not expected to issue DBM requests of any kind even though they could. A Subprogram and a Subprogram User Interface can make RETRIEVE requests directly without losing primary process control. They cannot, however, issue STORE or MODIFY requests directly. There are further limitations on RETRIEVES from lower levels which will become evident in a discussion on the forms of data retrieval. Of course the full powers of the DBM are at the disposal of the DBM User Interface and DBM Executive.

9.6.2 Information Storage

The actual process of storing information is the sole responsibility of the DBM/STORE routine. In order to invoke the store function, the DBM Subprogram must be loaded by the MAPPS System Executive for execution.

Although it will be possible to originate a store request in a Subprogram User Interface, it will only happen after the requesting program has relinquished control to the MAPPS System Executive. The procedure will be as follows:

- Move data to be stored to intermediate storage (i.e., DBM Common),
- Set the DBM/STORE request flag "ON",
- Save the data locator, and
- Relinquish control to the System Executive.

In all probability this procedure will be invokable with a single coded FORTRAN statement thereby relieving the analytic programmer of any administrative responsibilities.

It should be noted that a single request to store data may not produce a store function. Once the DBM Executive has been given control it will perform certain validity checks designed to protect data base integrity. Validity checks that are expected include, but are not limited to, identifying the user, identifying the data base and quality checking the data to be stored as to format and quantity. All errors will abort the STORE function and invoke the Error Processor for further evaluation.

9.6.3 Information Modification

The MODIFY process embodies the activities of the RETRIEVE process and the STORE process. Two MODIFY operations are provided to the user within the realm of the MAPPS System. These two options are Delete and Replace. Such other functions as text editing are to present the responsibility of the host computer operating system.

Since modification presumes existence of specific information requiring changes, the DBM response to a Delete or Replace request begins with a search of the data base to locate existing data. Under a Delete request, the resident information and all pointers to it are removed from the target data base. Under a Replace request, a substitution of the resident data by the new data is made. In either a Delete or Replace operation a full accounting is made to the user.

As with all data base write requests, the DBM executive will be extremely critical of MODIFY requests. Validity checks will be performed in order to prevent non-permitted users from altering a data base or to prevent erroneously formatted data from being written on the data base. All errors will abort the MODIFY operation and invoke the appropriate error process.

9.6.4 Information Retrieval

During execution of the DBM, information retrieval is expected to constitute the majority of DBM activities once the system becomes operational. The specific information retrieval function of the DBM is unique with respect to the other DBM functions in that it may be invoked at virtually every level of the system. This feature is made available because each subprogram is assumed to have need for retrieval access to the Data Base in order to perform effectively and is accomplished by attaching a DBM/RETRIEVE Subprogram to the MAPPS Executive program.

From the user viewpoint there are three ways to receive retrieval information as follows:

- External Display
- Memory Storage
- Mini-Data Base

Although each option is illustrated (Figure 44) separately, it does not preclude the possibility of simultaneous occurrence of two or all three options with a particular retrieve operation. The forms in which

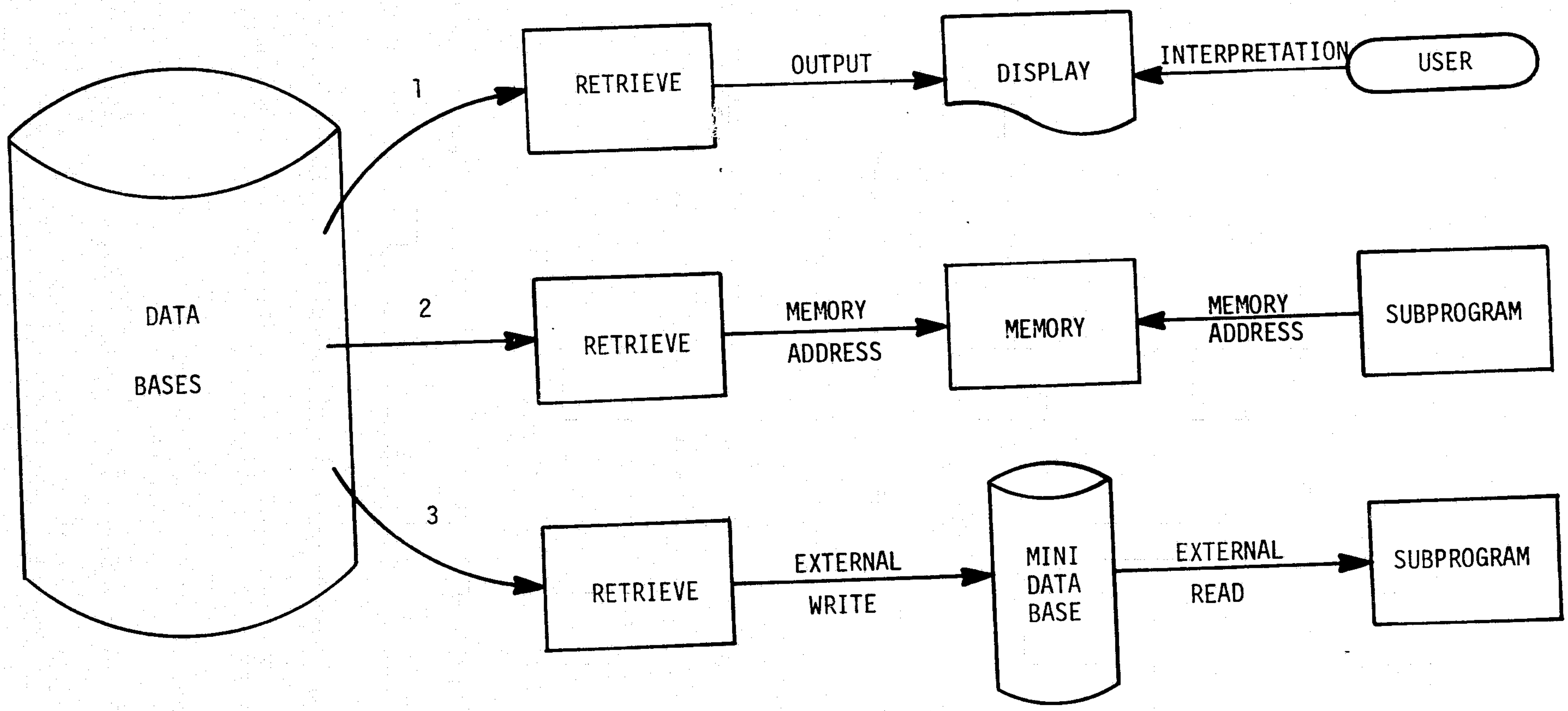


Figure 44 MAPPS Retrieval Data Flow Options

retrieved data may be received are illustrated and discussed separately because their respective use requires differing techniques.

Retrieval to external display requires user evaluation of the display and subsequently user action to cause employment of the retrieved data. The external display device could be a CRT, terminal printer, or line printer. Information displayed could be data, quantitative or qualitative messages, or both data and messages. The choice will be the user's and subject to the hardware capabilities of the host computer.

Retrieval to memory storage is special in that a predetermined scheme must exist for using the stored information. Predetermined implies programmed knowledge of the whereabouts of the data. There are two possible ways of handling memory storage of data; they are FIXED format and VARIABLE format. Discussions and comparison of these formats is in the Section for User Storage Common Arcitecture.

Retrieval to a Mini-Data Base involves creation of a condensed version of the original data base. The objective is to reduce the volume of information for immediate access through conditional retrieval operations. The Mini-Data Base is identical in format to the master from which it is derived and therefore requires no special access methods beyond DBM Retrieve.

Retrieve requests are classified as Specific or Conditional according to their form and the results they produce. Specific Retrieve requests are made to obtain restricted quantities, usually single values of particular data elements required for the immediate analytic operation. Use of the specific form requires explicit knowledge of the format and quantities of values returned. Specific requests will find their greatest use at the subprogram level. Conditional Retrieve requests generally produce a variety of values and require specific treatment before use in an analytic process. Conditionally retrieved data will normally be to intermediate storage and to display for further scrutiny. Conditional Retrieves will be used most often in the Subprogram User Interface and not in Subprograms.

During execution of the MAPPS System, combinations of the Conditional Retrieve and the Specific Retrieve may be employed in the process of obtaining information from the data bases. Figure 45 illustrates one example of interaction between the user and the MAPPS System using Conditional Retrieves to reduce the quantity of information retrieved prior to execution of a subprogram. The Conditional Retrieve will cause a copy of the information satisfying the requestors range of conditions to be transferred to DBM Common or similar intermediate storage. The user at his option could request that the retrieved data be displayed for observation or if the quantity of data retrieved was excessive, he could further restrict the conditions and execute another Retrieve. The form of the statement (program coded or English language) for requesting conditional retrieve will provide the user with the ability to conduct searches of the data base looking for items satisfying such conditions as "less than," "greater than," "equal," "not equal," and other conditions deemed useful to users of the system.

The purpose of the Specific Retrieve is to give the Analysis programmer the facility for coding data base access into his analysis program. The form of the Specific Retrieve statement will allow the user to code data base requests using element names with confidence in the fact that specific quantities of only named elements will be retrieved. Generally, all Specific Retrieve request communication will be through arguments of a FORTRAN Call statement.

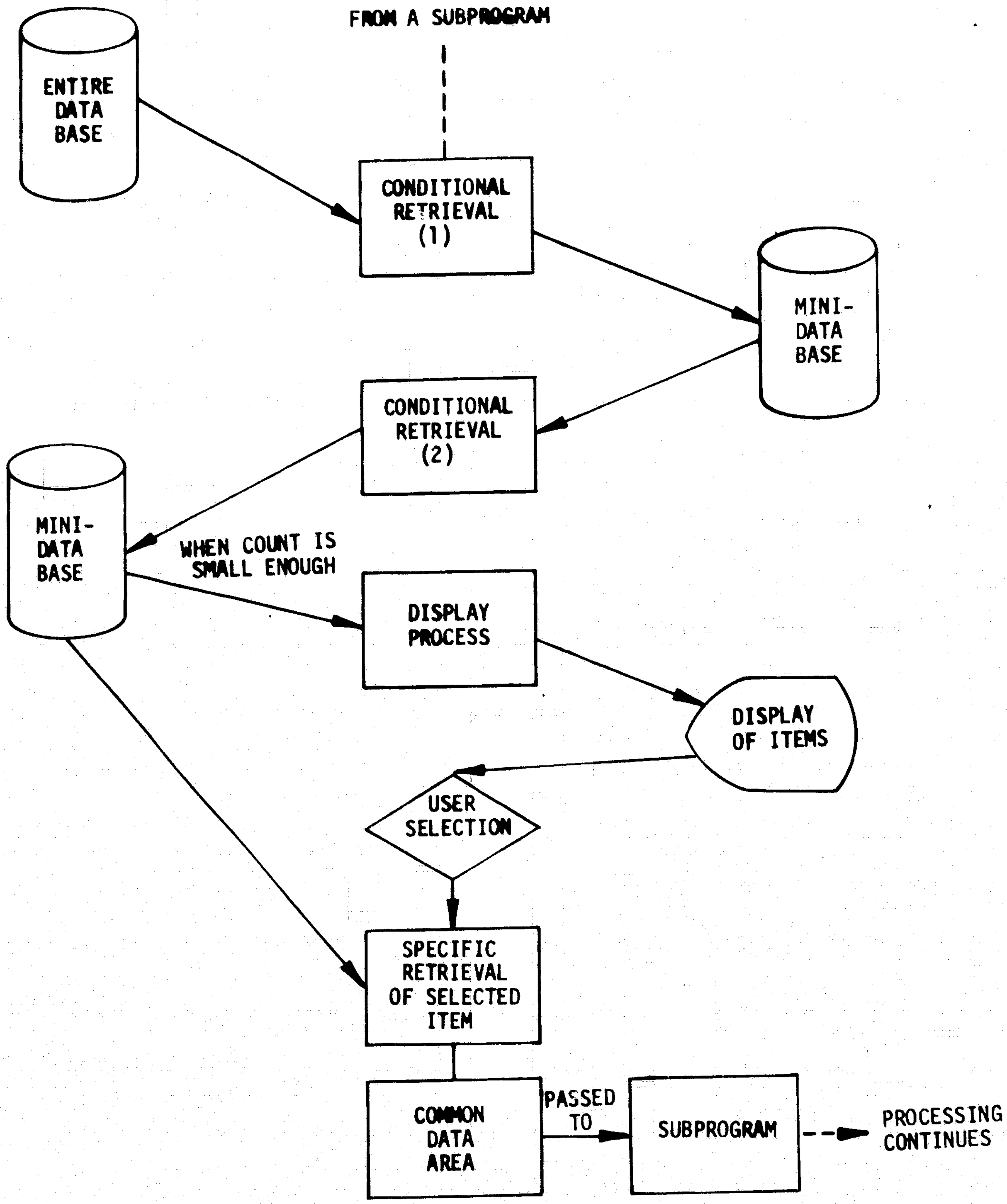


Figure 45 MAPPS Conditional Retrieval and Iteration

9.7 MAPPS SYSTEM OPERATION

The operational MAPPS System consists of three physical divisions:

1) the load modules (or compiled programs) that comprise the MAPPS Executive, DBM Subprograms and other MAPPS processors

2) the basic data base files required by all users, and

3) the individual data base files created and accessed by the user.

The MAPPS program/subprogram modules will reside in a library in the timesharing computer system. The MAPPS System data base files will reside on external input/output devices (disk or magnetic tape).

Both batch and interactive operation of the system is contemplated. It is anticipated that the interactive mode will be in greatest use. User Interface modules have been judiciously placed throughout the MAPPS System to insure effective interactive communication between the user and the system. The network of User Interface Modules includes the Executive User Interface (EUI), the Data Base Manager User Interface (DBMUI), and the Subprogram User Interfaces (SUI). Each User Interface module has its special purpose to satisfy.

The EUI is the point of initialization. It is through the EUI that the user has the first opportunity to communicate commands and requests to the system. Directives are issued which enable specific execution sequencing, connecting of data base files, establishing execution options, and determining error procedures.

The DBMUI gives the user the capability to work directly with the DBM exclusive of the other subprograms. The prime responsibility of the DBMUI will be to receive English language (external) statements, translate the statements to internal program commands and instruct the DBMI accordingly.

Each SUI will interact with the user on matters concerning its respective subprogram. Through it the user will be able to input control and analytic data, specify execution options, establish input data file pointers and generally control events within the subprogram.

To converse with the MAPPS System (Appendix T), the user signs on the timesharing system and then executes the MAPPS program. This is accomplished by retrieving the MAPPS modules from the library, attaching the data base files, and then loading and executing the MAPPS program modules. Activation of MAPPS leads to a conversation between the system and the user, first about which function of the system is wanted, and then the dialogue with the part of the system that actually performs that function. Varieties of exchanges of parameters and results take place with the user ultimately ending the session and storing either intermediate or final results of a design. The results are stored in the User Data Base File which can be recalled from the user's account files and accessed for reference at another time.

In the course of a terminal session, or "conversation," the system may recognize that a particular function will be excessively time consuming. It notifies the user and gives him the option of either continuing to process on-line or of setting up a remote batch job to accomplish the function while the user does something else. User requests may also generate listings of various data base files.

The MAPPS System will be sufficiently flexible to allow a sophisticated user to shortcut steps that are not needed because of the user's in-depth knowledge of the system. The new user will be presented with informative messages as processing goes forward and will also be able to retrieve some instructional text to clarify options at decision points.

Even though a Subprogram User Interface is planned for each subprogram installed in the system, it is not currently planned to have this interface supplant any of the already existing activities of the subprogram itself. The intention is for the SUI to merely supplement existing subprogram functions at the administrative level. This especially applies where the subprograms already exist as "stand alone" programs. Figure 46 illustrates the division of responsibility for inputing analytic data to a subprogram.

In the TRW/TSS, individual user-created data base files would reside on the individual user's account and be accessable only by that user unless the user gave specific permission via commands to TSS for another person to either read or write that file (or perhaps read and write). This is protection at the file level and external to the MAPPS System. Internal checks are also available in MAPPS for the protection of user files. When the DBM is directed to perform any data base function on a data base, it looks at the user's unique identification and determines if the requested function should be performed. If not, a diagnostic message will be issued to the user and the data base function not performed.

9.8 MAPPS SYSTEM PERSONNEL

Besides the Designer-Analyst user of the MAPPS System, there are two other categories of support personnel involved with the system. They are the Data Base Administrator and the Computer System Support personnel.

The Data Base Administrator is a person who is knowledgeable of the requirements and functions of the MAPPS System. This person maintains the MAPPS basic data base files such as the Component Library and the System/Equipment files and assures that the MAPPS

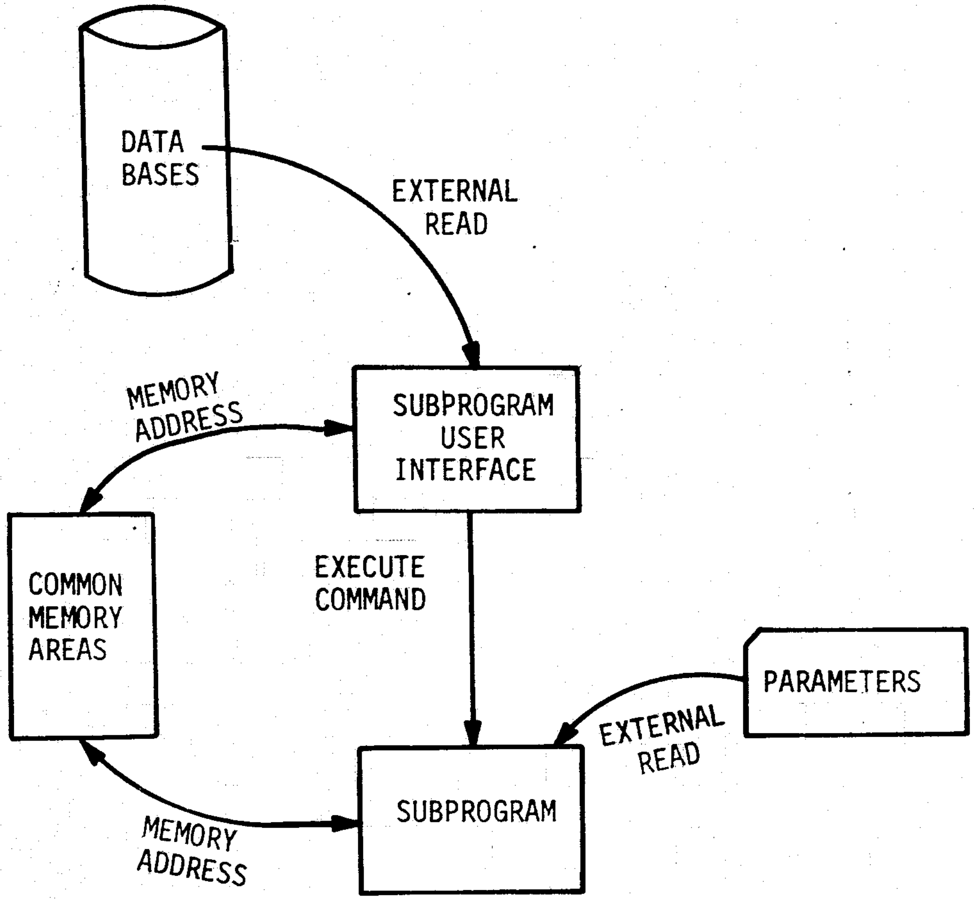


Figure 46 MAPPS Subprogram Communication Scheme

modules are available for use. This person may also be responsible for maintenance of parameterized security permissions internal to MAPPS.

The Computer System Support personnel are responsible for the maintenance and operation of the computer operating system under which the MAPPS System runs. They perform programming, operation and data base administrative tasks for the timesharing system as a whole.

Designers who wish to trade results back and forth may do so on the individual level or possibly by incorporating their results in the MAPPS General System/Equipment Data Base File. This last would be done through the Data Base Administrator in accordance with established regulations.

9.9 ERROR PROCESSING

An important aspect of the design of the MAPPS System is its handling of errors that occur in the course of a session with the user. Errors may result from abnormal conditions in either hardware or software.

Hardware errors concern themselves with the mechanical and electronic equipment of the host computer system, including the computer main-frame, the various peripheral devices attached to it, and the terminal utilized by the user. Hardware malfunctions will not be the responsibility of the MAPPS System Error Processor. Errors occurring in the host computer operating system are also outside the realm of the MAPPS System Error Processor.

Software errors result from the incorrect processing of data which may be due to the program accepting invalid input data or incorrectly operating upon valid input data. In a complex system like MAPPS, software errors may occur at several levels:

User/System Interfaces

- Subprogram
- Subprogram User Interface
- Executive User Interface

Inter-MAPPS Interfaces

- Between any two modules that have an interface (common memory area, file)

Errors at the User/System Interfaces will be dealt with in most cases by the Interfaces themselves. The programs accepting data from the user in the form of parameters, indications of decisions, etc. are responsible for making checks of validity and producing diagnostic messages to the user when the input is incorrect. A considerable effort will be spent in ensuring the sufficiency and correctness of the validity checks at the user interfaces.

Most errors in the interfaces between MAPPS modules will be removed in the debugging process. An Error Processor will be available to respond to certain types of errors and to provide a programmed means of attempting recovery. If recovery is not possible, the Error Processor will attempt to save whatever information it can for the user and for later error diagnosis before shutting down MAPPS System execution.

In the case of a sophisticated timesharing system such as TRW's TSS, the resident error processing routines and administration procedures provide an excellent degree of confidence by the user in being able to run his problem when he wants to. Hardware errors also fall within the boundaries of the resident system error processing routines. These usually require the re-execution of a problem using the data saved in the checkpoint procedure most recently performed to get a full backup of the system at that time. These checkpoints are normally taken at hourly intervals or every two hours. Thus, in the event of a catastrophic system failure, the user would lose what information was in memory and have to back up to the previous checkpoint.

If intermediate results had been stored in the MAPPS permanent data base files since the beginning of the session the user would most likely be able to retrieve them and start from that point as the permanent files are not very often disturbed in hardware malfunction situations.

The Error Processing (EP) module is provided for the purpose of evaluating MAPPS System execution errors and conducting a conversation with the user regarding potential solutions to the problem, providing that the problem is not catastrophic. In catastrophic situations the EP will take its own action in the most expeditious manner possible.

The Error Processing module is invoked by the Executive when it determines that an error in the control flow has occurred. This would most likely be an anomalous condition existing after a nested return of control or other condition affecting the manner in which the Executive normally handles control flow. The Error Processor will attempt to salvage the operation, but if not able to will attempt to maintain the conversation with the user. In the event that even this is not feasible, it will attempt to allow the user to save whatever intermediate results were obtained prior to the EP ending the terminal session.

10. CONCLUSIONS ON MAPPS, PAST, PRESENT, AND FUTURE

10.1 MAPPS BACKGROUND

Being a long range program, the MAPPS is currently at the conclusion of its initial Phase-II effort. The Phase-I program started in 1973 amidst a growing concern from both the government, the industry, and the university regarding the need for and the lack of such a program. The prevailing feeling at that time was that although there already had been numerous circuit developments, too much reliance had been placed on design experience, trial and error, and occasional brute force, that too much emphases had been focused on "it works" rather than "how and why it works", and that these semi-intuitive and design-by-the-bench approaches often placed cost/schedule in peril. The MAPPS objective, therefore, was to provide the needed modeling and analysis tools to reduce the design, analysis, and development time, and thus the cost, in achieving confidently the required performances for power processing equipment and systems. Since then, the significance of this objective has been enhanced by the evolving trend of power processing. First, the trend of higher power has diminished the readiness of the "bench design". Next, growing sensitivity to cost and the consequent standardization effort has placed more and more emphasis on an analysis-based design.

Power processing, by nature, is harware-oriented. Transient-prone semiconductors, insidious magnetics, evasive noises, and ever-changing equipment requirements, all seem to overshadow the subtle need for, say, control-loop analysis or power-circuit design optimization. Understandably, a designer in real life is too occupied to have that much time to dwell in modeling and analysis. After a few years in the industry, a designer becomes too valuable in producing the required hardware within the specified cost/schedule, with the consequence that usually one (or a few) analyst in a given organization ends up performing advanced analysis for all other engineers.

This distinct division between hardware and software can be costly for the following reasons:

- Due to their casted role, the analysts only analyze the design already generated by the designer, which may happen to be quite marginal to start with. Modifications recommended by the analysts may have surfaced too far down stream in the hardware unit development and testing; they often are tacitly disregarded, only to find that the marginal design to manifest itself later, causing even greater anguish in the final system integration testing.

- The analysts, working toward the improvement of certain specific circuit performances, may recommend changes that are experimentally revealed later to be detrimental to other performance characteristics, thus motivating further changes. Such long-period, costly vicious cycles of design iterations are not uncommon in the hardware development. How much it will be better, then, if one can combine analysis and design into one task, and do it right by the designer/analyst the first time.

10.2. MAPPS EMPHASES AND TWO DIVERSIFIED VIEWPOINTS

Accepting the premise that the designers are the backbone of the industry, and on whom the major benefits of the MAPPS program should fall, what remains to be seen is how should a program like MAPPS proceed in order to reach this intended goal. To this end there have been different schools of thoughts:

(1) The first school of thought rightfully asserts that a designer has to base the design on certain information gained from modeling and analysis, preferrably in the closed-form equations or insight-producing equivalent circuit models. The primary thrust of the MAPPS program should therefore be tutorial in generating, assembling, and disseminating the analytically-based, design-oriented information. A designer can then utilize this information to his advantage, and apply it to the specific applications as required.

(2) The second school of thought regards the primary thrust of the MAPPS program as the generation of analysis-based, design-oriented, computerized subprograms, which the users can readily adopt for solving the specific problems at hand. The designers look to these subprograms as ever-helpful and trustworthy working partners; it matters little to the designer that they really do not quite understand their powerful partners as long as the partners consistently deomonstrate the abilities to perform the needed design and analysis functions.

The validity of the first school of thought is beyond any dispute. An analytically-based design, well understood by the designer, is the ultimate design. The only attendent asumption is that the designers, confronted by all their semiconductor-, magnetics-, noise-, and specification-related hardware concerns and occasionally their own modest modeling, analysis, and computational backgrounds, are still sufficiently energetic and resourceful to comprehend and to skillfully apply the analysis and the analytically-based design information. This assumption becomes particularly vulnerable when applied to a more complicated problem in which closed-form representations and high-order equivalent circuits are generally inapplicable.

The strength of the second school of thought is derived from the fact that it can be very practical, particularly for complicated designs of highly-nonlinear origins. User's confidence toward the "subprogram partners" can be readily enhanced with a few applications, and the subprograms become ultimate engineering tools. However, there is a serious weakness inherent in this relationship. The subprograms, being numerical by nature, must be centered on a given circuit configuration based on which computerized subprogram analytical routines are generated and executed. Consequently, the circuit configurations or the problems implemented in the subprograms must be well standardized and suited for a multitude of users. Otherwise, individual subprograms will have to be custom-made for individual users to handle specific design/analysis applications.

10.3 MAPPS MODELING AND ANALYSIS EFFORT SUMMARY

Recognizing the merits and limitations of the two diversified thoughts, and realizing that the MAPPS program should not regard one with favor over the other, the modeling and analysis efforts conducted so far have been encompassing these diversifications. These efforts are summarized in the four major categories shown below. Notice the component library effort is not included here, as its nature is by no means related to the modeling and analysis of power processing systems.

- Control Performance Analysis
- Control Circuit Design

- Power Circuit Design Optimization
- System Analysis

To make MAPPS easy for a designer to use and to release the user's need for an extensive knowledge of computer systems and programming, an expandable Data Management Program is also implemented to coordinate all subprograms and their respective user interfaces.

10.3.1 Control Performance Analysis

The control performance analysis includes the discrete time-domain analysis, the impulse function analysis, the average time-domain analysis, and the discrete time-domain simulation.

The discrete time-domain approach provides the most accurate small-signal analysis. A step-by-step analysis procedure is clearly described to fulfill the tutorial objective of the MAPPS program. From this procedure, a user with the proper background can hopefully adapt the analytical approach to a specific problem at hand. As for subprogram generation, a multiple-loop control circuit configuration, developed in another NASA program and intended for future regulator control-circuit standardization, is used. The subprograms cover both the buck and boost power stages. In the buck regulator, both continuous and discontinuous conduction are handled in a single subprogram. Consequently, the two previously-described diversified schools of thought are all practiced in the MAPPS program in the area of the discrete time-domain analysis. In the immediate follow-on phase, three different subprograms will be completed, one for each of the buck, boost, and buck-boost power stages. Each subprogram will incorporate continuous and discontinuous inductor-current conduction modes, and will contain the aforementioned standardized multiple-loop configuration using various duty-cycle control methods.

The principle of the impulse-function approach is described, which provides as an end result the transfer function between the input duty-cycle signal and the output of the power stage. For both continuous and discontinuous conductions, conventional frequency domain transfer functions are generated for all three basic power stages, and can be easily adapted for regulator small-signal analysis. However, the lack of a complementary line-input-to-power-stage-output transfer function has hampered its utility. Further work in this area is not planned in the immediate follow-on phase.

The average time-domain analysis is the subject of another report, prepared by CalTech under a subcontract to TRW. The powerful canonical models generated by this approach for all three basic power stages are slightly modified into a dual-input (line and duty-cycle) power stage transfer functions in the conventional frequency domain, which can be readily adapted by a user. In conjunction with the linear analog signal processor and the linearized digital signal processor (via describing function), the control-dependent performances of a complete single-loop controlled regulator can be analyzed, almost routinely. Since there is a lack of the so called "standardized" single-loop analog and digital signal processors, no subprogram based on the average time-domain analysis is generated for the single-loop control. The application of the average time-domain analysis to multiple-loop control is currently the subject of another NASA program, NAS3-20102. There, the intimacy existed among the power stage, the digital-, and the analog-signal processor requiring a slightly different dual-input transfer block diagram for the complete regulator. In the next MAPPS follow-on program, results obtained from NAS3-20102 will be implemented in subprogram form for the standardized multiple-loop control. Again, the two aforementioned schools of thought are thus practiced in the MAPPS program in the area of average time-domain analysis.

The discrete time-domain simulation is a straight forward extension of the discrete analysis. Details of switched-interval propagation through the state transition matrices are outlined, and the computer iterations clearly described through examples of flow charts. Subprograms based on the aforementioned standardized multiple-loop control are generated to demonstrate the large-signal performance simulation such as the regulator stability-in-the large (startup) and the regulator responses to severe line/load step changes, thus fulfilling the tutorial as well as the application goals originally intended. With the simulation methodology and its cost-effectiveness vividly demonstrated, no definite simulation project is planned for the MAPPS immediate follow-on phase.

10.3.2 Control Circuit Design

Instead of analyzing the control-dependent performances, the essence of the control circuit design goes one step further, i.e., it allows one to perform a control-circuit design based on a given set of control-dependent performance specifications. Through an example on the single-loop basic buck regulator design, the essential design procedure in order to meet a given stability-related requirement is tutorially demonstrated and reduced to practice through a control design subprogram, which not only identifies asymptotically the needed lead/lag compensation, but also performs design synthesis of a given compensation network configuration to numerically determine the related control-circuit parameters. In the next MAPPS program phase, the control design will be extended to show how other performances such as audiosusceptibility and output impedance can be included in the control design procedure. Furthermore, control design based on results obtained from the aforementioned program of standardized multiple-loop control will be incorporated as control design subprograms, thus again satisfying the intended tutorial and application roles prescribed for the MAPPS program.

10.3.3 Power-Circuit Design Optimization

The design optimization pursued in the MAPPS program represents the first serious attempt by which an act of optimization is introduced into the power converter design. While the pioneering effort has been somewhat agonizing, its return is certainly gratifying. First, a design optimization methodology relating power-converter design requirements, design variables, and design constraints is tutorially developed. Based on this methodology, various mathematical and computational techniques are selectively applied to several practical power-converter design-optimization problems. The Lagrange-multiplier method is applied to magnetics design optimization, from which novel design equations are derived for optimum-weight and optimum-loss inductors and transformers. These design equations are assembled into separate design optimization subprograms to free a designer from tedious computations, thus again adhereing to a balanced tutorial and application program objective. For more complicated problems for which closed-form solutions are impractical, nonlinear programming optimization routines are used to seek out the optimum design numerically. In these endeavors, detailed design equations are given, and the specific nonlinear programming codes and program listings are provided. The most elaborate design optimization undertaken in the MAPPS program has been a complete buck converter including an input filter and containing twenty-three design variables, which has been reduced into a practical design optimization subprogram. In the immediate follow-on phase, the design optimization will be extended to include the complete boost and the buck boost power converters. This is perfectly suitable for subprogram generations, for the three basic power stages are universally-standardized circuit configurations.

10.3.4 System Analysis

In terms of system analysis, the numerically-oriented subprogram approach is more sensible, as even the least complicated system is likely to defy a purely analytically-based design. Since a power processing system is comprised of a multiple of interconnected power processing equipment, the system analysis is naturally related to the subprograms generated for equipment performance analysis and/or design optimization. In the MAPPS program, a 12th order regulator system is simulated for its startup characteristic thus demonstraing the feasibility of applying the cost-effective discrete time-domain simulation to large-scale power systems. A source-converter system is also successfully investigated for total system weight optimization, which identifies the optimum converter switching frequency as well as the optimum converter efficiency that will give an optimum system weight for a given source density (watt per grams). How much system analysis effort will be expended in the next follow-on depends primarily on the level of support; the best chance for engaging in extensive system analysis is for one of the NASA dedicated future missions such as the electric propulsion system and/or the direct-broadcast communication power system, for which the payoff of conducting system analysis can be well justified.

Thus, the present and immediate future MAPPS efforts have been briefly summarized. One aspect of MAPPS subprograms that repeatedly reinforcing itself is the need for "standardization." Aside from being obviously cost-effective from the viewpoint of hardware development and production, the standardization also enables the utilization of the most effective analytical approach for conducting performance analysis, control-circuit design, power-circuit design optimization, and, to a certain degree, system analysis. Purely from an analytical viewpoint, the validity of the current trend for standardization is thus enhanced.

10.4 CONCLUSIONS

To anyone working with switching regulators, converters, and systems comprised of these equipment, certain design and analysis intricacies inevitably make themselves felt throughout the equipment and system design and development stage. Empirical and intuitive reliances often intercede with the designer's desire to be "more scientific" and his commitment of being "on schedule". Handicapped by a general lack of established modeling, analysis, design, and optimization tools, it has not been uncommon for a power processing designer to face the perplexing situation of not being able to fulfill any of the desire or the commitment.

The cost/schedule plights that most equipment and system designers find themselves in, have to do with at least one of the following entities: weight/efficiency, performance requirement, and trial-and-error design iterations. While power processing as a technology has reached the level of sophistication where the modeling, analysis, design, and optimization of these entities should have been well established, a survey of literatures conducted at the initiation of the MAPPS program had proved the contrary. Needless to say, such inadequacies inevitably lead to weight/efficiency, performance, and cost penalties. In addition, the recent evolving trend of higher power and equipment standardization has further heightened the need for analytically-based design and optimization.

It is therefore the expressed objective of the MAPPS program to provide analytical engineering tools to enable conceptual design and tradeoff studies and to reduce the design, analysis, and development time, and thus the cost, in achieving the required performances for power processing equipment and systems. As is evident from the contents of this report, both tutorial- and application-oriented modeling/analysis/design/optimization efforts are emphasized, which have resulted in the following general achievements:

- The methodologies of power processing modeling, analysis, design, and optimization, are all well established.

- Application-oriented analysis, design, and optimization subprograms are becoming available for designer.

- Cost-effective system configuration study and system disturbance propagation are now feasible.

- With full support in the future, the MAPPS should become compatible "partners" to all designers.

- An expandable data management program intended for user's convenience in using the various MAPPS subprograms is also demonstrated

Based on progress made thus far, continued MAPPS effort undoubtedly will lead to the following:

- Analyze all performances for commonly-used power processing equipment and selected systems.

- Detailed power circuit design optimization to meet given power-dependent performance requirements.

- Standardized control-circuit design to meet all control-dependent performance requirements.

- Identification of optimum system configurations and system failure mode effects.

Power processing technology has been, by necessity, an evolving one. It is perhaps not an understatement that, in terms of modeling and analysis, the level of sophistication has been much below that of circuit developments. The industry, however, has reached the stage where such a gap can no longer be tolerated without incurring severe penalties. It is therefore to the advancement of power processing, modeling, analysis, design, and simulation that this program effort is dedicated. (Appendix U)

11. APPENDICES

The appendices supplement the presentations give- in the main text. They consist of papers presented in the various conferences as well as other unpublished work under the sponsorship of Contract NAS3-19690. Often containing details of analytical/computational effort, the appendices dealing with the following topics are hereby regarded as an inseparable entity to the main text:

APPENDIX A

TIME DOMAIN MODELLING AND STABILITY ANALYSIS OF AN INTEGRAL PULSE FREQUENCY MODULATED DC TO DC POWER CONVERTER

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ABSTRACT

Using state variable representation a nonlinear, discrete-time system is derived that models the converter exactly. This system is linearized about its steady state solution, and converter stability, transient response and audio susceptibility are studied. The steady state solution of the converter is stable if and only if all the roots of the linearized system are absolutely less than unity. Excellent agreement with laboratory test data has been observed.

I. INTRODUCTION

DC to DC power converters play an important role in satellite power distribution systems, and standardization and optimization of converter design and performance are of considerable interest to the aerospace power processing industry. In order to optimize converter design and performance a thorough understanding of the converter as a system is required and one must be able to analytically predict such important converter behavior as stability, transient response and audio susceptibility (closed loop frequency response). Power converters, also called regulators, of the class considered here, employ pulse modulation for controlling the dutycycle with which a primary power source is switched to a load so that a prescribed constant load voltage is maintained. The pulse modulation process presents considerable difficulties in analyzing the behavior of these regulators by conventional frequency domain analysis techniques and many approximations in system modelling are usually required. These difficulties are apparent from recently published frequency-domain analytical results, which either limit the analytical applicability to a specific dutycycle control mode (e.g., constant frequency, constant on-time, etc.,) or assume the validity of applying linear feedback theory to nonlinear control loops [1,2].

This paper presents a new approach to the problem of converter modelling based on time domain description and analysis of pulse modulation systems [3,4]. An equivalent, nonlinear discrete time system is derived that describes the pulse modulation process and the converter behavior exactly. After linearization about the discrete time equilibrium solution (steady state), stability is readily established as a function of any arbitrary converter parameter with the information being graphically displayed in terms of the locations of the system roots in the complex plane. Besides obtaining converter stability criteria this analysis technique also provides information on transient behavior and audio susceptibility (closed loop frequency response).

An important feature of the present approach is that it makes extensive use of a digital computer as an analysis tool, replacing many difficult and tedious analytical computations by numerical solutions and making thereby a certain degree of automation of power converter modelling and analysis possible. The developed technique promises to be a valuable tool in converter modelling and analysis. It is applied in this paper to analyze a series switched regulator (buck), but it is also applicable to other regulator configurations such as the boost and buck-boost, for example, and even to converters operating with a discontinuous inductor current. This will be described in a future paper.

II. TIME DOMAIN MODELLING

Consider the series switched regulator shown in Figure 1. The critical element of the regulator is the pulse modulator that controls the power switch Q (actually a transistor) by periodically opening and closing it in such a manner, that the output voltage e_o is maintained at some specified reference voltage E_R. By comparing the output voltage e_o with the voltage E_R an error signal is formed which is then integrated together with a voltage proportional to the derivative of e_o and an AC signal obtained from a secondary winding of the power stage inductor. Whenever the output e_c of the integrator exceeds a specified threshold E_T, the power switch closes for a predetermined fixed time T_{on}, here 20 μsec. If upon reopening $e_c < E_T$, the switch remains open for an unknown period T_{off} until once more the condition $e_c \geq E_T$ is satisfied and the switch closes again for T_{on} seconds; if $e_c \geq E_T$ upon reopening, the switch will remain open for a minimum, fixed off-time $T_{off-min}$. This technique of

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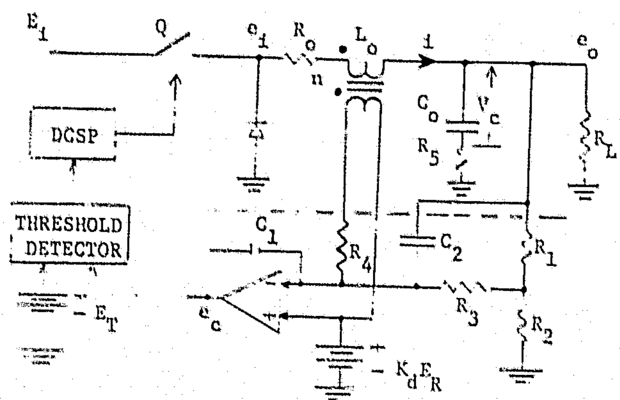
error signal encoding is generally known as integral pulse frequency modulation (IPFM) and it presents considerable difficulties in analyzing the behavior of the regulator circuit of Figure 1 by conventional frequency domain analysis techniques.



$K_d = R_2/(R_1+R_2)$

n = TURNS RATIO

Figure 1. Series Switched Regulator

Formulation of State Equations

From Figure 1 it is apparent that the system has three states which are defined as follows: the output voltage e_o, the current i flowing through the inductor L_o, and the output e_c of the integrator (operational amplifier). By inspection of Figure 1 one obtains the following equations, assuming that the input impedance of the control network inside the dashed box is nearly infinite relative to R_L, as is the case.

$$\frac{di}{dt} = \frac{1}{L_o}(e_i - e_o - R_o i) \tag{1}$$

$$e_o = R_5\left(i - \frac{e_o}{R_L}\right) + v_c \tag{2}$$

$$\frac{dv_c}{dt} = \frac{i}{C_o} - \frac{e_o}{R_L C_o} \tag{3}$$

Differentiating e_o in Equation (2) with respect to time, and substituting for di/dt and dv_c/dt from (1) and (3) yields

$$\frac{de_o}{dt} = e_o\left(-\frac{1}{C_o(R_5+R_L)} - \frac{R_5R_L}{L_o(R_5+R_L)}\right) + i\left(\frac{1}{C_o(R_5+R_L)} - \frac{R_oR_5R_L}{L_o(R_5+R_L)}\right) + e_i\left(\frac{R_5R_L}{L_o(R_5+R_L)}\right) \tag{4}$$

Equations (1) and (4) are the state equations of the power circuit. Assuming a continuous inductor current, the input voltage e_i is defined by

$$e_i = \begin{cases} E_i & \text{when switch Q is closed} \\ 0 & \text{when switch Q is open} \end{cases} \tag{5}$$

The operational amplifier is connected as an integrator with the noninverting input serving as the reference. Thus, the voltage e_c with respect to ground is given by

$$e_c = K_dE_R + \int_{t_o}^{t}\left\{\frac{K_d}{R_3C_1}(E_R - e_o) - \frac{n}{R_4C_1}(e_i - iR_o - e_o) - \frac{C_2}{C_1}\dot{e}_o\right\}d\tau \tag{6}$$

where the dot denotes differentiation with respect to time (d/dt).

Differentiating (6) yields

$$\dot{e}_c = \left(\frac{n}{R_4C_1} - \frac{K_d}{R_3C_1}\right)e_o - \frac{C_2}{C_1}\dot{e}_o + \frac{K_d}{R_3C_1}E_R - \frac{n}{R_4C_1}e_i + \frac{nR_o}{R_4C_1}i \tag{7}$$

The quantity $\dot{e}_o$ can be substituted from (4), and defining the state vector $\bar{x}$ as

$$\bar{x} = [e_o, i, e_c]^T \tag{8}$$

and the input vector $\bar{u}$ as

$$\bar{u} = [e_i, E_R]^T \tag{9}$$

Equations (1), (4) and (7) may be written in compact form as

$$\dot{\bar{x}} = F\bar{x} + G\bar{u} \tag{10}$$

where the entries of the 3 by 3 matrix F and the 3 by 2 matrix G are defined in terms of circuit parameters in Appendix A. Equation (10) is the state equation of the converter describing it regardless of whether the switch Q is open or closed. Merely the input $\bar{u}$ changes in accordance with (5) when the switch opens and closes.

Equivalent Nonlinear Discrete Time System

The solution to (10) is given by

$$\bar{x}(t) = e^{(t-t_o)F}\,\bar{x}(t_o) + \int_{t_o}^{t} e^{(t-\tau)F}\,G\bar{u}(\tau)d\tau \tag{11}$$

or, since $\bar{u}$ is piecewise constant,

$$\bar{x}(t_k+T) = e^{FT}\,\bar{x}(t_k) + e^{FT}\left[\int_0^T e^{-Fs}\,ds\right]G\bar{u}(t_k) \tag{12}$$

where $\bar{u}(t) = \bar{u}(t_k) =$ constant for $t_k < t \leq t_k + T$.

Define the following matrices:

$$\Phi(T) = e^{FT} \tag{13}$$

and

$$D(T) = e^{FT}\left[\int_0^T e^{-F\sigma}\, d\sigma\right] G \tag{14}$$

The matrix $\Phi(T)$ is known as the state transition matrix of the system. Equation (12) becomes now

$$\bar{x}(t_k+T) = \Phi(T)\,\bar{x}(t_k) + D(T)\,\bar{u}(t_k) \tag{15}$$

The value of the input vector $\bar{u}(t_k)$ depends on the state of the switch Q at time t_k^+. Note that the matrices Φ and D are only a function of the time step T which need not be constant and whose maximum permissible value is either T_{on}, or T_{off}, depending on the state of the switch at t_k^+.

For simple, low order systems the matrices $\Phi(T)$ and $D(T)$ can often be analytically evaluated as algebraic functions of T, as is the case for the present converter system (see Appendix B). But for a general analysis applicable to a variety of converter configurations (some of possibly high order), the matrices $\Phi(T)$ and $D(T)$ are evaluated numerically by a digital computer. The matrix exponential of Equation (13) is evaluated from its series representation, i.e.,

$$e^{FT} = I + FT + \frac{F^2T^2}{2!} + \frac{F^3T^3}{3!} + \ldots \tag{16}$$

with the number of terms to be added being determined by an error criterion. Computation of $D(T)$ is then straightforward using trapezoidal or Runge-Kutta integration over the interval $[0,T]$. The computation of $\Phi(T)$ and $D(T)$ is programmed as a FUNCTION SUBPROGRAM with T as a formal parameter so that $\Phi(T)$ and $D(T)$ can be evaluated for any specified T.

If one cannot, or even if one does not wish to, evaluate Φ and D in closed algebraic form, it is still useful to establish the structure of the matrices. This can be done quite easily by noting the structure of the matrices F and G and then applying the method of interpolation (Appendix B) for computing $\Phi(T) = e^{FT}$ without actually performing the computations. It follows that

$$\Phi = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 \\ \phi_{21} & \phi_{22} & 0 \\ \phi_{31} & \phi_{32} & 1 \end{bmatrix} \quad \text{and} \quad D = \begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix} \tag{17}$$

The zero entries in the third column of Φ indicate that between switch times the state x_3 of the integrator does not affect the power stage variables, and the entry $\phi_{33} = 1$ identifies with the integrator. This is also clear from physical reasoning by examining the circuit diagram of Figure 1. The zeroes in the matrix D have a similar physical interpretation with respect to the effect of the reference voltage E_R on the power stage of the regulator.

The equivalent discrete time system of the converter will now be derived. Figure 2 shows e_I as a function of time and merely serves the purpose of establishing notation regarding the time instances t_k. Note that $t_{k+1} - t_k$, for any k, is not restricted to be constant.

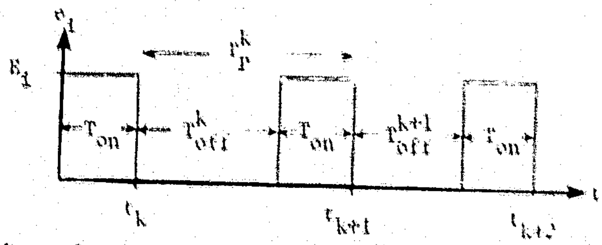


Figure 2. Input Voltage e_I as a Function of Time

The equivalent discrete time system to be given here describes the regulator behavior in terms of the time evolution of its state vector x at the discrete time instances t_k, $k = 0,1,2,\ldots$. Defining the inputs $\bar{u}_0$ and $\bar{u}_1$ as

$$\bar{u}_0 = \begin{bmatrix} 0 \\ E_R \end{bmatrix} \quad \text{and} \quad \bar{u}_1 = \begin{bmatrix} E_I \\ E_R \end{bmatrix} \tag{18}$$

It follows from Equation (15) that

$$\bar{x}(t_{k+1}) = \Phi(T_{on})\Phi(T_{off}^k)\bar{x}(t_k) + \Phi(T_{on})D(T_{off}^k)\bar{u}_0 + D(T_{on})\bar{u}_1 \tag{19}$$

where T_{off}^k is a function of $\bar{x}(t_k)$ described implicitly by the modulator threshold condition

$$E_T = \phi_{31}(T_{off}^k)x_1(t_k) + \phi_{32}(T_{off}^k)x_2(t_k) + x_3(t_k) + d_{32}(T_{off}^k)E_R \tag{20}$$

Note that given any initial state $x(t_0)$, Equations (19) and (20) can be used to compute recursively the state vector $\bar{x}(t_k)$ for all future time instances t_k. Therefore, these equations represent the equivalent discrete time system for the converter, describing its state at the time instances t_k exactly without any approximations. Note also that Equation (19) describes a nonlinear discrete time system because of the dependence of T_{off}^k on the state $\bar{x}(t_k)$ via Equation (20). Bringing the threshold voltage E_T to the right hand side of (20), the modulator threshold condition may be expressed in standard from as:

$$\zeta(\bar{x}(t_k), T_{off}^k) = 0 \tag{21}$$

Equilibrium Solution

The steady state behavior or equilibrium solution of the system (19) is of prime interest and it is defined by the condition

$$\begin{aligned}\bar{x}(t_{k+1}) &= \bar{x}(t_k) = \bar{x}^* = \text{constant for all } k\\ T_{off}^{k+1} &= T_{off}^{k} = T_{off}^{*} = \text{constant for all } k\end{aligned} \qquad (22)$$

First the approximate steady state solution is computed. From dutycycle and flux conservation considerations it follows that

$$T_{off}^{*} \approx T_{on}(E_i - E_R)/E_R \qquad (23)$$

where E_R is numerically equivalent to the regulated DC output voltage. Denoting

$$T_p^* = T_{off}^* + T_{on} \qquad (24)$$

and applying (17) and (22) when expanding (19) yields for the first two rows (the third row of (19) yields no information on x_3^*),

$$\begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix}\Bigg|_{T_p^*} \begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} + \begin{bmatrix} d_{11}(T_{on}) \\ d_{21}(T_{on}) \end{bmatrix} E_i \qquad (25)$$

which can be solved for x_1^* and x_2^* since T_p^* is approximately known. Thus,

$$\begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} = E_i \begin{bmatrix} 1-\phi_{11} & -\phi_{12} \\ -\phi_{21} & 1-\phi_{22} \end{bmatrix}^{-1}\Bigg|_{T_p^*} \begin{bmatrix} d_{11}(T_{on}) \\ d_{21}(T_{on}) \end{bmatrix} \qquad (26)$$

The third state x_3^* is determined from the threshold condition (20) as:

$$x_3^* = E_T - \phi_{31}(T_{off}^*)\, x_1^* - \phi_{32}(T_{off}^*)\, x_2^* - d_{32}(T_{off}^*) E_R \qquad (27)$$

The steady state solution $\bar{x}^*$ determined by this method is not exact because the power circuit is not completely lossless so that the dutycycle relationship of (23) is only an approximation, but a very good one. How well this $\bar{x}^*$ approximates the true equilibrium solution can be determined by checking how closely $\bar{x}_k$ and $\bar{x}_{k+1}$ match when using (19) for propagating the state through one cycle starting with $\bar{x}_k = \bar{x}^*$. The best method for determining the exact steady state is to determine the exact T_{off}^* by iterative linearization (Newton's method) on the cycle to cycle matching condition for the third state (which is the integrator output and directly controls the threshold condition). The iterative process is started with the above computed approximate steady state values and thus converges usually very fast. More details of this procedure are described next.

Define the system state when the power switch turns on as:

$$\bar{z}_k \triangleq \bar{x}(t_k + T_{off}^k) \qquad (28)$$

and clearly

$$z_3(t_k) = E_T \qquad \text{for all } k = 0,1,2,\ldots \quad (29)$$

In the steady state one has:

$$\begin{bmatrix} z_1^* \\ z_2^* \\ E_T \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 \\ \phi_{21} & \phi_{22} & 0 \\ \phi_{31} & \phi_{32} & 1 \end{bmatrix}\Bigg|_{T_{off}^*} \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} + \begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix}\Bigg|_{T_{off}^*} \begin{bmatrix} 0 \\ E_R \end{bmatrix} \qquad (30)$$

Clearly, if $\bar{x}^*$ and T_{off}^* are the exact steady state values, then one must satisfy the state matching condition:

$$\begin{aligned} S_{match} = x_3^* - [\phi_{31}(T_{on}) z_1^* + \phi_{32}(T_{on}) z_2^* + E_T + d_{31}(T_{on}) E_i \\ + d_{32}(T_{on}) E_R] = 0 \end{aligned} \qquad (31)$$

since the square bracketed term should equal x_3^*. Note now that via Equations (26), (27) and (30), the function S_{match} is really only a function of T_{off}^*, and one wishes to determine T_{off}^* such that

$$S_{match}(T_{off}^*) = 0 \qquad (32)$$

Iterative linearization (Newton's method [11]) may now be applied to (32) to determine the exact value for T_{off}^*. The entire procedure is performed by the computer with the required partial derivative $\partial S_{match}/\partial T_{off}$ being evaluated numerically. Convergence from the approximate steady state to the exact steady state is usually within 1-3 iterations.

Note that the difference between $\bar{x}^*$ and $\bar{z}^*$ denotes the peak-to-peak steady state ripple, provided the inductor current i and output voltage e_o are in phase. This is usually the case, unless the series equivalent resistance R_s of the capcitor C_o is equal to zero. Note that x_1^* denotes the maximum value, and z_1^* the minimum value, of the limit cycle of the regulated output e_o.

III. STABILITY ANALYSIS

Regarding stability of the discrete time nonlinear system (19)-(20) one may now consider two approaches: (1) Determine stability-in-the-large*, and (2) determine stability of the equilibrium solution.

*Given any initial state $\bar{x}(t_o)$, show that it will converge to the equilibrium solution.

The task of analytically determining stability-in-the-large appears to be a difficult one. Initial attempts of relating stability-in-the-large to the contraction mapping/fixed point theorem [7] approach to solving Equations (19) and (20) have failed. So have attempts of using the second method of Liapunov [3,8]. But hope for success at some future time has not been entirely dispelled so that further research in this area appears to be indicated. Establishing stability-in-the-large is basically equivalent to solving the converter start-up problem. This can, however, be studied using a digital simulation based on Equations (19) and (20), since usually a fixed start-up procedure is followed, i.e., convergence to the equilibrium solution from only a well defined set of initial states need be considered and not from any state in the entire state space.

Of more importance at the moment is to establish stability of the equilibrium solution, which will be accomplished by linearization. The linearized system can also be used to study small signal audio susceptibility and transient behavior of the converter. It should be kept in mind, however, that the results thus obtained will not be valid for arbitrarily large displacements of the system from its equilibrium, and that when certain system parameters are varied such that instability of the equilibrium is approached, the region to which the linearized system applies may become small.

The Linearized System

The nonlinear, discrete time system described by Equations (19) and (20) will now be linearized about its steady state equilibrium solution $\overline{x}^*$, and the nominal DC supply voltage E_i^*. Denoting

$$\delta\overline{x}(t_k)=\overline{x}(t_k)-\overline{x}^* \quad \text{and} \quad \delta E_i(t_k+T_{off}^*)=E_i(t_k+T_{off}^*)-E_i^* \tag{33}$$

it follows that

$$\delta\overline{x}(t_{k+1})=\left\{\Phi(T_{on})\frac{\partial}{\partial\overline{x}}\left[\Phi(T_{off}^k)\overline{x}(t_k)+D(T_{off}^k)\overline{u}_o\right]\Big|_{\overline{x}^*}\right\}\delta\overline{x}(t_k) + \left\{\frac{\partial}{\partial E_i}\left[D(T_{on})\overline{u}_1\right]\right\}\delta E_i(t_k+T_{off}^*) \tag{34}$$

where it is important to note that T_{off}^k is a function of $\overline{x}_k$ via the threshold condition (20), i.e., $\zeta(\overline{x}(t_k),T_{off}^k) = 0$.

In the previous developments it had been tacitly assumed that $E_i = E_i^*$ = constant for all time. This is not necessarily so and the nonlinear discrete time system (19)-(20) is also an exact description of the converter if E_i is time-varying, provided E_i remains constant over any T_{on} period. To assume a time-varying E_i composed of the nominal DC value E_i^* plus a small superimposed AC component δE_i, is a useful concept when investigating audio susceptibility of the converter and is the main reason why it is included here in the derivation of the linearized system.

Denoting the first curly bracketed term in (34) by Ψ, a constant 3 x 3 matrix, and the second curly bracketed term by Γ, a constant 3-dimensional column vector, Equation (34) can now be written as

$$\delta\overline{x}(t_{k+1}) = \Psi\,\delta\overline{x}(t_k) + \Gamma\,\delta E_i(t_k+T_{off}^*) \tag{35}$$

and it represents the sought linearized system. The matrix Ψ and the column vector Γ remain to be evaluated, however.

By definition,

$$\Psi = \Phi(T_{on})\frac{\partial}{\partial\overline{x}}\left[\Phi(T_{off}^k)\,\overline{x}(t_k) + D(T_{off}^k)\,\overline{u}_o\right]\Big|_{\overline{x}^*} \tag{36}$$

To evaluate the partial derivatives of the square bracketed term analytically turns out to be possible but a very tedious task and it is much easier evaluated numerically by using difference quotients. Denote the continuous function $\overline{f}(\overline{x})$ by

$$\overline{f}(\overline{x}) = \Phi(T_{off}^k)\,\overline{x}(t_k) + D(T_{off}^k)\,\overline{u}_o \tag{37}$$

and for sufficiently small Δx_i, $i = 1,2,3$, one has that

$$\frac{\partial\overline{f}}{\partial\overline{x}}\Big|_{\overline{x}^*} \approx \begin{bmatrix} \frac{f_1(x_1^*+\Delta x_1)-f_1(x_1^*)}{\Delta x_1} & \cdots & \frac{f_1(x_3^*+\Delta x_3)-f_1(x_3^*)}{\Delta x_3} \\ \vdots & & \vdots \\ \frac{f_3(x_1^*+\Delta x_1)-f_3(x_1^*)}{\Delta x_1} & \cdots & \frac{f_3(x_3^*+\Delta x_3)-f_3(x_3^*)}{\Delta x_3} \end{bmatrix} \tag{38}$$

In order to evaluate (38) one must first determine by how much T_{off} changes due to a change Δx_j, $j = 1,2,3$, and then use the new T_{off} to compute the $f_i(x_j+\Delta x_j)$, $i,j = 1,2,3$. The threshold condition

$$\zeta(\overline{x},T_{off}) = 0 \tag{39}$$

is used to determine the change in T_{off} due to a change in $\overline{x}$. Iterative linearization (Newton's method) is used to determine the new T_{off} that satisfies $\zeta = 0$ after $\overline{x}$ has been perturbed by Δx_j, $j = 1,2,3$. The only problem with numerical differentiation is to select the appropriate increments Δx_j. At the present the increments are taken as 1% of the value of the independent variable, i.e.,

$$\Delta x_j = 0.01\,|x_j^*| \tag{40}$$

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Some experimentation with the increment size is advisable, since the accuracy of the partial derivatives depends on it. For instance, if the function varies rapidly, a very small increment is clearly required. On the other hand, if the increment is chosen needlessly too small, then the accuracy degrades because of numerical problems, since in the limit a difference quotient assumes numerically the value 0/0. Studies on the increment size and its effect on the results have also physically significant implications. If the linearized system shows high sensitivity to increment size, then this points out that the nonlinear system changes its behavior rather rapidly as it moves away from its equilibrium point, and the results obtained for the linearized system are only valid for very small perturbations about the equilibrium. A computationally slightly more complex, but perhaps also more accurate way of computing a derivative numerically is to use the following approximation,

$$\left.\frac{\partial f}{\partial x}\right|_{x^*} \approx \frac{f(x^*+\Delta x)-f(x^*-\Delta x)}{2\Delta x} \qquad (41)$$

which can also detect discontinuities.

The 3 x 1 matrix Γ can be evaluated analytically, and by inspection of (34) it follows that:

$$\Gamma = \begin{bmatrix} d_{11}(T_{on}) \\ d_{21}(T_{on}) \\ d_{31}(T_{on}) \end{bmatrix} \qquad (42)$$

since E_I enters linearly into the system.

Stability of the Linearized System

To assess stability of the steady state solution one now examines the stability of the linearized system (35), restated here for convenience:

$$\delta\overline{x}(t_{k+1}) = \Psi\ \delta\overline{x}(t_k) + \Gamma\ \delta E_I(t_k+T^*_{off}) \qquad (43)$$

This system is stable if and only if all the eigenvalues λ_i of Ψ are absolutely less than unity, that is,

$$|\lambda_i(\Psi)| < 1, \qquad i=1,2,3 \qquad (44)$$

The eigenvalues of Ψ are evaluated by a digital computer and changes in the eigenvalues as a function of system parameters can be plotted in the complex plane. The locations of the eigenvalues, which are the roots of the system, do not only indicate stability, but also govern the transient behavior of the converter after a disturbance has displaced it from its equilibrium. The existing relationships between root locations inside the unit circle and corresponding system response times and damping are well known results from z-transform analysis of linear discrete time systems [9,10].

Stability Results

A digital computer program has been written that computes the equilibrium solution $\overline{x}^*$, evaluates the matrix Ψ, and computes the eigenvalues λ_i, $i = 1,2,3$. For nominal converter parameters as listed in Table 1 one expects to obtain three real and positive eigenvalues less than unity, since it is known from actual converter breadboard tests that this system is stable and that after a disturbance the resulting transient decays in a nonoscillatory manner. This was the case as can be ascertained from the computer results shown in Table 2. Note that one root (eigenvalue) is for all practical purposes equal to zero. This is because the incremental integrator output voltage δe_c can be shown to be a linear combination of the incremental inductor current δi and the incremental output voltage δe_o, provided the inductor series resistance R_o equals zero, which is almost the case here. The zero eigenvalue should, therefore, cause no concern: it does not affect stability, being clearly less than unity, and results will focus here mainly on the two other, nonzero eigenvalues.

Table 1. Nominal Circuit Parameter Values

Symbol	Parameter	Units	Value
E_I	Supply Voltage	volts	30
E_R	Reference (Desired Output) Voltage	volts	20
E_T	Integrator Threshold	volts	8
R_o	Inductor Series Resistance	ohms	0.015
R_1	Part of Output Voltage Divider	ohms	28.7K
R_2	Part of Output Voltage Divider	ohms	13.5K
R_3	Op-amp DC Input Resistor	ohms	10K
R_4	Op-amp AC Input Resistor	ohms	100K
R_5	Series-equivalent Resistance of C_o	ohms	0.077
R_L	Load	ohms	10.
C_o	Output Filter Capacitor	μF	300
C_1	Op-amp Feedback Capacitor	pF	2200
C_2	Lead Compensation Capacitor	μF	0.022
L_o	Output Filter Inductor/Transformer	μH	250
n	Transformer Turns Rate n_2/n_1	--	0.65
T_{on}	On-Time	μs	20
T_{off}-min	Minimum Off-Time	μs	5

Table 2. Computer Stability Results

```
EI=  3.0000E+01 (volts)
TON=  2.0000E-05 TOFF=  9.9951E-06 TP=  2.9995E-05 (sec)
X=  2.0033E+01  2.3966E+00  6.8015E+00 = X*  (volts, amps, volts)
Z=  1.9970E+01  1.6009E+00  8.0000E+00 = Z*
Y=  6.0989E-02  7.9777E-01 -1.1965E+00 = X* - Z* (Peak-to-Peak Ripple)

PSI=
  9.7102E-01  6.6839E-02  9.3872E-02
 -1.4513E-01  7.9768E-01  5.9146E-01
 -3.2488E-02 -5.3817E-01 -4.0041E-01

LAMBDA=
  4.1176E-01  0.          9.5659E-01  0.          1.9027E-15  0.
```

The developed computer program is now used to compute the roots of the linearized system as a function of important system parameters, thereby yielding valuable design information on system stability and transient behavior. Critical parameters are the AC loop gain embodied in R_4 or n_2, the DC loop gain embodied in R_3, and the lead capacitor C_2. The motion of the roots can be plotted in the complex plane, and as long as they remain inside the unit circle, the system is stable. The system is at the verge of instability for those parameter values for which the roots are just crossing the unit circle, and it is unstable when the roots are outside the unit circle. Figures 3 through 5 show some of the root locus plots that were obtained. Figure 4, for example, predicts that without the AC loop, the converter will become unstable as C_2 is decreased below 600 pF. It also shows that without the AC loop no complex roots are obtained which considerably restricts the ability to shape response time and damping of the converter transients. This clearly demonstrates that the main advantage of the AC loop is to provide an additional degree of design freedom for adjusting the transient behavior of the converter independent of the output filter parameters. Note that the present root locus plots are not exactly equivalent to those usually encountered in control systems design, since here no "zeros" exist because the system has not been characterized by a transfer function. From the results of the stability analysis the following conclusions could be drawn:

- The capacitor C_2 provides lead information and is critical for stability.
- The AC loop also acts as a stabilizing lead, but is less critical in the presence of C_2 compensation. Its advantage is that it can adjust the transient response independent of the output filter parameters L_0-C_0 and the load R_L.
- With $C_2 = 0$, the system can be stabilized by the AC loop alone, but it will be oscillatory and only marginally stable.
- Without the AC loop, the system can be stabilized by C_2 alone very well. The AC loop plays therefore a less important role in stabilizing the system.
- The present operating point of the converter is good, but its transient response can be improved (speeded up) by lowering C_2 from $C_2 = 22{,}000$ pF to $C_2 = 5{,}000$ pF. As can be seen in Figure 3, this creates a pair of complex roots with a 0.707 damping ratio and a higher natural frequency as before.
- Near instability the system is extremely sensitive to the series equivalent resistance R_5 of the capacitor C_0.

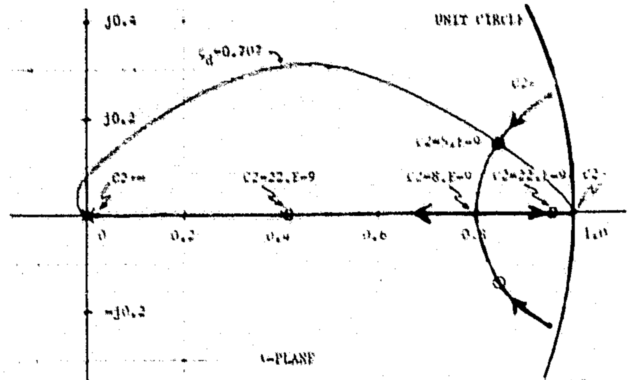

Figure 3. Root Loci for Linearized System: Effect of Lead Capacitor C_2 with Nominal AC Loop

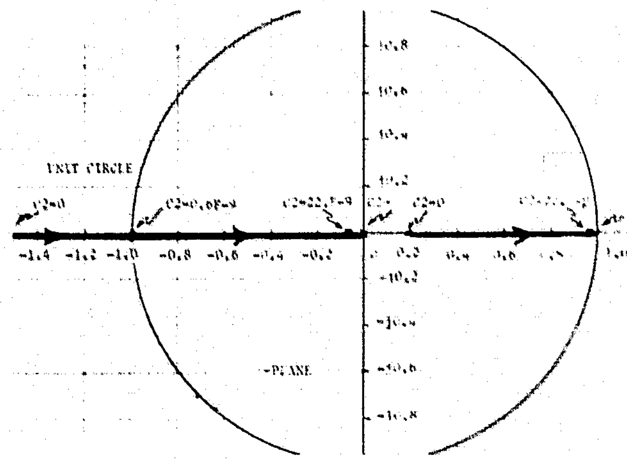

Figure 4. Root Loci for Linearized System: Effect of Lead Capacitor C_2 with AC Loop Open

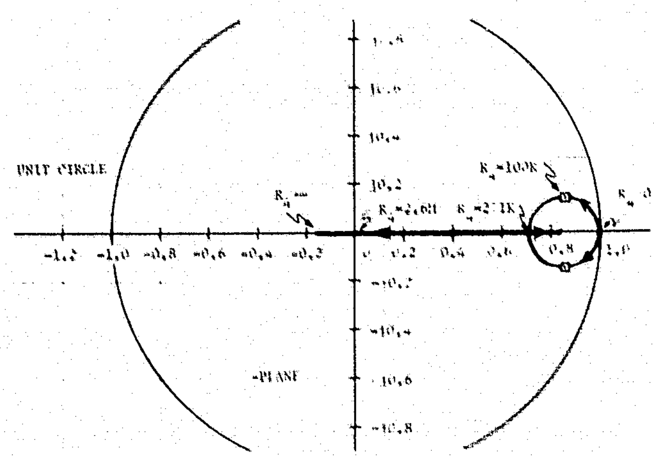

Figure 5. Root Loci of Linearized System: Effect of AC Loop When C_2 = 5000 pF

The analytically predicted results on stability and transient behavior were then compared with laboratory results obtained from an actual breadboard model of the converter and good agreement was observed. Reducing the capacitor C_2 from 22,000 pF to 5000 pF resulted, as predicted, in a faster transient response exhibiting an oscillatory overshoot of 5% that is characteristic for a damping ratio of $\zeta_d = 0.707$. When C_2 was reduced further to $C_2 = 0$, the system remained stable, but its transient response became now quite oscillatory with very little damping, just as expected in accordance with the corresponding root locations at $C_2 = 0$ as shown in Figure 3. When C_2 was reduced from 22,000 pF toward zero with the AC loop open, the behavior of the converter could be directly correlated with the corresponding root locations in Figure 4. The only observed discrepancy was that the breadboard model became unstable for values of $C_2 \leq 1000$ pF while the analysis predicted instability to occur only at $C_2 \leq 600$ pF, a relatively minor inconsistency. Near instability the region about the steady state to which the linearized system applies may be quite small and any otherwise insignificant disturbance may cause the system to leave this region and become unstable. Variations in the AC loop gain when C_2 was held constant at 5000 pF resulted in a converter behavior that also correlated well with the corresponding root locations in Figure 5.

IV. AUDIO SUSCEPTIBILITY

It is of interest to examine how sinusoidal oscillations of the supply voltage E_i about its nominal DC value affect the regulated output voltage e_o in the steady state. The z-transform method can be applied to derive a frequency domain transfer function since in the steady state the cycle period $T_p^* = T_{on} + T_{off}^*$ is constant. Furthermore, the amplitude of the supply voltage oscillations is constrained to be small and therefore the linearized system model of Equation (43) applies. Taking the z-transform of the vector difference equation (43) and noting that by definition $e_o = x_1$, one obtains

$$\delta E_o(z) = H(zI-\Psi)^{-1}\,\Gamma e^{sT_{off}^*}\,\delta E_i(z) \tag{45}$$

where

$$H = [1,0,0] \tag{46}$$

After setting $z = e^{j\omega T_p^*}$, the frequency domain transfer function $G = \delta E_o/\delta E_i$ is given by

$$G(j\omega)=H(Ie^{j\omega T_p^*}-\Psi)^{-1}\Gamma e^{j\omega T_{off}^*}, \qquad 0 \leq \omega T_p^* \leq \pi \tag{47}$$

which by virtue of the sampling theorem applies up to one-half the sampling frequency, i.e., up to $\omega T_p^* = \pi$. For the present converter this means up to 16.6 KHz which comprises the entire frequency band of interest. Note that the purely multiplicative factor $e^{j\omega T_{off}^*}$ contributes only to the phase information of $G(j\omega)$ and can be ignored for amplitude computations. This is also clear from physical reasoning since the term merely reflects the time shift of the sinusoidal input $\delta E_i(t)$ by T_{off} relative to the discrete reference times t_k, see Figure 2.

The transfer function $G(j\omega)$ of (47) can be easily evaluated at any desired ω by a digital computer. The results are shown in Figure 6 in comparison with laboratory test data obtained from a breadboard model of the converter and agreement is quite good. Between 50 Hz and 1.2 KHz the measured audio susceptibility differs from the computed values by only 1-2 db out of a total attenuation of about -42 db, while at higher frequencies a maximum deviation of up to 3.4 db can be observed, amounting to a maximum error of 8%. As can be seen, the computed frequency response predicts less attenuation than actually measured. This is most likely caused by the fact that the mathematical system model cannot be a perfect description of the actual physical system which apparently is slightly more lossy than predicted. The mathematical description modelled the power transistor and the diode as ideal switches, while in reality some losses are incurred in these devices; also, due to transistor storage time, the switch is not perfect. It should also be remembered that at higher frequencies the assumption that E_i is constant over the fixed time period $T_{on} = 20$ μsec becomes a poorer approximation; this is however expected to contribute only a minor error since the effect tends to average out.

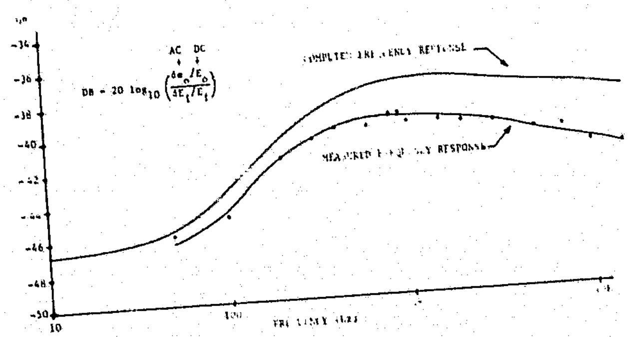

Figure 6. Audio Susceptibility of Converter

The measured frequency response data was obtained by feeding the regulator output voltage into an harmonic wave analyzer. This can also contribute to the discrepancy observed. For it will lead to slightly different results than obtained from computing the amplitude of the envelope of e_o, whenever the upper and lower envelopes of e_o are not exactly in-phase, as was observed here over several frequency ranges.

V. TRANSIENTS CAUSED BY SUPPLY VOLTAGE STEP CHANGES

Of great interest is the transient behavior of the converter after a step change in the supply voltage E_i. The linearized system remains valid for transient analysis, since the converter continues to operate about its steady state equilibrium. The transient resulting from a step change of E_I from, say 30 to 40 volts, should be looked at as a transient of the $E_I = 40$ volt system when displaced from its equilibrium. The closed loop root locations in the complex plane govern the decay of the transient with respect to damping and rapidity of response [9], but the peak overshoot observed after supply voltage switching depends on the "initial state", which is the state of the converter when the supply voltage step change first becomes effective. For the present converter note that the peak of the first cycle after switching E_I is completely independent of the controller (dashed box of Figure 1) and only depends on the output filter and load. This first peak can be readily computed by judiciously applying Equation (19) as follows. Using the old equilibrium $\vec{x}^*$, first compute the corresponding state $\vec{z}^*$ at $t_{k-1} + T^*_{off}$ (see Figure 2):

$$\begin{bmatrix} z_1^* \\ z_2^* \\ z_3^*=E_T \end{bmatrix} = \Phi(T^*_{off}) \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ d_{32}(T^*_{off})E_R \end{bmatrix} \tag{48}$$

Assuming that the supply voltage switch and corresponding change in T_{on} occurred at some time t between t_{k-1} and $t_{k-1} + T^*_{off}$, it follows that the peak of the first cycle at t_k is given by

$$\begin{bmatrix} x_1^o(t_k) \\ x_2^o(t_k) \\ x_3^o(t_k) \end{bmatrix} = \Phi(T^{new}_{on}) \begin{bmatrix} z_1^* \\ z_2^* \\ E_T \end{bmatrix} + \begin{bmatrix} d_{11} \\ d_{21} \\ d_{31} \end{bmatrix}_{T^{new}_{on}} E_I^{new} + \begin{bmatrix} 0 \\ 0 \\ d_{32}(T^{new}_{on}) \end{bmatrix} E_R \tag{49}$$

This first peak, $\vec{x}^o_k$, after switching now forms the initial state for the new system and the convergence from $\vec{x}^o_k$ to the new steady state equilibrium is governed by the linearized system (35), with the linearization having been performed about the new equilibrium, of course. Thus, defining the incremental initial state by

$$\delta\bar{x}(t_o) \triangleq \bar{x}^o(t_k) - \vec{x}^*_{new} \tag{50}$$

the time history of the transient is defined by the discrete time response of the linear system

$$\delta\bar{x}(t_{k+1}) = \Psi\, \delta\bar{x}(t_k) \tag{51}$$

starting with the initial state $\delta\bar{x}(t_o)$ given in (50).

Investigating the vehavior of the transient is now done best by propagating Equation (51) over a few cycles until the actual peak response has been observed. From then on the decay of the transient is solely determined by the roots. Propagation of (51) is done best by a digital computer, although the low order of the present system makes it possible to perform the required computations with a pocket size electronic calculator. Obtained results were compared with laboratory data from a breadboard model, and good agreement was observed.

VI. CONCLUSIONS

A time domain approach based on state space techniques has been applied to modelling and analysis of an integral pulse frequency modulated DC to DC power converter. An equivalent, nonlinear discrete time system was derived that describes the converter without approximations. This system was linearized about its equilibrium solution, which is the steady state of the converter, and from the obtained linear discrete time system, converter stability, transient response and audio susceptibility could readily be established. A key feature of this approach is that it makes extensive use of a digital computer as an analysis tool, thereby facilitating a certain degree of automation in power converter modelling and analysis. The analytically predicted results were compared with laboratory test data obtained from an actual breadboard model of the converter and very good agreement was observed.

The approach to converter modelling and analysis presented here has with very good results also been applied to a pulse width modulated buck regulator (the converter of Figure 1 with a different dutycycle control mode). Furthermore, the concept of system modelling by a state transition matrix was used in digital simulation of converters, resulting in significantly faster program execution times. Currently the approach is being successfully applied to other power converter configurations, such as boost and buck boost for instance, and to converters operating with a discontinuous inductor current. The results of this research will be presented in a future paper.

The analysis approach developed in this paper can be generalized and applied to a large variety of converters and it should prove to be a very valuable tool in power converter modelling and analysis in the future.

APPENDIX A

Entries of Matrices F and G

In expanded form Equation (10) can be written as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} f_{11} & f_{12} & 0 \\ f_{21} & f_{22} & 0 \\ f_{31} & f_{32} & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} g_{11} & 0 \\ g_{21} & 0 \\ g_{31} & g_{32} \end{bmatrix} \begin{bmatrix} e_I \\ E_R \end{bmatrix} \tag{A-1}$$

where

$$f_{11} = -\frac{1}{C_o(R_5+R_L)} - \frac{R_5R_L}{L_o(R_5+R_L)}$$

$$f_{12} = \frac{R_L}{C_o(R_5+R_L)} - \frac{R_oR_5R_L}{L_o(R_5+R_L)} \qquad \text{(A-2)}$$

$$f_{21} = -\frac{1}{L_o}, \qquad f_{22} = -\frac{R_o}{L_o}$$

$$f_{31} = \frac{n}{R_4C_1} - \frac{K_d}{R_3C_1} + \frac{C_2}{C_1C_o(R_5+R_L)} + \frac{C_2R_5R_L}{C_1L_o(R_5+R_L)}$$

$$f_{32} = \frac{C_2R_oR_5R_L}{C_1L_o(R_5+R_L)} - \frac{R_LC_2}{C_1C_o(R_5+R_L)} + \frac{R_on}{R_4C_1}$$

$$g_{11} = \frac{R_5R_L}{L_o(R_5+R_L)}, \qquad g_{21} = \frac{1}{L_o} \qquad \text{(A-3)}$$

$$g_{31} = -\frac{n}{R_4C_1} - \frac{C_2R_5R_L}{C_1L_o(R_5+R_L)}$$

$$g_{32} = \frac{K_d}{R_3C_1}$$

APPENDIX B

Analytic Determination of the State Transition Matrix $\Phi(T)$

The Cayley-Hamilton theorem [5] is applied to determine $\Phi(T) = e^{FT}$; this technique is also known as the method of interpolation [6]. Thus, since F is a 3 x 3 matrix,

$$\Phi(T) \triangleq e^{FT} = \gamma_oI + \gamma_1F + \gamma_2F^2 \qquad \text{(B-1)}$$

where the γ_i are scalar functions of T which must be determined. To do this the eigenvalues λ of F are needed, which are the roots of $\det(F-\lambda I) = 0$. Hence,

$$\lambda[\lambda^2 - (f_{11}+f_{22})\lambda - f_{12}f_{21} + f_{11}f_{22}] = 0$$

yields

$$\lambda_{1,2} = \frac{f_{11}+f_{22}}{2} \pm j\sqrt{f_{11}f_{22}-f_{12}f_{21}-(f_{11}+f_{22})^2/4}, \qquad \lambda_3 = 0 \qquad \text{(B-2)}$$

which is rewritten as

$$\lambda_1 = -\alpha+j\beta, \qquad \lambda_2 = -\alpha-j\beta, \qquad \lambda_3 = 0 \qquad \text{(B-3)}$$

Substituting λ's for F in (B-1) yields

$$e^{(-\alpha+j\beta)T} = \gamma_o + \gamma_1(-\alpha+j\beta) + \gamma_2(-\alpha+j\beta)^2$$
$$e^{(-\alpha-j\beta)T} = \gamma_o + \gamma_1(-\alpha-j\beta) + \gamma_2(-\alpha-j\beta)^2 \qquad \text{(B-4)}$$
$$1 = \gamma_o$$

Solving these equations for the γ's yields

$$\gamma_o = 1 \qquad \text{(B-5)}$$

$$\gamma_1 = \frac{2\alpha}{\alpha^2+\beta^2}\left\{1 - e^{-\alpha T}\left[\frac{\alpha^2-\beta^2}{2\alpha\beta}\sin\beta T + \cos\beta T\right]\right\} \qquad \text{(B-6)}$$

and

$$\gamma_2 = \frac{1}{\alpha^2+\beta^2}\left\{1 - e^{-\alpha T}\left[\frac{\alpha}{\beta}\sin\beta T + \cos\beta T\right]\right\} \qquad \text{(B-7)}$$

Thus, (B-1) represents a closed form expression of $\Phi(T)$.

Determination of the Matrix D(T)

The only nontrivial computation required is the evaluation of the matrix integral, see Equation (14). From (B-1) it follows that

$$\int_o^T e^{-sF}ds = TI + F\int_o^T \gamma_1(-s)ds + F^2\int_o^T \gamma_2(-s)ds \qquad \text{(B-8)}$$

$$= TI + F\xi_1(T) + F^2\xi_2(T)$$

By direct evaluation

$$\xi_1(T) = \frac{2\alpha}{\alpha^2+\beta^2}\left\{T - \frac{1}{\alpha^2+\beta^2}\left[e^{\alpha T}(\alpha\cos\beta T+\beta\sin\beta T)-\alpha\right] + \frac{\alpha^2-\beta^2}{2\alpha\beta(\alpha^2+\beta^2)}\left[e^{\alpha T}(\alpha\sin\beta T-\beta\cos\beta T)+\beta\right]\right\} \qquad \text{(B-9)}$$

$$\xi_2(T) = \frac{1}{\alpha^2+\beta^2}\left\{T - \frac{1}{\alpha^2+\beta^2}\left[e^{\alpha T}(\alpha\cos\beta T+\beta\sin\beta T)-\alpha\right] + \frac{\alpha}{\beta(\alpha^2+\beta^2)}\left[e^{\alpha T}(\alpha\sin\beta T-\beta\cos\beta T)+\beta\right]\right\} \qquad \text{(B-10)}$$

Then,

$$D(T) = \Phi(T)\,[TI + F\xi_1(T) + F^2\xi_2(T)]\,G \qquad \text{(B-11)}$$

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APPENDIX B

GENERALIZED COMPUTER-AIDED DISCRETE TIME DOMAIN MODELING AND ANALYSIS OF DC-DC CONVERTERS

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SUMMARY

A generalized discrete time domain modeling and analysis technique is presented for all types of switching regulators using any type of duty-cycle controller, and operating in both continuous and discontinuous inductor current. State space techniques are employed to derive an equivalent nonlinear discrete time model that describes the converter exactly. The system is linearized about its equilibrium state to obtain a linear discrete time model for small signal performance evaluations, such as stability, audiosusceptibility and transient response. The analysis makes extensive use of the digital computer as an analytical tool. It is universal, exact and easy to use.

I. INTRODUCTION

Switched dc-dc converters can be characterized, in Figure 1, by the three basic functional blocks: power stage, analog signal processor, and digital signal processor or duty cycle controller. The power stage, as illustrated in Figure 1 by the three basic configurations: buck, boost, and buck/boost, can operate either ina continuous inductor current mode or in a discontinuous inductor current mode. The analog signal processor usually contains an error amplifier, a compensation network and a single-feedback-control loop or multiple-feedback-control loops [1]. The digital signal processor includes a ramp generator, a threshold level, and a timing circuit in order to achieve one of the following means of duty cycle control of the power switch, namely, a fixed ON-time variable OFF-time control, a fixed OFF-time variable ON-time control, a fixed frequency control or a hysteresis control, etc. Partially due to the nonlinear discrete nature of such system and partially due to the rapidly-evolving new circuit technology, modeling and analysis of power processing systems has been constantly lagging behind the circuit development. To date analyses presented [2-7] have suffered from at least one of the following constraints:

- limited to certain types of power stage operating mostly in the continuous inductor-current mode
- limited to certain types of duty-cycle controllers
- good accuracy limited to low modulation frequencies
- complexity of mathematical derivations which often impedes practical usefulness
- limited to conventional single-loop systems, since the multiple-loop system has a rather unique way of pulse modulation implementation and therefore analysis

Recently, a time domain modeling and analysis of a constant ON-time controlled buck converter operating with a continuous inductor current has been presented [8]. An equivalent nonlinear discrete time model was derived that describes the converter behavior exactly. The system was linearized about its equilibrium state

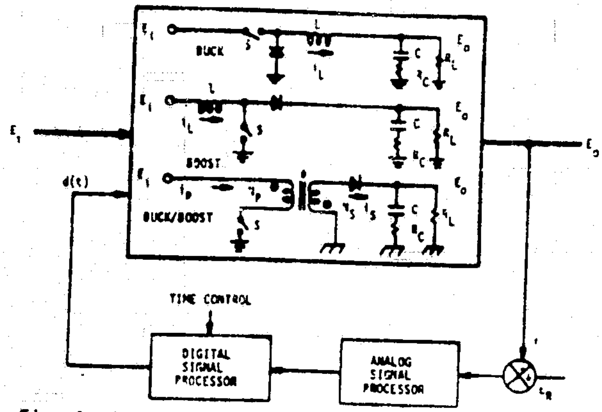

Fig. 1. Switched dc-dc converter with three basic power stage configurations.

to obtain a linear discrete time model for small signal performance evaluations, such as stability, audiosusceptibility and transient response. In the approach[8], the closed-loop converter is modeled as a single entity rather than the three aforedescribed individual functional blocks. The analysis, mostly performed numerically with low computer cost, is relatively easy to use because the complex mathematical integrations are performed by the computer. Such an approach is generalized and extended herein to include all types of power stages, all types of duty-cycle controllers with singal or multiple feedback loops, and both continuous and discontinuous inductor current operations.

A step-by-step procedure in performing this discrete time domain analysis is presented in a simple but general form applicable to a wide-variety of power stages and duty cycle control methods. Followed by this generalized analysis, two specific examples are presented to demonstrate the application of such an analysis scheme. The first example is a two-loop controlled boost converter operating in a discontinuous inductor current mode and using a constant frequency duty-cycle controller. The second example is a constant-frequency buck converter operating in both a continuous current mode at heavy loads and a discontinuous current mode at light loads. A composite computer program is developed such that the transition between the continuous current operation and the discontinuous current operation can be readily studied by varying the line or load condition.

II. GENERALIZED DISCRETE TIME DOMAIN ANALYSIS

Presented here is a step-by-step procedure in performing the discrete time domain analysis. This discrete time domain analysis not only provides the steady state solution but also, through eigenvalue analysis, provides closed-loop stability results and transient response. A method of time-domain to frequency-domain transformation is introduced such that a closed-loop input-to-output transfer function of the converter is

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obtained. The input-output transfer function is employed to analyze the propagation of a small signal disturbance from the converter input to its regulated output, normally known as the audiosusceptibility of the converter.

Step 1: State Space System Representation

The state variables of the system $\underline{x}$, a nx1 column vector, normally are selected as voltages across the capacitors and currents through the inductors. However, for the convenience of each individual problem, state variables can be chosen differently. System equations are written to characterize exactly the converter for the continuous current operation and the discontinuous current operation. The following definitions are used to simplify frequent references in this paper.

Mode 1 Operation: The current through the inductor is always greater than zero as shown in Fig. 2(a). The period of each switching cycle can be clearly divided into two time intervals, T_{ON} and T_{F1}. During T_{ON}, the power transistor is "ON" and the diode is "OFF", and during T_{F1}, the power transistor is "OFF" and the diode is "ON".

Mode 2 Operation: The current through the inductor reduces to zero and resides at zero for a T_{F2} time interval as shown in Fig. 2(b). In this T_{F2} time interval, both the transistor and the diode are "OFF". The time intervals T_{ON} and T_{F1} defined in the Mode 1 operation also are valid in the Mode 2 operation.

The system representation for the Mode 1 operation is:

$$\dot{\underline{x}} = F1\,\underline{x} + G1\,\underline{u} \quad \text{during } T_{ON} \qquad (1)$$

$$\dot{\underline{x}} = F2\,\underline{x} + G2\,\underline{u} \quad \text{during } T_{F1} \qquad (2)$$

The column vecter $\underline{u}$ is a (mx1) input vector, containing the input voltage E_i, the reference E_R, the saturation voltage drop across the power transistor E_Q, and the forward voltage drop across the diode E_D, etc. The nxn matrices F1 and F2 and the nxm matrices G1 and G2 are constant matrices represented by the various circuit parameters.

In Mode 2 operation, in addition to (1) and (2), equation (3) is added to complete the system representation.

$$\dot{\underline{x}} = F3\,\underline{x} + G3\,\underline{u} \ldots \quad \text{during } T_{F2} \qquad (3)$$

The dimensions of F3 and G3 are the same as those of F1 and G1, respectively.

The converters, which are basically nonlinear switching circuits, are accurately described by the differential equations represented by (1) to (3).

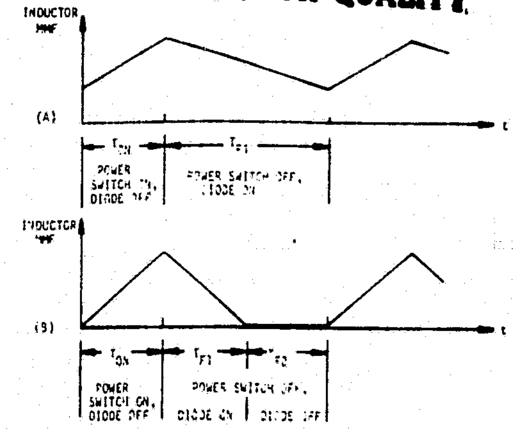

Fig. 2(a) Continuous inductor current operation, (b) Discontinuous inductor current operation.

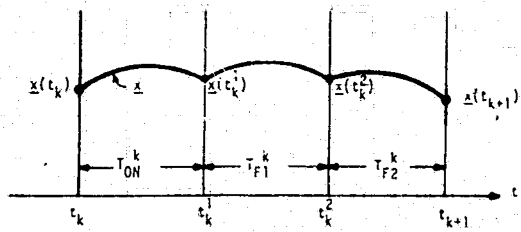

Fig.3. Propagation of state variale during one switching cycle.

The solution of the linear differential equations can be expressed by the following state transition equations.

$$\underline{x}(t+T) = \Phi i(T)\underline{x}(t) + Di(T)\,\underline{u} \qquad (4)$$

where

$$\Phi i(T) = e^{FiT} \qquad i = 1, 2, 3$$

$$Di(T) = e^{FiT}\left[\int_0^T e^{-FiS} ds\right] Gi \qquad i=1,2,3$$

$\Phi i(T)$ and $Di(T)$ for any given T can be computed either analytically or numerically. If they are computed numerically, the following Taylor series expansion is used.

$$e^{FiT} = I + FiT + \frac{(FiT)^2}{2!} + \frac{(FiT)^3}{3!} + \ldots i=1,2,3$$

Step 2: Nonlinear Discrete State Transition Representation

The state trajectory during one cycle of propagation is illustrated as Fig. 3. The discrete state transition equation for the converter in a complete switching cycle can be obtained by combining the two/three state transition equations expressed by (4), each corresponding to a specific switching time interval T_{ON}^k, T_{F1}^k and/or T_{F2}^k. The nonlinear discrete state transition representation for the converter is expressed by (5)

$$\underline{x}(t_{k+1}) \stackrel{\Delta}{=} \Phi\,\underline{x}(t_k) + V\,\underline{u} \qquad (5)$$

where t_k and t_{k+1} corresponding to the time instances at the beginning of the kth cycle and the (k+1)th cycle respectively. Equation (5) is nonlinear because the matrix Φ is a function of the time intervals T_{ON}^k, T_{F1}^k and T_{F2}^k which are all functions of the system state $\underline{X}(t_k)$ by virtue of the threshold conditions shown in the following:

Mode 1 Operation:

$$\Phi \triangleq \Phi 2(T_{F1}^k)\ \Phi 1(T_{ON}^k) \tag{6}$$

$$V \triangleq \Phi 2(T_{F1}^k)\ D1(T_{ON}^k) + D2(T_{F1}^k) \tag{7}$$

where T_{ON}^k and T_{F1}^k representing the T_{ON} and T_{F1} intervals during the kth cycle. The time intervals T_{ON}^k and T_{F1}^k can be determined through the following two threshold conditions:

Threshold Condition 1: A threshold condition determines the duty cycle ratio of the power switch which is normally implemented by comparing the analog error signal with a fixed threshold level to determine the duty cycle pulse width.

$$\varepsilon_1(\underline{x}(t_k),\ T_{ON}^k,\ T_{F1}^k) = 0 \tag{8}$$

Threshold Condition 2: A condition which specifies whether the converter is operating at a constant frequency, or a constant ON time, or a constant OFF time, or a constant voltage-second, or hysteresis control, etc.

$$\varepsilon_2(\underline{x}(t_k),\ T_{ON}^k,\ T_{F1}^k) = 0 \tag{9}$$

Mode 2 Operation:

$$\Phi \triangleq \Phi 3\ (T_{F2}^k)\ \Phi 2(T_{F1}^k)\ \Phi 1(T_{ON}^k) \tag{10}$$

$$V \triangleq \Phi 3(T_{F2}^k)\ \Phi 2(T_{F1}^k)\ D1(T_{ON}^k) + \Phi 3(T_{F2}^k)\ D2(T_{F1}^k) + D3(T_{F2}^k) \tag{11}$$

In order to determine the three time intervals T_{ON}^k, T_{F1}^k and T_{F2}^k, a third condition, in addition to (8) and (9), should be included to detect the time instant when the inductor current is reduced to zero.

Threshold Condition 3:

$$\varepsilon_3(\underline{x}(t_k),\ T_{ON}^k,\ T_{F1}^k,\ T_{F2}^k) = 0 \tag{12}$$

Of course, in Mode 2 operation, the time interval T_{F2}^k should be a parameter in a function corresponding to (8) and (9).

Equations (5-12), are the exact representation of the nonlinear switching nature of the converters.

Step 3: Equilibrium State

In order to solve for the equilibrium state of the system $\underline{x}^*$, the approximate steady state $\tilde{\underline{x}}^*$ is calculated first based on the given input and output conditions. The approximate solution is employed as an initial guess toward solving the exact steady state through Newton's iteration method. In the steady state, equation (5) can be written as

$$\underline{x}^* = \Phi\ \underline{x}^* + V\ \underline{u} \tag{13}$$

The Φ matrix and V matrix can be computed for the given T_{ON}, T_{F1} and T_{F2}. For given input-output requirements of the converter, the approximate time intervals, $\tilde{T}_{ON}$, $\tilde{T}_{F1}$ and $\tilde{T}_{F2}$ can be determined.[9] These approximate steady-state time intervals are substituted into equation (5) and the threshold condition to compute an approximate steady state $\underline{x}^*$. With $\underline{x}^*$ as an initial guess, the Newton's iteration method is employed to solve the steady-state solution. Equations (5) through (12) are computed continuously in the iteration process until a certain specified state-matching condition is satisfied. The state-matching condition can be defined in many different ways, for example:

$$\sqrt{\sum_{i=1}^{n} [x_i(t_{k+1}) - x_i(t_k)]^2} < \varepsilon \tag{14}$$

for an arbitrarily small positive number

Step 4: Linearized Discrete Time-Domain Model

The nonlinear discrete-time-domain equation (5) is linearized about the equilibrium state x^*. This linearized system is used to study the small signal related properties of the converter.

Equation (5) is rewritten as

$$\underline{x}(t_{k+1}) = f\ (\underline{x}(t_k),\ \underline{u},\ T_{ON},\ T_{F1},\ T_{F2}) \tag{15}$$

For a constant forcing function $\underline{u}$, equation (15) is linearized about $\underline{x}^*$.

$$\delta\underline{x}\ (t_{k+1}) = \left.\frac{\partial f}{\partial \underline{x}}\right|_{\underline{x}^*} \delta\underline{x}\ (t_k) \triangleq \Psi\ \delta\underline{x}\ (t_k) \tag{16}$$

where Ψ is a (nxn) matrix. The differentiation $\partial f/\partial \underline{x}$ can be performed analytically, if the problem is simple. Otherwise, it can be computed numerically by the difference quotients.

Step 5: Eigenvalue Stability Analysis

The eigenvalues of the matrix Ψ are evaluated by the computer. The linearized system (16) is stable if and only if all the eigenvalues of Ψ are absolutely less than unity, i.e.,

$$|\lambda_i| < 1 \qquad i = 1,\ldots,n \tag{17}$$

Changes of eigenvalues as a function of system parameters can be plotted in the complex Z-plane. The locations of the eigenvalues in the Z-plane indicate not only the stability but also the transient behavior of the system, i.e., damping and rapidity of response.

Step 6: Susceptibility to Audio Frequencies In The Supply Voltage

In space/military applications, it is a requirement to specify how a small sinusoidal disturbance of the dc supply voltage E_i affects the regulated output voltage E_o in the steady state operation. The audiosusceptibility of the converter is defined as the closed-loop input-to-output transfer function. In the previous development of the linearized discrete mode, a constant input voltage E_i is assumed. If E_i is time varying, but sufficiently slow so that the input voltage remains essentially constant over a switching period, the nonlinear discrete time varying system (15) can be linearized about the previously defined equilibrium state $\underline{x}^*$ and the nominal dc supply voltage E_i.

$$\delta\ \underline{x}\ (t_{k+1}) = \Psi\ \delta\ \underline{x}\ (t_k) + \Gamma\ \delta\ e_i\ (t_k) \tag{18}$$

where

$$F = \frac{\partial f}{\partial e_I}\Bigg|_{X^*,\,E_I}$$

and

$$\delta e_I(t_k) = E_I(t_k) - E_I$$

that is, the time varying $E_I(t)$ contains a dc component E_I plus a small ac component $\delta e_I(t)$.

The output voltage E_0 can be expressed as

$$E_0(t_k) = C\,X(t_k) \tag{19}$$

where C is a constant $(1\times n)$ row matrix.

Applying the Z transformation to (18), it yields

$$\delta X(Z) = (IZ - \Psi)^{-1}\,F\,\delta e_I(Z) \tag{20}$$

The frequency-domain transfer function can be derived after replacing Z by $e^{j\omega T_p}$ and combining (19) and (20).

$$G(j\omega) = \frac{\delta e_0(j\omega)/E_0}{\delta e_I(j\omega)/E_I} = \frac{E_I}{E_0}\,\frac{\delta e_0(j\omega)}{\delta X(j\omega)}\,\frac{\delta X(j\omega)}{\delta e_I}$$

$$= \frac{E_I}{E_0}\,C\,\left(I\,e^{j\omega T_p} - \Psi\right)^{-1} F \tag{21}$$

where E_I and E_0 are the dc average of the input voltage and the output voltage, respectively. The input-to-output frequency domain transfer function thus defined in (21) can be used to study the susceptibility of the converter to the small audio signal disturbance in the supply voltage.

III. APPLICATIONS OF THE DISCRETE-TIME ANALYSIS

Two specific examples are given to demonstrate applications of the generalized procedures presented in the previous section. The first is a multiple-loop boost converter operating at constant switching frequency, Mode 2 current mode. The detailed analysis is presented in this paper to show how the step-by-step procedures of the generalized method are carried out in this specific example. The second example is a two-loop buck converter operating at constant frequency, Mode 1 as well as Mode 2 current depending on line and load conditions. A composite computer program is developed, such that changes of the converter performance during the transition from Mode 1 to Mode 2 or vice verse can be readily studied by simply varying the line and load conditions.

3.1. Example 1:

A dc-dc voltage step-up (boost) converter in Fig. 4 employs two feedback-control loops: The dc loop and the ac loop. The dc loop senses the converter output voltage and compares it with a reference voltage to generate a dc error signal, similar to the conventional way. The ac loop serves two functions: One function is to sense the small signal ac voltage across the energy storage inductor to generate an ac error signal which combined with the dc error signal to serve as the input to the amplifier, the other function is to generate a large signal ramp function by integrating

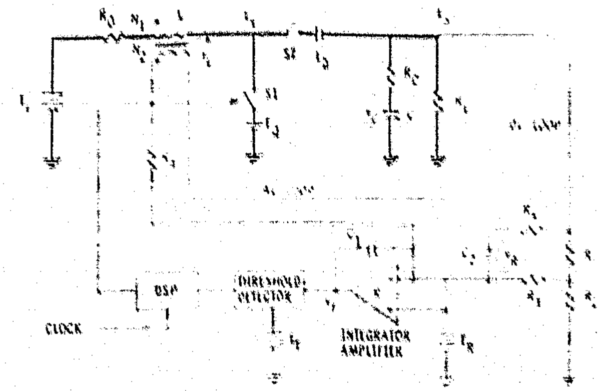

Fig. 4. A boost converter using two-loop control.

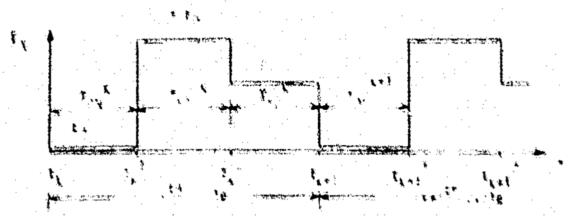

Fig. 5. The voltage across the power switch E_X as a function of time.

the steady state ac switching voltage appearing across the inductor. It is commonly known that the ramp function and a threshold detector are the necessary ingredients in order to convert an analog signal into a digital signal. In conventional single-loop systems, the ramp function is generated either by an external ramp generator or by converting the error output of the dc amplifier. For detailed descriptions of the two-loop system, please refer to references [1, 10].

The boost converter as shown in Fig. 4 was employed in the power processing system of the High Energy Astronomy Observatory Satellite (HEAO) which operates at constant switching frequency, discontinuous inductor current mode exclusively under all line and load conditions. It serves as an appropriate example to demonstrate the discrete time domain analysis since the continuous current operation is considered as the special case of the discontinuous current operation in this analysis approach.

The waveform of E_X, as shown in Fig. 5, is used to serve the purpose of establishing some notation regarding the time instant t_k when each cycle starts and each switching action occurs.

In steady state operation, the digital signal processor is implemented by the following duty cycle control laws:

at $t_k, t_{k+1}, t_{k+2}, \ldots$ the clock pulse turns on the power switch

at $t_k^1, t_{k+1}^1, t_{k+1}^1, \ldots$ the threshold condition turns off the power switch

at $t_k^2, t_{k+1}^2, t_{k+2}^2, \ldots$ the zero inductor current condition turns off the power diode.

The time intervals $t_k^1-t_k$, $t_k^2-t_k^1$, and $t_{k+1}-t_k^2$ are defined as T_{ON}^K, T_{F1}^k and T_{F2}^k, respectively. These time intervals may vary from cycle to cycle. However, the time interval between t_k and t_{k+1} is a constant equal to the period of oscillation, i.e.,

$$t_{k+1}-t_k = T_p \quad \text{for all } k \tag{22}$$

<u>Step 1: State Space System Representation</u>

System equations of Fig. 4 are represented by:

$$\dot{\underline{X}} = F1\underline{X} + G1\underline{U} \qquad t_k \leq t < t_k^1 \tag{23}$$

$$\dot{\underline{X}} = F2\underline{X} + G2\underline{U} \qquad t_k^1 \leq t < t_k^2 \tag{24}$$

$$\dot{\underline{X}} = F3\underline{X} + G3\underline{U} \qquad t_k^2 \leq t < t_{k+1} \tag{25}$$

The explicit representation for F's and G's are given in the appendix. The vectors $\underline{X}$ and $\underline{U}$ are state variables and forcing function, respectively. They are defined as:

$$\underline{X} \triangleq [v_C \; i_L \, v_R \; v_T]^T$$

$$\underline{U} \triangleq [E_I \; E_R \; E_Q \; E_D]^T$$

Each of the linear systems of equations (23-25) admits a closed form solution of the form

$$X(t_k^1)=\underline{X}(t_k+T_{ON}^k)=\phi1(T_{ON}^k)\underline{X}(t_k)+D1(T_{ON}^k)\underline{U} \tag{26}$$

$$\underline{X}(t_k^2)=\underline{X}(t_k^1+T_{F1}^k)=\phi2(T_{F1}^k)\underline{X}(t_k^1)+D2(T_{F1}^k)\underline{U} \tag{27}$$

$$\underline{X}(t_{k+1})=\underline{X}(t_k^2+t_{F2}^k)=\phi3(T_{F2}^k)\underline{X}(t_k^2)+D3(T_{F2}^k)\underline{U} \tag{28}$$

$$\text{where} \quad \phi i(T) = e^{FiT} \qquad i = 1,2,3 \tag{29}$$

$$Di(T) = e^{Fit}[\int_0^T e^{-FiS} dS]Gi \quad i = 1,2,3 \tag{30}$$

The elements of matrices ϕi and Di are defined by:

$$\phi i \triangleq (\phi i_{jk}) \qquad i = 1,2,3$$

$$Di \triangleq (di_{jk}) \qquad j,k = 1,2,3,4$$

The constraints of the system, as represented by (26) through (28), are governed by the threshold condition at $t = t_k^1, t_{k+1}^1$.

$$\xi_1(\cdot) = X_4(t_k^1) = E_T, \tag{31}$$

the zero inductor current condition at $t=t_k^2, t_{k+1}^2 \ldots$

$$\xi_2(\cdot) = X_2(t_k^2) = 0 \tag{32}$$

and the constant frequency condition

$$\xi_3(\cdot) = T_{ON}^k+T_{F1}^k+T_{F2}^k=T_p \text{ for all } K. \tag{33}$$

<u>Step 2: Nonlinear Discrete State Transition Representation</u>

The discrete state transition representation for the boost converter is given by:

$$\begin{aligned} X(t_{k+1}) &= \phi3(T_{F2}^k)\phi2(T_{F1}^k)\phi1(T_{ON}^k)\underline{X}(t_k) \\ &+ [\phi3(T_{F2}^k)\phi2(T_{F1}^k)D1(T_{ON}^k) \\ &+ \phi3(T_{F2}^k)D2(T_{F1}^k) + D3(T_{F2}^k)] \\ &= \phi\underline{x}(t_k) + V\,\underline{U} \end{aligned} \tag{34}$$

together with the threshold condition derived from (31)

$$\begin{aligned} &\phi1_{41}(T_{ON}^k)X_1(t_k) + \phi1_{42}(T_{ON}^k)X_2(t_k) + \phi1_{43}(T_{ON}^k)X_3(t_k) \\ &+ \phi1_{44}(T_{ON}^k)X_4(t_k) + d1_{41}(T_{ON}^k)U_1 + d1_{42}(T_{ON}^k)U_2 \\ &+ d1_{43}(T_{ON}^k)U_3 + d1_{44}(T_{ON}^k)U_4 = E_T, \end{aligned} \tag{35}$$

and the zero inductor current condition, derived from (32)

$$\begin{aligned} &\phi2_{21}(T_{F1}^k)X_1(t_k^1) + \phi2_{22}(T_{F1}^k)X_2(t_k^1) \\ &+ \phi2_{23}(T_{F1}^k)X_3(t_k^1) + \phi2_{24}(T_{F1}^k)X_4(t_k^1) \\ &+ d2_{21}(T_{F1}^k)U_1 + d2_{22}(T_{F1}^k)U_2 + d2_{23}(T_{F1}^k)U_3 \\ &+ d2_{24}(T_{F1}^k)U_4 = 0, \end{aligned} \tag{36}$$

and the constant frequency condition

$$T_{F2}^k = T_p-T_{ON}^k-T_{F1}^k \tag{37}$$

<u>Step 3: Equilibrium State</u>

In the steady state the following condition is satisfied:

$$\underline{X}(t_{k+1}) = \underline{X}(t_k) = \underline{X}^* = \text{constant} \tag{38}$$

The steady state switching time intervals are denoted as T_{ON}^*, T_{F1}^* and T_{F2}^*.

<u>The approximate steady state.</u> Switching time intervals, denoted by $\tilde{T}_{ON}^*$, $\tilde{T}_{F1}^*$ and $\tilde{T}_{F2}^*$, can be computed using the following formula [9]

$$\tilde{T}_{ON}^* = \sqrt{\frac{2L\;T_pP_o\;(E_0+E_D-E_I)}{\eta\;E_I\;(E_0+E_D-E_I)(E_0+E_D-E_Q)}} \tag{39}$$

$$\tilde{T}_{F1}^* = \sqrt{\frac{2L\;T_pP_o\;(E_I-E_Q)}{\eta\;E_I\;(E_0+E_D-E_I)(E_0+E_D-E_Q)}} \tag{40}$$

$$\tilde{T}_{F2}^* = T_p-\tilde{T}_{ON}^*-\tilde{T}_{F1}^* \tag{41}$$

where P_0 is the output power and η is the efficiency of the converter.

Substituting (38-41) into (34) and (35), the approximate steady state $\underline{\tilde{x}}^*$ can be computed

$$\begin{aligned} \tilde{x}_1^* = \phi_{11}\,\tilde{x}_1^* + \phi_{12}\,\tilde{x}_2^* + \phi_{13}\,\tilde{x}_3^* + V_{11}U_1 + \\ V_{12}U_2 + V_{13}U_3 + V_{14}U_4 \end{aligned} \tag{42}$$

$$\begin{aligned} \tilde{x}_2^* = \phi_{21}\,\tilde{x}_1^* + \phi_{22}\,\tilde{x}_2^* + \phi_{23}\,\tilde{x}_3^* + V_{21}U_1 + \\ V_{22}U_2 + V_{23}U_3 + V_{24}U_4 \end{aligned} \tag{43}$$

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$$\tilde{x}_3^* = \phi_{31}\tilde{x}_1^* + \phi_{32}\tilde{x}_2^* + \phi_{33}\tilde{x}_3 + V_{31}U_1 + V_{32}U_2 + V_{33}U_3 + V_{34}U_4 \quad (44)$$

and $$\tilde{x}_4^* = \frac{1}{\phi 1_{44}}[E_T - \phi 1_{41}\tilde{x}_1^* - \phi 1_{42}\tilde{x}_2^* - \phi 1_{43}\tilde{x}_3^* - d1_{41}U_1 - d1_{42}U_2 - d1_{43}U_3 - d1_{44}U_4] \quad (45)$$

where ϕ_{ij} and V_{ij} for $i,j = 1,\ldots,4$ are the entries of the matrix ϕ and V of the linearized system.

Notice that equations (42 - 44) are independent of $\tilde{x}_4^*$ ($\phi_{41} = \phi_{42} = \phi_{43} = 0$), and can be solved for $\tilde{x}_1^*$, $\tilde{x}_2^*$ and $\tilde{x}_3^*$. Equation (45) which is the same as the threshold condition (35) is used to compute $\tilde{x}_4^*$. In this approximation, the threshold condition (35) is automatically satisfied, however, the threshold condition (36) where the inductor current equals zero may not be satisfied. This approximation is merely employed as a starting point in order to search for the exact steady state.

The exact steady state. Define the system state when the power switch turns off as

$$\underline{Y}(t_k) \triangleq \underline{X}(t_k + T_{ON}^k)$$

and when the inductor current vanishes as

$$\underline{Z}(t_k) \triangleq \underline{X}(t_k + T_{ON}^k + T_{F1}^k)$$

In the steady state operation

$$\underline{Y}^* = \phi 1(T_{ON}^*)\underline{X}^* + D1(T_{ON}^*)\underline{U} \quad (46)$$

$$\underline{Z}^* = \phi 2(T_{F1}^*)\underline{Y}^* + D2(T_{F1}^*)\underline{U} \quad (47)$$

and

$$\underline{X}^* = \phi 3(T_{F2}^*)\underline{Z}^* + D3(T_{F2}^*)\underline{U} \quad (48)$$

If T_{ON}^* and T_{F1}^* are the exact steady state values, the steady state $\underline{X}^*$ calculated from (42-45) has to satisfy the following two matching conditions:

(1) The zero-inductor-current condition

$$B_{match} = Z_2^* = 0 \quad (49)$$

(2) The state matching condition can be defined as (50) by matching the state variable X_4 after one cycle of propagation.

$$\begin{aligned} S_{match} = X_4^*(t_{k+1}) - X_4^*(t_k) = &\phi 3_{41}(T_{F2}^*)Z_1^* + \phi 3_{42}(T_{F2}^*)Z_2^* \\ &+ \phi 3_{43}(T_{F2}^*)Z_3^* + \phi 3_{44}(T_{F2}^*)Z_4^* + d3_{41}(T_{F2}^*)U_1 \\ &+ d3_{42}(T_{F2}^*)U_2 + d3_{43}(T_{F2}^*)U_3 + d3_{44}(T_{F2}^*)U_4 \\ &- X_4^*(t_k) = 0 \end{aligned} \quad (50)$$

Iteration linearization (Newton's method) is employed to find T_{ON}^* and T_{F1}^* which satisfies the matching conditions (49) and (50). The step-by-step procedures are described as follows:

Step (a) Compute the approximate state $\tilde{\underline{X}}^*$ from (42-45).

Step (b) Find a new T_{F1}^* by iterative linearization.

$$\tilde{T}_{F1}^* = \tilde{T}_{F1}^* - \frac{B_{match}(\tilde{\underline{X}}^*, \tilde{T}_{ON}^*, \tilde{T}_{F1}^*)}{[\partial B_{match}/\partial T_{F1}]|_{\tilde{T}_{F1}^*}}$$

such that for the given $\tilde{X}^*$ and $\tilde{T}_{ON}^*$ together with the new $\tilde{T}_{F1}^*$, the zero current condition $B_{match}(\tilde{X}^*, \tilde{T}_{ON}^*, \tilde{T}_{F1}^*) = 0$ will be satisfied.

Step (c) Check if $S_{match} \approx 0$ is satisfied?

Step (d) If $S_{match} \approx 0$ is not satisfied, modify $\tilde{T}_{ON}^*$ according to

$$\tilde{T}_{ON}^* = \tilde{T}_{ON}^* - \frac{S_{match}(\tilde{X}^*, \tilde{T}_{ON}^*, \tilde{T}_{F1}^*)}{[\partial S_{match}/\partial \tilde{T}_{ON}]|_{\tilde{T}_{ON}^*}}$$

Step (e) Use the new $\tilde{T}_{ON}^*$ and $\tilde{T}_{F1}^*$ calculated in Step (b) and Step (d) and go back to Step (a) to derive a new approximate state $\tilde{X}^*$. Then to go to Step (b), (c) and (d) and repeat the process until the state matching condition $S_{match} \approx 0$ is satisfied.

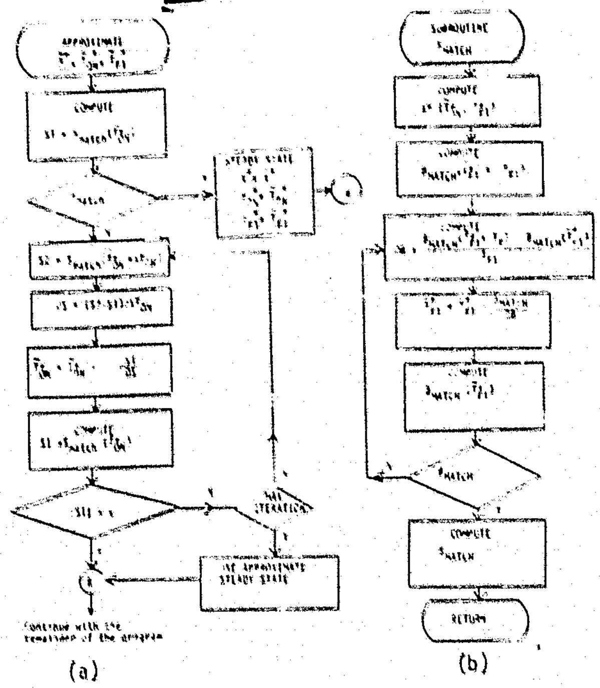

Fig. 6(a) Flow diagram for determining the steady state.
(b) Flow diagram for determining the state matching condition S_{match}.

A flow diagram for determining the steady state is presented in Fig. 6(a) and (b). A subroutine B_{match} is developed in order to search for a proper T_{F1} to satisfy the zero-inductor condition as shown in (49). This subroutine is embodied into the other subroutine S_{match} which ultimately computes the state matching condition as given in (50).

Step 4: Linearized Discrete Time Domain Model

The nonlinear discrete time system equation (34) is rewritten as:

$$\underline{x}(t_{k+1}) = \underline{f}\,(\underline{x}(t_k),\, \underline{U}) \tag{51}$$

This system is linearized about its equilibrium state $\underline{x}^*$.

$$\delta\underline{x}(t_{k+1}) = \Psi\; \delta\underline{x}(t_k) \tag{52}$$

The matrix Ψ is (4x4). The partial derivatives, approximated by difference quotients, are evaluated numerically, for sufficiently small Δx_j, $j = 1, \ldots, 4$.

$$\text{where}\quad \Psi = \left.\frac{\partial \underline{f}}{\partial \underline{x}}\right|_{\underline{x}^*} = \left\{\frac{fi(x_j^* + \Delta x_j) - fi(x_j^*)}{\Delta x_j}\right\}_{ij} \tag{53}$$

Since $\underline{x}$ does not appear explicitly in $\underline{f}$, in order to evaluate (53), the change of T_{ON}, T_{F1}, and T_{F2} due to a change of Δx_i, $i = 1, \ldots, 4$, must be determined first. The new T_{ON} and T_{F1} are computed according to the threshold conditions (35) and (36) in the iteration process described earlier.

It is important to select the appropriate increments Δx_j. Some experimentation with the increment size is advisable, since the accuracy of the partial derivatives depends on it. If the function varies rapidly, a very small increment is clearly required. On the other hand, if the increment is chosen needlessly small, then the accuracy decreases because of a numerical computation error, i.e., a difference quotient assumes numerically the value close to 0/0. Study on the increment size and its effect on the results also has physically significant implications. If the linearized system shows high sensitivity to incremental size, then this points out that the nonlinear system changes its behavior rather rapidly as it moves away from its equilibrium, and the result obtained for the linearized system are only valid for very small perturbations about the equilibrium.

Step 5: Eigenvalue Stability Analysis

A digital computer program has been developed that computes the equilibrium solution $\underline{x}^*$, the matrix Ψ, and the eigenvalues λ_i, $i = 1,2,3,4$ of Ψ. The perturbation Δx_i used to compute the linearized Ψ matrix is taken as 1% of the absolute value of the steady state, i.e.,

$$\Delta x_i = 0.01|x_i^*| \qquad i = 1,2,3,4 \tag{54}$$

Employing a set of nominal circuit parameters given in Table I, the system steady state, the Ψ matrix and its eigenvalues are computed, and the results are presented in Table II. Since the eigenvalues of the system are positive, real, and less than unity, the system is stable; and the transient response after a disturbance decays in a non-oscillatory manner. It is interesting to note that one eigenvalue, λ_4, is equal to zero. This indicates that the order of the system is reduced by one, which confirms the earlier findings [3,5]. It is also apparent from the circuit point of view that the inductor current x_2 is always reduced to zero after any small perturbation. The inductor current can no longer constitute a state variable since it loses the free boundary condition. The eigenvalue, λ_1, close to unity indicates the system has a long-time constant. In fact, the output voltage of the converter when subjected to a step change in load, will reach its new steady-state after a six-millisecond transient as observed in the laboratory.

Table I. Circuit parameter values for the boost converter.

F0	= [illegible]	[illegible]	= [illegible]
L	= [illegible]	N1	= [illegible]
C	= [illegible]	N2	= [illegible]
FC	= [illegible]	EFFICIENCY	= [illegible]
FL	= [illegible]	EI	= [illegible]
F1	= [illegible]	DF	= [illegible]
F2	= [illegible]	EO	= [illegible]
F3	= [illegible]	ED	= [illegible]
F4	= [illegible]	ET	= [illegible]
F5	= [illegible]	TF	= [illegible]
C1	= [illegible]	EA	= [illegible]

Table II. Steady state, Ψ matrix and eigenvalues.

STEADY STATE

EI =	[illegible]E+01	TF1= [illegible]E-05	TF2= [illegible]	
TON =	[illegible]E-05			
TP =	[illegible]E-05		[illegible]E+01	[illegible]E+00
[illegible] =	[illegible]	0.	[illegible]E+01	[illegible]
[illegible] =	[illegible]E+01	[illegible]	[illegible]E+01	[illegible]E+00
[illegible] =	3.753025E+01	[illegible]E-02		
FIPX=	[illegible]E-02	-4.0111[illegible]E+00	[illegible]E-02	0. Ripple Voltage
[illegible]=	-1.4[illegible]055E-06	Convergence Error		
IT=	[illegible]	Number of Iteration		

Ψ Matrix

PSI=

[illegible]E-01	0.	[illegible]E-02	[illegible]E-01
0.	0.	0.	0.
[illegible]E-01	0.	[illegible]E-01	[illegible]E-01
-1.11470[illegible]E+00	0.	[illegible]E+00	[illegible]E-01

Eigenvalues

LAMBDA= REAL	IMAGINARY
1.5[illegible]E-01	0.
7.463304E-01	0.
9.788275E-01	0.
0.	0.

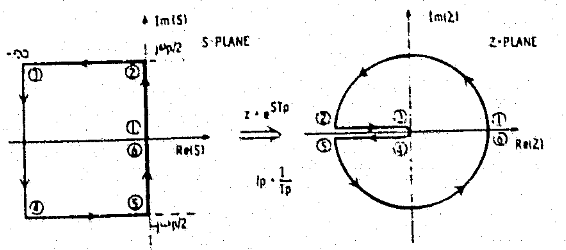

Fig. 7. Mapping from the s-plane to the z-plane.

The method of root locus plot on the z-plane [11], is employed to study loci of eigenvalues as a function of circuit parameters. To facilitate our discussion, a brief review is presented to show how the z-plane is related to the conventional s-plane by the mapping $z = e^{ST_p}$. On Figure 7, an infinite strip in the s-plane limited by one-half of the switching frequency $\pm j\omega_p/2$ is mapped into the entire z-plane. The semi-infinite strip of the left half s-plane embodied by the numbered contour is mapped into the z-plane inside the unit circle while the semi-infinite strip of the right half s-plane is mapped into the z-plane outside the unit cycle. The stability of the discrete system is thus defined if all eigenvalues are located inside the unit circle of the z-plane. If an eigenvalue is located on the circumference of the unit circle of the z-plane, corresponding to a pole on the imaginary axis of the s-plane, the system is on the verge of instability. An eigenvalue located along the positive real axis inside the unit circle of the z-plane corresponds to a pole on the negative real axis of the s-plane. An eigenvalue located along the negative real axis inside the unit circle corresponds to a pair of complex conjugate roots in the s-plane with natural frequency equal to one-half of the switching frequency. An eigenvalue at the origin of the z-plane, corresponds to a pole at $-\infty$ in the s-plane. Additional information concerning the mapping from the s-plane to the z-plane, can be found in [11].

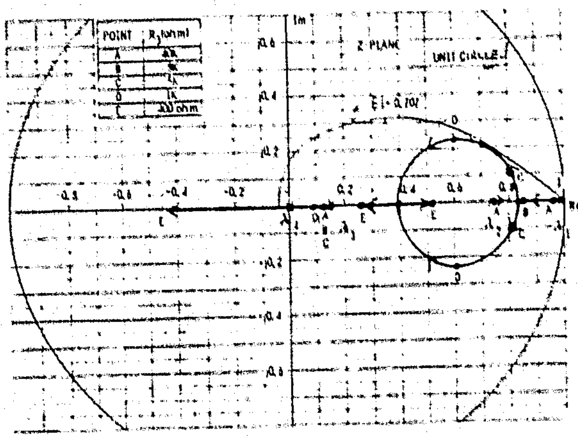

Fig. 8. Eigenvalues as a function of the dc-loop resistor R_3.

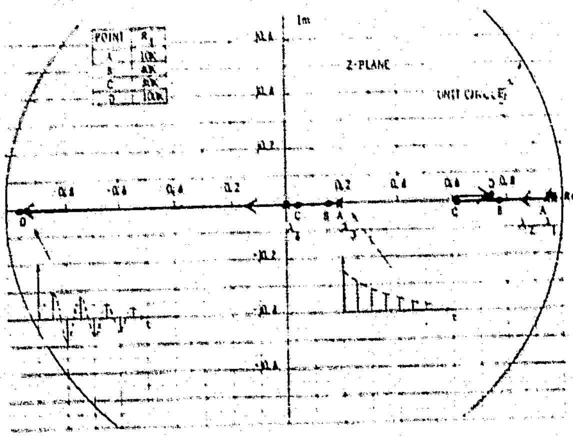

Fig. 9. Eigenvalues as a function of the ac-loop resistor R_4.

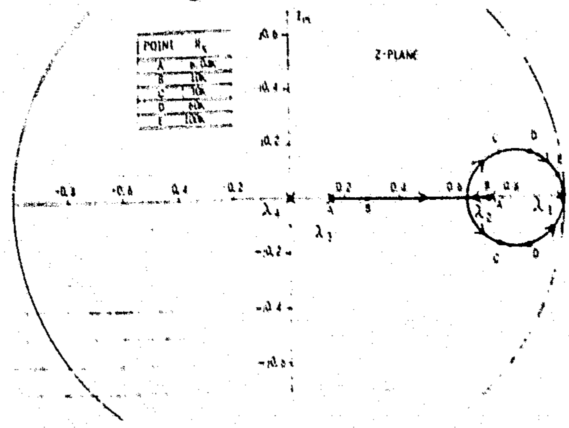

Fig.10. Eigenvalues as a function of the compensation loop resistor R_5.

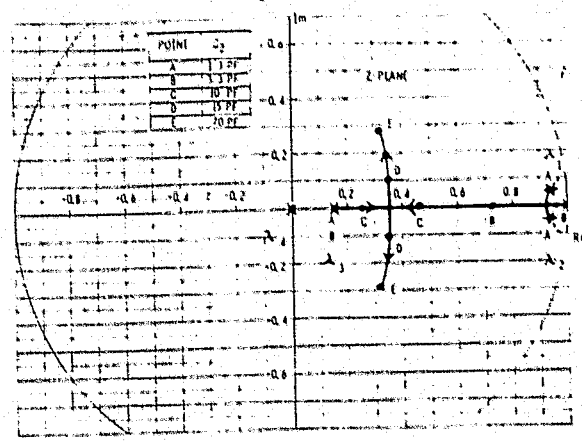

Fig. 11. Eigenvalues as a function of the compensation capacitor C_2.

Several root-locus analyses are presented which plot the eigenvalue loci as a function of dc-loop gain, ac-loop gain and the R-C compensation network. The effect of the dc-loop gain on stability is shown in Fig. 8 by varying the resistor R_3. When the dc-loop gain is increased by means of reducing the value of R_3, the eigenvalue $_1$ moves away from the unity and merges with $_2$ to form a pair of complex-conjugate roots. Further reducing R_3 beyond 400 can cause the eigenvalue $_3$ to move outside the unit circle and therefore to result in an unstable system. The eigenvalue $_4$ always stays at the origin as a result of the discontinuous current operation. The system transient response can be improved by reducing R_3 from 40K to 3K to bring the eigenvalues closer to the constant damping ratio locus of 0.707 for optimum transient response.

Figure 9 shows by reducing the ac loop gain or increasing the ac loop resistor R_4 from 10 kΩ to 140 kΩ, eigenvalues λ_1 and λ_2 move away from unity and the eigenvale λ_3 moves from the positive real axis to the negative real axis. The transient response changes from overdamp to underdamp with a natural resonant frequency equal to half of the switching frequency. It is interesting to note that when R_4 is equal to 85 kΩ, the eigenvalue λ_3 moves into the origin of the complex plane. In sampled data system, double roots at the origin means the transient response will die down in two sampling cycles. Therefore, the ac loop resistor equal to 85 kΩ will provide the optimum transient response.

The effect of the compensation loop, with a series R_5C_2 network, on the stability and the transient response of the system is shown in Fig.10 and Fig.11. when R_5 is increased from its nominal value toward infinite, as shown in Fig.10, all three eigenvalues approach unity asymptotically. The system becomes very marginally stable. Figure 11 shows by reducing C_2 beyond 1.3μf the eigenvalues λ_1 and λ_2 move toward outside the unit circle shown as the dotted lines. On the other hand, by increasing C_2, one eigenvalue approaches unity asymptotically and the other two eigenvalues form a complex conjugate pair and approach point E in the complex plane asymptotically. Therefore, a judicious design of the R-C compensation network is important to stabilize the system and to provide good transient response.

Each of the three feedback loops, ac loop, dc loop, and R-C compensation loop, is shown to play certain important roles of stabilizing the system and providing fast transient response. The analysis shows that a larger stability margin and a faster transient response can be obtained by properly designing the above discussed three feedback loops. The same technique also can be used to optimize the power stage parameters, such as the output filter L and C.

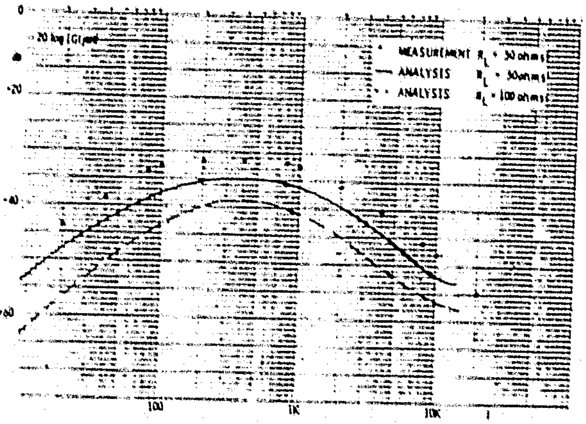

Fig. 12. audiosuscetibility for the boost converter.

Step 6: Susceptibility to Audio Frequencies in the Supply Voltage

The closed loop input-to-output transfer function is expressed by

$$G(j\omega) = \frac{E_I}{E_0}\ \frac{R_L}{R_c+R_L}\ H\ (Ie^{j\omega T}p-\Psi)^{-1}\Gamma \qquad (55)$$

where $H = [1\ 0\ 0\ 0]$

By virtue of sampling theorem, the frequency domain transfer function is only valid for the frequency less than one half of the sampling frequency, i.e., $\omega T_p=\pi$. For the HEAO converter this means the transfer function holds true for the audio frequency up to 16.5KHz which comprises the entire frequency band of interest for the audiosusceptibility performance of the converter.

Figure 12 shows the closed loop frequency response of the converter with the supply voltage E_i = 28V. The general shape of the closed loop frequency response agrees very well with the experimental data, except that a difference of approximately 4db is shown throughout the entire frequency range. It is interesting to note that the audiosusceptibility for the discontinuous current operation is a function of the converter loading, the lighter the load, the better the audiosusceptibility. This phenomenon is quite different from that of the continuous current operation where the audio performance is almost independent of the load.

3.2. Example 2:

The two loop buck converter as shown in Figure 13 has been selected as the second example to demonstrate the application of the generalized discrete time approach. The converter is designed to operate in the continuous current mode on heavy loads and discontinuous current mode on light loads. Employing the previously described analytical approach, a composite computer program is developed to incorporate both the continuous current operation and the discontinuous current operation. For a given line and load condition, the main program first detects the inductor current operating mode, mode 1 or mode 2, then enters into the appropriate subroutine for numerical computations. This composite computer program serves as a very powerful analytical tool to investigate certain often observed anomalous changes of the converter performance such as the stability and the transient response during the transition between the continuous current mode and the discontinuous current mode. Such anomalous changes are rather unlikely to be exposed through other means of analysis.

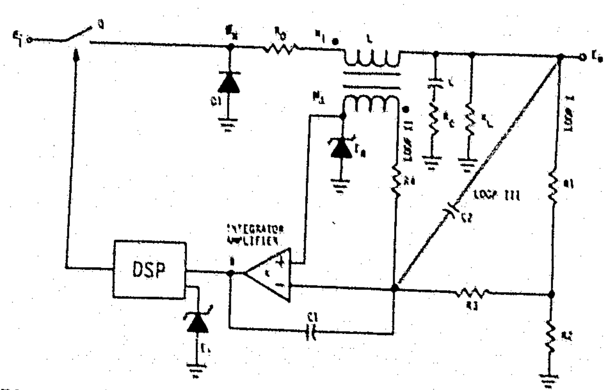

Fig. 13. A buck converter using two-loop control.

Table III. Circuit parameters for the buck converter.

EI	= 5.0E+01,		
EP	= 2.0E+01,	N1	= 4.0E+01,
ET	= [illegible]	NS	= [illegible]
FL	= 1.0E+01,	C1	= [illegible]
TE	= [illegible]	[illegible]	= [illegible]
L	= [illegible]	R1	= [illegible]
FC	= 1.5E-0[illegible]	R2	= 1.[illegible]E+04,
[illegible]	= [illegible]	R3	= 1.0E+04,
FO	= [illegible]	R4	= 1.[illegible]E+03,

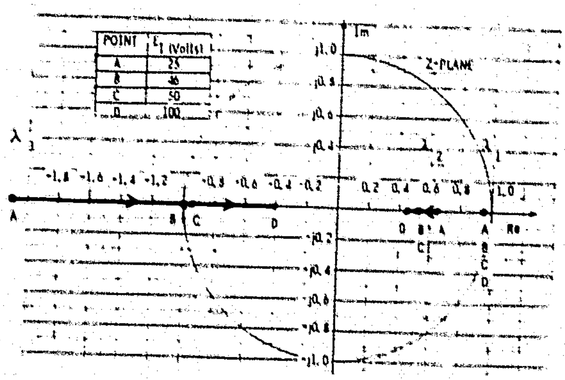

Fig. 14. Eigenvalues as a function of the supply voltage.

The detailed analysis of this converter is not included in the present paper due to the space limitation. However, several interesting results are presented to demonstrate the effectiveness of this analytical approach to a more complicated problem involving both mode 1 operation and mode 2 operation More detail is provided in reference [12].

An earlier computer simulation [13] has indicated in this type of two-loop converter a possible instability problem can occur at half of the switching frequency. Such a high frequency instability problem, while it would be rather difficult to analyze using the frequency domain techniques [2,7], can be readily analyzed using the discrete time domain method discussed in this paper. Figure 14 shows a root locus plot of eigenvalues as a function of the supply voltage E_i with the nominal circuit parameter values given in Table III. As can be seen, changes in E_i primarily move the eigenvalue λ_3 along the negative real axis. For E_i less than 46 volts, the converter is unstable. Certain interesting conclusions are drawn as follows: the converter, using the two-loop implementation described earlier, when operated in the constant frequency continuous current mode can result in instability under certain input-output conditions. The instability often occurs at half of

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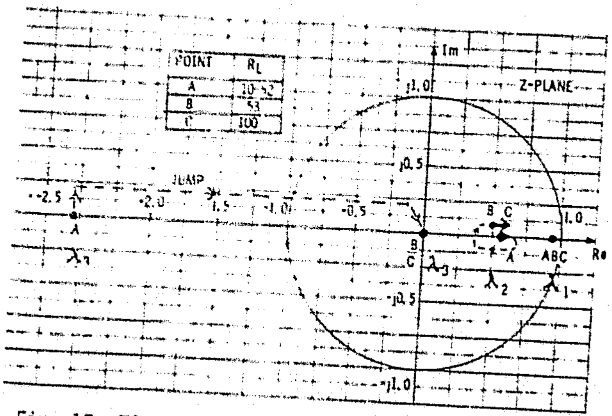

Fig. 15. Eigenvalues as a function of the converter load.

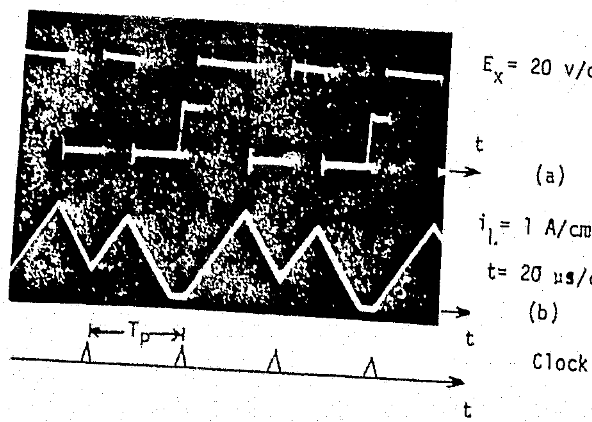

Fig. 16. Buck converter waveforms (a) voltage across the commutation diode, (b) inductor current for an unstable operation.

the switching frequency, when the duty cycle ratio is approximately equal to 0.5 or greater. This instability cannot be resolved by changing either control circuit parameters or the power stage parameters. The above conclusions apply to all power stage configurations: buck, boost, and buck/boost; nevertheless, it is only limited to continuous current operation using a constant frequency duty cycle controller. The detailed analysis of this instability problem is beyond the scope of the present paper. For detailed information, please refer to [10].

The changes of the stability nature and the transient response of the converter were also studied by reducing the load in a manner that the converter first operated in the continuous current mode, then in the discontinuous current mode. Figure 15 shows the change of eigenvalues as a function of the load. When the load was relatively heavy, R_L = 10 ohms to 52 ohms, and the input voltage E_I = 30 volts, the converter operated in a continuous current mode with a duty cycle ratio greater than 50%. The system was unstable. The system was stabilized by increasing R_L up to or above 53 ohms such that the converter began to operate in the discontinuous current mode. It should be noted that during the load variation, from 52 ohms to 53 ohms, a jump phenomenon was observed. The change of the eigenvalue λ_3 from 2.59 to 0 was due to a jump, rather than a fast continuous motion which could be represented by intermediate value of R_L.

Figure 16(a) and (b) shows the waveforms of the voltage E_X across the commutation diode D1 and the cur-

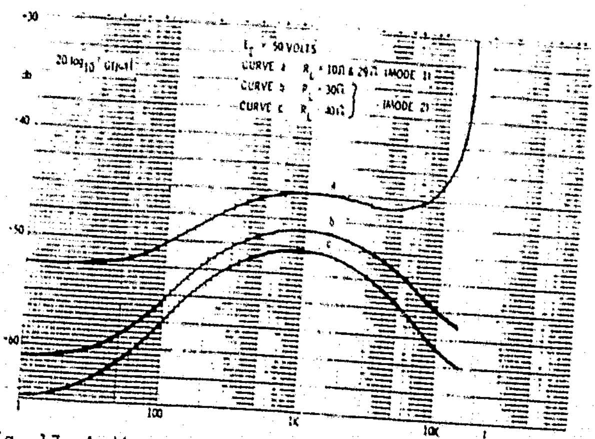

Fig. 17. Audiosusceptibility for the buck converter with continuous current and discontinuous current.

rent i_L through the energy storage inductor, respectively for an unstable operation when E_I = 40 volts and R_L = 22 ohms. Instead of having a growing amplitude as a result of instability, the inductor current waveform is asymmetrical but repetitive. This is because the converter operated alternately in the continuous current mode and the discontinuous current mode during each switching cycle. In fact, when the load resistance was slightly increased above 22 ohms, the converter was stabilized and operated entirely in the discontinuous current mode. This is a verification of the earlier statement that the converter can be stabilized by changing the operation mode from mode 1 to mode 2.

The susceptibility of the converter to an audio frequency disturbance in the supply voltage was also examined for both the mode 1 operation and the mode 2 operation. The audio susceptibility is independent of the load for mode 1 ($R_L < 29\Omega$), curve "a" of Fig. 17, and varies with the load for mode 2 ($R_L > 29\Omega$) such that the lighter the load the better the audiosusceptibility, curve "c" and curve "c". Comparing these three curves also shows a significant difference in the magnitude of audiosusceptibility between mode 1 and mode 2, especially when the frequency of the audio noise is approaching one-half of the switching frequency. The sharp, resonance-like rise in the frequency response at half of the switching frequency only exists with continuous current operation. This is expected since it reflects the closed loop eigenvalues at -0.95 for mode 1, see Fig. 14 and at the origin for mode 2. An eigenvalue located at -1.0 means an undamped resonance at half the switching frequency; as the eigenvalue moves into the circle, damping increases, as it moves out of the circle, exponential build-up and thus instability results.

IV. CONCLUSION

A computer-aided discrete time domain modeling and analysis technique has been presented which is applicable to all types of switching regulators using any types of duty cycle controllers and operating with continuous as well as discontinuous inductor current. State space techniques are employed to characterize converters exactly by the nonlinear discrete time domain equations in vector forms. Newton's iteration method is employed to solve for the exact equilibrium state of the converter. The system is then linearized about its equilibrium state to arrive at a linear discrete time model. The stability nature and transient responses are studied by examining the eigenvalues of the linear system. Changes in eigenvalues due to system parameter changes can be plotted in the complex z-plane yielding an excellent design tool very similar to conventional root-locus plots. The analysis is also extended to determining the frequency related performance characteristics sush as the closed loop input-to-output transfer function used to determine the audio-susceptibility of the converter. The modeling and analysis approach makes extensive use of the digital computer as an analytical tool, replacing highly complex and tedious analyses by numerical method and making automation in power converter design and analysis possible.

Followed by a generalized analysis procedure, two specific examples are presented to demonstrate the application of such an analysis scheme, one for a boost converter operating with constant frequency and discontinuous current, the other for a constant frequency buck converter operating with both continuous current and discontinuous current. A composite computer program is developed for the buck converter to include both current modes of operations. During the transition between the continuous current operation and the discontinuous current operation, an interesting jump phenomenon is observed by plotting the system eigenvalues on the z-plane. The jump of the system eigenvalues not only causes abrupt changes of the performance characteristics of the converter but also, under certain operating condition, the stability nature, from an unstable system to a stable one, or vice verse. The analysis reveals certain high frequency oscillation phenomena at the subharmonic of the switching frequency, an unstable operation normally associated with constant frequency, continuous current mode with a duty cycle ratio greater than fifty percent. Such a high frequency instability phenomenon may not likely be exposed through other means of analysis.

In addition to its particular utility at analyzing high-frequency control-loop related phenomena, the analysis also serves as a useful design tool which provides design guidelines for such important control parameters as the dc loop gain, the ac loop gain and the R-C compensation network of a two loop converter to optimize its transient response and to stablize the system.

APPENDIX: ENTRIES FOR MATRICES Fi AND Gi

The matrices Fi and Gi for i = 1,2,3,4 are 4 x 4. Define $Fi = \{fi_{jk}\}$ and $Fi = \{gi_{jk}\}$

The following entries of the respective matrices were derived assuming negligible loading of the feedback loops to the converter power stage.

$$f1_{11} = -\frac{1}{C}\frac{1}{R_C+R_L} \qquad f1_{22} = -\frac{R_0}{L}$$

$$f1_{31} = \frac{1}{C_2R_5}\frac{R_L}{R_C+R_L} \qquad f1_{33} = -\frac{1}{C_2R_5}$$

$$f1_{41} = \frac{R_L}{R_C+R_L}\left(-\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} - \frac{1}{C_1R_5}\right)$$

$$f1_{42} = \frac{nR_0}{C_1R_4} \quad \text{where } n \triangleq N_1/N_2$$

$$f1_{43} = \frac{1}{C_1R_5} \qquad g1_{21} = \frac{1}{L} \qquad g1_{23} = -\frac{1}{L}$$

$$g1_{41} = -\frac{n}{C_1R_4} \qquad g1_{42} = \frac{1}{C_1R_3} \qquad g1_{43} = \frac{n}{C_1R_4}$$

$$f2_{11} = f1_{11} \qquad f2_{12} = \frac{1}{C}\frac{R_L}{R_C+R_L} \qquad f2_{21} = -\frac{R_L}{L(R_C+R_L)}$$

$$f2_{22} = -\left(R_0 + \frac{R_CR_L}{R_C+R_L}\right)\frac{1}{L} \qquad f2_{31} = f1_{31}$$

$$f2_{32} = R_Cf1_{31} \qquad f2_{33} = f1_{33}$$

$$f2_{41} = f1_{41} + \frac{R_L}{R_C+R_L}\frac{n}{C_1R_4} \qquad f2_{42} = f1_{42} + R_Cf2_{41}$$

$$f2_{43} = 41_{43} \qquad g2_{21} = g1_{21} \qquad g2_{24} = g1_{23}$$

$$g2_{41} = g1_{41} \qquad g2_{42} = g1_{42} \qquad g2_{44} = g1_{43}$$

$$f3_{11} = f1_{11} \qquad f3_{31} = f1_{31} \qquad f3_{33} = f1_{33}$$

$$f3_{41} = f1_{41} \qquad f3_{43} = f1_{43} \qquad g3_{42} = g1_{42}$$

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APPENDIX C

DERIVATION OF EQUATIONS FOR CONSTANT FREQUENCY BUCK REGULATOR CONTINUOUS CONDUCTION OPERATION

C.1 EQUIVALENT DISCRETE TIME SYSTEM

Figure C-1 shows e_i as a function of time and mainly serves the purpose of establishing notation regarding the time instances t_k.

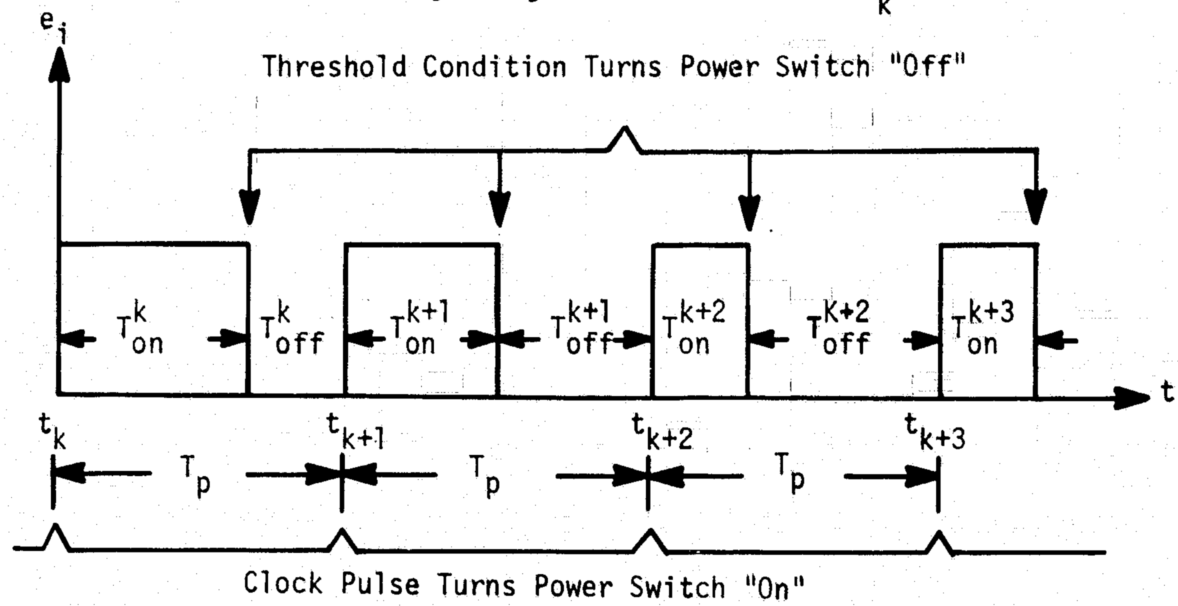

Figure C-1. Input Voltage e_i as a Function of Time

Note that the instances t_k differ from the previous definition used for the control in constant $-T_{on}$ mode, see Section 4.4.2. That is, the time instances t_k denote here the times when the clock turns the power switch was turned off. The reason for this is that in both cases the instances t_k must be selected such that they are at the beginning of that portion of the dutycycle that is controlled by the threshold condition. Note that for constant frequency operation.

$$t_{k+1} - t_k = T_p = \text{constant} \qquad \text{for all } k = 0,1,2... \qquad \text{(C-1)}$$

The equivalent discrete time system for the constant-frequency control is given by

$$\bar{x}(t_{k+1}) = \Phi(T^k_{off}) \left[\Phi(T^k_{on})\, \bar{x}(t_k) + D(T^k_{on})\, \bar{u}_1 \right] + D(T^k_{off})\, \bar{u}_o \qquad \text{(C-2)}$$

with the threshold condition

$$E_T = \phi_{31}(T^k_{on})\, x_1(t_k) + \phi_{32}(T^k_{on})\, x_2(t_k) + x_3(t_k) + d_{31}(T^k_{on})\, E_i + d_{32}(T^k_{on})\, E_R \qquad \text{(C-3)}$$

where as in earlier investigations the input vectors $\bar{u}$ are defined by

$$\bar{u}_o = \begin{bmatrix} 0 \\ E_R \end{bmatrix} \quad \text{and} \quad \bar{u}_1 = \begin{bmatrix} E_i \\ E_R \end{bmatrix} \qquad \text{(C-4)}$$

The threshold condition (C-3) defines T^k_{ON} implictly as a function of the system state $\bar{x}(t_k)$, and because of the constant frequency operation,

$$T^k_{off} = T_p - T^k_{on} \qquad \text{(C-5)}$$

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For the steady state one demands that

$$\bar{x}(t_{k+1}) = \bar{x}(t_k) = \bar{x}^* = \text{constant} \qquad \text{for all } k = 0,1,2\ldots \qquad \text{(C-6)}$$

which by the threshold condition implies that in the steady state also

$$T^{k+1}_{on} = T^k_{on} = T^*_{on} = \text{constant} \qquad \text{(C-7)}$$

First the approximate steady state solution is computed by using the duty-cycle formula

$$
\begin{aligned}
T_{on}^{*} &= (E_R/E_i)T_p \\
T_{off}^{*} &= T_p - T_{on}^{*}
\end{aligned}
\qquad \text{(C-8)}
$$

where E_R is numerically equivalent to the controlled dc output voltage. Using (C-6) and (C-7) when expanding (C-2) one obtains

$$
\begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} = \Phi(T_p) \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} + \left.\begin{bmatrix} \phi_{11} & \phi_{12} & 0 \\ \phi_{21} & \phi_{22} & 0 \\ \phi_{31} & \phi_{32} & 1 \end{bmatrix}\right|_{T_{off}^*} \cdot \left.\begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix}\right|_{T_{on}^*} \begin{bmatrix} E_i \\ E_R \end{bmatrix}
$$

$$
+ \left.\begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix}\right|_{T_{off}^*} \begin{bmatrix} 0 \\ E_R \end{bmatrix} \qquad \text{(C-9)}
$$

Since T_{on}^* and T_{off}^* are approximately known from (C-8), the first two scalar equations of (C-9) can be used to solve for $\overline{x}_1^*$ and $\overline{x}_2^*$.

$$
\begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} = \underbrace{\begin{bmatrix} \phi_{11}(T_p) & \phi_{12}(T_p) \\ \phi_{21}(T_p) & \phi_{22}(T_p) \end{bmatrix}}_{\Phi^{o}(T_p)} \begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} + \underbrace{\begin{bmatrix} \phi_{11}(T_{off}^*)\, d_{11}(T_{on}^*) + \phi_{12}(T_{off}^*)\, d_{21}(T_{on}^*) \\ \phi_{21}(T_{off}^*)\, d_{11}(T_{on}^*) + \phi_{22}(T_{off}^*)\, d_{21}(T_{on}^*) \end{bmatrix}}_{\overline{V}} E_i \qquad \text{(C-10)}
$$

Hence

$$\begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} = \left[I - \phi^o(T_p) \right]^{-1} \bar{v} \tag{C-11}$$

The third state x_3^* is determined from the threshold condition (C-3)

$$x_3^* = E_T - \phi_{31}(T_{on}^*)\, x_1^* - \phi_{32}(T_{on}^*)\, x_2^* - d_{31}(T_{on}^*)\, E_i - d_{32}(T_{on}^*)\, E_R \tag{C-12}$$

The steady state solution $\bar{x}^*$ determined by this method is not exact because the power circuit is not completely lossless so that the dutycycle relationship of (C-8) is only an approximation, but a very good one. How well this $\bar{x}^*$ approximates the true equilibrium solution can be determined by checking how closely $\bar{x}_k$ and $\bar{x}_{k+1}$ match when using (C-2) for propagating the state through one cycle starting with $\bar{x}_k = \bar{x}^*$. The best method for determining the exact steady state, is to determine the exact T_{on}^* by iterative linearization (Newton's method) on the cycle to cycle matching condition for the third state (which is the integrator output and directly controls the threshold condition). The iterative process is started with approximate steady state values and thus converges usually very fast. The details of this procedure are described next.

Define the system state when the power switch turns off as

$$\bar{z}_k \triangleq \bar{x}(t_k+T_{on}^k) \tag{C-13}$$

and clearly

$$z_3(t_k) = E_T \qquad \text{for all } k = 0,1,2,\ldots \tag{C-14}$$

In the steady state one has

$$\begin{bmatrix} z_1^* \\ z_2^* \\ z_3^* \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 \\ \phi_{21} & \phi_{22} & 0 \\ \phi_{31} & \phi_{32} & 1 \end{bmatrix}_{T_{on}^*} \cdot \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} + \begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix}_{T_{on}^*} \begin{bmatrix} E_i \\ E_R \end{bmatrix} \tag{C-15}$$

Clearly, if $\bar{x}^*$ and T_{on}^* are the exact steady state values, then one must satisfy the state matching condition

$$S_{match} = x_3^* - \left[\phi_{31}(T_{off}^*)\, z_1^* + \phi_{32}(T_{off}^*)\, z_2^* + E_T + d_{32}(T_{off}^*)\, E_R\right] = 0 \tag{C-16}$$

since the square-bracketed term should equal x_3^*. Note now that via Equations (C-11), (C-12) and (C-15), the function S_{match} is really only a function of T_{on}^* ($T_{off}^* = T_p - T_{on}^*$), and one wishes to determine T_{on}^* such that

$$S_{match}(T_{on}^*) = 0 \tag{C-17}$$

Iterative linearization (Newton's method) can now be applied to (C-17) to find T_{on}^*, by expanding S_{match} about the approximate steady state solution in a Taylor series and retaining only the linear term, i.e.,

$$S_{match}(T_{on}^*) = S_{match}(\hat{T}_{on}^*) + \left.\frac{\partial S_{match}}{\partial T_{on}}\right|_{\hat{T}_{on}^*} (T_{on}^* - \hat{T}_{on}^*) \tag{C-18}$$

where $\hat{T}_{on}^*$ is the approximate steady state value from (C-8). Since $S_{match}(T_{on}^*) = 0$, it follows that

$$T_{on}^* = \hat{T}_{on}^* - \frac{S_{match}(\hat{T}_{on}^*)}{[\partial S_{match}/\partial T_{on}]_{\hat{T}_{on}^*}} . \tag{C-19}$$

If this T_{on}^{*} satisfies $|S_{match}| < \varepsilon$, ε some very small number, the exact steady state has been found; if not, set $\tilde{T}_{on}^{*} = T_{on}^{*}$ and repeat the process until S_{match} converges to zero. Convergence is usually very fast and within 1-3 iterations. Describing the process sounds much more complicated than it actually is, and for completeness a computer flow diagram for determining the steady state solution is included. Note that the partial derivative $\partial S_{match}/\partial T_{on}$ is taken numerically by approximation by a difference quotient. Note that the difference between $\overline{x}^{*}$ and $\overline{z}^{*}$ denotes the peak-to-peak steady state ripple, provided the inductor current i and output voltage e_0 are in phase. This is usually the case, unless the series equivalent resistance R_5 of the capacitor C_0 is equal to zero.

C.3. LINEARIZED SYSTEM

The nonlinear, discrete time system described by Equations (C-2) and (C-3) will now be linearized about its steady-state equilibrium state $\overline{x}^{*}$. Denoting

$$\delta\overline{x}(t_k) = \overline{x}(t_k) - \overline{x}^{*} \quad \text{and} \quad \delta E_i(t_k) = E_i(t_k) - E_i^{*} \tag{C-20}$$

it follows that

$$\begin{aligned}\delta\overline{x}(t_{k+1}) = & \left\{\Phi(T_p) + \frac{\partial}{\partial\overline{x}}\left[\Phi(T_{off}^{k})\, D(T_{on}^{k})\, \overline{u}_1 + D(T_{off}^{k})\, \overline{u}_o\right]\Big|_{\overline{x}^{*},E_i^{*}}\right\}\delta\overline{x}(t_k) \\ & + \frac{\partial}{\partial E_i}\left[\Phi(T_{off}^{k})\, D(T_{on}^{k})\, \overline{u}_1 + D(T_{off}^{k})\, \overline{u}_o\right]\Big|_{\overline{x}^{*},E_i^{*}} \delta E_i(t_k)\end{aligned} \tag{C-21}$$

where it is important to note that T_{on}^{k} and T_{off}^{k} are functions of $\overline{x}$ and E_i via the threshold condition (C-3) which is here rewritten as $\zeta(\overline{x},E_i,T_{on}) = 0$, i.e.,

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$$\zeta(\overline{x},E_i,T_{on}) \;=\; -E_T + \phi_{31}(T_{on})\,x_1 + \phi_{32}(T_{on})\,x_2 + x_3 + d_{31}(T_{on})\,E_i + d_{32}(T_{on})\,E_R \;=\; 0 \qquad \text{(C-22)}$$

In the previous developments above it has been tacitly assumed that $E_i = E_i^* =$ constant for all time. This is not necessarily so and the non-linear discrete time system (C-2) - (C-3) is also an exact description of the converter if E_i is time-varying, provided E_i remains constant over any T_{on} period. To assume a time-varying E_i composed of the nominal dc value E_i^* plus a small super-imposed ac component δE_i, is a useful concept when investigating audio susceptibility of the converter and is the main reason why it is included here in the derivation of the linearized system. Note that a significant difference between the constant T_{on} control and the present, constant frequency mode of operation, is that T_{on} is directly dependent on E_i in the threshold condition (C-22).

Denoting the first curly bracketed term in (C-21) by Ψ, a constant 3x3 matrix, and the second curly bracketed term by Γ, a constant 3-dimensional column vector, Equation (C-21) can now be written as

$$\delta\overline{x}(t_{k+1}) \;=\; \Psi\,\delta\overline{x}(t_k) + \Gamma\,\delta E_i(t_k) \qquad \text{(C-23)}$$

and represents the sought linearized system. The matrix Ψ and the column vector Γ remain to be evaluated, however.

By definition,

$$\Psi \;=\; \Phi(T_p) + \frac{\partial}{\partial \overline{x}}\left[\Phi(T_{off}^k)\,D(T_{on}^k)\,\overline{u}_1 + D(T_{off}^k)\,\overline{u}_o\right]\Bigg|_{\overline{x}^*,E_i^*} \qquad \text{(C-24)}$$

To evaluate the partial derivatives of the square-bracketed term analytically, turns out to be a very difficult and tedious task, much more so, than for the constant T_{on} control. This is mainly because the matrices $D(T_{on}^k)$ and

$D(T^k_{off})$ are now involved, and compact analytical expressions are not available for them. The partial derivatives are therefore evaluated numerically by approximating them by difference quotients. Denote

$$\overline{f}(\overline{x},E_i) = \left[\Phi(T^k_{off})\, D(T^k_{on})\, \overline{u}_1 + D(T^k_{off})\, \overline{u}_0 \right] \tag{C-25}$$

and for sufficiently small Δx_i, $i = 1,2,3$,

$$\left.\frac{\partial \overline{f}}{\partial \overline{x}}\right|_{\overline{x}^*,E_i^*} \approx \begin{bmatrix} \frac{f_1(x_1^*+\Delta x_1)-f_1(x_1^*)}{\Delta x_1} & \cdots\cdots & \frac{f_1(x_3^*+\Delta x_3)-f_1(x_3^*)}{\Delta x_3} \\ \vdots & & \vdots \\ \frac{f_3(x_1^*+\Delta x_1)-f_3(x_1^*)}{\Delta x_1} & \cdots\cdots & \frac{f_3(x_3^*+\Delta x_3)-f_3(x_3^*)}{\Delta x_3} \end{bmatrix} \tag{C-26}$$

Since $\overline{x}$ does not appear explicitly in $\overline{f}$, in order to evaluate (C-26) one must first determine by how much T_{off} and T_{on} change due to a change Δx_i, $i = 1,2,3$, and then use the new T_{off} and T_{on} to compute the $f_i(x_j+\Delta x_j)$, $i,j = 1,2,3$. The threshold condition

$$\zeta(\overline{x},E_i,T_{on}) = 0 \tag{C-27}$$

(see A-22) is used to determine the change in T_{on} due to a change in $\overline{x}$ or E_i. Iterative linearization (Newton's method) is used to determine the new T_{on} that satisfies $\zeta = 0$ after $\overline{x}$ has been perturbed by Δx_i, $i = 1,2,3$.

The procedure for computing Γ of (C-23) which by definition is given by

$$\Gamma = \left. \frac{\partial \bar{f}}{\partial E_i} \right|_{\bar{x}^*, E_i^*} \tag{C-28}$$

is exactly the same as outlined above. The only problem with numerical differentiation is to select the appropriate increments Δx_j. At the present the increments are taken as 1% of the value of the independent variable, i.e.,

$$\Delta x_j = 0.01 \, |x_j^*| \tag{C-29}$$

Some experimentation with the increment size is advisable, since the accuracy of the partial derivatives depends on it. For instance, if the function varies rapidly, a very small increment is clearly required. On the other hand, if the increment is chosen needlessly too small, then the accuracy degrades because of numerical problems since in the limit, a difference quotient assumes numerically the value 0/0. Studies on the increment size and its effects on the results have also physically significant implications. If the linearized system shows high sensitivity to increment size, then this points out that the nonlinear system changes its behavior rather rapidly as it moves away from its equilibrium point, and the results obtained for the linearized system are only valid for very small perturbations about the equilibrium. A computationally more complex, but also more accurate way of computing a derivative numerically is to use the following approximation,

$$\left. \frac{\partial f}{\partial x} \right|_{x^*} = \frac{f(x^*+\Delta x) - f(x^*-\Delta x)}{2\Delta x} , \tag{C-30}$$

which "averages out" fast function changes and can detect discontinuities.

C.4. STABILITY OF THE LINEARIZED SYSTEM

The linearized system (C-23), i.e.,

$$\delta\overline{x}(t_{k+1}) = \Psi\ \delta\overline{x}(t_k) + \Gamma\ \delta E_i(t_k) \qquad \text{(C-31)}$$

is stable if and only if all the eigenvalues of Ψ are absolutely less than unity, i.e.,

$$|\lambda_i(\Psi)| < 1, \qquad i = 1,2,3 \qquad \text{(C-32)}$$

The eigenvalues are evaluated by the computer and changes in the eigenvalues as a function of system parameters can be plotted in the complex plane. The location of the eigenvalues, which are the roots of the system, does not only indicate stability, but also governs the transient behavior of the converter, i.e., damping and rapidity of response.

With the nominal parameter values as given in Table 2, of the main text, was unstable. While changes in such critical parameters as C_2, R_3, and n_2, as well as others, affected the system roots in one way or another, the only really effective parameter change for stabilizing the system was to decrease the dutycycle, i.e., to either increase the supply voltage E_i or to decrease the desired output voltage E_R. Figure C-2 shows a root locus plot as a function of the supply voltage E_i with E_R remaining constant at 20 volts. As can be seen, changes in E_i primarily move the negative real root, and at a value of E_i = 46 volts, i.e., a dutycycle of 0.435, the system is just barely stable. A reasonable operating point results when E_i = 50 volts, and it will be used in the following parameter variation studies.

Figure C-3 shows the effect of the lead capacitor C_2 on stability. Quite good operating points are achieved for C_2 between 5000 and 10,000 pF, with the system becoming unstable when C_2 grows beyond 35,000 pF.

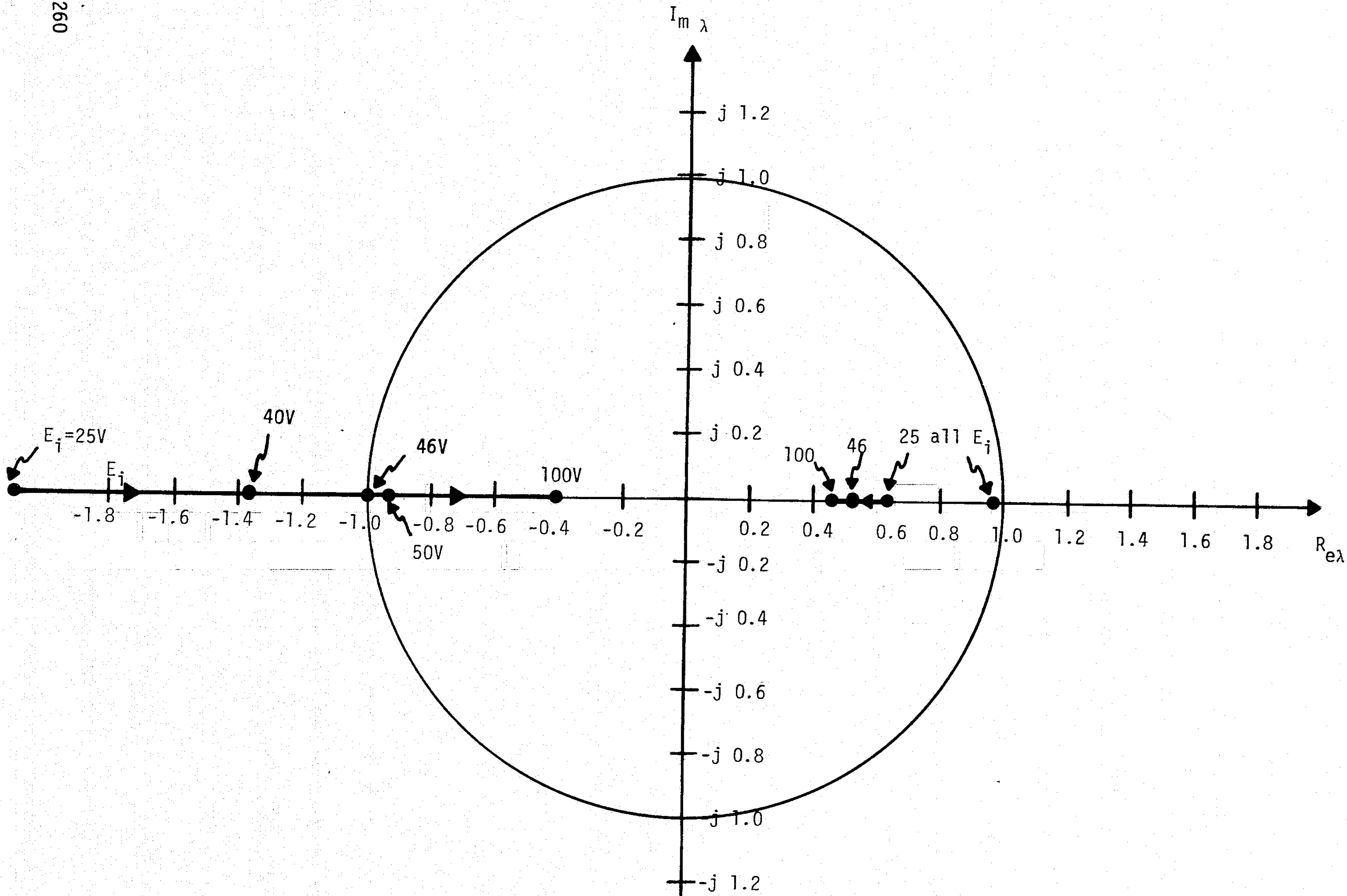

Figure C-2 Closed Loop Roots as a Function of Supply Voltage E_i

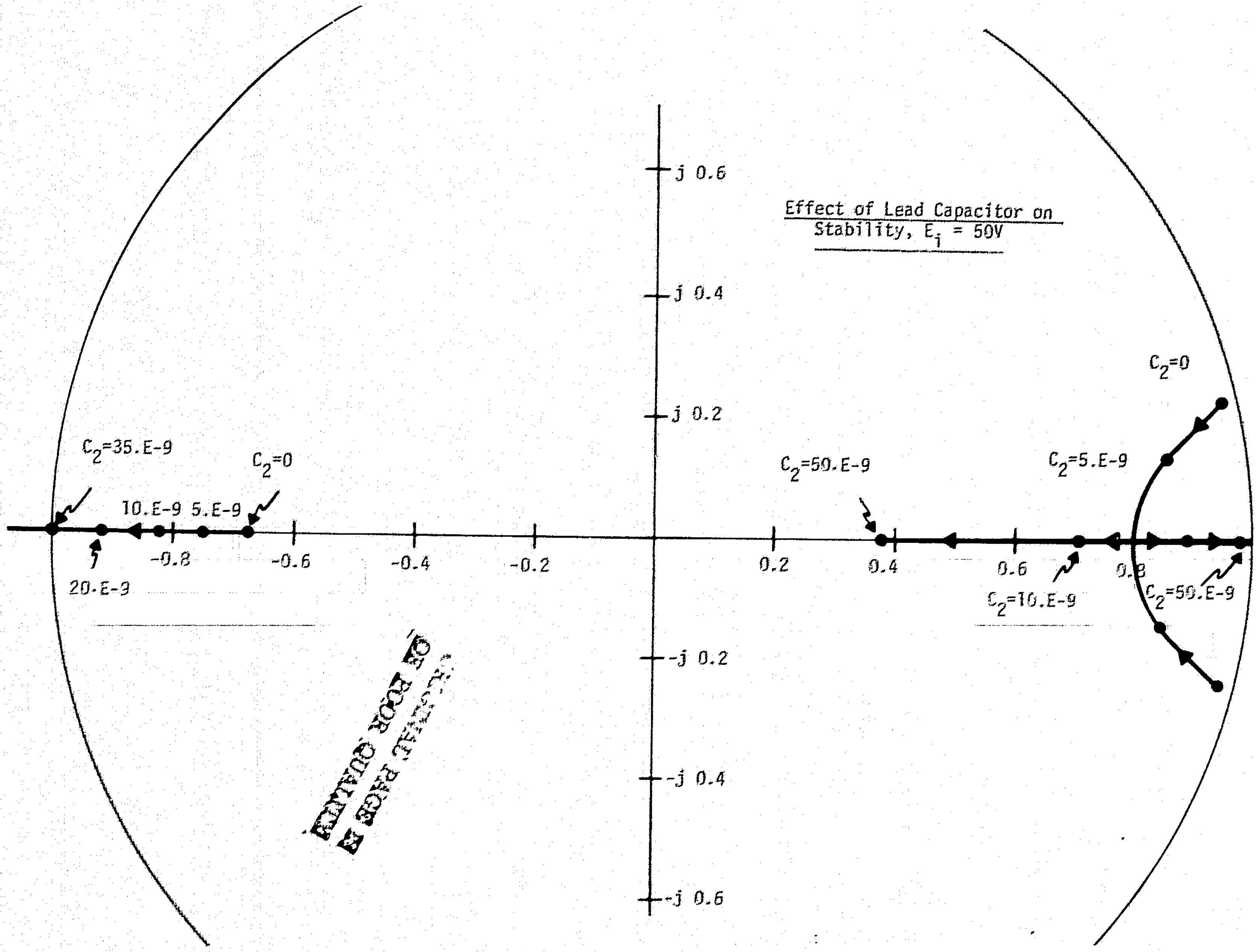

Figure C-3 Closed-Loop Roots as a Function of Lead Capacitor C2

APPENDIX D

BUCK REGULATOR DISCONTINUOUS CONDUCTION OPERATION

D.1 EQUIVALENT DISCRETE TIME SYSTEM

The waveform of e_i, as shown in Fig.D.1, is used to serve the purpose of establishing some notation regarding the time instant t_k when each cycle starts and each switching action occurs.

In steady state operation,

at t_k, t_{k+1}, t_{k+2} . . . . . the clock pulse turns the power switch "ON"

at t_1^k, t_1^{k+1}, t_1^{k+2} . . . . . the threshold condition turns the power switch "OFF"

at t_2^k, t_2^{k+1}, t_2^{k+2} . . . . . the zero inductor current condition turns off the power diode.

The time intervals $t_1^k - t_k$, $t_2^k - t_1^k$, and $t_{k+1} - t_2^k$ are defined as T_{ON}^K, T_{F1}^k and T_{F2}^k, respectively. These time intervals may vary from cycle to cycle. However, the time interval between t_k and t_{k+1} is a constant equal to the period of oscillation, i.e.,

$$t_{k+1} - t_k = T_P \quad \text{for all } k \qquad \text{(D-1)}$$

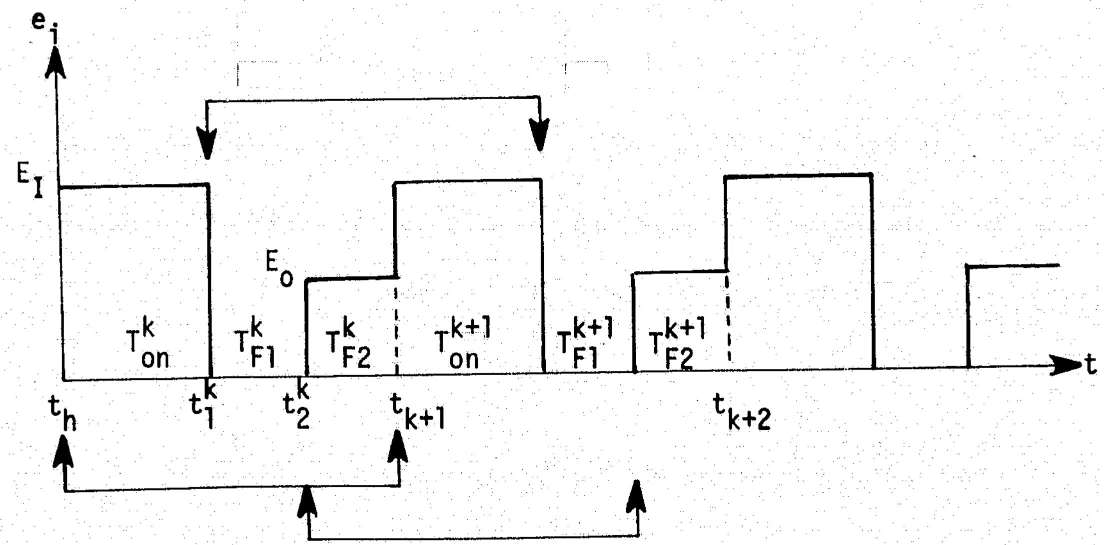

Figure D.1 Waveform of e_i

System equations of Fig.D.1 are represented by:

$$\dot{\underline{X}} = F1\underline{X} + G1\underline{U} \qquad t_k \leq t < t_1^k \qquad \text{(D-2)}$$

$$\dot{\underline{X}} = F2\underline{X} + G2\underline{U} \qquad t_1^k \leq t < t_2^k \qquad \text{(D-3)}$$

$$\dot{\underline{X}} = F3\underline{X} + G3\underline{U} \qquad t_2^k \leq t < t_{k+1} \qquad \text{(D-4)}$$

Where F1, F2, F3, G1, G2 and G3 are (3x3) constant matrix determined by the system parameters. They are:

$$F1=F2 = \begin{bmatrix} -\frac{1}{C_o(R_5+R_L)} - \frac{R_5R_L}{L_o(R_5+R_L)} & \frac{R_L}{C_o(R_5+R_L)} - \frac{R_oR_5R_L}{L_o(R_5+R_L)} & 0 \\ -\frac{1}{L_o} & -\frac{R_o}{L_o} & 0 \\ \frac{n}{R_4C_1} \quad \frac{k_d}{R_3C_1} \quad \frac{C_2}{C_1C_o(R_5+R_L)} \quad \frac{C_2R_5R_L}{C_1L_o(R_5+R_L)} & \frac{C_2R_oR_5R_L}{C_1L_o(R_5+R_L)} - \frac{R_LC_2}{C_1C_o(R_5+R_L)} & 0 \end{bmatrix}$$

$$F3 = \begin{bmatrix} -\frac{1}{C_o(R_5+R_L)} & \frac{R_L}{C_o(R_5+R_L)} - \frac{R_oR_5R_L}{L_o(R_5+R_L)} & 0 \\ 0 & -\frac{R_o}{L_o} & 0 \\ -\frac{k_d}{R_3C_1} + \frac{C_2}{C_1C_o(R_5+R_L)} & \frac{C_2R_oR_5R_L}{C_1L_o(R_5+R_L)} - \frac{R_LC_2}{C_1C_o(R_5+R_L)} & 0 \end{bmatrix}$$

$$G1 = \begin{bmatrix} \frac{R_5R_L}{L_o(R_5+R_L)} & 0 \\ \frac{1}{L_o} & 0 \\ -\frac{n}{R_4C_1} - \frac{C_2R_5R_L}{C_1L_o(R_5+R_L)} & \frac{k_d}{R_3C_1} \end{bmatrix}$$

and,

$$G_2 = G_3 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{k_d}{R_3 C_1} \end{bmatrix}$$

The vectors $\underline{X}$ and $\underline{U}$ are state variables and forcing function, respectively. They are defined as:

$$\underline{X} \triangleq \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} = \begin{bmatrix} e_o \\ i \\ e_c \end{bmatrix}$$

$$\underline{U} \triangleq \begin{bmatrix} U_1 \\ U_2 \end{bmatrix} \quad \begin{bmatrix} E_I \\ E_R \end{bmatrix}$$

The constraints of the system, as represented by (D-2) through (D-4) are governed by the threshold condition at $t = t_1^k, t_2^k \dots$

$$X_3 (t_k^1) = E_T, \tag{D-5}$$

the zero inductor current condition at $t = t_2^k, t_2^{k+1} \dots$

$$X_2 (t_k^2) = 0, \tag{D-6}$$

and the constant frequency condition

$$T_{ON}^k + T_{F1}^k + T_{F2}^k = T_p \quad \text{for all } k. \tag{D-7}$$

Each of the linear systems of equations (D-2) to (D-4) admits a closed form solution of the form.

$$\underline{X}(t_k^1) = \underline{X}(t_k+T_{ON}^k) = \Phi 1(T_{ON}^k)\ \underline{X}\ (t_k) + D1(T_{ON}^k)\ \underline{U} \tag{D-8}$$

$$\underline{X}(t_k^2) = X(t_k^1+T_{F1}^k) = \Phi 2(T_{F1}^k)\ \underline{X}\ (t_k^1) + D2(T_{F1}^k)\ \underline{U} \tag{D-9}$$

$$\underline{X}(t_{k+1}) = \underline{X}(t_k^2+T_{F2}^k) = \Phi 3(T_{F2}^k)\ \underline{X}\ (t_k^2) + D3(T_{F2}^k)\ \underline{U} \tag{D-10}$$

$$\text{where } \Phi i(T) = e^{FiT} \qquad i = 1, 2, 3 \tag{D-11}$$

$$Di(T) = e^{Fit}[\ \int_0^T e^{-FiS} dS\ ]\ Gi \qquad i = 1, 2, 3 \tag{D-12}$$

The structures of the matrices Φi and Di for i = 1, 2, 3 have the following forms:

$$\Phi i = \begin{bmatrix} \Phi i_{11} & \Phi i_{12} & 0 \\ \Phi i_{21} & \Phi i_{22} & 0 \\ \Phi i_{31} & \Phi i_{32} & 1 \end{bmatrix}$$

$$D1 = \begin{bmatrix} d1_{11} & 0 \\ d1_{21} & 0 \\ d1_{31} & d1_{32} \end{bmatrix}$$

$$Di = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & di_{32} \end{bmatrix} \qquad \text{for } i = 2, 3$$

The equivalent discrete time system for the constant frequency boost converter is given by:

$$\underline{X}(t_{k+1}) = \Phi 3(T_{F2}^k)\ \Phi 2(T_{F1}^k)\ \Phi 1(T_{ON}^k)\ \underline{X}\ (t_k) + \Phi 3(T_{F2}^k)\ \Phi 2(T_{F1}^k)\ D1(T_{ON}^k)\ \underline{U}$$
$$+ \Phi 3(T_{F2}^k)\ D2(T_{F1}^k)\ \underline{U} + D3(T_{F2}^k)\ \underline{U} \tag{D-13}$$

together with the threshold condition derived from (D-5)

$$\Phi 1_{31}(T_{ON}^k)\ X_1(t_k) + \Phi 1_{32}(T_{ON}^k)\ X_2(t_k) + \Phi 1_{33}(T_{ON}^k)\ X_3(t_k) + d1_{31}(T_{ON}^k)\ U_1$$
$$+ d1_{32}(T_{ON}^k)\ U_2 = E_T, \tag{D-14}$$

and the zero inductor current condition, derived from (D-6)

$$\Phi 2_{21}(T_{F1}^k)\ X_1(t_{k,1}) + \Phi 2_{22}(T_{F1}^k)\ X_2(t_{k,1}) = 0, \tag{D-15}$$

and the constant frequency condition

$$T_{F2}^k = T_P - T_{ON}^k - T_{F1}^k \tag{D-16}$$

D.2 EQUILIBRIUM SOLUTIONS

In the steady state the following conditions (D-17 to D-20) are satisfied:

$$\underline{X}(t_{k+1}) = \underline{X}(t_k) = \underline{X}^* = \text{constant} \qquad \text{for all } k \tag{D-17}$$

$$T_{ON}^{k+1} = T_{ON}^{k} = T_{ON}^{*} = \text{constant} \tag{D-18}$$

$$T_{F1}^{k+1} = T_{F1}^{k} = T_{F1}^{*} = \text{constant} \tag{D-19}$$

$$T_{F2}^{k+1} = T_{F2}^{k} = T_{F2}^{*} = \text{constant} = T_p - T_{ON}^{*} - T_{F1}^{*} \tag{D-20}$$

D.2.1 The Approximate Steady State

The approximate T_{ON}^*, T_{F1}^* and T_{F2}^* can be computed using the following formula

$$T_{ON}^{*} = \sqrt{\frac{2L_o T_p P_o}{E_I(E_I - E_R)}} \tag{D-21}$$

$$T_{F1}^{*} = \sqrt{\frac{2L_o T_p P_o\,(E_I - E_R)}{E_I\,E_R^2}} \tag{D-22}$$

$$T_{F2}^{*} = T_p - T_{ON}^{*} - T_{F1}^{*} \tag{D-20}$$

where L_o = the energy storage inductance

P_o = output power

E_I = input voltage

E_R = output voltage

Substituting (D-17 to (D-20) into (D-13), one obtains:

$$\left.\begin{aligned} \underline{X}^* &= \Phi 3(T^*_{F2})\ \Phi 2(T^*_{F1})\ \Phi 1(T^*_{ON})\ \underline{X}^* \end{aligned}\right\} \Phi(T^*_{ON}, T^*_{F1}, T^*_{F2})\ \underline{X}^*$$

$$\left.\begin{aligned} &+ [\Phi 3(T^*_{F2})\ \Phi 2(T^*_{F1})\ D1(T^*_{ON}) \\ &+ \Phi 3(T^*_{F2})\ D2(T^*_{F1}) + D3(T^*_{F2})\ ]\ \underline{U} \end{aligned}\right\} \underline{V}\ \underline{U}$$

$$\stackrel{\Delta}{=} \Phi\ (T^*_{ON}, T^*_{F1}, T^*_{F2})\ \underline{X}^* + \underline{V}\ (T^*_{ON}, T^*_{F1}, T^*_{F2})\ \underline{U} \qquad \text{(D-23)}$$

The magnitudes of T^*_{ON}, T^*_{F1}, and T^*_{F2} are obtained from equations (D-20) to (D-22)

Equation (D-23) can be solved for $\underline{X}^*$.

Let $\qquad X^*_2 = 0 \qquad$ (D-24)

then

$$\begin{aligned} X^*_1 = {} & [\Phi 3_{11}(\Phi 2_{11}\ \Phi 1_{11}+\Phi 2_{12}\Phi 1_{21}) + \Phi 3_{12}(\Phi 2_{21}\Phi 1_{11}+\Phi 2_{22}\Phi 1_{21})]\ X^*_1 \\ & + (\Phi 3_{11}\Phi 2_{11}d1_{11}+\Phi 3_{11}\Phi 2_{12}d1_{21} + \Phi 3_{12}\Phi 2_{21}d1_{11}+\Phi 3_{12}\Phi 2_{22}d1_{21})\ E_I \\ & + (\Phi 3_{11}d2_{11} + \Phi 3_{12}d2_{21})\ E_I \\ & + d3_{11}E_I \end{aligned}$$

Equation (D-21) can be solved for X^*_1..

$$\begin{aligned} X^*_1 = {} & \frac{1}{1 - [\Phi 3_{11}(\Phi 2_{11}\Phi 1_{11}+\Phi 2_{12}\Phi 1_{21}) + \Phi 3_{12}(\Phi 2_{21}\Phi 1_{11}+\Phi 2_{22}\Phi 1_{21})]} \\ & \{\Phi 3_{11}[\Phi 2_{11}d1_{11}+\Phi 2_{12}d1_{21}+d2_{11}] + \Phi 3_{12}[\Phi 2_{21}d1_{11}+\Phi 2_{22}d1_{21} \\ & + d2_{21}] + d3_{11}\ \}\ E_I \end{aligned} \qquad \text{(D-25)}$$

The state X_3^* can be derived from equation (D-14)

$$X_3^* = E_T - \Phi 1_{31} X^*_1 - \Phi 1_{32} X_2^* - d1_{31} E_I - d1_{32} E_R \tag{D-26}$$

In this approximation, the threshold condition where the inductor current equals zero may not be satisfied. This approximation is merely employed as a starting point in order to search for the exact steady state.

D.2.2 The Exact Steady State

Define the system state when the power switch turns off as

$$\underline{Y}(t_k) \triangleq \underline{X}\ (t_k + T_{ON}^k) \tag{D-27}$$

$$Z(t_k) \triangleq \underline{X}\ (t_k + T_{ON}^k + T_{F1}^k) \tag{D-28}$$

and clearly

$$Y_3(t_k) = E_T \qquad \text{for all } k \tag{D-29}$$

$$Z_2(t_k) = 0 \tag{D-30}$$

In the steady state operation

$$\underline{Y}^* = \Phi 1(T_{ON}^*)\underline{X}^* + D1(T_{ON}^*)\underline{U} = f1(T_{ON}^*, \underline{X}^*) \tag{D-31}$$

$$\underline{Z}^* = \Phi 2(T_{F1}^*)\underline{Y}^* + D2(T_{F1}^*)\underline{U} = f2(T_{F1}^*, \underline{Y}^*) \tag{D-32}$$

and

$$\underline{X}^* = \Phi 3(T_{F2}^*)Z^* + D3(T_{F2}^*)\ \underline{U} \tag{D-33}$$

It is important to note that T_{ON}^* and T_{F1}^* are functions of $\underline{X}^*$, $\underline{U}$ via the threshold conditions (D-29) and (D-30).

If T_{ON}^* and T_{F1}^* are the exact steady state values, the steady state $\underline{X}^*$ calculated from (D-24) to (D-26) has to satisfy the following two matching conditions.

(1) the zero-inductor-current condition

$$B_{match} = \Phi 2_{21}(T^*_{F1})\ Y_1 + \Phi 2_{22}(T^*_{F1})\ Y_2 = 0 \tag{D-34}$$

(2) the state matching condition

$$S_{match} = \Phi 3_{d1}(T^*_{F2})Z_1 + \Phi 3_{32}(T^*_{F2})\ Z_2 + E_T$$

$$+ d3_{32}(T^*_{F2})\ U_2 - X^*_3 = 0 \tag{D-35}$$

Iteration linearization (Newton's method) is employed to find T^*_{ON} and T^*_{F1} which satisfies the matching conditions

$$B_{match}(\underline{X}^*,\ T^*_{ON},\ T^*_{F1}) = 0$$

and

$$S_{match}(\underline{X}^*,\ T^*_{ON},\ T^*_{F1}) = 0$$

The step-by-step procedure is described as follows:

Step 1 Employing the approximate $\tilde{T}^*_{ON}$; $\tilde{T}^*_{F1}$ given in (D.21-22) derive the approximate state $\underline{X}^*$ from (D.24-26).

Step 2 Find a new T^*_{F1} by iteration linearization method

$$T^*_{F1} = \tilde{T}^*_{F1} - \frac{B_{match}(\tilde{T}^*_{ON}),\ \underline{\tilde{X}},\ \tilde{T}^*_{F1})}{[\partial B_{match}/\partial T_{F1}]\ \tilde{T}^*_{F1}}$$

such that for the given $\tilde{X}^*$ and $\tilde{T}^*_{ON}$ together with the new T^*_{F1}, the zero-current condition $B_{match}(\tilde{T}^*_{ON},\ \underline{\tilde{X}}^*,\ T^*_{F1}) = 0$ will be satisfied.

Step 3 Check if $S_{match} = 0$ is satisfied?

Step 4 If $S_{match} = 0$ is not satisfied, modify T^*_{ON} according to

$$T^*_{ON} = \tilde{T}^*_{ON} - \frac{S_{match}(\tilde{T}^*_{ON}, T^*_{F1})}{[\partial S_{match}/\partial T_{ON}]_{\tilde{T}^*_{ON}}}$$

Step 5 Use the new T^*_{ON} and T^*_{F1} calculated in Step 2 and Step 4 to derive a new approximate state $\underline{\tilde{X}}^*$. Then to go to Step 2 and repeat the process until the state matching condition $S_{match} = 0$ is satisfied.

A flow diagram for determining the steady state is presented in Fig. D.2(a) and (b). A subroutine B_{match} is developed to search for a proper T_{F1} to satisfy the zero-inductor condition as shown in (D-34). This subroutine is embodied into another subroutine S_{match} which ultimately computes the state matching condition as given in (D-35).

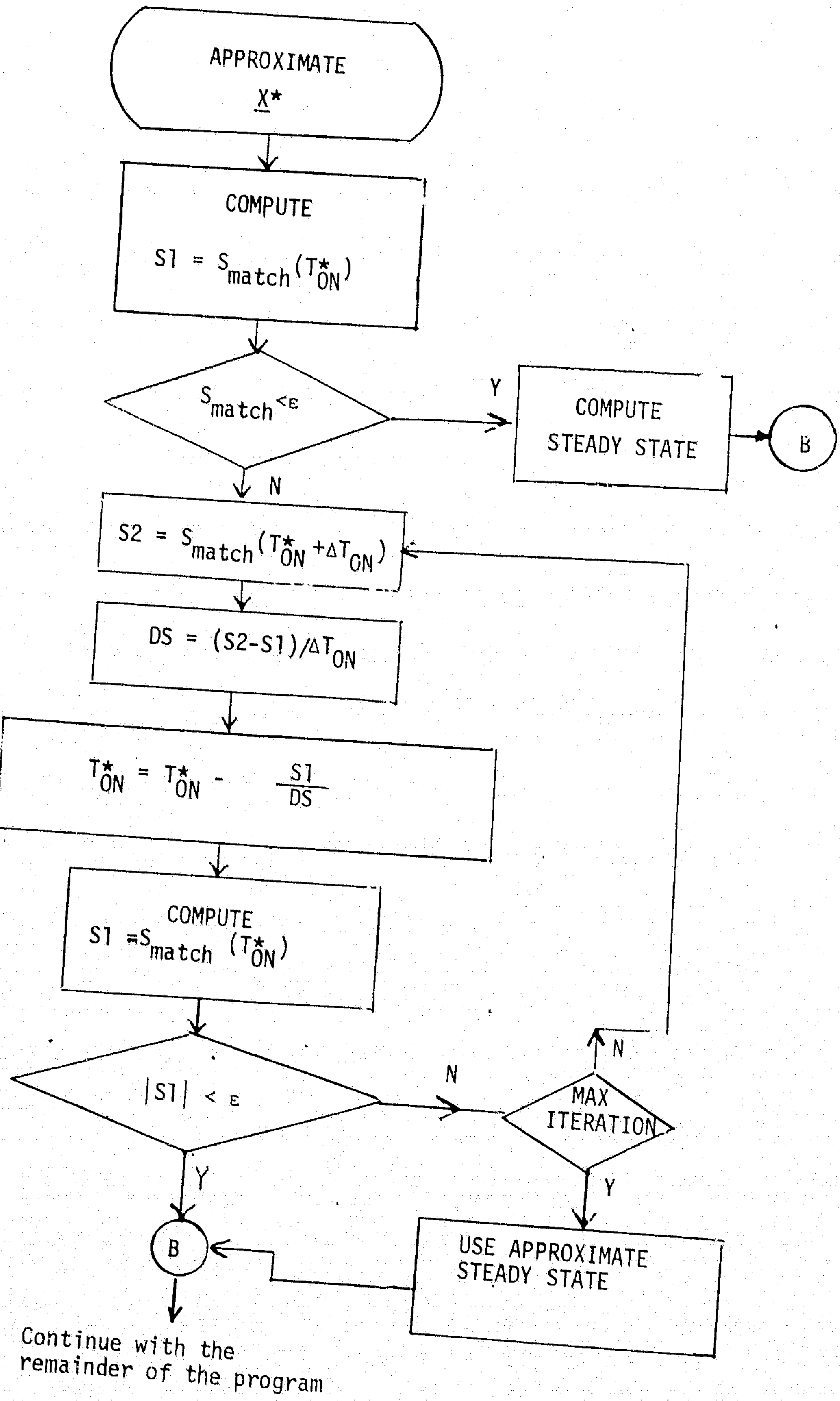

Figure D.2(a) Flow Diagram for Determining the Steady State

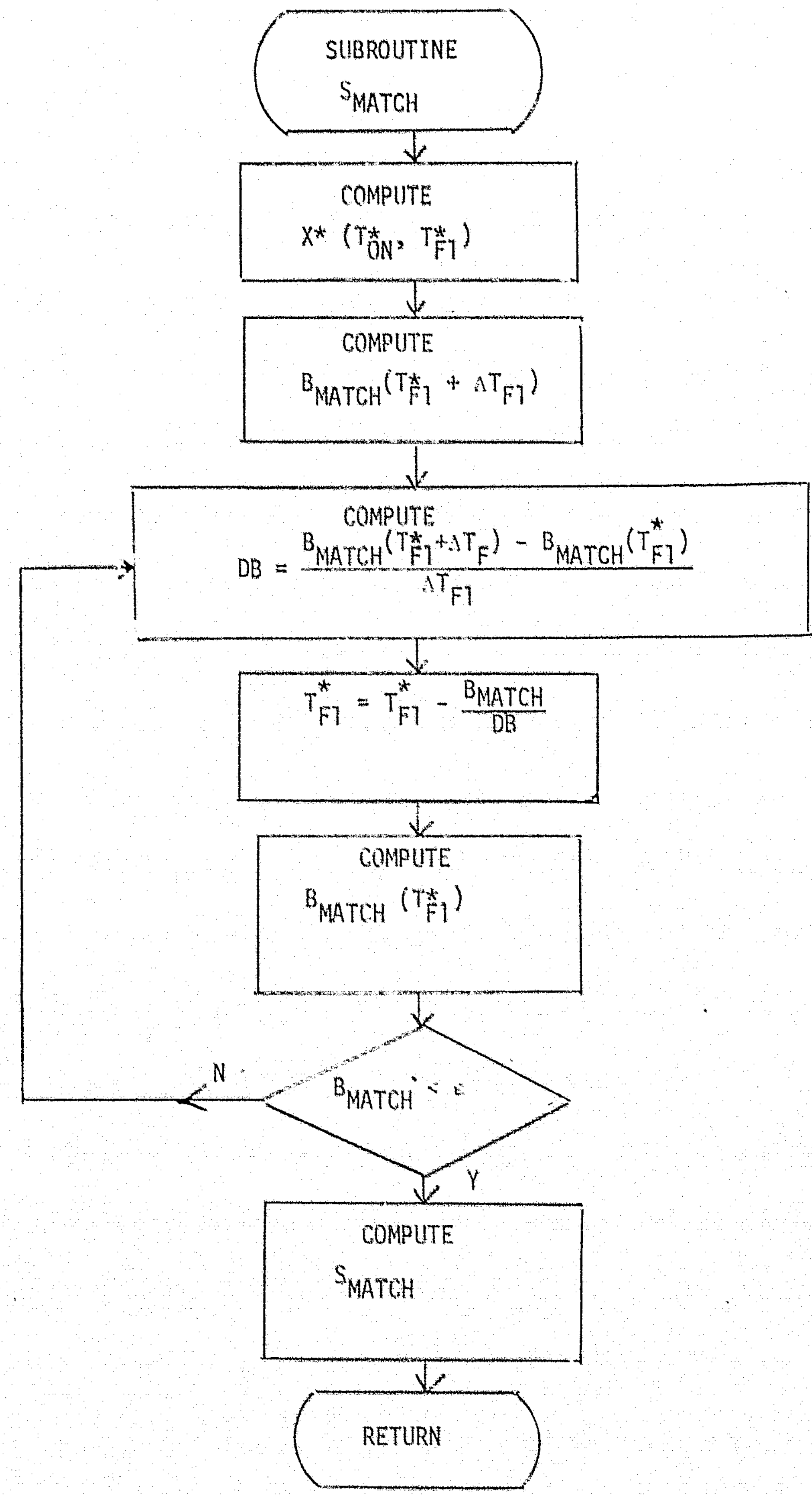

Figure D.2(b) Flow Diagram For Determining the Steady State

D.3 ANALYSIS OF LINEARIZED DISCRETE TIME SYSTEM

The analysis of stability, audio susceptibility, and transient response due to step change in the input voltage and the load is presented. The analysis is based on a linearized discrete system about its equilibrium state.

D.3.1 Derivation of Linearized System

The linearized system can be derived by perturbing the system at the kth cycle. After the perturbation the nonlinear discrete time system equation (D-13) can be rewritten as:

$$\underline{x}_{k+1} = \underline{f}\,(\underline{x}_k, \underline{U})$$

where
$$\underline{f}\,(\underline{X}_k, \underline{U}) = \Phi 3\,(T^k_{F2})\,\Phi 2\,(T^k_{F1})\,\Phi 1\,(T_{ON}{}^k)\,\underline{x}$$
$$+ \Phi 3\,(T^k_{F2})\,\Phi 2(T^k_{F1})\,D1\,(T^k_{ON})\,\underline{U}$$
$$+ \Phi 3\,(T^k_{F2})\,D2\,(T^k_{F1})\,\underline{U}$$
$$+ D3\,(T^k_{F2})\,\underline{U} \qquad \text{(D-36)}$$

This system can be linearized about its equilibrium state $\underline{x}^*$. Denoting:

$$\delta\underline{x}\,(t_k) = \underline{x}\,(t_k) - \underline{x}^*$$

and

$$\delta U_1\,(t_k) = U_1\,(t_k) - U_1{}^*$$

It follows that:

$$\delta\underline{x}\,(t_{k+1}) = \psi\,\delta\underline{x}\,(t_k) + \Gamma\delta U_1\,(t_k) \qquad \text{(D-37)}$$

where $\psi = \frac{\partial}{\partial x} \underline{f} (\underline{x}_k, \underline{U},) \Big|_{\underline{x}^*, \underline{U}^*}$ (D-38)

and $\Gamma = \frac{\partial}{\partial U_1} \underline{f} (\underline{x}_k, \underline{U}) \Big|_{\underline{x}^*, \underline{U}^*}$ (D-39)

The matrix ψ is (3x3) and the matrix Γ is (3x1).

The partial derivatives, approximated by difference quotients, are evaluated numerically by difference quotients.

For sufficiently small Δx_i, $i = 1, \ldots, 4$

$$\psi = \frac{\partial \underline{f}}{\partial \underline{x}} \Big|_{\underline{x}^*, \underline{U}^*} \approx \begin{bmatrix} \frac{f_1(x_1^*+\Delta X_1) - f_1(x_1^*)}{\Delta x_1} & - - - & \frac{f_1(x_3^*+\Delta x_3) - f_1(x_3^*)}{\Delta x_3} \\ & & \\ \frac{f_3(x_1^*+\Delta x_1) = f_3(x_1^*)}{\Delta x_1} & - - - & \frac{f_3(x_3^*+\Delta x_3) - f_3(x_3^*)}{\Delta x_3} \end{bmatrix} \tag{D-40}$$

Since $\underline{x}$ does not appear explicity in $\underline{f}$, in order to evaluate (D-40), the change of T_{on}, T_{F1}, and T_{F2} due to a change of Δx_i, $i = 1, \ldots, 3$, must be determined first. The new T_{on} and T_{F1} are computed according to the threshold conditions (D-14) and (D-15).

Similarly,

$$\Gamma = \frac{\partial f}{\partial u_1} \Big|_{\underline{x}^*, \underline{U}^*} \approx \begin{bmatrix} \frac{f_1(U_1+\Delta U_1) - f_1(U_1)}{\Delta U_1} \\ \\ \\ \frac{f_3(U_1+\Delta U_1) - f_3(U_1)}{\Delta U_1} \end{bmatrix}_{\underline{x}^*, \underline{U}^*} \tag{D-41}$$

It is important to select the appropriate increments Δx_j and ΔU_1. Some experimentation with the increment size is advisable, since the accuracy of the partial derivatives depends on it. If the linearized system shows high sensitivity to incremental size, then this points out that the non-linear system changes its behavior rather rapidly as it moves away from its equilibrium, and the result obtained for the linearized system are only valid for very small perturbations about the equilibrium.

D.3.2 The Stability of the Linearized System

The linearized system (D-37)

$$\delta \underline{x}(t_{k+1}) = \psi\ \delta \underline{x}\ (t_k) + \Gamma \delta U_1(t_k),$$

is stable if and only if all the eigenvalues of ψ are absolutely less than unity, i.e.,

$$|\lambda_i| < 1 \qquad i = 1, 2, 3, 4 \tag{D-42}$$

The eigenvalues are evaluated by the computer. Changes of eigenvalues as a function of system parameters can be plotted in the complex plane. The location of the eigenvalues in the complex plane indicates not only the stability but also the transient behavior of the system, i.e., damping and rapidity of response.

D.3.3. Stability Results

A computer program for the constant-frequency boost converter operating in the discontinuous inductor-current has been developed. Furthermore, the computer program developed previously in Appendix C for the same converter but operating in the continuous inductor-current was incorporated in the present program. Therefore, for a given set of circuit parameters, the main program first detected the modes of operation, the continuous current mode versus discontinuous current mode, then enter into the appropriate subroutine for the computa- tion. The stability nature of such a system when its inductor is operating on the merge from discontinuous mode to continuous mode is of particular interest on this phase of research and it is studied through such a program.

In the previous Appendix C , it was concluded that the con- verter was unstable for duty cycles higher than 50% and the only parameter change for stabilizing the system was to decrease the duty cycle. This statement again was verified by further investiga- tions. The results of two computer runs were presented in Figure D.3 and Figure D.4. The magnitude of the input voltage for these two runs was assigned 40 volts such that the converter is unstable. Decreasing the ac loop resistance, R_4 from 500KΩ, one eigenvalue λ3 asymptotically approached to -1 from outside the unit cycle and two other eigenvalues asymptotically approached to +1 from inside the unit cycle. The system cannot be stabilized by reducing the ac-loop resistance. Figure D.4 shows that the instability problem cannot be corrected by varying dc-loop-gain resistance R_3 from 1KΩ to 200KΩ.

The stability nature of the converter is studied by varying such important parameters as the input voltage to the regulator and the load in a manner that the operation of the converter varies from the continuous inductor-current mode to the discontinuous inductor current mode. Figure D.5 shows the change of eignevalues as a

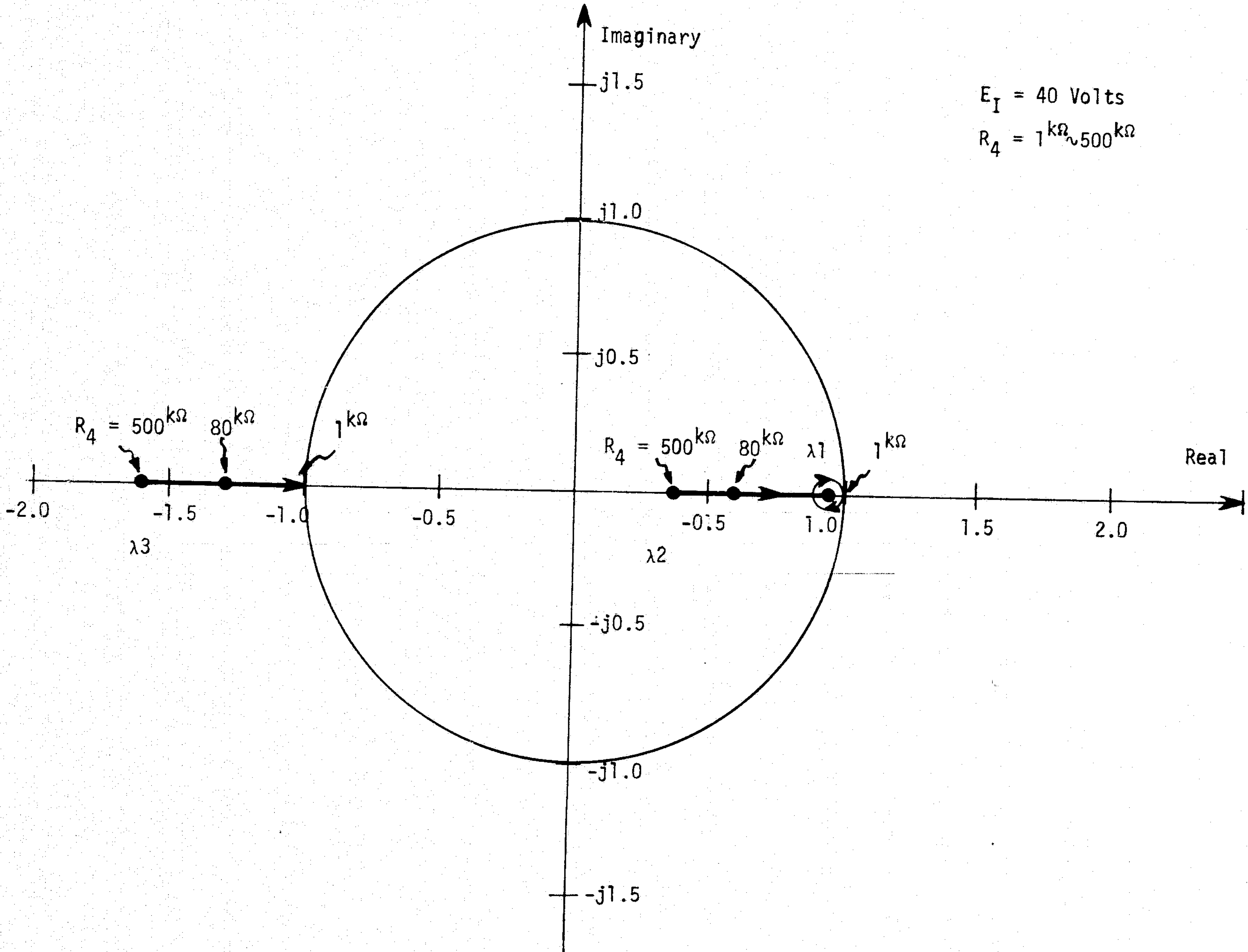

Figure D.3 Eigenvalues as a Function of AC Loop Resistance R_4.

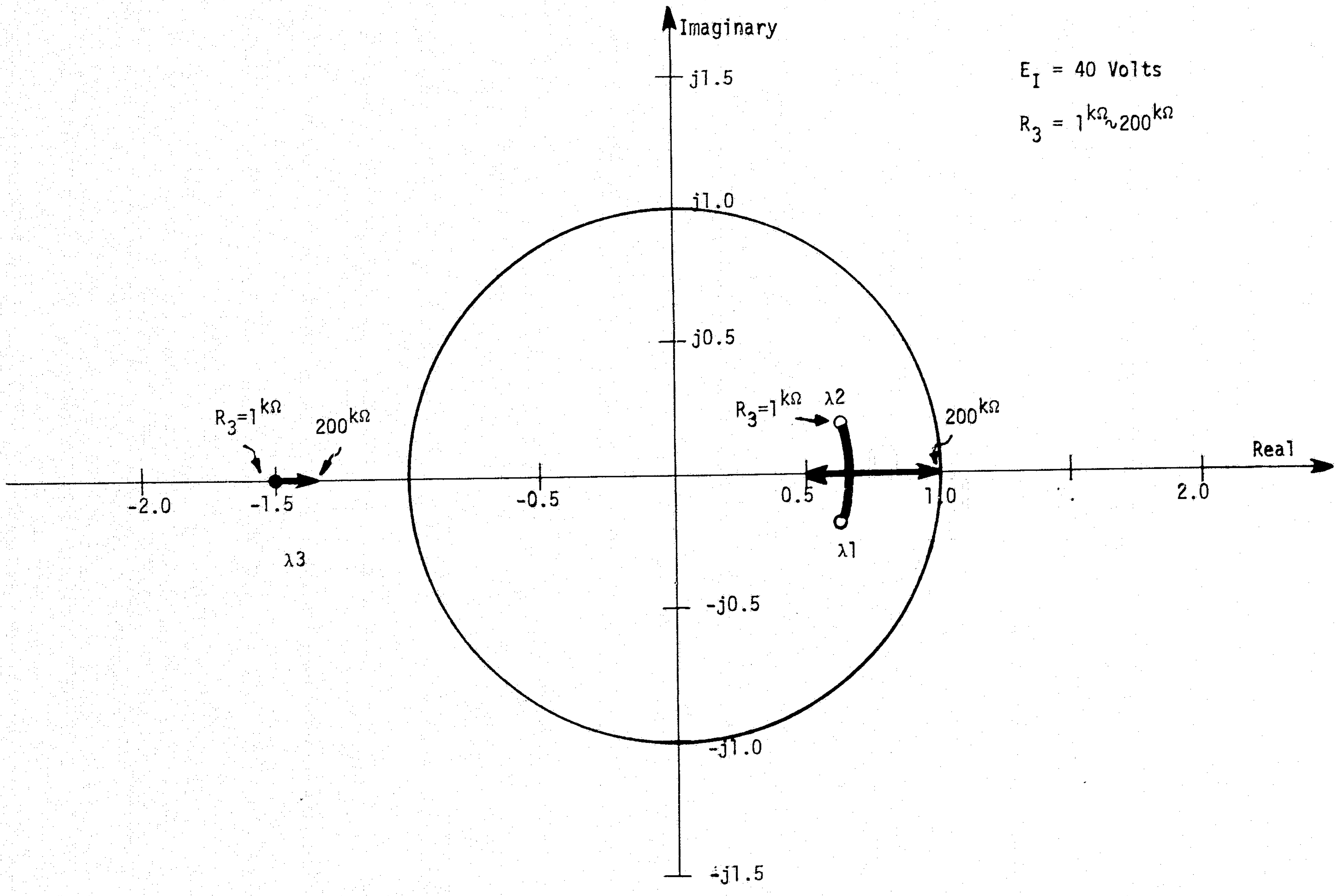

Figure D.4 Eigenvalues as a Function of DC Loop Resistance R_3.

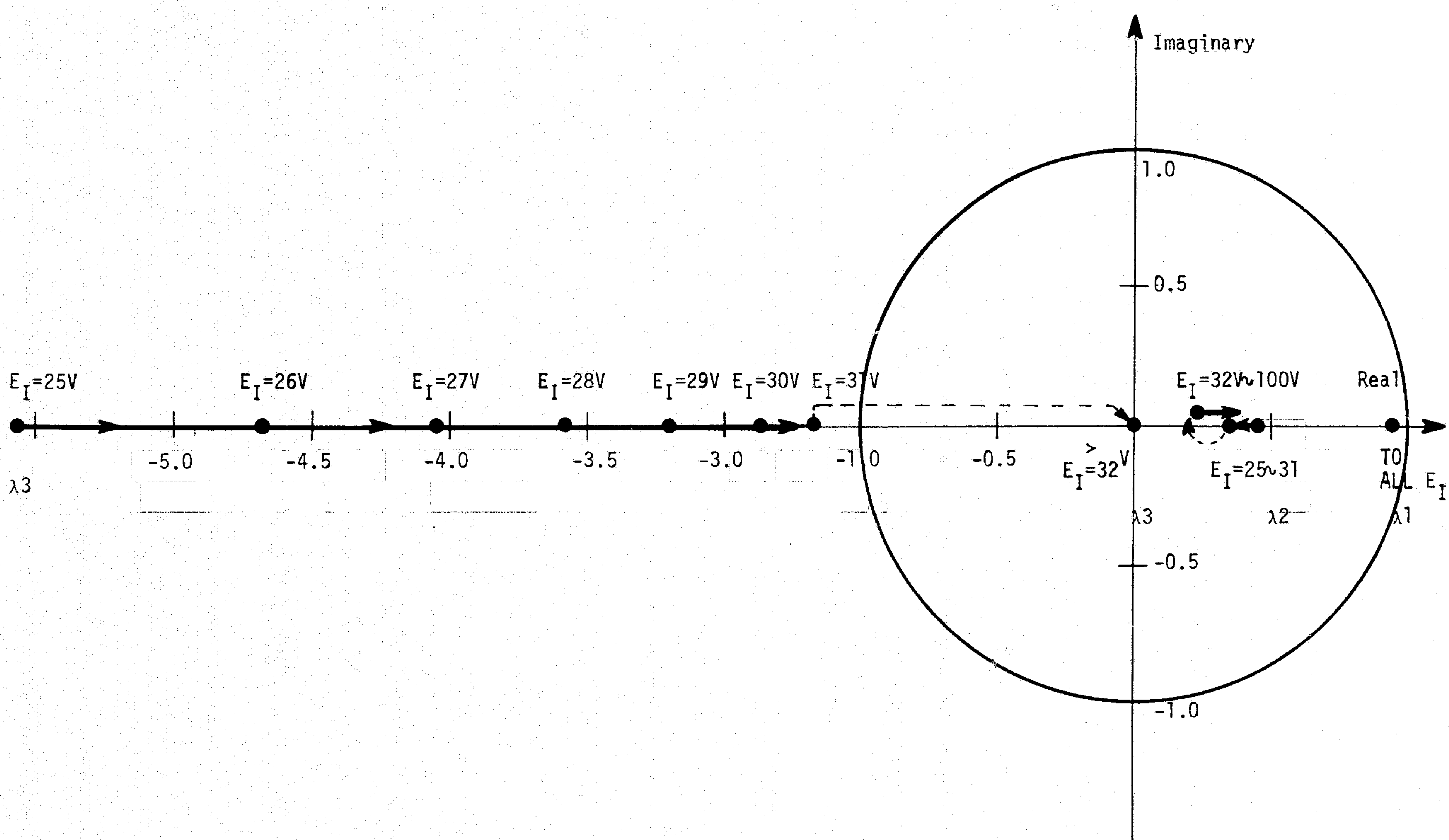

Figure D.5 Eigenvalues as a Function of Input Voltage function of the input voltage E_I, at $L_0 = 50\mu h$. When the magnitude of the input voltage is between 25 volts and 31 volts, the converter operates in the continuous current mode with a duty cycle greater than 50% and it is unstable. When the input voltage equals or is greater than 32 volts, all the three eigenvalues are inside the unit cycle and the system becomes stable regardless of the duty cycle ratio. It should be noted that during the input voltage variation, a jump phenomenon is observed. For example, as the input voltage varies from 31 volts to 32 volts, the eigenvalue $\lambda 3$ varies from 2.68 to 0 and it is caused by a jump phenomenon, not by a continuous motion which can be represented by intermediate value of E_I.

Figure D.6 shows the change of eigenvalues as a function of the load. When the load is relatively heavy, R_L = 10 ohms to 40 ohms, and the input voltage E_I = 30 volts, the converter operates in a continuous-current mode with a duty cycle ratio greater than 50%. The system is unstable. The system is stabilized by increasing R_L up to or above 50 ohms such that the converter begins to operate in the discontinuous-current mode. The jump phenomenon is again manifested by investigating the change of eigenvalues in Figure D.6.

Figure D.7 is another plot of eigenvalues as a function of load for a given supply voltage E_I = 50 volts. The converter first operates in a continuous - current mode for R_L equal to 10 ohms and 20 ohms and then operates in a discontinuous - current mode for R_L greater than 30 ohms. The eigenvalues λ_1 and λ_2 both approach unity as R_L approaches infinity. The system is stable under all load conditions.

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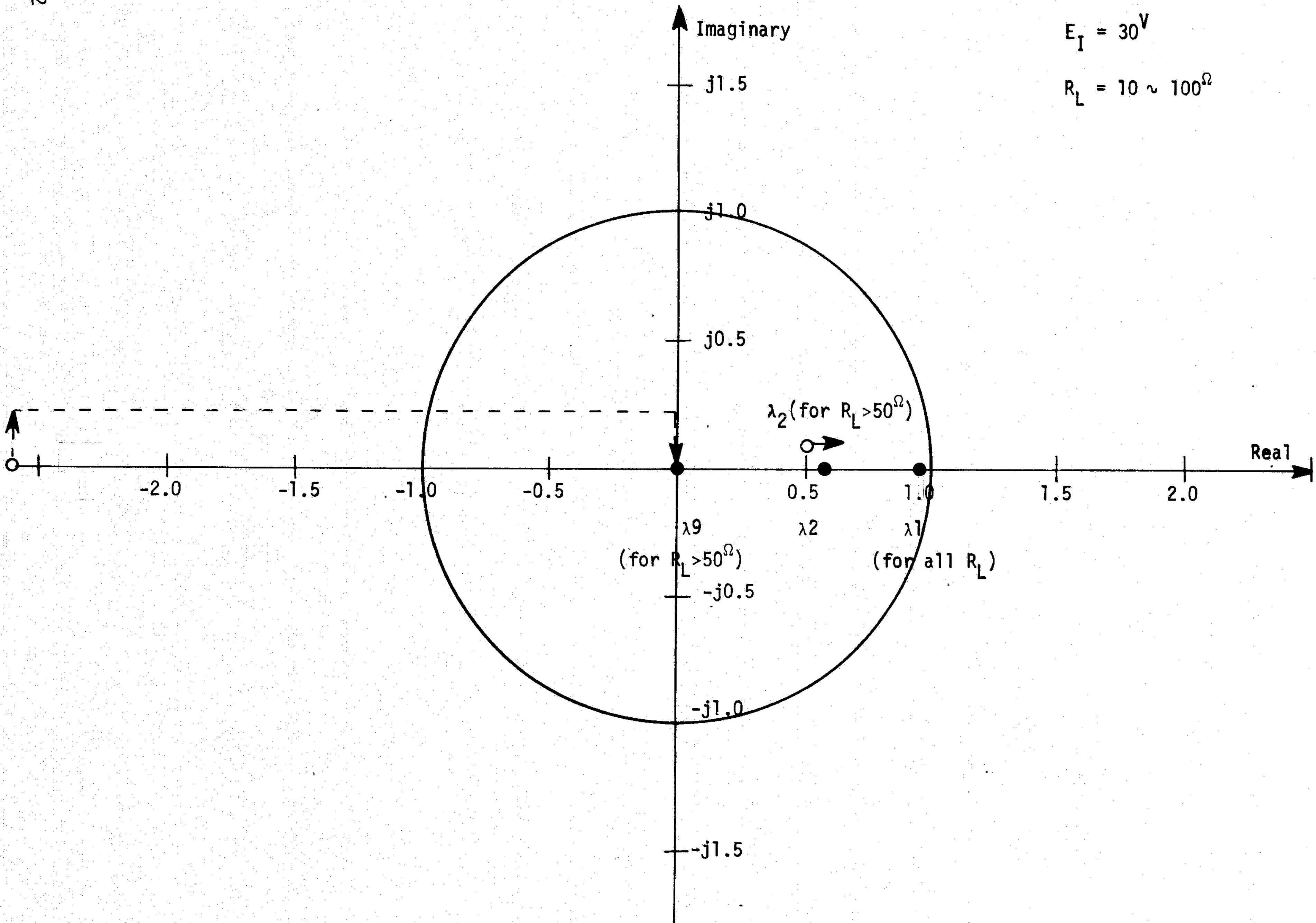

Figure D.6 Eigenvalues as a Function of Load When E_I = 30 Volts

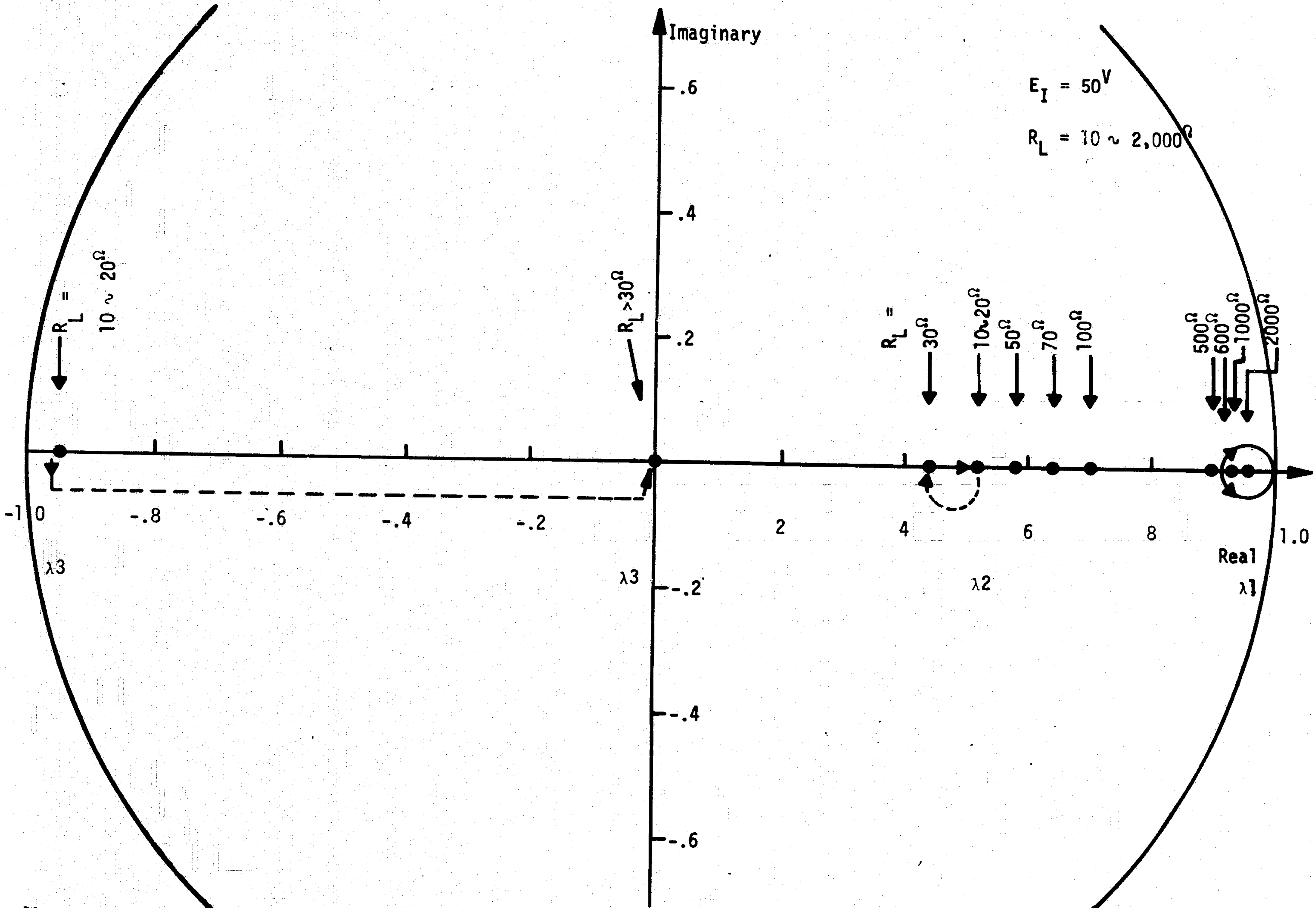

Fig. D.7 Eigenvalues as a Function of Load When E_I = 50 Volts

APPENDIX E

COMPUTER LISTING FOR A BUCK REGULATOR DISCRETE TIME DOMAIN ANALYSIS HANDLING BOTH THE CONTINUOUS AND DISCONTINUOUS CONDUCTION OPERATIONS

```
      PROGRAM BUCK(INPUT,OUTPUT,TAPE3=INPUT,
     XTAPE4,TAPE2)
      DIMENSION RIPX(3,1),PSI(3,3),PSY(3,3),GAM(3,1),INT(8),
     XXFP(3,1),PRAM(10),H(3),R(3,5),ITBL(3),IVD(3),DELX(3,1),
     XPHI1(3,3),PHI2(3,3),PHI3(3,3),D1(3,2),D2(3,2),D3(3,2),
     XTEMP1(3,3),TVEC1(3),PHIP(3,3)
      COMMON /PARAM/F1(3,3),F2(3,3),F3(3,3),G1(3,2),G2(3,2),
     XG3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      COMMON /STATE/X(3,1),Y(3,1),Z(3,1),U(2,1)
      EQUIVALENCE (PRAM(1),C1),(PRAM(2),C2),(PRAM(3),R3),
     X (PRAM(4),R4),(PRAM(5),R5),(PRAM(6),RN2),(PRAM(7),XLO),
     X (PRAM(8),CO),(PRAM(9),RL),(PRAM(10),EI)
      DATA EI, ER, ET, RL, TP/50.,20.,8.,10.,30.E-6/
      DATA EISWIT,XMU/60.,0.01/
      DATA XLO,RO,CO,R5,RN1,RN2/25.E-5,0.015,3.E-4,0.077,40.,26./
      DATA C1,C2,R1,R2,R3,R4/2200.E-12,0.022E-6,28.7E3,
     X13.5E3,10.E3,100.E3/
      DATA THETAO,DELTHET,THETAF,H/0.,5.,180.,1.,0.,0./
      DATA NIT,EPS/100,1.E-6/
      DATA MODE/2/
      DATA IPLOT,LIST,LPEAK,LFF,NK,LFREQ/0,0,0,0,15,0/
      DATA LRTL,NRL,DPRAM,PRAMF/0,2,0.,0./
      NAMELIST/TERMS/EI,ER,ET,RL,TP,XLO,RO,CO,R5,RN1,RN2,NK,
     XC1,C2,R1,R2,R3,R4,NIT,EPS,IPLOT,LIST,EISWIT,XMU,LPEAK,
     X LFREQ,THET O,DELTHET,THETAF,H,LRTL,NRL,DPRAM,PRAMF
      READ(3,TERMS)
      REWIND 2
      REWIND 4
      IF (LIST .EQ. 1) WRITE (2,TERMS)
    5 CONTINUE
      RKD=R2/(R1+R2)
      RN=RN2/RN1
      DO 8 I=1,3
      G1(I,1)=G1(I,2)=G2(I,1)=G2(I,2)=G3(I,1)=G3(I,2)=0.
      DO 8 J=1,3
    6 F1(I,J)=F2(I,J)=F3(I,J)=0.
      F1(1,1)=F2(1,1)=-1./(RL*CO+R5*CO)-R5*RL/(XLO*RL+XLO*R5)
      F3(1,1)=-1./(CO*(R5+RL))
      F1(1,2)=F2(1,2)=F3(1,2)=RL/(CO*RL+CO*R5)-RO*R5*RL/(XLO*RL+
     XXLO*R5)
      F1(2,1)=F2(2,1)=-1./XLO
      F1(2,2)=F2(2,2)=F3(2,2)=-RO/XLO
      F1(3,1)=F2(3,1)=C2/(RL*C1*CO+R5*C1*CO)+RN/(R4*C1)-RKD/(R3*
     X C1)+C2*R5*RL/(C1*XLO*RL+C1*XLO*R5)
      F3(3,1)=-RKD/(R3*C1)+C2/(RL*C1*CO+R5*C1*CO)
      F1(3,2)=F2(3,2)=F3(3,2)=C2*RO*R5*RL/(C1*XLO*R5+C1*XLO*RL)-
     X RL*C2/(C1*CO*R5+C1*CO*RL)+RN*RO/(R4*C1)
      G1(1,1)=R5*RL/(XLO*R5+XLO*RL)
      G1(2,1)=1./XLO
      G1(3,1)=-RN/(R4*C1)-C2*R5*RL/(C1*XLO*R5+C1*XLO*RL)
      G1(3,2)=G2(3,2)=G3(3,2)=RKD/(R3*C1)
      U(1,1)=EI
      U(2,1)=ER
      PO=ER**2/RL
    7 TON=SQRT(2.*XLO*TP*PO/(EI*(EI-ER)))
      TF1=SQRT(2.*XLO*TP*PO*(EI-ER)/(EI*ER**2))
      TF2=TP-TON-TF1
      DELTON=XMU*TON
      IF(TF2.GE.EPS) GO TO 6
      MODE=1
      TON=TP*ER/EI
      DELTON=XMU*TON
      IT=0
      SC1=XMATCH(TON,EI,ER)
   19 DMATCH=(XMATCH(TON+DELTON,EI,ER)-SC1)/DELTON
      TON=TON-SC1/DMATCH
      SC1=XMATCH(TON,EI,ER)
      IT=IT+1
      IF(ABS(SC1).LE.EPS) GO TO 20
      IF(IT.LT.NIT) GO TO 19
      TON=TP*ER/EI
   20 CONTINUE
      TF1=TP-TON
      CALL PHOMAT(PHIP,D2,TP,F1,G1)
      CALL PHOMAT(PHI2,D2,TF1,F1,G1)
      CALL PHOMAT(PHI1,D1,TON,F1,G1)
      DO 22 I=1,2
      DO 21 J=1,2
   21 TEMP1(I,J)=-PHIP(I,J)
   22 TEMP1(I,I)=1.+TEMP1(I,I)
      DET=TEMP1(1,1)*TEMP1(2,2)-TEMP1(2,1)*TEMP1(1,2)
      IF(ABS(DET).LT.1.E-8) GO TO 250
      TVEC1(1)=PHI2(1,1)*D1(1,1)+PHI2(1,2)*D1(2,1)
```

```
      TVEC1(2)=PHI2(2,1)*D1(1,1)+PHI2(2,2)*D1(2,1)
      X(1,1)=EI*(TEMP1(2,2)*TVEC1(1)-TEMP1(1,2)*TVEC1(2))/DET
      X(2,1)=EI*(TEMP1(1,1)*TVEC1(2)-TEMP1(2,1)*TVEC1(1))/DET
      X(3,1)=ET-PHI1(3,1)*X(1,1)-PHI1(3,2)*X(2,1)-D1(3,1)*EI
     X -D1(3,2)*ER
      Y(1,1)=PHI1(1,1)*X(1,1)+PHI1(1,2)*X(2,1)+D1(1,1)*EI
      Y(2,1)=PHI1(2,1)*X(1,1)+PHI1(2,2)*X(2,1)+D1(2,1)*EI
      Y(3,1)=ET
      SC1=PHI2(3,1)*Y(1,1)+PHI2(3,2)*Y(2,1)+ET+D2(3,2)*ER
      DO 32 I=1,3
   32 RIPX(I,1)=X(I,1)-Y(I,1)
C     IF(LRTL.EQ.2) GO TO 36
      WRITE(2,35) EI,MODE,TON,TF1,TP,X,Y,RIPX,SC1,IT
   35 FORMAT(/*EI=*,E12.4/*MODE=*,I3/*TON=*,E12.4,* TF1=*,
     X E12.4,*  TP=*,E12.4
     X/*X=*,3E12.4,/*Y=*,3E12.4,/*RIPX=*,3E12.4/*SC1=*,E12.4,
     X * IT=*,I3//)
   36 CONTINUE
      GO TO 56
    6 MODE=2
      CALL STATE(TON,TF1)
      PRINT 17,TON,TF1,TF2,X,Y,Z
   17 FORMAT(*APPROXIMATE STEADY STATE*/*TON=*,E15.6,
     X*  TF1=*,E15.6,*  TF2=*,E15.6/
     X*X=*,3E15.6/*Y=*,3E15.6/*Z=*,3E15.6//)
      IT=0
      CALL SMATCH(TON,TF1,TF2,SC1,XMU,XLO,PO)
    9 CALL SMATCH(TON+DELTON,TF1,TF2,SC2,XMU,XLO,PO)
      DSMATCH=(SC2-SC1)/DELTON
      TON=TON-SC1/DSMATCH
      CALL SMATCH(TON,TF1,TF2,SC1,XMU,XLO,PO)
      IT=IT+1
      IF(ABS(SC1).LE.EPS) GO TO 10
      IF(IT.LT.NIT) GO TO 9
      TF1=SQRT(2.0*XLO*TP*PO*(EI-ER)/(EI*ER**2))
      TON=SQRT(2.0*XLO*TP*PO/(EI*(EI-ER)))
      CALL SMATCH(TON,TF1,TF2,SC1,XMU,XLO,PO)
   10 CONTINUE
   13 DO 12 I=1,3
   12 RIPX(I,1)=X(I,1)-Y(I,1)
      IF(LRTL.EQ.2) GO TO 56
      WRITE(2,55) EI,MODE,TON,TF1,TF2,TP,X,Y,Z,RIPX,SC1,IT
   55 FORMAT(/*EI   =*,E15.6/*MODE=*,I3/*TON =*,E15.6,*  TF1=*,
     X E15.6,*  TF2=*,E15.6/*TP   =*,E15.6,
     X/*X    =*,3E15.6,/*Y    =*,3E15.6,/
     X*Z    =*,3E15.6,//*RIPX=*,3E15.6,/
     X*SC1=*,E15.6/*IT=*,I3//)
   56 CONTINUE
      CALL PSIMAT(PSI,TON,TF1,X,U,XMU)
      CALL RMCPY(PSY,PSI,3,3)
      ITBL(1)=3
      ITBL(3)=0
      CALL QRAL(PSY,R,3,H,V,INT,IVD,ITBL)
      IF (LRTL.EQ.2) GO TO 72
      WRITE(2,70) ((PSI(I,J),J=1,3),I=1,3)
   70 FORMAT(/*PSI=*,/3(3E15.6/)/)
   72 WRITE(2,74)((R(I,J),J=1,2),I=1,3)
      WRITE(2,71) ITBL(2)
   71 FORMAT(*NUMBER OF EIGENVALUES FOUNT=*,I3)
   74 FORMAT(*LAMBDA=    REAL        IMAGINARY *,/3(E15.6,E15.6/)/)
      IF(LFREQ.EQ.0) GO TO 150
      CALL GAMMAT(GAM,TON,TF1,X,U,XMU)
      WRITE(2,75)  (GAM(I,1),I=1,3)
   75 FORMAT(/*GAM=*/3(E15.6/))
      CALL FREQ(PSI,GAM,H,THETAO,THETAF,DELTHET,EI,ER)
      LFREQ=0
  150 CONTINUE
      IF(LFE.EQ.1) GO TO 160
      IF(LPEAK.EQ.0) GO TO 200
      EI=EISWIT
      U(1,1)=EI
      DO 152 I=1,3
  152 XFP(I,1)=X(I,1)
      LFE=1
      GO TO 7
  160 CALL OVSHOOT(PSI,XFP,NK)
  200 CONTINUE
      LPEAK=LFE=0
      IF(LRTL.EQ.2) GO TO 210
      IF(LRTL.EQ.0) GO TO 300
      LRTL=2
      WRITE(2,202) NRL,EI
  202 FORMAT(///*ROOT LOCUS ON PARAMETER NRL=*,I3,*. EI=*,F5.2/)
  210 CONTINUE
```

```
      PRAM(NRL)=PRAM(NRL)+DPRAM
      PRINT 212,PRAM(NRL)
      WRITE(2,212) PRAM(NRL)
  212 FORMAT(*PRAM=*,E15.6)
      IF(PRAM(NRL).LE.PRAMF) GO TO 5
      GO TO 300
  250 PRINT 251,IT,X
  251 FORMAT(*UNSCHADULED TERMINATION IT=*,I3,/*X=*,3E15.6/)
      GO TO 300
  255 PRINT 256,IT,Y
  256 FORMAT(*UNSCHADULED TERMINATION IT=*,I3/*Y=*,3E15.6/)
  300 CONTINUE
      END
C
C
      SUBROUTINE OVSHOOT(PSI,XFP,NK)
      DIMENSION PSI(3,3),XFP(3,1),DELXP(3,1),TVEC(3,1)
      COMMON/STATE/X(3,1),Y(3,1),Z(3,1),U(2,1)
      DO 10 I=1,3
   10 DELXP(I,1)=XFP(I,1)-X(I,1)
      DO 30 NN=1,NK
      WRITE(2,12) NN,DELXP
   12 FORMAT(I3,3E15.6)
      CALL RMMUL(TVEC,PSI,DELXP,3,3,1)
      DO 14 I=1,3
   14 DELXP(I,1)=TVEC(I,1)
   30 CONTINUE
      RETURN
      END
C
C
      FUNCTION ZETA(T,X,U)
      DIMENSION PHI1(3,3),D1(3,2),X(3,1),U(2,1)
      COMMON/PARAM/F1(3,3),F2(3,3),F3(3,3),G1(3,2),
     XG2(3,2),G3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      CALL PHDMAT(PHI1,D1,T,F1,G1)
      ZETA=-ET+PHI1(3,1)*X(1,1)+PHI1(3,2)*X(2,1)+PHI1(3,3)*X(3,1)
     X D1(3,1)*U(1,1)+D1(3,2)*U(2,1)
      RETURN
      END
C
C
      SUBROUTINE FREQ(PSI,DVEC,H,THETAO,THETAF,DELTHET,EI,ER)
      DIMENSION PSI(3,3),DVEC(3,1),H(3)
      DIMENSION A(3,3),AINV(3,3),B(3,3),U(3,3),V(3,3),TEMP1(3,3)
      DIMENSION TEMP2(3,3),TVEC1(3,1),TVEC2(3,1)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      DEGRAD=180./3.1415927
      RADDEG=1./DEGRAD
      THETA=THETAO-DELTHET
      DO 2 I=1,3
      DO 2 J=1,3
    2 B(I,J)=0.
      WRITE(4,1) EI
    1 FORMAT(//*EI=*,E12.6/,
     X * THETA    FREQ (HZ)    DBEL*,5X,*G*,11X,*REG*,10X,*IMG*,
     X 6X,*PHASE*)
    5 CONTINUE
      THETA=THETA+DELTHET
      THET=RADDEG*THETA
      FRE=THET/(6.2831853*TP)
      RX=COS(THET)
      RY=SIN(THET)
      DO 12 I=1,3
      DO 10 J=1,3
   10 A(I,J)=-PSI(I,J)
      A(I,I)=A(I,I)+RX
   12 B(I,I)=RY
      IF(ABS(RY).LT.1.E-10) GO TO 25
      RYIV=1./RY
      CALL RMMUL(TEMP1,A,A,3,3,3)
      CALL RMSCLR(TEMP2,RYIV,TEMP1,3,3)
      DO 14 I=1,3
   14 TEMP2(I,I)=TEMP2(I,I)+RY
      CALL RMINV(V,TEMP2,3)
      CALL RMMUL(U,A,V,3,3,3)
      DO 16 I=1,3
      DO 16 J=1,3
      U(I,J)=RYIV*U(I,J)
   16 V(I,J)=-V(I,J)
      GO TO 50
   25 CALL RMINV(AINV,A,3)
      DO 30 I=1,3
```

```
      DO 30 J=1,3
   30 TEMP1(I,J)=AINV(I,J)*RY**2
      CALL RMADD(TEMP2,A,TEMP1,3,3)
      CALL RMINV(U,TEMP2,3)
      CALL RMMUL(V,AINV,U,3,3,3)
      DO 34 I=1,3
      DO 34 J=1,3
   34 V(I,J)=-RY*V(I,J)
   50 CONTINUE
      CALL RMMUL(TVEC1,U,DVEC,3,3,1)
      CALL RMMUL(TVEC2,V,DVEC,3,3,1)
      GRE=GIM=0.
      DO 55 I=1,3
      GRE=GRE+H(I)*TVEC1(I,1)
   55 GIM=GIM+H(I)*TVEC2(I,1)
      G=SQRT(GRE**2+GIM**2)
      DBEL=20.*ALOG10(G*EI/ER)
      PHASE=DEGRAD*ATAN2(GIM,GRE)
      WRITE(6,60) THETA,FRE,DBEL,G,GRE,GIM,PHASE
   60 FORMAT(F6.2,E12.4,F9.2,3E12.4,F9.2)
      IF(THETA.LT.THETAF-0.5*DELTHET) GO TO 5
  100 CONTINUE
      RETURN
      END
C
C
      SUBROUTINE PHOMAT(PHI,D,T,F,G)
      DIMENSION PHI(3,3),D(3,2),FSQ(3,3),F(3,3),G(3,2),B(3,3)
      DIMENSION TAR1(3,3), TAR2(3,3), TVEC1(3)
      ALPHA=-0.5*(F(1,1)+F(2,2))
      DET=0.25*(F(1,1)+F(2,2))**2-F(1,1)*F(2,2)+F(1,2)*F(2,1)
      IF(DET.LT.0.) GO TO 20
      A=-ALPHA+SQRT(DET)
      B=-ALPHA-SQRT(DET)
      EXPA=EXP(A*T)-1.
      EXNA=EXP(-A*T)-1.
      EXPB=EXP(B*T)-1.
      EXNB=EXP(-B*T)-1.
      CC1=A*B*(A-B)
      GAM1=(A**2*EXPB-B**2*EXPA)/CC1
      GAM2=(B*EXPA-A*EXPB)/CC1
      CC2=A**2*(A-B)
      CC3=B**2*(A-B)
      XI1=-(A+B)*T/(A*B)-A*EXNB/CC3+B*EXNA/CC2
      XI2=T/(A*B)-EXNA/CC2+EXNB/CC3
      GO TO 30
   20 BETA=SQRT(-DET)
      CC3=1./(ALPHA**2+BETA**2)
      CC1=2.*ALPHA*CC3
      CC2=(ALPHA**2-BETA**2)/(2.*ALPHA*BETA)
      CC4=ALPHA/BETA
      SB=SIN(BETA*T)
      CB=COS(BETA*T)
      EMAL=EXP(-ALPHA*T)
      EPAL=EXP(ALPHA*T)
      GAM1=CC1*(1.-EMAL*(CC2*SB+CB))
      GAM2=CC3*(1.-EMAL*(CC4*SB+CB))
      GRAL1=CC3*(EPAL*(ALPHA*CB+BETA*SB)-ALPHA)
      GRAL2=CC3*(EPAL*(ALPHA*SB-BETA*CB)+BETA)
      XI1=CC1*(T-GRAL1+CC2*GRAL2)
      XI2=CC3*(T-GRAL1+CC4*GRAL2)
   30 CALL RMSCLR(TAR1,GAM1,F,3,3)
      CALL RMMUL(FSQ,F,F,3,3,3)
      CALL RMSCLR(TAR2,GAM2,FSQ,3,3)
      CALL RMADD(PHI,TAR1,TAR2,3,3)
      DO 10 I=1,3
   10 PHI(I,I)=PHI(I,I)+1.
C     MATRIX PHI(T) HAS BEEN COMPUTED
      CALL RMSCLR(TAR1,XI1,F,3,3)
      CALL RMSCLR(TAR2,XI2,FSQ,3,3)
      CALL RMADD(TAR1,TAR1,TAR2,3,3)
      DO 12 I=1,3
   12 TAR1(I,I)=TAR1(I,I)+T
      CALL RMMUL(B,PHI,TAR1,3,3,3)
C     MATRIX B(T) HAS BEEN COMPUTED
      CALL RMMUL(D,B,G,3,3,2)
C MATRIX D(T) HAS BEEN COMPUTED
      RETURN
      END
C
C
      SUBROUTINE STATE(TON,TF1)
      DIMENSION PHI1(3,3),PHI2(3,3),PHI3(3,3),D1(3,2),D2(3,2),
     XD3(3,2)
```

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```
      COMMON/PARAM/ F1(3,3),F2(3,3),F3(3,3),G1(3,2),G2(3,2),
     XG3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      COMMON/STATE/X(3,1),Y(3,1),Z(3,1),U(2,1)
      TF2=TP-TON-TF1
      CALL PHOMAT(PHI1,D1,TON,F1,G1)
      CALL PHOMAT(PHI2,D2,TF1,F2,G2)
      CALL PHOMAT(PHI3,D3,TF2,F3,G3)
      A=1.-PHI3(1,1)*(PHI2(1,1)*PHI1(1,1)+PHI2(1,2)*PHI1(2,1))
     X -PHI3(1,2)*(PHI2(2,1)*PHI1(1,1)+PHI2(2,2)*PHI1(2,1))
      B=PHI3(1,1)*(PHI2(1,1)*D1(1,1)+PHI2(1,2)*D1(2,1)+D2(1,1))
      C=PHI3(1,2)*(PHI2(2,1)*D1(1,1)+PHI2(2,2)*D1(2,1)+D2(2,1))
      IF(ABS(A).LT.EPS) GO TO 250
      X(1,1)=(B+C+D3(1,1))*U(1,1)/A
      X(2,1)=0.
      X(3,1)=ET-PHI1(3,1)*X(1,1)-PHI1(3,2)*X(2,1)-
     X D1(3,1)*U(1,1)-D1(3,2)*U(2,1)
      CALL STSTEP(Y,PHI1,X,D1,U)
      CALL STSTEP(Z,PHI2,Y,D2,U)
      GO TO 23
  250 PRINT 252,A
  252 FORMAT(/*UNSCHEDULED TERMINATION*/*A=*,E12.6)
   23 RETURN
      END
C
C
      SUBROUTINE STSTEP(W2,PHI,W1,D,U)
      DIMENSION PHI(3,3),W1(3,1),W2(3,1),D(3,2),U(2,1),
     XTEMPY1(3,1),TEMPY2(3,1)
      CALL RMMUL(TEMPY1,PHI,W1,3,3,1)
      CALL RMMUL(TEMPY2,D,U,3,2,1)
      CALL RMADD(W2,TEMPY1,TEMPY2,3,1)
      RETURN
      END
C
C
      SUBROUTINE PSIMAT(PSI,TON,TF1,X,U,XMU)
      DIMENSION X(3,1),FBARO(3,1),FBAR(3,1),PSI(3,3),
     XU(2,1),Y(3,1),PHI1(3,3),D1(3,3),
     XTEMPY1(3,1),TEMPY2(3,1),DELTX(3,1)
      COMMON/PARAM/F1(3,3),F2(3,3),F3(3,3),G1(3,2),
     XG2(3,2),G3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      VARTON=TON
      VARTF1=TF1
      DELTON=XMU*TON
      DELTF1=XMU*TF1
      DO 71 I=1,3
   71 DELTX(I,1)=XMU*ABS(X(I,1))
      CALL FFUNC(VARTON,VARTF1,X,U,FBARO)
C     PRINT 51,FBARO
   51 FORMAT(*FBARO=*,E15.6/2(6X,E15.6/))
      DO 68 J=1,3
      IF(J.NE.2) GO TO 54
      IF(MODE.EQ.2) GO TO 72
   54 X(J,1)=X(J,1)+DELTX(J,1)
      IT=0
      SC1=ZETA(VARTON,X,U)
   67 DZETA=(ZETA(VARTON+DELTON,X,U)-SC1)/DELTON
      IT=IT+1
      VARTON=VARTON-SC1/DZETA
      SC1=ZETA(VARTON,X,U)
      IF(ABS(SC1).LT.EPS) GO TO 64
      IF(IT.LT.NIT) GO TO 67
      PRINT 61,IT,SC1
   61 FORMAT(*MAX ITERATION ON TON. IT=*,I3,* SC1=*,E12.6/)
      GO TO 70
   64 IF(MODE.EQ.1) GO TO 65
      CALL PHOMAT(PHI1,D1,VARTON,F1,G1)
      CALL STSTEP(Y,PHI1,X,D1,U)
      IT=0
      B1=BMATCH(VARTF1,Y,U)
   63 DB=(BMATCH(VARTF1+DELTF1,Y,U)-B1)/DELTF1
      IT=IT+1
      VARTF1=VARTF1-B1/DB
      B1=BMATCH(VARTF1,Y,U)
      IF(ABS(B1).LT.EPS) GO TO 65
      IF(IT.LT.NIT) GO TO 63
      PRINT 66,IT,B1
   66 FORMAT(*MAX ITERATION ON TF1. IT=*,I3,* SC1=*,E12.6/)
      GO TO 70
   65 CALL FFUNC(VARTON,VARTF1,Y,U,FBAR)
C     PRINT 53,VARTON,VARTF1
   53 FORMAT(*VARTON=*,E15.6/*VARTF1=*,E15.6/)
```

```
      DO 69 I=1,3
   69 PSI(I,J)=(FBAR(I,1)-FBARO(I,1))/DELTX(J,1)
C     PRINT 52,FBAR
   52 FORMAT(*FBAR=*,E15.6/3(5X,E15.6/))
      X(J,1)=X(J,1)-DELTX(J,1)
      GO TO 68
   72 DO 74 I=1,3
   74 PSI(I,2)=0.
   68 CONTINUE
      IF(MODE.EQ.2) GO TO 70
      CALL PHOMAT(PHI1,D1,TP,F1,G1)
      CALL RMADD(PSI,PSI,PHI1,3,3)
   70 RETURN
      END
C
C
      FUNCTION BMATCH(TF1,Y,U)
      DIMENSION PHI2(3,3),D2(3,2),Y(3,1),U(2,1)
      COMMON/PARAM/ F1(3,3),F2(3,3),F3(3,3),G1(3,2),G2(3,2),
     XG3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      CALL PHOMAT(PHI2,D2,TF1,F2,G2)
      BMATCH=PHI2(2,1)*Y(1,1)+PHI2(2,2)*Y(2,1)
      RETURN
      END
C
C
      SUBROUTINE FFUNC(TON,TF1,X,U,F)
      DIMENSION TEMP1(3,3),TEMP2(3,3),PHI1(3,3),PHI2(3,3),
     XPHI3(3,3),D1(3,2),D2(3,2),D3(3,2),PHI(3,3),V(3,3),
     XFTEMP1(3,1),FTEMP2(3,1),F(3,1),X(3,1),U(2,1),TVEC1(3,1)
      COMMON/PARAM/F1(3,3),F2(3,3),F3(3,3),G1(3,2),G2(3,2),
     XG3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      IF(MODE.EQ.2) GO TO 1
      TF1=TP-TON
      CALL PHOMAT(PHI1,D1,TON,F1,G1)
      CALL PHOMAT(PHI2,D2,TF1,F1,G1)
      TVEC1(1,1)=D1(1,1)*U(1,1)
      TVEC1(2,1)=D1(2,1)*U(1,1)
      TVEC1(3,1)=D1(3,1)*U(1,1)+D1(3,2)*U(2,1)
      CALL RMMUL(F,PHI2,TVEC1,3,3,1)
      F(3,1)=F(3,1)+D2(3,2)*U(2,1)
      GO TO 2
    1 TF2=TP-TF1-TON
      CALL PHOMAT(PHI1,D1,TON,F1,G1)
      CALL PHOMAT(PHI2,D2,TF1,F2,G2)
      CALL PHOMAT(PHI3,D3,TF2,F3,G3)
      CALL RMMUL(TEMP1,PHI3,PHI2,3,3,3)
      CALL RMMUL(PHI,TEMP1,PHI1,3,3,3)
      CALL RMMUL(FTEMP1,PHI,X,3,3,1)
      CALL RMMUL(TEMP2,TEMP1,D1,3,3,2)
      CALL RMMUL(TEMP1,PHI3,D2,3,3,2)
      CALL RMADD(TEMP1,TEMP2,TEMP1,3,2)
      CALL RMADD(V,TEMP1,D3,3,2)
      CALL RMMUL(FTEMP2,V,U,3,2,1)
      CALL RMADD(F,FTEMP1,FTEMP2,3,1)
      F(2,1)=0.
    2 RETURN
      END
C
C
      SUBROUTINE GAMMAT(GAM,TON,TF1,X,U,XMU)
      DIMENSION X(3,1),U(2,1),FBARO(3,1),FBAR(3,1),GAM(3,1),
     XPHI1(3,3),D1(3,2),TEMPY1(3,1),TEMPY2(3,1),Y(3,1)
      COMMON/PARAM/F1(3,3),F2(3,3),F3(3,3),G1(3,2),
     XG2(3,2),G3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      VARTON=TON
      VARTF1=TF1
      DELTON=XMU*TON
      DELTF1=XMU*TF1
      DELU=XMU*ABS(U(1,1))
      CALL FFUNC(VARTON,VARTF1,X,U,FBARO)
      U(1,1)=U(1,1)+DELU
      IT=0
      SC1=ZETA(VARTON,X,U)
   67 DZETA=(ZETA(VARTON+DELTON,X,U)-SC1)/DELTON
      IT=IT+1
      VARTON=VARTON-SC1/DZETA
      SC1=ZETA(VARTON,X,U)
      IF(ABS(SC1).LT.EPS) GO TO 64
      IF(IT.LT.NIT) GO TO 67
      PRINT 61,IT,SC1
```

```
   61 FORMAT(*MAX ITERATION ON TON. IT=*,I3,* SC1=*,E12.6/)
      GO TO 70
   64 CALL PHOMAT(PHI1,D1,VARTON,F1,G1)
      CALL STSTEP(Y,PHI1,X,D1,U)
      IT=0
      IF(MODE.EQ.1) GO TO 65
      B1=BMATCH(VARTF1,Y,U)
   63 DB=(BMATCH(VARTF1+DELTF1,Y,U)-B1)/DELTF1
      IT=IT+1
      VARTF1=VARTF1-B1/DB
      B1=BMATCH(VARTF1,Y,U)
      IF(ABS(B1).LT.EPS) GO TO 65
      IF(IT.LT.NIT) GO TO 63
      PRINT 66,IT,B1
   66 FORMAT(*MAX ITERATION ON TF1. IT=*,I3,* SC1=*,E12.6/)
      GO TO 70
   65 CALL FFUNC(VARTON,VARTF1,X,U,FBAR)
      DO 69 I=1,3
   69 GAM(I,1)=(FBAR(I,1)-FBARO(I,1))/DELU
      U(1,1)=U(1,1)-DELU
   70 RETURN
      END
C
C
      SUBROUTINE SMATCH(TON,TF1,TF2,SMAT,XMU,XLO,PO)
      DIMENSION TEMPY1(3,1),TEMPY2(3,1),PHI1(3,3),D1(3,2),
     XPHI2(3,3),D2(3,2),PHI3(3,3),D3(3,2)
      COMMON/PARAM/ F1(3,3),F2(3,3),F3(3,3),G1(3,2),G2(3,2),
     XG3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      COMMON/STATE/X(3,1),Y(3,1),Z(3,1),U(2,1)
      TF2=TP-TON-TF1
      DELTF1=XMU*TF1
      CALL STATE(TON,TF1)
C     Y(3,1)=ET
      IT=0
      B1=BMATCH(TF1,Y,U)
      IF(ABS(B1).LT.EPS) GO TO 32
   31 B2=BMATCH(TF1+DELTF1,Y,U)
      DBMATCH=(B2-B1)/DELTF1
      TF1=TF1-B1/DBMATCH
      B1=BMATCH(TF1,Y,U)
      IF(ABS(B1).LT.EPS) GO TO 32
      IT=IT+1
      IF(IT.LT.NIT) GO TO 31
      PRINT 33,IT,TF1,B1
   33 FORMAT(*MAX. ITERATION ON IT=*,I3,*TF1=*,E15.6,* B1=*,E15.
      TF1=SQRT(2.*XLO*TP*PO*(U(1,1)-U(2,1))/(U(1,1)*U(2,1)**2))
   32 CALL PHOMAT(PHI2,D2,TF1,F2,G2)
      CALL STSTEP(Z,PHI2,Y,D2,U)
C     Z(2,1)=0.
      TF2=TP-TON-TF1
      CALL PHOMAT(PHI3,D3,TF2,F3,G3)
      SMAT=X(3,1)-PHI3(3,1)*Z(1,1)-PHI3(3,2)*Z(2,1)-
     XPHI3(3,3)*Z(3,1)-D3(3,2)*U(2,1)-D3(3,1)*U(1,1)
      RETURN
      END
C
C
      FUNCTION XMATCH(TON,EI,ER)
      DIMENSION PHIP(3,3),PHIF(3,3),PHIN(3,3),DF(3,2),DN(3,2),
     X TEMP1(2,2),X(3),Y(3),TVEC1(3)
      COMMON/PARAM/F1(3,3),F2(3,3),F3(3,3),G1(3,2),G2(3,2),
     X G3(3,2)
      COMMON/EXTPAR/NIT,EPS,TP,ET,MODE
      TF1=TP-TON
      CALL PHOMAT(PHIP,DF,TP,F1,G1)
      CALL PHOMAT(PHIF,DF,TF1,F1,G1)
      CALL PHOMAT(PHIN,DN,TON,F1,G1)
      DO 12 I=1,2
      DO 11 J=1,2
   11 TEMP1(I,J)=-PHIP(I,J)
   12 TEMP1(I,I)=1.+TEMP1(I,I)
      DET=TEMP1(1,1)*TEMP1(2,2)-TEMP1(2,1)*TEMP1(1,2)
      IF(ABS(DET).LT.1.E-8) GO TO 100
      TVEC1(1)=PHIF(1,1)*DN(1,1)+PHIF(1,2)*DN(2,1)
      TVEC1(2)=PHIF(2,1)*DN(1,1)+PHIF(2,2)*DN(2,1)
      X(1)=EI*(TEMP1(2,2)*TVEC1(1)-TEMP1(1,2)*TVEC1(2))/DET
      X(2)=EI*(TEMP1(1,1)*TVEC1(2)-TEMP1(2,1)*TVEC1(1))/DET
      X(3)=ET-PHIN(3,1)*X(1)-PHIN(3,2)*X(2)-DN(3,1)*EI-DN(3,2)*ER
      Y(1)=PHIN(1,1)*X(1)+PHIN(1,2)*X(2)+DN(1,1)*EI
      Y(2)=PHIN(2,1)*X(1)+PHIN(2,2)*X(2)+DN(2,1)*EI
      Y(3)=ET
      SC1=PHIF(3,1)*Y(1)+PHIF(3,2)*Y(2)+ET+DF(3,2)*ER
```

APPENDIX F

MODELING OF SWITCHING REGULATOR POWER STAGES WITH & WITHOUT ZERO-INDUCTOR-CURRENT DWELL TIME

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ABSTRACT

State space techniques are employed to derive accurate models for buck, boost, and buck/boost converter power stages operating with and without zero-inductor-current dwell time. A generalized procedure is developed which treats the continuous-inductor-current mode without the dwell time as a special case of the discontinuous-current mode, when the dwell time vanishes. An abrupt change of system behavior including a reduction of the system order when the dwell time appears is shown both analytically and experimentally.

1. INTRODUCTION

Modeling and analysis of the three basic dc-dc converter power stages, as shown in Fig. 1, has been achieved through frequency-domain averaging approaches.[1-5] However, they have been limited to analyzing a steady-state continuous operation where the MMF of the output filter inductor never vanishes, as illustrated in Fig. 2(A). Such an operation can be represented by a cyclic change of two power-stage topologies within each switching cycle; one for the on-time interval while the other for the off-time interval of the power switch. However, either by design intent or through light load operation, a steady-state cycle invariably contains an interval during which the inductor MMF vanishes, as shown in Fig. 2(B). This interval begins when the descending MMF reaches zero during the off time of the power switch, and ends when the power switch is turned on to initiate the next on-time interval. During this zero-inductor-current dwell time, the topology of the power stage consists only of the filter capacitor and the load, which is different from both the on-time interval of ascending MMF and the off-time interval of descending MMF. The addition of such a dwell time thus renders the afore-referenced analytical approaches powerless.

It is commonly known that there are significant differences in switching-regulator performances with continuous- and discontinuous-inductor current operations. Certain abrupt changes often can be observed in the breadboard performance when the inductor current leaves the continuous mode and enters into the discontinuous mode. For example, step transient response may change from oscillatory to well damped, and the audio susceptibility is generally improved. More significantly, the stability nature of the system can be changed from an unstable system to a stable one. Such important phenomena, which may very well affect converter

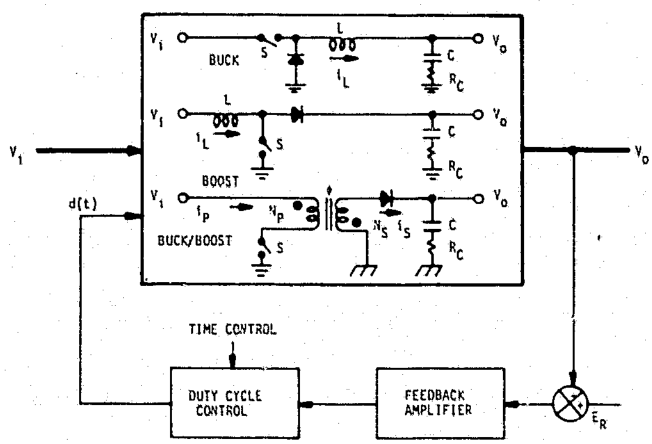

Fig.1 Dc-dc energy storage converter with three basic power stage configurations.

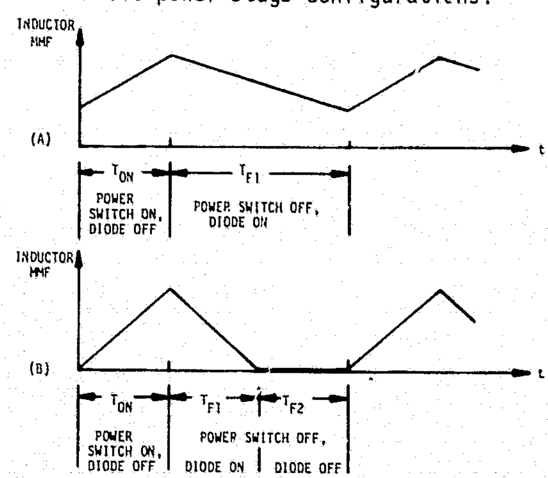

Fig.2(A) and (B) Continuous and discontinuous inductor current MMF.

design philosophies under certain conditions, have never been investigated for lack of a discontinuous-current power stage model.

Recently, Projoux et al. [6,7] has presented an approach capable of describing accurately certain nonlinear system under periodical structural changes by a linearized discrete time domain model, and has applied such a technique to a boost converter operating with zero-inductor current dwell time. The present paper extends the analysis to all three types of converters: buck, boost, and buck/boost, operating with and without such a dwell time. The duty-cycle-to-output-voltage

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TABLE I Matrices F's and G's for state variable representations of the three converters.

	$F1 = \begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix}$	F2	F3	G1	G2	G3
BUCK	$\begin{bmatrix} \frac{-R_CR_L}{L(R_C+R_L)} & \frac{-R_L}{L(R_C+R_L)} \\ \frac{R_L}{C(R_C+R_L)} & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} \frac{-R_CR_L}{L(R_C+R_L)} & \frac{-R_L}{L(R_C+R_L)} \\ \frac{R_L}{C(R_C+R_L)} & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$
BOOST	$\begin{bmatrix} \frac{-R_CR_L}{L(R_C+R_L)} & \frac{-R_L}{L(R_C+R_L)} \\ \frac{R_L}{C(R_C+R_L)} & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$
BUCK BOOST	$\begin{bmatrix} \frac{-\ell}{\mu A N_s^2} \frac{R_CR_L}{(R_C+R_L)} & \frac{-R_L}{N_s(R_C+R_L)} \\ \frac{\ell}{\mu A N_s} \frac{R_L}{C(R_C+R_L)} & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$\begin{bmatrix} \frac{1}{N_p} \\ 0 \end{bmatrix}$

Where μ = magnetic permeability; ℓ = mean length path ; A = cross section area

discrete time domain models are derived in closed forms, which describe converters about their equilibrium state exactly. These discrete models are then transformed into frequency domain transfer functions representing the small signal low frequency characteristics of the converter up to one half of the switching frequency. A generalized procedure is developed in this paper which not only avoids laborious derivations for each converter but also treats the continuous current mode without the dwell time as a special case of the discontinuous current mode when the dwell time vanishes.

The mathematical models derived from this unified approach thus serves as an ideal basis for comparitive studies between the two operating modes with and without the dwell time. The aforementioned pronounced changes of performance characteristics observed when the inductor current leaves the continuous mode and enters into the discontinuous mode are manifested by an abrupt reduction of system order both analytically and experimentally.

2. DEVELOPMENT OF POWER STAGE MODELS- A GENERAL PROCEDURE

Consider the small signal behavior of the converter about its equilibrium state is linear. When the converter is subjected to a small disturbance, the duty-cycle signal d(t) is modified as d(t)+Δd(t), shown as Fig. 3. Such a perturbed duty-cycle signal can be idealized as an impulse train when the perturbation is vanishing small. A linearized discrete impulse response which characterizes the small signal behavior of the power stage about its equilibrium state can be obtained if the perturbation of the output voltage, subjected to a small duty-cycle disturbance at the k th switching cycle can be computed after n cycles of propagation. This concept can be elaborated by Fig. 4 and the following equation.

$$\frac{\Delta V_0(t_{k+n})}{\Delta t_k} \triangleq g(nT_p) \qquad (1)$$

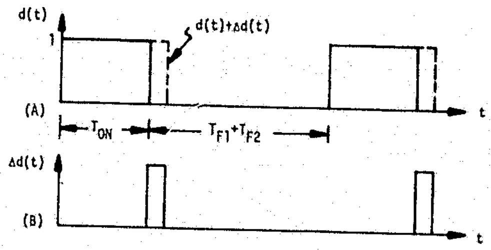

Fig.3(A) The duty-cycle signal at steady state d(t) and after small perturbation d(t)+ d(t).
(B) The perturbed duty cycle d(t).

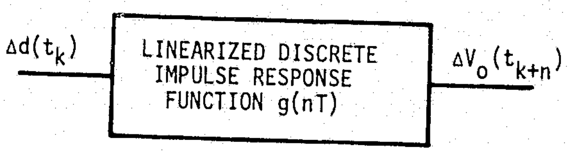

Fig.4 Linearized discrete power stage models.

where Δt_k is a small duty cycle disturbance at the kth switching cycle and $\Delta V_0(t_{k+n})$ is the resulting output voltage variation at the (k+n)th cycle. The sampling rate is equal to the switching frequency $1/T_p$. Through mathematical manipulation, the discrete impulse response $g(nT_p)$ can be expressed in the closed form as a function of nT_p, the power stage parameters, and the steady-state operating conditions. For convenience, the converter operations with and without zero inductor-current dwell time are referred to in the text as MODE 2 OPERATION and MODE 1 OPERATION, respectively.

2.1 State Space Representations

The switching regulator power stage, during one cycle of operation, can be represented by three piecewise linear vector diffential equations:

$$\dot{\underline{X}} = F1\ \underline{X} + G1\ \underline{U} \quad \text{during } T_{F1} \qquad (2)$$
$$\dot{\underline{X}} = F2\ \underline{X} + G2\ \underline{U} \quad \text{during } T_{F2} \qquad (3)$$
$$\dot{\underline{X}} = F3\ \underline{X} + G3\ \underline{U} \quad \text{during } T_{ON} \qquad (4)$$

where $\underline{U} = V_I$.

The time intervals T_{F1}, T_{F2}, and T_{ON} are defined in Fig. 2. The inductor current and the capacitor voltage, $\underline{X} = [i_L, v_c]^T$ are chosen as two state variables for buck and boost converters. For the buck/boost converter, however, the current through either the primary winding or the secondary winding of the inductor is not continuous. The magnetic flux ϕ instead of inductor current is chosen as one state variable. The F's and G's matrices for each converter are presented in Table I. It should be noted that, for Mode 1 operation, the time interval T_{F2} does not exist. Therefore, the vector differential equation (3) can be neglected.

2.2 Linearized Discrete Impulse Response

Consider the following duty cycle signal

$$d(t) = \begin{cases} 1 & \text{during } T_{ON} \\ 0 & \text{otherwise} \end{cases}$$

whose leading edge of T_{ON} is always initiated by a clock signal. When the converter is subjected to a small duty-cycle disturbance, the propagation of the perturbed state can be illustrated in Fig. 5. The steady state with a superscript "°" is shown as the solid curve, while the perturbed state with a superscript "*" is represented by the dotted curve. For a small duty-cycle perturbation at kth cycle from t_k° to t_k^*, the perturbed state after one cycle of propagation is expressed as $\underline{X}^*(t_{k+1}^\circ)$. The trajectories for the perturbed state during each piecewise linear region can be represented by the following state transition equations (5-7) which are the solutions for the vector differential equations (2-4).

$$\underline{X}^*(t_{k1}^\circ)=\phi 1(t_{k1}^\circ-t_k^*)\underline{X}^*(t_k^*)+\phi 1(t_{k1}^\circ)\int_{t_k^*}^{t_{k1}^\circ}\phi 1(-s)ds G1\underline{U} \quad (5)$$

$$\underline{X}^*(t_{k2}^\circ)=\phi 2(t_{k2}^\circ-t_{k1}^*)\underline{X}^*(t_{k1}^*)+\phi 2(t_{k2}^\circ)\int_{t_{k1}^*}^{t_{k2}^\circ}\phi 2(-s)ds G2\underline{U} \quad (6)$$

$$\underline{X}^*(t_{k+1}^\circ)=\phi 3(t_{k+1}^\circ-t_{k2}^*)\underline{X}^*(t_{k2}^*) +\phi 3(t_{k+1}^\circ)\int_{t_{k2}^*}^{t_{k+1}^\circ}\phi 3(-s)ds G3\underline{U} \quad (7)$$

where ϕi's are the state transition matrices defined as

$$\phi i(T) \triangleq e^{FiT} \qquad i = 1,2,3.$$

Since the clock signal initiates the turn-on time, the time instant t_{k2}^* is equal to t_{k2}° in equation(7).

The corresponding discrete impulse response for each switching power stage represented by (1) can be obtained by performing the following vector differentiation

$$g(nT_p) = \frac{C d\underline{X}^*(t_{k+n}^\circ)}{dt_k^*} \quad (8)$$

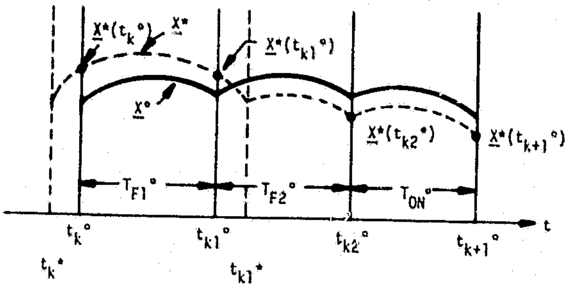

Fig.5 State trajectories for steady state (solid curve) and perturbed state (dotted curve)

Since the output voltage of the converter can be expressed as $V_o=C\underline{X}$, where C is a constant row matrix. Applying Chain Rule, one can express (8) by the following recurrence relation

$$\frac{d\underline{X}^*(t_{k+n}^\circ)}{dt_k^*} = \frac{d\underline{X}^*(t_{k+n}^\circ)}{d\underline{X}^*(t_{k+n-1}^\circ)}\cdots\frac{d\underline{X}^*(t_{k+1}^\circ)}{d\underline{X}^*(t_k^\circ)}\cdot\frac{d\underline{X}^*(t_k^\circ)}{dt_k^*}$$

$$= \left[\frac{d\underline{X}^*(t_{k+1}^\circ)}{d\underline{X}^*(t_k^\circ)}\right]^n \frac{d\underline{X}^*(t_k^\circ)}{dt_k^*} \quad (9)$$

where

$$\frac{d\underline{X}^*(t_{k+1}^\circ)}{d\underline{X}^*(t_k^\circ)} = \frac{d\underline{X}^*(t_{k+1}^\circ)}{d\underline{X}^*(t_{k2}^\circ)}\,\frac{d\underline{X}^*(t_{k2}^\circ)}{d\underline{X}^*(t_{k1}^\circ)}\,\frac{d\underline{X}^*(t_{k1}^\circ)}{d\underline{X}^*(t_k^\circ)} \quad (10)$$

- - - for Mode 2 Operation

$$= \frac{d\underline{X}^*(t_{k+1}^\circ)}{d\underline{X}^*(t_{k1}^\circ)}\,\frac{d\underline{X}^*(t_{k1}^\circ)}{d\underline{X}^*(t_k^\circ)} \quad (11)$$

- - - for Mode 1 Operation

It is proved in the APPENDIX A for all three converters that

$$\frac{d\underline{X}^*(t_{k+1}^\circ)}{d\underline{X}^*(t_k^\circ)} \triangleq \phi(T_p) = \phi 3(T_{ON}^\circ)\phi 2(T_{F2}^\circ)\begin{bmatrix}0 & 0\\0 & 1\end{bmatrix}\phi 1(T_{F1}^\circ)$$

- - - Mode 2 (12)

$$= \phi 3(T_{ON}^\circ)\phi 1(T_{F1}^\circ) \text{ - - - Mode 1} \quad (13)$$

and $$\frac{d\underline{X}^*(t_k^\circ)}{dt_k^*} \triangleq B = (F3-F1)\underline{X}^\circ(t_k^\circ)+(G3-G1)\underline{U} \quad (14)$$

Where $\underline{X}^\circ(t_k^\circ)$ is the state at the instant of sampling and is defined as $[I_M\ V_C]^T$ for buck and boost converters and $[\phi_M\ V_C]^T$ for buck/boost converter. It should be noted that, for boost and buck/boost converters, the output voltage V_o has a jump at the instant of sampling, since the current through the ESR R_C of the output filter capacitor is discontinuous at the sampling instant. Therefore, the sampling instants need to be carefully defined. In the present analysis, the samples are selected after the jump, $V_o(t_k^\circ) = V_o(t_k^\circ+)$, such that the effect of ESR to the jump is included in the model.

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TABLE II State transition matrices corresponding to the three time intervals: T_{ON}, T_{F1} and T_{F2}:

	$\Phi 1(T_{F1})$	$\Phi 2(T_{F2})$	$\Phi 3(T_{ON})$
Buck	$e^{-\alpha T_{F1}}\begin{bmatrix}\frac{\alpha+f_{11}}{\omega}\sin\omega T_{F1}+\cos\omega T_{F1} & \frac{f_{12}}{\omega}\sin\omega T_{F1}\\ \frac{f_{21}}{\omega}\sin\omega T_{F1} & \frac{\alpha+f_{22}}{\omega}\sin\omega T_{F1}+\cos\omega T_{F1}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\ 0 & e^{f_{22}T_{F2}}\end{bmatrix}$	$e^{-\alpha T_{ON}}\begin{bmatrix}\frac{\alpha+f_{11}}{\omega}\sin\omega T_{ON}+\cos\omega T_{ON} & \frac{f_{12}}{\omega}\sin\omega T_{ON}\\ \frac{f_{21}}{\omega}\sin T_{ON} & \frac{\alpha+f_{22}}{\omega}\sin\omega T_{ON}+\cos\omega T_{ON}\end{bmatrix}$
Boost	Same as $\Phi 1(T_{F1})$ of Buck Converter	Same as $\Phi 2(T_{F2})$ of Buck Converter	$\begin{bmatrix}1 & 0\\ 0 & e^{f_{22}T_{ON}}\end{bmatrix}$
Buck/Boost	Same as $\Phi 1(T_{F1})$ of Buck Converter	Same as $\Phi 2(T_{F2})$ of Buck Converter	Same as $\Phi 3(T_{ON})$ of Boost Converter
Where $\alpha \triangleq -(f_{11}+f_{22})/2$, $\omega^2 \triangleq f_{11}f_{22}-f_{12}f_{21}-(f_{11}+f_{22})^2/4$			

TABLE III Linearized state transition matrices.

	MODE 2		MODE 1	
	$\Phi(T_p) \triangleq e^{-aT_p}\begin{bmatrix}\phi_{11} & \phi_{12}\\ \phi_{21} & \phi_{22}\end{bmatrix}$	$\Phi^n(T_p)$	$\Phi(T_p) \triangleq e^{-aT_p}\begin{bmatrix}\phi_{11} & \phi_{12}\\ \phi_{21} & \phi_{22}\end{bmatrix}$	$\Phi^n(T_p)$
BUCK	$a = -f_{22}+(f_{22}+\alpha)(T_{ON}+T_{F1})/T_p$ $\phi_{11} = \frac{f_{12}f_{21}}{\omega^2}\sin\omega T_{ON}\sin\omega T_{F1}$ $\phi_{12} = \frac{f_{12}}{\omega}\sin\omega T_{ON}(\frac{\alpha+f_{22}}{\omega}\sin\omega T_{F1}+\cos\omega T_{F1})$ $\phi_{21} = (\frac{\alpha+f_{22}}{\omega}\sin\omega T_{ON}+\cos\omega T_{ON})\frac{f_{21}}{\omega}\sin\omega T_{F1}$ $\phi_{22} = (\frac{\alpha+f_{22}}{\omega}\sin\omega T_{ON}+\cos\omega T_{ON})(\frac{\alpha+f_{22}}{\omega}\sin\omega T_{F1}+\cos\omega T_{F1})$	$e^{-anT_p}(\phi_{11}+\phi_{22})^{n-1}\begin{bmatrix}\phi_{11} & \phi_{12}\\ \phi_{21} & \phi_{22}\end{bmatrix}$	$a = \alpha$ $\phi_{11} = \frac{\alpha+f_{11}}{\omega}\sin\omega T_p+\cos\omega T_p$ $\phi_{12} = \frac{f_{12}}{\omega}\sin\omega T_p$ $\phi_{21} = \frac{f_{21}}{\omega}\sin\omega T_p$ $\phi_{22} = \frac{\alpha+f_{22}}{\omega}\sin\omega T_p+\cos\omega T_p$	$\Phi^n(T_p) = \Phi(nT_p)$
BOOST	$a = -f_{22}+(f_{22}+\alpha)T_{F1}/T_p$ $\phi_{11} = 0$ $\phi_{12} = 0$ $\phi_{21} = \frac{f_{21}}{\omega}\sin\omega T_{F1}$ $\phi_{22} = \frac{\alpha+f_{22}}{\omega}\sin\omega T_{F1}+\cos\omega T_{F1}$	$e^{-anT_p}\begin{bmatrix}0 & 0\\ \phi_{21}\phi_{22}^{n-1} & \phi_{22}^n\end{bmatrix}$	$a = \alpha' T_{F1}/T_p$ $\phi_{11} = \frac{\alpha'+f_{11}}{\omega'}\sin\omega' T_{F1}+\cos\omega' T_{F1}$ $\phi_{12} = \frac{f_{12}}{\omega'}\sin\omega' T_{F1}$ $\phi_{21} = \frac{f_{21}}{\omega'}\sin\omega' T_{F1}$ $\phi_{22} = \frac{\alpha'+f_{22}/D'}{\omega'}\sin\omega' T_{F1}+\cos\omega' T_{F1}$	$\Phi^n(T_p) = \Phi(nT_p)$
BUCK BOOST	Same as Boost Converter	Same as Boost Converter	Same as Boost Converter	Same as Boost Converter
Where $D' \triangleq T_{F1}/T_p$, $\alpha' = (-f_{11}-f_{22}/D')/2$, $\omega'^2 \triangleq f_{11}f_{22}/D'-f_{12}f_{21}-(f_{11}+f_{22}/D')^2/4$				

Substituting (12-14) into (9), one can obtain

$$\frac{dX^*(t^\circ_{k+n})}{dt^*_k} = \phi^n(T_p)\,B \qquad (15)$$

The state transition matrices, $\phi 1(T^\circ_{F1})$, $\phi 2(T^\circ_{F2})$, and $\phi 3(T_{ON})$ are presented in Table II. The derivations for these state transition matrices are striaght forward and are neglected in the text. The explicit representations for $\phi(T_p)$ and $\phi^n(T_p)$ associated with each converter are given in Table III. The derivations for $\phi^n(T_p)$ are presented in APPENDIX B.

The linearized discrete impulse response is obtained by substituting (15) into (8)

$$g(nT_p) = C\phi^n(T_p)\,B \qquad (16)$$

Table IV shows the discrete impulse response for each converter at each operation mode. It should be noted that the derivations for the discrete impulse response is based on a constant frequency duty cycle control. However, the result is equally applicable to other types of control, such as constant T_{ON} and constant T_{OFF}. This is because the switching frequency in the steady state operation can be considered constant as long as the disturbance is small.

The steady state time intervals T°_{ON}, T°_{F1}, T°_{F2} for constant ON, constant OFF and constant frequency duty-cycle control are derived in Ref. 9.

TABLE IV Linearized discrete impulse response

	$B = \begin{bmatrix} B_{11} \\ B_{21} \end{bmatrix} = (F_3-F_1)\underline{X}^*(t_k^*)+(G_3-G_1)\underline{U}$	$C = [C_{11}\ C_{12}]$	$g(nT_p) = C\Phi^n(T_p)B$ Mode 2	Mode 1
BUCK	$\begin{bmatrix} \frac{V_I}{L} & 0 \end{bmatrix}^T$	$\begin{bmatrix} \frac{R_CR_L}{R_C+R_L} & \frac{R_L}{R_C+R_L} \end{bmatrix}$	$\frac{C_{11}\phi_{11}+C_{12}\phi_{21}}{\phi_{11}+\phi_{22}} B_{11} e^{[-a+\frac{1}{T_p}\ln(\phi_{11}+\phi_{22})]nT_p}$	$C\Phi(nT_p)B$
BOOST	$\begin{bmatrix} \frac{V_o}{L} & -f_{21}I_M \end{bmatrix}^T$	$\begin{bmatrix} \frac{R_CR_L}{R_C+R_L} & \frac{R_L}{R_C+R_L} \end{bmatrix}$	$C_{12}(B_{11}\frac{\phi_{21}}{\phi_{22}}+B_{21})e^{[-a+\frac{1}{T_p}\ln\phi_{22}]nT_p}$	$C\Phi(nT_p)B$
BUCK/BOOST	$\begin{bmatrix} \frac{V_o}{N_S}+\frac{V_I}{N_P} & -f_{21}\phi_M \end{bmatrix}^T$	$\begin{bmatrix} \frac{\ell}{\mu A N_S} & \frac{R_CR_L}{(R_C+R_L)} & \frac{R_L}{R_C+R_L} \end{bmatrix}$	$C_{12}(B_{11}\frac{\phi_{21}}{\phi_{22}}+B_{21})e^{[-a+\frac{1}{T_p}\ln\phi_{22}]nT_p}$	$C\Phi(nT_p)B$

TABLE V Continuous impulse response- time domain and frequency domain.

	MODE 2		MODE 1	
	TIME DOMAIN	FREQUENCY DOMAIN	TIME DOMAIN	FREQUENCY DOMAIN
	Impulse Response $g(t) = Ge^{-a't}$	$G(S) = \mathcal{L}\, g(t) = \frac{G_p}{1+\frac{S}{\omega_p}}$	$g(t) = e^{-at}(K_1\sin\omega t+K_2\cos\omega t)$	$G_{(S)} = G_p \frac{1+\frac{S}{\omega a}}{1+\frac{S}{Q\omega_o}+\frac{S^2}{\omega_o^2}}$
BUCK	$G = \frac{\gamma}{L} V_I \frac{-R_C\sin\omega T_{ON}\sin\omega T_{F1}+\sqrt{L/C}\cos(\omega T_{ON}-\theta)\sin\omega T_{F1}}{-\sin\omega T_{ON}\sin\omega T_{F1}+\cos(\omega T_{ON}-\theta)\cos(\omega T_{F1}-\theta)}$ $a' = \frac{\gamma}{R_LC}[1+\frac{1}{2}(-1+\frac{C}{L}R_CR_L)\frac{T_{ON}+T_{F1}}{T_p}] - \frac{1}{T_p}\ln\{\frac{\gamma^2}{\omega^2}\frac{1}{LC}$ $[-\sin\omega T_{ON}\sin\omega T_{F1}+\cos(\omega T_{ON}-\theta)\cos(\omega T_{F1}-\theta)]\}$	$G_p = G/a'$ $\omega_p = a'$	$K_1 = \frac{1}{\omega}\frac{\gamma^2}{LC}[1+\frac{R_C}{2R_L}-\frac{R_C^2C}{2L}]V_I$ $K_2 = \frac{R_C\gamma}{L}V_I$	$G_p = V_I$ $\omega_a = \frac{1}{R_CC}$ $\omega_o = \sqrt{\frac{\gamma}{LC}}$ $Q = \frac{1}{\omega_o}\frac{1}{R_CC+L/R_L}$
BOOST	$G = \gamma V_I[(1+\frac{T_{ON}}{T_{F1}})\frac{1}{\sqrt{LC}}\frac{\sin\omega T_{F1}}{\cos(\omega T_{F1}-\theta)} - \frac{\gamma}{LC}T_{ON}]$ $a' = \frac{\gamma}{R_LC}[1+\frac{1}{2}(-1+\frac{C}{L}R_CR_L)\frac{T_{F1}}{T_p}] - \frac{1}{T_p}\ln[\frac{\gamma}{\omega\sqrt{LC}}\cos(\omega T_{F1}-\theta)]$	$G_p = G/a'$ $\omega_p = a'$	$\omega = \omega'D'$ $K_1 = \frac{1}{\omega'}\frac{\gamma^2}{LC}[(1+\frac{R_C}{2R_LD'}-\frac{C}{2L}R_C^2)V_o$ $+\gamma(\frac{L}{2R_LD'C}+\frac{R_C}{2})I_M]$ $K_2 = \frac{R_C\gamma}{L}V_o - \frac{\gamma^2}{C}I_M$	$G_p = \frac{V_I}{D'^2}$ $\omega_a = \rho(-\frac{\gamma L}{R_LD'^2}-\frac{D}{2}\gamma T_p+\frac{R_CC}{D'})^{-1}$ $\omega_o = \sqrt{\frac{\gamma\rho}{LC}}D'$ $Q = \frac{\rho}{\omega_o}\frac{D'}{R_CC+L/R_LD'}$
BUCK/BOOST	$G = \frac{N_S}{N_p}\gamma V_I[(1+\frac{T_{ON}}{T_{F1}})\frac{1}{\sqrt{L_SC}}\frac{\sin\omega T_{F1}}{\cos(\omega T_{F1}-\theta)} - \frac{\gamma}{L_SC}T_{ON}]$ $a' = \frac{\gamma}{R_LC}[1+\frac{1}{2}(-1+\frac{C}{L_S}R_CR_L)\frac{T_{F1}}{T_p}] - \frac{1}{T_p}\ln[\frac{\gamma}{\omega\sqrt{L_SC}}\cos(\omega T_{F1}-\theta)]$	$G_p = G/a'$ $\omega_p = a'$	$\omega = \omega'D'$ $K_1 = \frac{1}{\omega'}\frac{\gamma^2}{L_SC}[(1+\frac{R_C}{2R_LD'}-\frac{CR_C^2}{2L_S})$ $(V_o+\frac{N_S}{N_p}V_I)+\gamma(\frac{R_C}{2L_S}+\frac{1}{2R_LD'C})N_S\phi_M]$ $K_2 = \frac{R_C\gamma}{L_S}(V_o+\frac{N_S}{N_p}V_I) - \frac{\gamma^2}{L_SC}N_S\phi_M$	$G_p = \frac{N_S}{N_p}\frac{V_I}{D'^2}$ $\omega_a = \rho(-\frac{\gamma L_SD}{R_LD'^2}-\frac{D}{2}\gamma T_p+\frac{R_CC}{D'})^{-1}$ $\omega_o = \sqrt{\frac{\gamma\rho}{L_SC}}D'$ $Q = \frac{\rho}{\omega_o}\frac{D'}{R_CC+L_S/R_LD'}$
	Where $\theta \triangleq \tan^{-1}\frac{\alpha+f_{22}}{\omega}$, $L_S \triangleq \mu AN_S^2/\ell$, $\gamma \triangleq \frac{R_L}{R_L+R_C}$		Where $D \triangleq T_{ON}/T_p$, $D' \triangleq T_{F1}/T_p$, $\rho = \gamma(1+\frac{R_C}{R_LD'})$	

2.3 Continuous Models-Time Domain and Frequency Domain

The linearized discrete impulse response $g(nT_p)$ developed in the previous section characterizes the small signal behavior of the converter exactly but only at discrete sampling instant. If one is willing to neglect the detail waveforms between samples and study the long range trend of the converter, an equivalent continuous linear impulse response g(t) can be obtained simply by substituting $t=nT_p$ into the expression for $g(nT_p)$ in Table V. [6,8] It is important to note that the discrete-to-continuous transformation is meaningful only if the system response is much slower then the sampling rate. Otherwise, a significant phase delay can be introduced. Such a transformation is made plausible, in the present analysis by the fact that every converter power stage inherently has a low-pass LC filter which largely attenuates the high frequency switching ripple; the natural resonant frequency of the output filter is usually designed to be 1/15 to 1/20 of the switching frequency to achieve good output voltage regulation. The continuous linear impulse response g(t) so derived represents small signal low frequency characteristics of the converter up to one-half of the switching frequency.

The continuous impulse response functions g(t) and their corresponding frequency domain transfer functions G(S) are presented in Table V for both Mode 2 and Mode 1 Operations. The relations given in Table VI are employed to derive the final

TABLE VI Equations for inductor current(boost converter), magnetic flux(buck/boost converter), and output voltage at the sampling instant.

	MODE 2	Mode 1
BOOST	$I_M = \frac{1}{L} T_{ON} V_I$ $V_o = (1 + \frac{T_{ON}}{T_{F1}})V_I$	$I_M = \frac{1}{D'^2 R_L} V_I + \frac{1}{2L} D T_P V_I$ $V_o = V_I/D'$
BUCK/ BOOST	$\phi_M = \frac{1}{N_P} T_{ON} V_I$ $V_o = \frac{N_S}{N_P} \frac{T_{ON}}{T_{F1}} V_I$	$\phi_M = \frac{1}{N_P} \frac{D}{D'^2} \frac{L_S}{R_L} V_I + \frac{1}{2N_P} D T_P V_I$ $V_o = \frac{N_S}{N_P} \frac{D}{D'} V_I$

expressions for g(t) and G(S) in terms of known circuit parameters and the input voltage. It should be noted that the transfer functions for Mode 1 Operation are presented in the same form as those developed using averaging techniques shown in Table 1 of Ref. 1, so that comparisons between corresponding models can be made conveniently later in the paper.

3. DISCUSSIONS

3.1 Model Interpretations

The discrete time domain modeling technique described in the previous sections provides a uniform approach which covers both Mode 1 and Mode 2 Operations. Employing this uniform technique, the mathematical models derived for both Mode 1 and Mode 2 therefore provide an ideal basis for comparitive studies. Conclusions of significant importance are drawn including the following:

- All three converter power stages behave as first-order systems in Mode 2, as contrary to second order systems in Mode 1. An abrupt transition of the transfer characteristic is shown when the inductor MMF emerges from Mode 1 to Mode 2 or vise versa.
- In Mode 2, the gain and the corner frequency are both functions of the input voltage, the load, all power stage parameters, the switching frequency, and the time intervals T_{ON} and T_{F1}; while in Mode 1, the gain is only related to the input voltage V_I and the duty cycle ratio $D' \triangleq T_{F1}/T_P$ and the corner frequency is dominated by the output filter LC and the duty cycle ratio D'.
- The transfer functions for boost converter and buck/boost converter in Mode 1 contain a right-half-plane zero(ω_a), if the following inequalities are satisfied

$$\left(\frac{L}{R_L D'^2} + \frac{D}{2} T_P\right) \frac{R_L}{R_L + R_C} > \frac{R_C C}{D'} \quad \text{for boost converter} \qquad (17)$$

$$\left(\frac{L_S D}{R_L D'^2} + \frac{D}{2} T_P\right) \frac{R_L}{R_L + R_C} > \frac{R_C C}{D'} \quad \text{for buck/boost converter} \qquad (18)$$

The above inequalities are often satisfied in Mode 1 design. The positive zero will provide an additional 90° phase lag. It is interesting to note that the positive zero is a function of the switching period T_P[7]. The longer the switching period the smaller the positive zero $-\omega_a$; therefore, the effect of the additional phase lag begins at lower corner frequency. [7]

The above conclusions are only general remarks. Additional insights to the models will be provided in the following section where analysis and test results of a single-loop controlled buck converter operating at both Mode 1 and Mode 2 are presented.

3.2 Model Improvements

The frequency domain transfer functions for Mode 1 Operation in the present analysis are compared with those developed using averaging technique by Wester et al., Table 1 of Ref. 1, with the following important conclusions. It should be noted that the single winding buck/boost converter presented in [1] is a special case of the two winding buck/boost when $N_p = N_S$.

- The transfer functions for the buck converter derived from both analyses are identical.
- The power stage gain G_P and the natural resonant frequency ω_o of boost and buck/boost are about the same as those derived using averaging technique. The Q factors are smaller than those of the corresponding average models.
- The transfer functions for boost and buck/boost have one positive zero and one negative zero in average models but only has one conditional positive zero in the present models.
- The positive zero for boost and buck/boost converters is a function of the switching frequency, while its counterpart is independent of the switching frequency

For convenience, the transfer function of the boost converter derived from averaging technique is presented in the following:

$$G(s) = G_P \frac{\left(1+\frac{s}{\omega_z}\right)\left(1-\frac{s}{\omega_a}\right)}{1+\frac{1}{Q}\frac{s}{\omega_o}+\frac{s^2}{\omega_o^2}} \qquad (19)$$

where

$$Q = \frac{1}{\omega_o}\left(CR_C + \frac{L}{R_L D'^2}\right)^{-1}, \quad \omega_a = \frac{D'^2 R_L}{L}, \quad \omega_z = \frac{1}{CR_C}$$

$$G_P = V_I/D'^2 \quad \text{and} \quad \omega_o^2 = \frac{1}{LC}\frac{D'^2 R_L}{R_L + R_C}$$

For comparison, the gain and phase plots of a boost converter derived from both the averaging technique and the present analysis are sketched in Fig. 6. The following numerical values are used:

$T_P = 10^{-4}$ secs, $L = 6mH$, $C = 41.7\mu f$, $R_L = 60\Omega$, $R_C = 1\Omega$, $V_I = 60V$, $V_o = 30V$.

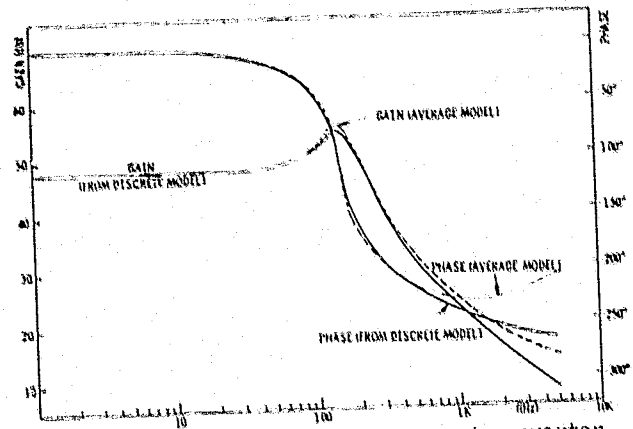

Fig.6 Frequency response for the boost converter power stage from the present analysis (solid curves) and from the average model(dotted curves)

Excellent agreements are shown between results of these two analytical approaches in the low frequency range, except a higher resonant peak is shown in the average model.[3] The differences of these two models become significant when the frequency is greater than 1kHz; the average model has larger gain and phase angle. This is primarily due to the somewhat different effects of the capacitor ESR as results of the two different modeling techniques. Comparing (19) with the corresponding transfer function in Table V, a stronger contribution of ESR to the phase lead is shown in the average model due to the additional second-order term, $-S^2/(\omega_a\omega_z)$, in the numerator. This may very well explain the reported discrepancy between averaging models and measurement data at high frequency. Take Fig. 17 of Ref. 1 as an example, the measurement data shows a less gain and a smaller phase angle beginning at about 1/10 of the switching frequency.

4. VERIFICATIONS

A buck converter, represented by the block diagram in Fig. 1, was designed to operate in the continuous current model under normal-to-heavy load conditions and in the discontinuous current mode at light load. The small signal block diagram of the converter is shown as Fig. 7. The compensation network is a lead-lag circuit having the following known transfer characteristic,

$$G_c = 193.3\,\frac{1+f/20}{1+f/0.3}\;\frac{1+f/1225}{1+f/3263} \qquad (20)$$

The pulsewidth modulator, as shown in Fig. 8, compares the error signal $V_e(t)$ with a fixed ramp $A(t)$.

$$A(t) = A_0(t-nT_p), \quad nT_p \le t \le (n+1)T_p \qquad (21)$$

Where $A_0 = 6.25\times10^4$ V/S is the slope of the ramp. The output of the PWM is a unity pulse train, with its pulse duration governed by (22).

$$d(t) = \begin{cases} 1 & \text{if } A(t) \le V_e(t) \\ 0 & \text{if } A(t) \ge V_e(t) \end{cases} \qquad (22)$$

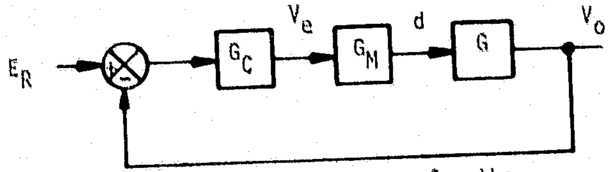

Fig.7 Simplified block diagram for the buck converter.

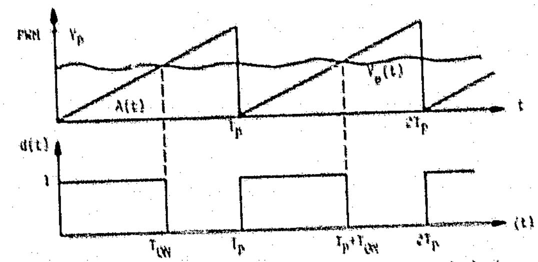

Fig.8 Waveforms for the pulsewidth modulator.

The describing function of the PWM was derived in Ref. 2; the gain of PWM is simply

$$k_M = \frac{1}{V_p} \qquad (23)$$

Due to the circuit implementation there is a 8μs delay from the signal d(t) to the power switch. For convenience this time delay is included in the PWM functional block in Fig. 7. The transfer function of the PWM is therefore represented as

$$G_M = \frac{1}{A_0 T_p}\, e^{j\omega\tau_d} \qquad (24)$$

The circuit parameters used for the power stage are listed: L = 1mH, C = 455μf, R_C = 0.034Ω, R_L = 150Ω, T_P = 50μs, V_I = 40V, and V_o = 20V.

Fig. 9 shows the frequency response of the power stage together with the PWM in Mode 2 Operation. Results from both analysis and measurement are presented with excellent correlation. For comparison, the analytical gain and phase of $G_M G$ for Mode 1, when R_L = 6.67Ω, is also presented in Fig. 9 as dotted-line curves. It is evident that the converter behaves as a first-order system in mode 2 in contrary to a second-order system in mode 1. In mode 2, since the phase lag of $G_M G$ is at most 90° and the corner frequency is usually low, only a gain compensation(an error amplifier) is needed to improve the transient response and to ensure the loop stability. The improvement of audiosusceptibility of the converter in mode 2 is due to the fact that the transfer function of the power stage is only first order with low corner frequency and no peaking effect.

It has been made evident in the analysis that an abrupt reduction of system order (a jump phenomenon) is shown when the inductor MMF emerges from Mode 1 to Mode 2 or vise versa. This was verified by measuring the open-loop crossover frequency of the converter when the load is gradually reduced. The crossover frequency, as shown in Table VII, remains unchanged as long as the converter is operating in Mode 1. When the load is reduced to approximately 90 to 100 ohms, the

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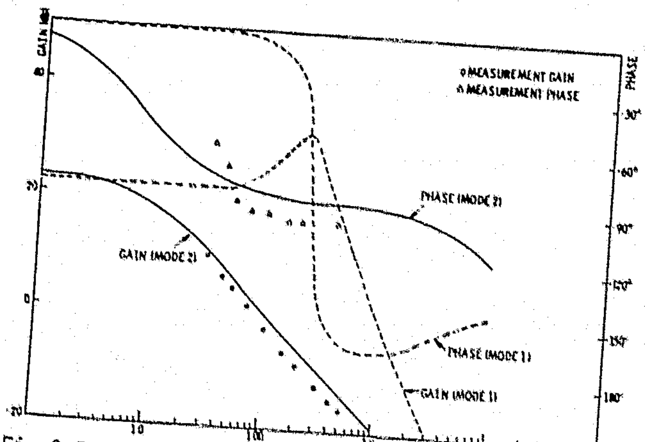

Fig.9 Frequency response for buck converter power stage together with PWM in mode 2(solid curves), when R_L=150 ohms,and mode 1(dotted curves), when R_L=6.67 ohms.

TABLE VII Open-Loop Crossover Frequency as a Function of Load

R_L (ohms)	10-70	80	90	100	110	120	130	140
Open Loop Crossover Frequency(Hz)	1650	1600	1450	450	250	215	205	200

converter begins to operate in between Mode 1 and Mode 2 affected by the disturbance of the small injected signals for measurement purpose. A very significant reduction of the crossover frequency can be seen when the load is lighter than 110 ohms. Further increasing R_L only results in a gradual reduction of the crossover frequency.

In Mode 2 operation, the gain Gp and the corner frequency ω_p of the transfer function are plotted in Fig. 10(A-F) as a function of circuit parameters L and C, the switching frequency f_P,the load R_L, the input voltage V_I, and the output voltage V_O, respectively. For decreasing L, Gp increases but ω_p remains essentially constant; the magnitude of L only affects the gain but not the phase. For decreasing C, ω_p increases but Gp remains constant; the effect of C is preserved when the converter operates in Mode 2. The characteristics of L and C presented in Fig. 10(A) and (B) have the following significant meanings: a desirable crossover frequency together with sufficient phase margin, greater than 90°, of the system open loop characteristics can be obtained by simply adjusting the magnitudes of L and C or employing only a gain compensation network, i.e., an error amplifier. The effect of reducing the switching frequency is similar to that of reducing L. Fig. 10(D-F) shows the effect of changing T_{F2}/T_P by varying R_L, V_I and V_O, respectively. In general, larger T_{F2}/T_P ratio corresponds to larger G_p and smaller ω_p. This can be accomplished by increasing R_L or V_I or reducing V_O.

The previous discussions reveal certain unique performance characteristics associated with mode 2 operation, which very much affect the basic design philosophies. For example, the loop

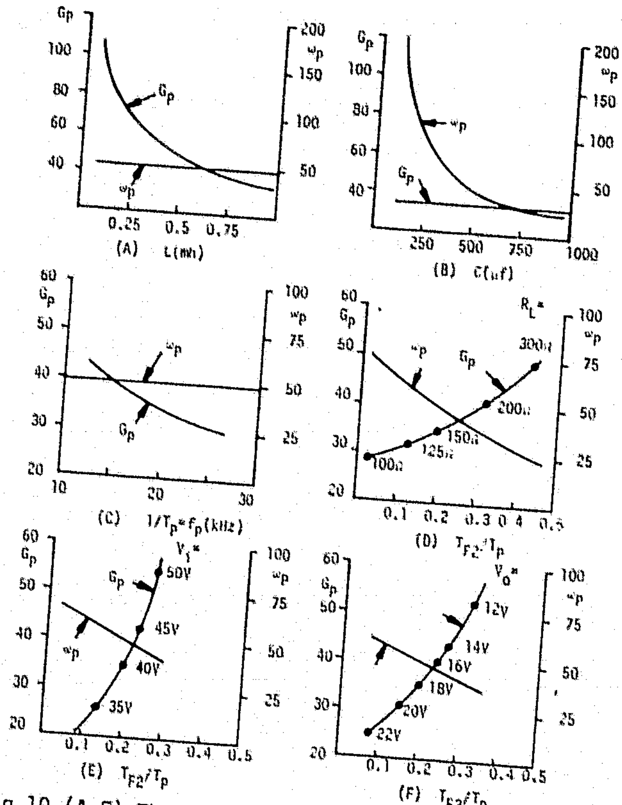

Fig.10.(A-F) The gain G_p and the corner frequency ω_p of the buck converter in mode 2 are plotted as functions of the following parameters: L,C, f_P, R_L, V_I and V_O, respectively.

stability becomes a trivial problem and the transient response is well damped rather than oscillotory. The analysis also provides guidelines upon which the power stage parameters can be designed and the switching frequency can be selected to achieve certain performance specifications.

5. CONCLUSIONS

State space techniques are employed to derive discrete models for buck, boost and buck/boost converters operating with and without zero-inductor MMF dwell time. The duty-cycle-to-output linear discrete-time-domain models are derived in closed forms,which describe the discrete behavior of converters about their equilibrium state exactly. These discrete models are then approximated by frequency domain transfer functions representing the low frequency characteristics of converters up to one-half of the switching frequency.

The power stage models are shown to be first order for all three converters with the dwell time, as contrary to second order without the dwell time. The analysis makes evident certain abrupt changes of system behavior often observed in the breadboard performance when the dwell time appears. These include pronounced improvements of stability margin, audio susceptibility and transient response, from oscillatory to well damped. Graphs are presented to illustrate influences of power stage parameters, switching frequency, input voltage, load, and the time intervals corresponding to the ON and OFF of the power switch to a buck converter with the dwell time. Foundation is laid for power stage design and trade-off evaluation for converter operating with and without zero-inductor-current dwell time.

Evaluations of converter performance are also made between the present models and the corresponding average models, in continuous current operation. Certain improvements of the present models are shown in the high frequency range when the output-filter capacitor ESR begins to shape the gain and phase of their corresponding frequency responses.

The present analysis can be extended to include the input filter and second stage of the output filter which in many applications are the integral parts of the power processor.

APPENDIX A

DERIVATIONS FOR $\frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_k°)}$ and $\frac{d\underline{X}^*(t_k°)}{dt_k^*}$

A.1 Derivations for $\frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_k°)}$

Applying Chain Rule, one can express

$$\frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_k°)} = \frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_{k2}°)}\ \frac{d\underline{X}^*(t_{k2}°)}{d\underline{X}^*(t_{k1}°)}\ \frac{d\underline{X}^*(t_{k1}°)}{d\underline{X}^*(t_k°)} \quad \text{(A-1)}$$

The derivations for each term on the right hand side of (A.1) is presented in the following:

(1) Computing $\frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_{k2}°)}$

Differentiate (7) in the main text $\frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_{k2}°)}$

$$= \phi3(t_{k+1}°-t_{k2}^*)\left[-F3\underline{X}^*(t_{k2}^*)\ \frac{dt_{k2}^*}{d\underline{X}^*(t_{k2}°)} + \frac{d\underline{X}^*(t_{k2}^*)}{d\underline{X}^*(t_{k2}°)}\right] - \phi3(t_{k+1}°-t_{k2}^*)G3\ V_I\ \frac{dt_{k2}^*}{d\underline{X}^*(t_{k2}°)} \quad \text{(A-2)}$$

Consider the following state transition equation

$$\underline{X}^*(t_{ki}^*) = \phi i(t_{ki}^*-t_{ki}°)\ \underline{X}^*(t_{ki}°) + \int_{t_{ki}°}^{t_{ki}^*} \phi i\ (t_{ki}^*-S)d\ S\ Gi\ \underline{U}$$

$$i = 1,\ 2,\ 3 \quad \text{(A-3)}$$

Differentiate $\underline{X}^*(t_{ki}^*)$ with respect to $\underline{X}^*(t_{ki}°)$

$$\frac{d\underline{X}^*(t_{ki}^*)}{d\underline{X}^*(t_{ki}°)} = \phi i(t_{ki}^*-t_{ki}°) + \frac{d\phi i(t_{ki}^*-t_{ki}°)}{d\ t_{ki}^*}\ \underline{X}^*(t_{ki}°)\ \frac{dt_{ki}^*}{d\underline{X}^*(t_{ki}°)} + \phi i(t_{ki}^*-t_{ki}^*)Gi\ \underline{U}\ \frac{dt_{ki}^*}{d\underline{X}^*(t_{ki}°)}$$

For small disturbance about equilibrium

$$\phi i(t_{ki}^*-t_{ki}°) = I$$

$$\frac{d\underline{X}^*(t_{ki}^*)}{d\underline{X}^*(t_{ki}°)} \approx I + \left[F_i\ \underline{X}^*(t_{ki}°)+G_i\ \underline{U}\right]\frac{dt_{ki}^*}{d\underline{X}^*(t_{ki}°)} \quad \text{(A-4)}$$

Since the clock signal initiate the turn on of the power transistor

$$\frac{dt_{k2}^*}{d\underline{X}^*(t_{k2}°)} \equiv 0 \quad \text{(A-5)}$$

Substituting (A-4) and (A-5) into (A-2)

$$\frac{d\underline{X}^*(t_{k+1}°)}{d\underline{X}^*(t_{k2}°)} = \phi3(t_{k+1}°-t_{k2}^*) \approx \phi3(T_{ON}°) \quad \text{(A-6)}$$

(2) Computing $\frac{d\underline{X}^*(t_{k2}°)}{d\underline{X}^*(t_{k1}°)}$

Differentiating equation (6) in the main text, and substituting (A-4) into the result, one can obtain

$$\frac{d\underline{X}^*(t_{k2}°)}{d\underline{X}^*(t_{k1}°)} = \phi(t_{k2}°-t_{k1}^*)\left\{I + \left[(F1-F2)\underline{X}^*(t_{k1}°) + (G1-G2)\ \underline{U}\right]\ \frac{dt_{k1}^*}{d\underline{X}^*(t_{k1}°)}\right\} \quad \text{(A-7)}$$

In the vicinity of $t_{k1}°$, consider the following equation:

$$\underline{X}^*(t_{k1}^*) = \phi1(t_{k1}^*-t_{k1}°)\underline{X}^*(t_{k1}°) + \int_{t_{k1}°}^{t_{k1}^*} \phi1(t_{k1}^*-S)G1\ \underline{U}\ dS \quad \text{(A-8)}$$

At $t = t_{k1}^*$ the inductor MMF is equal to zero

$$C1\ \underline{X}^*(t_{k1}^*) = 0 \quad \text{(A-9)}$$

where $C1 = [1 \quad 0]$

Differentiating (A-9) with respect to $\underline{X}^*(t_{k1}°)$

$$C1\left[\frac{\partial\underline{X}^*(t_{k1}^*)}{\partial t_{k1}^*}\ \frac{dt_{k1}^*}{d\underline{X}^*(t_{k1}°)} + \frac{\partial\underline{X}^*(t_{k1}^*)}{\partial\underline{X}^*(t_{k1}°)}\right] = 0$$

therefore $\frac{dt_{k1}^*}{d\underline{X}^*(t_{k1}°)}$

$$= \frac{-C1\phi1(t_{k1}^*-t_{k1}°)}{C1[F1\ \phi1(t_{k1}^*-t_{k1}°)\underline{X}^*(t_{k1}°)+\phi1(t_{k1}^*-t_{k1}\ )G1\ \underline{U}]} \quad \text{(A-10)}$$

If the perturbance is very small,

$$\frac{dt_{k1}}{d\underline{X}^*(t_{k1}°)} = \frac{-C1}{C1[F1\underline{X}^*(t_{k1}°)+G1\ \underline{U}]} \quad \text{(A-11)}$$

Substituting (A-11) into (A-7), one can obtain

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$$\frac{d\underline{X}^*(t_{k2}°)}{d\underline{X}^*(t_{k1}°)} = \Phi 2(T_{F2}) \Big\{ I+[(F1-F2)\underline{X}^*(t_{k1}°) +(G1-G2)\underline{U}] \frac{-C1}{C1[F1\ \underline{X}^*(t_{k1}°)+G1\ \underline{U}]} \Big\} \quad (A-12)$$

For small signal disturbances, the following expression can be simplified, for all converters.

$$I+[(F1-F2)\underline{X}^*(t_{k1}°)+(G1-G2)\underline{U}] \frac{-C1}{C1F1\ \underline{X}^*(t_{k1}°)+G1\ \underline{U}}$$

$$=I - [(F1-F2)\begin{bmatrix} o \\ V_o \end{bmatrix}+(G1-G2)\underline{U}]\ C1/[C1F1\begin{bmatrix} o \\ V_o \end{bmatrix} + G1\ \underline{U}] = \begin{bmatrix} o & o \\ o & 1 \end{bmatrix} \quad (A-13)$$

(3) Computing $\frac{d\underline{X}^*(t_{k1}°)}{d\underline{X}^*(t_k°)}$

Differentiating equation (5) in the main text and and substituting (A-4) into it, one can obtain

$$\frac{d\underline{X}^*(t_{k1}°)}{d\underline{X}^*(t_k°)} = \Phi 1(t_{k1}°-t_k^*) \Big\{[(F3-F1)\underline{X}^*(t_k^*)+(G3-G1)\underline{U}] \times \frac{dt_k^*}{d\underline{X}^*(t_k°)} + I \Big\} \approx \Phi 1(T_{F1}°) \quad (A-14)$$

where $\frac{dt_k^*}{d\underline{X}^*(t_k°)} \cong 0$, since the duty cycle disturbance is determined by the control loop.

A.2 Derivations for $\frac{d\underline{X}^*(t_k°)}{dt_k^*}$

In the neighborhood of $t_k°$, one can express

$$\underline{X}^*(t_k°) = \Phi 1(t_k°-t_k^*)\ \underline{X}^*(t_k^*) +\Phi 1(t_k°) \int_{t_k^*}^{t_k°} \Phi 1(-S)\ dS\ G1\ \underline{U} \quad (A-15)$$

Differentiate (A-15) with respect to t_k^*,

$$\frac{d\underline{X}^*(t_{k1}°)}{dt_k^*} = \Phi 1(t_k°-t_k^*) \frac{d\underline{X}^*(t_k^*)}{dt_k^*} -F1\Phi 1(t_k°-t_k^*)\ \underline{X}^*(t_k^*) -\Phi 1(t_k°-t_k^*)\ G1\ \underline{U} \approx (F3-F1)\underline{X}^{\bullet}(t_k^{\bullet}) +(G3-G1)\ \underline{U} \quad (A-16)$$

APPENDIX B

DERIVATIONS FOR $\Phi^n(T_p)$

Matrices $\Phi^n(T_p)$ are derived for buck, boost, and buck/boost converters in both Mode 1 and Mode 2 operations.

B.1 Mode 2 Operation

The expressions for $\Phi^n(T_p)$ of the three converters are derived individually.

(1) Buck Converter

Referring to Table III

$$\Phi(T_p) = e^{-aT_p} \begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix} \quad (B-1)$$

since $\quad \Phi_{11}\Phi_{22} - \Phi_{12}\Phi_{21} = 0 \quad$ (B-2)

One can express

$$[\Phi(T_p)]^2 = e^{-aT_p}\ (\Phi_{11}+\Phi_{22})\ \Phi(T_p) \quad (B-3)$$

The following result is obtained by mathematical induction:

$$[\Phi(T_p)]^n = e^{-(n-1)aT_p}\ (\Phi_{11}+\Phi_{22})^{n-1}\Phi(T_p) \quad (B-4)$$

(2) Boost Converter and Buck/Boost Converter

It is shown in Table III that the expression $\Phi^n(T_p)$ for the boost converter and buck/boost converter is a special case of buck converter where $\Phi_{11} = \Phi_{12} = 0$. Therefore, it is straight forward to show that

$$\Phi^n(T_p) = e^{-anT_p}\Phi_{22}\ ^{n-1} \begin{bmatrix} o & o \\ \Phi_{21} & \Phi_{22} \end{bmatrix} \quad (B-5)$$

B.2 Mode 1 Operation

(1) Buck Converter

Since F3=F1 for the buck converter, it is obvious that

$$\Phi(T_p) = \Phi 3(T_{ON})\ \Phi 1(T_{F1}) = e^{F1(T_{ON}+T_{F1})} = e^{F1\ Tp} \quad (B-6)$$

and $\quad \Phi^n(T_p) = e^{F1(nT_p)} \quad$ (B-7)

(2) Boost Converter and Buck/Boost Converter

By definition $\Phi(T_p) \triangleq e^{F3T_{ON}}\ e^{F1T_{F1}} \quad$ (B-8)

Applying Baker-Campbell-Hausdorff Series [10], which says

$$e^A\ e^B = e^C \quad (B-9)$$

where

$$C = A+B+\frac{1}{2}(AB-BA) + \text{higher order terms} \quad (B-10)$$

Employing the first two terms of (B-10), one can approximate (B-8) by

$$\phi(T_p) \triangleq e^{FT_p} \approx e^{F3T_{ON}+F1T_{F1}+(F3T_{ON})(F1T_{F1})} - (F1T_{F1})(F3T_{ON}) \quad (B-11)$$

Applying Table I of the main text, one can express

$$FT_p = \begin{bmatrix} f_{11}D' & f_{12}D'(1-f_{22}T_{ON}) \\ f_{21}D'(1+f_{22}T_{ON}) & f_{22} \end{bmatrix} T_p \quad (B-12)$$

Since the following inequality is always true

$$|f_{22}T_{ON}| = \frac{T_{ON}}{C\ (R_C+R_L)} << 1,$$

equation (B-12) can be simplified by

$$FT_p = \begin{bmatrix} f_{11}D' & f_{12}D' \\ f_{21}D' & f_{22} \end{bmatrix} T_p \quad (B-13)$$

Therefore

$$\phi^n(T_p) = e^{FnT_p} = \phi(nT_p) \quad (B-14)$$

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APPENDIX G

DERIVATION OF Φ AND D MATRICES FOR EXAMPLE 2 OF SECTION 4.7.2.

G.1 SYSTEM EQUATIONS

The circuit diagram of the boost regulator has been given in Figure 22 in the main text. The system is of 4th order. The following variables are chosen:

v_C = the voltage across the output capacitor C_o

i = the current through the energy storage inductor L_o

e_R = the voltage at the R_5C_2 compensation network as shown in Fig. 1

e_C = the integrator output voltage.

Two dummy variables e_i, i_D are introduced to represent nonlinear characteristics of the system.

The system equations are, in the power stage,

$$\frac{dv_C}{dt} = -\frac{1}{C_o}\frac{1}{R_S+R_L}v_C + \frac{1}{C_o}\frac{R_L}{R_S+R_L}i_D \tag{G1}$$

$$\frac{di}{dt} = (-R_o i - e_i + E_I)\frac{1}{L_o} \tag{G2}$$

in the control loops,

$$\frac{de_R}{dt} = \frac{1}{C_2R_5}\frac{R_L}{R_S+R_L}v_C + \frac{1}{C_2R_5}\frac{R_SR_L}{R_S+R_L}i_D - \frac{1}{C_2R_5}e_R \tag{G3}$$

$$\begin{aligned}\frac{de_C}{dt} = &\left(-\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} - \frac{1}{C_1R_5}\right)\frac{R_L}{R_S+R_L}v_C + \frac{nR_o}{C_1R_4}i \\ &+ \left(-\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} - \frac{1}{C_1R_5}\frac{R_L}{R_S+R_L}\right)\frac{R_SR_L}{R_S+R_L}i_D \\ &+ \frac{1}{C_1R_5}e_R + \frac{n}{C_1R_4}e_i - \frac{n}{C_1R_4}E_I + \frac{1}{C_1R_3}E_R\end{aligned} \tag{G4}$$

The output voltage e_o (not a variable of the system)

$$e_o = \frac{R_SR_L}{R_S+R_L}i_D + \frac{R_L}{R_S+R_L}v_C \tag{G5}$$

G.2 DIFFERENTIAL-DIFFERENCE EQUATIONS

Since the power transistor and the diode are served as switches S1 and S2, three possible modes of operation are presented:

(1) S1:ON, S2:OFF } the power transistor is ON and the diode is OFF,

(2) S1:OFF, S2:ON } the power transistor is OFF and the diode is ON,

(3) S1:OFF, S2:OFF } the power transistor and the diode are both OFF.

The system is designed to operate in these three modes in the steady state operation. However, during transient, the system may operate in mode 1 and mode 2 only.

The time intervals during mode 1, mode 2, and mode 3 operation are assigned as t_{ON}, T_{OFF}', and t_{OFF}'', respectively. In these three modes of operation, dummy variables e_i and i_D are assigned to different variables. The waveform of e_i is shown in Fig. 2.

System equations (G1 to G4) can be rewritten in the form of state equations.

Let

$$x_1 \triangleq v_C \qquad u_1 = E_I$$

$$x_2 \triangleq i \qquad u_2 = E_R$$

$$x_3 \triangleq e_R \qquad u_3 = E_Q$$

$$x_4 \triangleq e_C \qquad u_4 = E_D$$

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(1) During t_{ON}, S1:ON, S2:OFF

$$e_i = E_Q$$

$$i_D = o$$

$$\dot{x}_1 = -\frac{1}{C_o(R_S+R_L)}\, x_1$$

$$\dot{x}_2 = -\frac{R_o}{L_o} x_2 + \frac{1}{L_o} u_1 - \frac{1}{L_o}\, u_3$$

$$\dot{x}_3 = \frac{1}{C_2R_5}\,\frac{R_L}{R_S+R_L}\, x_1 - \frac{1}{C_2R_5}\, x_3$$

$$\dot{x}_4 = \frac{R_L}{R_S+R_L}\left(-\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} - \frac{1}{C_1R_5}\right)x_1 + \frac{nR_o}{C_1R_4}x_2$$
$$+ \frac{1}{C_1R_5}x_3 - \frac{n}{C_1R_4}u_1 + \frac{1}{C_1R_3}u_2 + \frac{n}{C_1R_4}u_3$$

(2) During T_{F1} ', S1:OFF, S2:ON

$$e_i = E_D + \frac{R_L}{R_S+R_L}v_C + \frac{R_SR_L}{R_S+R_L}i$$

$$i_D = i$$

$$\dot{x}_1 = -\frac{1}{C_o(R_S+R_L)}x_1 + \frac{1}{C_o}\frac{R_L}{R_S+R_L}x_2$$

$$\dot{x}_2 = -\frac{R_L}{L_o(R_S+R_L)}x_1 - \left(R_o + \frac{R_SR_L}{R_S+R_L}\right)\frac{1}{L_o}x_2 + \frac{1}{L_o}u_1$$
$$-\frac{1}{L_o}u_4$$

$$\dot{x}_3 = \frac{1}{C_2R_5}\frac{R_L}{R_S+R_L}x_1 + \frac{1}{C_2R_5}\frac{R_SR_L}{R_S+R_L}x_2 - \frac{1}{C_2R_5}x_3$$

$$\dot{x}_4 = -\left(\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} + \frac{1}{C_1R_5} - \frac{n}{C_1R_4}\right)\frac{R_L}{R_S+R_L}x_1$$
$$+ \left[\frac{nR_o}{C_1R_3} - \left(\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} + \frac{1}{C_1R_5} - \frac{n}{C_1R_4}\right)\frac{R_SR_L}{R_S+R_L}\right]x_2$$
$$+ \frac{1}{C_1R_5}x3 - \frac{n}{C_1R_4}u_1 + \frac{1}{C_1R_3}u_2 + \frac{n}{C_1R_4}u_4$$

(3) During T_{F2} , S1:OFF, S2:OFF

$$e_i = E_I$$

$$i_D = i = 0$$

$$\dot{x}_1 = -\frac{1}{C_o}\frac{1}{R_S+R_L}x_1$$

$$\dot{x}_2 = 0$$

$$\dot{x}_3 = \frac{1}{C_2R_5}\frac{R_L}{R_S+R_L}x_1 - \frac{1}{C_2R_5}x_3$$

$$\dot{x}_4 = \left(-\frac{1}{C_1R_3}\frac{R_2}{R_1+R_2} - \frac{1}{C_1R_5}\right)\frac{R_L}{R_S+R_L}x_1 + \frac{1}{C_1R_5}x_3 + \frac{1}{C_1R_3}u_2 \qquad (9\text{-}3)$$

The output voltage, equation (5), can be written in the same pattern

(1) During t_{ON}

$$e_o = \frac{R_L}{R_S+R_L}x_1$$

(2) During t_{OFF}'

$$e_o = \frac{R_L}{R_S+R_L}x_1 + \frac{R_SR_L}{R_S+R_L}x_2$$

(3) During t_{OFF}''

$$e_o = \frac{R_L}{R_S+R_L}x_1$$

The above system equations can be written in the following compact forms

(1) During t_{ON} (G6)

$$\dot{\underline{x}} = F1\,\underline{x} + G1\,\underline{u}$$

$$e_o = \frac{R_L}{R_S+R_L}x_1$$

(2) During T_{F1} (G7)

$$\dot{\underline{x}} = F2\,\underline{x} + G2\,\underline{u}$$

$$e_o = \frac{R_L}{R_S+R_L}x_1 + \frac{R_SR_L}{R_S+R_L}x_2$$

(3) During T_{F2} (G8)

$$\dot{\underline{x}} = F3\,\underline{x} + G3\,\underline{u}$$

$$e_o = \frac{R_L}{R_S+R_L}x_1$$

where F1, F2, F3, G1, G2, and G3 are (4 x 4) matrices

$$\dot{\underline{x}} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} , \quad \underline{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix}$$

$$\underline{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \end{bmatrix}$$

3.2 Discrete Time Model

The solution of a linear system equation of the form

$$\dot{\underline{x}} = F\,\underline{x} + G\,\underline{u} \tag{G9}$$

is

$$\underline{x}(t) = e^{(t-t_o)F}\,\underline{x}(t_o) + \int_{t_o}^{t} e^{(t-\tau)F}\,G\,\underline{u}\,d\tau \tag{G10}$$

where t_o is the initial time and $\underline{x}(t_o)$ is the initial state. The solution (G10) can be generalized so that the state at $t = t_k + T$ can be represented by the state at $t = t_k$ and the time increment T.

$$\underline{x}(t_k+T) = e^{FT}\,\underline{x}(t_k) + e^{FT}\,[\int_0^T e^{-FS}ds]\,G\,\underline{u} \tag{G11}$$

Define the following matrices:

$$\Phi(T) = e^{FT} \quad \text{(state transition matrix)} \tag{G12}$$

$$B(T) = e^{FT} \int_0^T e^{-FS}ds \tag{G13}$$

$$D(T) = B(T)\,G \quad \text{(input matrix)} \tag{G14}$$

Then, equation (G11) becomes

$$\underline{x}\,(t_k+T) = \Phi(T)\,\underline{x}\,(t_k) + D(T)\,u \tag{G15}$$

The system equations (G6) to (G8) have the following close form equations.

$$\underline{x}\,(t_1^K) = \underline{x}(t_K+T_1^K) = \Phi_1(T_1^K)\,\underline{x}\,(t_K) + D_1\,(T_1^K)\,\underline{u} \tag{G16}$$

$$\underline{x}\,(t_2^K) = \underline{x}(t_1^K + T_2^K) = \Phi_2\,(T_2^K)\,\underline{x}\,(t_1^K) + D_2(T_2^K)\,\underline{u} \tag{G17}$$

$$\underline{x}\,(t_{K+1}) = \underline{x}(t_2^K+T_3^K) = \Phi_3\,(T_3^K)\,\underline{x}\,(t_2^K) + D_3(T_3^K)\,\underline{u} \tag{G18}$$

where the state transition matrices Φ_i are

$$\Phi_i(T) = e^{F_i\,T} \qquad i = 1, 2, 3 \tag{G19}$$

and the input matrices D_i are

$$D_i(T) = e^{F_i\,T}\,[\int_0^T e^{-F_i\,S}ds]\,G_i \qquad i = 1, 2, 3 \tag{G20}$$

The nonlinear discrete time system that describes the converter behavior exactly, can now be obtained by combining the closed form solutions (G16) to (G18):

$$\underline{x}(t_{K+1}) = \Phi_3(T_3^K)\,\{\,\Phi_2(T_2^K)[\Phi_1(T_1^K)\,\underline{x}\,(t_K) + D_1(T_1^K)\,\underline{u}]$$
$$+ D_2(T_2^K)\,\underline{u}\,\} + D_3(T_3^K)\,\underline{u}$$

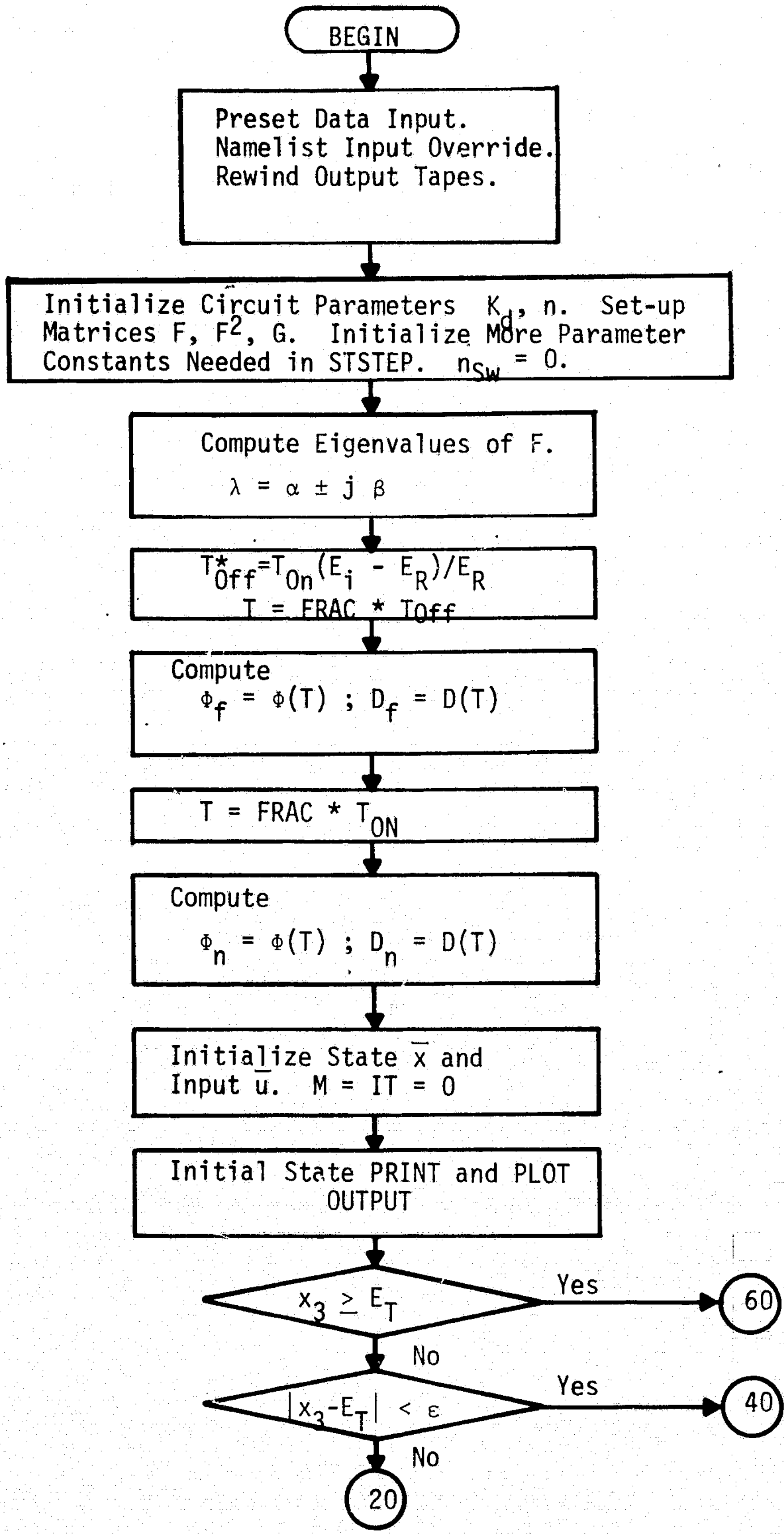
which can be written in the short form as

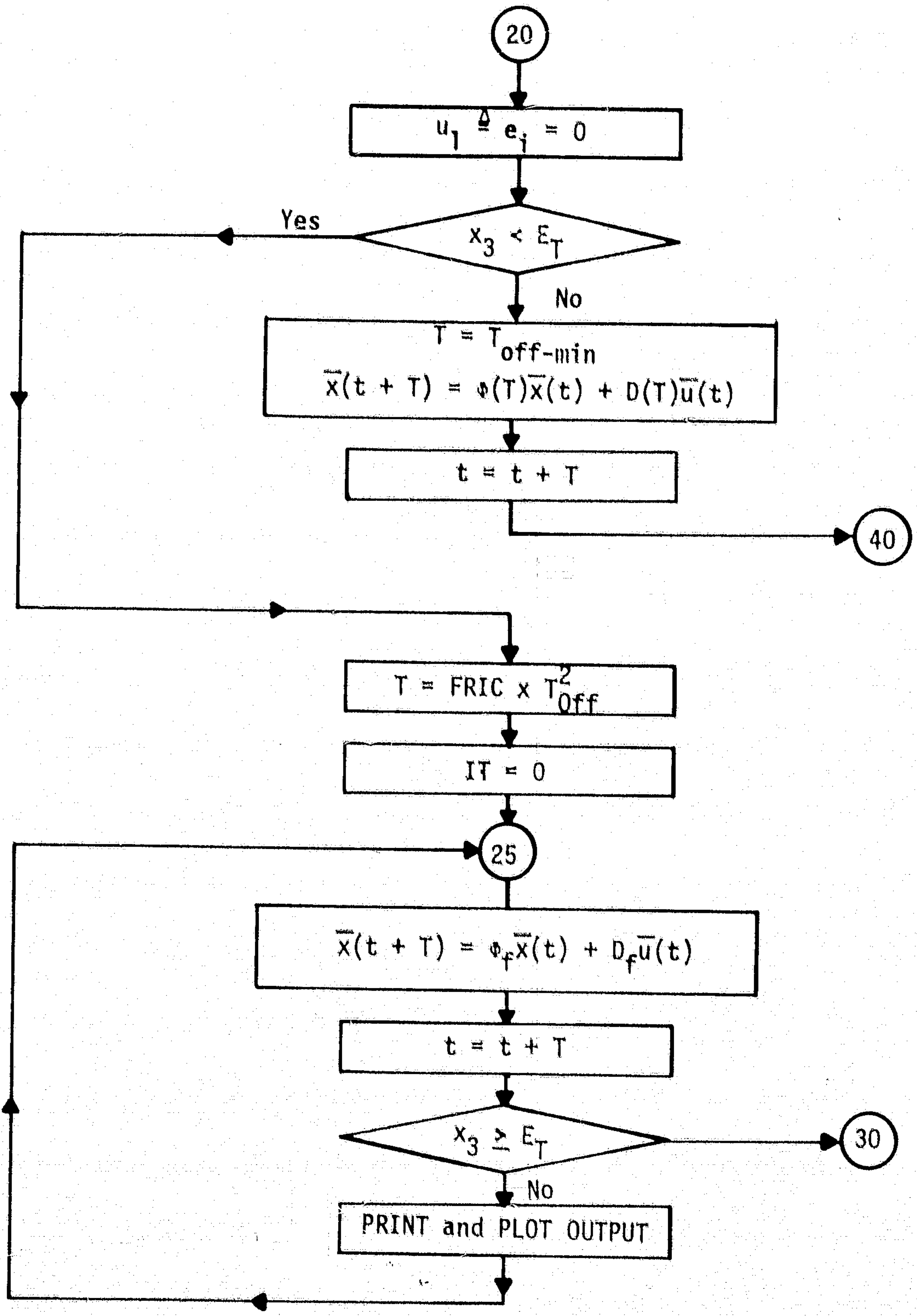
$$\underline{x}(t_{K+1}) = f\,(\underline{x}(t_K),\, T_1^K\,,\, T_2^K\,,\, T_3^K\,,\, \underline{u})$$

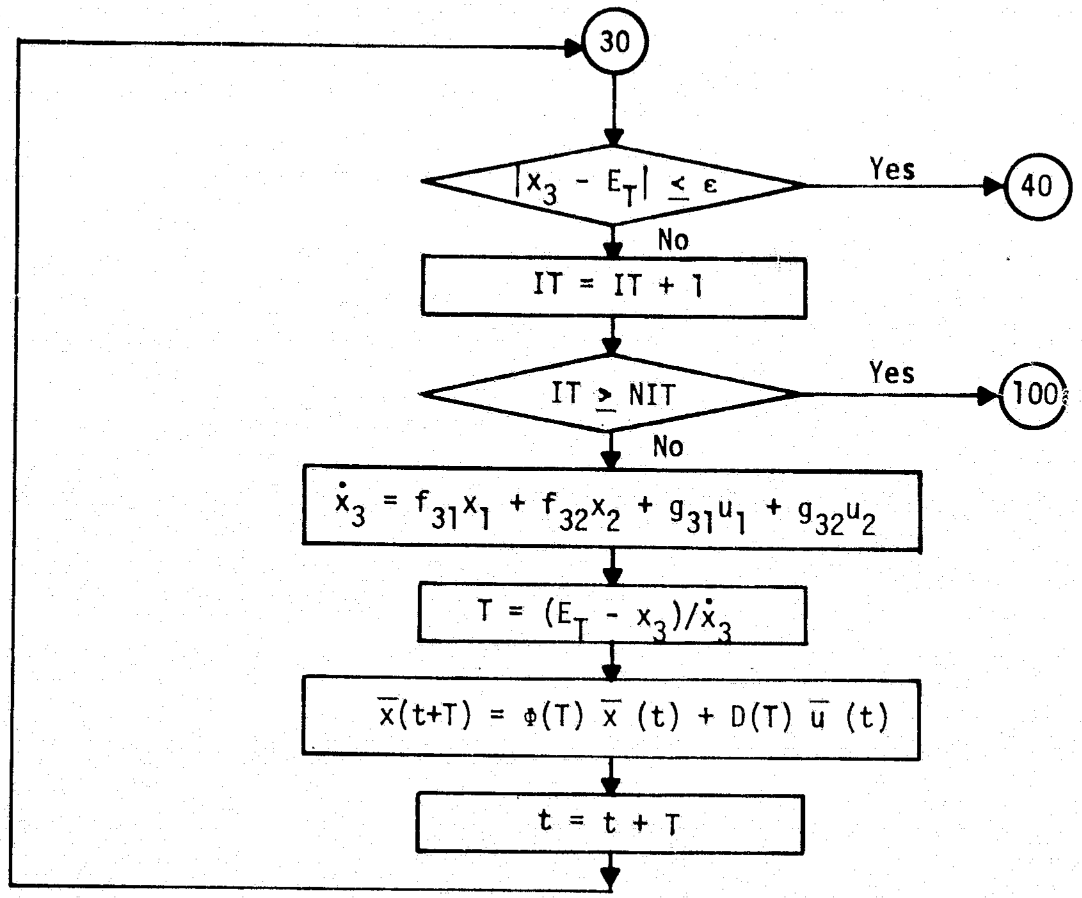
The time period T_1^K is a function of the current system stage $\underline{x}(t_K)$, the threshold condition, or the peak current limitor, or T_{OFF}, min control. The time period T_2^K is a function of the current system state $\underline{x}(t_1^K)$, the inductor current, or the period of oscillation. The time period T_3^K, is a function of T_1^K, T_2^K and the period of oscillation.

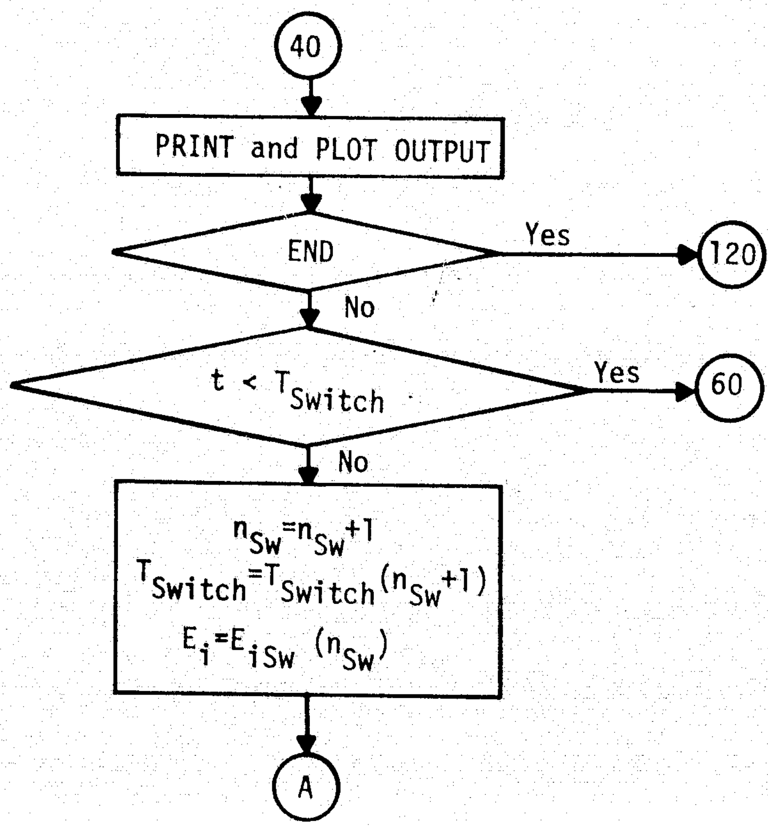
APPENDIX H

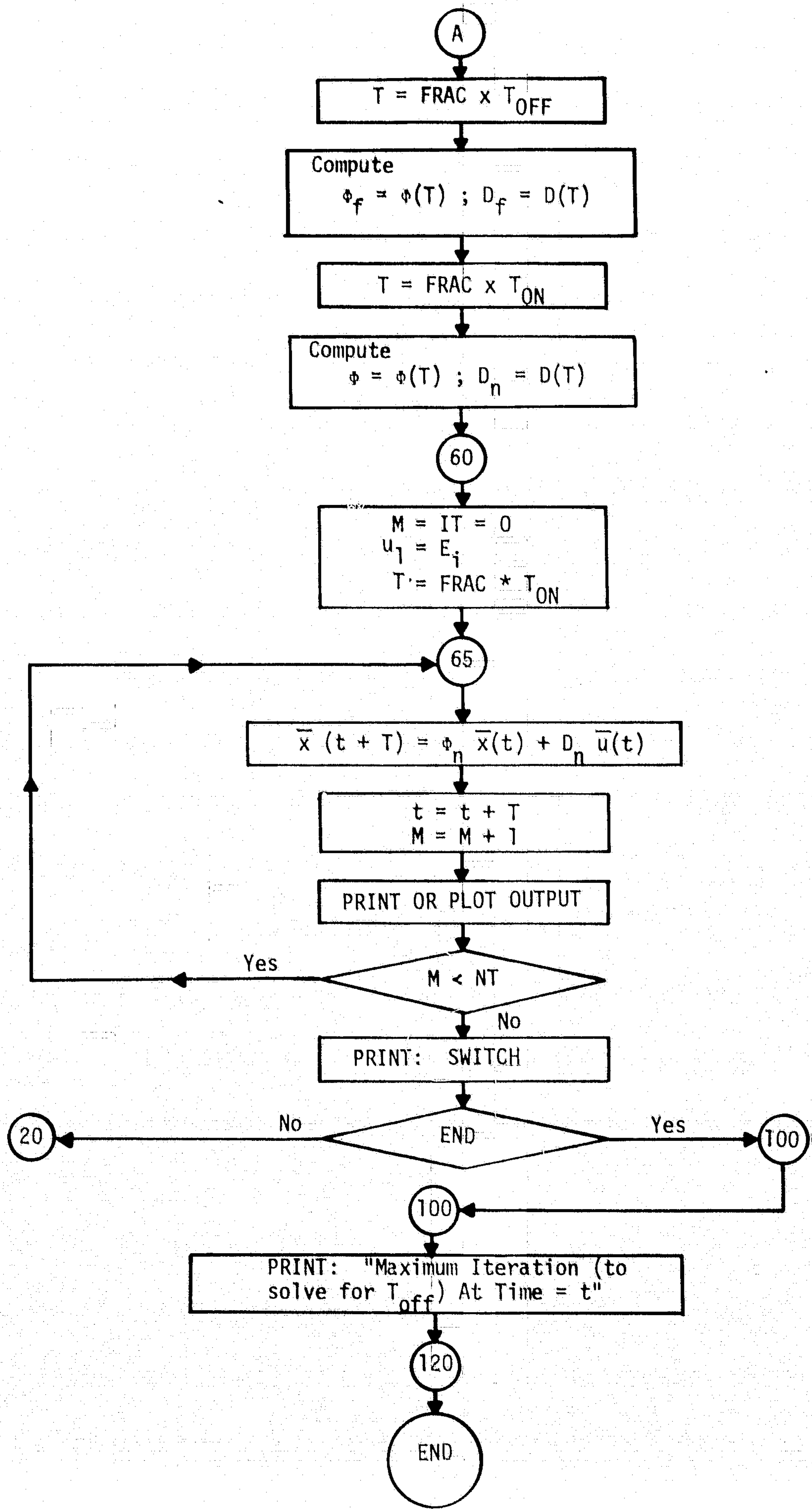
FLOW CHART OF THE SIMULATION PROGRAM




20
$u_1 \triangleq e_i = 0$
Yes
$x_3 < E_T$
No
$T = T_{off-min}$
$\overline{x}(t + T) = \Phi(T)\overline{x}(t) + D(T)\overline{u}(t)$
$t = t + T$
40
$T = FRIC \times T^2_{Off}$
IT = 0
25
$\overline{x}(t + T) = \Phi_f\overline{x}(t) + D_f\overline{u}(t)$
$t = t + T$
$x_3 \geq E_T$
30
No
PRINT and PLOT OUTPUT


30
$|x_3 - E_T| \leq \varepsilon$
Yes
40
No
IT = IT + 1
IT ≥ NIT
Yes
100
No
$\dot{x}_3 = f_{31}x_1 + f_{32}x_2 + g_{31}u_1 + g_{32}u_2$
$T = (E_T - x_3)/\dot{x}_3$
$\overline{x}(t+T) = \Phi(T)\ \overline{x}\ (t) + D(T)\ \overline{u}\ (t)$
t = t + T


40
PRINT and PLOT OUTPUT
END
Yes
120
No
$t < T_{Switch}$
Yes
60
No
$n_{Sw}=n_{Sw}+1$
$T_{Switch}=T_{Switch}(n_{Sw}+1)$
$E_i=E_{iSw}\ (n_{Sw})$
A



A
T = FRAC x T_OFF
Compute
Φ_f = Φ(T) ; D_f = D(T)
T = FRAC x T_ON
Compute
Φ = Φ(T) ; D_n = D(T)
60
M = IT = 0
u_1 = E_i
T = FRAC * T_ON
65
x̄ (t + T) = Φ_n x̄(t) + D_n ū(t)
t = t + T
M = M + 1
PRINT OR PLOT OUTPUT
Yes
M < NT
No
PRINT: SWITCH
20
No
END
Yes
100
100
PRINT: "Maximum Iteration (to
solve for T_off) At Time = t"
120
END

APPENDIX I

IEEE Power Electronics Specialists Conference, NASA Lewis Research Center, Cleveland, Ohio, June 8 - 10, 1976

A GENERAL UNIFIED APPROACH TO MODELLING SWITCHING-CONVERTER POWER STAGES

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ABSTRACT

A method for modelling switching-converter power stages is developed, whose starting point is the unified state-space representation of the switched networks and whose end result is either a complete state-space description or its equivalent small-signal low-frequency linear circuit model.

A new canonical circuit model is proposed, whose fixed topology contains all the essential input-output and control properties of any dc-to-dc switching converter, regardless of its detailed configuration, and by which different converters can be characterized in the form of a table conveniently stored in a computer data bank to provide a useful tool for computer aided design and optimization. The new canonical circuit model predicts that, in general, switching action introduces both zeros and poles into the duty ratio to output transfer function in addition to those from the effective filter network.

1. INTRODUCTION

1.1 Brief Review of Existing Modelling Techniques

In modelling of switching converters in general, and power stages in particular, two main approaches - one based on state-space modelling and the other using an averaging technique - have been developed extensively, but there has been little correlation between them. The first approach remains strictly in the domain of equation manipulations, and hence relies heavily on numerical methods and computerized implementations. Its primary advantage is in the unified description of all power stages regardless of the type (buck, boost, buck-boost or any other variation) through utilization of the exact state-space equations of the two switched models. On the other hand, the approach using an averaging technique is based on equivalent circuit manipulations, resulting in a single equivalent linear circuit model of the power stage. This has the distinct advantage of providing the circuit designer with physical insight into the behaviour of the original switched circuit, and of allowing the powerful tools of linear circuit analysis and synthesis to be used to the fullest extent in design of regulators incorporating switching converters.

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1.2 Proposed New State-Space Averaging Approach

The method proposed in this paper bridges the gap earlier considered to exist between the state-space technique and the averaging technique of modelling power stages by introduction of state-space averaged modelling. At the same time it offers the advantages of both existing methods - the general unified treatment of the state-space approach, as well as an equivalent linear circuit model as its final result. Furthermore, it makes certain generalizations possible, which otherwise could not be achieved.

The proposed state-space averaging method, outlined in the Flowchart of Fig. 1, allows a unified treatment of a large variety of power stages currently used, since the averaging step in the state-space domain is very simple and clearly defined (compare blocks 1a and 2a). It merely consists of averaging the two exact state-space descriptions of the switched models over a single cycle T, where $f_s = 1/T$ is the switching frequency (block 2a). Hence there is no need for special "know-how" in massaging the two switched circuit models into topologically equivalent forms in order to apply circuit-oriented procedure directly, as required in [1] (block 1c). Nevertheless, through a hybrid modelling technique (block 2c), the circuit structure of the averaged circuit model (block 2b) can be readily recognized from the averaged state-space model (block 2a). Hence all the benefits of the previous averaging technique are retained. Even though this outlined process might be preferred, one can proceed from blocks 2a and 2b in two parallel but completely equivalent directions: one following path a strictly in terms of state-space equations, and the other along path b in terms of circuit models. In either case, a perturbation and linearization

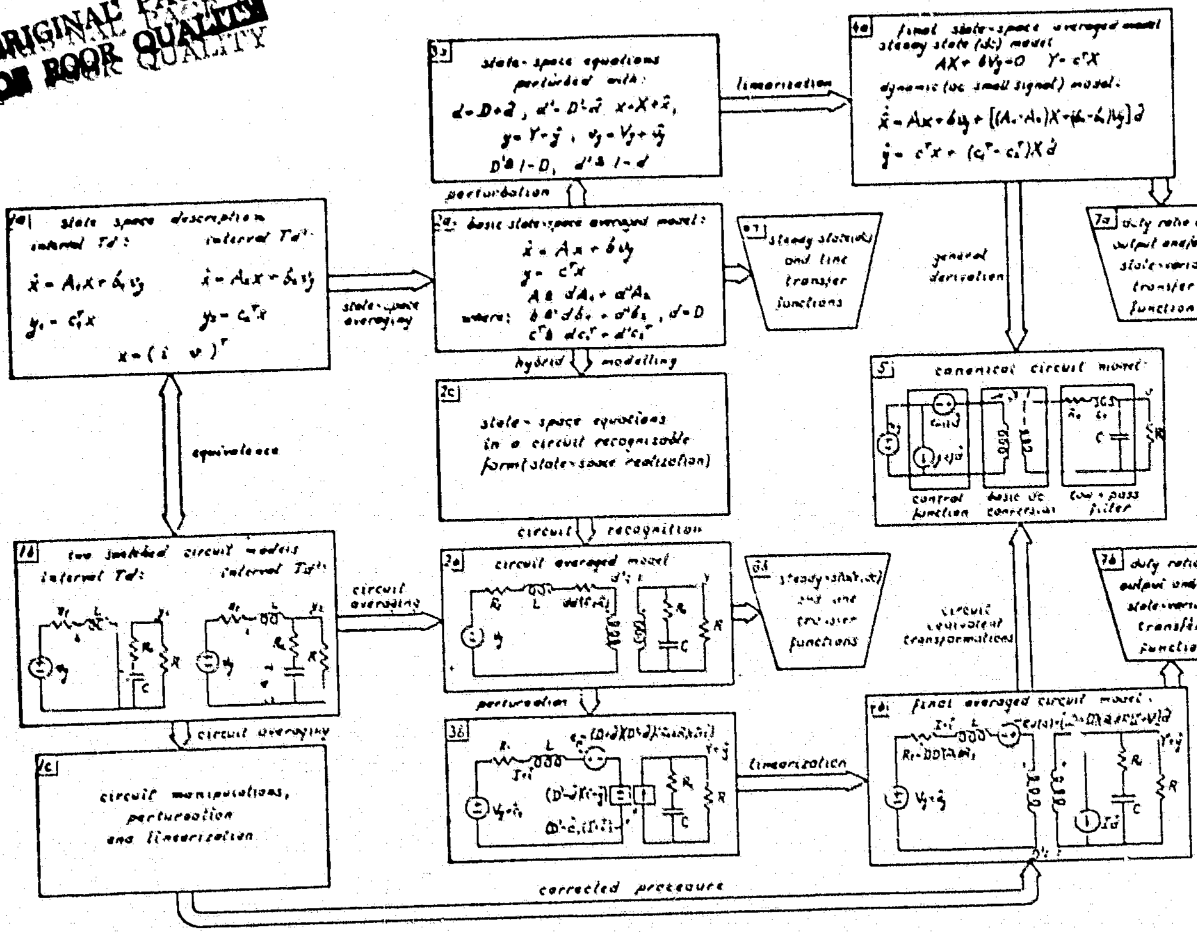

Fig. 1. Flowchart of averaged modelling approaches

process required to include the duty ratio modulation effect proceeds in a very straightforward and formal manner, thus emphasizing the corner-stone character of blocks 2a and 2b. At this stage (block 2a or 2b) the steady-state (dc) and line to output transfer functions are already available, as indicated by blocks 6a and 6b respectively, while the duty ratio to output transfer function is available at the final-stage model (4a or 4b) as indicated by blocks 7a and 7b. The two final stage models (4a and 4b) then give the complete description of the switching converter by inclusion of both independent controls, the line voltage variation and the duty ratio modulation.

Even though the circuit transformation path b might be preferred from the practical design standpoint, the state-space averaging path a is invaluable in reaching some general conclusions about the small-signal low-frequency models of any dc-to-dc switching converter (even those yet to be invented). Whereas, for path b, one has to be presented with the particular circuit in order to proceed with modelling, for path a the final state-space averaged equations (block 4a) give the complete model description through general matrices A_1, A_2 and vectors b_1, b_2, c_1^T, and c_2^T of the two starting switched models (block 1a). This is also why along path b in the Flowchart a particular example of a boost power stage with parasitic effects was chosen, while along path a general equations have been retained. Specifically, for the boost power stage $b_1 = b_2 = b$. This example will be later pursued in detail along both paths.

In addition the state-space averaging approach offers a clear insight into the quantitative nature of the basic averaging approximation, which becomes better the further the effective low-pass filter corner frequency f_c is below the switching frequency f_s, that is, $f_c/f_s \ll 1$. This is, however, shown to be equivalent to the requirement for small output voltage ripple, and hence does not pose any serious restriction or limitation on modelling of practical dc-to-dc converters.

Finally, the state-space averaging approach serves as a basis for derivation of a useful general circuit model that describes the input-output and control properties of any dc-to-dc converter.

1.3 New Canonical Circuit Model

The culmination of any of these derivations along either path a or path b in the Flowchart of Fig. 1 is an equivalent circuit (block 5), valid for small-signal low-frequency variations superimposed upon a dc operating point, that represents the two transfer functions of interest for a switching converter. These are the line voltage to output and duty ratio to output transfer functions.

The equivalent circuit is a canonical model that contains the essential properties of any dc-to-dc switching converter, regardless of the detailed configuration. As seen in block 5 for the general case, the model includes an ideal transformer that describes the basic dc-to-dc transformation ratio from line to output; a low-pass filter whose element values depend upon the dc duty ratio; and a voltage and a current generator proportional to the duty ratio modulation input.

The canonical model in block 5 of the Flowchart can be obtained following either path a or path b, namely from block 4a or 4b, as will be shown later. However, following the general description of the final averaged model in block 4a, certain generalizations about the canonical model are made possible, which are otherwise not achievable. Namely, even though for all currently known switching dc-to-dc converters (such as the buck, boost, buck-boost, Venable [3], Weinberg [4] and a number of others) the frequency dependence appears only in the duty-ratio dependent voltage generator but not in the current generator, and then only as a first-order (single-zero) polynomial in complex frequency s; however, neither circumstance will necessarily occur in some converter yet to be conceived. In general, switching action introduces both zeros and poles into the duty ratio to output transfer function, in addition to the zeros and poles of the effective filter network which essentially constitute the line voltage to output transfer function. Moreover, in general, both duty-ratio dependent generators, voltage and current, are frequency dependent (additional zeros and poles). That in the particular cases of the boost or buck-boost converters this dependence reduces to a first order polynomial results from the fact that the order of the system which is involved in the switching action is only two. Hence from the general result, the order of the polynomial is at most one, though it could reduce to a pure constant, as in the buck or the Venable converter [3].

The significance of the new circuit model is that any switching dc-to-dc converter can be reduced to this canonical fixed topology form, at least as far as its input-output and control properties are concerned, hence it is valuable for comparison of various performance characteristics of different dc-to-dc converters. For example, the effective filter networks could be compared as to their effectiveness throughout the range of dc duty cycle D (in general, the effective filter elements depend on duty ratio D), and the configuration chosen which optimizes the size and weight. Also, comparison of the frequency dependence of the two duty-ratio dependent generators provides insight into the question of stability once a regulator feedback loop is closed.

1.4 Extension to Complete Regulator Treatment

Finally, all the results obtained in modelling the converter or, more accurately, the network which effectively takes part in switching action, can easily be incorporated into more complicated systems containing dc-to-dc converters. For example, by modelling the modulator stage along the same lines, one can obtain a linear circuit model of a closed-loop switching regulator. Standard linear feedback theory can then be used for both analysis and synthesis, stability considerations, and proper design of feedback compensating networks for multiple loop as well as single-loop regulator configurations.

2. STATE-SPACE AVERAGING

In this section the state-space averaging method is developed first in general for any dc-to-dc switching converter, and then demonstrated in detail for the particular case of the boost power stage in which parasitic effects (esr of the capacitor and series resistance of the inductor) are included. General equations for both steady-state (dc) and dynamic performance (ac) are obtained, from which important transfer functions are derived and also applied to the special case of the boost power stage.

2.1 Basic State-Space Averaged Model

The basic dc-to-dc level conversion function of switching converters is achieved by repetitive switching between two linear networks consisting of ideally lossless storage elements, inductances and capacitances. In practice, this function may be obtained by use of transistors and diodes which operate as synchronous switches. On the assumption that the circuit operates in the so-called "continuous conduction" mode in which the instantaneous inductor current does not fall to zero at any point in the cycle, there are only two different "states" of the circuit. Each state, however, can be represented by a linear circuit model (as shown in block 1b of Fig. 1) or by a corresponding set of state-space equations (block 1a). Even though any set of linearly independent variables can be chosen as the state variables, it is customary and convenient in electrical networks to adopt the inductor currents and capacitor voltages. The total number of storage elements thus determines the order of the system. Let us denote such a choice of a vector of state-variables by x.

It then follows that any switching dc-to-dc converter operating in the continuous conduction mode can be described by the state-space equations for the two switched models:

(i) interval Td: (ii) interval Td':

$$\dot{x} = A_1 x + b_1 v_g \qquad \dot{x} = A_2 x + b_2 v_g$$
$$y_1 = c_1^T x \qquad y_2 = c_2^T x \tag{1}$$

where Td denotes the interval when the switch is in the on state and $T(1-d) \equiv Td'$ is the interval for which it is in the off state, as shown in Fig. 2. The static equations $y_1 = c_1^T x$ and $y_2 = c_2^T x$ are necessary in order to account for the case when the output quantity does not

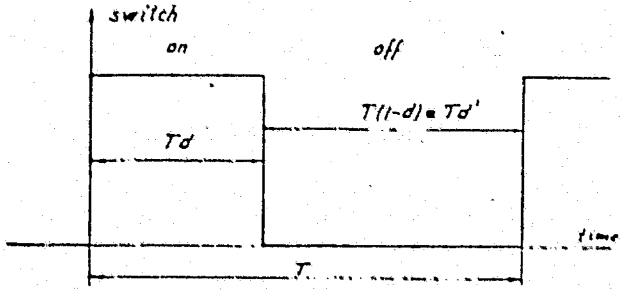

Fig. 2. Definition of the two switched intervals Td and Td'.

coincide with any of the state variables, but is rather a certain linear combination of the state variables.

Our objective now is to replace the state-space description of the two linear circuits emanating from the two successive phases of the switching cycle T by a single state-space description which represents approximately the behaviour of the circuit across the whole period T. We therefore propose the following simple averaging step: take the average of both dynamic and static equations for the two switched intervals (1), by summing the equations for interval Td multiplied by d and the equations for interval Td' multiplied by d'. The following <u>linear continuous system</u> results:

$$\dot{x} = d(A_1 x + b_1 v_g) + d'(A_2 x + b_2 v_g)$$
$$y = dy_1 + d'y_2 = (dc_1^T + d'c_2^T)x \tag{2}$$

After rearranging (2) into the standard linear continuous system state-space description, we obtain the basic averaged state-space description (over a single period T):

$$\dot{x} = (dA_1 + d'A_2)x + (db_1 + d'b_2)v_g$$
$$y = (dc_1^T + d'c_2^T)x \tag{3}$$

This model is the basic averaged model which is the starting model for all other derivations (both state-space and circuit oriented).

Note that in the above equations the duty ratio d is considered constant; it is not a time dependent variable (yet), and particularly not a switched discontinuous variable which changes between 0 and 1 as in [1] and [2], but is merely a fixed number for each cycle. This is evident from the model derivation in Appendix A. In particular, when d = 1 (switch constantly on) the averaged model (3) reduces to switched model (ii), and when d = 0 (switch off) it reduces to switched model (iii).

In essence, comparison between (3) and (1) shows that the system matrix of the averaged model is obtained by taking the average of two switched model matrices A_1 and A_2, its control is the average of two control vectors b_1 and b_2, and its output is the average of two outputs y_1 and y_2 over a period T.

The justification and the nature of the approximation in substitution for the two switched models of (1) by averaged model (3) is indicated in Appendix A and given in more detail in [6]. The basic approximation made, however, is that of approximation of the fundamental matrix $e^{At} = I + At + \cdots$ by its first-order linear term. This is, in turn, shown in Appendix B to be the same approximation necessary to obtain the dc condition independent of the storage element values (L,C) and dependent on the dc duty ratio only. It also coincides with the requirement for low output voltage ripple, which is shown in Appendix C to be equivalent to $f_c/f_s \ll 1$, namely the effective filter corner frequency much lower than the switching frequency.

The model represented by (3) is an averaged model over a single period T. If we now assume that the duty ratio d is constant from cycle to cycle, namely, d = D (steady state dc duty ratio), we get:

$$\dot{x} = Ax + bv_g$$
$$y = c^T x \tag{4}$$

where

$$A = DA_1 + D'A_2$$
$$b = Db_1 + D'b_2 \tag{5}$$
$$c^T = Dc_1^T + D'c_2^T$$

Since (4) is a linear system, superposition holds and it can be perturbed by introduction of line voltage variations $\hat{v}_g$ as $v_g = V_g + \hat{v}_g$, where V_g is the dc line input voltage, causing a corresponding perturbation in the state vector $x = X + \hat{x}$, where again X is the dc value of the state vector and $\hat{x}$ the superimposed ac perturbation. Similarly, $y = Y + \hat{y}$, and

$$\dot{\hat{x}} = AX + bV_g + A\hat{x} + b\hat{v}_g$$
$$Y + \hat{y} = c^T X + c^T \hat{x} \tag{6}$$

Separation of the steady-state (dc) part from the dynamic (ac) part then results in the steady state (dc) model

$$AX + bV_g = 0;\ Y = c^TX \Rightarrow Y = -c^TA^{-1}bV_g \qquad (7)$$

and the dynamic (ac) model

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + b\hat{v}_g \\ \hat{y} &= c^T\hat{x} \end{aligned} \qquad (8).$$

It is interesting to note that in (7) the steady state (dc) vector X will in general only depend on the dc duty ratio D and resistances in the original model, but not on the storage element values (L's and C's). This is so because X is the solution of the linear system of equations

$$AX + bV_g = 0 \qquad (9)$$

in which L's and C's are proportionality constants. This is in complete agreement with the first-order approximation of the exact dc conditions shown in Appendix B, which coincides with expression (7).

From the dynamic (ac) model, the line voltage to state-vector transfer functions can be easily derived as:

$$\begin{aligned} \frac{\hat{x}(s)}{\hat{v}_g(s)} &= (sI-A)^{-1}b \\ \frac{\hat{y}(s)}{\hat{v}_g(s)} &= c^T(sI-A)^{-1}b \end{aligned} \qquad (10)$$

Hence at this stage both steady-state (dc) and line transfer functions are available, as shown by block 6a in the Flowchart of Fig. 1. We now undertake to include the duty ratio modulation effect into the basic averaged model (3).

2.2 Perturbation

Suppose now that the duty ratio changes from cycle to cycle, that is, $d(t) = D + \hat{d}$ where D is the steady-state (dc) duty ratio as before and $\hat{d}$ is a superimposed (ac) variation. With the corresponding perturbation definition $x = X + \hat{x}$, $y = Y + \hat{y}$ and $v_g = V_g + v_g$ the basic model (3) becomes:

$$\dot{\hat{x}} = \underbrace{AX+bV_g}_{\text{dc term}} + \underbrace{A\hat{x}+b\hat{v}_g}_{\text{line variation}} + \underbrace{[(A_1-A_2)X + (b_1-b_2)V_g]\hat{d}}_{\text{duty ratio variation}}$$

$$+ \underbrace{[(A_1-A_2)\hat{x} + (b_1-b_2)\hat{v}_g]\hat{d}}_{\text{nonlinear second-order term}} \qquad (11)$$

$$Y + \hat{y} = \underbrace{c^TX}_{\text{dc term}} + \underbrace{c^T\hat{x}}_{\text{ac term}} + \underbrace{(c_1^T-c_2^T)X\hat{d}}_{\text{ac term}} + \underbrace{(c_1^T-c_2^T)\hat{x}\hat{d}}_{\text{nonlinear term}}$$

The perturbed state-space description is nonlinear owing to the presence of the product of the two time dependent quantities $\hat{x}$ and $\hat{d}$.

2.3 Linearization and Final State-Space Averaged Model

Let us now make the small-signal approximation, namely that departures from the steady state values are negligible compared to the steady state values themselves:

$$\frac{\hat{v}_g}{V_g} \ll 1, \qquad \frac{\hat{d}}{D} \ll 1, \qquad \frac{\hat{x}}{X} \ll 1 \qquad (12)$$

Then, using approximations (12) we neglect all nonlinear terms such as the second-order terms in (11) and obtain once again a linear system, but including duty-ratio modulation $\hat{d}$. After separating steady-state (dc) and dynamic (ac) parts of this linearized system we arrive at the following results for the final state-space averaged model.

Steady-state (dc) model:

$$X = -A^{-1}bV_g; \quad Y = c^TX = -c^TA^{-1}bV_g \qquad (13)$$

Dynamic (ac small-signal) model:

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\hat{d} \\ \hat{y} &= c^T\hat{x} + (c_1^T-c_2^T)X\hat{d} \end{aligned} \qquad (14)$$

In these results, A, b and c^T are given as before by (5).

Equations (13) and (14) represent the small-signal low-frequency model of any two-state switching dc-to-dc converter working in the continuous conduction mode.

It is important to note that by neglect of the nonlinear term in (11) the source of harmonics is effectively removed. Therefore, the linear description (14) is actually a linearized describing function result that is the limit of the describing function as the amplitude of the input signals $\hat{v}_g$ and/or $\hat{d}$ becomes vanishingly small. The significance of this is that the theoretical frequency response obtained from (14) for line to output and duty ratio to output transfer functions can be compared with experimental describing function measurements as explained in [1], [2], or [8] in which small-signal assumption (12) is preserved. Very good agreement up to close to half the switching frequency has been demonstrated repeatedly ([1], [2], [3], [7]).

2.4 Example: Boost Power Stage with Parasitics

We now illustrate the method for the boost power stage shown in Fig. 3.

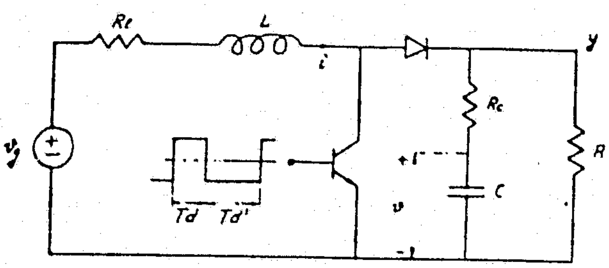

Fig. 3. Example for the state—space averaged modelling: boost power stage with parasitics included.

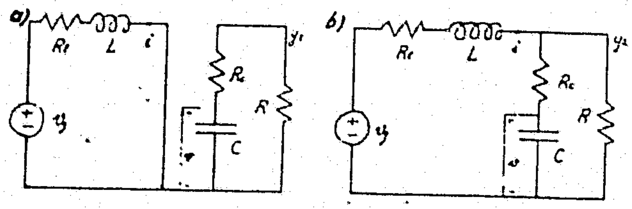

Fig. 4. Two switched circuit models of the circuit in Fig. 3 with assumption of ideal switches. All elements in the final state-space averaged model (13) and (14) are obtained: A_1, b_1, c_1^T from a) for interval Td, and A_2, b_2, c_2^T from b) for interval Td'.

With assumption of ideal switches, the two switched models are as shown in Fig. 4. For choice of state-space vector $x^T = (i\ v)$, the state space equations become:

(i) interval Td: $\dot{x} = A_1 x + b v_g$ $\qquad$ (ii) interval Td': $\dot{x} = A_2 x + b v_g$ $\qquad$ (15)

where $y_1 = c_1^T x$ $\qquad$ $y_2 = c_2^T x$

$$A_1 = \begin{bmatrix} -\frac{R_\ell}{L} & 0 \\ 0 & -\frac{1}{(R+R_c)C} \end{bmatrix} \qquad A_2 = \begin{bmatrix} -\frac{R_\ell + R_c \| R}{L} & -\frac{R}{L(R+R_c)} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix}$$

$$c_1^T = \begin{bmatrix} 0 & \frac{R}{R+R_c} \end{bmatrix} \qquad c_2^T = \begin{bmatrix} R \| R_c & \frac{R}{R+R_c} \end{bmatrix} \tag{16}$$

Note that (15) is the special case of (1) in which $b_1 = b_2 = b = [1/L\ \ 0]^T$.

Using (16) and (5) in the general result (13) and (14), we obtain the following final state-space averaged model.

Steady-state (dc) model:

$$X = \begin{bmatrix} I \\ V \end{bmatrix} = \frac{V_g}{R'} \begin{bmatrix} 1 \\ (1-D)R \end{bmatrix}; \quad Y = \frac{V_g (1-D) R}{R'} \tag{17}$$

in which I is the dc inductor current, V is the dc capacitor voltage, and Y is the dc output voltage.

Dynamic (ac small signal) model:

$$\frac{d}{dt}\begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} = \begin{bmatrix} -\frac{R_\ell + (1-D)(R_c \| R)}{L} & -\frac{(1-D)R}{L(R+R_c)} \\ \frac{(1-D)R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{R}{L}\ \frac{(D'R+R_c)}{R+R_c} \\ -\frac{R}{(R+R_c)C} \end{bmatrix} \frac{V_g}{R'} \hat{d} \tag{18}$$

$$\hat{y} = \begin{bmatrix} (1-D)(R_c \| R) & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} - V_g \frac{R_c \| R}{R'} \hat{d}$$

in which $R' \triangleq (1-D)^2 R + R_\ell + D(1-D)(R_c \| R)$.

We now look more closely at the dc voltage transformation ratio in (17):

$$\frac{V}{V_g} = \frac{Y}{V_g} = \underbrace{\frac{1}{1-D}}_{\text{ideal dc gain}} \ \underbrace{\frac{(1-D)^2 R}{(1-D)^2 R + R_\ell + D(1-D)(R_c \| R)}}_{\text{correction factor}} \tag{19}$$

This shows that the ideal dc voltage gain is 1/D' when all parasitics are zero ($R_\ell = 0$, $R_c = 0$) and that in their presence it is slightly reduced by a correction factor less than 1. Also we observe that nonzero esr of the capacitance ($R_c \neq 0$) (with consequent discontinuity of the output voltage) affects the dc gain and appears effectively as a resistance $R_1 = DD'(R_c \| R)$ in series with the inductor resistance R_ℓ. This effect due to discontinuity of output voltage was not included in [2], but was correctly accounted for in [1].

From the dynamic model (18) one can find the duty ratio to output and line voltage to output transfer functions, which agree exactly with those obtained in [1] by following a different method of averaged model derivation based on the equivalence of circuit topologies of two switched networks.

The fundamental result of this section is the development of the general state-space averaged model represented by (13) and (14), which can be easily used to find the small-signal low-frequency model of any switching dc-to-dc converter. This was demonstrated for a boost power stage with parasitics resulting in the averaged model (17) and (18). It is important to emphasize that, unlike the transfer function description, the state-space description (13) and (14) gives the complete system behaviour. This is very useful in implementing two-loop and multi-loop feedback when two or more states are used in a feedback path to modulate the duty ratio $\hat{d}$. For example, both output voltage and inductor current may be returned in a feedback loop.

3. HYBRID MODELLING

In this section it will be shown that for any specific converter a useful circuit realization of the basic averaged model given by (3) can always be found. Then, in the following section, the perturbation and linearization steps will be carried out on the circuit model finally to arrive at the circuit model equivalent of (13) and (14).

The circuit realization will be demonstrated for the same boost power stage example, for which the basic state-space averaged model (3) becomes:

$$\begin{bmatrix}\frac{di}{dt}\\[4pt] \frac{dv}{dt}\end{bmatrix} = \begin{bmatrix} -\frac{R_\ell + d'(R_c\|R)}{L} & -\frac{d'R}{L(R+R_c)} \\[4pt] \frac{d'R}{(R+R_c)C} & -\frac{1}{(R+R_c)C}\end{bmatrix}\begin{bmatrix} i\\ v\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix} v_g$$

$$y = \begin{bmatrix} d'(R_c\|R) & \frac{R}{R+R_c}\end{bmatrix}\begin{bmatrix} i\\ v\end{bmatrix} \qquad (20)$$

In order to "connect" the circuit, we express the capacitor voltage v in terms of the desired output quantity y as:

$$v = \frac{R+R_c}{R}\, y - (1-d)R_c i$$

or, in matrix form

$$\begin{bmatrix} i\\ v\end{bmatrix} = \begin{bmatrix} 1 & 0\\ d'R_c & \frac{R+R_c}{R}\end{bmatrix}\begin{bmatrix} i\\ y\end{bmatrix} \qquad (21)$$

Substitution of (21) into (20) gives

$$\begin{bmatrix} L\frac{di}{dt}\\[4pt] C\frac{dv}{dt}\end{bmatrix} = \begin{bmatrix} -(R_\ell + \underbrace{dd'(R_c\|R)}_{\text{additional resistance}}) & \underbrace{-d'}_{\text{ideal transformer}}\\[4pt] d' & -\frac{1}{R}\end{bmatrix}\begin{bmatrix} i\\ y\end{bmatrix} + \begin{bmatrix} 1\\ 0\end{bmatrix} v_g \qquad (22)$$

From (22) one can easily reconstruct the circuit representation shown in Fig. 5.

The basic model (22) is valid for the dc regime, and the two dependent generators can be modeled as an ideal d':1 transformer whose range extends down to dc, as shown in Fig. 6.

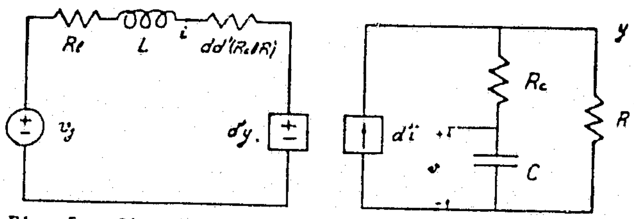

Fig. 5. Circuit realization of the basic state-space averaged model (20) through hybrid modelling.

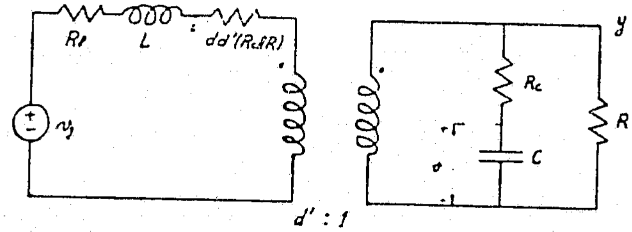

Fig. 6. Basic circuit averaged model for the boost circuit example in Fig. 3. Both dc-to-dc conversion and line variation are modelled when d(t)=D.

As before, we find that the circuit model in Fig. 6 reduces for d = 1 to switched model in Fig. 4a, and for d = 0 to switched model in Fig. 4b. In both cases the additional resistance $R_1 = dd'(R_c\|R)$ disappears, as it should.

If the duty ratio is constant so d = D, the dc regime can be found easily by considering inductance L to be short and capacitance C to be open for dc, and the transformer to have a D':1 ratio. Hence the dc voltage gain (19) can be directly seen from Fig. 6. Similarly, all line transfer functions corresponding to (10) can be easily found from Fig. 6.

It is interesting now to compare this ideal d':1 transformer with the usual ac transformer. While in the latter the turns ratio is fixed, the one employed in our model has a dynamic turns ratio d':1 which changes when the duty ratio is a function of time, d(t). It is through this ideal transformer that the actual controlling function is achieved when the feedback loop is closed. In addition the ideal transformer has a dc transformation ratio d':1, while a real transformer works for ac signals only. Nevertheless, the concept of the ideal transformer in Fig. 6 with such properties is a very useful one, since after all the switching converter has the overall property of a dc-to-dc transformer whose turns ratio can be dynamically adjusted by duty ratio modulation to achieve the controlling function. We will, however, see in the next section how this can be more explicitly modelled in terms of duty-ratio dependent generators only.

Following the procedure outlined in this section one can easily obtain the basic averaged circuit models of three common converter power stages, as shown in the summary of Fig. 7.

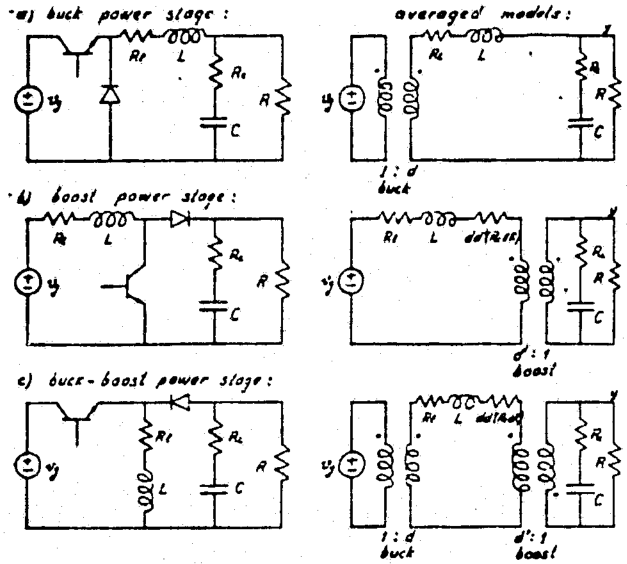

Fig. 7. Summary of basic circuit averaged models for three common power stages: buck, boost, and buck-boost.

The two switched circuit state-space models for the power stages in Fig. 7 are such that the general equations (1) reduce to the special cases $A_1 = A_2 = A$, $b_1 \neq b_2 = 0$ (zero vector) for the buck power stage, and $A_1 \neq A_2$, $b_1 = b_2 = b$ for the boost power stage, whereas for the buck-boost power stage $A_1 \neq A_2$ and $b_1 \neq b_2 = 0$ so that the general case is retained.

4. CIRCUIT AVERAGING

As indicated in the Introduction, in this section the alternative path b in the Flowchart of Fig. 1 will be followed, and equivalence with the previously developed path a firmly established. The final circuit averaged model for the same example of the boost power stage will be arrived at, which is equivalent to its corresponding state-space description given by (17) and (18).

The averaged circuit models shown in Fig. 7 could have been obtained as in [2] by directly averaging the corresponding components of the two switched models. However, even for some simple cases such as the buck-boost or tapped inductor boost [1] this presents some difficulty owing to the requirement of having two switched circuit models topologically equivalent, while there is no such requirement in the outlined procedure.

In this section we proceed with the perturbation and linearization steps applied to the circuit model, continuing with the boost power stage as an example in order to include explicitly the duty ratio modulation effect.

4.1 Perturbation

If the averaged model in Fig. 7b is perturbed according to $v_g = V_g + \hat{v}_g$, $i = I + \hat{i}$, $d = D + \hat{d}$, $d' = D' - \hat{d}$, $v = V + \hat{v}$, $y = Y + \hat{y}$ the nonlinear model in Fig. 8 results.

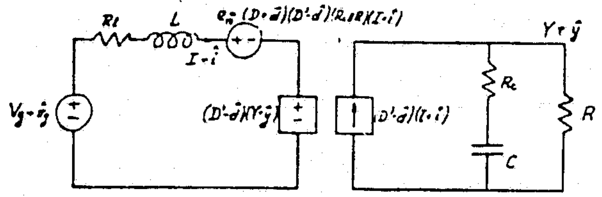

Fig. 8. Perturbation of the basic averaged circuit model in Fig. 6 includes the duty ratio modulation effect $\hat{d}$, but results in this nonlinear circuit model.

4.2 Linearization

Under the small-signal approximation (12), the following linear approximations are obtained:

$$e_n \approx DD'(R_c \| R)(I+\hat{i}) + \hat{d}(D'-D)(R_c \| R)I$$

$$(D'-\hat{d})(Y+\hat{y}) \approx D'(Y+\hat{y}) - \hat{d}Y$$

$$(D'-\hat{d})(I+\hat{i}) \approx D'(I+\hat{i}) - \hat{d}I$$

and the final averaged circuit model of Fig. 9 results. In this circuit model we have finally obtained the controlling function separated in terms of duty ratio $\hat{d}$ dependent generators e_1 and j_1, while the transformer turns ratio is dependent on the dc duty ratio D only. The circuit model obtained in Fig. 9 is equivalent to the state-space description given by (17) and (18).

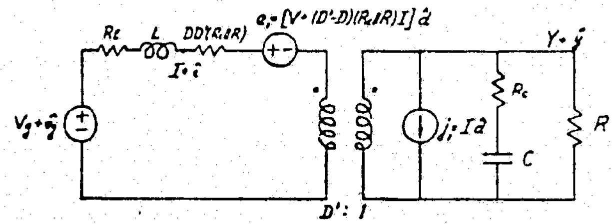

Fig. 9. Under small-signal assumption (12), the model in Fig. 8 is linearized and this final averaged circuit model of the boost stage in Fig. 3 is obtained.

5. THE CANONICAL CIRCUIT MODEL

Even though the general final state-space averaged model in (13) and (14) gives the complete description of the system behaviour, one might still wish to derive a circuit model describing its input-output and control properties as illustrated in Fig. 10.

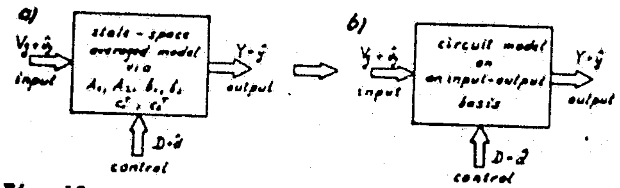

Fig. 10. Definition of the modelling objective: circuit averaged model describing input-output and control properties.

In going from the model of Fig. 10a to that of Fig. 10b some information about the internal behaviour of some of the states will certainly be lost but, on the other hand, important advantages will be gained as were briefly outlined in the Introduction, and as this section will illustrate.

We propose the following fixed topology circuit model, shown in Fig. 11, as a realization

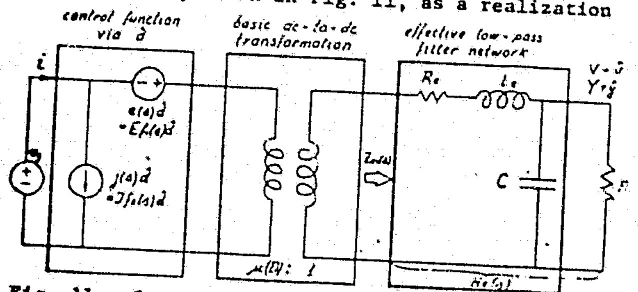

Fig. 11. Canonical circuit model realization of the "black box" in Fig. 10b, modelling the three essential functions of any dc-to-dc converter: control, basic dc conversion, and low-pass filtering.

of the "black box" in Fig. 10b. We call this model the canonical circuit model, because any switching converter input-output model, regardless of its detailed configuration, could be represented in this form. Different converters are represented simply by an appropriate set of formulas for the four elements $e(s)$, $j(s)$, μ, $H_e(s)$ in the general equivalent circuit. The polarity of the ideal μ:1 transformer is determined by whether or not the power stage is polarity inverting. Its turns ratio μ is dependent on the dc duty ratio D, and since for modelling purposes the transformer is assumed to operate down to dc, it provides the basic dc-to-dc level conversion. The single-section low-pass L_eC filter is shown in Fig. 11 only for illustration purposes, because the actual number and configuration of the L's and C's in the effective filter transfer function realization depends on the number of storage elements in the original converter.

The resistance R_e is included in the model of Fig. 11 to represent the damping properties of the effective low-pass filter. It is an "effective" resistance that accounts for various series ohmic resistances in the actual circuit (such as R_ℓ in the boost circuit example), the additional "switching" resistances due to discontinuity of the output voltage (such as $R_1 = DD'(R_c \| R)$ in the boost circuit example), and also a "modulation" resistance that arises from a modulation of the switching transistor storage time [1].

5.1 Derivation of the Canonical Model through State-Space

From the general state-space averaged model (13) and (14), we obtain directly using the Laplace transform:

$$\hat{x}(s)=(sI-A)^{-1}\hat{v}_g(s)+(sI-A)^{-1}[(A_1-A_2)X+(b_1-b_2)V_g]\hat{d}(s)$$

$$\hat{y}(s)=c^T\hat{x}(s)+(c_1{}^T-c_2{}^T)X\hat{d}(s) \tag{23}$$

Now, from the complete set of transfer functions we single out those which describe the converter input-output properties, namely

$$\begin{aligned}\hat{y}(s) &= G_{vg}\,\hat{v}_g(s) + G_{vd}\,\hat{d}(s)\\ \hat{i}(s) &= G_{ig}\,\hat{v}_g(s) + G_{id}\,\hat{d}(s)\end{aligned} \tag{24}$$

in which the G's are known explicitly in terms of the matrix and vector elements in (23).

Equations (24) are analogous to the two-port network representation of the terminal properties of the network (output voltage $y(s)$ and input current $\hat{i}(s)$). The subscripts designate the corresponding transfer functions. For example G_{vg} is the source voltage $\hat{v}_g$ to output voltage $\hat{y}$ transfer function, G_{id} is the duty ratio $\hat{d}$ to input current $\hat{i}(s)$ transfer function, and so on.

For the proposed canonical circuit model in Fig. 11, we directly get:

$$\begin{aligned}\hat{y}(s) &= (\hat{v}_g+e\hat{d})\,\frac{1}{\mu}\,H_e(s)\\ \hat{i}(s) &= j\,\hat{d} + (e\hat{d}+\hat{v}_g)\,\frac{1}{\mu^2 Z_{ei}(s)}\end{aligned} \tag{25}$$

or, after rearrangement into the form of (24):

$$\begin{aligned}\hat{y}(s) &= \frac{1}{\mu}H_e(s)\,\hat{v}_g(s) + e\,\frac{1}{\mu}H_e(s)\hat{d}(s)\\ \hat{i}(s) &= \frac{1}{\mu^2 Z_{ei}(s)}\,\hat{v}_g(s) + \left[j + \frac{e}{\mu^2 Z_{ei}(s)}\right]\hat{d}(s)\end{aligned} \tag{26}$$

Direct comparison of (24) and (26) provides the solutions for $H_e(s)$, $e(s)$, and $j(s)$ in terms of the known transfer functions G_{vg}, G_{vd}, G_{ig} and G_{id} as:

$$e(s) = \frac{G_{vd}(s)}{G_{vg}(s)}, \qquad j(s) = G_{id}(s) - e(s)G_{ig}(s) \tag{27}$$

$$H_e(s) = \mu G_{vg}(s)$$

Note that in (27) the parameter $1/\mu$ represents the ideal dc voltage gain when all the parasitics are zero. For the previous boost power stage example, from (19) we get $\mu = 1\text{-}D$ and the correction factor in (19) is then associated with the effective filter network $H_e(s)$. However, μ could be found from

$$\frac{Y}{V_g} = -c^T A^{-1} b = \frac{1}{\mu} \times (\text{correction factor}) \qquad (28)$$

by setting all parasitics to zero and reducing the correction factor to 1.

The physical significance of the ideal dc gain μ is that it arises as a consequence of the switching action, so it cannot be associated with the effective filter network which at dc has a gain (actually attenuation) equal to the correction factor.

The procedure for finding the four elements in the canonical model of Fig. 11 is now briefly reviewed. First, from (28) the basic dc-to-dc conversion factor μ is found as a function of dc duty ratio D. Next, from the set of all transfer functions (23) only those defined by (24) are actually calculated. Then, by use of these four transfer functions G_{vd}, G_{vg}, G_{id}, G_{ig} in (27) the frequency dependent generators $e(s)$ and $j(s)$ as well as the low-pass filter transfer function $H_e(s)$ are obtained.

The two generators could be further put into the form

$$e(s) = E f_1(s)$$

$$j(s) = J f_2(s)$$

where $f_1(0) = f_2(0) = 1$, such that the parameters E and J could be identified as dc gains of the frequency dependent functions $e(s)$ and $j(s)$.

Finally, a general synthesis procedure [10] for realization of L,C transfer functions terminated in a single load R could be used to obtain a low-pass ladder-network circuit realization of the effective low-pass network $H_e(s)$. Though for the second-order example of $H_e(s)$ this step is trivial and could be done by inspection, for higher-order transfer functions the orderly procedure of the synthesis [10] is almost mandatory.

5.2 Example: Ideal Buck-boost Power Stage

For the buck-boost circuit shown in Fig. 7c with $R_\ell = 0$, $R_c = 0$, the final state-space averaged model is:

$$\begin{bmatrix} \dfrac{d\hat{i}}{dt} \\ \\ \dfrac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{D'}{L} \\ \\ \dfrac{D'}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \dfrac{D}{L} \\ \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \dfrac{V_g - V}{L} \\ \\ \dfrac{-V}{D'RC} \end{bmatrix} \hat{d} \qquad (29)$$

in which the output voltage $\hat{y}$ coincides with the state-variable capacitance voltage $\hat{v}$.

From (28) and (29) one obtains $\mu = D'/D$. With use of (29) to derive transfer functions, and upon substitution into (27), there results

$$e(s) = \frac{-V}{D^2}\left(1 - s\frac{DL}{D'^2R}\right), \quad j(s) = \frac{-V}{(1-D)^2R}$$

$$H_e(s) = \frac{1}{1 + s/RC + s^2 L_e C}, \quad \mu = \frac{1-D}{D} \qquad (30)$$

in which V is the dc output voltage.

The effective filter transfer function is easily seen as a low-pass LC filter with $L_e = L/D'^2$ and with load R. The two generators in the canonical model of Fig. 11 are identified by

$$E = \frac{-V}{D^2}, \qquad f_1(s) \equiv 1 - s\frac{DL}{D'^2R}$$

$$J = \frac{-V}{(1-D)^2R}, \qquad f_2(s) \equiv 1 \qquad (31)$$

We now derive the same model but this time using the equivalent circuit transformations and path b in the Flowchart of Fig. 1.

After perturbation and linearization of the circuit averaged model in Fig. 7c (with $R_\ell = 0$, $R_c = 0$) the series of equivalent circuits of Fig. 12 is obtained.

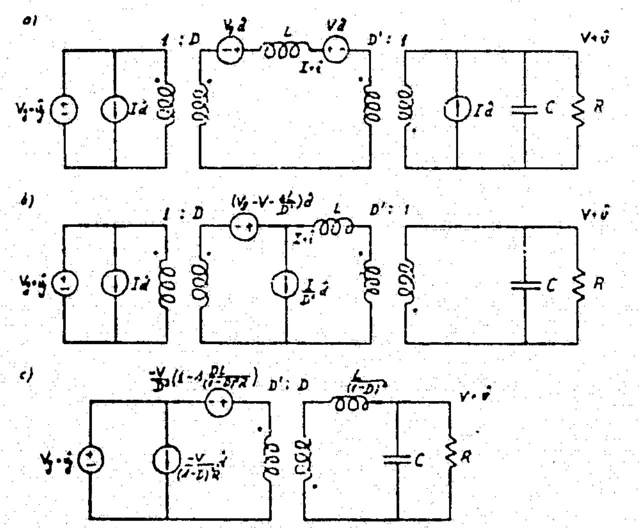

Fig. 12. Equivalent circuit transformations of the final circuit averaged model (a), leading to its canonical circuit realization (c) demonstrated on the buck-boost example of Fig. 7c (with $R_\ell = 0$, $R_c = 0$).

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The objective of the transformations is to reduce the original four duty-ratio dependent generators in Fig. 12a to just two generators (voltage and current) in Fig. 12c which are at the input port of the model. As these circuit transformations unfold, one sees how the frequency dependence in the generators arises naturally, as in Fig. 12b. Also, by transfer of the two generators in Fig. 12b from the secondary to the primary of the 1:D transformer, and the inductance L to the secondary of the D':1 transformer, the cascade of two ideal transformers is reduced to the single transformer with equivalent turns ratio D':D. At the same time the effective filter network L_e, C, R is generated.

Expressions for the elements in the canonical equivalent circuit can be found in a similar way for any converter configuration. Results for the three familiar converters, the buck, boost, and buck-boost power stages are summarized in Table I.

	$\mu(D)$	E	$f(s)$	J	$j(s)$	L_e
buck	$\frac{1}{D}$	$\frac{V}{D^2}$	1	$\frac{V}{R}$	1	L
boost	$1-D$	V	$1-s\frac{L_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$
buck-boost	$\frac{1-D}{D}$	$\frac{-V}{D^2}$	$1-s\frac{DL_e}{R}$	$\frac{-V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$

Table I Definition of the elements in the canonical circuit model of Fi.. 11 for the three common power stages of Fig. 7.

It may be noted in Table I that, for the buck-boost power stage, parameters E and J have negative signs, namely $E = -V/D^2$ and $J = -V/(D'^2R)$. However, as seen from the polarity of the ideal D':D transformer in Fig. 12c this stage is an inverting one. Hence, for positive input dc voltage V_g, the output dc voltage V is negative ($V < 0$) since $V/V_g = -D/D'$. Therefore $E > 0$, $J > 0$ and consequently the polarity of the voltage and current duty-ratio dependent generators is not changed but is as shown in Fig. 12c. Moreover, this is true in general: regardless of any inversion property of the power stage, the polarity of two generators stays the same as in Fig. 11.

5.3 Significance of the Canonical Circuit Model and Related Generalizations

The canonical circuit model of Fig. 11 incorporates all three basic properties of a dc-to-dc converter: the dc-to-dc conversion function (represented by the ideal μ:1 transformer); control (via duty ratio $\hat{d}$ dependent generators); and low-pass filtering (represented by the effective low-pass filter network $H_e(s)$). Note also that the current generator $j(s)\,\hat{d}$ in the canonical circuit model, even though superfluous when the source voltage $v_g(s)$ is ideal, is necessary to reflect the influence of a nonideal source generator (with some internal impedance) or of an input filter [7] upon the behaviour of the converter. Its presence enables one easily to include the linearized circuit model of a switching converter power stage in other linear circuits, as the next section will illustrate.

Another significant feature of the canonical circuit model is that any switching dc-to-dc converter can be reduced by use of (23), (24), (27) and (28) to this fixed topology form, at least as far as its input-output and control properties are concerned. Hence the possibility arises for use of this model to compare in an easy and unique way various performance characteristics of different converters. Some examples of such comparisons are given below.

1. The filter networks can be compared with respect to their effectiveness throughout the dynamic duty cycle D range, because in general the effective filter elements depend on the steady state duty ratio D. Thus, one has the opportunity to choose the configuration and to optimize the size and weight.

2. Basic dc-to-dc conversion factors $\mu_1(D)$ and $\mu_2(D)$ can be compared as to their effective range. For some converters, traversal of the range of duty ratio D from 0 to 1 generates any conversion ratio (as in the ideal buck-boost converter), while in others the conversion ratio might be restricted (as in the Weinberg converter [4], for which $\frac{1}{2}\leq\mu<1$).

3. In the control section of the canonical model one can compare the frequency dependences of the generators e(s) and j(s) for different converters and select the configuration that best facilitates stabilization of a feedback regulator. For example, in the buck-boost converter e(s) is a polynomial, containing actually a real zero in the right half-plane, which undoubtedly causes some stability problems and need for proper compensation.

4. Finally, the canonical model affords a very convenient means to store and file information on various dc-to-dc converters in a computer memory in a form comparable to Table I. Then, thanks to the fixed topology of the canonical circuit model, a single computer program can be used to calculate and plot various quantities as functions of frequency (input and output impedance, audio susceptibility, duty ratio to output transfer response, and so on). Also, various input filters and/or additional output filter networks can easily be added if desired.

We now discuss an important issue which has been intentionally skipped so far. From (27) it is concluded that in general the duty ratio dependent generators e(s) and j(s) are rational functions of complex frequency s. Hence, in general both some new zeros and poles are introduced into the duty ratio to output transfer function owing to the switching action, in addition to the poles and zeros of the effective filter network (or line to output transfer function). However, in special cases, as in all those shown in Table I, the frequency dependence might reduce simply to polynomials, and even further it might show up only in the voltage dependent generators (as in the boost, or buck-boost) and reduce to a constant ($f_2(s) \equiv 1$) for the current generator. Nevertheless, this does not prevent us from modifying any of these circuits in a way that would exhibit the general result -- introduction of both additional zeros as well as poles.

Let us now illustrate this general result on a simple modification of the familiar boost circuit, with a resonant L_1,C_1 circuit in series with the input inductance L, as shown in Fig. 13.

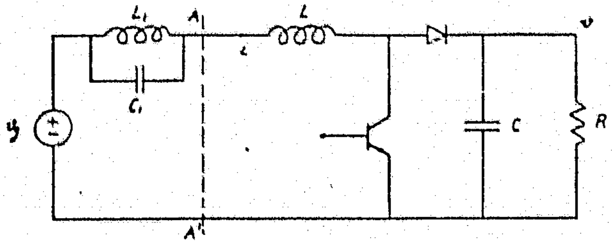

Fig. 13. Modified boost circuit as an illustration of general frequency behaviour of the generators in the canonical circuit model of Fig. 11.

By introduction of the canonical circuit model for the boost power stage (for the circuit to the right of cross section AA') and use of data from Table I, the equivalent averaged circuit model of Fig. 14a is obtained. Then, by application of the equivalent circuit transformation as outlined previously, the averaged model in the canonical circuit form is obtained in Fig. 14b. As can be seen from Fig. 14b, the voltage generator has a double pole at the resonant frequency $\omega_r = 1/\sqrt{L_1C_1}$ of the parallel L_1,C_1 network. However, the effective filter transfer function has a double zero (null in magnitude) at precisely the same location such that the two

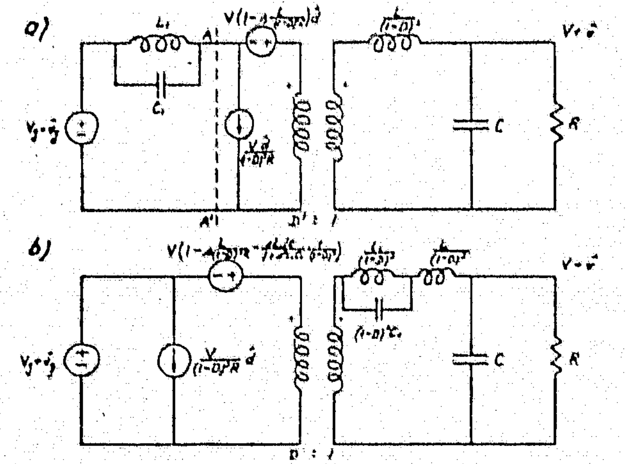

Fig. 14. Equivalent circuit transformation leading to the canonical circuit model (b) of the circuit in Fig. 13.

pairs effectively cancel. Hence, the resonant null in the magnitude response, while present in the line voltage to output transfer function, is not seen in the duty ratio-to output transfer function. Therefore, the positive effect of rejection of certain input frequencies around the resonant frequency ω_r is not accompanied by a detrimental effect on the loop gain, which <u>will not</u> contain a null in the magnitude response.

This example demonstrates yet another important aspect of modelling with use of the averaging technique. Instead of applying it directly to the whole circuit in Fig. 13, we have instead implemented it only with respect to the storage element network which effectively takes part in the switching action, namely L, C, and R. Upon substitution of the switched part of the network by the averaged circuit model, all other linear circuits of the complete model are retained as they appear in the original circuit (such as L_1,C_1 in Fig. 14a). Again, the current generator in Fig. 14a is the one which reflects the effect of the input resonant circuit.

In the next section, the same property is clearly displayed for a closed-loop regulator-converter with or without the input filter.

6. SWITCHING MODE REGULATOR MODELLING

This section demonstrates the ease with which the different converter circuit models developed in previous sections can be incorporated into more complicated systems such as a switching-mode regulator. In addition, a brief discussion of modelling of modulator stages in general is included, and a complete general switching-mode regulator circuit model is given.

A general representation of a switching-mode regulator is shown in Fig. 15. For concreteness, the switching-mode converter is represented by a buck-boost power stage, and the input and possible additional output filter are represented by a

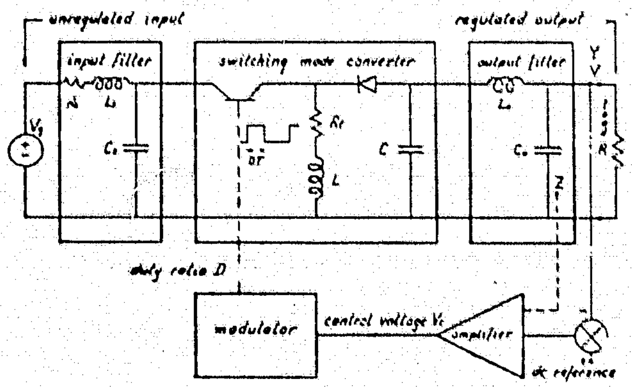

Fig. 15. General switching-mode regulator with input and output filters. The block diagram is general, and single-section LC filters and a buck-boost converter are shown as typical realizations.

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single-section low-pass LC configuration, but the discussion applies to any converter and any filter configuration.

The main difficulty in analysing the switching mode regulator lies in the modelling of its nonlinear part, the switching-mode converter. However, we have succeeded in previous sections in obtaining the small-signal low-frequency circuit model of any "two-state" switching dc-to-dc converter, operating in the continuous conduction mode, in the canonical circuit form. The output filter is shown separately, to emphasize the fact that in averaged modelling of the switching-mode converter only the storage elements which are actually involved in the switching action need be taken into account, thus minimizing the effort in its modelling.

The next step in development of the regulator equivalent circuit is to obtain a model for the modulator. This is easily done by writing an expression for the essential function of the modulator, which is to convert an (analog) control voltage V_c to the switch duty ratio D. This expression can be written $D = V_c/V_m$ in which, by definition, V_m is the range of control signal required to sweep the duty ratio over its full range from 0 to 1. A small variation v_c superimposed upon V_c therefore produces a corresponding variation $\hat{d} = \hat{v}_c/V_m$ in D, which can be generalized to account for a nonuniform frequency response as

$$\hat{d} = \frac{f_m(s)}{V_m} \hat{v}_c \qquad (32)$$

in which $f_m(0) = 1$. Thus, the control voltage to duty ratio small-signal transmission characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved. Hence, by substitution for $\hat{d}$ from (32) the two generators in the canonical circuit model of the switching converter can be expressed in terms of the ac control voltage $\hat{v}_c$, and the resulting model is then a linear ac equivalent circuit that represents the small-signal transfer properties of the nonlinear processes in the modulator and converter.

It remains simply to add the linear amplifier and the input and output filters to obtain the ac equivalent circuit of the complete closed-loop regulator as shown in Fig. 16.

The modulator transfer function has been incorporated in the generator designations, and the generator symbol has been changed from a circle to a square to emphasize the fact that, in the closed-loop regulator, the generators no longer are independent but are dependent on another signal in the same system. The connection from point Y to the error amplifier, via the reference voltage summing node, represents the basic voltage feedback necessary to establish the system as a voltage regulator. The dashed connection from point Z indicates a possible additional feedback sensing; this second feedback signal may

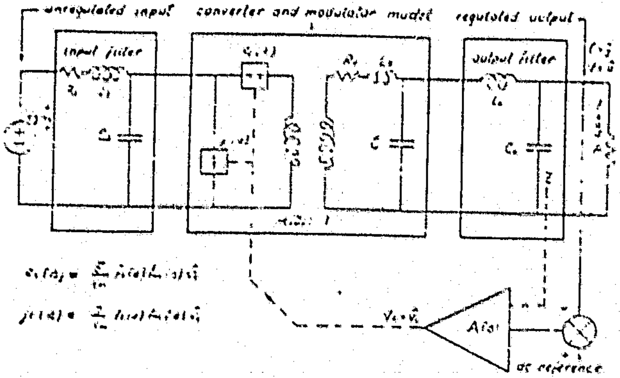

Fig. 16. General small-signal ac equivalent circuit for the switching-mode regulator of Fig. 15.

be derived, for example, from the inductor flux, inductor current, or capacitor current, as in various "two-loop" configurations that are in use [9].

Once again the current generator in Fig. 16 is responsible for the interaction between the switching-mode regulator-converter and the input filter, thus causing performance degradation and/or stability problems when an arbitrary input filter is added. The problem of how properly to design the input filter is treated in detail in [7].

As shown in Fig. 16 we have succeeded in obtaining the linear circuit model of the complete switching mode-regulator. Hence the well-known body of linear feedback theory can be used for both analysis and design of this type of regulator.

7. CONCLUSIONS

A general method for modelling power stages of any switching dc-to-dc converter has been developed through the state-space approach. The fundamental step is in replacement of the state-space descriptions of the two switched networks by their average over the single switching period T, which results in a single continuous state-space equation description (3) designated the basic averaged state-space model. The essential approximations made are indicated in the Appendices, and are shown to be justified for any practical dc-to-dc switching converter.

The subsequent perturbation and linearization step under the small-signal assumption (12) leads to the final state-space averaged model given by (13) and (14). These equations then serve as the basis for development of the most important qualitative result of this work, the canonical circuit model of Fig. 11. Different converters are represented simply by an appropriate set of formulas ((27) and (28)) for four elements in this general equivalent circuit. Besides its unified description, of which several examples are given in Table I, one of the advantages of the canonical circuit model is that various performance characteristics of different switching converters can be compared in a quick and easy manner.

Although the state-space modelling approach has been developed in this paper for two-state switching converters, the method can be extended to multiple-state converters. Examples of three-state converters are the familiar buck, boost, and buck-boost power stages operated in the discontinuous conduction mode, and dc-to-ac switching inverters in which a specific output waveform is "assembled" from discrete segments are examples of multiple-state converters.

In contrast with the state-space modelling approach, for any particular converter an alternative path via hybrid modelling and circuit transformation could be followed, which also arrives first at the final circuit averaged model equivalent of (13) and (14) and finally, after equivalent circuit transformations, again arrives at the canonical circuit model.

Regardless of the derivation path, the canonical circuit model can easily be incorporated into an equivalent circuit model of a complete switching regulator, as illustrated in Fig. 16.

Perhaps the most important consequence of the canonical circuit model derivation via the general state-space averaged model (13), (14), (23) and (24) is its prediction through (27) of additional zeros as well as poles in the duty ratio to output transfer function. In addition frequency dependence is anticipated in the duty ratio dependent current generator of Fig. 11, even though for particular converters considered in Table I, it reduces merely to a constant. Furthermore for some switching networks which would effectively involve more than two storage elements, higher order polynomials should be expected in $f_1(s)$ and/or $f_2(s)$ of Fig. 11.

The insights that have emerged from the general state-space modelling approach suggest that there is a whole field of new switching dc-to-dc converter power stages yet to be conceived. This encourages a renewed search for innovative circuit designs in a field which is yet young, and promises to yield a significant number of inventions in the stream of its full development. This progress will naturally be fully supported by new technologies coming at an ever increasing pace. However, even though the efficiency and performance of currently existing converters will increase through better, faster transistors, more ideal capacitors (with lower esr) and so on, it will be primarily the responsibility of the circuit designer and inventor to put these components to best use in an optimal topology. Search for new circuit configurations, and how best to use present and future technologies, will be of prime importance in achieving the ultimate goal of near-ideal general switching dc-to-dc converters.

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APPENDICES

In this sequence of Appendices several of the questions related to substitution of the two switched models (1) by the state-space description (3) are discussed.

In Appendix A it is briefly indicated for a simplified autonomous example how the correlation between the state-space averaging step and the linear approximation of the fundamental matrix is established. In Appendix B the exact dc conditions, which are generally dependent on the storage element values, are shown to reduce under the same linear approximation to those obtained from (7). In Appendix C it is demonstrated both analytically and quantitatively (numerically), for a typical set of parameter values for a boost power stage, that the linear approximation of the fundamental matrix is equivalent to $f_c \ll f_s$, where f_c is the effective corner frequency of the low-pass filter and f_s is the switching frequency. This inequality is in turn connected with the condition for low output voltage ripple, and hence does not impose any significant restriction on the outlined modelling procedure.

APPENDIX A

The fundamental approximation in the state-space averaging approach

Let the two linear systems be described by

i) interval Td, $0<t<t_o$: ii) interval Td', $t_o<t<T$:

$$\dot{x} = A_1 x \qquad\qquad \dot{x} = A_2 x \tag{33}$$

The exact solutions of these state-space equations are:

$$\begin{aligned} x(t) &= e^{A_1 t} x(0), & t \in [0,t_o] \\ x(t) &= e^{A_2 (t-t_o)} x(t_o), & t \in [t_o,T] \end{aligned} \tag{34}$$

The state-variable vector $x(t)$ is continuous across the switching instant t_o, and so:

$$x(T) = e^{A_2 (T-Td)} x(t_o) = e^{d'A_2 T} e^{dA_1 T} x(0) \tag{35}$$

Suppose that the following approximation is now introduced into (35):

$$e^{d'A_2 T} e^{dA_1 T} \approx e^{(dA_1+d'A_2)T} \tag{36}$$

resulting in an approximate solution

$$x(T) \approx e^{(dA_1+d'A_2)T} x(0) \tag{37}$$

However, this is the same as the solution of the following linear system equation for $x(T)$:

$$\dot{x} = (dA_1+d'A_2)x \tag{38}$$

The last model (38) is, therefore, the averaged model obtained from the two switched models given by (33) and is valid provided approximation (36) is well satisfied. This is so if the following linear approximations of the fundamental matrices hold:

$$\begin{aligned} e^{dA_1 T} &\approx I + dA_1 T \\ e^{d'A_2 T} &\approx I + d'A_2 T \end{aligned} \tag{39}$$

In essence, (36) is the first approximation to the more general result Baker-Campbell-Hausdorff series [5]:

$$AT = (dA_1+d'A_2)T + dd'(A_1A_2-A_2A_1)T^2 + \cdots \tag{40}$$

where

$$e^{AT} = e^{d'A_2 T} e^{dA_1 T} \tag{41}$$

Hence, when two matrices are commutative, that is $A_1A_2 = A_2A_1$, then $A = dA_1 + d'A_2$ and (36) becomes an exact result.

APPENDIX B

Derivation of the exact dc conditions and their simplification under linear approximation of the fundamental matrices

We now derive the exact steady-state (dc) condition from the general state-space description of the two switched circuit models. Let $x = x_1$ be the state-variable vector for interval TD $(0<t<t_o)$ and $x = x_2$ that for interval TD' $(t_o<t<T)$.

i) interval TD, $(0<t<t_o)$: ii) interval TD' $(t_o<t<T)$:

$$\dot{x}_1 = A_1 x + bv_g \qquad\qquad \dot{x}_2 = A_2 x + bv_g \tag{42}$$

The respective solutions are:

$$\begin{aligned} x_1(t) &= e^{A_1 t} x_1(0) + V_g B_1(t) b \\ x_2(t) &= e^{A_2 t} x_2(t_o) + V_g B_2(t-t_o) b \end{aligned} \tag{43}$$

where

$$B_i(t) = \int_0^t e^{A_i \tau} d\tau = A_i^{-1}(e^{A_i t} - I) \quad \text{for } i = 1,2 \tag{44}$$

provided inverse matrices A_1^{-1}, A_2^{-1} exist.

Solutions (43) contain two yet undetermined constants, $x_1(0)$ and $x_2(t_o)$. We therefore impose two boundary conditions:

a) the vector of state variables is continuous across the switching instant t_o, since the inductor currents and capacitor voltages cannot change instantaneously. Hence

$$x_1(t_o) = x_2(t_o) \tag{45}$$

b) from the steady state requirement, all the state variables should return after period T to their initial values. Hence:

$$x_1(0) = x_2(T) \tag{46}$$

The boundary conditions (45) and (46) are illustrated in Fig. 17, where $v(0) = v(T)$, $i(0) = i(T)$ and $i(t)$ and $v(t)$ are continuous across the switching instant t_o.

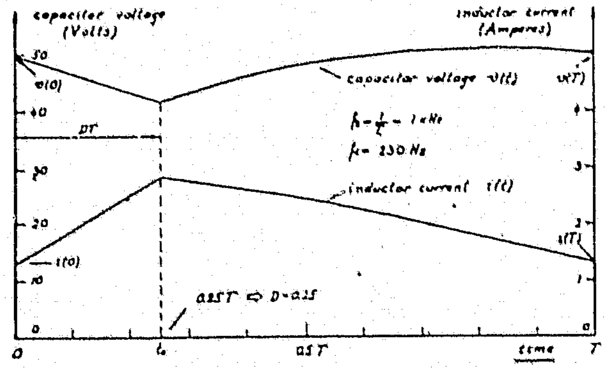

Fig. 17. Typical state-variable time dependence over a single period T in the steady-state, for the boost circuit numerical example with f_s=1kHz.

Insertion of (45) and (46) into (43) results in solution for the initial condition:

$$x_1(0) = V_g(I-e^{D'A_2T}e^{DA_1T})^{-1}(e^{D'A_2T}B_1(DT)+B_2(D'T))b \tag{47}$$

As seen from Fig. 17, the average values of inductor current and capacitor voltage could be found by integration over the period T; in general, the steady-state vector X is found from:

$$X = \frac{1}{T}\left[\int_0^{t_o} x_1(\tau)d\tau + \int_{t_o}^{T} x_2(\tau)d\tau\right] \tag{48}$$

Hence, by use of (43) through (47) in (48), the integration could be carried out and the explicit solution obtained as

$$X(T) = g(A_1,A_2,D,T) \tag{49}$$

in which the actual expression could easily be found [6].

For the boost circuit example of Fig. 3, and with parameter values $V_g = 37.5V$, $D = 0.25$, $R_\ell = 0.46\Omega$, $R_c = 0.28\Omega$, $L = 6mH$, $C = 45\mu F$, and $R = 30\Omega$, the output dc voltage obtained from (49) and the initial inductor current i(0) from (47) are plotted as functions of switching frequency $f_s = 1/T$ in Fig. 18 via a computer program. As seen from Fig. 18, the point where the initial inductor current becomes zero determines the boundary between continuous and discontinuous

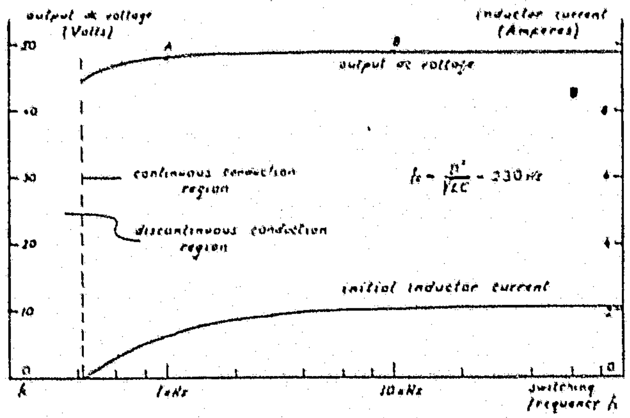

Fig. 18. Typical dependence of the steady-state (dc) conditions (output voltage) on the switching frequency f_s in the continuous conduction region (to the right of the dotted line).

conduction regions. It is also evident from Fig. 18 that the output dc voltage changes with switching frequency f_s, particularly when f_s becomes close to f_c, the effective filter corner frequency.

If the linear approximations (39) are substituted into (49), the first-order approximation of the dc state-vector X becomes independent of T, namely

$$X = -(DA_1+D'A_2)^{-1}b\ V_g \tag{50}$$

which is equivalent to the state-space averaged result (13).

For a given switching frequency, one can find the initial condition $x_1(0)$ and, with use of (43), plot the time dependence of the state variables during a period T to obtain the steady state switching ripple. For the same numerical example for the boost power stage, and with switching frequency $f_s = 1$ kHz (point A on Fig. 18), substantial ripple in the output voltage and inductor current is observed as demonstrated by Fig. 17. However, if all conditions are retained but the switching frequency is increased to $f_s = 10$ kHz (point B on Fig. 18), the plot of Fig. 19 is obtained, from which it is evident that the switching ripple is substantially reduced. Moreover the state variables show very strong linearity in the two intervals Td and Td'. This is by no means an accident, but a consequence of the fact that linear approximations (39) are well satisfied at point B since $f_s/f_c = 43.5 >> 1$, as verified in Appendix C.

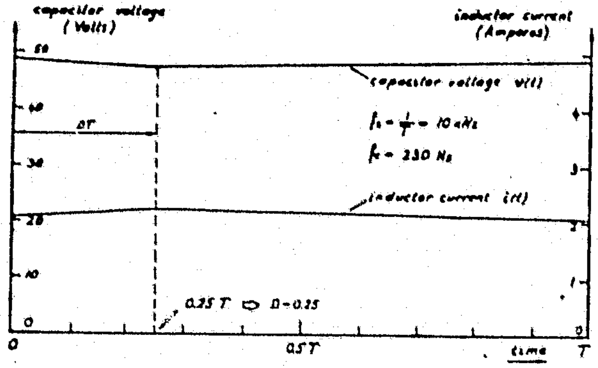

Fig. 19. Same as Fig. 17 but with f_s=10kHz. Strong linearity and small ripple exhibited by the curves are consequences of $e^{AT} \approx I + AT$, since $f_c/f_s \ll 1$.

APPENDIX C

On the linear approximation of the fundamental matrix

We now demonstrate the linear approximations (39) for the boost circuit example (16), in which for simplicity of presentation $R_\ell = 0$ and $R_c = 0$ is assumed. The two exponential (fundamental) matrices are:

$$e^{A_1DT} = \begin{bmatrix} 1 & 0 \\ 0 & e^{-2\alpha DT} \end{bmatrix}$$

(51)

$$e^{A_2DT} = e^{-\alpha D'T} \begin{bmatrix} \cos\omega_o D'T + \frac{\alpha}{\omega_o}\sin\omega_o D'T & -\frac{\sin\omega_o D'T}{\omega_o L} \\ \frac{\sin\omega_o D'T}{\omega_o C} & \cos\omega_o D'T - \frac{\alpha}{\omega_o}\sin\omega_o D'T \end{bmatrix}$$

where

$$\alpha = \frac{1}{2RC}, \quad \omega_o = \sqrt{\frac{1}{LC} - \alpha^2}$$

Suppose now that the switching frequency $f_s = 1/T$ is much greater than the natural frequencies α and ω_o of the converter, such that

$$\omega_o D'T \ll 1 \quad \text{and} \quad \alpha D'T \ll 1 \qquad (52)$$

Then, by introduction of the linear approximations

$$e^{-\alpha D'T} \approx 1-\alpha D'T, \quad \cos\omega_o D'T \approx 1, \quad \sin\omega_o D'T \approx \omega_o D'T \qquad (53)$$

equations (51) reduce to:

$$e^{A_1DT} \approx I + A_1DT$$
$$e^{A_2D'T} \approx I + A_2D'T \qquad (54)$$

For the typical numerical values in Appendix B, and for f_s = 10kHz, replacement of the fundamental matrices by their linear approximations introduces insignificant error (less than 2%) since conditions (52) are well satisfied. Furthermore, since usually $\omega_o \gg \alpha$ (as also in this case), condition (52) becomes

$$\omega_c T \ll 1 \qquad (55)$$

or, with an even greater degree of inequality,

$$f_c \ll f_s \qquad (56)$$

where $2\pi f_c = \omega_c = D'/\sqrt{LC}$ is the effective filter corner frequency.

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A GENERAL UNIFIED APPROACH TO MODELLING SWITCHING DC-TO-DC CONVERTERS IN DISCONTINUOUS CONDUCTION MODE

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ABSTRACT

A method for modelling switching converters in the discontinuous conduction mode is developed, whose starting point is the unified state-space representation, and whose end result is a complete linear circuit model which correctly represents all essential features, namely, the input, output, and transfer properties (static dc as well as dynamic ac small signal). While the method is generally applicable to any switching converter operating in the discontinuous conduction mode, it is extensively illustrated for the three common power stages (buck, boost, and buck-boost). The results for these converters are then easily tabulated owing to the fixed equivalent circuit topology of their canonical circuit model.

The outlined method lends itself easily to investigation of the discontinuous conduction mode in more complex structures (cascade connection of buck and boost converters, for example), in which more than one inductor current may become discontinuous.

As opposed to other modelling techniques, the new method considers the discontinuous conduction mode as a special case of the continuous conduction mode.

1 INTRODUCTION

Switching-mode dc-to-dc converters afford an efficient means of transforming power at one dc voltage to another. There are many circuit configurations capable of performing dc-to-dc conversion, of which the most common are the buck, boost, and buck-boost converters shown in Fig. 1. In each converter, the basic dc-to-dc conversion function is achieved by control of the switch fractional closed-time (transistor on-time), or duty ratio, D ($0 < D < 1$) with constant switching frequency $f_s \triangleq 1/T_s$, where T_s is the switching period.

Two modes of switching converter operation may be distinguished: the *continuous conduction mode* (inductor current never falls to zero, as in Fig. 2a), and the *discontinuous conduction mode* (inductor current becomes zero for a portion of switching period, as in Fig. 2b).

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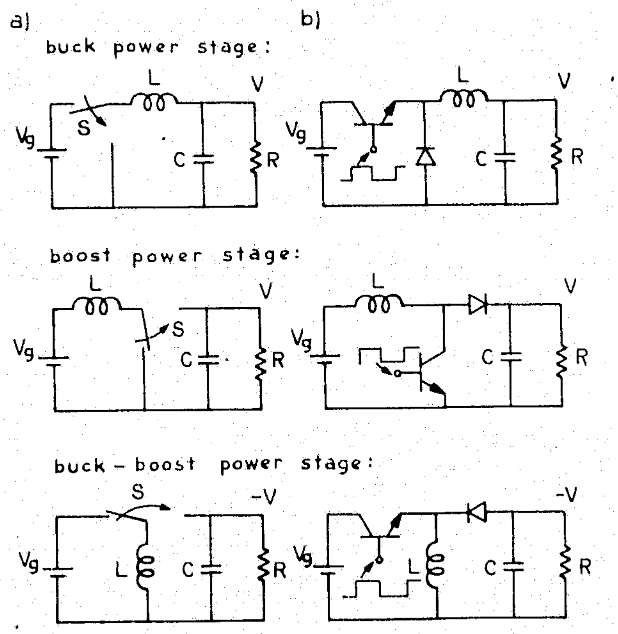

Fig. 1. Three common switching dc-to-dc converters: a) topological configuration independent of switch realization; b) bipolar transistor implementation of the switch S.

Consider, for example, the buck-boost converter of Fig. 1. If the energy stored in the inductor during the first interval $DT_s \equiv D_1T_s$ is completely released to the output load before the switching cycle T_s has ended, the inductor current becomes zero for the last portion D_3T_s, as seen in Fig. 2b.

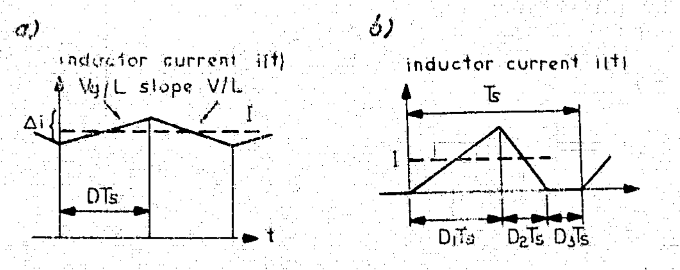

Fig. 2. Inductor current waveforms and definition of two conduction modes: a) continuous conduction mode; b) discontinuous conduction mode.

Thus the transition from continuous to discontinuous conduction mode is obtained by either *increase* of load R (hence by lowering of the average dc current I) or by *decrease* of inductance L or switching frequency f_s. In any case, however, the operation in the discontinuous conduction mode results in *three* different switched networks, as illustrated in Fig. 3 for the buck-boost converter (as opposed to two switched networks for continuous conduction operation). An analogous situation exists for the other two converters of Fig. 1 as well as for a number of other switching converters.

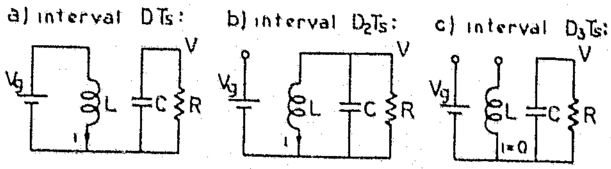

Fig. 3. Three switched networks for the buck-boost converter operating in the discontinuous conduction mode: a) transistor on, diode off; b) transistor off, diode on; c) transistor off, diode off.

In Section 2 an extensive overview of the complete structure of modelling of switching converters and regulators in the discontinuous conduction mode by use of the new method is provided. In particular, the steps leading to the equivalent circuit models that describe both steady-state (dc) and dynamic (ac small signal) behaviour are briefly explained. The subsequent sections then give a detailed and thorough account of the new method outlined in Section 2.

First, in Section 3, the procedure for modelling in discontinuous conduction mode is viewed as a special case of that for continuous conduction mode [1,2,3] (provided the state-space averaging step of [2] is properly generalized to include three or more structural changes within each switching period as shown in Appendix) and *additional constraints* imposed to model special inductor current behaviour. Though the results obtained are in terms of linear equations, the useful circuit realizations may be obtained as in Section 4. The straightforward perturbation and linearization steps in Section 5 lead to dc and ac *circuit* models. They result for three common converters of Fig. 1 in the fixed topology, *canonical circuit model* and are easily tabulated. Because of the need for complete presentation of the theoretical background of the new method, and lack of space, only cursory experimental verification is included at the end of Section 6. Finally, in Section 7 the *completeness* of the obtained converter circuit models is reemphasized by their direct incorporation in *switching regulator* models.

Since the method presented here is essentially a consistent extension of the technique for continuous conduction mode [2], the exposition will closely follow the format given in [2], such that the common steps to both methods become immediately transparent, and those that are different clearly distinguished.

2 REVIEW OF THE NEW STATE-SPACE MODELLING TECHNIQUE IN THE DISCONTINUOUS CONDUCTION MODE

2.1 Brief review of existing modelling techniques

Owing to the relatively more complicated nature of the converter operation in the discontinuous conduction mode, dynamic (ac small signal) models have been lacking (even though valid models for continuous conduction mode have already been obtained) until recently several approaches ([4]-[10]) have been proposed. However, while all these techniques ([4]-[10]) provide through various linearization procedures the proper linearized transfer functions (duty ratio modulation $\hat{d}$ to output voltage $\hat{v}$ and line voltage $\hat{v}_g$ to output voltage $\hat{v}$ transfer functions), they are incapable of representing the input properties of the converter, and hence fail to arrive at the *complete* linearized converter model. This is an entirely analogous situation to that for continuous conduction mode [2,3], where these methods could not model the input properties (open- and closed-loop input impedance, for example) of the converters and regulators in continuous conduction mode of operation. In addition, they stay throughout modelling in the domain of *equation manipulations* only, and thus the useful insight which can be gained from *linear circuit* models (as demonstrated in [1,2,3] is lost. Hence the primary objective of the development here becomes to overcome all these difficulties by extending the powerful state-space averaging technique of [2], together with its circuit model realizations, to the discontinuous conduction mode of converter operation and finally to arrive at the *complete linear circuit model* of various converters (like, for example, those of Fig. 1).

2.2 New state-space and circuit averaging methods for switching converters in the discontinuous conduction mode

The state-space and circuit averaging methods presented in [2] are now to be suitably modified to account for the discontinuous conduction mode of operation, and the results are summarized in the Flowchart of Fig. 4. As before for the continuous conduction mode, the starting model for the switching converter (block 1 in the Flowchart of Fig. 4) is either in terms of the *state-space description* of the switched networks (as in block 1a), or in terms of *linear circuit models* of the switched networks (as in block 1b).

The difference, however, from the previous description is not only that now there are *three* different structural configurations within each switching period, but also in the fact that instantaneous inductor current is *restricted* in its behavior: it starts at zero at the beginning of a switching period and falls to zero current again even before the switching period has expired (see the instantaneous inductor current waveform in block 1 of Fig. 4).

It is actually this second difference which clearly distinguishes the discontinuous conduction mode of operation, while the first difference, that of having three different structural configurations, appears in a way to be merely incidental. That is, in Appendix A it is shown that the state-space averaging step of [2] can be directly extended to include "three-state" converters (converters with three structural changes within each switching period), provided such converters are operated in the continuous conduction mode, and any restrictions on state-space variables (inductor currents and capacitor voltages) are avoided. Therefore, our objective in modelling converters operating in the discontinuous conduction mode (and exhibiting "three-state" configuration behavior) becomes that of supplementing this generalized state-space averaging step for "three-state" converters by additional constraints which reflect the special behavior of one of the state variables, the inductor current. Hence the switching-mode converter operating in the discontinuous conduction mode (and having three structural changes) may be viewed as a *special case* of the ordinary "three-state" converters which are free from any restrictions on state variables. Thus the primary goal is properly to determine these additional constraints and to find how they propagate through various paths of the modelling (such as paths *a* and *b* on the Flowchart of Fig. 4).

From the Flowchart of Fig. 4 it is immediately clear that path *a* follows a development strictly in terms of state-space equations, the state-space averaged modelling technique, while the other path *b* proceeds in terms of circuit models, circuit averaged modelling. Moreover, as before for the continuous conduction mode, along path *a* the general equations (through general matrices A_1, A_2, A_3 and vectors b_1, b_2, and b_3) are retained to emphasize the fact that the outlined procedure is applicable to *any* "three-state" converter operating in the discontinuous conduction mode, while along path *b* a particular example of the boost con-

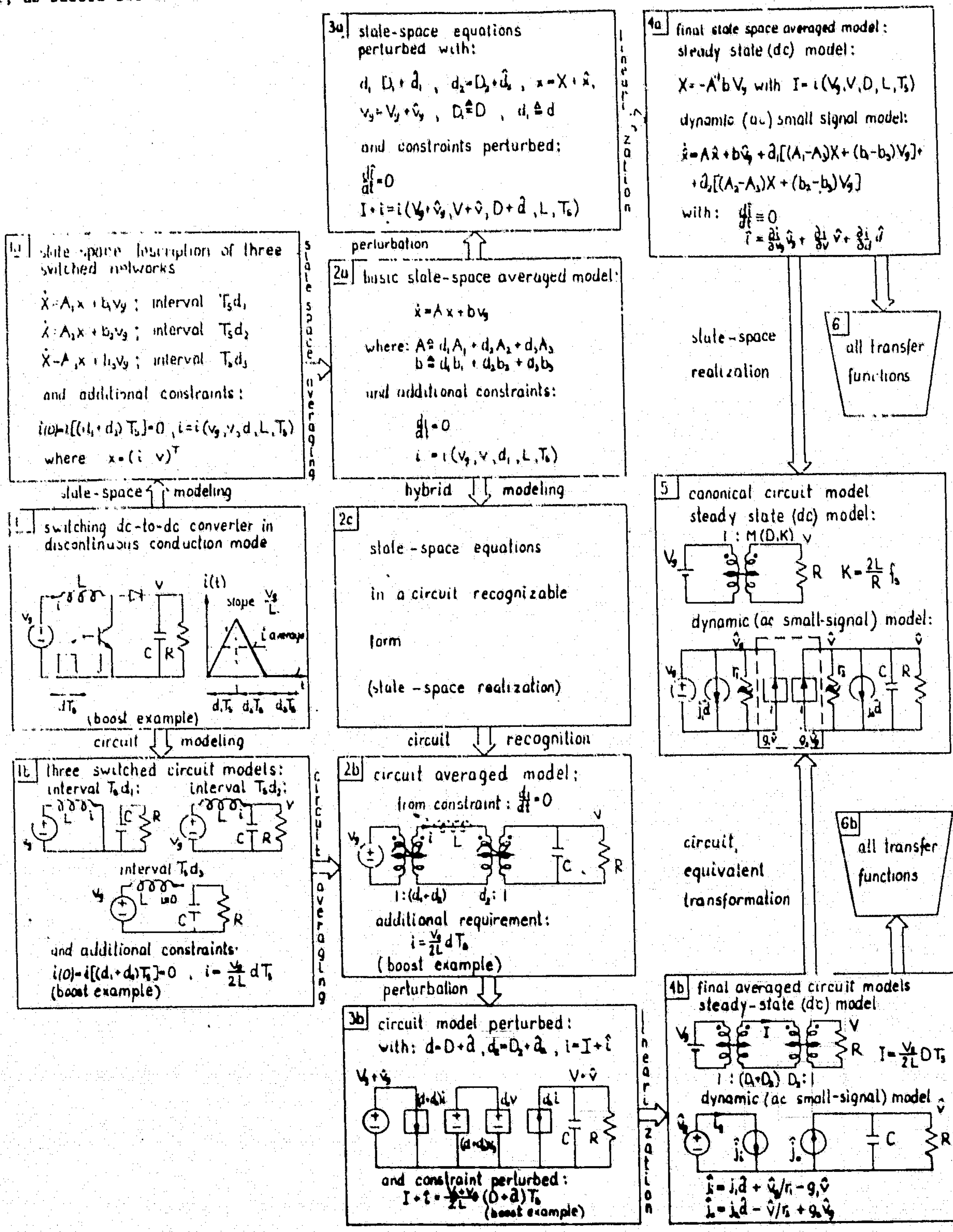

Fig. 4. Flowchart of averaging approaches in modelling switching dc-to-dc converters in the discontinuous conduction mode. Path a: general state-space modelling; Path b: circuit transformation method.

verter is followed, owing to the requirement for the specific converter topology along that path. Specifically, for the boost power stage, $A_1 = A_3 \neq A_2$ are 2 x 2 matrices, and $b_1 = b_2 \neq 0$, $b_3 = 0$ are vectors. This example will later be pursued in detail along both paths.

We now follow path *a* more closely. The crucial step is made in going from block 1a to 2a in that the original description through three state-space equations (block 1a) is substituted by a single state-space averaged model (block 2a). This is justified as follows. The fundamental performance requirement of switching converters (negligible switching ripple) results in natural frequencies ω_a and f_c much lower than the switching frequency f_s. This, in turn, leads as shown in Appendix A to the generalized state-space averaging step. So far this would be the same averaging step as applied to any ordinary "three-state" switching converter. However, as indicated before, the inductor current i *does not* behave as a true state-space variable in the discontinuous conduction mode since it does not have free boundary conditions (but fixed at zero) which is shown to lead to the following constraint:

$$\frac{di}{dt} \equiv 0 \qquad (1)$$

This immediately reduces by one the order of the basic state-space averaged model (block 2a), since one of the dynamic equations (that for inductor current) reduces to a static equation. In addition to this, an expression describing the average inductor current i can be found directly from the converter itself (block 1) and becomes the second constraint, termed perturbation equation I, which is

$$i = i(v_g, v, d, L, T_s) \qquad (2)$$

Thus, the two additional constraints (1) and (2), together with the generalized state-space averaging step, completely determine the converter model in the discontinuous conduction mode. It remains only to apply the standard perturbation techniques (block 3a) and (on the basis of the small-signal assumption) the linearization techniques to both state-space averaged equations and the perturbation equation of block 2a in order to arrive at the final state-space averaged model (block 4a). This model gives separately both dc and ac small-signal descriptions through general matrices A_1, A_2, A_3 and vectors b_1, b_2, b_3 of the starting switched models (block 1a) and constraints corresponding to those of (1) and (2).

Naturally, we can now proceed from the basic state-space averaged model (block 2a) via hybrid modelling and circuit recognition (block 2c) to arrive at the very useful *circuit* realization (block 2b). Note, however, that now the constraint (1) effectively leads to shorting the inductance L in the circuit model since $v_L = L\, di/dt = 0$. This, for the particular boost circuit example, reduces the circuit to first order. The other constraint (2) is also easily specified (see additional constraint in block 2b) with the help of the inductor current waveform (block 1). The same circuit model (block 2b) could, however, be obtained directly from the switched circuit models (block 1b), by following the circuit averaging path, provided the circuit averaging step for "three-state" converters is supplemented by the aforementioned equivalents of the constraints (1) and (2). Again, the remaining circuit perturbation (block 3b) and circuit linearization steps are straightforward and result in the final circuit averaged models (block 4b) separately for dc and ac small-signal. As seen from block 4b, the dc part of the perturbation equation, current I, together with the dc circuit model, completely determines the dc conditions, while its ac part $\hat{i}$ contributes to the final ac circuit averaged model.

Finally, both models (block 4a or 4b) can be used to determine the transfer functions of interest: line voltage variation $\hat{v}_g$ and duty ratio modulation $\hat{d}$ to output voltage $\hat{v}$ (blocks 6a and 6b respectively).

2.3 New canonical circuit model for discontinuous conduction mode

As for the continuous conduction mode, the culmination of the modelling is again a canonical circuit model (block 5 of Fig. 4), whose fixed topology (though different from the one for continuous conduction mode) has all the features necessary to present a *complete circuit model*. However, this fixed topology of the model for discontinuous conduction mode came merely as a by-product, since for the three converters of Fig. 1 (buck, boost, and buck-boost) the ac small-signal models all resulted in the fixed topological structure of the model in block 4b of Fig. 4 without any need for equivalent circuit or other transformations. It does not appear that this canonical circuit topology could be directly extended to some arbitrary converter. Even though this canonical circuit model is not so general as that for two-state converters [2], a useful comparison between the two canonical circuit topologies can be made (at least for the common converters of Fig. 1 in both operating modes).

While in the continuous conduction mode the effect of duty ratio modulation $\hat{d}$ was represented by *voltage* and *current* duty ratio dependent generators at the input port (hence properly representing negative closed-loop input impedance at low frequencies as shown in [2], here in discontinuous conduction mode there are *two* duty ratio dependent *current* generators, one in the input circuit (again, properly to model converter input properties as shown later in Section 7), and the other in the output circuit to generate the duty ratio $\hat{d}$ to output transfer function.

The salient feature of the canonical circuit model in block 5 of the Flowchart in Fig. 4 is that both transfer functions are obtained using only the output port of the complete canonical circuit model, unlike the situation for continuous conduction mode where the complete circuit model was necessary to determine them. This is also why other methods which properly represent the transfer function in discontinuous conduction mode ([4]-[10]) have completely omitted modelling of the converter input properties.

2.4 Extension to complete regulator treatment

It will be shown in Section 7 how the linear model of the modulator stage can be obtained. It remains simple to incorporate the canonical circuit model (block 5 in the Flowchart of Fig. 4) to arrive at the linear circuit model of a closed-loop switching regulator operating in the discontinuous conduction mode.

A word of caution, however, is appropriate here. Namely, since the very nature of operation in the discontinuous conduction mode is that the order of the system is reduced at least by one, this would definitely change the dynamics and possible compensation networks necessary for stable operation of the closed-loop regulator. Furthermore, if both conduction modes are expected to take place for the particular application, the compensation network should be designed to ensure stability of the closed-loop and acceptable transient performance for either of the two modes. Hence canonical circuit models for both continuous and discontinuous conduction mode become an invaluable tool in the proper design of switching regulators. In addition, comparison of the advantages and/or disadvantages between the two modes of operation become feasible, and possible trade-offs between regulator performance and choice of parameters and operating conditions is clearly displayed.

In summary, the new method is generally applicable to *any* "three-state" converter operating in the discontinuous conduction mode (block 4a), even though for an arbitrary converter the final circuit model (block 4b) may have different (more complicated) topology than the canonical circuit model for the three common converters (block 5). We also emphasize the fact that the methods for finding dc and ac small-signal models are *consistent* with each other. Namely, for both models we need only the standard state-space or circuit averaging step (depending on whether path a or b is chosen) applicable to any converter with *three* switched network configurations. Then to distinguish that the converter is operating in the discontinuous conduction mode, additional restrictions (1) and (2) are imposed. Now, the dc part of perturbation equation (2) together with the dc state-space or circuit averaged model completely determines the final dc model, while the ac part $\hat{i}$ of (2) helps in complete definition of the final ac small-signal state-space or circuit averaged model.

It may seem that the method outlined holds only for "three-state" converters in discontinuous conduction mode. This is not so, since it can easily be generalized to include more complicated schemes of discontinuous conduction mode of operation. As an illustration of this generality, consider the new class of switching converters of Appendix A, the cascade connection of ordinary buck and boost converters, which could also be classified as two-inductor converters (as opposed, for example, to the converters of Fig. 1 which are one-inductor converters). Suppose also that the two switches are driven synchronously with the same switch duty ratio D, thus resulting in a two-state converter for continuous conduction operation. If, however, one of the two inductor currents becomes discontinuous, a three-state converter operating in the discontinuous conduction mode is obtained. But now the matrices A_1, A_2, A_3 and A would be of 4th order (as opposed to 2nd order for the converters of Fig. 1) and the final state-space or circuit averaged model would be of the 3rd order (reduction of order by one due to discontinuity of one of the two inductor currents). Moreover, there is also the possibility that both inductor currents could become discontinuous under certain operating conditions in which case four-state converters are generated. Therefore, the generalized state-space averaging step (Appendix A) applicable to four-state converters is supplemented with additional constraints: for each discontinuous current there will be two constraints imposed analogous to (1) and (2). The immediate consequence of these constraints is that the fourth-order original converter model becomes only a second-order final state-space or circuit averaged model (with two inductances effectively disappearing from the final circuit averaged model).

Despite this demonstration of the generality of the method, we will restrict ourselves in the remaining Sections to the "three-state" converters in the discontinuous conduction mode since all the essential features of the method are present there.

3 STATE-SPACE AVERAGING IN DISCONTINUOUS CONDUCTION MODE

Various paths on the Flowchart of Fig. 4 will now be followed in detail, first with general derivation and then illustrated by examples.

3.1 State-space averaging

In this section, the final state-space averaged model (block 4a of Fig. 4) is derived, first in general for any three-state switching converter in discontinuous conduction mode, and then demonstrated on the idealized boost circuit example (parasitic effects not included). Steady state (dc) conditions are obtained for this particular example and discussed in depth, including determination of the boundary between the two modes of converter operation.. From the dynamic (ac small-signal) model, the two transfer functions of interest ($\hat{v}(s)/\hat{v}_g(s)$ and $\hat{v}(s)/\hat{d}(s)$) are also determined to enable comparison with the corresponding transfer functions derived from the final circuit averaged model for the boost converter presented in Section 3.3.

Basic state-space averaged model

We first define the time-domain description of an arbitrary three-state switching converter operating in the discontinuous conduction mode with the help of Fig. 5, which displays the switch drive (Fig. 5a) and instantaneous inductor current (Fig. 5b) which becomes discontinuous. The definition of the three intervals $T_s d_1$, $T_s d_2$, and $T_s d_3$ (or corresponding steady-state quantities $T_s D_1$, $T_s D_2$, and $T_s D_3$) is also clearly visible on Fig. 5.

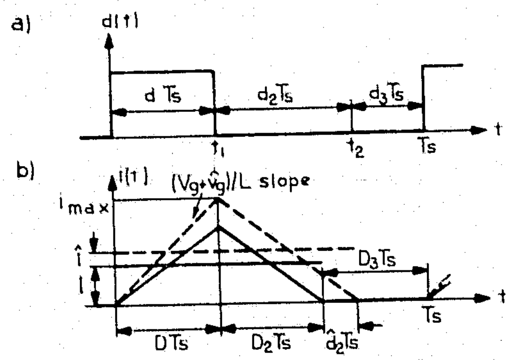

Fig. 5. Definition of the time intervals and perturbation quantities: a) transistor switch drive; b) instantaneous inductor current.

As seen from Fig. 5, the "off" interval $[t_1, T_s]$ is now subdivided into two intervals $T_s d_2$ and $T_s d_3$ (or $T_s D_2$ and $T_s D_3$). While the first "on" interval $T_s D$ is dictated by the switch drive and is a known quantity (at least in open-loop converter usage), the second interval $T_s d_2$ (or $T_s D_2$), which will be termed the "decay" interval, is as yet unknown and depends in general on both the length of the first interval and some circuit parameters, and describes how deep in the discontinuous conduction mode the converter is operating. Nevertheless we assume that the decay interval $T_s D_2$ exists (hence the discontinuous conduction mode) and leave it to the modelling procedure itself to reveal how it is actually determined.

For each of the three intervals in Fig. 5, there exists in general a different switched network (compare with Fig. 3 for the buck-boost converter example), which can be described by a corresponding state-space equation as follows:

$$
\begin{aligned}
\dot{x} &= A_1 x + b_1 v_g \quad \text{for interval } d_1 T_s, \quad (0 \le t \le t_1) \\
\dot{x} &= A_2 x + b_2 v_g \quad \text{for interval } d_2 T_s, \quad (t_1 \le t \le t_2) \\
\dot{x} &= A_3 x + b_3 v_g \quad \text{for interval } d_3 T_s, \quad (t_2 \le t \le T_s)
\end{aligned}
\qquad (3)
$$

While for the continuous conduction mode a similar expression is sufficient to describe the converter, here in discontinuous conduction mode, (3) does not describe the switching converter completely. Namely, the instantaneous inductor current is restricted in its evolution since from Fig. 5

$$i(0) = i[(d_1 + d_2)T_s] = 0 \text{ and } i(t) \equiv 0 \text{ for } t \in [t_2, T_s] \quad (4)$$

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Therefore (3) together with (4) completely determine the behavior of the switching converter. However, directly from this description, even the determination of the steady-state (dc) conditions on an *exact* basis might be a very difficult (if not insurmountable) task, and moreover the tremendous complexity of the result may be unnecessary. In addition, the direct perturbation of (3) and (4) to obtain the dynamic response of the converter would become by an order of magnitude more difficult if not virtually impossible. Our objective then becomes, as it was in [2] for the continuous conduction mode, to replace the original converter description through three state-space equations (3) by a single state-space description which will accurately represent the evolution of the state-vector at the switching instants. It is also desirable that the additional constraint (4) be appropriately accounted for to modify this averaging equivalent, but in such a way as to interfere the least possible with its orderly procedure.

The first task is accomplished by application of the generalized state-space averaging step for three-state converters (Appendix A) to (3), which results in a single state-space description

$$\dot{x} = (d_1A_1 + d_2A_2 + d_3A_3)x + (d_1b_1 + d_2b_2 + d_3b_3)v_g \quad (5)$$

Note, however, that this continuous description is a *continuous equivalent* to the originally derived approximate discrete system [1]. Hence the definition of a discrete derivative [1] transforms the constraint (4) into

$$\frac{di}{dt}(nT_s) = \frac{i(T_s) - i(0)}{T_s} = 0 \quad (6)$$

It follows that the inductor current in the equivalent continuous system (5) *ceases to be a true state-space variable*, since according to (6) it has lost its dynamic properties. Nevertheless, despite the zero constraints $i(nT_s) = 0$ and $di/dt(nT_s) = 0$ for $n = 0,1,\ldots,$ a line voltage perturbation $\hat{v}_g$ (as seen in Fig. 5b) *does* cause a perturbation of the instantaneous inductor current (shown in dotted lines on Fig. 5b) from its steady-state waveform (heavy line in Fig. 5b), which in turn results in a corresponding perturbation $\hat{v}$ of the output steady-state voltage. Note that there is also perturbation of the average inductor current i (defined in Fig. 5b for interval $(d_1 + d_2)T_s$ when instantaneous inductor current $i(t)$ is different from zero) from its steady-state average current I. This is in sharp contrast to the situation in the continuous conduction mode where the average inductor current *does not change* under any small-signal perturbation, but rather initial and final conditions $i(0)$ and $i(T_s)$ change accordingly to accommodate perturbation. Here, $i(0)$ and $i(T_s)$ are fixed at zero. and the average inductor current is the quantity which reflects the effect of introduced perturbation.

Since the objective in modelling the dynamic performance of the converter is faithfully to represent departure from the steady-state, we introduce the average inductor current as a substitute for the "lost" state-variable (the instantaneous inductor current). But, rather than change the symbol, we assign to the same designation i this new meaning. Then from Fig. 5b we obtain

$$i = \frac{i_{max}}{2} = i(v_g, v, d, L, T_s) \quad (7)$$

and designate it *perturbation equation 1*, for reasons which will become apparent later. Naturally, the other constraint (6) for this average inductor current i is maintained (as seen also from Fig. 5b) and we finally obtain the basic state-space averaged model for discontinuous conduction mode:

$$\dot{x} = (d_1A_1 + d_2A_2 + d_3A_3)x + (d_1b_1 + d_2b_2 + d_3b_3)v_g \quad (8)$$

with additional constraints

$$\frac{di}{dt} = 0 \quad (9)$$

$$i = i(v_g, v, d_1, L, T_s) \quad (10)$$

The two additional constraints (9) and (10) modify the ordinary averaged model (8) to account for the discontinuity of the inductor current. This model (block 2a in the Flowchart of Fig. 4) is the starting point for all other derivations (both state-space and circuit-oriented) and represents an averaged model over a single period T_s.

Note, also from (7) that the caluclation of the average inductor current i is actually based on the assumption of the linearity of the inductor current waveform (triangular waveshape in Fig. 5). However, this does not pose any limitations at all, since the linearity of the inductor waveform is again a consequence of the small switching ripple requirement and therefore consistent with the same basic assumption made in the continuous conduction mode.

We now consider first the simplest possible case, determination of the basic dc conditions in the steady state regime. In the steady state all quantities become dc quantities and are denoted by capital letters, that is, $d_1 = D_1 = D$, $d_2 = D_2$, $d_3 = D_3$, $v_g = V_g$, $x = X$. The average inductor current i becomes the *steady state* average inductor current I (see Fig. 5b, for example) and the steady-state vector $X = (I \;\; V \ldots)$. Since then $dX/dt \equiv 0$, the state-space equation (8) reduces to the linear algebraic system

$$AX + bV_g = 0 \quad (11)$$

where

$$A = D_1A_1 + D_2A_2 + D_3A_3$$
$$b = D_1b_1 + D_2b_2 + D_3b_3 \quad (12)$$

while the first constraint (9) is automatically satisfied and the second constraint becomes

$$I = i(V_g, V, D_1, L, T_s) \quad (13)$$

It is now interesting to compare these results for dc conditions (11),(12) and (13) with those for the continuous conduction mode [2]. For easier correlation of these results, the notation $d_1 = d$ and $D_1 = D$ henceforth will be used interchangeably. The steady state vector X is the solution of the linear system (11) as it was before in [2]. Hence storage elements (L's and C's) are proportionality constants in the linear system (11) and it appears as though solution X of (11) is independent of them and dependent on dc duty ratios and resistances in the original model. However, since $D_1 + D_2 + D_3 \equiv 1$ or $D_3 = 1 - (D+D_2)$ from (11) and (12) it follows that the steady state vector X is now dependent on *two* duty ratios D (given) and D_2 (as yet undetermined) as opposed to only D in [2]. The additional constraint (13) which expresses the *average steady state* inductor current I in terms of circuit parameter values can now be used together with (11) to solve for the unknown duty ratio D_2, and hence to determine the length of the second interval D_2T_s. In general, then, D_2 is dependent on circuit parameters (such as L and T_s, for example) and hence dc conditions are also substantially dependent on switching frequency f_s and inductance L. This is in sharp contrast to the continuous conduction mode [2], where dc conditions are dependent on duty ratio D and resistances only.

In summary, expressions (11) and (13) *completely* determine the dc conditions in the discontinuous conduction mode, and at the same time help to determine the length of the second interval D_2T_s, which was unknown at the beginning of this analysis.

We now undertake to obtain the dynamic model by perturbation of the basic model (8-10).

Perturbation

Suppose that the switch drive duty ratio d changes from cycle to cycle, in addition to the line voltage variation. Hence, the general perturbation equations

$$d = D + \hat{d} \qquad d_2 = D_2 + \hat{d}_2, \qquad d_3 = D_3 + \hat{d}_3, \tag{14}$$
$$v_g = V_g + \hat{v}_g, \qquad x = X + \hat{x}, \qquad \text{and} \quad i = I + \hat{i}$$

introduced into the basic-state space averaged model given by (8), (9), and (10) result in

$$\dot{\hat{x}} = [(D+\hat{d})A_1 + (D_2+\hat{d}_2)A_2 + (D_3-\hat{d}-\hat{d}_2)A_3](X+\hat{x}) + \tag{15}$$
$$+ [(D+\hat{d})b_1 + (D_2+\hat{d})b_2 + (D_3-\hat{d}-\hat{d}_2)b_3](V_g+\hat{v}_g)$$

with additional constraints

$$\frac{d\hat{i}}{dt} = 0 \tag{16}$$

$$I + \hat{i} = i(V_g+\hat{v}_g,\ V+v,\ D+\hat{d},\ L,\ T_s) \tag{17}$$

From $d + d_2 + d_3 \equiv 1$, when perturbed by (14), we got $D + \hat{d} + D_2 + \hat{d}_2 + D_3 + \hat{d}_3 \equiv 1$ or, since also $D + D_2 + D_3 \equiv 1$, we finally arrive at

$$\hat{d}_3 = -(\hat{d}+\hat{d}_2) \tag{18}$$

which was then used in (15).

The perturbed model given by (15), (16), and (17) is nonlinear owing to the presence of at least second-order terms.

Linearization and final state-space averaged model for discontinuous conduction mode

We now make the small-signal approximation, namely that the departures from the steady-state values are small compared to the steady-state values themselves:

$$\frac{\hat{v}_g}{V_g} \ll 1, \quad \frac{\hat{d}}{D} \ll 1, \quad \frac{\hat{d}_2}{D_2} \ll 1, \quad \frac{\hat{x}}{X} \ll 1 \tag{19}$$

Using approximations (19) we neglect all second (or higher) order terms, and obtain once again a linear system but including duty-ratio modulation d. After separating the steady-state (dc) and dynamic (ac) parts of both state-space equations (15) and constraints (16) and (17) we arrive at the following results for the final state-space averaged model.

Steady state (dc) model:

$$X = -A^{-1}bV_g \tag{20}$$

Subject to constraint

$$I = i(V_g,\ V,\ D,\ L,\ T_s) \tag{21}$$

Dynamic (ac small signal) model:

$$\dot{\hat{x}} = A\hat{x}+b\hat{v}_g+\hat{d}[(A_1-A_3)X+(b_1-b_3)V_g]+\hat{d}_2[(A_2-A_3)X+(b_2-b_3)V_g] \tag{22}$$

subject to constraints

$$\frac{d\hat{i}}{dt} = 0 \tag{23}$$

$$\hat{i} = \frac{\partial i}{\partial v_g}\hat{v}_g + \frac{\partial i}{\partial v}\hat{v} + \frac{\partial i}{\partial d}\hat{d} \tag{24}$$

where A and b are as given before by (12).

From (24) it also becomes obvious why (7) was originally called "perturbation equation I." In addition, since $\dot{\hat{x}} = [d\hat{i}/dt\ \ d\hat{v}/dt\ \ldots]^T$ the introduction of constraint (23) into (22) reduces the first dynamic equation to a static one, from which the unknown modulation $\hat{d}_2$ can be determined in terms of $\hat{v}_g$ and $\hat{i}$ modulations and circuit parameters.

The dynamic state-space equation which, because of (23), became a static one, can now be designated "perturbation equation II," since it helps to determine the other unknown perturbation quantity $\hat{d}_2$. Together with (24) this uniquely defines the line transfer function $\hat{v}(s)/\hat{v}_g(s)$ and duty ratio modulation transfer function $\hat{v}(s)/\hat{d}(s)$. However, owing to the presence of constraints (23) and (24) no closed-form expression is available for the transfer functions, unlike the case for the continuous conduction mode.

We conclude this section with illustration of these general results on the boost converter. Both dc and ac small-signal models are then analyzed in detail and some unique insights into the operation of the boost converter in the discontinuous conduction mode are obtained. Dc conditions and the determination of the boundary of the two modes of operation are particularly thoroughly analyzed.

Example: ideal boost power stage in discontinuous conduction mode

For the ideal boost power stage of Fig. 1 the three switched networks in the discontinuous conduction mode of operation are shown in Fig. 6.

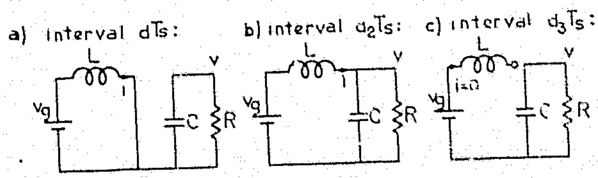

Fig. 6. *Three switched networks of the ideal boost converter of Fig. 1 operating in the discontinuous conduction mode.*

For the choice of state-space vector $x = (i\ \ v)^T$, the state-space equations of the three linear switched networks in Fig. 6 become:

$$\dot{x} = A_1x + b_1v_g \qquad \text{for interval } dT_s$$
$$\dot{x} = A_2x + b_2v_g \qquad \text{for interval } d_2T_2 \tag{25}$$
$$\dot{x} = A_3x + b_3v_g \qquad \text{for interval } d_3T_s$$

where

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$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$$

$$b_1 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T \quad b_2 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T \quad b_3 = \begin{bmatrix} 0 & 0 \end{bmatrix}^T \tag{26}$$

In addition to this, perturbation equation I (7) is needed. However, it can easily be found from Fig. 6a as

$$i = \frac{i_{max}}{2} = \frac{v_g}{2L} dT_s = i(v_g, d, L, T_s) \tag{27}$$

The same result could have been concluded also from Fig. 5b, which actually represents instantaneous inductor current for the boost converter (or buck-boost converter since both have the same slope during interval dT_s).

Equations (26) and (27) contain now all that is needed to determine both dc and ac small-signal models by application of the general result, equations (20) through (24). We first analyze in greater depth the steady-state (dc) model.

Steady state (dc) model analysis

By use of (26) in (20) the following linear algebraic system results

$$\underset{\underline{A}}{\begin{bmatrix} 0 & -\frac{D_2}{L} \\ \frac{D_2}{C} & -\frac{1}{RC} \end{bmatrix}} \underset{\underline{X}}{\begin{bmatrix} I \\ V \end{bmatrix}} + \underset{\underline{b}}{\begin{bmatrix} \frac{D+D_2}{L} \\ 0 \end{bmatrix}} V_g = 0 \tag{28}$$

in which the quantities A, X and b are clearly identified and obtained by use of their definition (12). The general remark made previously about the solution of this linear algebraic system (28) becomes clearly visible. Storage elements (L's and C's) are indeed proportionality constants, and the solution of (28) is

$$\frac{V}{V_g} = 1 + \frac{D}{D_2} \tag{29}$$

$$I = \frac{V}{D_2 R} \tag{30}$$

Hence, the dc conditions depend only on duty ratios D and D_2 and resistance R. From (29) we conclude also that the boost converter has even in the discontinuous conduction mode the boosting property (dc gain $V/V_g \geq 1$), since D, D_2 are by definition positive quantities. However, the dc conditions are not quite determined since D_2 is as yet unknown. But, by use of the additional constraint (21), as further specified in (27) as

$$I = \frac{V_g DT_s}{2L} \tag{31}$$

together with (29) and (30), dc conditions (and also D_2) are *completely* determined. For example, substitution of (31) into (30) results in

$$D_2 = \frac{V}{RI} = \frac{V}{R}\frac{2L}{DT_s V_g} = \frac{V}{V_g}\frac{K}{D} = \frac{MK}{D} \tag{32}$$

where the important dimensionless quantity K is defined as

$$K \triangleq \frac{2L}{RT_s} \triangleq \frac{2L}{R} f_s \tag{33}$$

This dimensionless parameter K plays a key role in the discontinuous conduction mode since it combines uniquely all the parameters responsible for such behavior. Another quantity which will frequently appear is the dc voltage gain V/V_g, so we define also another dimensionless parameter M as

$$M \triangleq \frac{V}{V_g} \tag{34}$$

Finally, by use of (32) and (34) in yet unused dc relation (29), the quadratic equation for dc gain M is obtained

$$M^2 - M - D^2/K = 0 \tag{35}$$

Since from (29) the dc gain M is positive, only the positive solution of (35) is meaningful and we obtain

$$M = \frac{1 + \sqrt{1 + 4D^2/K}}{2} \tag{36}$$

Finally, the substitution of (36) in (32) determines the previously unknown duty ratio D_2 as

$$D_2 = \frac{K}{D}\frac{1 + \sqrt{1 + 4D^2/K}}{2} \tag{37}$$

Hence, we have succeeded in expressing, through (36) and (37), two important quantities, the dc gain M and duty ratio D_2, in terms of the driving condition (duty ratio D of the transistor switch), and the *single* dimensionless quantity K which solely reflects the effect of circuit parameter values (L and R) and the other operating condition, the switching frequency f_s, upon the dc conditions in the discontinuous conduction mode. If desired, the remaining dc quantity, the steady-state average inductor current I, may be found in terms of D and K by use of (37) in (30).

All these expressions (36), (37), and (30) are very useful in predicting the dc conditions when the switching converter is used alone, that is in an *open-loop fashion*, since the duty ratio D is given (independently generated) and the constant K may be calculated from element values with use of (33). However, if the converter is used in a closed-loop switching regulator the output dc voltage V is predetermined by the choice of the reference voltage and kept constant regardless of any variation of input dc voltage V_g, by appropriate self-adjustment of the dc duty ratio D (internally generated) in a negative feedback manner. Hence in *closed-loop operation*, D and D_2 become *dependent* on the external dc gain M and the dimensionless parameter K. These dependences can easily be found from (36) and (37) to get, for closed-loop consideration:

$$D = \sqrt{KM(M-1)} \tag{38}$$

$$D_2 = \sqrt{\frac{KM}{M-1}} \tag{39}$$

Hence, (36) and (37) conveniently determine dc quantities for open-loop considerations, while (38) and (39) are likewise useful for closed-loop considerations.

It is now interesting to compare the open-loop dc gain in the discontinuous conduction mode given by (36) with the corresponding dc gain in the continuous conduction mode, which, for the ideal boost converter is

$$M = \frac{1}{1 - D} \tag{40}$$

Hence, the ideal dc gain (40) is dependent on duty ratio D only and not on circuit parameters (such as L, R) or switching frequency f_s. In sharp contrast to this, the dc gain M in the discontinuous conduction mode (36) is dependent also on K in addition to D and hence is a strong function of switching frequency f_s, inductance L, and load R. Nevertheless, when the converter is used in this mode in a closed-loop regulator, the self-correcting feature of the duty ratio D would compensate any possible changes of load R or switching frequency f_s and still keep the output voltage relatively constant.

Another question naturally arises in comparison of the two dc gains: when do we calculate dc gain from one (36) or the other formula (40), or, what is the criterion to determine in which of the two modes (continuous or discontinuous) the converter is operating? The answer is provided easily with reference to Fig. 5. When the second interval D_2T_s is smaller than interval $(1-D)T_s$, the converter is operating in the discontinuous conduction mode, and in continuous mode otherwise, so the criterion becomes

continuous conduction mode

$$D_2 > 1 - D \tag{41}$$

discontinuous conduction mode

$$D_2 < 1 - D \tag{42}$$

To obtain a convenient quantitative measure we find, first, what happens exactly on the boundary between the two modes of converter operation, or

boundary between two conduction modes

$$D_2 = 1 - D \tag{43}$$

By use of (37) in (43), the equation to determine the critical value of parameter K, that is, K_{crit} for which this happens, is

$$\sqrt{K_{crit}^2 + 4K_{crit}D^2} = 2DD' - K_{crit} \tag{44}$$

from which

$$K_{crit} = DD'^2 \tag{45}$$

The solution (45) is the proper solution of (44) since $2DD' - K_{crit} = 2DD' - DD'^2 = 2DD'(2-D') = 2DD'(1+D)$ is always positive regardless of D, resulting in a proper positive right-hand side of (44). With this, the criteria (41) and (42) for determination of the operating mode become

continuous conduction mode $\quad K > K_{crit} \qquad (46)$

discontinuous conduction mode

$$K < K_{crit} \tag{47}$$

boundary between two conduction modes

$$K = K_{crit} \tag{48}$$

where K, as given before by (33), is a function of parameters L, R, and f_s, while K_{crit} is a function of the duty ratio D only.

We now investigate how these criteria, (46) through (48), behave throughout the duty ratio range $D \in [0,1]$. To facilitate this insight, K_{crit} is plotted as a function of duty ratio D in Fig. 7. As seen in Fig. 7a, $K_{crit}(D)$ has a maximum of 4/27 at D = 1/3. This now enables an important conclusion about operating mode to be drawn. Namely, if the parameters L, R, and f_s are such that the computed parameter K is greater than 4/27, expression (46) is satisfied *regardless* of duty ratio D. Hence for K > 4/27 the converter *always* operates in the continuous conduction mode, no matter what the operating condition (duty ratio D) is. However, if parameters L, R, and f_s are such that K < 4/27 ~ 0.15 the situation becomes as shown in Fig. 7a, where the particular example of K = 0.08 < 0.15 is chosen. For a certain range of duty ratio D, that is $D_{min} < D < D_{max}$ (as shown by the shaded area in Fig. 7a), the condition (47) is satisfied and the converter operates in the *discontinuous conduction* mode, while for the remaining portions of the operating range ($0 < D < D_{min}$ and $D_{max} < D < 1.0$) it again operates in the continuous conduction mode, since then inequality (46) holds.

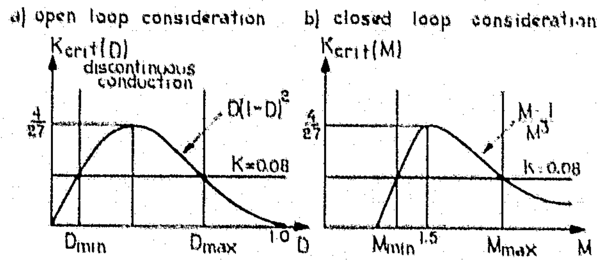

Fig. 7. Determination of the operating mode (continuous or discontinuous) for the ideal boost converter of Fig. 1.

This discussion has been in terms of open-loop considerations, when duty ratio D is given and externally controlled. However, as before for dc conditions, it is desirable to have the boundary condition (45) in terms of the dc gain M, which is a more suitable quantity for closed-loop considerations. This can easily be done since the dc gain M is *continuous* across the boundary (as seen by use of (43) in (29) resulting in (40)), and thus substitution D = (M-1)/M in (45) gives

$$K_{crit} = \frac{M-1}{M^3} \tag{49}$$

This function $K_{crit}(M)$ is plotted in Fig. 7b, and a similar discussion applies. However, now the maximum of $K_{crit}(M)$ of 4/27 is obtained for gain M = 1.5. As before, for K < 4/27, the converter is in the discontinuous conduction mode, but now for dc gain M in the range $M_{min} < M < M_{max}$ as shown by the shaded area in Fig. 7b. This reveals a potentially serious problem if the boost regulator were designed (and compensated) to operate in the discontinuous conduction mode only. Namely, during the initial turn-on process, the output voltage starts from zero, and the converter would have to pass through the continuous conduction region *first* (for $1 < M < M_{min}$), before coming to the discontinuous conduction region (shaded area in Fig. 7b). This would suggest possible stability problems, if the closed-loop were not compensated to assure *stable* operation in the continuous conduction mode as well.

From the standpoint of the dc gains (as a function of duty ratio D), the situation corresponding to that of Fig. 7 is shown in Fig. 8 for some K < 4/27.

From the dc gains for both conduction modes shown in Fig. 8, it becomes obvious that the *actual* dc gain will follow *the larger* of the two gains, thus the mode of operation will change accordingly as the duty ratio changes from 0 to 1. Also in the close vicinity of gain M = 1 ($1 \leq M \leq M_{min}$), the converter is always operating in the continuous conduction mode. Thus, the problem of having, for example, D_2 infinite when $M{\to}1$ from (39) is only a fictitious one, since (39) is for the discontinuous conduction mode and hence not applicable in the vicinity of and at gain $M = 1$.

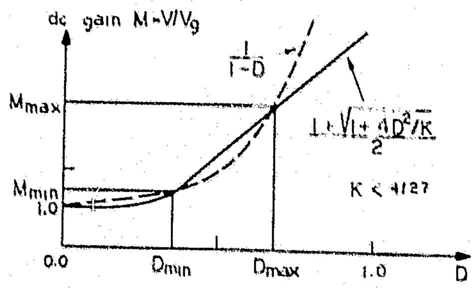

Fig. 8. Boost converter dc voltage gains in continuous and discontinuous conduction modes as a function of duty ratio D.

We conclude this dc analysis with some numerical examples and related quantitative and qualitative significance of the dimensionless parameter K. For example, for the set of parameters $L = 880\mu H$, $R = 220\Omega$ and $f_s = 20kHz$, we compute $K = 2Lf_s/R = 0.16$. Therefore, since $K = 0.16 > 4/27$, the converter will with this set of parameters always operate in the continuous conduction mode. However if, for example, the switching frequency is reduced to $f_s = 10kHz$, this results in $K = 0.08 < 4/27$ and some range of discontinuous conduction operation should be expected (see Figs. 7 and 8). Therefore, the reduction of parameter K below 4/27 causes this transition. From the definition of K in (33) this reduction and change to the discontinuous conduction mode is qualitatively achieved by three means: increase of load R, decrease of the inductance L or switching frequency f_s. There is also a fourth way to enter the discontinuous conduction mode, and that is to change the operating condition, the duty ratio D, as illustrated in Fig. 7 and Fig. 8, but only if the condition $K < 4/27$ is met.

Very often, however, out of all these four possibilities, one is mostly interested in how the change of load R affects the operating mode. Namely, the parameters L and f_s are usually design parameters whose choice may depend on the size and efficiency requirements of the converter or regulator. On the other hand, the range of variation of duty ratio D, or equivalently of gain M, is a design requirement in a closed-loop implementation since the output voltage V is maintained constant against the range of variation of input voltage V_g (hence range of $M = V/V_g$) by the action of negative feedback. The load R also can have a wide range of change depending on the user of the regulator, and is often out of the designer's control. Hence, determination of the converter operating mode with respect to changes of load R becomes important. This can be easily accomplished by finding an equivalent of (45) and (49) respectively, as

$$R_{crit} = \frac{1}{DD'^2} R_{nom} \tag{50}$$

$$R_{crit} = \frac{M^3}{M-1} R_{nom} \tag{51}$$

where R_{nom} is a design parameter defined by

$$R_{nom} \triangleq 2Lf_s \tag{52}$$

The criteria for determination of the operating mode, (46), (47), and (48), then become

continuous conduction mode

$$R < R_{crit} \tag{53}$$

discontinuous conduction mode

$$R > R_{crit} \tag{54}$$

boundary between two modes

$$R = R_{crit} \tag{55}$$

Let us now illustrate this on a numerical example. For $L = 880\mu F$, $f_s = 20kHz$ we calculate $R_{nom} = 35.2\Omega$. By the same argument as before (see Figs. 7 and 8, for example), the converter will *always* operate in the continuous conduction mode if

$$R < \frac{27}{4} R_{nom} \tag{56}$$

or for the given numerical example for $R < 238\Omega$. When $R > 238\Omega$ there will be a range of gain M (see Fig. 8) for which the converter operates in the discontinuous conduction mode.

This concludes the extensive dc analysis and we now turn to the dynamic (ac small-signal) model analysis of this ideal boost converter example.

Dynamic (ac small-signal) model analysis

Before we apply the general result to this ideal boost converter example, let us first put the constraint (27) into a more suitable form by using the steady-state average inductor current I of (31) to get

$$i = \frac{v_g d T_s}{2L} = \frac{v_g d}{V_g D} I \tag{57}$$

By use of perturbation equation (57), model description (26) and definition (12) in the general result given by (22) through (24), we obtain

dynamic (ac small-signal) model

$$\begin{bmatrix} \frac{d\hat{i}}{dt} \\ \frac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D_2}{L} \\ \frac{D_2}{C} & \frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \frac{D+D_2}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{V_g - V}{L} \\ \frac{I}{C} \end{bmatrix} \hat{d}_2 \tag{58}$$

with additional constraints

$$\frac{d\hat{i}}{dt} = 0 \tag{59}$$

$$\hat{i} = \frac{I}{V_g} \hat{v}_g + \frac{I}{D} \hat{d} \tag{60}$$

As opposed to the general result, we can now for this specific example enter the constraints (59) and (60) into dynamic model description (58). The introduction of (59) reduces the first dynamic equation in (58) to a static one, and after proportionality constant L is removed the dynamic model becomes

$$0 = -D_2\hat{v} + (D+D_2)\hat{v}_g + V_g\hat{d} + (V_g - V)\hat{d}_2 \quad (61)$$

$$C\frac{d\hat{v}}{dt} = D_2\hat{i} - \hat{v}/R + I\hat{d}_2 \quad (62)$$

with additional constraint (60). Note, however, that now the first static equation (61) actually determines the *unknown* modulation quantity d_2 (modulation of the second interval $\hat{d}_2T_s$ as shown in Fig. 5, for example) in terms of the other dc and ac quantities. In the remaining dynamic equation (62), besides this modulation $\hat{d}_2$ which we can now express from (61), current modulation $\hat{i}$ also appears. But, from the perturbation equation I (60) it is also determined in terms of the known ac quantities (forced modulations $\hat{v}_g$ and $\hat{d}$). In general, both equations (60) and (61) could have both modulation quantities $\hat{i}$ and $\hat{d}_2$ for some arbitrary converter. But, they are linear algebraic equations and could be solved for $\hat{i}$ and $\hat{d}_2$ in terms of other ac quantities and then substituted in the remaining dynamic description (which could be, for some converter with more than two storage elements, higher than the first order model given by (62)).

Another general feature, which is hidden in this model, is that (61) can be considered as a consequence of the equation

$$(d+d_2)v_g = d_2v \quad (63)$$

which after usual perturbation and linearization steps and subtraction of dc terms reduces to (61). Hence, in analogy to (57), equation (63) can now be designated perturbation equation II. The appearance of (63) in the modelling will become more apparent later in the hybrid modelling and circuit averaging techniques. But in any case, the unknown modulation quantities $\hat{i}$ and $\hat{d}_2$ come as the solution of two linear algebraic equations, which are essentially linearized versions of perturbation equations I and II, (57) and (63) respectively.

To complete the dynamic model description we simply substitute (60) and the solution of $\hat{d}_2$ from (61) in (62) to get

$$C\frac{d\hat{v}}{dt} = -\left(\frac{D_2 I}{V-V_g} + \frac{1}{R}\right)\hat{v} + \left(\frac{D_2}{V_g} + \frac{D+D_2}{V-V_g}\right)I\hat{v}_g + \left(\frac{D_2}{D} + \frac{V_g}{V-V_g}\right)I\hat{d} \quad (64)$$

Since this dynamic model has significance only for the closed-loop regulator, it is convenient to express all dc quantities in terms of M, K, R and output voltage V, as was explained before in the dc analysis. Hence by use of (38), (39) and (30) we obtain

$$C\frac{d\hat{v}}{dt} = -\frac{2M-1}{M-1}\frac{1}{R}\hat{v} + \frac{M}{M-1}\frac{2M-1}{R}\hat{v}_g + \frac{2V}{R}\frac{1}{\sqrt{KM(M-1)}}\hat{d} \quad (65)$$

In (65) all proportionality constants would become infinite and meaningless when $M = 1$. However, it was explained in the dc analysis that in the vicinity of and at gain $M = 1$, the boost converter always operates in the *continuous conduction* mode, hence a different dynamic model applies.

Is is now easy to obtain from (65) two transfer functions of interest

$$G_{vg} = \frac{\hat{v}(s)}{\hat{v}_g(s)} = G_{og}\frac{1}{1 + s/\omega_p} \quad (66)$$

$$G_{vd} = \frac{\hat{v}(s)}{\hat{d}(s)} = G_{od}\frac{1}{1 + s/\omega_p}$$

where

$$\omega_p = \frac{2M-1}{M-1}\frac{1}{RC} \quad (67)$$

and

$$G_{og} = M, \quad G_{od} = \frac{2V}{2M-1}\sqrt{\frac{KM}{M-1}} \quad (68)$$

As seen from (66) both transfer functions have a single pole ω_p and no zeros. This is qualitatively completely different dynamic behavior than in the continuous conduction mode where two poles and even a right half-plane zero are obtained [2] (for the G_{vd} transfer function only). This in turn suggests easier compensation (even no compensation at all) and reduced stability problems if the converter as a part of a switching regulator is operating *consistently* in the discontinuous conduction mode. But, a potential danger exists there: any significant transient changes (such as sudden change of input voltage or temporary substantial change of load R) could move the operating point to the continuous conduction region (see Fig. 8) and cause instability. Another problem is inherent to the discontinuous conduction mode. In addition to the output current, now the input current becomes pulsating as well (as shown in Fig. 5) which increases electromagnetic interference problems. Hence, a decision on the choice of operating mode becomes a complex one, depending on the particular design requirements. To facilitate that decision, we now undertake the task of developing useful *circuit* models of the switching converter operating in the discontinuous conduction mode.

4 HYBRID MODELLING IN DISCONTINUOUS CONDUCTION MODE

We demonstrate in this section how for any specific converter a useful *circuit* model of the basic state-space averaged model (8) can be found, appropriately modified by inclusion of the constraint (9), and supplemented by the additional constraint (10). In terms of the Flowchart of Fig. 4 we will proceed from block 2a through 2c to arrive at the circuit model in block 2b. Again this is illustrated on the same ideal boost converter example as in the previous section.

When the boost converter description (26) and (27) is applied to (8), (9) and (10) the following basic state-space averaged model results:

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d_2}{L} \\ \frac{d_2}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{d+d_2}{L} \\ 0 \end{bmatrix} v_g \quad (69)$$

with additional constraints

$$\frac{di}{dt} = 0 \quad (70)$$

$$i = \frac{v_g dT_s}{2L} \quad (71)$$

It now becomes clear that introduction of (70) into (69) reduces the first dynamic equation to perturbation equation II as given before by (63). But, instead of introducing this substitution, let us first find the circuit realization of the state-space equations (69) as shown in Fig. 9.

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The constraint (70) leads, in the circuit model of Fig. 9, to effective disappearance of the inductance L, since $v_L = L\,di/dt = 0$. The resulting equality of the two voltage generators produces again the perturbation equation II given by (63). At the same time shorting of the inductance causes reduction of system order by one, and effectively a single pole transfer function result becomes apparent.

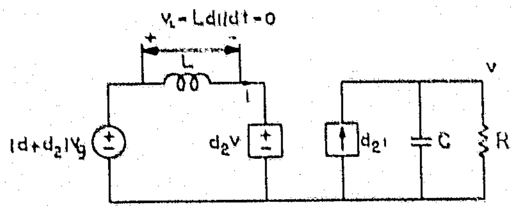

Fig. 9. Circuit realization of the state-space model (69), with constraint (70) also included.

Let us now put the circuit of Fig. 9 into more elegant form, by introducing a dc and ac transformer in place of the two dependent generators in Fig. 9. Also it is desirable to have source voltage v_g effectively at the input of the converter, rather than as some modified quantity as $(d+d_2)v_g$ in Fig. 9. However, this is easily accomplished by introduction of another dc and ac transformer at the input of the converter. In addition, the true input current into the converter becomes properly exposed as seen in the basic circuit-averaged model of Fig. 10. In addition to the circuit model in Fig. 10 we need the remaining constraint (71) to complete the description of the converter in discontinuous conduction mode (as also displayed in Fig. 10). As before, the circuit model and the additional perturbation equation are valid for both dc and ac conditions. Hence the two transformers in Fig. 10 are operating both at ac and dc and the appropriate symbol is introduced.

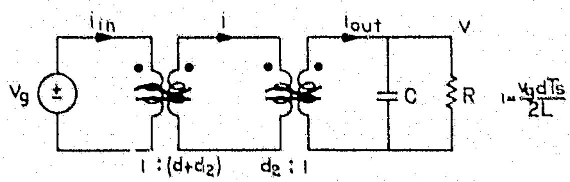

Fig. 10. Basic circuit averaged model for the ideal boost converter in the discontinuous conduction mode.

A word about the new transformer symbol introduced in Fig. 10 is appropriate here. In the modelling of dc-to-dc converters a need naturally arises to have as a *convenient modelling tool* special types of transformers: a transformer which operates for both ac and dc signals, as for example that in Fig. 10, and also a transformer which only works at dc (for which the need will arise later in Section 5.1). Even though these transformers are not physically realizable they are, nevertheless, useful in modelling the basic converter function: dc-to-dc conversion. Hence, as an indicator of their specific functions, the symbols of Fig. 11 are introduced. For consistency, the conventional, physically realizable, ac transformer only, is pictorially represented as in Fig. 11c. Later in Section 5.2, for similar purposes, the same overprint glyphs will be used with resistance symbols.

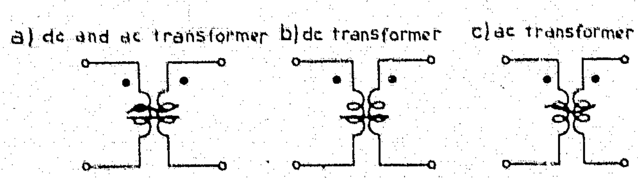

Fig. 11. Definition of various transformer symbols used in modelling switching dc-to-dc converters.

Following the procedure outlined in this section one can easily obtain the basic averaged circuit models of the three common power stages of Fig. 1. These models for discontinuous conduction mode are summarized in Fig. 12.

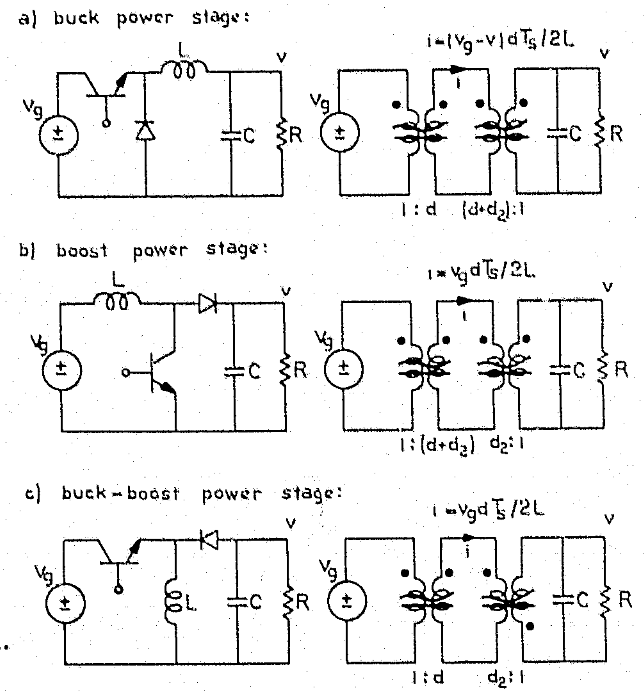

Fig. 12. Summary of the basic circuit averaged models for three common power stages in discontinuous conduction mode.

5 CIRCUIT AVERAGING IN DISCONTINUOUS CONDUCTION MODE

In this section the alternative path *b* in the Flowchart of Fig. 4 is followed and the perturbation and linearization steps corresponding to those in state-space averaging path *a* are applied to the circuit model to arrive at the final circuit averaged models, separately for steady-state (dc) and dynamic (ac) response.

We continue with the same ideal boost converter example and hence use as a starting model the circuit model of Fig. 10. Even though that circuit model was obtained by following hybrid modelling, we emphasize also the other possibility. Namely, it could have been obtained directly by averaging the *three switched circuit models* of Fig. 6 using the standard circuit averaging technique and supplementing it by the appropriate constraints (70) and (71).

Perturbation

If the averaged circuit model of Fig. 10 is perturbed together with its perturbation equation I according to

$$v_g = V_g+\hat{v}_g, \quad i = I+\hat{i}, \quad d = D+\hat{d}, \quad d_2 = D_2+\hat{d}_2, \quad v = V+\hat{v} \tag{72}$$

the nonlinear model of Fig. 13 results.

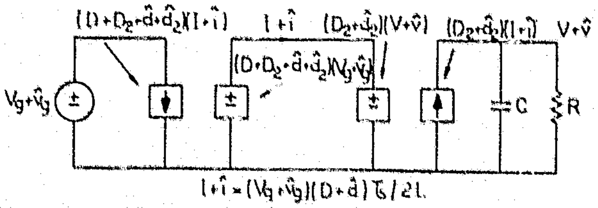

Fig. 13. Perturbation of the basic averaged circuit model in Fig. 10 results in this nonlinear circuit model.

Linearization

With the small-signal assumption on perturbation, that is

$$\hat{d} \ll D, \quad \hat{d}_2 \ll D_2, \quad \hat{i} \ll I, \quad \hat{v} \ll V, \quad \hat{v}_g \ll V_g \quad (73)$$

the second-order terms in Fig. 13 can be neglected and the linearized model of Fig. 14 obtained.

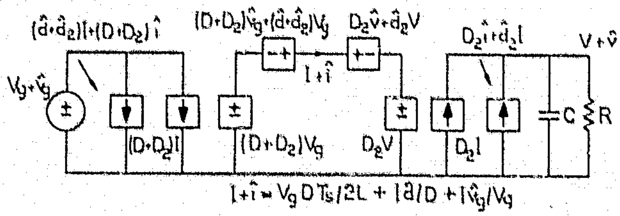

Fig. 14. Model of Fig. 13 linearized to include dc and ac small-signal models.

The circuit model in Fig. 14 together with the dc and ac part of the perturbation equation I (also shown in Fig. 14) completely determines both models. At this point, we continue to develop separately the two circuit models -- the steady-state (dc) circuit model and the dynamic (ac small-signal) model.

5.1 Steady-state (dc) circuit model

With all ac quantities set to zero, the dc circuit model is obtained directly from Fig. 14, and upon substitution of dc dependent generators by the dc transformer symbols, the circuit model in Fig. 15 results.

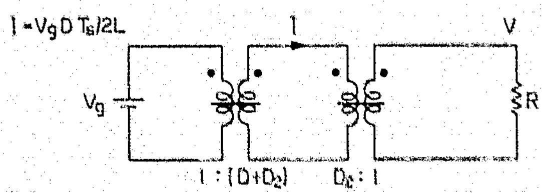

Fig. 15. Final dc circuit model for the boost converter in the discontinuous conduction mode.

This circuit model is also supplemented by the dc part of the perturbation equation I, which is, of course, the same as (31). From the circuit model in Fig. 15 the other two dc relations (29) and (30) are obtained. Hence the dc circuit model leads to the *same* dc conditions and results discussed at length in Section 3.1 on state-space averaging.

We now turn to the development of the dynamic (ac) circuit model.

5.2 Dynamic (ac) circuit model

After the steady-state (dc) quantities are subtracted from the circuit model in Fig. 14 (and perturbation equation as well) the ac circuit model in Fig. 16 is obtained.

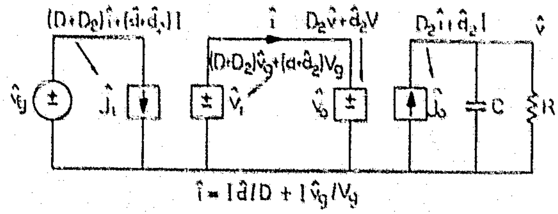

Fig. 16. Dynamic (ac small-signal) circuit model for the boost converter with the constraint on modulation $\hat{i}$ (perturbation equation I) not yet included in the circuit model.

From Fig. 16 it is obvious that the two dependent current generators are functions of two yet undetermined modulation quantities $\hat{d}_2$ and $\hat{i}$, since the other quantities are either already determined from the dc circuit model (such as D_2, I) or are known driving quantities (as D and $\hat{d}$). While the current modulation is already available through the linearized perturbation equation I (see Fig. 16), the other modulation quantity $\hat{d}_2$ can easily be obtained from the inside loop of Fig. 16. Namely, since the two voltage generators in Fig. 16 must be equal, we get

$$(D+D_2)\hat{v}_g + (\hat{d}+\hat{d}_2)V_g = D_2\hat{v} + \hat{d}_2 V \quad (74)$$

Note that this is the same equation as the first (static) equation (61) of the state-space averaged model. Now it is easy to see that (74) and (61) came out actually as a consequence of the perturbation and linearization steps applied to the perturbation equation II (63), since the voltage generators in Fig. 16 resulted from the perturbation and linearization of the voltage generators in Fig. 9, which have been shown to be equal for discontinuous conduction mode (owing to di/dt = 0 constraint).

The equation (74) can now be solved for the unknown modulation $\hat{d}_2$ and, together with the perturbation equation defining $\hat{i}$, determines the two current generators in terms of the known modulation quantities as follows:

$$\hat{j}_i = (\hat{d}+\hat{d}_2)I + (D+D_2)\hat{i} = \frac{2VI}{V-V_g}\hat{d} + \frac{V}{V_g}\frac{(D+D_2)I}{V-V_g}\hat{v}_g - \frac{D_2 I}{V-V_g}\hat{v} \quad (75)$$

$$\hat{j}_o = \hat{d}_2 I + D_2\hat{i} = \frac{2V_g I}{V-V_g}\hat{d} + \frac{V}{V_g}\frac{2V-V_g}{V-V_g}\frac{1}{R}\hat{v}_g - \frac{V}{V-V_g}\frac{1}{R}\hat{v} \quad (76)$$

Since the converter dynamic model is usually used in closed-loop regulator applications, we conveniently express all dc quantities in terms of M, K, R and output regulated voltage V (as explained before) to arrive at

$$\hat{j}_i = \frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}\,\hat{d} + \frac{M^3}{M-1}\frac{1}{R}\hat{v}_g - \frac{M}{M-1}\frac{1}{R}\hat{v} \quad (77)$$

$$\hat{j}_o = \frac{2V}{R}\frac{1}{\sqrt{KM(M-1)}}\,\hat{d} + \frac{M(2M-1)}{M-1}\frac{1}{R}\hat{v}_g - \frac{M}{M-1}\frac{1}{R}\hat{v} \quad (78)$$

By use of (77) and (78) in the circuit model of Fig. 16, the circuit model in Fig. 17 is generated.

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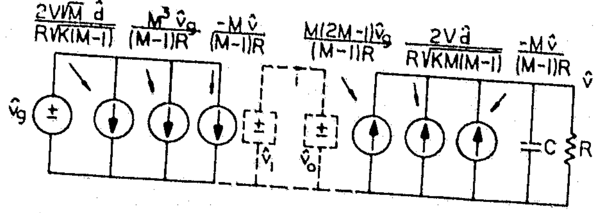


Fig. 17. Dynamic (ac small-signal) circuit model of the boost converter with perturbation equation I (for modulation $\hat{d}$) and perturbation equation II (equality of the voltage generators $\hat{v}_i$ and $\hat{v}_o$) included in the circuit model.

The two voltage generators $\hat{v}_i$ and $\hat{v}_o$ in Fig. 17 are purposely shown in dotted lines to emphasize the fact that they are *no longer essential*, since the information provided by them (74) has already been used to find modulation $\hat{d}_2$ and substituted elsewhere in the circuit model. Therefore they can now be omitted from the circuit model. Finally, by modelling the current generators in Fig. 17 which are proportional to voltages across them as ac resistors only, the final circuit model of Fig. 18 is obtained.

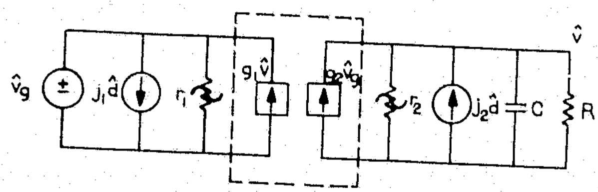


Fig. 18. Final ac small-signal circuit model for boost converter in the discontinuous conduction mode.

The element values in Fig. 18 are defined as

$$j_1 = \frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}, \quad r_1 = \frac{M-1}{M^3}R, \quad g_1 = \frac{M}{M-1}\frac{1}{R} \qquad (79)$$

$$j_2 = \frac{2V}{R}\frac{1}{\sqrt{KM(M-1)}}, \quad r_2 = \frac{M-1}{M}R, \quad g_2 = \frac{M(2M-1)}{M-1}\frac{1}{R} \qquad (80)$$

Also since r_1 and r_2 are ac resistances only, the appropriate symbol consistent with that adopted for the ideal transformer designation (see Fig. 11, for example) is used in Fig. 18. The two current generators inside the dotted-line box in Fig. 18 are used with square symbols to emphasize the fact that they are *dependent* current generators (on some other quantities in the circuit).

From the circuit model in Fig. 18 and by use of element definitions (79) and (80), the two transfer functions G_{vd} and G_{vg} can be derived. It can easily be verified that they agree exactly with those obtained before, ((66), (67) and (68)), using state-space averaging. An interesting observation with regard to the topology of the circuit model in Fig. 18 can be made. Namely, to arrive at these two transfer functions, only the elements in the output port j_2, r_2 and g_2 have been used, without *any* need for input port description. However, the input port description becomes mandatory if the determination of the *complete* circuit model is desired, since it properly models the important input properties (both open- and closed-loop input impedances, for example), as will be illustrated in Section 7.2. Moreover, the output port model now *does* affect the input properties through the dependent current generator $g_1\hat{v}$ in Fig. 18.

An interesting comparison with the circuit model topologies for the continuous conduction mode [1,2] seems appropriate here. While in the continuous conduction mode the effect of duty ratio modulation $\hat{d}$ was expressed through duty ratio dependent voltage and current generators, here two duty ratio dependent current generators (one at the input and the other at the output port) appropriately account for both input and transfer properties (and output properties, as well). Another distinction and unique feature of the circuit model of Fig. 18 is the presence of ac resistances only (which are in general dependent on an operating condition, the gain M), a characteristic not present in the continuous conduction mode. But despite these topological and qualitative differences, the circuit models for continuous conduction mode [1,2] and discontinuous conduction mode (Fig. 18) have something very important in common: they both represent a *complete* linearized circuit model which accurately represents not only transfer properties but input and output properties as well.

The method outlined in this section, and illustrated for the boost converter, is applied to the other two converters of Fig. 1 and results are presented in various tabular forms (including the boost circuit example) in Section 6 on a canonical circuit model.

6 CANONICAL CIRCUIT MODEL FOR DISCONTINUOUS CONDUCTION MODE

In this section the canonical circuit model for discontinuous conduction mode (block 5 in the Flowchart of Fig. 4 or Fig. 18) is obtained for the three common switching converters of Fig. 1, and thanks to its fixed circuit topology, the results are conveniently summarized in the form of various tables, separately for dc and for ac small-signal circuit models.

From the dc conditions and by following the derivations presented in Section 3.1, the simple formulas for determination of the boundary between the two conduction modes may also be found for the buck and buck-boost converters. These results, analogous to (45) and (49) through (51) for the boost converter, are again tabulated for all three common converters of Fig. 1. This then ultimately determines which of the circuit models (those of [2] or those of Sections 5.1 and 5.2) should be chosen for given parameter values and operating conditions of a closed-loop switching regulator. An interesting pictorial interpretation facilitating this decision is given in terms of the frequency scale and position of another "inherent" frequency ω_β (frequency defined by converter element values, like ω_α and f_c before) with respect to switching frequency f_s.

Finally, both dc and ac transfer properties are experimentally verified on a particular buck-boost converter breadboard and excellent agreement with the predictions is observed, thus confirming the high accuracy of the circuit models for the discontinuous conduction mode.

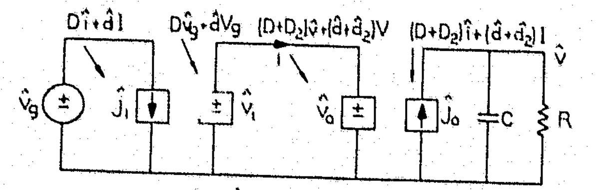
6.1 Derivation of the canonical circuit models for discontinuous conduction mode

In this section the canonical circuit models (both dc and ac small-signal circuit models) for the two remaining converters of Fig. 1 are derived from the basic circuit averaged models in Fig. 12.

Buck converter in discontinuous conduction mode

With regard to the dc circuit model derivation, a general observation seems appropriate here. Namely, the dc circuit model of the boost converter (Fig. 15) could have been obtained *directly* from the unperturbed circuit model in Fig. 12b by simply taking all quantities to be dc quantities and as usual considering the capacitance C to be open for dc signals. Hence, as should have been expected, the circuit models in Fig. 12 together with the additional expressions for the average inductor current i are *valid* dc models. But this is exactly why it was previously emphasized that the presented methods for finding dc and ac models are *consistent* with each other. After all, ac small-signal models really represent the linearized perturbation around some steady-state (dc) conditions. Hence, by perturbation and linearization of the circuit models in Fig. 12, the ac circuit models consistent with the superimposed dc circuit models result. Therefore, the dc circuit model for the buck converter is as in Fig. 12a with dc quantities $d = D$, $d_2 = D_2$, $i = I$, $v_g = V_g$, $v = V$ and *dc* transformers only.

After usual perturbation and linearization steps are applied to the circuit model of Fig. 12a, the dynamic (ac) circuit model in Fig. 19 is obtained.



$$\hat{i} = \frac{I}{V_g-V}\hat{v}_g - \frac{I}{V_g-V}\hat{v} + \frac{I}{D}\hat{d}$$

Fig. 19. Dynamic (ac small-signal) circuit model for the buck converter in discontinuous conduction mode with corresponding perturbation equation I for modulation $\hat{i}$.

The perturbation equation I is different from that for the boost converter and is

$$i = \frac{(v_g-v)dT_s}{2L} = \frac{(v_g-v)d}{(V_g-V)D} I \tag{81}$$

After perturbation and linearization of (81) we get

$$\hat{i} = \frac{I}{V_g-V}\hat{v}_g + \frac{I}{D}\hat{d} - \frac{I}{V_g-V}\hat{v} \tag{82}$$

When the unknown modulation quantity $\hat{d}_2$ is found from equality of the two voltage generators in Fig. 19, and by use of (82), the two current generators in Fig. 19, after expression of dc quantities in terms of closed-loop parameters M, K, R, and V, become

$$\hat{j}_i = j_1\hat{d} + \hat{v}_g/r_1 - g_1\hat{v}; \qquad \hat{j}_o = j_2\hat{d} + g_2\hat{v}_g - \hat{v}/r_2 \tag{83}$$

where

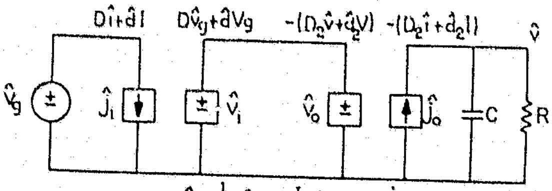
$$j_1 = \frac{2V}{R}\sqrt{\frac{1-M}{K}}, \quad r_1 = \frac{1-M}{M^2}R, \quad g_1 = \frac{M^2}{1-M}\frac{1}{R} \tag{84}$$

$$j_2 = \frac{2V}{R}\frac{1}{M}\sqrt{\frac{1-M}{K}}, \quad r_2 = (1-M)R, \quad g_2 = \frac{M(2-M)}{1-M}\frac{1}{R} \tag{85}$$

Hence the *same topology* of the dynamic (ac) model for the boost converter shown in Fig. 18 is also obtained for the buck converter in the discontinuous conduction mode, but with the model *element values* defined by (84) and (85).

Buck-boost converter in the discontinuous conduction mode

The dc circuit model for the buck-boost converter is obtained directly from the circuit model in Fig. 12c. After perturbation and linearization of the model, the dynamic (ac) circuit model in Fig. 20 is obtained.



$$\hat{i} = \frac{I}{V_g}\hat{v}_g + \frac{I}{D}\hat{d}$$

Fig. 20. Dynamic (ac small-signal) circuit model for the buck-boost converter in discontinuous conduction mode with perturbation equation I (for $\hat{i}$) shown explicitly.

The perturbation equation I is now the same as for the boost converter (71), and the two current generators $\hat{j}_i$ and $\hat{j}_o$ in Fig. 20 are as defined in (83) but with the following element values for the buck-boost converter:

$$j_1 = \frac{2|V|}{\sqrt{KR}}, \quad r_1 = \frac{R}{M^2}, \quad g_1 = 0 \tag{86}$$

$$j_2 = 2\frac{|V|}{\sqrt{KR}}\frac{1}{M}, \quad r_2 = R, \quad g_2 = \frac{2M}{R} \tag{87}$$

Again the same circuit topology of Fig. 18 results, but with element values (86) and (87). However, there is a small distinction from the previous two models since now, as seen in (86), $g_1 = 0$. Therefore there is no feedback effect from the output port to the input circuit model as in the other two converters, and the open-loop input impedance is just r_1. But, this is reasonable to expect for the buck-boost converter, since it is the only converter in which the energy transferring inductance is present either solely in the input circuit (interval DT_s) or solely in the output circuit (interval D_2T_s). In the other two converters (buck and boost), on the other hand, the output circuit (including C and R) is at least for a portion of period T_s *connected* to the input and represents a loading effect on it. Hence the feedback action through current generator $g_1\hat{v}$ is to be expected in these two converters.

The results for all three converters (buck, boost and buck-boost) are summarized in the next section.

6.2 Summary of the canonical circuit model results for three common converters

In this section the results for both dc and dynamic (ac) canonical circuit models for buck, boost, and buck-boost converter are summarized and, owing to the fixed circuit model topology, conveniently listed in several tables.

In Fig. 21 the polarity of the second transformer $1:M_2$ is inverting for the buck-boost converter and otherwise as shown. The parameters in the dc circuit model of Fig. 21 are *defined* in the first three columns of Table I, while the remaining two columns tabulate the dc relations *derived* from this circuit model. Note, however, that this circuit model can be used to determine other dc quantities as well, such as the dc input durrent I_{in} in terms of the defining parameters.

STEADY STATE (DC) CIRCUIT MODEL

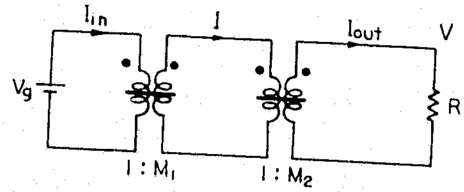


Fig. 21. Steady-state (dc) circuit model for the converters of Fig. 1 in the discontinuous conduction mode.

converter type	definition of dc model			derived quantities	
	M_1	M_2	I (average)	$I = M_2 V/R$	$M = M_1 M_2$
buck	D	$\frac{1}{D+D_2}$	$\frac{(V_g - V)DT_s}{2L}$	$\frac{V}{(D+D_2)R}$	$\frac{D}{D+D_2}$
boost	$D+D_2$	$\frac{1}{D_2}$	$\frac{V_g D T_s}{2L}$	$\frac{V}{D_2 R}$	$\frac{D+D_2}{D_2}$
buck-boost	D	$\frac{1}{D_2}$	$\frac{V_g D T_s}{2L}$	$\frac{V}{D_2 R}$	$\frac{D}{D_2}$

TABLE I. Definition of the dc circuit model in Fig. 21 for the three common converters of Fig. 1 operating in the discontinuous conduction mode.

converter type	open-loop consideration		closed-loop consideration	
	$M(D,K)$	$D_2(D,K)$	$D(M,K)$	$D_2(M,K)$
buck	$\frac{2}{1+\sqrt{1+4K/D^2}}$	$\frac{K}{D}\frac{2}{1+\sqrt{1+4K/D^2}}$	$\sqrt{\frac{KM^2}{1-M}}$	$K(1-M)$
boost	$\frac{1+\sqrt{1+4D^2/K}}{2}$	$\frac{K}{D}\frac{1+\sqrt{1+4D^2/K}}{2}$	$\sqrt{KM(M-1)}$	$\sqrt{\frac{KM}{M-1}}$
buck-boost	$\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$M\sqrt{K}$	$\sqrt{K}$

TABLE II. Summary of dc transfer properties of the three common converters of Fig. 1 in the discontinuous conduction mode expressed for open-loop as well as for closed-loop considerations.

With use now of the last three columns of Table I and the procedures outlined in Section 3, the very useful Table II can be generated, in which the dimensionless parameter K is defined as before with $K = 2L/RT_s = 2Lf_s/R$.

The element values of the dynamic (ac) circuit model in Fig. 22 for the three converters are shown in Table III.

Again, as Table II was generated from Table I and only input-output dc transfer properties obtained, we can similarly generate from Table III another, Table IV, in which only input-output ac transfer properties (transfer functions G_{vg} and G_{vd}) are listed for the three converters.

DYNAMIC (AC SMALL SIGNAL) CIRCUIT MODEL

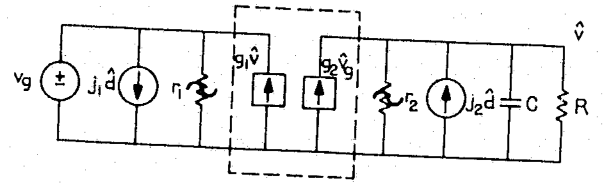


Fig. 22. Final ac small-signal circuit model for converters of Fig. 1 in the discontinuous conduction mode.

type	j_1	r_1	g_1	j_2	r_2	g_2
buck	$\frac{2V}{R}\sqrt{\frac{1-M}{K}}$	$\frac{1-M}{M^2}R$	$\frac{M^2}{1-M}\frac{1}{R}$	$\frac{2V}{RM}\sqrt{\frac{1-M}{K}}$	$(1-M)R$	$\frac{M(2-M)}{1-M}\frac{1}{R}$
boost	$\frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}$	$\frac{M-1}{M^3}R$	$\frac{M}{M-1}\frac{1}{R}$	$\frac{2V}{R\sqrt{KM(M-1)}}$	$\frac{M-1}{M}R$	$\frac{M(2M-1)}{M-1}\frac{1}{R}$
buck-boost	$\frac{2\lvert V\rvert}{R\sqrt{K}}$	$\frac{R}{M^2}$	0	$\frac{2\lvert V\rvert}{R\sqrt{K}M}$	R	$\frac{2M}{R}$

TABLE III. Definition of the elements in the canonical circuit model of Fig. 22 for the three common converters of Fig. 1 operating in the discontinuous conduction mode.

type	G_{og}	G_{od}	ω_p
buck	M	$\frac{2V(1-M)^{3/2}}{\sqrt{K}M(2-M)}$	$\frac{2-M}{1-M}\frac{1}{RC}$
boost	M	$\frac{2V}{2M-1}\sqrt{\frac{KM}{M-1}}$	$\frac{2M-1}{M-1}\frac{1}{RC}$
buck-boost	M	$\frac{V}{\sqrt{K}M}$	$\frac{2}{RC}$
$G_{vg} = \frac{\hat{v}}{\hat{v}_g} = G_{og}\frac{1}{1+s/\omega_p}$; $G_{vd} = \frac{\hat{v}}{\hat{d}} = G_{od}\frac{1}{1+s/\omega_p}$			

TABLE IV. Summary of the ac transfer properties of the three common converters of Fig. 1 operating in the discontinuous conduction mode.

All the results presented in this section are applicable *only to the discontinuous conduction mode* of operation of these three switching converters. To determine when these results ought to be applied and when those for continuous conduction mode [2], the boundary between the two modes of operation is determined for these three converters and tabulated in the next section.

6.3 Determination of the boundary between two conduction modes

As explained in detail in Section 3.1 the criteria for determination of the converter conduction mode are *boundary between the two conduction modes*

$$K = K_{crit} \quad \text{or} \quad R = R_{crit} \tag{88}$$

continuous conduction mode

$$K > K_{crit} \quad \text{or} \quad R < R_{crit} \tag{89}$$

discontinuous conduction mode

$$K < K_{crit} \quad \text{or} \quad R > R_{crit} \tag{90}$$

where K is as defined before $K = 2L/RT_s = 2Lf_s/R$. Following the same procedure outlined in Section 3.1 for the boost converter example, the parameters K_{crit} and R_{crit} can easily be found for the other two converters and all results are shown tabulated in Table V.

converter type	open-loop consideration		closed-loop consideration	
	$K_{crit}(D)$	$R_{crit}(D,R_{nom})$	$K_{crit}(M)$	$R_{crit}(M,R_{nom})$
buck	$1-D$	$\frac{R_{nom}}{1-D}$	$1-M$	$\frac{R_{nom}}{1-M}$
boost	$D(1-D)^2$	$\frac{R_{nom}}{D(1-D)^2}$	$\frac{M-1}{M^3}$	$\frac{M^3}{M-1}R_{nom}$
buck-boost	$(1-D)^2$	$\frac{R_{nom}}{(1-D)^2}$	$\frac{1}{(M+1)^2}$	$(M+1)^2 R_{nom}$

TABLE V. *Determination of the boundary between the two conduction modes, expressed for open-loop as well as for closed-loop considerations.*

In Table V nominal resistance R_{nom} is a design parameter defined by

$$R_{nom} = 2Lf_s \tag{91}$$

It has already been demonstrated in Section 3.1 for the boost converter that parameter K can be chosen ($K > 4/27$), such that the converter is *always* operating in the continuous conduction mode regardless of the operating point, that is dc duty ratio D, while the discontinuous conduction mode can occur only for $K < 4/27$, and then only for a portion of the dynamic range of duty ratio D. The same holds true for the other two converters, and the following criteria can be set:

a) when $K > K_M$ the converter is always in continuous conduction mode regardless of D.

b) when $K < K_M$ discontinuous conduction mode can occur, but only for a limited range of duty ratio D.

Parameter K_M is actually the maximum of the duty ratio D dependent function of first column in Table V, and is for comparison purposes listed in Table VI.

	buck	boost	buck-boost
K_M	1	$\frac{4}{27}$	1

TABLE VI. *Summary of the parameter K_M determining the region of unconditional continuous conduction for three common converters of Fig. 1.*

From Table VI it is obvious that when $K > 1$ any of the three converters listed will *always* operate in the continuous conduction mode, and when $K < 4/27$ each of them will operate in the discontinuous conduction mode for a portion of the duty ratio range. With this, and the first column in Table II, the dc voltage gain as a function of duty ratio can be shown as in Fig. 23b for $K < 4/27$, while the corresponding result for continuous conduction mode is illustrated for comparison purposes in Fig. 23a for $K > 1$.

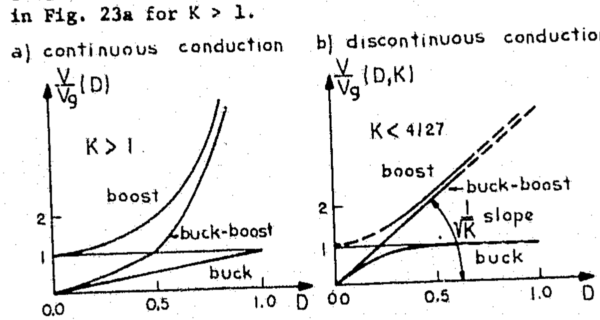


Fig. 23. Comparison of the dc voltage gain characteristics in the two conduction modes for the common converters of Fig. 1.

In Fig. 23b heavy lines designate the region of actual discontinuous conduction operation, whereas dotted lines signify that the continuous conduction mode takes over and the dc gain characteristics begin to follow those for the continuous conduction mode (see for comparison Fig. 8). From Fig. 23b it is also evident that in the buck and the buck-boost converter, the transition between the two conduction modes occurs only once at higher duty ratio D, and *not* also at the lower end as it does in the boost converter. Therefore during initial start-up of the converter, when the duty ratio changes from zero to the value required by the steady-state gain M, the two converters (buck and buck-boost) can be designed to stay in the discontinuous conduction mode only, even in this transitional period.

We now present another viewpoint, which in an interesting pictorial way and a unique frequency interpretation, illuminates the determination of the converter operating mode and the basic small switching ripple requirement. Namely, from Fig. 1 it is apparent that the three common converters essentially consist of the single switch S positioned differently among the source voltage V_g and three elements, inductance L, capacitance C, and load R. With only these three elements three different "inherent" frequencies can be defined regardless of the converter type. Two of them, ω_α and ω_c, termed natural frequencies, are defined as

$$\omega_\alpha = \frac{1}{2RC}, \quad \omega_c = \frac{1}{\sqrt{LC}} \tag{92}$$

However, yet another "inherent" frequency ω_β can be defined by these three elements as

$$\omega_\beta = \frac{R}{2L} \tag{93}$$

The dimensionless parameter K, which plays a crucial role in the determination of the conduction mode, can now be expressed as

$$K = \frac{f_s}{\omega_\beta} \tag{94}$$

Therefore, the position of this new frequency ω_β with respect ot the switching frequency f_s determines the conduction mode. Hence for $K > 1$ or $\omega_\beta < f_s$, each of the three converters will always be in continuous conduction mode regardless of D. On the other hand, $\omega_c \ll f_s$ and $\omega_c \ll f_s$ are requirements for small switching ripple.[8] The information contained in the position of these three "inherent" frequencies ω_α, ω_β and f_c with respect to the switching frequency f_s is concisely summarized in Fig. 24. The diagram in Fig. 24, with the

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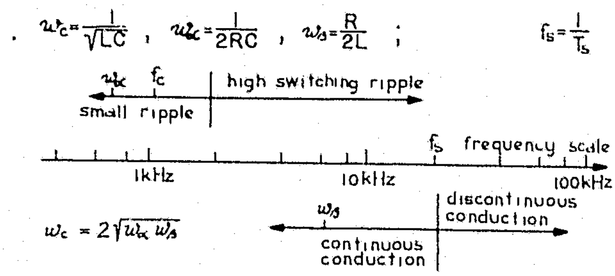

Fig. 24. Frequency interpretation of the conduction mode type and small switching ripple requirement.

help of definitions (92) and (93), displays in a convincing manner the interplay between conduction mode types, switching ripple requirement and choice of parameter values L, C, R, and f_s. For example, increase of load R can cause change to discontinuous conduction mode without deterioration in switching ripple. However, if inductance L or switching frequency is reduced, change to discontinuous conduction mode can occur, but at the price of higher switching ripple since separation between ω_c and f_s is also reduced. One would have to increase capacitance C to remain at an acceptable switching ripple level. Thus the frequency diagram of Fig. 24 gives valuable insight, both qualitative and quantitative, into the basic relationships inherent to switching converters. It is interesting that from (92) and (93) a very simple relationship follows

$$\omega_c = 2\sqrt{\omega_\alpha \omega_\beta} \qquad (95)$$

which may further facilitate quantitative analysis.

6.4 Experimental verification of the transfer properties

Both dc and ac transfer properties have been experimentally verified on a circuit breadboard of the buck-boost converter shown in Fig. 12c. Because of lack of space, only cursory experimental verification is included here.

The buck-boost converter was chosen because of several unique features which clearly distinguish it form the other two converters, and which are easy to check. A quick look at Table II, for example, reveals that it is the only converter whose second interval D_2T_s is independent of the operating conditions (duty ratio D or gain M), but rather is fixed determined by the parameter K only.

Likewise, a look at Table III shows that the ac resistance r_2 is also independent of steady-state operating condition (gain M). Therefore, the single pole of the two transfer funcitons G_{vg} and G_{vd} does not move with change of operating condition (gain M) as it does in the other two converters.

Finally, the open-loop input impedance of the buck-boost converter is $R_1 = R/M^2$ since there is no internal feedback ($g_1 = 0$). Hence the input impedance is purely resistive, which is not the case for the other two converters.

The transfer properties have been verified on the test buck-boost converter with the following switching components: transistor 2N2880 and diode TRW SVD 100-6.

Dc gain measurements

For the choice of element values L = 890μH, C = 12μF, R = 220Ω, f_s = 10kHz and V_g = 6V we compute $K = 2Lf_s/R$ = 0.81 and $D_2 = \sqrt{K} = 0.28$. Therefore, the buck-boost converter operates in the discontinuous conduction mode from D = 0 until D = $1-D_2$ = 0.72, and the experimental dc gain characteristic is shown in this duty ratio range on Fig. 25.

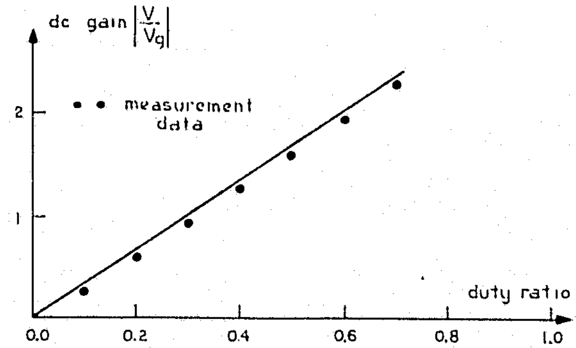

Fig. 25. Dc voltage gain measurements for the buck-boost converter in the discontinuous conduction mode.

As seen in Fig. 25, the experimental points follow very closely the theoretical straight line characteristic. The experimental data, however, are slightly lower than the theoretical curve since the transistor saturation voltage and diode drop have not been accounted for in the theoretical model, although this could easily be accomplished. The inductor current waveform was monitored, and confirmed discontinuous conduction operation for D ε[0,0.72] while D_2 measured was constant as predicted, at D_2 = 0.28.

Ac transfer function measurements

The duty ratio modulation $\hat{d}$ to output voltage $\hat{v}$ transfer function G_{vd} is now measured using the describing function measurement technique [11] and results are shown in Fig. 26.

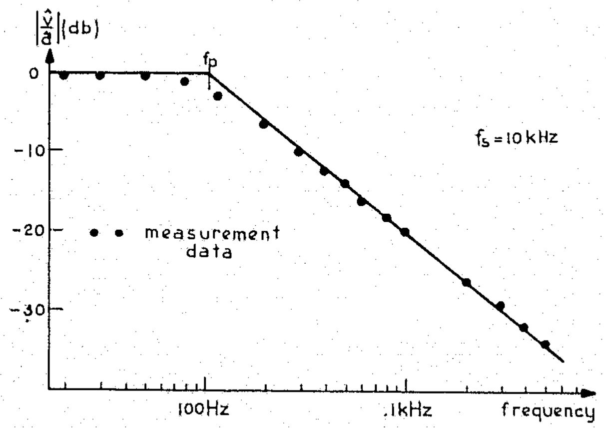

Fig. 26. Experimental magnitude-frequency response of $G_{vd} = \hat{v}/\hat{d}$ transfer function for buck-boost converter in the discontinuous conduction mode.

The element values used are the same as for the dc measurements, except that the inductance was increased four times to L = 3.5mH to reduce the superimposed switching ripple and to reduce the ringing effect in the D_3T_s interval. Hence for L = 3.5mH, C = 12μF, R = 220Ω, f_s = 10kHz, V_g = 6V we calculate K = 1.62 and D_2 = 0.56. The range of discontinuous conduction operation is then reduced to D ε [0,0.44]. The single pole of the transfer functions G_{vg} and G_{vd} (see Table IV) becomes $f_p = 1/\pi RC$ = 120Hz, which is in excellent agreement with the experimental data shown in Fig. 26.

The measurements were repeated for several operating points in the discontinuous conduction region, namely, for $D = 0.1$, 0.2, 0.3, and 0.4 but the single pole at f_p, as predicted, did not move.

The experimental measurements therefore have confirmed the high degree of accuracy of the canonical circuit model (Fig. 22) for the discontinuous conduction mode of operation.

The question of input properties of switching converters and regulators, and particularly of open- and closed-loop input impedances, is thoroughly analyzed in the next section on modelling of a switching mode *regulator* in the *discontinuous conduction mode*.

7 MODELLING OF SWITCHING REGULATOR IN DISCONTINUOUS CONDUCTION MODE

This section demonstrates how the canonical circuit model for a switching converter operating in the discontinuous conduction mode can easily be incorporated into the complete switching-mode regulator model. Consider now a switching-mode regulator as shown in Fig. 27, an illustrative example since the discussion applies to any converter.

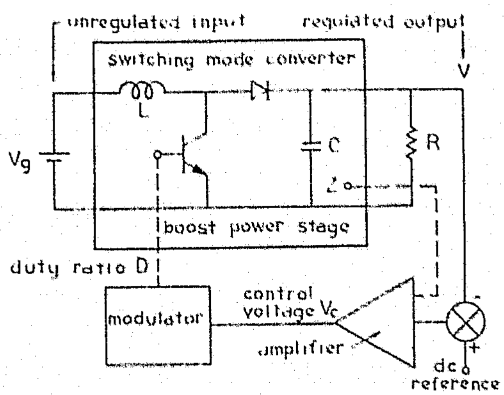

Fig. 27. Switching-mode regulator

7.1 Modulator stage modelling and complete regulator circuit model

So far, we have obtained the canonical circuit model for the switching-mode converter. The next step in development of the regulator equivalent circuit is to obtain a model for the modulator. This is easily done by writing an expression for the essential function of the modulator, which is to convert an (analog) control voltage V_c to the switch duty ratio D. This expression can be written $D = V_c/V_m$ in which, by definition, V_m is the range of control signal required to sweep the duty ratio over its full range from 0 to 1. A small variation $\hat{v}_c$ superimposed upon V_c therefore produces a corresponding variation $\hat{d} = \hat{v}_c/V_m$ in D, which can be generalized to account for a nonuniform frequency response as

$$\hat{d} = \frac{f_m(s)}{V_m}\hat{v}_c \tag{96}$$

in which $f_m(0) = 1$. Thus, the control voltage to duty ratio small-signal transmission characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved.

The inclusion of the canonical circuit model (Fig. 22) and an appropriate model for the modulator stage (96) into the switching regulator (Fig. 27) results in a complete circuit model of a switching regulator in the discontinuous conduction mode, as shown in Fig. 28.

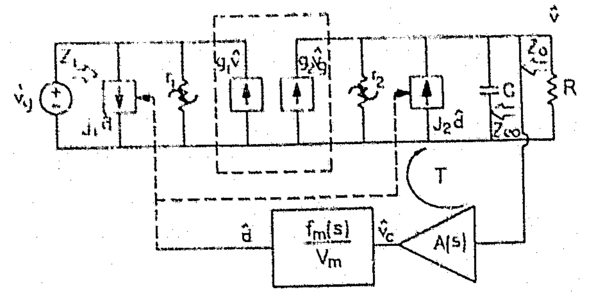

Fig. 28. General ac small-signal circuit model for the switching regulator of Fig. 25 operating in the discontinuous conduction mode.

The generator symbol for the current generators $j_1(s)\hat{d}$ and $j_2(s)\hat{d}$ at the input and output ports, respectively, has been changed from a circle to a square to emphasize that in the closed-loop regulator they have become *dependent* generators (on output voltage variation $\hat{v}$ in particular). A closer look at the circuit model in Fig. 28 reveals some unique properties of this negative feedback circuit. Namely, it has been previously shown in Section 3 that only the output port network (consisting of current generators $g_2\hat{v}_g$, $j_2\hat{d}$, resistances r_2 and R and capacitance C) effectively takes part in determination of the open-loop transfer functions G_{vg} and G_{vd}. The immediate implication of this is that for *ideal source voltage* v_g, the loop gain T is defined only with respect to the output port as shown in Fig. 28. Likewise, the output impedance Z_o and line transmission characteristic F (audio-susceptibility) become solely defined in terms of the output port elements, while the input port takes part only in determination of the input impedance Z_i. This is easily confirmed by analysis of the equivalent circuit in Fig. 28, which leads to

$$T = G_{vd}(s)A(s)f_m(s)/V_m \tag{97}$$

$$Z_o = \frac{Z_{eo}(s)}{1+T} \tag{98}$$

$$F = \frac{G_{vg}(s)}{1+T} \tag{99}$$

$$\frac{1}{Z_i} = -\frac{T}{1+T}\left(\frac{G_{vg}}{G_{vd}}j_1 - \frac{1}{r_1}\right) + \frac{1}{1+T}\left(\frac{1}{r_1} - g_1G_{vg}\right) \tag{100}$$

The first three expressions are rather obvious and are a consequence of the general results of linear feedback theory. They also confirm that T, Z_o, and F are functions of the output port elements only, since the open-loop transfer functions G_{vg} and G_{vd} are independent of input port elements.

It should be noted, however, that this peculiar dependence of some feedback quantities T, Z_o, and F on output port elements only, is a quite *special* case, which is a consequence of the *ideal source voltage* $\hat{v}_g$. If the source voltage had an internal impedance, or an input filter were included in front of the converter, even the open-loop transfer functions G_{vg} and G_{vd} would become *dependent on all* circuit elements, the feedback quantities even more so, and this special feature would

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disappear. This once again demonstrates how powerful these converter equivalent circuit models are, since any of such additional effects can be *directly* included in the circuit model of Fig. 28, owing to its *complete circuit* representation of the converter properties.

We now investigate in more detail the important input properties of the circuit model in Fig. 28.

7.2 Input properties of switching regulators in discontinuous conduction mode

As seen in (100) the input impedance Z_i is also dependent on the input quantities j_1, r_1, and g_1. In addition the input duty ratio dependent current generator j_1 is now responsible for the negative input impedance at low frequencies. Indeed, if $j_1 = 0$, and since at low frequencies $T\to\infty$, the input resistance R_i would appear to be positive, in obvious conflict with the actual physical requirement.

Let us now verify this for the discontinuous conduction mode, and consider first the limiting case of (100) for high loop gain $T\to\infty$ (at low frequencies)

$$\frac{1}{R_i} = -\left(\frac{G_{vg}}{G_{vd}}\, j_1 - \frac{1}{r_1}\right) \qquad (101)$$

From the circuit model in Fig. 28 the converter open-loop transfer functions G_{vg} and G_{vd} are easily found as

$$G_{vg} = g_2(r_2\|R)\frac{1}{1 + sC(r_2\|R)}$$
$$G_{vd} = j_2(r_2\|R)\frac{1}{1 + sC(r_2\|R)} \qquad (102)$$

By use of (102) in (101) we finally obtain the *closed-loop* incremental resistance R_i as

$$R_i = -\left(\frac{j_1}{j_2}\, g_2 - \frac{1}{r_1}\right) \qquad (103)$$

Using now the definitions of element values j_1, j_2, g_2, and r_1 from Table III in (103), we obtain for *all* three converters (buck, boost and buck-boost) that

$$R_i = -\frac{R}{M^2} = -\left(\frac{V_g}{V}\right)^2 R \qquad (104)$$

From (103) it is also evident that despite the presence of the positive term, the negative term has prevailed, correctly predicting the negative closed-loop input resistance.

Let us now consider the other extreme when the loop gain is very small, that is $T\to 0$ (or equivalently at high frequencies). Then, the input impedance approaches the open-loop input impedance Z_{in} obtained from (100) as

$$\frac{1}{Z_{in}} = \frac{1}{r_1} - g_1 G_{vg} \qquad (105)$$

The same result could be obtained directly from the open-loop converter model in Fig. 22. From (105) it seems as though Z_{in} could be negative owing to this negative internal effect of the current generator $g_1 v$ in the model of Fig. 22. However, this is not true, since the low-frequency value of the open-loop input impedance R_{in} becomes from (105)

$$R_{in} = \frac{r_1}{1 - g_1 r_1 g_2 (r_2\|R)} \qquad (106)$$

Again by using element definitions from Table III in (106) we get for *all* three converters

$$R_{in} = \frac{R}{M^2} = \left(\frac{V_g}{V}\right)^2 R \qquad (107)$$

which correctly predicts the open-loop low-frequency input resistance to be positive.

From these results and the corresponding one for continuous conduction mode [1], it follows that the closed-loop low-frequency input resistance R_i is given by (104) *regardless* of the conduction mode type and switching converter type (buck, boost, or buck-boost). The same is also true for the open-loop low-frequency input resistance R_{in} given by (107).

Hence, this section has confirmed that the canonical circuit model for discontinuous conduction mode (Fig. 28) properly models the regulator input properties (closed-loop input impedance) in much the same way as the canonical circuit model for continuous conduction mode [1,2] did, through the presence of duty ratio dependent current generators at the input of the converter model. The immediate consequence of this is that the regulator circuit model (Fig. 28) is a *complete* circuit model which represents all essential properties; input, output and transfer properties.

8 CONCLUSIONS

A general method for modelling *any* three-state switching converter operating in the discontinuous conduction mode has been presented. The fundamental step is in replacement of the state-space descriptions of the three switched networks (3) by their average (8) over the single period T_s, the same step as taken for any ordinary three-state converter. This is then supplemented by additional constraints (9) and (10) which properly account for the discontinuous conduction mode of operation.

The subsequent perturbation and linearization steps are applied not only to the state-space or circuit averaged models but also to the constraints, which then provide the additional information needed to define completely both dc and ac small-signal models.

An extensive analysis of the dc conditions in the discontinuous conduction mode has been given, in Section 3, which then enabled the definition of the boundary between the two operating modes for a specific boost converter example. An easily interpretable formula ((45) or (49)) led to simple criteria ((46), (47) and (48)) for determination of the converter mode of operation.

Analysis of the dynamic (ac small-signal) model confirmed the general modelling prediction - reduction of the system order by one. Thus, common converters of Fig. 1 showed a single-pole frequency response in the discontinuous conduction mode, as opposed to their two-pole response in the continuous conduction mode.

Then, following the hybrid modelling path (Section 4) and the circuit averaging path (Section 5), a new circuit model (Fig. 18) with a rather unusual topological structure is obtained for the boost converter, which provides a complete model for dynamic (ac small-signal) behavior.

The canonical circuit model with the same topology (Fig. 18), but with different element values, is obtained in Section 6 for the other two converters of Fig. 1, and the results are conveniently summarized in various tables. Experimental verification of dc and ac transfer properties of a buck-boost converter in discontinuous conduction mode are also provided.

Finally, the model of the switching-mode *regulator* operating in the *discontinuous conduction mode* is obtained in Section 7, and important input properties (both open- and closed-loop) are thoroughly analyzed.

The outlined method is general and *directly* applicable to investigation of the discontinuous conduction mode in more complex switching converter structures, such as those described in [12,13], involving more than a single inductor.

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APPENDIX A

STATE-SPACE AVERAGING STEP EXTENDED TO CONVERTERS WITH MULTISTRUCTURAL (THREE OR MORE) TOPOLOGICAL CHANGES

We derive the state-space averaging step for switching converters characterized by *three* structural changes within each switching period. Each topological structure can be described as before by linear state-space equations, hence

$$\begin{aligned}
\dot{x}_1 &= A_1x_1 + b_1v_g \quad \text{for interval } d_1T_s, \quad (0 \le t \le t_1)\\
\dot{x}_2 &= A_2x_2 + b_2v_g \quad \text{for interval } d_2T_s, \quad (t_1 \le t \le t_2)\\
\dot{x}_3 &= A_3x_3 + b_3v_g \quad \text{for interval } d_3T_s, \quad (t_2 \le t \le T_s)
\end{aligned} \tag{A.1}$$

Two boundary conditions are now imposed. Since the state-space vector is continuous in transition from first to second and from second to third regions,

$$\begin{aligned}
x_2(t_1) &= x_1(t_1)\\
x_3(t_2) &= x_2(t_2)
\end{aligned} \tag{A.2}$$

Solution of (A.1) under the small signal assumption for $\hat{v}_g$ (where $v_g = V_g + \hat{v}_g$ and $\hat{v}_g << V_g$) yields

$$\begin{aligned}
x_1(t) &= e^{A_1t}x_1(0) + v_gB_1(t)b_1 \quad \text{for } t \in [0,t_1]\\
x_2(t) &= e^{A_2(t-t_1)}x_2(t_1) + v_gB_2(t-t_1)b_2 \quad \text{for } t \in [t_1,t_2]\\
x_3(t) &= e^{A_3(t-t_2)}x_2(t_2) + v_gB_3(t-t_2)b_3 \quad \text{for } t \in [t_2,T_s]
\end{aligned} \tag{A.3}$$

where

$$B_i(t) = \int_0^t e^{A_i\tau}d\tau\,, \quad i = 1,2,3 \tag{A.4}$$

Use of boundary conditions (A.2) in (A.3) gives

$$\begin{aligned}
x_3(T_s) = {} & e^{A_3d_3T_s}e^{A_2d_2T_s}e^{A_1d_1T_s}x_1(0) +\\
& + v_g[e^{A_3d_3T_s}e^{A_2d_2T_s}B_1(d_1T_s)b_1 +\\
& + e^{A_3d_3T_s}B_2(d_2T_s)b_2 + B_3(d_3T_s)b_3]
\end{aligned} \tag{A.5}$$

With introduction of the linear approximations

$$e^{A_id_iT_s} \sim I + A_id_iT_s\,, \quad i = 1,2,3 \tag{A.6}$$

into (A.4) and (A.5), and after retention of only first-order terms (linear in T_s), (A.5) reduces to

$$x_3(T_s') = (I+d_1A_1+d_2A_2+d_3A_3)x_1(0) + (d_1b_1+d_2b_2+d_3b_3)v_g \quad (A.7)$$

This leads to a single continuous linear system

$$\dot{x} = Ax + bv_g \quad \text{where} \quad \begin{array}{l} A \triangleq d_1A_1 + d_2A_2 + d_3A_3 \\ b \triangleq d_1b_1 + d_2b_2 + d_3b_3 \end{array} \quad (A.8)$$

It remains, finally, to characterize the state-space averaging step for the generalized switching converter with n structural changes within each switching period, namely, one described by

$$\dot{x} = A_ix + b_iv_g, \quad \begin{array}{l} d_iT_s = t_i - t_{i-1} \\ t \in [t_{i-1}, t_i] \end{array} \quad i = 1,2,\ldots,n \quad (A.9)$$

for which the corresponding basic state-space averaged model is

$$\dot{x} = Ax + bv_g ; \quad \begin{array}{l} A = \sum_{i=1}^{n} d_iA_i \\ b = \sum_{i=1}^{n} d_ib_i \end{array} \quad (A.10)$$

As an illustration of a switching converter with such multistructural change, consider the converter shown in Fig. A.1a whose two switches S_1 and S_2 are driven as specified in Fig. A.1b. The two switches S_1 and S_2 are shown in their "on" position in Fig. A.1a. It can easily be recognized that this converter is actually a boost converter cascaded by a buck converter whose switches are driven synchronously but with different duty ratios, d_1 and d_1+d_2 respectively.

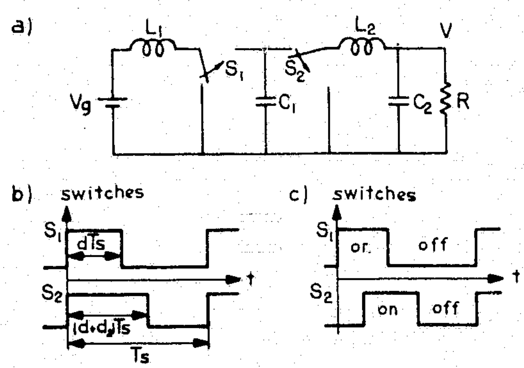

Fig. A.1 Switching converter exhibiting multistructural change: a) boost converter cascaded by a buck converter; b) switch drive for "three-state" behavior; c) switch drive for "four-state" behavior.

However, if this converter is looked upon as single system, the switching action of Fig. A.1b would produce periodic sequential change among three different structures (shown in Fig. A.2b,c, and d), while that of Fig. A.1.c would produce periodic sequential change among all four different switched networks of Fig. A.2. In any case, it demonstrates the feasibility of realization of a switching converter having three or more switched network configurations, *even in the continuous conduction mode* of operation.

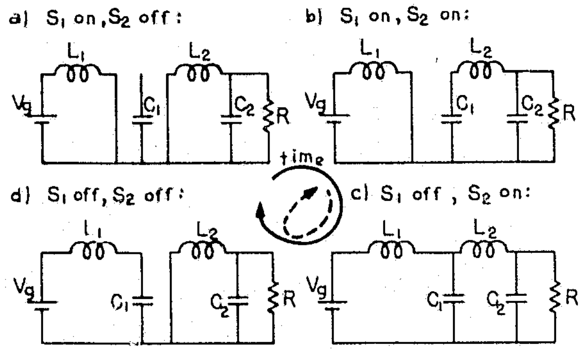

Fig. A.2 Various switched networks for the converter in Fig. A.1a.

On the other hand if the converter is looked upon as consisting of cascaded boost and buck converters and each of them has been modelled separately as a "two-state" converter as in [2], and their models put together, the same result would have been obtained.

However, for the discontinuous conduction mode, in addition to the state-space averaging step (A.8) for "three-state" converters, other restrictions ((1), (2)) are imposed to reflect the limited behavior of inductor current (Fig. 2b) with fixed (zero) boundary values.

But in any case, for either continuous conduction mode [2], or discontinuous conduction mode, the corresponding state-space averaging step is justified on the basis of the fundamental performance requirement for switching dc-to-dc converters of small (negligible) switching ripple, as follows:

switching ripple small ⇨ natural frequencies << switching frequency ⇨ fundamental matrices ~ linear approximation ⇨ state-space averaging step

This, together with proper inclusion of the inductor current discontinuity as additional constraints (1), (2), enable the extremely simple, powerful and accurate scheme for modelling and analysis of switching converters in *discontinuous conduction* mode to be established.

APPENDIX K

DERIVATION OF DESCRIBING FUNCTION OF THE DIGITAL SIGNAL PROCESSOR IN A MULTIPLE-LOOP CONTROLLED SYSTEM

Inherent in the multiple-loop digital signal processor (DSP), shown in Figure 8 on page 38 of the text, is the triangular ramp at the integrator-amplifier output as a result of the rectangular inductor voltage at the integrator input. This ramp, when working in unison with the externally-generated threshold level, produces the necessary mechanism to effect the regulator duty-cycle control.

One is therefore interested in how the duty cycle d(t) of the power switch is being effected by a sinusoidal disturbance at point B. The use of d(t) is more versatile than the voltage at point A, as the result is then applicable to all types of power-circuit configurations. In the case of the buck regulator shown in Figure 8, the voltage at point A is simply $E_i d(t)$ where E_i is the input voltage t, the regulator.

The sinusoidal-disturbance propagation is protrayed in the figure included. The figure includes both circuit implementation and waveform propagation. The switching-frequency triangular ramp and the lower-frequency distrubance are designated by v_x and v_y, respectively. The sum of v_x and v_y is compared to threshold level E_T. Using a constant T_{ON} duty-cycle control as an example, the intersection of (v_x+v_y) with E_T marks the initiation of the T_{ON} interval. The length of T_{ON} is unperturbed by v_y, as the DSP is configured for a constant T_{ON}. After the programmed T_{ON} interval elapses, the length of the subsequent off time is determined by the next intersection of (v_x+v_y) with E_T. Following this pattern, the duty-cycle signal d(t) is illustrated accordingly.

Let the DSP input signal be:

$$(v_x+v_y) = A \sin \omega t$$

and let the DSP output, d(t), be expressed by its Fourier series as:

$$d(t) = D + a_1 \sin \omega t + v_1 \cos \omega t \ldots$$

Then, by definition, the describing function of the pulse modulation becomes:

$$F_M \triangleq \frac{(a_1{}^2 + b_1{}^2)^{1/2}}{A} e^{-j \tan^{-1}(b_1/a_1)}$$

Once a_1 and b_1 can be determined, the gain/phase of the pulse modulation are obtained.

Derivations for a_1 and b_1 are rather tedious tasks. Since the major objective of this appendix is the formulation of the physical mechanism through which d(t) is being effected by (v_x+v_y), the detailed mathematical derivations is not included.

For the constant-T_{ON} duty-cycle control, the describing function can be shown to be:

$$F_M = \frac{2D}{S_F T_n} \left[1 + \left(\frac{\omega T_{ON}}{2}\right)^2\right]^{1/2} e^{-j\omega T_{ON}}$$

where D is the steady-state duty cycle without the disturbance, S_F is the slope of the steady-state integrator output ramp during the off time, and ω is the angular velocity of the sinusoidal disturbance. Based on this describing function, the gain$|_{\text{phase}}$ from point B to A clockwise in Figure 8 becomes:

$$K_p = \frac{2DE_i}{S_F T_{ON}} \left[1 + \left(\frac{\omega T_{ON}}{2}\right)^2\right]^{1/2} e^{-j\omega T_{ON}}$$

This value of K_p, when used in conjunction with eq. (150) on page 107 of the test, completely defines the open-loop transfer function of the multiple-loop control.

A point of particular interest is that the gain of the digital signal processor stage increases with the frequency of the disturbance signal. Realizing the validity of the equation for K_p only holds for frequencies much lower than the switching frequency due to approximations made in its derivation, the equation for K_p has been indeed verified within the signal-frequency range from essentially dc to a decade above the corner frequency of the output filter.

Optimum-Weight Inductor Design With Wire Size Predetermined

STORED PROGRAM

```
[ LIST,INDS1)

      PROGRAM INDS1(INPUT,OUTPUT,TAPE 5=INPUT,TAPE6=OUTPUT)
      REAL L,IP,N
      DATA FC,FW,DC,DI,RHO/2.,.4,8.9,7.8,1.724E-8/
      NAMELIST /B/ DC,DI,FC,FW,RHO,AC,BS,IP,L
      DISPLAY *THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN*
      DISPLAY *OPTIMUM WEIGHT INDUCTOR DESIGN WHEN THE WIRE SIZE*
      DISPLAY *OF THE CONDUCTOR IS ALREADY CHOSEN.*
      DISPLAY *TO USERS: PLEASE READ THE FOLLOWING STATEMENTS*
      DISPLAY *   CAREFULLY BEFORE EXECUTING THE PROGRAM.*
      DISPLAY *NEEDED INPUT PARAMETERS ARE THE FOLLOWING:*
      DISPLAY *   DC : CONDUCTOR DENSITY IN GRAMS CUBIC CM.*
      DISPLAY *          IF NOT GIVEN BY THE USER, DC IS SET*
      DISPLAY *          AT 8.9 BY DEFAULT.*
      DISPLAY *   DI : CORE DENSITY IN GRAMS CUBIC CM.*
      DISPLAY *          IF NOT GIVEN BY USER, DI IS SET*
      DISPLAY *          AT 7.8 BY DEFAULT.*
      DISPLAY *   FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE*
      DISPLAY *          CORE CIRCUMFERENCE.*
      DISPLAY *          IF NOT GIVEN, FC IS SET AT 2. BY DEFAULT.*
      DISPLAY *   FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.*
      DISPLAY *          IF NOT GIVEN,FW IS SET AT .4 BY DEFAULT.*
      DISPLAY *   RHO: CONDUCTOR RESISTIVITY IN OHM-METER. IF*
      DISPLAY *          NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAUL
     + T.*
      DISPLAY *   AC : CONDUCTOR AREA PER TURN, IN CIRCULAR MILS.*
      DISPLAY *   BS : MAXIMUM FLUX DENSITY IN KILOGAUSS.*
      DISPLAY *   IP : PEAK INDUCTOR CURRENT IN AMPERES.*
      DISPLAY *   L  : NEEDED INDUCTANCE IN MICROHENRIES.*
      DISPLAY *PLEASE GIVE INPUT DATA FOR L,IP,BS,AND AC BELOW.*
      DISPLAY *PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,*
      DISPLAY *   DI,FC,FW,AND RHO IF ANY OF DEFAULTED SETTINGS*
      DISPLAY *   IS NOT DESIRED.*
      DISPLAY *NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.*
      DISPLAY *FOR THE ANSWERS AT THE END OF THE RUN,*
      DISPLAY *A IS CORE AREA, Z IS MEAN CORE LENGTH,*
      DISPLAY *N IS NUMBER OF TURNS, U IS PERMEABILITY,*
      DISPLAY *AZ IS PRODUCT OF A AND Z,*
      DISPLAY *W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN AC, AND*
      DISPLAY *P IS THE LOSS OF THE OPTIMUM WEIGHT INDUCTOR.*
      READ (5,B)
      WRITE (6,B)
      S=(1.+12.*FC*FW*DC/DI)**(.5)-1.
      A=1.339E-4*(L*IP*AC/(BS*FW))**(.5)*S
      N=746.9*(L*IP*FW/(AC*BS))**(.5)*(1/S)
      Z=.1961*(L*IP*AC/(BS*FW))**(.25)*(S**(-.5)+S**(.5)/6.)
      U=.275*(IP/BS)**(-1.25)*(AC/FW)**(.75)*L**(-.25)
     C      *S*(S**(-.5)+S**(.5)/6.)
      W=2.93E-5*DC*(L*IP*AC/(BS*FW))**(.75)*S**(-.5)*(6.*FC*FW
     C      +(DI/DC)*(S+S*S/6.))
      AZ=2.624E-5*(L*IP*AC/(BS*FW))**(.75)*(S**(.5)+S**(1.5)/6.)
      P=4*IP*IP*RHO*FC*N*A**.5/AC*1.974E7
      WRITE (6,1)A
    1 FORMAT(*A =*,E10.3, 5X,*SQUARE CENTIMETER*)
      WRITE(6,2)Z
    2 FORMAT(*Z =*,E10.3, 5X,*CENTIMETERS*)
      WRITE(6,3)N
    3 FORMAT(*N =*,E10.3, 5X,*TURNS*)
      WRITE(6,4)U
    4 FORMAT(*U =*,E10.3, 5X,*GAUSS/OERSTED*)
      WRITE(6,5)AZ
    5 FORMAT(*AZ=*,E10.3, 5X,*CUBIC CENTIMETERS*)
      WRITE(6,6)W
    6 FORMAT(*W =*,E10.3, 5X,*GRAMS*)
      WRITE(6,7)P
    7 FORMAT(*P =*,E10.3, 5X,*WATTS*)
      END
```

Program Objective

User Instruction Part of the Program

Program

Output Format Specification

SAMPLE RUN

```
[ RUN,I=INDS1,6
 THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN
 OPTIMUM WEIGHT INDUCTOR DESIGN WHEN THE WIRE SIZE
 OF THE CONDUCTOR IS ALREADY CHOSEN.
 TO USERS: PLEASE READ THE FOLLOWING STATEMENTS
    CAREFULLY BEFORE EXECUTING THE PROGRAM.
 NEEDED INPUT PARAMETERS ARE THE FOLLOWING:
    DC : CONDUCTOR DENSITY IN GRAMS CUBIC CM.
           IF NOT GIVEN BY THE USER, DC IS SET
           AT 8.9 BY DEFAULT.
    DI : CORE DENSITY IN GRAMS/CUBIC CM.
           IF NOT GIVEN BY USER, DI IS SET
           AT 7.8 BY DEFAULT.
    FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE
           CORE CIRCUMFERENCE.
           IF NOT GIVEN, FC IS SET AT 2. BY DEFAULT.
    FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.
           IF NOT GIVEN,FW IS SET AT .4 BY DEFAULT.
    RHO: CONDUCTOR RESISTIVITY IN OHM-METER. IF
           NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT.
    AC : CONDUCTOR AREA PER TURN, IN CIRCULAR MILS.
    BS : MAXIMUM FLUX DENSITY IN KILOGAUSS.
    IP : PEAK INDUCTOR CURRENT IN AMPERES.
    L  : NEEDED INDUCTANCE IN MICROHENRIES.
 PLEASE GIVE INPUT DATA FOR L,IP,BS,AND AC BELOW.
 PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,
    DI,FC,FW,AND RHO IF ANY OF DEFAULTED SETTINGS
    IS NOT DESIRED.
 NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
 FOR THE ANSWERS AT THE END OF THE RUN,
 A IS CORE AREA, Z IS MEAN CORE LENGTH,
 N IS NUMBER OF TURNS, U IS PERMEABILITY,
 AZ IS PRODUCT OF A AND Z,
 W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN AC, AND
 P IS THE LOSS OF THE OPTIMUM WEIGHT INDUCTOR.
  $B
? L=200.,IP=4.5,BS=3.5,AC=3000.$
 $B
 DC       = 8.9,
 DI       = 7.8,
 FC       = 2.0,
 FW       = 4.0E-01,
 RHO      = 1.724E-08,
 AC       = 3.0E+03,
 BS       = 3.5,
 IP       = 4.5,
 L        = 2.0E+02,
 $END
A = 4.579E-01      SQUARE CENTIMETER
Z = 6.571E+00      CENTIMETERS
N = 5.628E+01      TURNS
U = 9.512E+01      GAUSS/OERSTED
AZ= 3.001E+00      CUBIC CENTIMETERS
W = 6.746E+01      GRAMS
P = 6.991E-01      WATTS
```

Computer Printout of User Instruction

User's Input

Printout of User Input Summary

Printout of Calculated Output

Optimum-Weight Inductor Design With A Given Loss Constraint

STORED PROGRAM

```
[ LIST,INDOS2

      PROGRAM INDOS2(INPUT,OUTPUT,TAPE5=INPUT,TAPE6=OUTPUT)
      REAL L,IP,N
      DATA FC,FW,DC,DI,RHO /2.,.4,8.9,7.8,1.724E-8/
      NAMELIST /B/ DC,DI,FC,FW,RHO,P,BS,IP,L
      DISPLAY *THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN*
      DISPLAY *OPTIMUM WEIGHT INDUCTOR DESIGN FOR A GIVEN LOSS.*
      DISPLAY *TO USERS: PLEASE READ THE FOLLOWING STATEMENTS*
      DISPLAY *   CAREFULLY BEFORE EXECUTING THE PROGRAM.*
      DISPLAY *THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:*
      DISPLAY *   DC : CONDUCTOR DENSITY IN GRAMS/CUBIC CM.*
      DISPLAY *        IF NOT GIVEN BY THE USER, DC IS SET*
      DISPLAY *        AT 8.9 BY DEFAULT.*
      DISPLAY *   DI : CORE DENSITY IN GRAMS/CUBIC CM.*
      DISPLAY *        IF NOT GIVEN BY THE USER, DI IS SET*
      DISPLAY *        AT 7.8 BY DEFAULT.*
      DISPLAY *   FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE*
      DISPLAY *        CORE CIRCUMFERENCE.*
      DISPLAY *        IF NOT GIVEN,FC IS SET AT 2. BY DEFAULT.*
      DISPLAY *   FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.*
      DISPLAY *        IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.*
      DISPLAY *   RHO: CONDUCTOR RESISTIVITY IN OHM-METER. IF*
      DISPLAY *        NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAU
+ T.*
      DISPLAY *   P  : DESIGNED POWER LOSS IN WATTS.*
      DISPLAY *   BS : MAXIMUM FLUX DENSITY IN KILOGAUSSES.*
      DISPLAY *   IP : PEAK INDUCTOR CURRENT IN AMPERES.*
      DISPLAY *   L  : DESGNED INDUCTANCE IN MICROHENRIES.*
      DISPLAY *PLEASE GIVE INPUT DATA FOR L,IP,BS,AND P BELOW.*
      DISPLAY *PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,*
      DISPLAY *   FC,FW,AND RHO IS ANY OF DEFAULTED SETTINGS IS*
      DISPLAY *   NOT DESIRED.*
      DISPLAY *NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
      DISPLAY *FOR ANSWERS AT THE END OF THE RUN,*
      DISPLAY *A IS CORE AREA, Z IS MEAN CORE LENGTH,*
      DISPLAY *N IS NUMBER OF TURNS, U IS PERMEABILITY,*
      DISPLAY *AZ IS PRODUCT OF A AND Z,AC IS CONDUCTOR AREA PER*
      DISPLAY *TURN,W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN P.*
      READ(5,B)
      WRITE (6,B)
      S=(DI*FC/(DC*FW))**.5+(DI*FC/(DC*FW)+96.*FC*FC)**.5
      A=10.*(RHO*DC*FC**4./(BS*BS*DI))**.4*S**(-.8)*
     C     (IP**4.*L*L/P)**.4
      N=9.88E-3*(DI*DI/(DC*DC*BS*RHO*RHO*FC**8.))**.2*S**.8
     C     *(L*P*P/IP**3.)**.2
      Z=(1.25*(DI**3.*RHO*RHO/(FW**5.*DC**3.*BS**4.*FC**7.))**.1
     C     *S**.6+10.0*(RHO*FC**4.*DC/(BS*BS*DI))**.2*S**(-.4))
     C     *(IP**4.*L*L/P)**.2
      AC=2.481E6*(DI*FC*RHO**4./(DC*BS**3.))**.2*S**.4*
     C     (IP**11.*L**3./P**4.)**.2
      U=79.58*L*Z/(A*N*N)
      AZ=A*Z
      W=2.0E-5*FC*DC*AC*N*A**.5+DI*A*Z
      WRITE (6,1)A
    1 FORMAT(*A =*,E10.3,5X,*SQUARE CENTIMETERS*)
      WRITE (6,2)Z
    2 FORMAT(*Z =*,E10.3,5X,*CENTIMETERS*)
      WRITE (6,3)N
    3 FORMAT(*N =*,E10.3,5X,*TURNS*)
      WRITE (6,4)U
    4 FORMAT(*U =*,E10.3,5X,*GAUSS/OERSTED*)
      WRITE (6,5)AZ
    5 FORMAT(*AZ=*,E10.3,5X,*CUBIC CENTIMETER*)
      WRITE (6,6)AC
    6 FORMAT(*AC=*,E10.3,5X,*CIRCULAR MILS*)
      WRITE (6,7)W
    7 FORMAT(*W =*,E10.3,5X,*GRAMS*)
      END
```

Program Objective

User Instruction Part of the Program

Program

Output Format Specification

SAMPLE RUN

```
[ RUNX,I=INDOS2,G
 THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN
 OPTIMUM WEIGHT INDUCTOR DESIGN FOR A GIVEN LOSS.
 TO USERS: PLEASE READ THE FOLLOWING STATEMENTS
    CAREFULLY BEFORE EXECUTING THE PROGRAM.
 THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:
    DC : CONDUCTOR DENSITY IN GRAMS/CUBIC CM.
         IF NOT GIVEN BY THE USER, DC IS SET
         AT 8.9 BY DEFAULT.
    DI : CORE DENSITY IN GRAMS/CUBIC CM.
         IF NOT GIVEN BY THE USER, DI IS SET
         AT 7.8 BY DEFAULT.
    FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE
         CORE CIRCUMFERENCE.
         IF NOT GIVEN,FC IS SET AT 2. BY DEFAULT.
    FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.
         IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.
    RHO: CONDUCTOR RESISTIVITY IN OHM-METER. IF
         NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT.
    P  : DESIGNED POWER LOSS IN WATTS.
    BS : MAXIMUM FLUX DENSITY IN KILOGAUSSES.
    IP : PEAK INDUCTOR CURRENT IN AMPERES.
    L  : DESGNED INDUCTANCE IN MICROHENRIES.
 PLEASE GIVE INPUT DATA FOR L,IP,BS,AND P BELOW.
 PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,
    FC,FW,AND RHO IF ANY OF DEFAULTED SETTINGS IS
    NOT DESIRED.
 NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
 FOR ANSWERS AT THE END OF THE RUN,
 A IS CORE AREA, Z IS MEAN CORE LENGTH,
 N IS NUMBER OF TURNS, U IS PERMEABILITY,
 AZ IS PRODUCT OF A AND Z,AC IS CONDUCTOR AREA PER
 TURN,W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN P.
  $B
? L=200.,IP=4.5,BS=3.5,P=0.6991$
 $B
 DC      = 8.9,
 DI      = 7.8,
 FC      = 2.0,
 FW      = 4.0E-01,
 RHO     = 1.724E-08,
 P       = 6.991E-01,
 BS      = 3.5,
 IP      = 4.5,
 L       = 2.0E+02,
 $END
A = 6.939E-01      SQUARE CENTIMETERS
Z = 6.391E+00      CENTIMETERS
N = 3.661E+01      TURNS
U = 1.094E+02      GAUSS/OERSTED
AZ= 4.435E+00      CUBIC CENTIMETER
AC= 2.419E+03      CIRCULAR MIL
W = 6.085E+01      GRAMS
```

Computer Printout of User Instruction

User's Input

Printout of User Input Summary

Printout of Calculated Output

Optimum-Loss Inductor Design With
A Given Weight Constraint

STORED PROGRAM

```
C LIST,INDOS3

      PROGRAM INDOS3(INPUT,OUTPUT,TAPE5=INPUT,TAPE6=OUTPUT)
      REAL L,IP,N
      DATA FC,FW,DC,DI,RHO /2.,.4,8.9,7.8,1.724E-8/
      NAMELIST /B/DC,DI,FC,FW,RHO,W,BS,IP,L
      DISPLAY *THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN*
      DISPLAY *OPTIMUM LOSS INDUCTOR DESIGN FOR A GIVEN WEIGHT.*
      DISPLAY *TO USERS: PLEASE READ THE FOLLOWING STATEMENTS*
      DISPLAY *   CAREFULLY BEFORE EXECUTING THE PROGRAM.*
      DISPLAY *THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:*
      DISPLAY *   DC : CONDUCTOR DENSITY IN GRAM/CUBIC CM.*
      DISPLAY *          IF NOT GIVEN BY THE USER, DC IS SET*
      DISPLAY *          AT 8.9 BY DEFAULT.*
      DISPLAY *   DI : CORE DENSITY IN GRAMS/CUBIC CM.*
      DISPLAY *          IF NOT GIVEN BY THE USER, DI IS SET*
      DISPLAY *          AT 7.8 BY DEFAULT.*
      DISPLAY *   FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE*
      DISPLAY *          CORE CIRCUMFERENCE.*
      DISPLAY *          IF NOT GIVEN, FC IS SET AT 2. BY DEFAULT.*
      DISPLAY *   FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.*
      DISPLAY *          IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.*
      DISPLAY *   RHO:CONDUCTOR RESISTIVITY IN OHM-METER. IF*
      DISPLAY *        NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT
     + .*
      DISPLAY *   W  : ALLOWED INDUCTOR WEIGHT IN GRAMS.*
      DISPLAY *   BS : MAXIMUM FLUX DENSITY IN KILOGAUSSES.*
      DISPLAY *   IP : PEAK INDUCTOR CURRENT IN AMPERES.*
      DISPLAY *   L  : NEEDED INDUCTANCE IN MICROHENRIES.*
      DISPLAY *PLEASE GIVE INPUT DATA FOR L,IP,BS,AND W BELOW.*
      DISPLAY *PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,*
      DISPLAY *   FC,FW,RHO IF ANY OF DEFAULTED SETTINGS IS*
      DISPLAY *   NOT DESIRED.*
      DISPLAY *NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
      DISPLAY *FOR THE ANSWERS AT THE END OF THE RUN,*
      DISPLAY *A IS CORE AREA, Z IS MEAN CORE LENGTH,*
      DISPLAY *N IS NUMBER OF TURNS,U IS PERMEABILITY,*
      DISPLAY *AZ IS PRODUCT OF A AND Z, AC IS CONDUCTOR AREA PER
      DISPLAY *TURN, P IS OPTIMUM INDUCTOR LOSS FOR A GIVEN W.*
      READ (5,B)
      WRITE (6,B)
      S=1+16.*FC*DC*FW/DI+(1+96.*FC*DC*FW/DI)**.5
   30 Q=.0789*(DI*DI*S/(FC*DC*FW))**.3333
      A=Q**(-2.)*W**.6667+0.01
      N=(10.*Q*Q/BS)*(L*IP/W**.667)
      U=7958.*(BS*BS/DI)*(1-(S/10.)*(1-16.*FC*DC*FW/(DI*S))**2)
C         *(W/(IP*IP*L))
      Z=1.257E-2*U*A*N*N/L
      AC=1.974E5*(W-DI*A*Z)/(4.*FC*DC*N*A**.5)
      AZ=A*Z
      P=4.*IP*IP*RHO*FC*N*A**.5/AC*1.974E7
      IF (U-0.) 10,10,20
   10 S=1+16.*FC*DC*FW/DI-(1+96.*FC*DC*FW/DI)**.5
      GO TO 30
   20 WRITE (6,1)A
    1 FORMAT(*A =*,E10.3,5X,*SQUARE CENTIMETERS*)
      WRITE (6,2)Z
    2 FORMAT(*Z =*,E10.3,5X,*CENTIMETERS*)
      WRITE (6,3)N
    3 FORMAT(*N =*,E10.3,5X,*TURNS*)
      WRITE (6,4)U
    4 FORMAT(*U =*,E10.3,5X,*GAUSS/OERSTED*)
      WRITE (6,5)AZ
    5 FORMAT(*AZ=*,E10.3,5X,*CUBIC CENTIMETERS*)
      WRITE (6,6)AC
    6 FORMAT(*AC=*,E10.3,5X,*CIRCULAR MILS*)
      WRITE (6,7)P
    7 FORMAT(*P =*,E10.3,5X,*WATTS*)
      END
```

Program Objective

User Instruction Part of the Program

Program

Output Format Specification

SAMPLE RUN

```
C RUN,I=INDOS3,G
 THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN
 OPTIMUM LOSS INDUCTOR DESIGN FOR A GIVEN WEIGHT.
 TO USERS: PLEASE READ THE FOLLOWING STATEMENTS
    CAREFULLY BEFORE EXECUTING THE PROGRAM.
 THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:
    DC : CONDUCTOR DENSITY IN GRAM/CUBIC CM.
           IF NOT GIVEN BY THE USER, DC IS SET
           AT 8.9 BY DEFAULT.
    DI : CORE DENSITY IN GRAMS/CUBIC CM.
           IF NOT GIVEN BY THE USER, DI IS SET
           AT 7.8 BY DEFAULT.
    FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE
           CORE CIRCUMFERENCE.
           IF NOT GIVEN, FC IS SET AT 2. BY DEFAULT.
    FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.
           IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.
    RHO:CONDUCTOR RESISTIVITY IN OHM-METER. IF
         NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT.
    W  : ALLOWED INDUCTOR WEIGHT IN GRAMS.
    BS : MAXIMUM FLUX DENSITY IN KILOGAUSSES.
    IP : PEAK INDUCTOR CURRENT IN AMPERES.
    L  : NEEDED INDUCTANCE IN MICROHENRIES.
 PLEASE GIVE INPUT DATA FOR L,IP,BS,AND W BELOW.
 PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,
    FC,FW,RHO IF ANY OF DEFAULTED SETTINGS IS
    NOT DESIRED.
 NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
 FOR THE ANSWERS AT THE END OF THE RUN,
 A IS CORE AREA, Z IS MEAN CORE LENGTH,
 N IS NUMBER OF TURNS,U IS PERMEABILITY,
 AZ IS PRODUCT OF A AND Z, AC IS CONDUCTOR AREA PER
 TURN, P IS OPTIMUM INDUCTOR LOSS FOR A GIVEN W.
  $B
? L=200.,IP=4.5,BS=3.5,W=60.85$
? $
$
 $B
 DC       = 8.9,
 DI       = 7.8,
 FC       = 2.0,
 FW       = 4.0E-01,
 RHO      = 1.724E-08,
 W        = 6.085E+01,
 BS       = 3.5,
 IP       = 4.5,
 L        = 2.0E+02,
 $END
A = 6.954E-01     SQUARE CENTIMETERS
Z = 6.342E+00     CENTIMETERS
N = 3.693E+01     TURNS
U = 1.064E+02     GAUSS/OERSTED
AZ= 4.410E+00     CUBIC CENTIMETERS
AC= 2.381E+03     CIRCULAR MILS
P = 7.130E-01     WATTS
```

Computer Printout of User Instruction

User's Input

Printout of User Input Summary

Printout of Calculated Output

ORIGINAL PAGE IS OF POOR QUALITY

APPENDIX M

FORMULATION OF A METHODOLOGY FOR POWER CIRCUIT DESIGN OPTIMIZATION

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ABSTRACT

A power processing optimization methodology is established to effectively conceive a design, to meet all requirement specifications and concurrently optimize a given design quantity deemed particular desirable. Such a quantity can be the weight, efficiency, regulator response, or any other physically-realizable entity. Four design examples are given to demonstrate the methodology. The method of Lagrange multipliers is applied to three examples to acquire optimum solutions are not closed form. When closed-form solutions are not amendable in the other example, a nonlinear programming algorithm is used to conceive the optimum design numerically. Areas of future investigations are outlined to foster the power processing optimization into its ultimate maturity.

1. INTRODUCTION

Partially due to the traditional supporting role it serves in relation to other seemingly more glamorous technology areas, and partially due to its own rapidly evolving nature, power processing technology has been hampered by a lack of rigorous design, modeling, and optimization techniques. As a result, empirical and intuitive reliances often intercede with the designer's desire to be "more scientific" and his commitment of being "on schedule". Handicapped by a general lack of established design,analysis, and optimization tools, the tendency has been for a designer to become competent in dealing with a certain particular circuit approach, rather than to be familiar with other available approaches and the optimization techniques which can be used to identify the optimum design for a given set of specification requirements. Such inadequacies invariably lead to penalties involving equipment weight, efficiency, or other performances. In view of the forthcoming needs for use of considerable higher level of power and the severe penalties that may be incurred in the absence of useful design and tradeoff tools, the need for establishing a design optimization methodology has become increasingly evident.

To be specific, the utility of the design optimization is that it will not only pinpoint the detailed power processor design to meet given specifications, but also achieve the optimization with respect to a certain power-processor characteristic deemed particularly desirable by the designer. The characteristic can be the weight, the efficiency, or any other realizable entity of the power processor. While power processing as a technology has reached a level of sophistication where the analysis and optimization of these characteristics should have been well established, a survey of existing literatures has proven the contrary.

In the following sections, the power processing design optimization effort is first surveyed. The methodology entailed in this work is then described. Design optimization examples are provided to demonstrate the methodology. Starting with simple problems admitting closed-form optimum solutions,examples of ascending complexity are presented for which the use of nonlinear programming algorithms becomes necessary in achieving numerically the intended optimization. Prior to the conclusion, areas of future investigations are briefly discussed to outline the ingredients needed to foster the power processing design optimization into its ultimate maturity.

2. EXISTING POWER PROCESSING OPTIMIZATION

Since power magnetics represent a major portion of the total power processor weight whenever switching regulators and input/output filters are used, it is to be expected that optimization of magnetics design has received considerable attention.[1,2,3] However, most of these studies assume the use of a certain conductor size for a given current(e.g., 1000 circular mils per ampere); the design is reduced to the development of a search routine to select the optimum core configuration. Closed-form solutions for optimum core parameters are not derived. As a consequence, weight-loss tradeoff is only possible through the parametric-data approach.[4]

*This work was performed under Contract NAS3-19690,"Modeling and Analysis of Power Processing Systems," by TRW Systems, Redondo Beach, CA, for NASA Lewis Research Center.

Beyond the magnetics design, optimization study on power processors seems to be quite rare in view of the vast power and control circuit development.

As far as the power circuit is concerned, attempts have been made to accumulate the parametric data of functional designs (input filters, inversion and rectification, output filters, etc.) within a converter in order to identify an optimum overall converter design.[5] Primarily due to the lack of proper modeling for the individual functions as well as the inability to mathematically incorporate the interdependences existing among the functions, the attempts have failed. A manifestation of this failure is the current inability of a power circuit designer to determine an optimum converter switching frequency that will minimize the converter loss (weight) for a given converter weight (loss).

When power and control circuits are combined to form a switching regulator, the regulator steady-state and dynamic performances add significantly to the complexity of design optimization far beyond that of the power circuit alone. Although a computer nonlinear programming technique was utilized to conceive the design of a hysteresis-controlled self-oscillating regulator [6], practically all existing performance optimization has been confined to breadboard experimentation and computer simulation. However, with the recent availability of power and control circuit models [7,8,9,10], analytical optimization of regulator performances such as stability and dynamic response has for the first time become a distinct possibility.

As the power processing modeling and analysis gradually approaches its full development, the trend for power processing optimization is likely to open an area of most zealous research. It is for the promotion of this trend that the following optimization methodology and examples are formulated.

3. POWER PROCESSING OPTIMIZATION METHODOLOGY

A methodology is formulated here to apply the optimization theory in achieving non-iterative optimum design of power processing circuits. Simply stated, the task is to minimize an objective function $f(x,k)$, subject to design constraints $g_j(x,k,r)=0$.

Here, $x = (x_1, x_2, \ldots x_n)^T$ is a n-dimensional vector representing circuit parameters to be determined. Examples of x include the values of R, L, and C, the operating frequency, and the design details of magnetic components including the effective core area, the mean core length, the permeability, the wire size, and the number of winding turns.

The k's represent various constants known from common knowledge or designer's experience.

Examples include copper resistivity, core and winding densities, core window fill factor, saturation flux density, capacitor energy-storage capabilities, etc.

The r's are requirement specifications which the optimum design must meet. Examples include filter attenuation, output ripple amplitude, maximum weight, minimum efficiency, source EMI, etc. These requirements are usually prescribed to the power processor designer by someone presumably knowledgeable in the entire power system.

The function $f(x,k)$ is the particular power processor characteristic to be optimized. Examples include the total weight, the total loss, the dynamic response, the figure of merit of a specific design, or any other preferrable design quantity such as reliability and cost.

Equation $g_j(x,k,r) = 0$ represent a total of "j" design constraints relating x, k, and r. For example, one of the equations may relate the filter attenuation required at a given frequency to the RLC filter parameters, and a second equation may relate the output-ripple amplitude to the LC output filter, the ESR of C, the switching frequency, the input and output converter voltages, and the output power. Still another equation may relate the sum of all losses to the required efficiency. The number of constraints will be sufficiently large to allow all requirements "r" and all constants "k" to find their ways into governing the design of all circuit parameters "x". Consequently, solutions acquired for equations $g_j(x,k,r) = 0$ to minimize the objective function $f^j(x,k)$ would authentically portray a detailed optimum design, down to the component level, in accordance with the requirements and the optimization objective specified.

4. METHODOLOGY IMPLEMENTATION

From the foregoing description, the key to implementing the methodology rests on suitable mathematical or computer techniques that can be used to solve the simultaneous constraints and concurrently minimize the objective function.

As shown in the optimization examples to be presented later, the nature of the power processor design often leads to highly nonlinear constraints and objective function, thus rendering the well-coded linear programming techniques inapplicable.

While the theory regarding nonlinear constrained optimization has been well developed, only few problems with rather simplistic nature can be solved in closed form. Most larger problems arising from practical applications are sufficiently complicated that, to identify their optimum solutions one has to resort to computational means.

4.1 Optimization Theory Using Lagrange Multipliers

Quite amendable to generalization, optimization theory in terms of Lagrange multipliers [11] provides a practical method in seeking an extremum for objective function $f(x,k)$, subjecting to a total of "j" nonlinear constraints

$$g_j(x,k,r) = 0 , \qquad (1)$$

where x is a n-dimensional vector. The method proceeds by first forming a function F, where

$$F = f + \Sigma h_j g_j \qquad (2)$$

Here, the h_j's are Lagrange multipliers independent of x's.

Next, for function F to have an extremum, the requirement is:

$$\frac{\partial F}{\partial x_i} = \frac{\partial f}{\partial x_i} + h_1 \frac{\partial g_1}{\partial x_i} + \ldots + h_j \frac{\partial g_j}{\partial x_i} = 0$$

$$i = 1, 2, \cdots n . \qquad (3)$$

Between equations (1) and (3), there are a total of (j+n) equations, which can be used to solve the "n" unknown variables x_1 to x_n and the "j" unknown multipliers h_1 to h_j.

Application of this method to simple power processing optimization problems occasionally yields closed-form solutions. Three such examples are given in Section 5.

4.2 Nonlinear Programming Techniques Using Penalty Functions

The key to nonlinear programming is an algorithm that enables optimum numerical solutions to be reached, with fast convergence, from an initial guess of the solutions. Since the effectiveness of a given nonlinear programming technique is invariably affected by the global and local properties of a multi-dimensional problem to which the technique is applied, the unfortunate consequence is that there is no uniformly good method on which an algorithm can be based to handle satisfactorily most optimization problems.

From the numerous existing methods of nonlinear programming, two popular ones were selected to test their utilities in power processor optimizations: the method of reduced gradient [12] and the method of penalty functions [13]. The particular codes used to implement these two approaches are, respectively, the Generalized Reduced Gradient (GRG) and the Sequential Unconstrained Minimization Technique (SUMT). [14,15] Based solely on our application experience to date, both codes handle simple power processing optimization problems equally well, but the SUMT seems to have a distinct edge in achieving convergence for more complicated problems. Consequently, the SUMT code, which is a notable member of the penalty function class of algorithms, is used in the demonstration examples shown in Section 5.

At this juncture, a note is in order to clarify the meaning of the penalty function. A penalty function is one which, when added to the original objective function to form a penalized objective function, will detract from achieving a minimum objective when an associated constraint is violated. A particular useful penalty function used in the SUMT code is thus the quadratic form of $g_j(x,k,r)$, which results in the formulation of the following equation:

$$f_p(x,k) = f(x,k) + c \sum_{j=1}^{j} [g_j(x,k,r)]^2 \qquad (4)$$

Here, $f(x,k)$ is the original objective function, $f_p(x,k)$ is the penalized objective function, c is a positive weighing coefficient when a minimum of $f_p(x,k)$ is desired, and $g_j(x,k,r) = 0$ are the nonlinear equality constraints. From eq.(4), it is apparent that the constrained minimum of $f(x,k)$ subject to constraints $g_j = 0$ is identical to unconstrained minimum of $\lim_{c\to\infty} f_p(x,k)$.

The SUMT code thus accomodates the initial "c", the conditions under which "c" is to be increased, and the criterion of bypassing the increasing "c" when the minimization procedure has run its course.

Before leaving for power circuit optimization examples, the following important considerations are stated:

(1) Notice that the penalty-function method of seeking numerical solutions does not represent an extension of the theory of Lagrange multipliers presented in Section 4.1. Despite its sound theoretical background, the Lagrange multipliers method is less attractive, in general, from the computational viewpoint, as the number of search parameters is increased by the number of Lagrange multipliers.

(2) Since most SUMT subroutines are written in FORTRAN IV, the program can be run on any large computer with a Fortran compiler. However, being primarily a research tool, the user generally needs to experiment with SUMT in order to realize all its capabilities as well as its limitations.

(3) Given a specific search algorithm, one can generally find an objective function and a set of constraints for which the given algorithm performs best. This characteristic makes it difficult to compare objectively the general merits of different algorithms. The fact that SUMT has provided a better performance than GRG in our application does in no way imply its overall superiority over other codes. The production of a technique applicable to solve efficiently all nonlinear programming problems is not in sight, at least not in the near future.

5. DEMONSTRATION EXAMPLES

Four examples of power processing optimization kkk

are presented to demonstrate the methodology previously described. They are:

(1) Optimum-weight core selection for an inductor, with winding size predetermined.

(2) Optimum-weight inductor design with a given loss constraint.

(3) Optimum-loss inductor design with a given weight constraint.

(4) Comparison of optimum-weight single-stage and two-stage input filter design with identical loss and other requirement constraints.

The nature of the first three examples are such that they admit closed-form solutions based on the application of Lagrange multiplier method. The solutions of the other one, however, are acquired numerically through the use of the SUMT program.

Before presenting the examples, it is convenient to recall that $f(x,k)$ is the objective function, and $g_j(x,k,r) = 0$ are constraints. The k's represent all known constants needed for the design, the r's are requirement specifications which the optimum design must meet, and the x's are optimum circuit and component parameters to be determined.

Example 1 Optimum-Weight Inductor Core Selection

Quite often in actual inductor design, the designer wishes to identify a core to achieve a certain inductance and to accomodate all windings for which the conductor size of each turn has been predetermined either intuitively or empirically. In this case, one is not interested in an optimum design strictly from a fixed-loss-minimum-weight or a fixed-weight-minimum-loss standpoint. All that is wanted is the selection of a core that is just right, i.e., it is neither too small nor too large for the application.

In this design, the following parameters are needed:

Known Constants k's

- A_c: Predetermined cross-sectional area of one turn conductor
- B_s: Saturation flux density of the core
- D_c: Conductor density
- D_i: Iron core density
- F_c: Ratio of one turn condcutor average length to core circumference
- F_W: The proportion of core window area actually occupied by the conductor when the window is filled

Given Requirements r's.

- L : Inductance needed
- I_p: Peak current in the inductor winding

Unknown Variables x's

- A : Core cross-sectional area
- N : Number of turns
- Z : Mean length of core
- μ : Permeability of core

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Constraint Equations g_j's

All magnetic core flux capability is utilized:

$$B_sNA - LI_p = 0 \tag{5}$$

All window area of the toroid core is occupied:

$$(NA_c/\pi F_W)^{1/2} - (Z/2\pi) + (\sqrt{A}/2) = 0 \tag{6}$$

In deriving eq.(6), a core with a square cross-sectional area A is assumed so that the circumference of the core becomes $4\sqrt{A}$.

Objective Function f(x,k)

Let the total inductor weight be W, then,

$$\begin{aligned} W = f(x,k) &= \text{conductor weight} + \text{core weight} \\ &= 4F_cD_cA_cN\sqrt{A} + D_iAZ \end{aligned} \tag{7}$$

Having identified the problem, it is recalled that the objective here is to find solutions for the x's so that W of eq.(7) is minimized and at the same time eqs. (5) and (6) are satisfied. Unless otherwise specified, the use of international metric system units is assumed.

Substituting x_1 for $\sqrt{A}$, x_2 for $\sqrt{N}$, and x_3 for Z, eqs. (5) to (7) become, respectively,

$$g_1(x,k,r) = B_sx_2^2x_1^2 - LI_p = 0 \tag{8}$$

$$g_2(x,k,r) = \sqrt{\frac{A_c}{\pi F_W}}\, x_2 - \frac{x_3}{2\pi} + \frac{x_1}{2} = 0 \tag{9}$$

$$f(x,k) = 4F_cD_cA_cx_2^2x_1 + D_ix_1^2x_3 \tag{10}$$

Using the method of Lagrange multipliers described in Section 4.1, eq.(2) becomes:

$$F = 4F_cD_cA_cx_2^2x_1 + D_ix_1^2x_3 - h_1(B_sx_2^2x_1^2 - LI_p) - h_2[(A_c/\pi F_W)^{0.5}x_2 - (x_3/2\pi) + (x_1/2)] \tag{11}$$

As prescribed in eq.(3), partial differentiation of eq.(11) with respect to x_i gives:

$$\frac{\partial F}{\partial x_1} = 4F_cD_cA_cx_2^2 + 2D_ix_1x_3 - 2h_1B_sx_2^2x_1 - (h_2/2) = 0 \tag{12}$$

$$\frac{\partial F}{\partial x_2}=8F_cD_cA_cx_1x_2-2h_1B_sx_2x_1^2-h_2(A_c/\pi F_w)^{0.5}=0 \qquad (13)$$

$$\frac{\partial F}{\partial x_3}=D_ix_1^2+(h_2/2\pi) = 0 \qquad (14)$$

From the five equations (8), (9), (12), (13), and (14), the five unknowns x_1 to x_3 and h_1 to h_2 can be solved.

Solutions of h_1 and h_2 are irrelevant to the inductor design. The relevant ones are:

$$A=x_1^2= (1/3)(LI_pA_c/B_s\pi F_w)^{1/2}S \qquad (15)$$

$$N=x_2^2= 3(LI_p\pi F_w/A_cB_s)^{1/2}\ S^{-1} \qquad (16)$$

$$Z=x_3=(2\sqrt{3}\ \pi)(LI_pA_c/B_s\pi F_w)^{1/4}(S^{-1/2}+\frac{S^{1/2}}{6}), \qquad (17)$$

where

$$S=(1+\frac{12F_cF_wD_c}{D_i})^{1/2} - 1 . \qquad (18)$$

From eqs.(15) to (18), the permeability and the weight of the inductor can be derived as:

$$\mu=(2\pi/\sqrt{3})(B_s/I_p)^{5/4}(A_c/\pi F_w)^{3/4}L^{-1/4}S(S^{-\frac{1}{2}}+\frac{S^{\frac{1}{2}}}{6}) \qquad (19)$$

$$W=(2\pi D_c/\sqrt{3})(LI_pA_c/\pi B_sF_w)^{3/4}S^{-1/2}\cdot [6F_cF_w+(D_i/D_c)(S+\frac{S^2}{6})]. \qquad (20)$$

Equations (15) to (20) illustrate the particular set of A, N, Z, and μ that will produce the minimum combined copper and iron weight of an inductor with inductance L, peak winding current I_p, conductor cross-sectional area A_c, saturation flux density B_s, winding factor F_w, pitch factor F_c, and specific densities D_c for the conductor and D_i for the core. In these equations, A and Z are in square meters and meters respectively, W is in kilograms, and μ is in Weber/Ampere-Turn-Meter. To convert μ into Gauss/Oersted, eq.(19) is divided by a factor $4\pi \times 10^{-7}$.

To demonstrate the utility of these equations, the following constants are assumed for the molypermalloy-powder-core inductor:

$F_w = 0.4$, $F_c = 2$, $B_s= 0.35$ Weber/meter^2, $D_c = 8900$ kg/m^3, and $D_i= 7800$ kg/m^3.

Using these constants and making the necessary conversions to the more familiar engineering units, then, with L expressed in microhenries, I_p in amperes, and A_c in circular mils, equations (15) to (20) become:

$A = 2.8\times 10^{-4}(LI_pA_c)^{1/2}$	cm^2	(21)
$N = 103\ (LI_p/A_c)^{1/2}$	turns	(22)
$Z = 0.18(LI_pA_c)^{1/4}$	cm	(23)
$\mu = 6.1(I_p)^{5/4}(L)^{-1/4}(A_c)^{3/4}$	Gauss/Oersted	(24)
$W = 0.001(LI_pA_c)^{3/4}$	grams.	(25)

Notice that once L, I_p, and A_c are known, the inductor weight is determined from eq.(25) without the need for actually designing the inductor.

Example 2 Optimum -Weight Inductor Design Subjecting to a Given Loss Constraint

This example deals with the design of an iron core inductor to be used in an input filter. The allowed loss for the inductor is given as a constraint. The inductor current is assumed to be essentially dc, thus producing negligible iron loss. The results obtained here are of considerable practical significance; the results define in closed form the optimum-weight magnetics design parameters including core area, mean length, permeability, winding size, and number of turns once the loss in the inductor is given. Furthermore, the optimum inductor weight for a given loss is known directly without even designing the inductor.

Known Constants k's

P : Power loss allowed in the inductor

B_s: Saturation flux density

ρ : Resistivity of the conductor

D_c, D_i, F_c, and F_w are identical to Example 1.

Given Requirements r's

I_{dc}: dc current in the inductor

L : Inductance

Unknown Variables x's

A_c: Conductor size

A, N, Z, and μ are identical to Example 1.

Constraint Equations g_j's

Equations (26) and (27) are identical to eqs. (5) and (6):

$$B_sNA - LI_{dc} = 0 \qquad (26)$$

$$\sqrt{\frac{A_cN}{\pi F_w}} - \frac{Z}{2\pi} + \frac{A^{1/2}}{2} = 0 \qquad (27)$$

In addition, the copper loss in the inductor is:

$$P - (4I_{dc}{}^2 \rho F_c N \sqrt{A} / A_c) = 0. \tag{28}$$

<u>Objective Function f(x,k)</u>

$$W = 4F_c D_c A_c N \sqrt{A} + D_i AZ. \tag{29}$$

Substituting x_1 for $\sqrt{A}$, x_2 for $\sqrt{N}$, x_3 for Z, and x_4 for $\sqrt{A_c}$, setting up function F of eq. (2), and differentiating F with respect to x_1, x_2, x_3, and x_4 yield the following seven equations:

$$B_s x_1{}^2 x_2{}^2 - LI_{dc} = 0 \tag{30}$$

$$\sqrt{1/\pi F_w}\, x_2 x_4 - (x_3/2\pi) + (x_1/2) = 0 \tag{31}$$

$$P - (4I_{dc}{}^2 \rho\, F_c x_2{}^2 x_1 / x_4{}^2) = 0 \tag{32}$$

$$4F_c D_c x_4{}^2 x_2{}^2 + 2D_i x_1 x_3 - 2h_1 B_s x_2{}^2 x_1 - (h_2/2) + (4I_{dc}{}^2 \rho F_c x_2{}^2 h_3 / x_4{}^2) = 0 \tag{33}$$

$$8F_c D_c x_4{}^2 x_2 x_1 - 2h_1 B_s x_2 x_1{}^2 - (1/\pi F_w)^{1/2} h_2 x_4 + (8h_3 I_{dc}{}^2 \rho F_c x_2 x_1 / x_4{}^2) = 0 \tag{34}$$

$$D_i x_1{}^2 + (h_2/2\pi) = 0 \tag{35}$$

$$8F_c D_c x_4 x_2 x_1 - (1/\pi F_w)^{1/2} h_2 - (8I_{dc}{}^2 \rho F_c h_3 x_2 x_1 / x_4{}^3) = 0. \tag{36}$$

Solving for A, N, Z, and A_c, it can be shown that the following closed-form solutions exist:

$$A = 16(\rho D_c F_c{}^4 / B_s{}^2 \pi D_i)^{2/5} (S)^{-4/5} (I_{dc}{}^4 L^2/P)^{2/5} \tag{37}$$

$$N = (1/16)(\pi^2 D_i{}^2 / D_c{}^2 B_s \rho^2 F_c{}^8)^{1/5} (S)^{4/5} \cdot (LP^2/I_{dc}{}^3)^{1/5} \tag{38}$$

$$\begin{aligned} Z &= [(1/2)(\pi^8 D_i{}^3 \rho^2 / F_w{}^5 D_c{}^3 B_s{}^4 F_c{}^7)^{1/10} (S)^{3/5} \\ &\quad + 4(\rho \pi^4 F_c{}^4 D_c / B_s{}^2 D_i)^{1/5} (S)^{-2/5}] (I_{dc}{}^4 L^2/P)^{1/5} \\ &\triangleq T(I_{dc}{}^4 L^2/P)^{1/5} \end{aligned} \tag{39}$$

$$A_c = (\pi D_i F_c \rho^4 / D_c B_s^3)^{1/5} (S)^{2/5} (I_{dc}{}^{11} L^3/P^4)^{1/5}. \tag{40}$$

where T represents the quantity in the bracket on the right-hand side of eq.(39), and S is:

$$S = (D_i F_c / D_c F_w)^{1/2} + [(D_i F_c / D_c F_w) + 96F_c^2]^{1/2} \tag{41}$$

From these equations, one can obtain:

$$\mu = 16(D_c B_s^3 \rho F_c^4 / \pi D_i)^{2/5} (T)(S)^{-4/5} (I_{dc}^2 L/P^3)^{1/5} \tag{42}$$

$$W = [(\pi^2 D_i^2 D_c^3 \rho^3 F_c^2 / B_s^6)^{1/5} (S)^{4/5} + 16(\rho F_c^4 D_c D_i^{3/2} / B_s^2 \pi)^{2/5} (S)^{-4/5} (T)] (L^6 I_{dc}^{12}/P^3)^{1/5} \tag{43}$$

Several significant characteristics exposed by these equations are:

(1) For a given core material, the minimum weight expressed in eq.(43) can be calculated directly from the inductance L, the dc current I_{dc}, and the loss limit P, without attending to the design details of the inductor.

(2) For a given loss, the inductor weight is proportional to $(LI_{dc}^2)^{6/5}$, but is inversely proportional to $P^{3/5}$.

(3) The two terms in the bracket on the right-hand side of eq.(43) represent the conductor and core weight, respectively. Since they are both proportional to the same quantity $(I_{dc}{}^{12} L^6/P^3)^{1/5}$, there is one, and only one, optimum weight design for a given loss. Varying the conductor-to-core proportion in an alternate design would only result in a heavier inductor.

Using powder cores as an example, the following parameters can be assumed without losing much of the generality:

$B_s = 0.35$ W/m^2, $D_c = 8900$ kg/m^3
$D_i = 7800$ kg/m^3, $\rho = 1.724\times10^{-8}$ ohmmeter
$F_c = 1.9$, $F_w = 0.42$

Substituting these parameters into eqs.(37) to (43) and making necessary unit conversions for engineering convenience, one has:

$$A = 0.00076(I_{dc}^4 L^2/P)^{2/5} \quad \text{cm}^2 \tag{44}$$

$$N = 37.6(LP^2/I_{dc}{}^3)^{1/5} \quad \text{turns} \tag{45}$$

$$Z = 0.21(I_{dc}^4 L^2/P)^{1/5} \quad \text{cm} \tag{46}$$

$$A_c = 2.68(I_{dc}^{11} L^3/P^4)^{1/5} \quad \text{cir. mils} \tag{47}$$

$$\mu = 15.6(I_{dc}^2 L/P^3)^{1/5} \quad \text{Gauss/Oersted} \tag{48}$$

$$W = 0.0022(I_{dc}^{12} L^6/P^3)^{1/5} \quad \text{grams} \tag{49}$$

In these equations, I_{dc} is in amperes, L is in microhenries, and P is in watts.

Example 3 Optimum-Loss Inductor Design Subjecting to a Given Weight Constraint

In addition to the two constraints identical to eqs.(26) and (27) concerning the flux capability and the full window, a third constraint is that of weight W, where

$$W - 4F_cD_cNA_c\sqrt{A} - D_iAZ = 0, \qquad (50)$$

The objective function is the loss,

$$P = 4I_{dc}^2\rho F_cN\sqrt{A} / A_c, \qquad (51)$$

Performing similar manipulations as Example 2, the following closed-form solutions can be obtained after rather laborious derivations:

$$A = M^{-2}W^{2/3} \qquad (52)$$

$$N = M^2(1/B_s)(LI_{dc}/W^{2/3}) \qquad (53)$$

$$A_c=(B_sF_w/25D_i^2\pi)(2M-5\pi D_iM^{-2})^2(W^{4/3}/LI_{dc}) \qquad (54)$$

$$Z=(1/D_i)[M^2-(S/40)(2M-5\pi D_iM^{-2})^2]\ W^{1/3} \qquad (55)$$

$$\mu=(B_s^2/D_i)[1-(S/10)(1-\frac{16F_cD_cF_w}{D_iS})^2](W/I_{dc}^2L) \qquad (56)$$

$$P=(25\rho F_cD_i^2\pi/B_s^2F_wM)\left(\frac{1}{1-\frac{16F_cD_cF_w}{D_iS}}\right)^2(L^2I_{dc}^4/W^{5/3}), \qquad (57)$$

where

$$M = (5\pi D_i^2S/32F_cD_cF_w)^{1/3} \qquad (58)$$

$$S = 1+(16F_cD_cF_w/D_i) \pm \sqrt{1+(96F_cD_cF_w/D_i)}, \qquad (59)$$

Here, A and A_c are in meter^2, Z is in meters, μ is in Weber/amp-turn-meter, P is in watts, W is in kilograms, L is in henries, I_{dc} is in amperes, B_s is in weber/meter^2, and D_i and D_c are in kilograms per meter^3.

Notice the plus and minus sign in eq.(59). Only that which will produce positive Z, P, and μ will be chosen for S in eq.(59). Using the powder core for illustration with the following numerical inputs:

B_s = 0.35 Weber/m^2	L = 225x10^{-6}	Henry
D_c = 8900 kg/m^3	W = 50x10^{-3}	kilogram
D_i = 7800 kg/m^3	ρ = 1.724x10^{-8}	ohm-meter
F_c = 2, F_w = 0.4	I_{dc}=4	amperes,

the following simplified equations are obtained:

$A = 0.045\ W^{2/3}$	cm^2	(60)
$N = 0.635(LI_{dc}/W^{2/3})$	turns	(61)
$Z = 1.617\ W^{1/3}$	cm	(62)
$\mu = 7100\ (W/I_{dc}^2L)$	Gauss/Oersted	(63)
$P = 4.124\times10^{-5}(L^2I_{dc}^4/W^{5/3})$	Watts	(64)
$A_c = 8881(W^{4/3}/LI_{dc})$	cir. mils	(65)

In equations (60) to (65), W, L, I_{dc} are in grams, microhenries, and amperes, respectively.

Example 4 Comparison of Optimum-Weight Input Filter Design Using Single-Stage and Two-Stage Filters

In this example, the optimum-weight designs of two different input-filter configurations are compared to assess their relative utility. The first configuration is a conventional LC filter shown in Figure 1, where R is the winding resistance of L. The second configuration shown in Figure 2 is a two-stage filter [16], in which R1 and R2 are the winding resistance of L1 and L2, R3 is the lumped sum of ESR of C1 and a much higher external resistance added in series with C1, and C2 is a high-quality capacitor with negligible ESR. The advantage of the two-stage filter is that while a high efficiency can be maintained through the use of C2 in the second stage to handle most of the switching current, the resonant peaking of the entire filter is being controlled by the external resistance R3 in the first stage. During normal operations, the current in C1 is negligible.

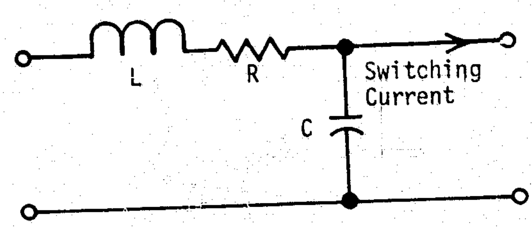

Figure 1 A Single-Stage Filter

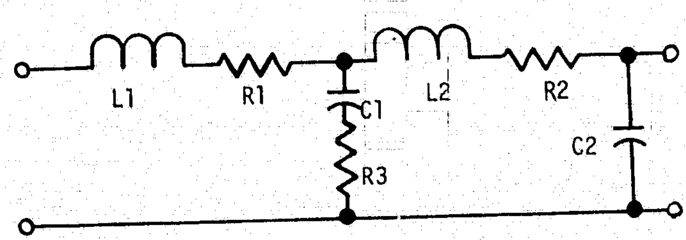

Figure 2 Two-Stage Filter

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Known Constants k's

B_s: Identical saturation flux density assumed for L, L1, and L2

K_c: Capacitor weight per farad of capacitance for C. For a given voltage rating and case size, the weight of the capacitor is divided by the highest capacitance of that case size to arrive at a value for K_c.

K_{c1}: Capacitor weight per farad of capacitance for C1.

K_{c2}: Capacitor weight per farad of capacitance for C2

D_c, D_i, F_c, F_w, and ρ are identical to Example 1, and are assumed to be the same for L, L1, and L2.

Given Requirements r's

B : Resonant peaking limit for the filter of Figure 1

B_1 : Resonant peaking limit for the first stage filter of Figure 2

B_2 : Resonant peaking limit for the second stage filter of Figure 2

F : Frequency of the switching current

G : Attenuation required at frequency F

I_{dc}: Dc current in the inductors

P : Power loss allowed

The last four requirements are assumed identical for both filters to facilitate a realistic comparison.

Unknown Variables x's

The variables for the filter of Figure 1 are:

A, N, Z, A_c, L, C, R

$(R = P/I_{dc}^2)$

The variables for the filter of Figure 2 are:

$A_1, N_1, Z_1, A_{c1}, L_1, C_1, R_1$

$A_2, N_2, Z_2, A_{c2}, L_2, C_2, R_2, R_3$

$(R_1 + R_2 = P/I_{dc}^2)$

Constraint Equations g_j's

Five constraints exist for Figure 1:

No Saturation:

$$B_s NA - LI_{dc} = 0 \quad (66)$$

Full Window:

$$(NA_c/\pi F_w)^{1/2} - (Z/2\pi) + (\sqrt{A}/2) = 0 \quad (67)$$

Loss Limit:

$$(4\rho F_c N\sqrt{A}/A_c) - (P/I_{dc}^2) = 0 \quad (68)$$

Resonant Peaking Limit:

$$L - CB^2R^2 = 0 \quad (69)$$

Required Attenuation:

$$(1 - 4\pi^2F^2LC)^2 + 4\pi^2F^2R^2C^2 - G^{-2} = 0 \quad (70)$$

Eight constraints exist for Figure 2:

No Saturation For L1 and L2:

$$B_s N_1 A_1 - L_1 I_{dc} = 0 \quad (71)$$

$$B_s N_2 A_2 - L_2 I_{dc} = 0 \quad (72)$$

Full Window For L1 and L2:

$$(N_1 A_{c1}/\pi F_w)^{1/2} - (Z_1/2\pi) + (\sqrt{A_1}/2) = 0 \quad (73)$$

$$(N_2 A_{c2}/\pi F_w)^{1/2} - (Z_2/2\pi) + (\sqrt{A_2}/2) = 0 \quad (74)$$

Loss Limit:

$$4\rho F_c[(N_1\sqrt{A_1}/A_{c1}) + (N_2\sqrt{A_2}/A_{c2})] - (P/I_{dc}^2) = 0 \quad (75)$$

Resonant Peaking At First Stage Filter:

$$\frac{1 + \dfrac{L_1}{C_1 R_3^2}}{\left(\dfrac{C_2}{C_1}\right)^2 + \dfrac{L_1}{C_1 R_3^2}\left(1 - \dfrac{C_2}{C_1} - \dfrac{L_2 C_2}{L_1 C_1}\right)^2} - B_1^2 = 0 \quad (76)$$

Resonant Peaking At Second Stage Filter:

$$(L_2/L_1) - B_2 = 0 \quad (77)$$

Required Attenuation:

$$G = \frac{1}{\dfrac{L_2 C_2}{L_1 C_1}\left(\dfrac{F}{f_1}\right)^3 \dfrac{R_3}{(L_1/C_1)^{1/2}} - \dfrac{C_2}{C_1}\left(\dfrac{F}{f_1}\right)^2} \quad (78)$$

where f_1 is the first stage resonant frequency:

$$f_1 = 1/[2\pi(L_1 C_1)^{1/2}] \quad (79)$$

Objective Functions f(x,k)

The weight for the filter of Figure 1 is:

$$W = 4F_c D_c A_c N\sqrt{A} + D_i AZ + K_c C \quad (80)$$

The weight for the filter of Figure 2 is:

$$W = 4F_c D_c(A_{c1}N_1\sqrt{A_1} + A_{c2}N_2\sqrt{A_2}) + D_i(A_1 Z_1 + A_2 Z_2) + K_{c1}C_1 + K_{c2}C_2 \quad (81)$$

+ Negligible weight for R3

To obtain the optimum design for Figure 1, notice that in eqs.(69) and (70) all parameters are given except for L and C. Thus L and C are solved directly, from which the capacitor weight $K_c C$ is known. Furthermore, eqs.(66) to (68) are identical to those of Example 2, where a closed-form expression for optimum inductor weight is already available from eq.(43). Consequently, the minimum filter weight is derived without resorting to SUMT. Assuming the following:

B_s	= 0.35	Weber/m^2	D_c = 8900	kg/m^3
F_c	= 1.9		D_i = 7800	kg/m^3
F_w	= 0.42		B = 2	(6 db)
ρ	= 1.724×10^{-8}	ohmmeter	G = 0.002	
F	= 20	kHz	P = 0.6	Watts
I_{dc}	= 3	Amp	K_c = 372	kg/Farad

Then, it can be found from eqs.(69) and (70) that

L = 23.7	μH		C = 1335	μF

Equation (49) thus gives

$$W = 0.0022(I_{dc}{}^{12}L^6/P^3)^{1/5} + K_cC$$

$$= 1.9 + 497 = 499 \text{ grams}$$

The overwhelming portion of the total weight is contributed by the capacitor. The large capacitance is needed to meet the prescribed resonant peaking B and power loss limit P.

As for Figure 2, the closed-form solutions for L1,L2,C1,C2, etc., are unattainable. The optimum filter weight must be obtained numerically from SUMT. Using the same constants given in Example 1 and assuming

K_{c1} = 372 kg/Farad, and K_{c2} = 2600 kg/Farad

for foil tantalum and polycarbonate capacitors respectively, the SUMT processing gives the following optimum design:

A_1	= 0.70	cm^2	A_2	= 0.138	cm^2
N_1	= 30	turns	N_2	= 51	turns
Z_1	= 6.38	cm	Z_2	= 6.33	cm
A_{c1}	= 2919	cir. mils	A_{c2}	= 3257	cir. mils
L_1	= 309	μH	L_2	= 103	μH
C_1	= 75	μF	C_2	= 20	μF
R_1	= 0.0237	ohm	R_2	= 0.0159	ohm
μ_1	= 249	Gauss/Oer.	μ_2	= 145	Gauss/Oer.
R_3	= 2.12	ohm	W	= 171	grams.

Notice the smaller W of Figure 2 filter as compared with that of Figure 1, thus demonstrating the lighter optimum weight of the two-stage filter in relation to its single-stage counterpart when they are designed to meet identical peaking, attenuation, and efficiency requirements. The difference in weight will increase (decrease) with a lower (higher) allowance on either the resonant peaking or the power loss for a given attenuation requirement.

6. FUTURE INVESTIGATIONS

Through the demonstration examples, the objective of establishing a power processing optimization methodology is achieved. However, like any other emerging branch within the modeling and analysis of power processing, the optimization application can only grow into a future state of maturity with constant enhancememt from efforts of research and development. Imminent future investigation should include, but not limit to, the following areas:

(1) Without an accurate model for power component losses, the application of optimization principle to weight-loss study is of dubious value. Loss elements such as (A) core loss as a function of frequency, flux density, and excitation waveform, and (B) semiconductor switching losses as related to various magnetics-semiconductor hybrid circuits and energy recovery schemes, must be authentically depicted to achieve a meaningful optimization.

(2) The four examples given in Section 5 contain only constraints which do not include requirements involving feedback control such as regulator stability, output impedance, and audio susceptibility. However, with the recent availability of switching-regulator models [7,8,9,10], the inclusion of these requirements as constraints for the design of a complete regulator system now looms as the next vital step for power processing design optimization.

(3) To effect power processing design optimization, the parallel devleopment of computer search methods applicable to broad classes of power processing problems is desirable. However, since no single method can be expected to cope with all problems equally well, the development of dedicated computer programs for a given class of power processing optimization will likely become an area of highly specialized research.

7. CONCLUSIONS

A power processing optimization methodology is established to effectively conceive a design, which not only accomodates all requirement specifications, but also optimizes a given design quantity deemed particularly desirable. Such a quantity can be either weight, efficiency, regulator response, or any other physically realizable entity.

As an initial demonstration of the optimization methodology, four design examples are presented. The method of Lagrange multipliers is applied to three examples to secure closed-form optimum solutions. These solutions prescribe an optimum-weight inductor design for a given loss constraint,and an optimum-loss inductor design for a given weight constraint. When closed-form solutions are not amendable in the other example, a nonlinear programming algorithm is used to conceive the design numerically.

Successful optimization effort eventually will achieve the following significant results: (1) there will be no need for heavy empirical reliances to perform the necessary design, (2) the penalties that may be incurred due to a sub-optimum design can be eliminated, which is particularly important in view of the forthcoming trend for use of considerable higher level of power, and (3) the optimization tool will, for the first time, allow a power processing system designer to perform intelligently the tradeoff study of candidate systems and to define confidently the optimum requirement specifications for the various equipment within a given system.

In perspective, one must realize that an optimization is generally associated with physical phenomena. Thus, the power processing optimization is of practical value only when there exists an accurate understanding of the physical principles upon which the constraints and the problem solutions depend. As a consequence, knowledge of power processing circuit and device characteristics (such as core losses, regulator control model, semiconductor switching phenomenon, etc.,) is a prerequisite to a successful power processing optimization. Furthermore, since most optimization problems are sufficiently complicated to defy closed-form solutions, the successful adoption of existing or dedicated search algorithms to power processing design optimization is an essential parallel development. It is only through continuous efforts in power processing modeling and analysis and in computer nonlinear programming can the design optimization be fostered into its future maturity.

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APPENDIX N

PROGRAM LISTING OF SUMT PROCESSING FOR CONVERTER DESIGN OPTIMIZATION

```
      SUBROUTINE EERRXX
      ENDFILE 6
      STOP
      END
      PROGRAM MAIN7(DATA7,OUTPUT,TAPE5=DATA7,TAPE6)
C*    CONSTRAINT OPTIMIZATION USING SUMT
C*
C*    THIS VERSION IS A 25 VARIABLE PROBLEM WITH 16 CONSTRAINTS
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     1CO1,CO2,CO3,CO4,CO5,CO6,CO7,CO8,CO9,CO10,CO11,CO12,CO13,
     1XK1,XK2,XK3,XK4
      COMMON/INIT/XI(25)
      COMMON/SHARE/X(100),DEL(100),A(100,100),N,M,MN,NP1,NM1
      COMMON/CRST/DELX(100),DELXO(100),RHOIN,RATIO,EPSI,THETAO,
     1RSIG1,G1,XI(100),X2(100),X3(100),XR2(100),XR1(100),PR1,
     2PR2,P1,F1,RJ1(200),DOTT,PGRAD(100),DIAG(100),
     3PKEV3,ADELX,NTCTR,NUMINI,NPHASE,NSATIS
      COMMON/TIMES/TMMAX
      COMMON/EQAL/H,H1,MZ
      COMMON/EXPOPT/NEXOP1,NEXOP2,XEP1,XEP2
      COMMON/OPTNS/NT1,NT2,NT3,NT4,NT5,NT6,NT7,NT8,NT9,NT10
      COMMON/CONSTM/C(20)
      REAL L1,L2,L3,KC,KC1,KC2,KC3
      NAMELIST/CON/PO,EFF,EI,EO,FC,FW,RO,VCES,VBE,TSNT,TSFT,
     1 VD,TSND,TSFD,TRD,PE1,PE2,BS1,BS2,BS3,VR,RCK,CK,DI,
     2 DC,KC1,KC2,KC3,KC,K
      NAMELIST/PRI/EPSI,THETAO,RHOIN,RATIO,TMMAX
      NAMELIST/OP1/NT1,NT2,NT3,NT4,NT5,NT6,NT7,NT8,NT9,NT10
      NAMELIST/TOP/XEP1,XEP2,NEXOP1,NEXOP2
      NAMELIST/XIN/XI
      READ(5,CON)
      WRITE(6,CON)
      READ(5,PRI)
      WRITE(6,PRI)
      READ(5,OP1)
      WRITE(6,OP1)
      READ(5,TOP)
      WRITE(6,TOP)
      READ(5,XIN)
      X1=XI(1)
      X2=XI(2)
      X3=XI(3)
      X4=XI(4)
      X5=XI(5)
      X6=XI(6)
      X7=XI(7)
      X8=XI(8)
      X9=XI(9)
      X10=XI(10)
      X11=XI(11)
      X12=XI(12)
      X13=XI(13)
      X14=XI(14)
      X15=XI(15)
      X16=XI(16)
      X17=XI(17)
      X18=XI(18)
      X19=XI(19)
      X20=XI(20)
      X21=XI(21)
      X22=XI(22)
      X23=XI(23)
      X24=XI(24)
      X25=XI(25)
      PI=3.141592654
      XM1=4.*FC*DC
      XM2=DI
      XM3=4.*RO*FC
      XM4=1./PE2
      XM5=1./(2.*PI)
      XM6=PO/EFF/EI
      XM7=SQRT(1./(PI*FW))
      XM8=.5
      XM9=PO/EO
      XM10=PO*VCES/EI+0.1*PO*VBE/EI
      XM11=EI*PO/6./EO
      XM12=(EI-EO)*EO/12.
      XM13=(EI-EO)*PO*VD/EI/EO
      XM14=80.*EO*(EI-EO)/EI
      XM15=XM12/EI
      XM16=PO
```

```
      XM17=EO/EI
      XM18=(CK*KCK)**2
      XM19=4.*EI*EI/EO/(EI-EO)
      XM20=(4.*XM5*XM9*SIN(PI*XM17))**2
      XM21=(24.*XM5*XM15*(COS(PI*XM17)-SIN(PI*XM17)/PI/XM17))**2
      XK1=KC
      XK2=KC1
      XK3=KC2
      XK4=KC3
      C01=VR
      C02=TSNT
      C03=TSFT
      C04=PE1**2
      C05=R
      C07=TSND
      C08=TSFD
      C09=TRD
      C010=EFF
      C011=BS1
      C012=BS2
      C013=BS3
      IST=0
      PIF=XM6**2*(X13+X14)
      PO=XM10+XM11*(C02+C03)*X25
      PD=XM13+0.5*XM11*(C08+3.*C09+C07)*X25
      POL=0.0022*XM14*X25**0.5*X22+XM9**2*X23*X18**2
      C(1)=ABS(XM16*(1./C010-1.)*X18**2-X18**2*(PIF+PO+PD)-POL)
      C(2)=ABS(X13*X3**2-XM3*X1*X2**2)
      C(3)=ABS(X14*X6**2-XM3*X4*X5**2)
      Y1=X9-X10*(1.+XM4)
      C(4)=ABS((1.+X15*X15)*X9*X9-C04*(X10**2+X15**2*Y1**2))
      Y1=XM4*X10*X25**3-X10*X25**2*X16*X15
      Y3=X16**3*X9*X15
      C(5)=ABS(Y1*X24-Y3)
      C(6)=ABS(X7*X9*X16**2-XM5**2)
      C(7)=ABS((X1*X2)**2-X7*XM6/C011)
      C(8)=ABS((X4*X5)**2-X8*XM6/C012)
      C(9)=ABS(XM7*X2*X3-XM5*X11+XM8*X1)
      C(10)=ABS(XM7*X5*X6-XM5*X12+XM8*X4)
      C(11)=ABS(C05-X13-X14)
      Y1=XM9*X20
      C(12)=ABS(X17*X17*X18*X18-Y1/C013)
      C(13)=ABS(X18*X19*XM7-XM5*X22+X17/2.)
      C(14)=ABS(X10-1.0E-6)
      Y1=(1.-XM17)*(1.+XM19*XM18*X25*X25)
      C(15)=ABS(8.*C01*X20*X21*X25**2-Y1)
      C(16)=ABS(X23*X19**2-XM3*X17*X18**2)
      Y1=(1.+(X25/2000.)**2)*(XM20*X20*X25*X20*X25+XM21)
      C(17)=ABS(4.*X24**2*Y1-X20*X25*X20*X25)
      C(1)=1./C(1)*0.01
      C(2)=1./C(2)*0.01
      C(3)=1./C(3)*0.01
      C(4)=1./C(4)
      C(5)=1./C(5)*0.01
      C(6)=1./C(6)*0.01
      C(7)=1./C(7)*0.01
      C(8)=1./C(8)*0.01
      C(9)=1./C(9)*0.01
      C(10)=1./C(10)*0.01
      C(11)=1./C(11)*0.01
      C(12)=1./C(12)*0.01
      C(13)=1./C(13)*0.01
      C(14)=1./C(14)*0.01
      C(15)=1./C(15)
      C(16)=1./C(16)*0.01
      C(17)=1./C(17)
      WRITE(6,9035)
 9035 FORMAT(*0 THE CONSTANT MULTIPLIERS ARE*)
      DISPLAY(6)*C(1)=*,C(1),*C(2)=*,C(2),*C(3)=*,C(3),*C(4)=*,C(4)
      DISPLAY(6)*C(5)=*,C(5),*C(6)=*,C(6),*C(7)=*,C(7),*C(8)=*,C(8)
      DISPLAY(6)*C(9)=*,C(9),*C(10)=*,C(10),*C(11)=*,C(11),
     1 *C(12)=*,C(12)
      DISPLAY(6)*C(13)=*,C(13),*C(15)=*,C(15)
      DISPLAY(6)*C(16)=*,C(16),*C(17)=*,C(17)
      WRITE(6,XIN)
      IST=IST+1
      CALL SUMT(IER)
      IF (IER.EQ.1)GO TO 20
      WRITE(6,9000)IST
 9000 FORMAT(*0SUMT CONVERGED TO A SOLUTION FROM STARTING POINT*,I3
      GO TO 30
   20 WRITE(6,9010)IST
```

ORIGINAL PAGE IS OF POOR QUALITY

```
 9010 FORMAT(*0SUMT DID NOT CONVERGE TO A SOLUTION*,
     C* FROM STARTING POINT*,I3)
C30   WRITE(6,9020)(X(I),I=1,25)
 30   TX1=X(1)*X(1)
      TX2=X(2)**2
      TX3=X(3)**2
      TX4=X(4)**2
      TX5=X(5)**2
      TX6=X(6)**2
      TX7=X(17)**2
      TX8=X(18)**2
      TX9=X(19)**2
      X(8)=X(7)/3.
      R4=X(15)*SQRT(X(7)/X(9))
      WRITE(6,9025)TX1,TX2,TX3,TX4
 9025 FORMAT(*0A1=*G15.5,* N1=*,G15.5,* AC1=*,G15.5,* A2=*,G15.5)
      WRITE(6,9026)TX5,TX6,X(7),X(8)
 9026 FORMAT(*0N2=*,G15.5,* AC2=*,G15.5,* L1=*,G15.5,* L2=*,G15.5)
      WRITE(6,9027)X(9),X(10),X(11),X(12)
 9027 FORMAT(*0C1=*,G15.5,* C2=*,G15.5,* Z1=*,G15.5,* Z2=*,G15.5)
      WRITE(6,9028)X(13),X(14),X(15),X(16)
 9028 FORMAT(*0R1=*,G15.5,* R2=*,G15.5,* D=*,G15.5,*F1=*,G15.5)
      WRITE(6,9001)TX7,TX8,TX9,X(20)
 9001 FORMAT(*0A3=*,G15.5,* N3=*,G15.5,* AC3=*,G15.5,* L3=*,G15.5)
      WRITE(6,9002)X(21),X(22),X(23),X(24)
 9002 FORMAT(*0C3=*,G15.5,* Z3=*,G15.5,* R3=*,G15.5,* G=*,G15.5)
      WRITE(6,9003)X(25),R4
 9003 FORMAT(*0F=*,G15.5,* R4=*,G15.5)
 9020 FORMAT(*0FINAL X VALUES*/(1X,4F20.5))
      PIF=XM6**2*(X(13)+X(14))
      PO=XM10+XM11*(CO2+CO3)*X(25)
      PD=XM13+0.5*XM11*(CO8+3.*CO9+CO7)*X(25)
      POL=0.0022*XM14*X(25)**0.5*X(22)/X(18)**2+XM9**2*X(23)
      PT=PIF+PO+PD+POL
      Y1=1.+X(15)**2
      Y2=(1.-X(10)/X(9)-X(8)/X(7)*X(10)/X(9))**2
      BSO=Y1/((X(10)/X(9))**2+X(15)**2*Y2)
      RATIO=X(8)/X(7)
      Y1=X(10)/X(9)*((X(25)/X(16))**2)
      ATT=1./(RATIO*Y1*X(25)/X(16)/X(15)-Y1)
      DL1=CO11-X(7)*XM6/(X(2)**2*X(1)**2)
      DL2=CO12-X(8)*XM6/(X(4)**2*X(5)**2)
      DL3=CO13-XM9*X(20)/(X(17)**2*X(18)**2)
      DL12=XM7*X(2)*X(3)-X(11)*XM5+X(1)/2.
      DL13=XM7*X(5)*X(6)-X(12)*XM5+X(4)/2.
      DL14=X(18)*X(19)*XM7-XM5*X(22)+0.5*X(17)
      DISPLAY(6)* R1=*,X(13)
      DISPLAY(6)* R2=*,X(14)
      DISPLAY(6)* D=*,X(15)
      DISPLAY(6)* PIF=*,PIF
      DISPLAY(6)* PO=*,PO
      DISPLAY(6)* PD=*,PD
      DISPLAY(6)* POL=*,POL
      DISPLAY(6)* PT(TOTAL)=*,PT
      DISPLAY(6)*INPUT FILTER PEAK.SO*,BSO
      DISPLAY(6)*RATIO OF L2/L1*,RATIO
      DISPLAY(6)* ATT.=*,ATT
      DISPLAY(6)* DEL(B1)=*,DL1
      DISPLAY(6)* DEL(B2)=*,DL2
      DISPLAY(6)* DEL(B3)=*,DL3
      DISPLAY(6)* DEL(AREA1)=*,DL12
      DISPLAY(6)* DEL(AREA2)=*,DL14
      DISPLAY(6)* DEL(AREA3)=*,DL14
      END
      SUBROUTINE READPR
      COMMON/SHARE/X(100),DEL(100),A(100,100),N,M,MN,NP1,NM1
      COMMON/EQAL/H,H1,MZ
      COMMON/INIT/X1(25)
      ENTRY R50
      M=3
      N=25
      MZ=14
      RETURN
      ENTRY R60
      DO 10 I=1,N
 10   X(I)=X1(I)
      RETURN
      ENTRY R80
      RETURN
      ENTRY R601
      RETURN
      ENTRY R801
```

```
      RETURN
      ENTRY PUNCH
      RETURN
      END
      SUBROUTINE RESTNT (II,VAL)
C     THIS SUBROUTINE EVALUATES THE O.F. IF I=0
C     OR THE CONSTRAINT II IF II NOT EQUAL TO 0
      COMMON/SHARE/X(100),DEL(100),A(100,100),N,M,MN,NP1,NM1
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     1CO1,CO2,CO3,CO4,CO5,CO6,CO7,CO8,CO9,CO10,CO11,CO12,CO13,
     1XK1,XK2,XK3,XK4
      COMMON/CONSTM/C(20)
      EQUIVALENCE (X1,X(1)),(X2,X(2)),(X3,X(3)),(X4,X(4)),
     1(X5,X(5)),(X6,X(6)),(X7,X(7)),(X8,X(8)),(X9,X(9)),
     2(X10,X(10)),(X11,X(11)),(X12,X(12)),(X13,X(13))
      EQUIVALENCE (X14,X(14)),(X15,X(15)),(X16,X(16)),(X17,X(17)),
     1(X18,X(18)),(X19,X(19)),(X20,X(20)),(X21,X(21)),
     2(X22,X(22)),(X23,X(23)),(X24,X(24)),(X25,X(25))
      IT=II+1
      GO TO (1000,14,11,5,7,8,12,9,10,13,15,1,2,3,4,6,16,17),IT
 1000 Y1=XM2*(X1**2*X11+X4**2*X12+X17**2*X22)
      Y2=XM1*(X1*X2**2*X3**2+X4*X5*X5*X6*X6+X17*X18**2*X19**2)
      Y3=XK2*X9+XK3*X10+XK4*X21
      VAL=Y1+Y2+Y3
      RETURN
C     EVAL.CONSTR.1
    1 PIF=XM6**2*(X13+X14)
      PO=XM10+XM11*(CO2+CO3)*X25
      PD=XM13+0.5*XM11*(CO8+3.*CO9+CO7)*X25
      POL=0.0022*XM14*X25**0.5*X22+XM9**2*X23*X18**2
      VAL=((XM15*(1./CO10-1.)-PIF-PO-PD)*X18**2-POL)*C(1)
C     DISPLAY(6)* PIF=*,PIF
C     DISPLAY(6)* PO=*,PO
C     DISPLAY(6)* PD=*,PD
C     DISPLAY(6)* POL=*,POL
      RETURN
C     EVAL.CONSTR.2
    2 VAL=(X13*X3**2-XM3*X1*X2**2)*C(2)
      RETURN
C     EVAL.CONSTR.3
    3 VAL=(X14*X6**2-XM3*X4*X5**2)*C(3)
      RETURN
C     EVAL.CONSTR.4
    4 Y1=X9-X10*(1.+XM4)
      VAL=(1.+X15*X15)*X9*X9-CO4*(X10*X10+X15*X15*Y1*Y1)
      VAL=-VAL*C(4)
      RETURN
C     EVAL.CONSTR.5
    5 Y1=XM4*X10*X25*X25*X25-X10*X25*X25*X16*X15
      Y3=X16*X9*X15*X16**2
      VAL=(Y1*X24-Y3)*C(5)
      RETURN
C     EVAL.CONSTR.6
    6 VAL=(X7*X9*X16*X16-XM5*XM5)*C(6)
      RETURN
C     EVAL.CONSTR.7
    7 VAL=((X1*X1*X2*X2)-X7*XM6/CO11)*C(7)
      RETURN
C     EVAL.CONSTR.8
    8 VAL=(X4*X4*X5*X5-X7*XM4*XM6/CO12)*C(8)
      RETURN
C     EVAL.CONSTR.9
    9 VAL=-(XM7*X2*X3-XM5*X11+XM8*X1)*C(9)
      RETURN
C     EVAL.CONSTR.10
   10 VAL=-(XM7*X5*X6-XM5*X12+XM8*X4)*C(10)
      RETURN
C     EVAL.CONSTR.11
   11 VAL=(CO5-X13-X14)*C(11)
      RETURN
C     EVAL.CONSTR.12
   12 VAL=(X17**2*X18**2-(XM9*X20)/CO13)*C(12)
      RETURN
C     EVAL.CONSTR.13
   13 VAL=-(X18*X19*XM7-XM5*X22+0.5*X17)*C(13)
      RETURN
C     EVAL.CONSTR.14
   14 VAL=(X10-1.0E-6)*C(14)
      RETURN
C     EVAL.CONSTR.15
   15 Y1=(1.-XM17)*(1.+XM19*XM18*X25**2)
```

```
      VAL=-(8.*CO1*X20*X21*X25**2-Y1)*C(15)
      RETURN
C     EVAL.CONSTR.16
 16   VAL=(X23*X19**2-XM3*X17*X18**2)*C(16)
      RETURN
C     EVAL.CONSTR.17
 17   Y1=X25*X25/2000./2000.
      Y2=XM20*X20*X25*X20*X25+XM21
      VAL=(4.*X24**2*(1.+Y1)*Y2-X20*X25*X20*X25)*C(17)
      RETURN
C     EVAL.CONSTR.18
C18   VAL=0.2-X22
C     RETURN
      END
      SUBROUTINE GRADI(II)
C     THIS SUBROUTINE EVALUATES THE GRADIENT OF THE
C     O.F. IF II=0 OR OF CONSTRAINT II
      COMMON/SHARE/X(100),DEL(100),A(100,100),N,M,MN,NP1,NM1
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     1CO1,CO2,CO3,CO4,CO5,CO6,CO7,CO8,CO9,CO10,CO11,CO12,CO13,
     1XK1,XK2,XK3,XK4
      COMMON/CONSTM/C(20)
      EQUIVALENCE (X1,X(1)),(X2,X(2)),(X3,X(3)),(X4,X(4)),
     1(X5,X(5)),(X6,X(6)),(X7,X(7)),(X8,X(8)),(X9,X(9)),
     2(X10,X(10)),(X11,X(11)),(X12,X(12)),(X13,X(13))
      EQUIVALENCE (X14,X(14)),(X15,X(15)),(X16,X(16)),
     1 (X17,X(17)),(X18,X(18)),(X19,X(19)),(X20,X(20)),
     1 (X21,X(21)),(X22,X(22)),(X23,X(23)),(X24,X(24)),
     1 (X25,X(25))
      IT=II+1
      DO 50 I=1,25
 50   DEL(I)=0.
      GO TO (100,14,11,5,7,8,12,9,10,13,15,1,2,3,4,6,16,17),IT
C     EVAL.GRAD. OF O.F.
 100  DEL(1)=XM1*X2*X2*X3*X3+2.*XM2*X1*X11
      DEL(2)=2.*XM1*X1*X2*X3*X3
      DEL(3)=2.*XM1*X1*X2*X2*X3
      DEL(4)=XM1*X5*X5*X6*X6+2.*XM2*X4*X12
      DEL(5)=2.*XM1*X4*X5*X6*X6
      DEL(6)=2.*XM1*X4*X5*X5*X6
      DEL(9)=XK2
      DEL(10)=XK3
      DEL(11)=XM2*X1*X1
      DEL(12)=XM2*X4*X4
      DEL(17)=2.*XM2*X17*X22+XM1*X18**2*X19**2
      DEL(18)=2.*XM1*X17*X18*X19**2
      DEL(19)=2.*XM1*X17*X18**2*X19
      DEL(21)=XK4
      DEL(22)=XM2*X17**2
      RETURN
C     EVAL.GRAD.OF CONSTR.1
 1    Y1=XM16*(1./CO10-1.)
      PIF=XM6**2*(X13+X14)
      PO=XM10+XM11*(CO2+CO3)*X25
      PD=XM13+0.5*XM11*(CO8+3.*CO9+CO7)*X25
      DEL(13)=-XM6*XM6*X18*X18*C(1)
      DEL(14)=-XM6*XM6*X18*X18*C(1)
      DEL(18)=(2.*X18*(Y1-PIF-PO-PD)-2.*XM9**2*X23*X18)*C(1)
      DEL(22)=(-0.0022*XM14*X25**0.5)*C(1)
      DEL(23)=-XM9*XM9*X18*X18*C(1)
      Y2=XM11*(CO2+CO3)+0.5*XM11*(CO8+3.*CO9+CO7)
      DEL(25)=(-X18**2*Y2-0.0011*XM14*X22/(X25**0.5))*C(1)
      RETURN
C     EVAL.GRAD.OF CONSTR.2
 2    DEL(1)=-XM3*X2*X2*C(2)
      DEL(2)=-2.*XM3*X1*X2*C(2)
      DEL(3)=2.*X3*X13*C(2)
      DEL(13)=X3*X3*C(2)
      RETURN
C     EVAL.GRAD. OF CONSTR.3
 3    DEL(4)=-XM3*X5*X5*C(3)
      DEL(5)=-2.*XM3*X4*X5*C(3)
      DEL(6)=2.*X6*X14*C(3)
      DEL(14)=X6*X6*C(3)
      RETURN
C     EVAL.GRAD.OF CONSTR.4
 4    Y1=X9-X10*(1+XM4)
      DEL(9)=-(2.*X9*(1+X15**2)-2.*CO4*X15**2*Y1)*C(4)
      DEL(10)=(2.*CO4*(X10-X15**2*(1+XM4)*Y1))*C(4)
      DEL(15)=(2.*X15*(-X9**2+CO4*(Y1**2)))*C(4)
      RETURN
```

```
C     EVAL.GRAD.OF CONSTR.5
  5   DEL(9)=-X15*X16*X16**2*C(5)
      DEL(10)=(XM4*X25-X15*X16)*X25*X24*X25*C(5)
      DEL(15)=-X16*(X10*X25**2*X24+X16*X9*X16)*C(5)
      DEL(16)=-X15*(X10*X24*X25**2+3.*X16*X9*X16)*C(5)
      DEL(24)=X10*X25**2*(XM4*X25-X15*X16)*C(5)
      DEL(25)=X10*X24*X25*(3.*XM4*X25-2.*X16*X15)*C(5)
      RETURN
C     EVAL.GRAD.OF CONSTR.6
  6   Y1=X16*X16
      DEL(7)=X9*Y1*C(6)
      DEL(9)=X7*Y1*C(6)
      DEL(16)=2.*X7*X9*X16*C(6)
      RETURN
C     EVAL.GRAD.OF CONSTR.7
  7   DEL(1)=2.*X1*X2*X2*C(7)
      DEL(2)=2.*X1*X1*X2*C(7)
      DEL(7)=-XM6/CO11*C(7)
      RETURN
C     EVAL.GRAD.OF CONSTR.8
  8   Y1=2.*X4*X5
      DEL(4)=Y1*X5*C(8)
      DEL(5)=Y1*X4*C(8)
      DEL(7)=-XM6*XM4/CO12*C(8)
      RETURN
C     EVAL.GRAD.OF CONSTR.9
  9   DEL(1)=-XM8*C(9)
      DEL(2)=-XM7*X3*C(9)
      DEL(3)=-X2*XM7*C(9)
      DEL(11)=XM5*C(9)
      RETURN
C     EVAL.GRAD.OF CONSTR.10
 10   DEL(4)=-XM8*C(10)
      DEL(5)=-XM7*X6*C(10)
      DEL(6)=-XM7*X5*C(10)
      DEL(12)=+XM5*C(10)
      RETURN
C     EVAL.GRAD.OF CONSTR.11
 11   DEL(13)=-C(11)
      DEL(14)=-C(11)
C     DEL(23)=-C(11)
      RETURN
C     EVAL.GRAD.OF CONSTR.12
 12   DEL(17)=C(12)*(2.*X17*X18**2)
      DEL(18)=C(12)*(2.*X17**2*X18)
      DEL(20)=C(12)*(-XM9/CO13)
      RETURN
C     EVAL. GRAD.OF.CONSTR.13
 13   DEL(17)=-C(13)*(0.5)
      DEL(18)=-C(13)*(X19*XM7)
      DEL(19)=-C(13)*(XM7*X18)
      DEL(22)=C(13)*(XM5)
      RETURN
C     EVAL.GRAD.OF.CONSTR.14
 14   DEL(10)=C(14)
      RETURN
C     EVAL.GRAD.OF.CONSTR.15
 15   DEL(20)=-C(15)*(8.*CO1*X25*X25*X21)
      DEL(21)=+C(15)*(-8.*CO1*X20*X25**2)
      DEL(25)=+C(15)*((1.-XM17)*2.*X25*XM18*XM19
     1 -16.*CO1*X20*X25*X21)
      RETURN
C     EVAL.GRAD.OF.CONSTR.16
 16   DEL(17)=-XM3*X18**2*C(16)
      DEL(18)=-2.*XM3*X17*X18*C(16)
      DEL(19)=2.*X19*X23*C(16)
      DEL(23)=X19**2*C(16)
      RETURN
C     EVAL.GRAD.OF.CONSTR.17
 17   Y1=X25*X25/2000./2000.
      Y2=XM20*X20*X25*X20*X25+XM21
      DEL(20)=2.*(4.*X24**2*(1.+Y1)*XM20-1.)*X20*X25*X25*C(17)
      DEL(24)=8.*X24*(1.+Y1)*Y2*C(17)
      DEL(25)=(4.*X24**2* (1.+Y1)*(2.*XM20*X20*X25*X20)
     1 +(2.*X25/2000.**2)*Y2)-2.*X20*X25*X20)*C(17)
      RETURN
C     EVAL.GRAD.OF.CONSTR.18
C18   DEL(22)=-1.0
C     RETURN
      END
      SUBROUTINE MATRIX(II,L)
C     EVALUATES SECOND PARTIALS OF THE O.F. IF II=0
```

```
C     OR CONSTRAINTS II IF II NOT 0
      COMMON/SHARE/X(100),DEL(100),A(100,100),N,M,MN,NP1,NM1
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     2C01,C02,C03,C04,C05,C06,C07,C08,C09,C010,C011,C012,C013,
     3XK1,XK2,XK3,XK4
      COMMON/CONSTM/C(20)
      EQUIVALENCE (X1,X(1)),(X2,X(2)),(X3,X(3)),(X4,X(4)),
     1(X5,X(5)),(X6,X(6)),(X7,X(7)),(X8,X(8)),(X9,X(9)),
     2(X10,X(10)),(X11,X(11)),(X12,X(12)),(X13,X(13))
      EQUIVALENCE (X14,X(14)),(X15,X(15)),(X16,X(16)),
     1(X17,X(17)),(X18,X(18)),(X19,X(19)),(X20,X(20)),
     2(X21,X(21)),(X22,X(22)),(X23,X(23)),(X24,X(24)),
     3(X25,X(25))
      IT=II+1
      GO TO (100,14,11,5,7,8,12,9,10,13,15,1,2,3,4,6,16,17),IT
C     O.F.
  100 A(1,1)=2.*XM2*X11
      A(1,2)=2.*XM1*X2*X3*X3
      A(1,3)=2.*XM1*X2*X2*X3
      A(1,11)=2.*XM2*X1
      A(2,2)=2.*XM1*X1*X3*X3
      A(2,3)=4.*XM1*X1*X2*X3
      A(3,3)=2.*XM1*X1*X2*X2
      A(4,4)=2.*XM2*X12
      A(4,5)=2.*XM1*X5*X6*X6
      A(4,6)=2.*XM1*X5*X5*X6
      A(4,12)=2.*XM2*X4
      A(5,5)=2.*XM1*X4*X6*X6
      A(5,6)=4.*XM1*X4*X5*X6
      A(6,6)=2.*XM1*X4*X5*X5
      A(17,17)=2.*XM2*X22
      A(17,18)=2.*XM1*X18*X19**2
      A(17,19)=2.*XM1*X18**2*X19
      A(17,22)=2.*XM2*X17
      A(18,18)=2.*XM1*X17*X19**2
      A(18,19)=4.*XM1*X17*X18*X19
      A(19,19)=2.*XM1*X17*X18**2
      RETURN
C     CONSTR.1
    1 Y1=XM16*(1./C010-1.)
      PIF=XM6*XM6*(X13+X14)
      PO=XM10+XM11*(C02+C03)*X25
      PD=XM13+0.5*XM11*(C08+3.*C09+C07)*X25
      A(13,18)=-2.*XM6*X18*XM6*C(1)
      A(14,18)=-2.*XM6*X18*XM6*C(1)
      A(18,18)=(2.*Y1-2.*(PIF+PO+PD)-2.*XM9*XM9*X23)*C(1)
      A(18,23)=(-2.*XM9*XM9*X18)*C(1)
      Y2=XM11*(C02+C03)+0.5*XM11*(C08+3.*C09+C07)
      A(18,25)=-2.*X18*Y2*C(1)
      A(22,25)=-0.0011*XM14/X25**0.5*C(1)
      A(25,25)=0.00055*XM14*X22/X25**1.5*C(1)
      RETURN
C     CONSTR.2
    2 A(1,2)=-2.*XM3*X2*C(2)
      A(2,2)=-2.*XM3*X1*C(2)
      A(3,3)=2.*X13*C(2)
      A(3,13)=2.*X3*C(2)
      RETURN
C     CONSTR.2
    3 A(4,5)=-2.*XM3*X5*C(3)
      A(5,5)=-2.*XM3*X4*C(3)
      A(6,6)=2.*X16*C(3)
      A(6,14)=2.*X6*C(3)
      RETURN
C     CONSTR.4
    4 Y1=1.+X15**2
      Y2=X9-X10*(1.+XM4)
      A(9,9)=-(2.*Y1-2.*C04*X15*X15)*C(4)
      A(9,10)=-(2.*C04*X15*X15*(1.+XM4))*C(4)
      A(9,15)=-(4.*X9*X15-4.*C04*X15*Y2)*C(4)
      A(10,10)=-(-2.*C04-2.*X15*X15*(1.+XM4)**2*C04)*C(4)
      A(10,15)=-(4.*X15*Y2*(1.+XM4)*C04)*C(4)
      A(15,15)=-(2.*X9*X9-2.*C04*Y2*Y2)*C(4)
      RETURN
C     CONSTR.5.
    5 A(9,15)=-X16*X16*X16*C(5)
      A(9,16)=-3.*X15*X16*X16*C(5).
      A(10,15)=-X16*X24*X25**2*C(5)
      A(10,16)=-X15*X24*X25*X25*C(5)
      A(10,24)=X25**2*(XM4*X25-X15*X16)*C(5)
      A(10,25)=X24*X25*(3.*XM4*X25-2.*X15*X16)*C(5)
```

```
      A(15,16)=-(X10*X24*X25**2+3.*X9*X16**2)*C(5)
      A(15,24)=-X10*X16*X25*X25*C(5)
      A(15,25)=-2.*X10*X16*X24*X25*C(5)
      A(16,16)=-6.*X15*X16*X9*C(5)
      A(16,24)=-X10*X15*X25**2*C(5)
      A(16,25)=-2.*X10*X15*X24*X25*C(5)
      A(24,25)=X10*X25*(3.*XM4*X25-2.*X15*X16)*C(5)
      A(25,25)=X10*X24*(6.*XM4*X25-2.*X15*X16)*C(5)
      RETURN
C     CONSTR.6
 6    Y1=X16*X16
      A(7,9)=Y1*C(6)
      A(7,16)=2.*X9*X16*C(6)
      A(9,16)=2.*X7*X16*C(6)
      A(16,16)=2.*X7*X9*C(6)
      RETURN
C     CONSTR.7
 7    A(1,1)=2.*X2*X2*C(7)
      A(1,2)=4.*X1*X2*C(7)
      A(2,2)=2.*X1*X1*C(7)
      RETURN
C     CONSTR.8
 8    A(4,4)=2.*X5*X5*C(8)
      A(4,5)=4.*X4*X5*C(8)
      A(5,5)=2.*X4*X4*C(8)
      RETURN
C     CONSTR.9
 9    A(2,3)=-XM7*C(9)
      RETURN
C     CONSTR.10
 10   A(5,6)=-XM7*C(10)
      RETURN
C     CONSTR.11
 11   L=1
      RETURN
C     CONSTR.12
 12   A(17,17)=2.*X18**2*C(12)
      A(17,18)=4.*X17*X18*C(12)
      A(18,18)=2.*X17**2*C(12)
      RETURN
C     CONSTR.13
 13   A(18,19)=-XM7*C(13)
      RETURN
C     CONSTR.14
 14   L=1
      RETURN
C     CONSTR.15
 15   Y1=1-XM17
      A(20,21)=-8.*CU1*X25**2*C(15)
      A(20,25)=-16.*C01*X21*X25*C(15)
      A(21,25)=(-16.*C01*X20*X25)*C(15)
      A(25,25)=(+2.*Y1*XM18*XM19-16.*C01*X20*X21)*C(15)
      RETURN
C.    CONSTR.16
 16   A(17,18)=-2.*XM3*X18*C(16)
      A(18,18)=-2.*XM3*X17*C(16)
      A(19,19)=2.*X23*C(16)
      A(19,23)=2.*X19*C(16)
      RETURN
C     CONSTR.17
 17   Y1=X25*X25/2000./2000.
      Y2=XM20*X20*X25*X20*X25+XM21
      A(20,20)=(4.*X24**2*(1.+Y1)*XM20-1.)*2.*X25**2*C(17)
      A(20,24)=16.*X24*(1.+Y1)*XM20*X20*X25**2*C(17)
      A(20,25)=4.*X20*X25*(4.*X24*XM20*X24*(1.+2.*Y1)-1.)*C(17)
      A(24,24)=8.*(1.+Y1)*Y2*C(17)
      A(24,25)=16.*X24*((1.+Y1)*(XM20*X20*X25*X20)+X25*Y2/2000.
     1 /2000.)*C(17)
      A(25,25)=(8.*X24*X24*(XM20*X20*X20*(1.+5.*Y1)+Y2/2000.
     1 /2000.)-2.*X2(*X20)*C(17)
      RETURN
C     CONSTR.18
C18   L=1
C     RETURN
      END
```

```
20    WRITE(6,9010)IST
9010  FORMAT(*0SUMT DID NOT CONVERGE TO A SOLUTION*,
     C* FROM STARTING POINT*,I3)
C30   WRITE(6,9020)(X(I),I=1,25)
30    TX1=X(1)*X(1)
      TX2=X(2)**2
      TX3=X(3)**2
      TX4=X(4)**2
      TX5=X(5)**2
      TX6=X(6)**2
      TX7=X(17)**2
      TX8=X(18)**2
      TX9=X(19)**2
      X(8)=X(7)/3.
      R4=X(15)*SQRT(X(7)/X(9))
      WRITE(6,9025)TX1,TX2,TX3,TX4
9025  FORMAT(*0A1=*G15.5,* N1=*,G15.5,* AC1=*,G15.5,* A2=*,G15.5)
      WRITE(6,9026)TX5,TX6,X(7),X(8)
9026  FORMAT(*0N2=*,G15.5,* AC2=*,G15.5,* L1=*,G15.5,* L2=*,G15.5)
      WRITE(6,9027)X(9),X(10),X(11),X(12)
9027  FORMAT(*0C1=*,G15.5,* C2=*,G15.5,* Z1=*,G15.5,* Z2=*,G15.5)
      WRITE(6,9028)X(13),X(14),X(15),X(16)
9028  FORMAT(*0R1=*,G15.5,* R2=*,G15.5,* D=*,G15.5,*F1=*,G15.5)
      WRITE(6,9001)TX7,TX8,TX9,X(20)
9001  FORMAT(*0A3=*,G15.5,* N3=*,G15.5,* AC3=*,G15.5,* L3=*,G15.5
      WRITE(6,9002)X(21),X(22),X(23),X(24)
9002  FORMAT(*0C3=*,G15.5,* Z3=*,G15.5,* R3=*,G15.5,* G=*,G15.5)
      WRITE(6,9003)X(25),R4
9003  FORMAT(*0F=*,G15.5,* R4=*,G15.5)
9020  FORMAT(*0FINAL X VALUES*/(1X,4F20.5))
      PIF=XM6**2*(X(13)+X(14))
      PQ=XM10+XM11*(CO2+CO3)*X(25)
      PD=XM13+0.5*XM11*(CO8+3.*CO9+CO7)*X(25)
      POL=0.0022*XM14*X(25)**0.5*X(22)/X(18)**2+XM9**2*X(23)
      PT=PIF+PQ+PD+POL
      Y1=1.+X(15)**2
      Y2=(1.-X(10)/X(9)-X(8)/X(7)*X(10)/X(9))**2
      BSQ=Y1/((X(10)/X(9))**2+X(15)**2*Y2)
      RATIO=X(8)/X(7)
      Y1=X(10)/X(9)*((X(25)/X(16))**2)
      ATT=1./(RATIO*Y1*X(25)/X(16)/X(15)-Y1)
      DL1=CO11*X(2)**2*X(1)**2-X(7)*XM6
      DL2=CO12*X(5)**2*X(4)**2-X(8)*XM6
      DL3=CO13*X(17)**2*X(18)**2-(XM9*X(20)+6.*XM15/X(25))
      DL12=XM7*X(2)*X(3)-X(11)*XM5+X(1)/2.
      DL13=XM7*X(5)*X(6)-X(12)*XM5+X(4)/2.
      DL14=X(18)*X(19)*XM7-XM5*X(22)+0.5*X(17)
      WI=XM2*(X(1)**2*X(11)+X(4)**2*X(12)+X(17)**2*X(22))
      WW=XM1*(X(1)*X(2)**2*X(3)**2+X(4)*X(5)**2*X(6)**2+
     1 X(17)*X(18)**2*X(19)**2)
      WL=WI+WW
      WC=XK2*X(9)+XK3*X(10)+XK4*X(21)
      WT=WL+WC
      DISPLAY(6)* EFFICIENCY=*,EFF
      DISPLAY(6)* INDUCTOR WEIGHT=*,WL
      DISPLAY(6)* CAPACITOR WEIGHT=*,WC
      DISPLAY(6)* TOTAL WEIGHT=*,WT
      DISPLAY(6)* R1=*,X(13)
      DISPLAY(6)* R2=*,X(14)
      DISPLAY(6)* R3=*,X(23)
      DISPLAY(6)* R4=*,R4
      DISPLAY(6)* D=*,X(15)
      DISPLAY(6)* PIF=*,PIF
      DISPLAY(6)* PQ=*,PQ
      DISPLAY(6)* PD=*,PD
      DISPLAY(6)* POL=*,POL
      DISPLAY(6)* PT(TOTAL)=*,PT
      DISPLAY(6)* INPUT FILTER PEAK.SQ*,BSQ
      DISPLAY(6)* RATIO OF L2/L1*,RATIO
      DISPLAY(6)* ATTENUATION=*,ATT
      DISPLAY(6)* DEL(B1)=*,DL1
      DISPLAY(6)* DEL(B2)=*,DL2
      DISPLAY(6)* DEL(B3)=*,DL3
      DISPLAY(6)* DEL(AREA1)=*,DL12
      DISPLAY(6)* DEL(AREA2)=*,DL13
      DISPLAY(6)* DEL(AREA3)=*,DL14
      END
      SUBROUTINE READPR
      COMMON/SHARE/X(40),DEL(40),A(40,40),N,M,MN,NP1,NM1
      COMMON/EQAL/H,H1,MZ
      COMMON/INIT/XI(25)
      ENTRY R50
```

```
      XM16=PO
      XM17=EO/EI
      XM18=(CK*RCK)**2
      XM19=4.*EI*EI/EO/(EI-EO)
      XM20=(4.*XM5*XM9*SIN(PI*XM17))**2
      XM21=(24.*XM5*XM15*(COS(PI*XM17)-SIN(PI*XM17)/PI/XM17))**2
      XK1=KC
      XK2=KC1
      XK3=KC2
      XK4=KC3
      CO1=VR
      CO2=TSNT
      CO3=TSFT
      CO4=PE1**2
      CO5=R
      CO7=TSND
      CO8=TSFD
      CO9=TRD
      CO10=EFF
      CO11=BS1
      CO12=BS2
      CO13=BS3
      IST=0
      PIF=XM6**2*(X13+X14)
      PQ=XM10+XM11*(CO2+CO3)*X25
      PD=XM13+0.5*XM11*(CO8+3.*CO9+CO7)*X25
      POL=0.0022*XM14*X25**0.5*X22/X18/X18+XM9**2*X23
      C(1)=ABS(XM16*(1./CO10-1.)-PIF-PQ-PD-POL)
      C(2)=ABS(X13*X3**2-XM3*X1*X2**2)
      C(3)=ABS(X14*X6**2-XM3*X4*X5**2)
      Y1=X9-X10*(1.+XM4)
      C(4)=ABS((1.+X15*X15)*X9*X9-CO4*(X10**2+X15**2*Y1**2))
      Y1=XM4*X10*X25**3-X10*X25**2*X16*X15
      Y3=X1[illegible]**3*X9*X15
      C(5)=ABS(Y1*X24-Y3)
      C(6)=ABS(X7*X9*X16**2-XM5**2)
      C(7)=ABS((X1*X2)**2-X7*XM6/CO11)
      C(8)=ABS((X4*X5)**2-X7*XM4*XM6/CO12)
      C(9)=ABS(XM7*X2*X3-XM5*X11+0.5*X1)
      C(10)=ABS(XM7*X5*X6-XM5*X12+0.5*X4)
      C(11)=ABS(CO5-X13-X14-X23)
      Y1=XM9*X20
      C(12)=ABS(X17*X17*X18*X18-Y1/CO13)
      C(13)=ABS(X18*X19*XM7-XM5*X22+X17/2.)
      C(14)=ABS(X10-1.0E-6)
      Y1=(1.-XM17)*(1.+XM19*XM18*X25*X25)
      C(15)=ABS(8.*CO1*X20*X21*X25**2-Y1)
      C(16)=ABS(X23*X19**2-XM3*X17*X18**2)
      Y1=(1.+(X25/2000.)**2)*(XM20*X20*X25*X20*X25+XM21)
      C(17)=ABS(X24**2*Y1-XM8**2*X20*X25*X20*X25)
      C(1)=1./C(1)
      C(2)=1./C(2)*0.01
      C(3)=1./C(3)*0.01
      C(4)=1./C(4)
      C(5)=1./C(5)*0.01
      C(6)=1./C(6)*0.01
      C(7)=1./C(7)*0.01
      C(8)=1./C(8)*0.01
      C(9)=1./C(9)*0.01
      C(10)=1./C(10)*0.01
      C(11)=1./C(11)*0.01
      C(12)=1./C(12)*0.01
      C(13)=1./C(13)*0.01
      C(14)=1./C(14)*0.01
      C(15)=1./C(15)
      C(16)=1./C(16)*0.01
      C(17)=1./C(17)
      WRITE(6,9035)
 9035 FORMAT(*0 THE CONSTANT MULTIPLIERS ARE*)
      DISPLAY(6)*C(1)=*,C(1),*C(2)=*,C(2),*C(3)=*,C(3),*C(4)=*,C(
      DISPLAY(6)*C(5)=*,C(5),*C(6)=*,C(6),*C(7)=*,C(7),*C(8)=*,C(
      DISPLAY(6)*C(9)=*,C(9),*C(10)=*,C(10),*C(11)=*,C(11),
     1 * C(12)=*,C(12)
      DISPLAY(6)*C(13)=*,C(13),*C(15)=*,C(15)
      DISPLAY(6)*C(16)=*,C(16),*C(17)=*,C(17)
      WRITE(6,XIN)
      IST=IST+1
      CALL SUMT(IER)
      IF (IER.EQ.1)GO TO 20
      WRITE(6,9000)IST
 9000 FORMAT(*0SUMT CONVERGED TO A SOLUTION FROM STARTING POINT*,
      GO TO 30
```

```
      SUBROUTINE EERRXX
      ENDFILE 6
      STOP
      END
      PROGRAM MAIN8(DATA8,OUTPUT,TAPE5=DATA8,TAPE6)
C*    CONSTRAINT OPTIMIZATION USING SUMT
C*
C*    THIS VERSION IS A 25 VARIABLE PROBLEM WITH 17 CONSTRAINTS
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     1C01,C02,C03,C04,C05,C06,C07,C08,C09,C010,C011,C012,C013,
     1XK1,XK2,XK3,XK4
      COMMON/INIT/XI(25)
      COMMON/SHARE/X(40),DEL(40),A(40,40),N.M,MN,NP1,NM1
      COMMON/CRST/DELX(40),DELX0(40),RHOIN,RATIO,EPSI,THETA0,
     1RSIG1,G1,X1(40),X2(40),X3(100),XR2(40),XR1(40),PR1,
     2PR2,P1,F1,RJ1(80),DOTT,PGRAD(40),DIAG(40),
     3PREV3,ADELX,NTCTR,NUMINI,NPHASE,NSATIS
      COMMON/TIMES/TMMAX
      COMMON/EQAL/H,H1,MZ
      COMMON/EXPOPT/NEXOP1,NEXOP2,XEP1,XEP2
      COMMON/OPTNS/NT1,NT2,NT3,NT4,NT5,NT6,NT7,NT8,NT9,NT10
      COMMON/CONSTM/C(20)
      REAL L1,L2,L3,KC,KC1,KC2,KC3,IEMI
      NAMELIST/CON/PO,EFF,EI,EO,FC,FW,RO,VCES,VBE,TSNT,TSFT,
     1 VD,TSND,TSFD,TRD,PE1,PE2,BS1,BS2,BS3,VR,RCK,CK,DI,
     2 DC,KC1,KC2,KC3,KC,R,IEMI
      NAMELIST/PRI/EPSI,THETA0,RHOIN,RATIO,TMMAX
      NAMELIST/OP1/NT1,NT2,NT3,NT4,NT5,NT6,NT7,NT8,NT9,NT10
      NAMELIST/TOP/XEP1,XEP2,NEXOP1,NEXOP2
      NAMELIST/XIN/XI
      READ(5,CON)
      WRITE(6,CON)
      READ(5,PRI)
      WRITE(6,PRI)
      READ(5,OP1)
      WRITE(6,OP1)
      READ(5,TOP)
      WRITE(6,TOP)
      READ(5,XIN)
      X1=XI(1)
      X2=XI(2)
      X3=XI(3)
      X4=XI(4)
      X5=XI(5)
      X6=XI(6)
      X7=XI(7)
      X8=XI(8)
      X9=XI(9)
      X10=XI(10)
      X11=XI(11)
      X12=XI(12)
      X13=XI(13)
      X14=XI(14)
      X15=XI(15)
      X16=XI(16)
      X17=XI(17)
      X18=XI(18)
      X19=XI(19)
      X20=XI(20)
      X21=XI(21)
      X22=XI(22)
      X23=XI(23)
      X24=XI(24)
      X25=XI(25)
      PI=3.141592654
      XM1=4.*FC*DC
      XM2=DI
      XM3=4.*RO*FC
      XM4=1./PE2
      XM5=1./(2.*PI)
      XM6=PO/EFF/EI
      XM7=SQRT(1./(PI*FW))
      XM8=IEMI
      XM9=PO/EO
      XM10=PO*VCES/EI+0.1*PO*VBE/EI
      XM11=EI*PO/6./EO
      XM12=(EI-EO)*EO/12.
      XM13=(EI-EO)*PO*VD/EI/EO
      XM14=80.*EO*(EI-EO)/EI
      XM15=XM12/EI
```

```
      M=3
      N=25
      MZ=14
      RETURN
      ENTRY R60
      DO 10 I=1,N
   10 X(I)=XI(I)
      RETURN
      ENTRY R80
      RETURN
      ENTRY R601
      RETURN
      ENTRY R801
      RETURN
      ENTRY PUNCH
      RETURN
      END
      SUBROUTINE RESTNT (II,VAL)
C     THIS SUBROUTINE EVALUATES THE O.F. IF I=0
C     OR THE CONSTRAINT II IF II NOT EQUAL TO 0
      COMMON/SHARE/X(40),DEL(40),A(40,40),N,M,MN,NP1,NM1
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     1CO1,CO2,CO3,CO4,CO5,CO6,CO7,CO8,CO9,CO10,CO11,CO12,CO13,
     1XK1,XK2,XK3,XK4
      COMMON/CONSTM/C(20)
      EQUIVALENCE (X1,X(1)),(X2,X(2)),(X3,X(3)),(X4,X(4)),
     1(X5,X(5)),(X6,X(6)),(X7,X(7)),(X8,X(8)),(X9,X(9)),
     2(X10,X(10)),(X11,X(11)),(X12,X(12)),(X13,X(13))
      EQUIVALENCE (X14,X(14)),(X15,X(15)),(X16,X(16)),(X17,X(17))
     1(X18,X(18)),(X19,X(19)),(X20,X(20)),(X21,X(21)),
     2(X22,X(22)),(X23,X(23)),(X24,X(24)),(X25,X(25))
      IT=II+1
      GO TO (1000,14,11,5,7,8,12,9,10,13,15,1,2,3,4,6,16,17),IT
 1000 Y1=XM2*(X1**2*X11+X4**2*X12+X17**2*X22)
      Y2=XM1*(X1*X2**2*X3**2+X4*X5*X5*X6*X6+X17*X18**2*X19**2)
      Y3=XK2*X9+XK3*X10+XK4*X21
      VAL=Y1+Y2+Y3
      RETURN
C     EVAL.CONSTR.1
    1 PIF=XM6**2*(X13+X14)
      PQ=XM10+XM11*(CO2+CO3)*X25
      PD=XM13+0.5*XM11*(CO8+3.*CO9+CO7)*X25
      POL=0.0022*XM14*X25**0.5*X22/X18/X18+XM9**2*X23
      VAL=(XM16*(1./CO10-1.)-PIF-PQ-PD-POL)*C(1)
C     DISPLAY(6)* PIF=*,PIF
C     DISPLAY(6)* PQ=*,PQ
C     DISPLAY(6)* PD=*,PD
C     DISPLAY(6)* POL=*,POL
      RETURN
C     EVAL.CONSTR.2
    2 VAL=(X13*X3**2-XM3*X1*X2**2)*C(2)
      RETURN
C     EVAL.CONSTR.3
    3 VAL=(X14*X6**2-XM3*X4*X5**2)*C(3)
      RETURN
C     EVAL.CONSTR.4
    4 Y1=X9-X10*(1.+XM4)
      VAL=(1.+X15*X15)*X9*X9-CO4*(X10*X10+X15*X15*Y1*Y1)
      VAL=-VAL*C(4)
      RETURN
C     EVAL.CONSTR.5
    5 Y1=XM4*X10*X25*X25*X25-X10*X25*X25*X16*X15
      Y3=X16*X9*X15*X16**2
      VAL=(Y1*X24-Y3)*C(5)
      RETURN
C     EVAL.CONSTR.6
    6 VAL=(X7*X9*X16*X16-XM5*XM5)*C(6)
      RETURN
C     EVAL.CONSTR.7
    7 VAL=((X1*X1*X2*X2)-X7*XM6/CO11)*C(7)
      RETURN
C     EVAL.CONSTR.8
    8 VAL=(X4*X4*X5*X5-X7*XM4*XM6/CO12)*C(8)
      RETURN
C     EVAL.CONSTR.9
    9 VAL=-(XM7*X2*X3-XM5*X11+0.5*X1)*C(9)
      RETURN
C     EVAL.CONSTR.10
   10 VAL=-(XM7*X5*X6-XM5*X12+0.5*X4)*C(10)
      RETURN
C     EVAL.CONSTR.11
```

```
   11 VAL=(C05-X13-X14-X23)*C(11)
      RETURN
C     EVAL.CONSTR.12
   12 VAL=(X17**2*X18**2-(XM9*X20)/C013)*C(12)
      RETURN
C     EVAL.CONSTR.13
   13 VAL=-(X18*X19*XM7-XM5*X22+0.5*X17)*C(13)
      RETURN
C     EVAL.CONSTR.14
   14 VAL=(X10-1.0E-6)*C(14)
      RETURN
C     EVAL.CONSTR.15
   15 Y1=(1.-XM17)*(1.+XM19*XM18*X25**2)
      VAL=-(8.*C01*X20*X21*X25**2-Y1)*C(15)
      RETURN
C     EVAL.CONSTR.16
   16 VAL=(X23*X19**2-XM3*X17*X18**2)*C(16)
      RETURN
C     EVAL.CONSTR.17
   17 Y1=X25*X25/2000./2000.
      Y2=XM20*X20*X25*X20*X25+XM21
      VAL=(X24**2*(1.+Y1)*Y2-XM8**2*X20*X25*X20*X25)*C(17)
      RETURN
      END
      SUBROUTINE GRAD1(II)
C     THIS SUBROUTINE EVALUATES THE GRADIENT OF THE
C     O.F. IF II=0 OR OF CONSTRAINT II
      COMMON/SHARE/X(40),DEL(40),A(40,40),N,M,MN,NP1,NM1
      COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
     1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
     1C01,C02,C03,C04,C05,C06,C07,C08,C09,C010,C011,C012,C013,
     1XK1,XK2,XK3,XK4
      COMMON/CONSTM/C(20)
      EQUIVALENCE (X1,X(1)),(X2,X(2)),(X3,X(3)),(X4,X(4)),
     1(X5,X(5)),(X6,X(6)),(X7,X(7)),(X8,X(8)),(X9,X(9)),
     2(X10,X(10)),(X11,X(11)),(X12,X(12)),(X13,X(13))
      EQUIVALENCE (X14,X(14)),(X15,X(15)),(X16,X(16)),
     1 (X17,X(17)),(X18,X(18)),(X19,X(19)),(X20,X(20)),
     1 (X21,X(21)),(X22,X(22)),(X23,X(23)),(X24,X(24)),
     1 (X25,X(25))
      IT=II+1
      DO 50 I=1,25
   50 DEL(I)=0.
      GO TO (100,14,11,5,7,8,12,9,10,13,15,1,2,3,4,6,16,17),IT
C     EVAL.GRAD. OF O.F.
  100 DEL(1)=XM1*X2*X2*X3*X3+2.*XM2*X1*X11
      DEL(2)=2.*XM1*X1*X2*X3*X3
      DEL(3)=2.*XM1*X1*X2*X2*X3
      DEL(4)=XM1*X5*X5*X6*X6+2.*XM2*X4*X12
      DEL(5)=2.*XM1*X4*X5*X6*X6
      DEL(6)=2.*XM1*X4*X5*X5*X6
      DEL(9)=XK2
      DEL(10)=XK3
      DEL(11)=XM2*X1*X1
      DEL(12)=XM2*X4*X4
      DEL(17)=2.*XM2*X17*X22+XM1*X18**2*X19**2
      DEL(18)=2.*XM1*X17*X18*X19**2
      DEL(19)=2.*XM1*X17*X18**2*X19
      DEL(21)=XK4
      DEL(22)=XM2*X17**2
      RETURN
C     EVAL.GRAD.OF CONSTR.1
    1 Y1=XM16*(1./C010-1.)
C     PIF=XM6**2*(X13+X14)
C     PQ=XM10+XM11*(C02+C03)*X25
C     PD=XM13+0.5*XM11*(C08+3.*C09+C07)*X25
      DEL(13)=-XM6*XM6*C(1)
      DEL(14)=-XM6*XM6*C(1)
      DEL(18)=+.0044*XM14*X25**0.5*X22/X18/X18/X18*C(1)
      DEL(22)=(-0.0022*XM14*X25**0.5/X18/X18)*C(1)
      DEL(23)=-XM9*XM9*C(1)
      Y2=XM11*(C02+C03)+0.5*XM11*(C08+3.*C09+C07)
      DEL(25)=(-Y2-0.0011*XM14*X22/(X25**0.5)/X18/X18)*C(1)
      RETURN
C     EVAL.GRAD.OF CONSTR.2
    2 DEL(1)=-XM3*X2*X2*C(2)
      DEL(2)=-2.*XM3*X1*X2*C(2)
      DEL(3)=2.*X3*X13*C(2)
      DEL(13)=X3*X3*C(2)
      RETURN
C     EVAL.GRAD. OF CONSTR.3
    3 DEL(4)=-XM3*X5*X5*C(3)
```

```
      DEL(5)=-2.*XM3*X4*X5*C(3)
      DEL(6)=2.*X6*X14*C(3)
      DEL(14)=X6*X6*C(3)
      RETURN
C     EVAL.GRAD.OF CONSTR.4
    4 Y1=X9-X10*(1+XM4)
      DEL(9)=-(2.*X9*(1+X15**2)-2.*CO4*X15**2*Y1)*C(4)
      DEL(10)=(2.*CO4*(X10-X15**2*(1+XM4)*Y1))*C(4)
      DEL(15)=(2.*X15*(-X9**2+CO4*(Y1**2)))*C(4)
      RETURN
C     EVAL.GRAD.OF CONSTR.5
    5 DEL(9)=-X15*X16*X16**2*C(5)
      DEL(10)=(XM4*X25-X15*X16)*X25*X24*X25*C(5)
      DEL(15)=-X16*(X10*X25**2*X24+X16*X9*X16)*C(5)
      DEL(16)=-X15*(X10*X24*X25**2+3.*X16*X9*X16)*C(5)
      DEL(24)=X10*X25**2*(XM4*X25-X15*X16)*C(5)
      DEL(25)=X10*X24*X25*(3.*XM4*X25-2.*X16*X15)*C(5)
      RETURN
C     EVAL.GRAD.OF CONSTR.6
    6 Y1=X16*X16
      DEL(7)=X9*Y1*C(6)
      DEL(9)=X7*Y1*C(6)
      DEL(16)=2.*X7*X9*X16*C(6)
      RETURN
C     EVAL.GRAD.OF CONSTR.7
    7 DEL(1)=2.*X1*X2*X2*C(7)
      DEL(2)=2.*X1*X1*X2*C(7)
      DEL(7)=-XM6/CO11*C(7)
      RETURN
C     EVAL.GRAD.OF CONSTR.8
    8 Y1=2.*X4*X5
      DEL(4)=Y1*X5*C(8)
      DEL(5)=Y1*X4*C(8)
      DEL(7)=-XM6*XM4/CO12*C(8)
      RETURN
C     EVAL.GRAD.OF CONSTR.9
    9 DEL(1)=-0.5*C(9)
      DEL(2)=-XM7*X3*C(9)
      DEL(3)=-X2*XM7*C(9)
      DEL(11)=XM5*C(9)
      RETURN
C     EVAL.GRAD.OF CONSTR.10
   10 DEL(4)=-0.5*C(10)
      DEL(5)=-XM7*X6*C(10)
      DEL(6)=-XM7*X5*C(10)
      DEL(12)=+XM5*C(10)
      RETURN
C     EVAL.GRAD.OF CONSTR.11
   11 DEL(13)=-C(11)
      DEL(14)=-C(11)
      DEL(23)=-C(11)
      RETURN
C     EVAL.GRAD.OF CONSTR.12
   12 DEL(17)=C(12)*(2.*X17*X18**2)
      DEL(18)=C(12)*(2.*X17**2*X18)
      DEL(20)=C(12)*(-XM9/CO13)
      RETURN
C     EVAL. GRAD.OF.CONSTR.13
   13 DEL(17)=-C(13)*(0.5)
      DEL(18)=-C(13)*(X19*XM7)
      DEL(19)=-C(13)*(XM7*X18)
      DEL(22)=C(13)*(XM5)
      RETURN
C     EVAL.GRAD.OF.CONSTR.14
   14 DEL(10)=C(14)
      RETURN
C     EVAL.GRAD.OF.CONSTR.15
   15 DEL(20)=-C(15)*(8.*CO1*X25*X25*X21)
      DEL(21)=+C(15)*(-8.*CO1*X20*X25**2)
      DEL(25)=+C(15)*((1.-XM17)*2.*X25*XM18*XM19
     1 -16.*CO1*X20*X25*X21)
      RETURN
C     EVAL.GRAD.OF.CONSTR.16
   16 DEL(17)=-XM3*X18**2*C(16)
      DEL(18)=-2.*XM3*X17*X18*C(16)
      DEL(19)=2.*X19*X23*C(16)
      DEL(23)=X19**2*C(16)
      RETURN
C     EVAL.GRAD.OF.CONSTR.17
   17 Y1=X25*X25/2000./2000.
      Y2=XM20*X20*X25*X20*X25+XM21
      DEL(20)=2.*(X24**2*(1.+Y1)*XM20-XM8**2)*X20*X25*X25*C(17)
```

```
03630        DEL(24)=2.*X24*(1.+Y1)*Y2*C(17)
03632        DEL(25)=(X24**2*((1.+Y1)*(2.*XM20*X20*X25*X20)
03633       1 +(2.*X25/2000.**2)*Y2)-2.*XM8**2*X20*X25*X20)*C(17)
03634        RETURN
03638        END
03640        SUBROUTINE MATRIX(II,L)
03642 C      EVALUATES SECOND PARTIALS OF THE O.F. IF II=0
03644 C      OR CONSTRAINTS II IF II NOT 0
03646        COMMON/SHARE/X(40),DEL(40),A(40,40),N,M,MN,NP1,NM1
03648        COMMON/CONS/XM1,XM2,XM3,XM4,XM5,XM6,XM7,XM8,XM9,XM10,XM11,
03650       1XM12,XM13,XM14,XM15,XM16,XM17,XM18,XM19,XM20,XM21,
03652       2C01,C02,C03,C04,C05,C06,C07,C08,C09,C010,C011,C012,C013,
03654       3XK1,XK2,XK3,XK4
03660        COMMON/CONSTM/C(20)
03670        EQUIVALENCE (X1,X(1)),(X2,X(2)),(X3,X(3)),(X4,X(4)),
03680       1(X5,X(5)),(X6,X(6)),(X7,X(7)),(X8,X(8)),(X9,X(9)),
03690       2(X10,X(10)),(X11,X(11)),(X12,X(12)),(X13,X(13))
03700        EQUIVALENCE (X14,X(14)),(X15,X(15)),(X16,X(16)),
03702       1(X17,X(17)),(X18,X(18)),(X19,X(19)),(X20,X(20)),
03704       2(X21,X(21)),(X22,X(22)),(X23,X(23)),(X24,X(24)),
03706       3(X25,X(25))
03710        IT=II+1
03720        GO TO (100,14,11,5,7,8,12,9,10,13,15,1,2,3,4,6,16,17),IT
03730 C      O.F.
03740   100  A(1,1)=2.*XM2*X11
03750        A(1,2)=2.*XM1*X2*X3*X3
03760        A(1,3)=2.*XM1*X2*X2*X3
03770        A(1,11)=2.*XM2*X1
03780        A(2,2)=2.*XM1*X1*X3*X3
03790        A(2,3)=4.*XM1*X1*X2*X3
03800        A(3,3)=2.*XM1*X1*X2*X2
03810        A(4,4)=2.*XM2*X12
03820        A(4,5)=2.*XM1*X5*X6*X6
03830        A(4,6)=2.*XM1*X5*X5*X6
03840        A(4,12)=2.*XM2*X4
03850        A(5,5)=2.*XM1*X4*X6*X6
03860        A(5,6)=4.*XM1*X4*X5*X6
03862        A(6,6)=2.*XM1*X4*X5*X5
03864        A(17,17)=2.*XM2*X22
03866        A(17,18)=2.*XM1*X18*X19**2
03868        A(17,19)=2.*XM1*X18**2*X19
03870        A(17,22)=2.*XM2*X17
03872        A(18,18)=2.*XM1*X17*X19**2
03874        A(18,19)=4.*XM1*X17*X18*X19
03876        A(19,19)=2.*XM1*X17*X18**2
03880        RETURN
03882 C      CONSTR.1
03884    1   Y1=0.0044*XM14*X25**0.5*X22/X18**3
03885 C      PIF=XM6*XM6*(X13+X14)
03886 C      PO=XM10+XM11*(C02+C03)*X25
03890 C      PD=XM13+0.5*XM11*(C08+3.*C09+C07)*X25
03892 C      A(13,18)=-2.*XM6*X18*XM6*C(1)
03894 C      A(14,18)=-2.*XM6*X18*XM6*C(1)
03906        A(18,18)=-3.*Y1/X18*C(1)
03908        A(18,22)=Y1/X22*C(1)
03910 C      Y2=XM11*(C02+C03)+0.5*XM11*(C08+3.*C09+C07)
03911        A(18,25)=0.5*Y1/X25*C(1)
03920        A(22,25)=-0.0011*XM14/X25**0.5/X18/X18*C(1)
03922        A(25,25)=0.00055*XM14*X22/X25**1.5/X18/X18*C(1)
03926        RETURN
03928 C      CONSTR.2
03930    2   A(1,2)=-2.*XM3*X2*C(2)
03940        A(2,2)=-2.*XM3*X1*C(2)
03950        A(3,3)=2.*X13*C(2)
03960        A(3,13)=2.*X3*C(2)
03970        RETURN
03980 C      CONSTR.2
03990    3   A(4,5)=-2.*XM3*X5*C(3)
04000        A(5,5)=-2.*XM3*X4*C(3)
04010        A(6,6)=2.*X14*C(3)
04020        A(6,14)=2.*X6*C(3)
04030        RETURN
04040 C      CONSTR.4
04050    4   Y1=1.+X15**2
04060        Y2=X9-X10*(1.+XM4)
04070        A(9,9)=-(2.*Y1-2.*C04*X15*X15)*C(4)
04080        A(9,10)=-(2.*C04*X15*X15*(1.+XM4))*C(4)
04090        A(9,15)=-(4.*X9*X15-4.*C04*X15*Y2)*C(4)
04100        A(10,10)=-(-2.*C04-2.*X15*X15*(1.+XM4)**2*C04)*C(4)
04110        A(10,15)=-(4.*X15*Y2*(1.+XM4)*C04)*C(4)
04120        A(15,15)=-(2.*X9*X9-2.*C04*Y2*Y2)*C(4)
04130        RETURN
```

```
04131 C     CONSTR.5.
04140  5    A(9,15)=-X16*X16*X16*C(5)
04142       A(9,16)=-3.*X15*X16*X16*C(5)
04156       A(10,15)=-X16*X24*X25**2*C(5)
04158       A(10,16)=-X15*X24*X25*X25*C(5)
04159       A(10,24)=X25**2*(XM4*X25-X15*X16)*C(5)
04160       A(10,25)=X24*X25*(3.*XM4*X25-2.*X15*X16)*C(5)
04164       A(15,16)=-(X10*X24*X25**2+3.*X9*X16**2)*C(5)
04169       A(15,24)=-X10*X16*X25*X25*C(5)
04170       A(15,25)=-2.*X10*X16*X24*X25*C(5)
04172       A(16,16)=-6.*X15*X16*X9*C(5)
04174       A(16,24)=-X10*X15*X25**2*C(5)
04176       A(16,25)=-2.*X10*X15*X24*X25*C(5)
04184       A(24,25)=X10*X25*(3.*XM4*X25-2.*X15*X16)*C(5)
04188       A(25,25)=X10*X24*(6.*XM4*X25-2.*X15*X16)*C(5)
04210       RETURN
04220 C     CONSTR.6
04230  6    Y1=X16*X16
04240       A(7,9)=Y1*C(6)
04250       A(7,16)=2.*X9*X16*C(6)
04260       A(9,16)=2.*X7*X16*C(6)
04270       A(16,16)=2.*X7*X9*C(6)
04280       RETURN
04290 C     CONSTR.7
04300  7    A(1,1)=2.*X2*X2*C(7)
04310       A(1,2)=4.*X1*X2*C(7)
04320       A(2,2)=2.*X1*X1*C(7)
04330       RETURN
04340 C     CONSTR.8
04350  8    A(4,4)=2.*X5*X5*C(8)
04360       A(4,5)=4.*X4*X5*C(8)
04370       A(5,5)=2.*X4*X4*C(8)
04380       RETURN
04390 C     CONSTR.9
04400  9    A(2,3)=-XM7*C(9)
04410       RETURN
04420 C     CONSTR.10
04430  10   A(5,6)=-XM7*C(10)
04440       RETURN
04450 C     CONSTR.11
04460  11   L=1
04470       RETURN
04480 C     CONSTR.12
04490  12   A(17,17)=2.*X18**2*C(12)
04500       A(17,18)=4.*X17*X18*C(12)
04510       A(18,18)=2.*X17**2*C(12)
04530       RETURN
04550 C     CONSTR.13
04560  13   A(18,19)=-XM7*C(13)
04570       RETURN
04590 C     CONSTR.14
04600  14   L=1
04610       RETURN
04630 C     CONSTR.15
04640  15   Y1=1-XM17
04641       A(20,21)=-8.*C01*X25**2*C(15)
04642       A(20,25)=-16.*C01*X21*X25*C(15)
04660       A(21,25)=(-16.*C01*X20*X25)*C(15)
04680       A(25,25)=(+2.*Y1*XM18*XM19-16.*C01*X20*X21)*C(15)
04700       RETURN
04710 C     CONSTR.16
04720  16   A(17,18)=-2.*XM3*X18*C(16)
04730       A(18,18)=-2.*XM3*X17*C(16)
04740       A(19,19)=2.*X23*C(16)
04750       A(19,23)=2.*X19*C(16)
04760       RETURN
04770 C     CONSTR.17
04780  17   Y1=X25*X25/2000./2000.
04781       Y2=XM20*X20*X25*X20*X25+XM21
04790       A(20,20)=(X24**2*(1.+Y1)*XM20-XM8**2)*2.*X25**2*C(17)
04800       A(20,24)=4.0*X24*(1.+Y1)*XM20*X20*X25**2*C(17)
04810       A(20,25)=4.*X20*X25*(X24*XM20*X24*(1.+2.*Y1)-XM8**2)*C(17)
04820       A(24,24)=2.*(1.+Y1)*Y2*C(1.)
04830       A(24,25)=4.0*X24*((1.+Y1)*(XM20*X20*X25*X20)+X25*Y2/2000.
04832      1 /2000.)*C(17)
04840       A(25,25)=(2.*X24*X24*(XM20*X20*X20*(1.+5.*Y1)+Y2/2000.
04842      1 /2000.)-2.*XM8**2*X20*X20)*C(17)
04850       RETURN
04890       END
"
```

POWER CONVERTER DESIGN OPTIMIZATION

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SUMMARY

Utilizing the demonstrated capability of nonlinear programming algorithms, a practical design optimization approach for power converters is established to conceive a design to meet all power-circuit performance requirements and concurrently optimize a defined quantity such as weight or losses. In addition to facilitate a cost-effective design, the computer-aided approach provides a means to readily assess (1) the weight-efficiency tradeoff, (2) impacts of converter requirements and component characteristics on a given design, and (3) optimum power system configurations.

1. Introduction

In the design of a power converter, the number of variables to be designed generally exceeds that of the constraints linking the variables to various performance requirements. Consequently, after the design constraints are defined, there exists virtually an infinite set of design solutions. The essence of the design optimization, therefore, is to pinpoint a set of design variables to meet all given constraints, and concurrently to achieve the optimization of a certain converter characteristic deemed particularly desirable. The characteristic can be the converter weight, loss, or any other physically-realizable entity associated with a converter.

Before venturing into more detailed design optimization aspects, it is perhaps worthwhile to review the state of the art in power converter design. Comparing with an ideal design optimization approach that will demand extremely sophisticated computer processing, a practical power-converter design optimization approach within existing computational programming capabilities is then adapted.

1.1 State-of-the-Art Design Approach

The state-of-the-art power-converter design, as perceived by the authors, contains the following major sequences:

(1) The designer obtains all specified converter requirements prescribed by someone presumably knowledgeable. Based on the nature of these requirements, the designer selects the basic power-circuit configuration:

- Buck
- Boost
- Buck Boost
- Series Resonant
- Parallel Inverter, etc.

Power electronics components such as magnetics, semiconductor switches, and capacitors are also selected.

(2) The designer's previous experience and occasionally the particular requirements are called upon to elect the control-circuit configuration and the duty cycle control method that includes:

- constant frequency, variable on/off time;
- constant on time and variable off time;
- constant off time and variable on time;
- constant hysteresis, two-state modulation;
- variable frequency, variable on/off time.

(3) Having selected the power and control-circuit configurations, the designer starts the power-circuit design by empirically or intuitively picking a power-converter switching frequency. Along with the control-independent performance requirements such as source and load voltages, load power demand, source EMI, output-voltage ripple, and the allowed weight (loss) for a given loss (weight), the designer proceeds to obtain semiconductor choices, input/output filter parameters, and design details of inductors and transformers. Such a design is characterized by the designer's subjective judgment which is often profusely arbitrary. Crude weight-loss analysis is then made, with occasional feeble attempt for piecemeal weight or loss optimization. The same procedure is repeated many times for different switching frequencies before completing a preliminary power-circuit design. Despite the time-consuming iterations, optimization of the overall power circuit is seldom achieved.

(4) Due to duty-cycle related nonlinearities in the power stage and the analog-to-discrete-time pulse modulation stage, the design of the control circuit for a given power circuit to meet the control-dependent performance requirements such as stability, responses to source/load step or sinusoidal disturbances is presently beyond the capability of the majority of the converter designers. Compliance with performance requirements is usually achieved by "bench design" (i.e., breadboard component-parameter iterations), and assured through elaborate testing.

Against this background, it is gratifying to note the strides made recently in the area of power-converter control-related modeling and analysis. [1 - 6] Undoubtedly these analyses will be advanced in the future to form the bases of analytically-based design guidelines which, when coupled with standardization of control-circuit configurations, will culminate in a complete control circuit design meeting all given performance requirements. For the time being, however, the preponderant converter designs are by no means analytically based. Additional effort is involved in advancing from "analysis for a given power and control circuit design in assessing performance compliance" to "analytically-based power- and control-circuit design to meet all performance requirements".

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1.2 An Ideal Design Optimization Approach

As previously stated, the utility of a design optimization is to pinpoint the detailed converter design to meet given performance specifications, and to achieve concurrently the minimization of a certain converter characteristic defined by the designer. Simply stated, the task is to minimize an objective function $f(x,k)$, subjected to design constraints $g_j(x,k,r) = 0$.

Here, $x = (x_1, x_2, \ldots x_n)^T$ is a n-dimensional vector representing power and control circuit parameters to be designed. Examples of x are values of R,L, and C, the switching frequency, and the design details of magnetic components including core area, mean core length, permeability, wire size, number of turns, and turns ratio of multiple-winding magnetics.

The k's represent various constants related to component characteristics. These constants are known to designers through common sense or design experiences. Examples include winding and core densities, winding resistivity, window fill factor of the core, winding pitch factor (i.e., the ratio of the mean length of one-turn winding to the core circumference), transistor and diode conduction and switching characteristics, core-loss parameters, intended maximum operating flux density of given magnetics, and ESR as well as energy-storage characteristics of filter capacitors.

The r's are performance requirements to be met by the optimum design. Control-independent requirements include input/output voltages, output power, maximum weight, minimum efficiency, source EMI, and maximum output ripple. Control-dependent requirements include regulator stability, minimum audiosusceptibility rejection, and maximum output impedance.

The function $f(x,k)$ represents the converter optimization criterion. Examples include the total weight, the total loss, the figure of merit of a specific design, a particular control-oriented performance, or any selected design quantity such as reliability and cost. The criterion generally can be expressed as a function of the x's and the k's.

Equations $g_j(x,k,r) = 0$ represent a total of "j" constraints relating requirements r to design variables x and design constants k. Examples of these equations include the relationship of an efficiency requirement to the sum of copper loss, core loss, semiconductor conduction and switching losses, and the loss in the capacitor ESR, the relationship of source EMI to the input-filter design parameters, the switching frequency, and the input/output voltage and current levels. Equations $g_j = 0$ allow all performance requirements "r" and all component constants "k" to be integrated into governing the design of all variables "x". Consequently, solutions acquired for equations $g_j = 0$ to minimize the objective function $f(x,k)$ would represent a detailed optimum design, down to the component level, in accordance with the performance requirements and the optimization criterion specified.

Thus, an ideal design optimization approach is to analytically portray $g_j = 0$ for all control-dependent and control-independent performance requirements. In conjunction with the defined optimization criterion $f(x,k)$, computer techniques are then applied to seek out the x's that would satisfy $g_j = 0$ and concurrently minimize $f(x,k)$.

Comparing the ideal optimization approach to present state-of-the-art design, the following notes are made:

(1) Both approaches start by obtaining requirements and selecting basic power- and control-circuit configurations.

(2) The switching frequency, which is fundamental to the power-circuit design, is selected in the ideal approach consistent with the optimization criterion. Unlike the state-of-the-art piecemeal design, the ideal approach acquires all design variables, including those prescribing detailed magnetics design, in an inclusive manner. Interdependences between various variables in different converter functions (e.g., input filter and output filter) are thus inherently preserved.

(3) The ideal approach would eliminate the need for excessive "bench design" of control-circuit variables. It will also reduce the role of converter testing to that of verification only, rather than its current role of being the major vehicle through which compatibility between converter requirements and capabilities can be demonstrated.

1.3 A Practical Design Optimization Approach

While the aforedescribed ideal approach represents the ultimate in converter design, its actual implementation is presently not without major difficulties. To begin with, it is realized that the well-developed computer linear programming techniques are inapplicable to converter optimization due to the nonlinear nature of the converter problems involved. As a result, the key to a successful design optimization of a complicated converter is to secure a nonlinear programming algorithm that enables optimum numerical solutions to be reached, with fast convergence, from an initial guess of the solutions. Since the effectiveness of any nonlinear programming technique is invariably affected by the global and local properties of the multi-dimensional design problem, the unfortunate consequence is that there is no uniformly good method on which an algorithm can be based to handle optimization problems as complicated as those involved with the design of a complete power converter. Naturally, the likelihood of securing an applicable nonlinear programming routine improves as the number, the nonlinearity, and the complexity of the nonlinear constraints diminish.

Some of the most nonlinear and complex constraints are those describing the control-dependent performance requirements. Stability, audiosusceptibility, and output-impedance characteristics involve all power- and control-circuit RLC parameters as well as the converter switching frequency. Furthermore, the characteristics themselves are functions of the signal modulation frequency via s-transform or z-transform, thus compounding the complexity of the control-dependent performance design constraints. Based on experiences gained to date on the application of various nonlinear programming routines, the chance for a successful inclusion of all control-dependent performance constraints in an overall power-converter design optimization is extremely slim for the foreseeable future.

To realize a practical approach within the demonstrated capability of nonlinear programming, one is, for the time being, forced to forsake the control-circuits, and to concentrate instead on the design optimization of the converter power circuit. The scope of the optimization criteria is reduced to include only those related to power-circuit performance characteristics, such as weight and losses.

Admittedly a less meritorious approach, its utility is still significant for the following reasons:

- The prevailing trend toward converters designed for higher power places increasing emphasis on loss and weight optimizations.
- Sensitivity to program cost and space/military equipment standardization encourages analysis-based designs to reduce weight, loss, and cost penalties resulting from suboptimum designs and developments.
- For a given power- and control-circuit configuration, converter design experience has indicated that, once the power-circuit parameters are properly designed, generally it is possible to design compatible coverter control-circuit parameters to meet stability and other control-dependent performance requirements. Thus, while the inclusion of control-dependent constraints in an overall converter design optimization represents a increase in the optimization effort, it is not likely to alter the weight-loss optimization results obtained from considering power-circuit related constraints alone. The results obtianed from power-circuit optimization are, therefore, both practical and meaningful.
- Comparing to the number of control-circuit configurations proposed and in use to date, there are relatively few commonly-used power-circuit configurations. The utility of the power circuit design optimization should be widespread and well-defined.

Consequently, given the limited nonlinear-programming capability currently demonstrable, a practical and useful design optimization approach can be formulated, which consists of the following two major steps:

(1) Desigh the power-circuit parameters to achieve the weight-loss optimization of a given power circuit configuration that will meet all control-independent performance requirements.

(2) Based on the power circuit parameters thus obtained, guidelines to design detailed control-circuit parameters to meet specified control-dependent performance requirements are then used to fulfill the design of a complete power converter. This step does not involve the use of a nonlinear programming routine. Design guidelines for control-circuit parameters will be conceived analytically based on work currently in progress, and should be within reach in the near future.

At present, the generation of design guidelines mentioned in step (2) appears to be the likely major thrust of near-term power-converter modeling and analysis. Undoubtedly, many significant contributions are forthcoming from industry/university/government research effort, both here and abroad. The emphasis of this paper is placed on step (1). It is hoped that the work reported here will provide the needed complement for results emerging from the step (2) effort. Together they are expected to shape the standardized power-converter design approach in the foreseeable future.

In the following sections, the methodology implementation of the step-(1) design optimization is discussed. Several computer-based optimization examples are given to demonstrate the utility of the said approach. Some needed improvements to enhance design optimization are also briefly outlined.

2. Implementation of Design Optimization

Continued rapid growth by applied optimization as a scientific discipline has been fostered by the application of optimization theory and the high-speed computer developments. In power converter design, it follows naturally that the key in implementing the design optimization approach rests on the availability of suitable mathematical and computer techniques.

2.1 The Lagrange Multiplier Method

A general mathematical optimization technique is the Lagrange Multiplier method [7], which can be used to seek an extremum for the objective function $f(x,k)$, subjected to a total of "j" constraints:

$$g_j(x,k,r) = 0, \qquad x = (x_1, x_2, \ldots x_n)^T$$

The method forms a function F, where $F = f + \Sigma h_j g_j$, with the h_j's being the Lagrange multipliers. For F to have an extremum, the requirement is:

$$\frac{\partial F}{\partial x_i} = 0, \quad i = 1,2,\ldots n.$$

From $g_j = 0$ and $\partial F/\partial x_i = 0$, a total of (j+n) equations are available to determine the "n" design variables and the "j" Lagrange multipliers.

Application of this method occasionally yields closed form solutions for simple power-converter optimization problems. Three such examples on optimum-weight and optimum-loss magnetics design were presented. [8] However, when the problem transcends the simple component level, the method generally does not yield closed form solutions.

2.2 Nonlinear Programming Techniques

Most larger problems arising from practical power-converter applications are sufficiently complicated to defy closed-form solutions. To identify numerically an optimum design, one has to resort to nonlinear programming algorithms which provide fast convergence to optimum solutions from a reasonable set of initial guesses. While there exist numerous methods of non-linear programming, the effectiveness of each method depends greatly on the global and local properties of the particular multi-dimensional problem to which the method is applied. The dependency makes it difficult to compare objectively the general merits of different algorithms. Based solely on our application experience to date, the Sequential Unconstrained Minimization Technique (SUMT) based on the method of a penalty function seems to be most effective in achieving convergence for highly nonlinear power-converter design optimization problems. [9,10]

A penalty function is one, which, when added to the original objective function $f(x,k)$ to form a penalized objective function $f_p(x,k)$, will detract from achieving a minimum objective when an associated constraint within constraints $g_j(x,k,r) = 0$ is not satisfied.

The particular penalty function used in the SUMT code is the quadratic form of g_j, which gives:

$$f_p = f + c \sum_{1}^{j} [g_j]^2$$

Here, c is a weighting coefficient when a minimum of f_p is desired. From the above equation, it is apparent that the constrained minimum of $f(x,k)$

subjected to constraints $g_j=0$ is identical to the unconstrained minimum of $f_p^j(x,k)$ when c approaches infinity. The SUMT code thus accommodates the initial "c", the conditions under which "c" is to be increased, and the criterion of bypassing the increasing "c" when the intended minimization process has run its course.

Before presenting design examples, the following application experience on SUMT are stated:

- Being primarily a research tool not specifically designed for power converter applications, the user generally needs to experiment with SUMT to realize its capabilities as well as limitations.
- To save computer time, the number of variables should be reduced to a minimum by combining all interpendent ones.
- Numerically the g_j's vary over a very wide range. To avoid conditions where certain g_j in the equation for f_p may be so large as to obscure the effects of the rest of the g_j's, each g_j must be properly scaled by a factor to insure that the effect of violating a given constraint is of the same order of magnitude as the effect of violating any other constraint.
- Depending on the problem involved, the initial set of guesses for optimum solutions can very important in determining the rate of convergence.

3. Demonstration Examples

Three design examples, one based on closed-form optimum solutions obtained from Lagrange multiplier method, the other two utilizing the SUMT, are provided to demonstrate power-converter design optimization.

3.1 Example 1 Optimum Weight Inductor Design

Using the method of Lagrange multipliers, the closed-form solution for an optimum-weight inductor design with a given loss constraint were presented. [8] The solutions prescribe core area A, core length Z, winding turns N, permeability U, core volume AZ, conductor area AC, and the minimum weight W. These parameters, in turn, are expressed as functions of conductor density DC, core density DI, winding pitch factor FC, window fill factor FW, conductor resistivity RHO, intended operating flux density BS, peak conductor current IP, needed inductance L, and allowed loss P. These closed-form solutions are implemented into a user-oriented computer subprogram, complete with user instruction, input request, input summary printout, and the optimum design results.

Upon executing the subprogram on a remote terminal, the computer will provide the following instructions:

```
C RUNX,I=INDO32,G
 THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN
 OPTIMUM WEIGHT INDUCTOR DESIGN FOR A GIVEN LOSS.
 TO USERS: PLEASE READ THE FOLLOWING STATEMENTS
    CAREFULLY BEFORE EXECUTING THE PROGRAM.
 THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:
     DC : CONDUCTOR DENSITY IN GRAMS CUBIC CM.
          IF NOT GIVEN BY THE USER, DC IS SET
          AT 8.9 BY DEFAULT.
     DI : CORE DENSITY IN GRAMS CUBIC CM.
          IF NOT GIVEN BY THE USER, DI IS SET
          AT 7.8 BY DEFAULT.
     FC : RATIO OF AVERAGE ONE TURN LENGTH TO THE
          CORE CIRCUMFERENCE.
          IF NOT GIVEN,FC IS SET AT 2. BY DEFAULT.
     FW : RATIO OF CONDUCTOR AREA TO WINDOW AREA.
          IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.
     RHO: CONDUCTOR RESISTIVITY IN OHM-METER. IF
          NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT.
     P  : DESIGNED POWER LOSS IN WATTS.
     BS : MAXIMUM FLUX DENSITY IN KILOGAUSSES.
     IP : PEAK INDUCTOR CURRENT IN AMPERES.
     L  : DESGNED INDUCTANCE IN MICROHENRIES.
 PLEASE GIVE INPUT DATA FOR L,IP,BS,AND P BELOW.
 PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,
     FC,FW,AND RHO IF ANY OF DEFAULTED SETTINGS IS
     NOT DESIRED.
 NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
 FOR ANSWERS AT THE END OF THE RUN,
 A IS CORE AREA, Z IS MEAN CORE LENGTH,
 N IS NUMBER OF TURNS, U IS PERMEABILITY,
 AZ IS PRODUCT OF A AND Z,AC IS CONDUCTOR AREA PER
 TURN,W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN P.
```

Subsequently, the computer requests input data from the user with regard to DC,DI,FC,FW,RHO, P,BS,IP, and L. Here, conductor density DC, resistivity RHO, core density DI, and operating flux density BS are known to a designer for given conductor and core materials. Factors FC and FW are generally known by a designer with given winding and core configurations. For parameters DC, DI, FC, FW, and RHO, the inherent values set by the subprogram are 8.9 g/cm^3, 7.8 g/cm^3, 2, 0.4, and 1.724×10^{-8} ohm-meter, respectively, representing the commonly-used copper density, core density, pitch factor for a filled window, fill factor for a filled window, and copper resistivity. The values of these parameters can be supplanted by a user's own design numbers. However, if no user inputs with regard to these parameters are received, the subprogram will utilize the inherently-set values by default. The power loss P, the peak current IP, and the required inductance L, are, of course, individually assigned by the user for specific applications.

In this example, the user needs a 200-uH inductor carrying a peak current IP of 4.5 amperes and utilizing an operating flux density BS of 3.5 kilogauss (i.e., a molypermalloy powder core). The loss allowed by the user is 0.699 watts. For DC, DI, FC, FW, and RHO, the user decides to use those set by the subprogram. The user thus responds to the computer input request by typing the following:

```
L=200.,IP=4.5,BS=3.5,P=0.699
```

Upon completion of input data, the computer prints out a summary of assigned input parameters including the defaulted ones:

```
DC      = 8.9,
DI      = 7.8,
FC      = 2.0,
FW      = 4.0E-01,
RHO     = 1.724E-08,
P       = 6.991E-01,
BS      = 3.5,
IP      = 4.5,
L       = 2.0E+02,
```

Finally, the optimum design values are computed by the subprogram and delivered as outputs:

```
A = 6.939E-01      SQUARE CENTIMETERS
Z = 6.391E+00      CENTIMETERS
N = 3.661E+01      TURNS
U = 1.094E+02      GAUSS OERSTED
AZ= 4.435E+00      CUBIC CENTIMETERS
AC= 2.419E+03      CIRCULAR MIL
W = 6.085E+01      GRAMS
```

With A=0.694 cm^2, Z=6.39 cm, U=109 gauss/oersted, and AC=2419 cir. mils, a compatible design using the commercially-available components is either core 55930 of Magnetics, Inc., or core A930157-2 of Arnold Engineering, with a wire size of #17 AWG. Such a design guarantees a loss limit around 0.7 watts as specified. From the printout, the inductor core and winding weight is approximately 61 grams.

The cost for this design session is 51 cents. This compares favorably to hours of laborious and suboptimum design iterations needed by an experienced designer using the paper-and-pencil approach.

Similar subprograms are conceived for the following:

- Optimum-weight inductor/transformer, with loss given as a constraint
- Optimum-weight inductor/transformer, with wire size given as a constraint
- Optimum-loss inductor/transformer, with weight given as a constraint

For details regarding these user-oriented subprograms, the readers are referred to Reference [11], to be published in the Fall, 1977.

3.2 Example 2 Optimum-Weight Switching-Regulator

This example deals with optimization on a vastly expanded scale in relation to the previous example. The design objective is to minimize the total component weight of a buck switching regulator power circuit, shown in Figure 1. The total loss allowed is given as a constraint.

Twenty-three variables "x" exist in this example, i.e., $x = (x_1, x_2, \ldots x_{23})^T$:

R_1, R_2, R_3 : Dc winding resistances of inductors L1, L2, and L3

L_1, L_2, C_1, C_2, R_4 : Input filter parameters

L_3, C_3 : Output filter parameters. The ESR of C3 is known to be RC.

A_1, A_2, A_3 : Core cross-sectional area of inductors L1, L2, and L3

Z_1, Z_2, Z_3 : Mean length of inductors L1, L2, and L3

N_1, N_2, N_3 : Number of turns on inductors L1, L2, and L3

A_{C1}, A_{C2}, A_{C3} : Inductor winding areas per turn for L1, L2, and L3

F : Switching frequency

The design constants "k" are described below. Numerical values used in this example are given in the parenthesis at the end of each corresponding description:

F_{C1}, F_{C2}, F_{C3} : Assigned winding pitch factor for inductors L1, L2, and L3 (2, 2, 2)

F_{W1}, F_{W2}, F_{W3} : Assigned window fill factor for inductors L1, L2, and L3 (.4,.4,.4)

RHO : Common conductor resistivities for L1, L2, and L3 (1.724×10^{-8}, 1.724×10^{-8}, 1.724×10^{-8} ohm-meter)

DI_1, DI_2, DI_3 : Core densities of inductors L1, L2, and L3 (7.8, 7.8, 7.8 g/cm^3)

DC_1, DC_2, DC_3 : Conductor densities of inductors L1, L2, and L3 (8.9, 8.9, 8.9 g/cm^3)

B_{S1}, B_{S2}, B_{S3} : Operating flux densities intended for inductors L1, L2, and L3 (3.5, 3.5, 3.5 kilogauss)

DCP_1, DCP_2, DCP_3 : Weight per microfarad for C1, C2, and C3 (210, 1100, 72 kilogram/farad)

V_{st} : Collector-emitter drop when transistor Q conducts (0.25 V)

V_{be} : Base-emitter forward drop of Q(0.8 V)

T_{sr} : Transistor switching rise time(.15us)

T_{sf} : Transistor switching fall time(.2 us)

V_d : Forward drop of diode D (.9 V)

T_{nd} : Diode turn-on time (.03us)

T_{fd} : Diode turn-off time (.05us)

T_{re} : Diode recovery time (.03us)

$O_e(F)$: Frequency-dependent core-loss factor for inductor L3, which processes a large ac flux excursion.

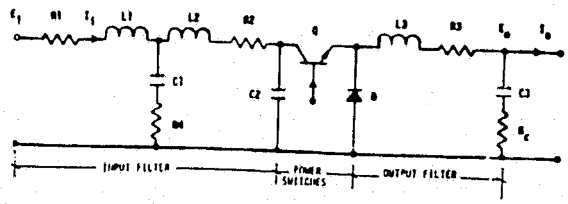

Figure 1 Buck Converter Power Circuit

Performance requirements "r" and their values used in this example are the following:

PE :	Input filter resonant peaking limit	(6 db)
P_o :	Output power	(100 W)
E_i :	Input voltage	(20-40 V)
E_o :	Output voltage	(15 V)
s(F):	Frequency-dependent source conducted interference	(see Fig.2)
r_i :	Output ripple	(1% of E_o)
e: :	Required efficiency	(93%)

In addition, constraints of sufficient core window and maximum operating flux density for inductors are also observed.

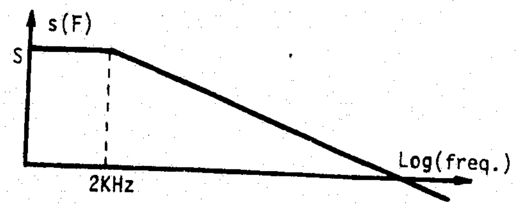

Figure 2 Source EMI Requirement Used in Example 2. S=0.1 A and S=0.5 A are used for design #1 and design #2

The constraints $g_j(x,k,r)=0$ include the following expressions:

Loss Constraint

In this constraint, the sum of all component losses should not exceed the total losses allowed by the minimum efficiency requirement, or,

$$P_{if} + P_t + P_d + P_{ofi} + P_{oc} = P_o(1-e)/e \qquad (1)$$

where:

P_{if} = Input filter copper losses

$$= \left(\frac{P_o}{eE_i}\right)^2 [4(RHO)]\left(\frac{F_{c1}N_1A_1^{0.5}}{A_{c1}} + \frac{F_{c2}N_2A_2^{0.5}}{A_{c2}}\right) \qquad (2)$$

P_t = Transistor saturation loss

+ Base drive loss based on 10-to-1 current drive

+ transistor turn-on switching loss

+ transistor turn-off switching loss

$$
\begin{aligned}
&= PV_{st}/E_i \\
&\quad + 0.1P_oV_{be}/E_i \\
&\quad + (E_iT_{sr}F/6)[(P_o/E_o) - (E_i-E_o)E_o/2L_3E_iF] \\
&\quad + (E_iT_{sf}F/6)[(P_o/E_o) + (E_i-E_o)E_o/2L_3E_iF] \qquad (3)
\end{aligned}
$$

$$
\begin{aligned}
P_d &= \text{Diode conduction loss} \\
&\quad + \text{Turn off and recovery losses} \\
&\quad + \text{Turn-on loss} \\
&= (E_i-E_o)P_oV_d/E_oE_i \\
&\quad + [E_iF(T_{fd}+3T_{re})/12][(P_o/E_o)-(E_i-E_o)E_o/2L_3E_iF] \\
&\quad + [E_iFT_{nd}/12][(P_o/E_o)+(E_i-E_o)E_o/2L_3E_iF] \qquad (4)
\end{aligned}
$$

$$
\begin{aligned}
P_{ofi} &= \text{Output inductor core loss} \\
&\quad + \text{Output inductor copper loss} \\
&= 80E_o(E_i-E_o)Z_3O_e(F)/N_3E_i \\
&\quad + [4(RHO)F_{c3}N_3A_3^{0.5}/A_{c3}] \\
&\quad \cdot \{(P_o/E_o)^2 + [(E_i-E_o)E_o/12L_3E_iF]^2\} \qquad (5)
\end{aligned}
$$

$$
\begin{aligned}
P_{oc} &= \text{Output filter ESR losses} \\
&= (1/12)[(E_i-E_o)E_o/12L_3E_iF]^2R_c \qquad (6)
\end{aligned}
$$

Notice the dependence on switching frequency F in equations (3) to (6).

Frequency-Dependent Source EMI Constraint

The frequency-dependent source EMI requirement sketched in Figure 2 has a constant peak-current allowance of "S" amperes when the frequency is below 2kHz, and decreases linearly on a logarithmic scale from 2KHz up. The input filter must be designed so that:

$$
\text{Required attenuation at switching frequency} = \frac{\text{EMI Requirement}}{\text{Fundamental switching current}}
$$

Thus,

$$
\begin{aligned}
&[(L_2C_2/L_1C_1)(2\pi F\sqrt{L_1C_1})^3(1/D)-(C_2/C_1)(2\pi F\sqrt{L_1C_1})^2]^{-1} \\
&= [S/\sqrt{1+(F/2000)^2}\,] / (A^2 + B^2)^{0.5} \qquad (7)
\end{aligned}
$$

where:

$$A = (2P_o/\pi E_o)\ \mathrm{Sin}(\pi E_o/E_i)$$

$$B = [(E_i-E_o)E_o/L_3F\pi E_i][\mathrm{Cos}(\pi E_o/E_i - \frac{\mathrm{Sin}(\pi E_o/E_i)}{\pi\ E_o/E_i}]$$

$$D = R_4(C_1/L_1)^{0.5}$$

Other Input Filter Design Constraints

In addition to source EMI, other critical aspects of an input filter design include its resonant peaking and its output impedance. While these characteristics are important in determining the audiosusceptibility performance and the control-loop stability of the converter, they are normally not specified in the converter specification sheet. However, to ensure that the optimum-weight power circuit design will be compatible with its companion feedback control circuit, the inclusion of the self-imposed resonance and impedance characteristics becomes highly desirable.

In this example, the requirement "PE" concerning resonant peaking is included as a design constraint:

$$
(PE)^2 = \frac{1 + (R_4{}^2C_1/L_1)}{(C_2/C_1)^2 + (R_4{}^2C_1/L_1)[1-(C_2/C_1)-(L_2C_2/L_1C_1)]^2} \qquad (9)
$$

Output Ripple

$$
r_i = \frac{1}{8L_3C_3}\left(1-\frac{E_o}{E_i}\right)\left[\left(\frac{1}{F}\right)^2 + \frac{4C_3{}^2R_c{}^2E_i{}^2}{E_o(E_i-E_o)}\right] \qquad (10)
$$

Window Area Constraint

All inductor windings must be accommodated within the physical confine of the available core window area. Thus, for inductors L1 to L3,

$$
(N_kA_{ck}/\pi F_{wk})^{0.5} - Z_k/2 + A_k^{0.5}/2 = 0,\ k=1,2,3 \qquad (11,12,13)
$$

Operating Flux Density Constraint

The inductor design must not exceed the intended operating flux density level. Since inductors L1 and L2 only conduct direct current,

$$
N_kA_k - L_kP_o/eE_iB_{sk} = 0,\quad k = 1,2 \qquad (14,15)
$$

Inductor L3 handles both dc and ac components,

$$
N_3A_3 - (L_3/B_{s3})[(P_o/E_o)+(E_i-E_o)E_o/2L_3E_iF] = 0 \qquad (16)
$$

The objective function f(x,k) in this example is the total iron, copper, capacitor, and semiconductor weight. Since the semiconductor weight is essentially fixed, the function f(x,k) becomes:

$$
\begin{aligned}
f(x,k) &= \text{core weight} + \text{winding weight} \\
&\quad + \text{capacitor weight} \\
&= \Sigma(DI)_kA_kZ_k + 4\cdot (DC)_kA_k^{0.5}F_{ck}N_kA_{ck} \\
&\quad + \Sigma\ (DCP)_kC_k,\qquad k = 1,2,3 \qquad (17)
\end{aligned}
$$

Having defined all variables x's, constants k's, requirements r's, contraints g_j's, and the objective function f(x,k), the goal of this design is to solve all x's to satisfy each constraint prescribed in eqs. (1) to (16), and concurrently to minimize the quantity specified in eq. (17).

Obviously, a problem of this complexity is not amenable to closed-form solutions. The SUMT computer program is used to acquire optimum solutions numerically. The program contains fourteen pages of Fortran listing dealing mostly with constraints and their first and second derivatives with respect to variables within the constraints. Considering the limited information such a listing can provide without extensive descriptive supplements, the program itself is not included here. It is, however, available in Reference [11].

Two sets of optimum design results are illustrated in Table 1. The difference between them is that design #1 assumes a three-times higher ESR for the output filter capacitor and a five-times more stringent source EMI requirement than those of design #2. In each design, all RLC parameters, the switching frequency, the design details of all magnetics, and the minimum weight, are collectively achieved in a single computer run which represents minimum component-weight designs.

Table 1 Optimum Converter Component Weight

Optimum Design Results

	Design #1 (R_c = 0.3 ohm, S = 0.1A)	Design #2 (R_c = 0.1 ohm, S = 0.5A)
Z1 (cm)	5.10	3.11
A1 (cm^2)	0.438	0.161
N1 (turns)	40	21
AC1 (mm^2)	0.779	0.519
Z2 (cm)	3.86	2.35
A2 (cm^2)	0.251	0.092
N2 (turns)	22	12
AC2 (mm^2)	0.756	0.507
Z3 (cm)	7.84	5.20
A3 (cm^2)	0.694	0.235
N3 (turns)	46	36
AC3 (mm^2)	1.9	1.21
L1 (μH)	253	53.7
L2 (μH)	84	17.9
L3 (μH)	192	52.5
C1 (μF)	89.5	47
C2 (μF)	30.8	10
C3 (μF)	710	325
R1 (milliohm)	41.5	20.9
R2 (milliohm)	17.9	9.1
R3 (milliohm)	25.3	18.3
R4 (ohms)	2.97	0.94
F (kHz)	22.0	43.9
W (grams)	239.5	78.1

Notice the impact exerted by ESR and source EMI on the two data columns of Table 1. For the same loss constraint, every parameter of design #2 is smaller than its counterpart of design #1. The only exception occurs at the analytically-determined optimum switching frequency, where the 43.9 kHz for design #2 is almost twice that of the design #1. As a result, the combined magnetics and capacitor weight of design #2 is barely one-third of that for design #1.

The total computer cost per run for a problem of this magnitude is generally within the $20-to-$40 range. This compares favorably with days of suboptimum paper-and-pencil design iterations.

3.3 Example 3 Optimum-Weight Source-Converter System

In this example, the buck converter shown in Figure 1 is integrated with a solar-array battery source of a known power density(kilogram/watt). The converter mechanical packaging weight is also included in the overall design optimization. Since the converter loss is supplied from the power source, and since the converter packaging weight (heat sink included) increases with the converter losses, for a given output power it follows that the combined source-and-mechanical-package weight becomes heavier if more converter loss is allowed. On the other hand, experience also indicates that the total converter component weight (magnetics and capacitors) tends to diminish with more allowable losses. Consequently, for a given output power as well as a given source density and packaging density, there must exist an optimum converter efficiency at which the combined system weight including power source, converter packaging, and converter component, is at its minimum. The objective of this example is to identify numerically such an optimum efficiency. The minimum efficiency requirement "e" used in Example 2 for component weight optimization only thus is no longer a design constraint. Instead, the efficiency becomes an unknown variable in this example.

Comparing this example to Example 2, the different formation of design variables, design constants, performance requirements, and the objective function are as follows:

- Efficiency "e" becomes a variable in addition to the twenty-three variables listed in Example 2.
- Two more design constants, KS and KH, for source and packaging densities respectively (in kilograms per watt), are added to the twenty-eight constants shown in Example 2.
- Efficiency "e" is no longer a performance requirement. All other requirements in Example 2, however, remain applicable to this example.
- The loss constraint used in Example 2 is eliminated. The sum of all losses, i.e., the quantity

  $$\Sigma P = P_{if} + P_t + P_d + P_{ofi} + P_{oc}$$

  is being used in this example as part of the new objective function. All other constraints in Example 2 remain effective in this example.
- The new objective function for this example is:

$$\begin{aligned} W &= \text{Core Weight} + \text{Winding Weight} \\ &+ \text{Capacitor Weight} + \text{Source Weight} \\ &+ \text{Packaging Weight} \\ &= \Sigma\,(DI)_k A_k Z_k + 4\,\Sigma(DC)_k A_k^{0.5} F_{ck} N_k A_{ck} \\ &+ \Sigma\,(DCP)_k C_k + (P_o + \Sigma P)(KS) \\ &+ (\Sigma P)(KH), \quad k = 1,2,3 \end{aligned} \tag{18}$$

Since (ΣP) is shown in Example 2 to be a function of multiple factors;

$$\Sigma P = \text{function of } (N_k, A_k, A_{ck}, L_3, Z_3, F, R_c), \quad k=1,2,3 \tag{19}$$

it can be seen that, after all variables are numerically identified by SUMT, the term (ΣP) can be calculated to reveal the particular converter efficiency that will produce a minimum combined source-converter weight.

Again, the detailed computer programming for this problem is available in Reference [11]. Numerical values for design constants and performance requirements are identical to those used in design #1 of Example 2. Two sets of optimum design results for minimum system weight are illustrated in Table 2. The difference between them is the different source density "KS" and packaging density "KH" assumed.

Table 2 Optimum Source-Converter System

	Design #1	Design #2
	(K_S = 0.065 Kg/W)	(K_S = 0.0163 Kg/W)
	(K_H = 0.065 Kg/W)	(K_H = 0.0325 Kg/W)
Z1 (cm)	4.98	4.63
A1 (cm^2)	0.413	0.360
N1 (turns)	25	35
AC1 (mm^2)	1.13	0.701
Z2 (cm)	3.79	3.53
A2 (cm^2)	0.238	0.207
N2 (turns)	14	20
AC2 (mm^2)	1.133	0.701
Z3 (cm)	7.87	6.87
A3 (cm^2)	0.395	0.53
N3 (turns)	43	40
AC3 (mm^2)	2.6	1.58
L1 (μH)	154	188
L2 (μH)	51	62.7
L3 (μH)	101	126
C1 (μF)	133	108
C2 (μF)	19	15
C3 (μF)	1346	1075
R1 (millionm)	18.3	39
R2 (millionm)	8.1	17
R3 (millionm)	13.[illegible]	22.5
R4 (ohms)	0.81	0.99
F (kHz)	22.1	22.2
W (kg)	7.562	2.167
Eff. (%)	94.12	93.6

Several impacts exerted by different KS's and KH's are noted:

- As expected, a decrease in kg/w of source and package densities from design #1 to design #2 allows more loss in design #2 to achieve an optimum-weight system. The converter efficiency for such a system is reduced from 94.1% of design #1 to 93.6% of design #2. The 94.1% efficiency, incidently, represents nearly the maximum possible efficiency consistent with the various loss-related design constants specified in Example 2. The most influencial design constants limiting the efficiency achievable are transistor and diode conduction drops in conjunction with the required output power and voltage levels.
- For a four-to-one reduction in source density, the optimum efficiency only decreases from the approximate maximum limit of 94.1% by 0.5%. Since the realistic source density (including source and source conditioning) currently available is in the proximity of that used in design #1, it is not surprising that the system designer has currently placed the highest emphasis on obtaining the highest converter efficiency possible.

4. Needed Improvements on Design Optimization

While a practical design optimization approach has been successfully demonstrated to solve rather complex problems, it is not the intention of this paper to paint an over-simplified picture concerning power converter design optimization in general.

To start with, one must realize that an optimization is generally associated with physical phenomena. Thus, the design optimization is of practical value only when there exists an accurate understanding of the physical principles and mathematical models upon which the design constraints and the design constants all depend. Since weight and loss generally are used as power-converter optimization criteria, knowledge of power-device weight-loss characteristics is thus a prerequisite to a successful optimization. Of these characteristics, the more important ones are:

- The accurate core-loss data as a function of the switching frequency and the asymmetrical rectangular-waveform excitation
- The "effective resistance" of magnetic windings in high-frequency, high-current applications
- An acceptable semiconductor switching-loss profile for power transistors and diodes in a given magnetics-semiconductor power-circuit configuration, and the likely impacts exerted by the commonly-used means of energy recovery on switching losses.

These characteristics, at the present time, are insufficiently defined. Considering that they are needed in the day-to-day design effort without any excursion into the realm of optimization, better understanding of component behavior must be regarded as a necessity that is long overdue. Without further knowledge of these characteristics, the selection of the optimum switching frequency, which is the most important parameter in power converter design and weight-loss tradeoff, will continue to be determined empirically. Since the optimization results are as accurate as the participating design constants and constraints, the design optimization approach thus brings into sharp focus the pressing need for knowledge of these characteristics.

Furthermore, since most practical power converter optimization problems are sufficiently complicated to defy closed-form solutions, the availability of powerful and fast-convergent nonlinear programming algorithms is indispensable. However, no general-purpose algorithms can be expected to cope with specialized nonlinear power converter problems. The SUMT used in the examples performs well in the presence of good starting guesses of variables for constraints whose partial derivatives with respect to all variables are well behaved. On the other hand, the guarantee that it "almost always converges" is not inherent in SUMT, nor is it expected from other algorithms in the foreseeable future. Consequently, the development of dedicated computer optimization routines for a given class of power converters will likely become a highly specialized yet essential research.

5. Conclusions

A practical power converter design optimization approach is proposed in Section 1, and its implementation is discussed in Section 2. Through three practical engineering design examples given in Section 3, the approach is demonstrated to greatly facilitate several endeavors heretofore regarded as difficult or unattainable:

(1) It allows a cost-effective optimum design for a power component or a complete power converter, down to the component level. The design includes the identification of the optimum switching frequency and detailed magnetics design parameters. Not only meeting all power-circuit related performance requirements, the optimization of either the weight, the loss, or any other realizable entity of a power converter can be achieved.

(2) The design takes into account the interdependent nature of the various functions within a power converter (e.g., the impact of output-filter parameters on the input-filter design). The total computer cost for a complete power circuit design is within the $20-to-$40 range, which compares favorably with days of suboptimum, piecemeal, hand-iterated design effort. Savings in both design and development cost are thus achieved.

(3) It provides a fast and accurate weight-loss trade-off as well as a means for ready assessment of the impact of a given requirement or a particular component characteristic on an optimum design.

(4) It can assist the power system designer to conceive the optimum system configuration and the proper converter specifications to achieve an overall optimum system, thus setting the stage for a more "scientific" design approach not relying heavily on subjective judgements.

Proper fostering for power-converter design optimization takes the form of accurate device characterizations and dedicated programming developments. These needed improvements are briefly outlined in Section 4.

The importance of identifying an optimum design among all designs is underscored by the fact that, all other performances being equal, the design that is best in a specified sense is the one usually prevails. However, being extremely hardware oriented and forever engrossed with necessary evils such as "schedule" and "cost", a power converter designer often considers the design tasks successfully fulfilled even though the design itself may be, knowingly or unwittingly, quite "suboptimum". With the advent of high-speed computers, applied optimization has become increasingly popular in practically all engineering disciplines. It is for the promotion of this trend in the field of power-converter design that the cost-effective optimization effort reported herein is strived.

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APPENDIX Q

SAMPLES OF COMPONENT DATA COMPILATIONS

In this appendix, data bases for (1)Foil Tantalum Polarized Capacitors, and (2) Copper Wire Sizes, are illustrated as samples of data compilation.

Q.1 DATA BASE FOR FOIL-TANTALUM POLARIZED CAPACITORS

The DB for foil-tantalum polarized capacitors is given in Table 1. Each row represents information for a given capacitor that is commercially available. Major headings of this table are discussed as the following.

VDC Rating (V)

This represents the temperature-dependent dc voltage rating of the capacitors in volts. For $T \leq 85°C$, the ratings under the 85°C column apply. In most PPS applications, the maximum temperature specified is either 85°C or 125°C. Obviously, if the specification is 125°C, then the reduced ratings under the 125°C column prevail.

Capacitance (μF)

The capacitance in micro-farad for each capacitor is listed for low, nominal, and high temperatures. The capacitance at 25°C (room temperature), along with the dc voltage rating for a specified temperature, are the key indices in locating a commercial parts. For example, a certain DOS run has identified that the dc voltage needed is 68V and the capacitance needed is 51μF. The temperature range, say, is specified to be between -30°C to +85°C. Then, one determines 75V-capacitor is required for it is the voltage level that is higher than 68V. We don't want to overkill by using 100, 150, or 200V capacitors, for they are generally heavier and more bulky. Having decided on 75V, one looks for the minimum capacitance at -30°C to be larger than the 51μF calculated. From Table 1, the 75V, 100μF capacitor then emerges as the best choice among commercially-available parts.

Often, the DOS run would demand a capacitance that cannot be satisfied by a single capacitor. For example, instead of 51μF, the DOS may identify a value of 151μF. When that happens, three 75V, 100μF capacitors in parallel will have to be chosen in order to achieve a minimum of $3 \times 60 = 180\mu F > 151\mu F$ at -30°C.

Case Size

The case size of capacitors represents their physical dimensions. For foil-tantalum capacitors, there are four different case sizes. For reasons beyond me, case 4 is the smallest size, case 1 is larger than case 4, case 2 is larger than case 1, and case 3 is the largest. They all take the tubular form:

	Length (cm/in)	Diameter (cm/in)
Case 4	2.70/1.062	0.754/0.297
Case 1	3.81/1.500	0.993/0.391
Case 2	5.55/2.187	0.993/0.391
Case 3	7.14/2.812	0.993/0.391

This information should be stored somewhere, and should be made readily available upon user's request.

Weight (grm)

This column gives the weight of each capacitor. Notice that i is only a function of the case size. The larger the case size, the heavier is the weight.

IRMS (A)

This is the RMS current rating for each capacitor, in amperes, at 25°C and a current frequency of 0.05kHz. For other temperatures and frequencies, the correction factors are prescribed by the following equation:

$$\text{AC Current Rating} = (\text{IRMS})(1.175-0.007T)(2.753F^{1/3}) \qquad (1)$$

Where (IRMS) is shown in Table 2, T in °C, and F in kHz. For example, at 85°C and 10kHz, the AC current rating for the first-row capacitor would be:

$$\text{AC Current Rating} = (0.42)(1.175-0.007\text{x}85)(2.753\text{x}10^{1/3}) = 1.43\ \text{A}$$

Since the operating frequency can be different for different DOS applications, it is impossible to present the ac current rating of a given capacitor in Table 1. Consequently, equation (1) must be invoked every time to provide the capacitor current rating for each capacitor in a given application.

ESR (Ohms)

ESR is the abbreviation for "Equivalent Series Resistance." It is of vital importance in all aspects of performance. It is again a function of temperature, being much higher at low temperatures. The capacitor manufacturers are rather uncommittal in their assessment of ESR. As a result, the ESR values presented in Table 1 are by no means final. Using manufacturer's data, the ESR's for all capacitors at a given temperature are identical.

MIL-Spec

This column shows the military specifications governing these capacitors. Most of these specifications do not concern the DOS (e.g., humidity, lead length, etc.).

Q.2 DATA BASE FOR WIRE SIZES

The American Wire Gauge (AWG) will be used as the wire size standard. The wire area is expressed both in circular mils and in $(\text{millimeter})^2$ to facilitate users of different preferences. The resistance per length, expressed in milliohms per meter, is expressed for three different temperatures covering -30°C, +25°C, and +100°C. Calculation of different performances will require the use of milliohms/meter at different temperatures. For worst-case loss evaluation, the 100°C-data will be used. However, for performance such as damping factor of the filter, the opposite low-temperature data will be used.

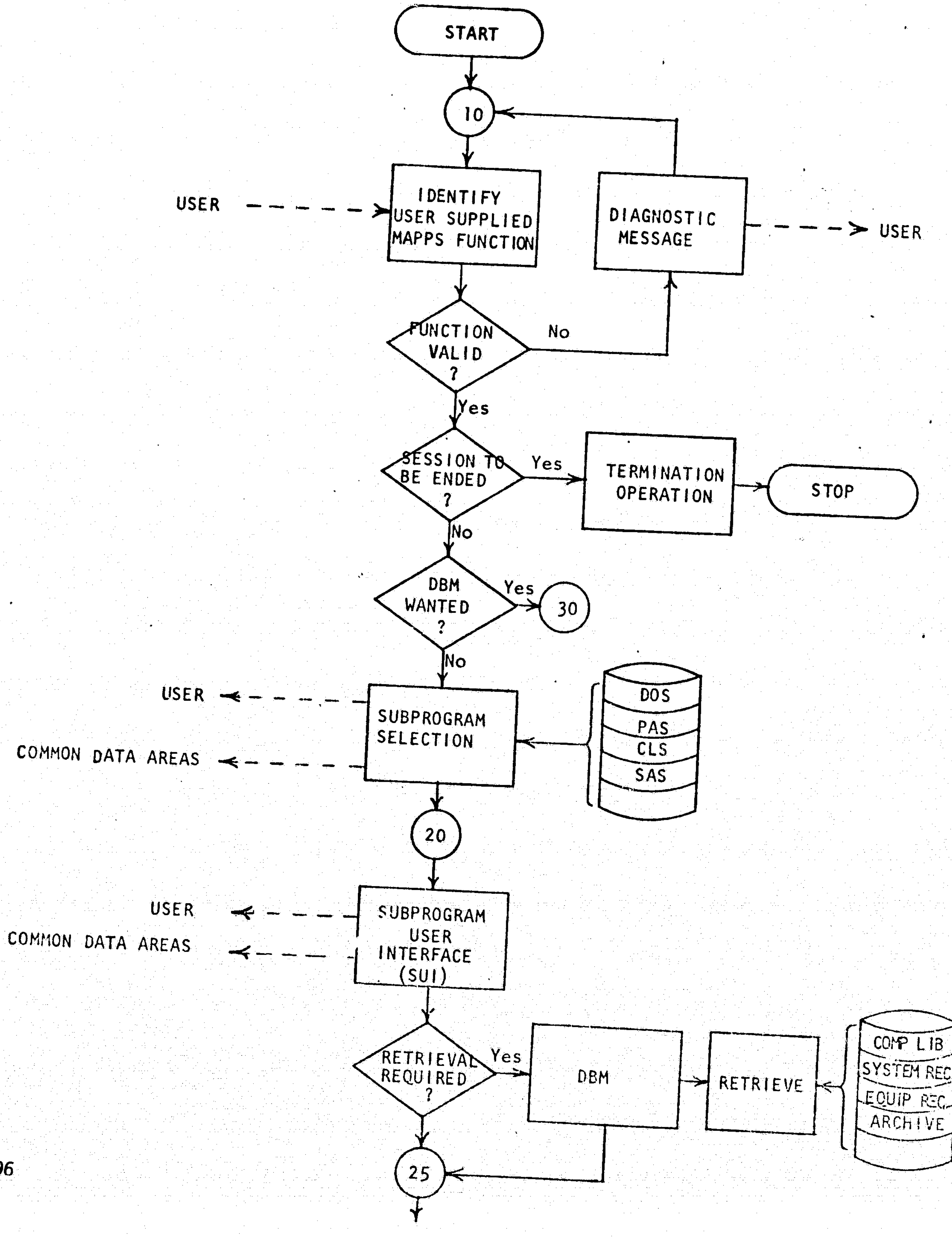
Table 1 Data Base for Foil Tantalum Polarized Capacitors

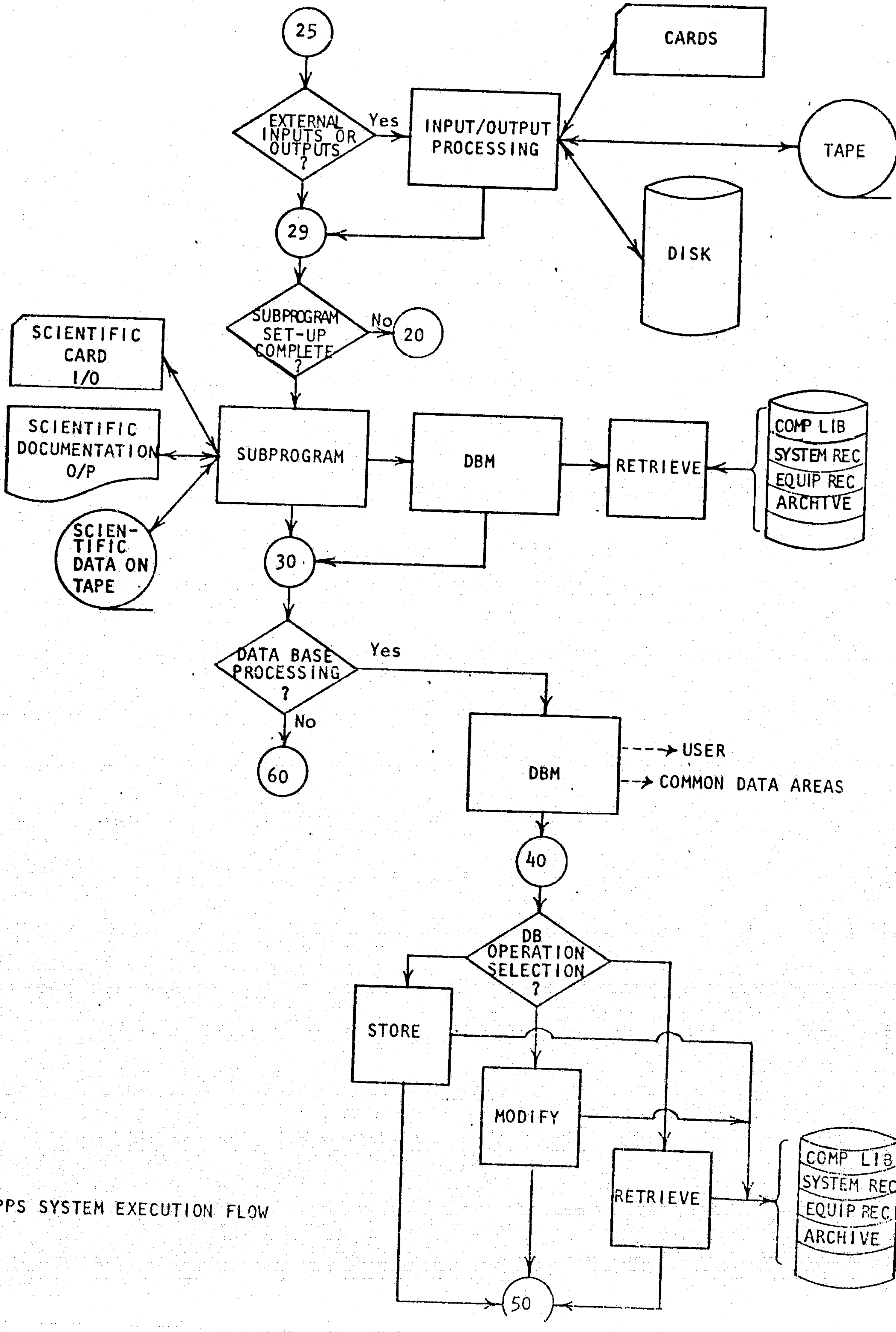
VDC Rating (V)		CAPACITANCE (µF)					DIMENSION		WEIGHT (gm)	IRMS AT 85°C(A)							IRMS AT 125°C (A)							ESR(OHMS)			MIL-SPEC
85°C	125°C	-55°C	-30°C	25°C	85°C	125°C	Length (cm/in)	Diameter (cm/in)		10kHz	20	30	40	50	75	100	10	20	30	40	50	75	100	-30°C	25°C	85°C	
15	10	37	40	55	75	82	3.81/1.500	0.993/0.391	8.0	1.44	1.82	2.08	2.29	2.47	2.82	3.11	0.75	0.94	1.07	1.18	1.28	1.46	1.61	0.5	0.1	0.05	C-39006
25	15	20	24	40	76	105	2.70/1.062	0.754/0.297	3.5	0.48	0.61	0.69	0.76	0.82	0.94	1.04	0.25	0.31	0.36	0.40	0.43	0.49	0.54				
25	15	50	60	100	190	262	3.81/1.500	0.993/0.391	8.0	1.00	1.26	1.44	1.58	1.71	1.95	2.15	0.52	0.65	0.74	0.82	0.88	1.01	1.11				
30	20	54	60	85	110	117	7.14/2.812	0.993/0.391	17.5	2.61	3.29	3.77	4.15	4.47	5.12	•5.63	1.35	1.70	1.95	2.15	2.31	2.64	2.91				
30	20	152	180	300	570	920	7.14/2.812	0.993/0.391	17.5	2.58	3.25	3.72	4.10	4.41	5.05	5.55	1.33	1.68	1.92	2.12	2.28	2.61	2.87				
50	30	3.8	4	6	8	8.3	2.70/1.060	0.754/0.297	3.5	0.38	0.48	0.55	0.60	0.65	0.74	0.82	0.20	0.25	0.28	0.31	0.33	0.38	0.42				
50	30	9	11	18	34	40	2.70/1.060	0.754/0.297	3.5	0.31	0.39	0.45	0.49	0.53	0.61	0.67	0.16	0.20	0.23	0.25	0.27	0.31	0.34				
50	30	12	14	20	28	30	3.81/1.500	0.993/0.391	8.0	0.89	1.13	1.29	1.42	1.53	1.75	1.93	0.46	0.58	0.67	0.73	0.79	0.91	1.00				
50	30	24	28	40	55	60	5.55/2.187	0.993/0.391	13.0	1.58	1.99	2.28	2.51	2.71	3.10	3.41	0.82	1.03	1.18	1.30	1.40	1.61	1.76				
50	30	24	28	47	89	106	3.81/1.500	0.993/0.391	8.0	0.65	0.82	0.94	1.04	1.12	1.28	1.40	0.34	0.43	0.49	0.54	0.58	0.66	0.73				
50	30	76	90	150	285	394	5.55/2.187	0.993/0.391	13.0	1.44	1.82	2.08	2.29	2.47	2.83	3.11	0.75	0.94	1.08	1.19	1.28	1.46	1.61				
75	50	6.5	7	12	23	24	2.70/1.060	0.754/0.291	3.5	0.28	0.35	0.40	0.44	0.47	0.54	0.59	0.14	0.18	0.21	0.23	0.24	0.28	0.31				
75	50	7.5	9	15	28	34	3.81/1.500	0.993/0.391	8.0	0.41	0.52	0.60	0.66	0.71	0.81	0.90	0.21	0.27	0.31	0.34	0.37	0.42	0.46				
75	50	17	20	33	63	74	3.81/1.500	0.993/0.391	8.0	0.55	0.69	0.79	0.87	0.94	1.08	1.19	0.28	0.36	0.41	0.45	0.49	0.56	0.61				
75	50	24	30	40	50	55	7.14/2.812	0.993/0.391	17.5	1.79	2.23	2.58	2.84	3.06	3.50	3.85	0.93	1.17	1.33	1.47	1.58	1.81	1.99				
75	50	24	28	47	89	123	3.81/1.500	0.993/0.391	8.0	0.65	0.82	0.94	1.04	1.12	1.28	1.41	0.34	0.43	0.49	0.54	0.58	0.66	0.73				
75	50	39	42	70	120	137	5.55/2.187	0.993/0.391	13.0	1.03	1.30	1.49	1.64	1.76	2.02	2.22	0.53	0.67	0.77	0.85	0.91	1.04	1.15				
75	50	72	20	100	175	195	5.55/2.187	0.993/0.391	13.0	1.20	1.52	1.74	1.91	2.06	2.36	2.59	0.62	0.78	0.90	0.99	1.06	1.22	1.34				
100	65	13	15	25	37	42	3.81/1.500	0.993/0.391	8.0	0.52	0.65	0.74	0.82	0.88	1.01	1.11	0.27	0.34	0.38	0.42	0.46	0.52	0.57				
100	65	28	30	50	75	85	5.55/2.187	0.993/0.391	13.0	0.86	1.08	1.24	1.37	1.47	1.68	1.85	0.44	0.55	0.64	0.71	0.76	0.87	0.96				
100	65	38	45	75	130	141	7.14/2.812	0.993/0.391	17.5	1.24	1.56	1.79	1.97	2.12	2.42	2.67	0.64	0.81	0.92	1.02	1.10	1.25	1.38				
150	100	1.2	1.5	2	2.5	2.8	2.70/1.060	0.754/0.297	3.5	0.21	0.26	0.30	0.33	0.35	0.40	0.44	0.11	0.13	0.15	0.17	0.18	0.21	0.23				
150	100	2.2	3	4	6	6.7	2.70/1.060	0.754/0.297	3.5	0.14	0.17	0.20	0.22	0.24	0.27	0.30	0.07	0.09	0.10	0.11	0.12	0.14	0.15				
150	100	5	7	10	15	17	3.81/1.500	0.993/0.391	8.0	0.31	0.39	0.45	0.49	0.53	0.61	0.67	0.16	0.20	0.23	0.25	0.27	0.31	0.34				
150	100	7.5	9	15	29	34	3.81/1.500	0.993/0.391	8.0	0.38	0.48	0.55	0.60	0.65	0.74	0.82	0.20	0.25	0.28	0.31	0.33	0.38	0.42				
150	100	14	15	25	47	49	5.55/2.187	0.993/0.391	13.0	0.62	0.78	0.89	0.98	1.06	1.21	1.33	0.32	0.40	0.46	0.51	0.55	0.63	0.69				
150	100	17	20	33	62	75	5.55/2.187	0.993/0.391	13.0	0.72	0.91	1.04	1.15	1.24	1.41	1.56	0.37	0.47	0.54	0.59	0.64	0.73	0.80				
150	100	24	28	47	89	107	7.14/2.812	0.993/0.391	17.5	0.99	1.26	1.44	1.58	1.71	1.95	2.15	0.51	0.65	0.74	0.82	0.89	1.01	1.11				
200	150	1	1.2	1.5	1.8	2	2.70/1.060	0.754/0.297	3.5	0.17	0.22	0.25	0.27	0.29	0.34	0.37	0.09	0.11	0.13	0.14	0.15	0.17	0.19				
200	150	6.5	7	10	12	13	5.55/2.187	0.993/0.391	13.0	0.83	1.04	1.19	1.31	1.41	1.62	1.78	0.43	0.54	0.62	0.68	0.73	0.84	0.92				
200	150	9.6	11	15	18	20	7.14/2.812	0.993/0.391	17.5	1.14	1.43	1.64	1.80	1.94	2.22	2.45	0.59	0.74	0.85	0.93	1.00	1.15	1.26				

Table 2   Data Base For Wire Conductors

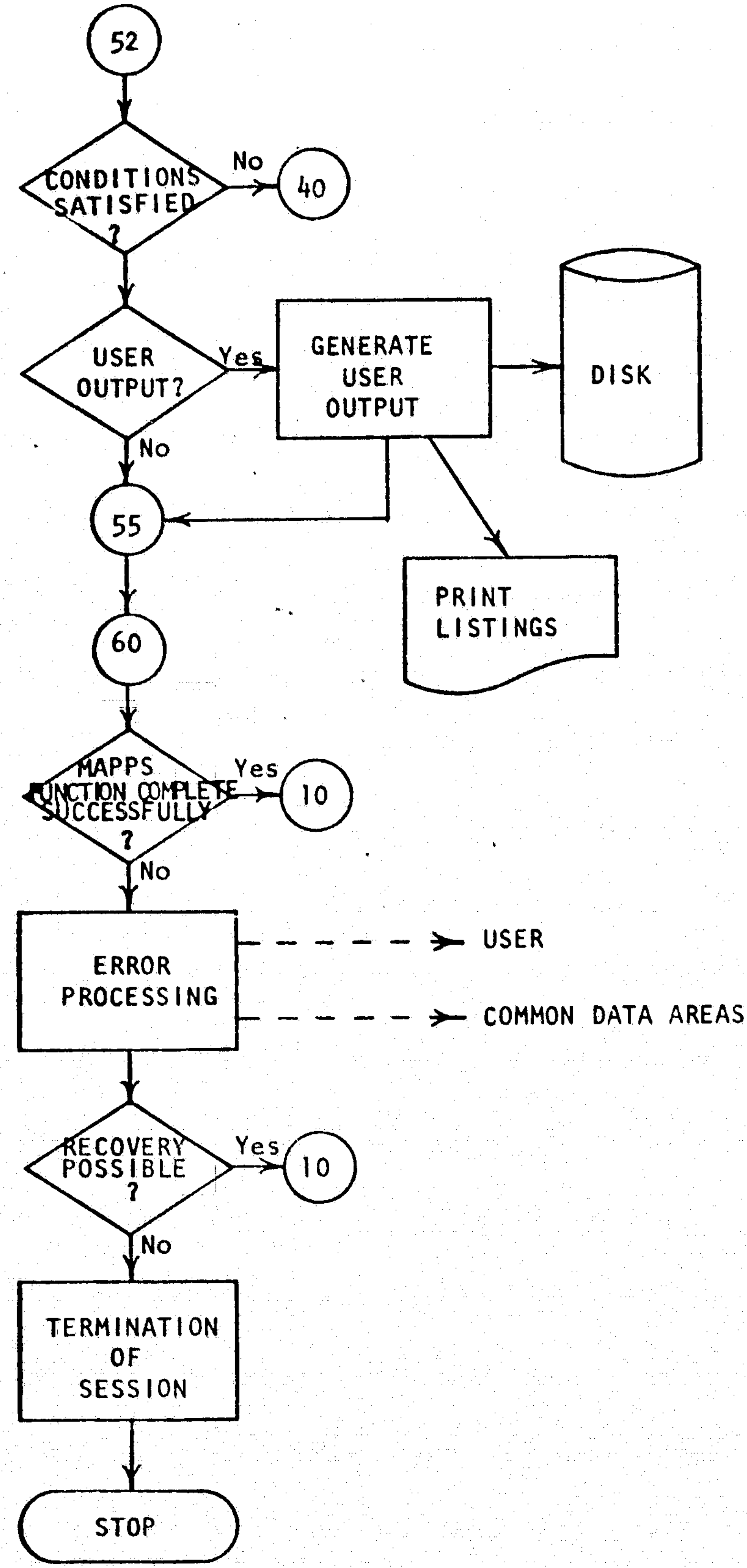
Wire Size AWG	Wire Area		Resistance/Length (milliohms/meter)		
	Cir Mil	$(mm)^2$	-30°C	+40°C	100°C
8	18010	9.127	1.67	2.18	2.67
9	14350	7.272	2.11	2.75	3.37
10	11470	5.812	2.66	3.47	4.25
11	9158	4.641	3.35	4.38	5.36
12	7310	3.704	4.22	5.52	6.75
13	5852	2.965	5.32	6.96	8.51
14	4679	2.371	6.71	8.77	10.7
15	3758	1.904	8.46	11.0	13.5
16	3003	1.522	10.7	14.0	17.1
17	2421	1.227	13.4	17.6	21.5
18	1936	0.981	16.9	22.1	27.1
19	1560	0.791	21.4	28.0	34.2
20	1246	0.631	26.9	35.2	43.0
21	1005	0.509	33.9	44.4	54.3
22	807	0.409	43.1	56.3	68.9
23	650	0.329	53.9	70.5	86.3
24	524	0.266	68.2	89.2	109
25	424	0.215	85.9	112	137
26	342	0.173	109	143	175
27	272	0.138	137	179	219
28	219	0.111	173	227	277
29	180	0.091	216	283	346
30	144	0.073	275	360	440
31	117	0.059	347	454	556
32	96	0.049	431	563	689
33	77	0.039	547	715	874
34	61	0.031	694	908	1110
35	49	0.025	879	1149	1405
36	40	0.020	1102	1441	1762
37	33	0.017	1361	1779	2176
38	26	0.013	1723	2252	2754
39	20	0.010	2250	2942	3598
40	16	0.008	2870	3752	4588
41	13	0.007	3516	4597	5622
42	10	0.005	4410	5765	7050
43	8	0.004	5596	7447	9106
44	7	0.004	6891	9010	11018

MAPPS SYSTEM EXECUTION FLOW





MAPPS SYSTEM EXECUTION FLOW

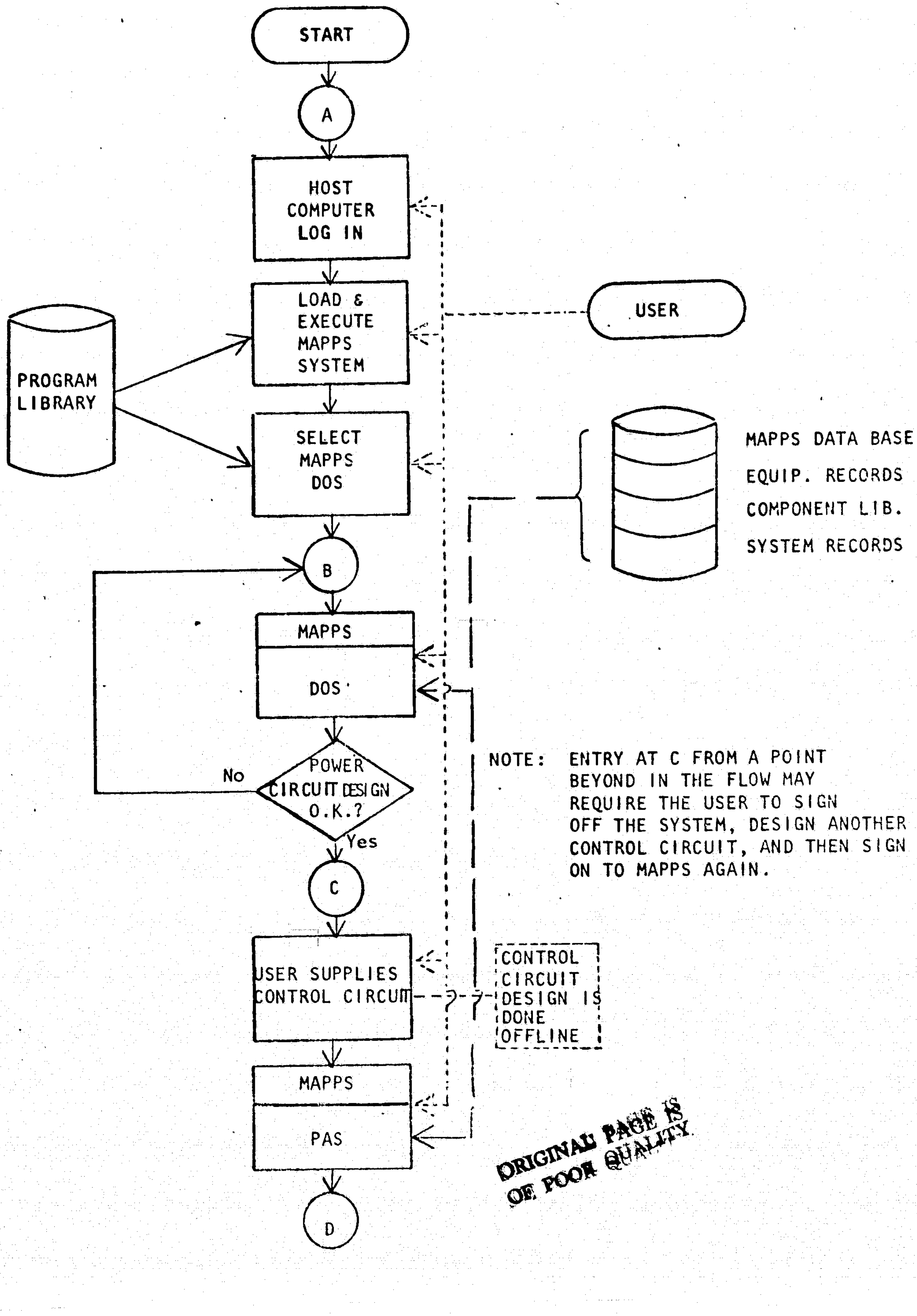

52
CONDITIONS SATISFIED ?
No
40
USER OUTPUT?
Yes
GENERATE USER OUTPUT
DISK
No
55
PRINT LISTINGS
60
MAPPS FUNCTION COMPLETE SUCCESSFULLY ?
Yes
10
No
ERROR PROCESSING
USER
COMMON DATA AREAS
RECOVERY POSSIBLE ?
Yes
10
No
TERMINATION OF SESSION
STOP

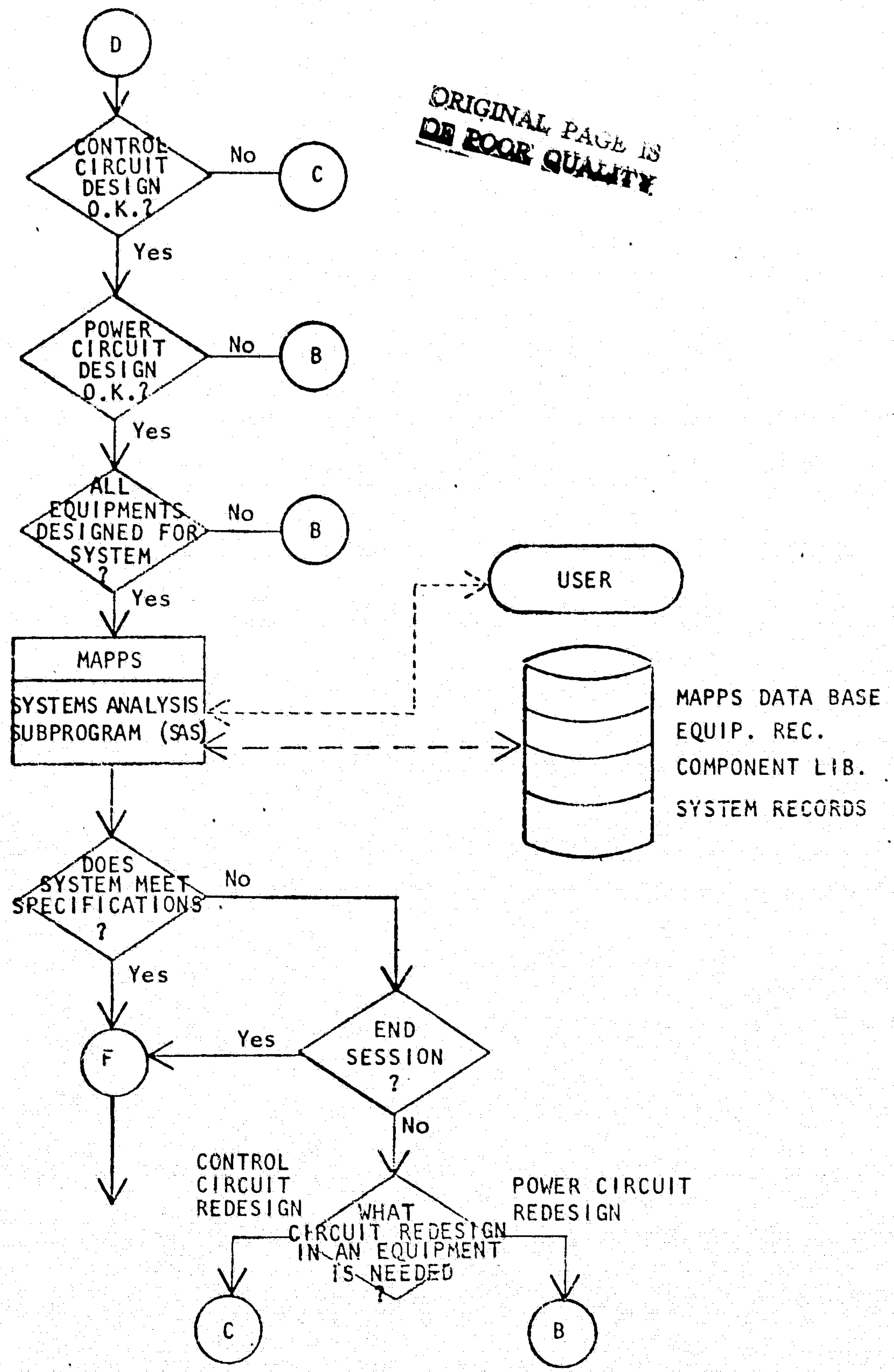
APPENDIX S

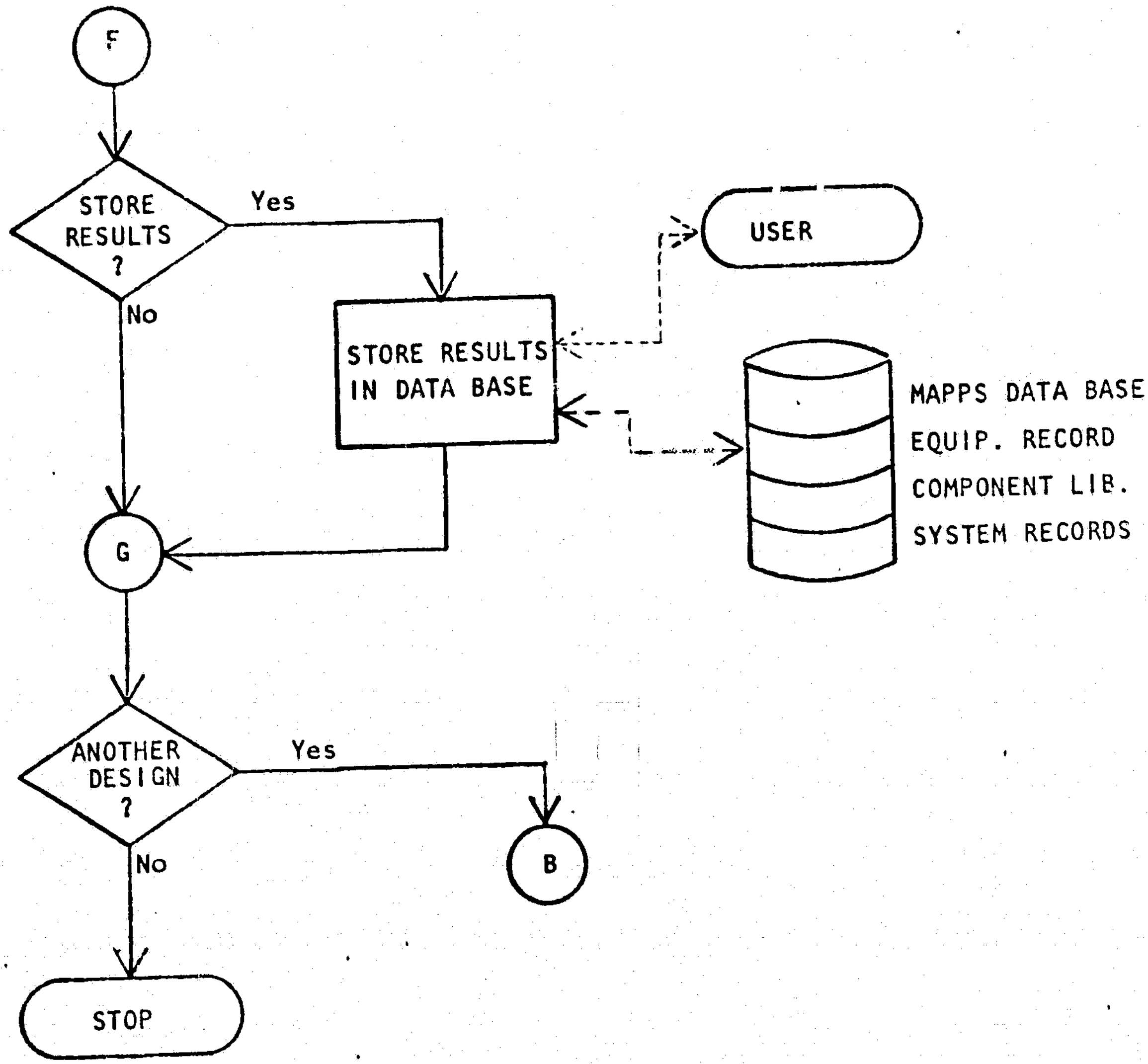
DATA BASE MANAGEMENT COMMON DATA AREA (DBMCOM)

DBFNR	Data Base File Number
DBTF	Data Base Table File
SETNAM	Set Name
RECNAM	Record Name
ITMNAM	Item Name
DBIERR	Data Base Error Code
DBKEY	Data Base Record Key Identifier
DBARY	Data Base Array
DBRA	Data Base Record Area
DBFSW	Data Base Function Switch
DBNBUF	Data Base Number of Buffers
DBFUNC	Data Base Function

MAPPS POWER PROCESSING SYSTEM DESIGN PROCESS




D
CONTROL CIRCUIT DESIGN O.K.?
No
C
Yes
POWER CIRCUIT DESIGN O.K.?
No
B
Yes
ALL EQUIPMENTS DESIGNED FOR SYSTEM ?
No
B
Yes
USER
MAPPS
SYSTEMS ANALYSIS SUBPROGRAM (SAS)
MAPPS DATA BASE
EQUIP. REC.
COMPONENT LIB.
SYSTEM RECORDS
DOES SYSTEM MEET SPECIFICATIONS ?
No
Yes
F
Yes
END SESSION ?
No
CONTROL CIRCUIT REDESIGN
WHAT CIRCUIT REDESIGN IN AN EQUIPMENT IS NEEDED ?
POWER CIRCUIT REDESIGN
C
B


F
STORE RESULTS ?
Yes
No
STORE RESULTS IN DATA BASE
USER
MAPPS DATA BASE
EQUIP. RECORD
COMPONENT LIB.
SYSTEM RECORDS
G
ANOTHER DESIGN ?
Yes
No
B
STOP

APPENDIX U

MODELING AND ANALYSIS OF POWER PROCESSING SYSTEMS*

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ABSTRACT

Effort of a NASA-sponsored, computer-based program on "Modeling and Analysis of Power Processing Systems" is reported. The overall program objective is to provide an engineering tool to reduce the design, analysis and development time, and thus the cost, in achieving the required performances for power processing equipment and systems. Program structures, and design/analysis examples are given to illustrate the program's utility in power and control circuit design, performance analysis, and design optimization.

1. INTRODUCTION

Electric power processing technology is a rather complex field encompassing disciplines of power conversion and control electronics, magnetics, and analog as well as digital signal processing. However, primarily due to its rapidly-evolving nature and its preoccupation with hardware production, the technology development has been hampered by the lack of vigorous modeling, analysis, design, and optimization techniques. As a result, heavy reliance on empirical and intuitive methods has become the necessary ingredient in power processing equipment designs. Needless to say, such inadequacies inevitably lead to penalties involving equipment performance, weight, reliability, and cost. In view of (1) the forthcoming needs for use of considerably higher level of power in future missions, (2) the prevailing trend of equipment standardization which must rely on an analysis-based design, and (3) the ever-increasing sensitivity on equipment cost, in which brute-force and single-minded power processing techniques would only result in more severe penalties than those suffered today, the pressing need for power processing modeling and analysis cannot be overemphasized.

To fulfill such a need, a program entitled "Modeling and Analysis of Power Processing Systems (MAPPS)", is described in this paper. Being a long-range program, it is currently at the conclusion of the initial Phase II effort. Phase I of the program addressed the formulation of a methodology for the MAPPS approaches [1]. In the initial Phase II, certain selected approaches were implemented through computer-based subprograms dealing with design, analysis, and optimization at the equipment level. To provide the basic coordination for the various subprograms, the framework of an expandable Data Management Program is also completed within the initial Phase II.

In the following sections, commonly-used power processing terminologies are defined first to avoid later ambiguity. MAPPS subprogram categories and their specific objectives with respect to analysis, design, and optimization are next described; examples are provided to illustrate each subprogram category. Following a short introduction of the data management program, the eventual MAPPS capability and its future are concluded.

2. COMMONLY-USED TERMS AND MODELING/ANALYSIS OBJECTIVE

Certain basic terms frequently used in this paper are summarized as the following to facilitate terminology clarification:

Component:	Electronic parts such as magnetics, capacitors, semiconductors, etc.
Circuit:	A combination of electronic circuits to perform a given function. Examples are input filter, output filter, feedback amplifiers, etc.
Equipment:	A black box containing many components to satisfy certain specified input/output compatibilities. Examples are line regulators, dc to dc converters, etc. An equipment can be divided into the power circuit and the control circuit; the former processes the power flow from input to output, the latter controls the power flow.
System:	A combination of multiple equipment aimed to fulfill source/load power processing application in a spacecraft.

* This work was performed under NASA Contrace NAS3-19690, "Modeling and Analysis of Power Processing Systems," by TRW Defense and Space Systems, Redondo Beach, California, for NASA Lewis Research Center.

Performance: Steady-state or transient behavior of the equipment or system.

Design: Conceive a scheme for equipment or system to meet a given set of performance requirements.

Analysis: Analytically/numerically determine the performance of a given design.

Design Optimization: To design equipment or system and concurrently to minimize a defined quantity (such as weight or loss).

Performance Requirements: (Control-independent) These requirements are closely associated with the power circuit design:

- Source EMI
- Output Ripple
- Weight
- Loss
- Input/Output Voltage Levels
- Load Power

Performance Requirements: (Control-dependent) These requirements are closely associated with the control circuit design:

- Stability
- Attenuation of Source Disturbances (audiosusceptibility)
- Response to Load Disturbances (output impedance)
- Response to Step Line/Load Changes
- DC Regulation

Based on these defined terminologies, the MAPPS overall objective is to provide the engineering tools to reduce the design, analysis, and optimization time, and thus the development time and the cost, in achieving the required performances for power processing equipment and systems.

3. MAPPS MAJOR SUBPROGRAMS

The four major MAPPS subprograms, designated as Design Optimization (DOS), Control Design (CDS), Performance Analysis (PAS), and System Analysis (SAS), are described in Table 1.

For detailed information regarding contents of Table 1, the readers are referred to reference [2], to be published in Fall, 1977. The Data Management Program mentioned in Section 1, which coordinates the user interfaces for all subprograms, will also be treated thoroughly in [2].

In this paper, each subprogram will be represented by key examples illustrating the utility and the effectiveness of the subprograms. While they are inherently computer-based, the design requirements and the analytical foundation leading to the formulation of the particular subprogram are present to supplement the numerical demonstration of the analytical results.

4. DESIGN OPTIMIZATION SUBPROGRAM (DOS)

As previously stated, the utility of the design optimization is that it will not only pinpoint the detailed equipment design to meet given performance specifications, but also achieve the minimization of a certain equipment characteristic deemed desirable by the designer. Simply stated, the task is to minimize an objective function $f(x,k)$, subject to design constraints $g_j(x, k, r)=0$.

Here, $x = (x_1,x_2,\dots x_n)^T$ is a n-dimensional vector representing circuit parameters to be determined. Examples of x include the values of R, L, and C, the operating frequency, and the design details of magnetic components including the effective core area, the mean core length, the permeability, the wire size, and the number of winding turns.

The k's represent various constants known from common knowledge or designer's experience. Examples include copper resistivity, core and winding densities, core window fill factor, saturation flux density, capacitor energy-storage capabilities, etc.

The r's are performance specifications which the optimum design must meet. Examples include filter attenuation, output ripple amplitude, maximum weight, minimum efficiency, source EMI, etc. These requirements are usually prescribed to the equipment designer by someone presumably knowledgeable in the entire power system.

The function $f(x,k)$ is the particular equipment characteristic to be optimized. Examples include the total weight, the total loss, the figure of merit of a specific design, or any other preferable design quantity such as reliability and cost.

Equation $g_j(x,k,r) = 0$ represent a total of "j" constraints relating x, k, and r. For example, one of the equations may relate the filter attenuation required at a given frequency to the RLC filter parameters, and a second equation may relate the sum of all losses to the required efficiency. The number of constraints will be sufficiently large to allow all requirements "r" and all constants "k" to be integrated into governing the design of all circuit parameters "x". Consequently, solutions acquired for equations $g_j(x,k,r) = 0$ to minimize the objective function $f(x,k)$ would authentically portray a detailed optimum design, down to the component level, in accordance with the performances and the optimization objective specified.

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TABLE 1. SUBPROGRAM DESCRIPTIONS

SUBPROGRAMS / DESCRIPTIONS	DESIGN OPTIMIZATION SUBPROGRAMS (DOS)	CONTROL DESIGN SUBPROGRAMS (CDS)	PERFORMANCE ANALYSIS SUBPROGRAMS (PAS)	SYSTEM ANALYSIS SUBPROG (SAS)
Basic Objective	Power Circuit Design including Optimum Switching Frequency Selection	Control Circuit Design to meet specified regulator performances	Regulator performance analysis for a given power and control circuit design.	Optimum system configuration and propagation of large-signal disturbance within a system.
Utility	Allow one to conceive a power component or a power circuit design to meet all control-independent performances, and concurrently optimize a certain design quantity deemed as particularly desirable by the designer. The quantity can be weight, loss, or any other physically-realizable entity.	Allow one to perform a control-circuit design based on a given set of control-dependent performance specifications. The power circuit design and the switching frequency are assumed given, perhaps from the DOS applications.	Allow one to predict control-dependent performance characteristics of a given equipment design. By necessity, standardized control-circuit configurations, including both single and multiple-loop control concepts, are used for PAS.	To provide a power processing system designer with proper design and tradeoff tools, thus minimizing the need for subjective bias from the system designer by providing a common linkage between the system engineers and equipment design engineers.
Design/ Analysis Categories	• Magnetics components • Circuits • Equipment	• Single-loop control • Multiple-loop control	• Continuous frequency domain analysis and its worst case • Discrete time domain analysis • Discrete time domain cost-effective simulation	• System configuration design including source, energy storage and power processing equipment • Dynamic intra-system interactions
Major Difficulty in Subprogram Implementation	Fast convergence of optimization routines.	Provide concise design guidelines for a complex regulator with high-order input/output filters and loop compensation.	NONE	Extreme complexity of a complete power processing system.
Initial Phase II Accomplishments	• Implement inductor and transformer design optimization • Implement input filter design optimization • Implement buck switching regulator design optimization	• Buck switching regulator control circuit design using standardized amplifier compensation • Ready to incorporate multiple-loop control-circuit design currently in progress through other R & D programs.	• Establish analytical/computational tools for all above categories • Implement three PASs for single- and multiple-loop controlled converters.	• Complete a design for source-regulator system • Demonstrate a cost-effective time-domain simulation for a 12th order system.
Eventual Expectation	Optimum design and switching-frequency selection, including values and ratings of all power and magnetic components, for all commonly-used power-circuit configurations.	Reduction of "bench-design" effort during breadboard stage. In the limit, achieve confident design without breadboarding.	Accurate and cost-effective equipment control-dependent performance predication including worst-case.	A more "scientific" system design and analysis approach relative to the present state-of-the-art.

From the foregoing description, the key to implementing the design optimization rests on suitable mathematical or computer techniques that can be used to solve the simultaneous constraints and concurrently minimize the objective function. However, only few problems with rather simplistic nature can be solved in closed form, using techniques such as Lagrange Multipliers [3,4]. Most larger problems arising from practical applications are sufficiently complicated that, to identify their optimum solutions, one has to resort to computational means.

In the initial Phase II, the following five DOS's have been successfully implemented:

- Optimum weight inductor/transformer design, with loss constraint given.
- Optimum weight inductor/transformer design, with wire size given.
- Optimum loss inductor/transformer design, with weight constraint given.
- Optimum weight input filter design.
- Optimum weight buck switching regulator design.

The first and the last subprograms are given here as illustrative examples.

Using the method of Lagrange Multipliers, the closed-form solutions for the first example have been presented [4]. The solutions prescribe a minimum-weight inductor design through core area A, core length Z, number of turns N, permeability U, core colume AZ, conductor area AC, and minimum weight W. These parameters, in turn, are expressed as functions of the copper density DC, the iron density DI, winding pitch factor FC, window filling factor FW, resistivity RHO, loss constraint P, flux density BS, peak winding current IP, and the needed inductance L. These closed-form solutions are implemented into a computer-based subprogram. Upon executing the subprogram on a remote terminal, the computer will provide the following printout of instruction for an uninitiated user:

```
THE OBJECTIVE OF THIS PROGRAM IS TO PERFORM AN
OPTIMUM WEIGHT INDUCTOR DESIGN FOR A GIVEN LOSS.
TO USERS: PLEASE READ THE FOLLOWING STATEMENTS
   CAREFULLY BEFORE EXECUTING THE PROGRAM.
THE NEEDED INPUT PARAMETERS ARE THE FOLLOWING:
   DC  : CONDUCTOR DENSITY IN GRAMS CUBIC CM.
         IF NOT GIVEN BY THE USER, DC IS SET
         AT 8.9 BY DEFAULT.
   DI  : CORE DENSITY IN GRAMS CUBIC CM.
         IF NOT GIVEN BY THE USER, DI IS SET
         AT 7.8 BY DEFAULT.
   FC  : RATIO OF AVERAGE ONE TURN LENGTH TO THE
         CORE CIRCUMFERENCE.
         IF NOT GIVEN,FC IS SET AT 2. BY DEFAULT.
   FW  : RATIO OF CONDUCTOR AREA TO WINDOW AREA.
         IF NOT GIVEN, FW IS SET AT .4 BY DEFAULT.
   RHO : CONDUCTOR RESISTIVITY IN OHM-METER. IF
         NOT GIVEN, RHO IS SET AT 1.724E-8 BY DEFAULT.
   P   : DESIGNED POWER LOSS IN WATTS.
   BS  : MAXIMUM FLUX DENSITY IN KILOGAUSSES.
   IP  : PEAK INDUCTOR CURRENT IN AMPERES.
   L   : DESIGNED INDUCTANCE IN MICROHENRIES.
 PLEASE GIVE INPUT DATA FOR L,IP,BS,AND P BELOW.
 PLEASE ALSO GIVE INDIVIDUAL INPUT DATA FOR DC,DI,
   FC,FW,AND RHO IF ANY OF DEFAULTED SETTINGS IS
   NOT DESIRED.
 NO INPUT IS NEEDED IF DEFAULTED SETTINGS ARE USED.
 FOR ANSWERS AT THE END OF THE RUN,
 A IS CORE AREA, Z IS MEAN CORE LENGTH,
 N IS NUMBER OF TURNS, U IS PERMEABILITY,
 AZ IS PRODUCT OF A AND Z,AC IS CONDUCTOR AREA PER
 TURN,W IS OPTIMUM INDUCTOR WEIGHT FOR A GIVEN P.
```

Subsequently, the computer will request input data from the user with regard to L, IP, BS, P, DC, DI, FC, FW, and RHO. This is the only information the user is required to furnish. In this example, the user needs a 200-uH inductor carrying a peak current of 4.5 A based on a core having a 3.5 kilogauss flux capability. The loss allowed is 0.699 W. For values of DC, DI, FC, FW, and RHO, the user selects to use those set by the program in the absence of any user's input. The user then types:

```
L=200.,IP=4.5,BS=3.5,P=0.6991$
```

Upon completion of input data, the computer prints out a summary of these inputs:

```
DC     = 8.9,
DI     = 7.8,
FC     = 2.0,
FW     = 4.0E-01,
RHO    = 1.724E-08,
P      = 6.991E-01,
BS     = 3.5,
IP     = 4.5,
L      = 2.0E+02,
```

Finally, the optimum design parameters, along with their conventional units, are computed and delivered as outputs:

```
A = 5.939E-01     SQUARE CENTIMETERS
Z = 6.391E+00     CENTIMETERS
N = 1.661E+01     TURNS
U = 1.094E+02     GAUSS-OERSTED
AZ= 4.475E+00     CUBIC CENTIMETER
AC= 2.419E+03     CIRCULAR MIL
W = 2.085E+01     GRAMS
```

The cost for this design session is $0.51. This compares to hours and perhaps days of design iterations using paper-and-pencil approach.

The next example deals with optimization on a vastly-expanded scale - an optimum-weight design for the complete buck switching-regulator power circuit shown in Figure 1.

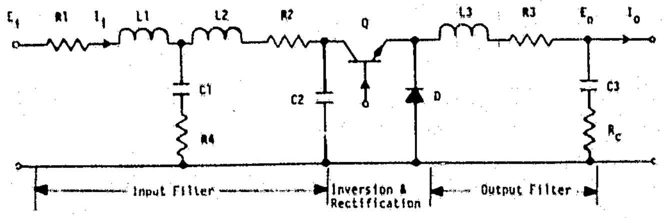

Figure 1 Buck Power Circuit

Here, R1 to R3 are winding resistances of L1 to L3, respectively. The input filter is composed of L1-C1-R4-L2-C2, with L3-C3 being the output filter, and RC being the ESR of C3. Counting in addition the area A, turns N, length Z, and conductor area AC required to completely define each inductor, and including the switching frequency F, a total of twenty-three variables are involved. These variables, along with design constraints that include efficiency, source current ripple, output voltage ripple, input filter resonance, full utilization of inductor window areas, and no inductor saturation, are presented in Table 2. Most constraints are complicated nonlinear functions of the aforementioned variables; the most complicated one being equation (1) of Table 2, which includes copper losses, semiconductor conduction losses, capacitor dissipations, and frequency-dependent core losses and semiconductor switching lesses. The objective of the optimum design is to solve for all variables, with the intent to satisfy each constraint, and concurrently minimize the optimization criterion - the total weight of copper, iron, capacitors, and the heat sink. Notice in particular the switching frequency is not a pre-set value; its optimum design is an integral part of the total converter design.

Table 2 Design Optimization Summary

Variables	(Components)	L1	L2	L3	R1	R2	R3	R4	C1	C2	C3	f
A	Core Cross-sectional area	X	X	X								
N	Number of turns	X	X	X								
AC	Area per turn of conductor	X	X	X								
Z	Mean length of core	X	X	X								
L	Inductance needed	X	X	X								
R	Winding & external resistance				X	X	X	X				
C	Capacitance needed								X	X	X	
f	Switching frequency											X

Requirements	Constraints	
P_o = Output power	$P_o(1-e)/e$ = (input filter loss) +(transistor and diode losses) +(output filter loss)	(1)
e = Minimum efficiency required		
E_i = Input voltage range		
S = Frequency-dependent source ripple	$S = f_1(L1,L2,L3,C1,C2,R4,F,P_o,E_i,E_o)$	(2)
E_o = Output voltage		
r = Output ripple	$r = f_2(L3,C3,RC,F,E_i,E_o)$	(3)
P_e = Maximum input-filter resonant peaking	$P_e = f_3(C1,C2,L1,L2,R4)$	(4)
Full window	$f_4(ACk,Nk,Zk,Ak) = 0,\ k=1,2,3$	(5,6,7)
No inductor saturation	$f_5(Nk,Ak,Lk,P_o,E_i) = 0,\ k=1,2,3$	(8,9,10)

Optimization Criterion

Weight W : Iron weight + Copper weight + capacitor weight + Heat sink weight

$= f_7[\Sigma(Ak\ Zk)] + f_8[\Sigma(Ck \cdot Nk \cdot Ak)] + f_9(\Sigma Ck) + f_{10}P_o(1-e)/e$

Obviously, a problem of this complexity is not amenable for closed-form solutions. The nonlinear programming algorithm, SUMT, is used to conceive the design numerically [5]. The computer program for this problem contains fourteen pages of Fortran listing dealing mostly with constraints and their first and second partial derivatives. Considering the limited information such a listing can provide without extensive descriptive elaborations, the program itself is not included here. It is, however, available in Reference [2].

Two sets of optimum design results are illustrated in Table 3. The difference between them is that design #1 assumes a three-times higher ESR for the output filter capacitor and a five-times more stringent source EMI requirement than those of design #2. In each design, all RLC parameters, the switching frequency, the design details of all magnetics, and the minimum weight, are collectively achieved in a single run. The design not only meets all specified performances, it also represents the minimum possible weight.

Table 3 Optimum Design Results

	Design #1 (ESR 0.3 ohm, S= 0.1A)	Design #2 (ESR = 0.1 ohm, S= 0.5A)
Z1 (cm)	5.10	3.11
A1 (cm^2)	0.438	0.161
N1 (turns)	40	21
AC1 (mm^2)	0.725	0.519
Z2 (cm)	3.86	2.36
A2 (cm^2)	0.251	0.092
N2 (turns)	22	12
AC2 (mm^2)	0.756	0.507
Z3 (cm)	7.84	5.20
A3 (cm^2)	0.694	0.235
N3 (turns)	46	36
AC3 (mm^2)	1.9	1.21
L1 (μH)	253	53.7
L2 (μH)	84	17.9
L3 (μH)	192	53.5
C1 (μF)	89.5	47
C2 (μF)	30.8	10
C3 (μF)	714	125
R1 (milliohm)	41.5	20.9
R2 (milliohm)	17.9	9.1
R3 (milliohm)	25.3	18.3
R4 (ohms)	2.47	0.94
F (kHz)	22.0	43.9
W (grams)	239.5	78.1

Notice the impact exerted by ESR and source EMI on the two data columns of Table 3. For the same efficiency constraint, every parameter of design #2 is smaller than its counterpart of design #1. The only exception occurs at the analytically-determined optimum switching frequency, where the 43.9 kHz for design #2 is almost twice that of the 22kHz for design #1. Due to the higher frequency and smaller physical parameters, the combined magnetics and capacitor weight for design #2 is barely one-third of of that for design #1.

The total computer cost per run for a problem of this magnitude is generally within the $20-to-$40 range. This compares favorably with days of non-optimum paper-and-pencil design iterations.

The Design Optimization Subprograms thus greatly facilitate the following endeavors heretofore regarded as unattainable:

(1) Allow a cost-effective optimum design from component to equipment level, including the identification of the optimum switching frequency. The cost per run is negligible when compared with days and perhaps weeks of non-optimum design and development iterations.

(2) Provide a fast and accurate weight-efficiency tradeoff as well as a means for ready assessment of the impact of a given requirement or a particular component characteristic on an optimum equipment design.

Continued DOS effort is planned for Phase II of the MAPPS program to extend from the present buck converter to buck boost, boost, and other most-commonly used power-circuit configurations.

5. CONTROL DESIGN SUBPROGRAMS (CDS)

From a feedback control viewpoint, a switching regulator can be generally divided into three major functions: the power stage, the pulse modulation, and the error processor.

The power stage includes the input filter, the power switches, and the output filter. They can be assembled together, in Figure 2A, to form a buck, a boost, and a buck boost circuit. Each circuit can be further divided in accordance with the status of inductor MMF; the MMF can be continuous or discontinuous during nominal operation, as illustrated in Figure 2B. Even though the power stage is a linear circuit during each time interval of Figure 2B, the combination of all different linear circuits for the purpose of analyzing a complete operating cycle becomes a piecewise-linear nonlinear analysis problem. Fortunately, the solution to this problem has made significant advance in recent years, both here and abroad. Approaches based on topology deduction [6,7], discrete time domain modeling [8, 9,10], and average time domain modeling [11] have been successfully performed.

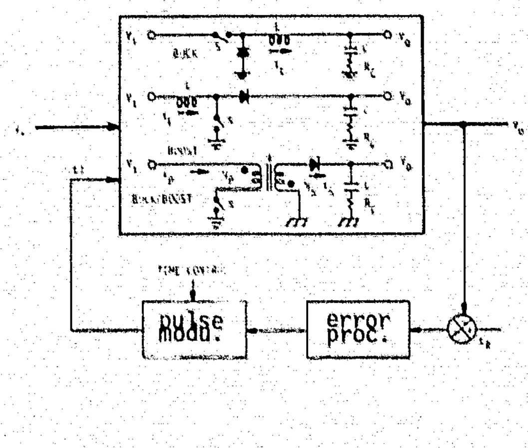

Figure 2A Switching Regulator Major Functions

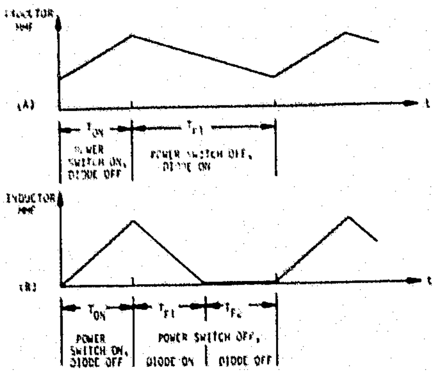

Figure 2B Continuous and Discontinuous Inductor MMF

Depending on the pulse-modulation mechanization, different forms of duty-cycle control of the power switch are possible. These forms include constant frequency, constant on time, constant off time, bistable trigger, and variable frequency based on variable on time and off time. While the ways of pulse-modulation implementation proposed and in use today may appear numerous, they can always be reduced to two basic ingredients; a threshold level and a ramp function. The intersection of these two ingredients initiates the switching action for the duty-cycle control. In single-loop controlled switching regulators, the ramp or the threshold is derived from the output of the error processor, which, in turn, derives its input from sensing the regulated quantity at the output of the power stage. However, in certain more recent multiple-loop developments [12,13], incentive in much improved stability performance has resulted in an additional loop through which the needed ramp generation is obtained from a steady-state ac switching waveform inherent within the regulator. Regardless the details of ramp or threshold generation, when a low-frequency disturbance is applied to the pulse modulation, the time needed for the ramp to intersect the threshold is also perturbed. It is based on this mechanism that the low-frequency pulse-modulation transfer function can be formulated. Essentially, the describing function technique is used to obtain the gain and phase of the pulse-modualtion stage. Certain examples of pulse-modulation analysis are given in Reference [2].

The error processor processes the amplification and compensation of the sensed analog signal at the power-stage output. The analog-to-analog conversion presents no particular difficulty for analysis, as only small signal, linear circuits are involved. However, for most regulators the design of the power stage and the pulse modulation are set by requirements other than control-dependent performances. Consequently, the error-processor design usually determines, to a large extent, the quality of the regulator feedback loop.

The function of the Control Design Subprograms, therefore, is to utilize the analytical results already achieved from the power stage and the pulse modulation, and to determine numerically the design of the error processor based on a pre-selected compensation configuration in order to meet a given set of performance requirements.

As a simple example, the design of the RC compensation in Figure 3 is illustrated. Here, the buck regulator power stage parameters are given: E_i = 25 to 50 V, L = 1 mH, C = 455 uF, R_c = .068 ohms, E_o = 20 V, R_L = 6.7 ohms, and switching frequency = 20 kHz. The values of R1 to R4, C1, C2, and open-loop dc gain K are to be determined so that the following performance requirements can be met:

Crossover frequency = 2 kHz
Phase margin = 40 deg.
Dc regulation at room temperature = .1%

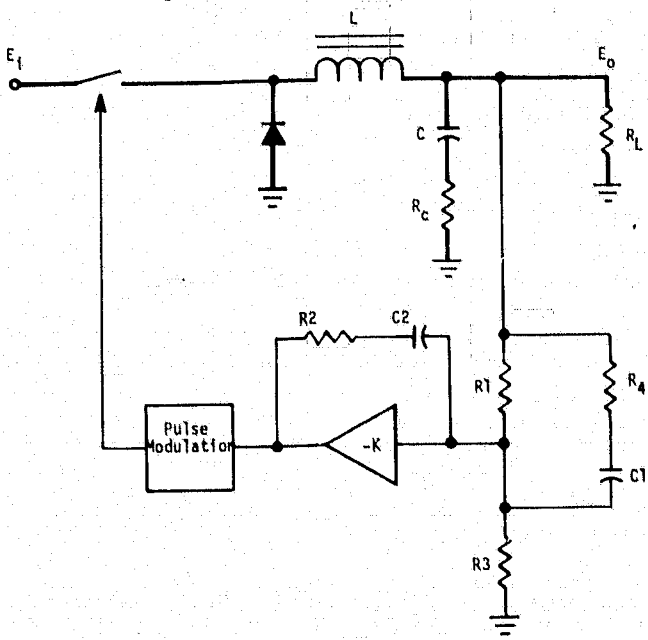

Figure 3. Error Processor RC Compensation

Upon executing the program with the needed inputs, the computer will print out an input summary as shown below:

```
EIMIN   = 2.5E+01,
EIMAX   = 5.0E+01,
EO      = 2.0E+01,
PO      = 6.0E+01,
REG     = 1.0E-03,
L       = 1.0E-03,
C       = 4.55E-04,
RS      = 6.8E-02,
FS      = 2.0E+04,
FX      = 2.0E+03,
THETX   = 4.0E+01,
```

The program then proceeds to calculate all parameters, and prints out the numerical results:

```
DESIGN SYNTHESIS OF COMP. NETWORK
R1= 4.181E+03   R2= 1.0796493558E+04   R3= [illegible]E+03   R4=
2.8436755028E+03
C1= 1.[illegible]E-08   C2= [illegible]E-0[illegible]
MINIMUM OP.AMP.GAIN= 1.[illegible]E+0[illegible]
```

The user can exercise the option to obtain a gain/phase Bode plot for design verification:

DO .DO WHAT BODE ANALYSIS

THETA	FREQ (HZ)	DBEL	MAG	PHASE
5.00	2.7778E+02	36.61	6.7662E+01	49.29
10.00	5.5556E+02	18.54	8.4524E+00	26.56
15.00	8.3333E+02	11.26	3.6551E+00	31.24
20.00	1.1111E+03	6.73	2.1691E+00	36.22
25.00	1.3889E+03	3.49	1.4942E+00	40.41
30.00	1.6667E+03	.99	1.1206E+00	43.80
35.00	1.9444E+03	-1.04	8.8706E-01	46.57
40.00	2.2222E+03	-2.75	7.2849E-01	48.86
45.00	2.5000E+03	-4.23	6.1442E-01	50.22
50.00	2.7778E+03	-5.53	5.2879E-01	52.52
55.00	3.0556E+03	-6.70	4.6241E-01	54.03
60.00	3.3333E+03	-7.75	4.0963E-01	55.41
65.00	3.6111E+03	-8.71	3.6662E-01	56.67
70.00	3.8889E+03	-9.59	3.3150E-01	57.84
75.00	4.1667E+03	-10.40	3.0195E-01	58.94
80.00	4.4444E+03	-11.15	2.7693E-01	59.98
85.00	4.7222E+03	-11.85	2.5551E-01	60.96
90.00	5.0000E+03	-12.50	2.3701E-01	61.88

From this analysis, a 1.85 kHz crossover frequency and a phase margin of approximately 45 deg. is obtained, thus meeting the requirements previously specified. The computer cost for the entire design and analysis is $0.81.

In the continuation of Phase II, the CDS will be expanded to cover other ac performance requirements such as audiosusceptibility and output impedance. All three basic power stages and all commonly-used pulse modulations will be included. Single- and multiple-loop error processors will be incorporated.

6. PERFORMANCE ANALYSIS SUBPROGRAM (PAS)

While the small-signal frequency-domain modeling approach used in the CDS allows a user to gain more insight to enhance the initial parameter design, one also realizes that a switching regulator is inherently a highly nonlinear circuit containing analog-to-discrete-time conversion, and as such, can be more accurately analyzed through the discrete time-domain modeling and analysis. Furthermore, in case of large line/load disturbances, the ensuing duty cycle of a switching regulator is no longer time-invariant. Since any practical equipment is likely to be higher than second order, there is simply no general method applicable to large-signal analysis of such nonlinear systems. Thus, in addition to continuous frequency domain analysis and discrete time-domain analysis for which the operating duty cycle is assumed to be either fixed or step-changed, the discrete time-domain simulation capable of dealing with a time-varying duty cycle must be regarded as an important tool in the PAS. The basic modeling approach, the needed analysis background, and the merits and limitations associated with the frequency-domain analysis and time-domain analysis/simulation are summarized in Table 4.

Techniques for all four approaches given in Table 4 are well established in MAPPS. The most

Table 4 Modeling Approach Descriptions

DESCRIPTION \ MODELING APPROACH	AVERAGE FREQUENCY DOMAIN	EXACT FREQUENCY DOMAIN	DISCRETE TIME DOMAIN ANALYSIS	DISCRETE TIME DOMAIN SIMULATOR
BASIC MODELING	Take advantage of the much lower output-filter resonant frequency in relation to the equipment switching frequency, the nonlinear switching power stage is approximated by a continuous small-signal average model.	Represent the power stage with a linearized discrete impulse response function. The discrete time model is then transferred into the frequency domain.	Exact formulation of state equations, and use iteration method (Newton's) to solve for the exact equilibrium state. Linearized about the equilibrium state to become linear and time-invariant. Z-transformation to frequency domain when needed.	Base on recurrent discrete time-domain analytical expressions, and propagate recurrent equations through Fortran computation.
BACKGROUND NEEDED	Linear control theory and/or linear state space model.	State space techniques.	State space techniques and Fortran programming.	State space techniques and Fortran programming.
MERITS	• Gain more insight on equipment parameter design. • Analytical skill resides in many design engineers. • Readily applicable to high-order circuits and equipment.	• More accurate power stage model at higher signal frequencies, up to one-half of the switching frequency.	• Most accurate stability analysis through eigenvalues. • No need to separate a converter into functional blocks. Most straightforward analysis. • Directly lead to cost-effective performance simulation. • Most suitable for a standardized design.	• Handle large-signal disturbance analysis such as sudden output short and regulator starting. • much faster than general purpose simulation programs such as ECAP, SCEPTRE, etc.
MAJOR LIMITATIONS	Diminishing accuracy beyond 10-15% of switching frequency. Not suitable for high bandwidth regulators.	Difficult to incorporate input filter and pulse modulation.	Basically a numerical approach. No closed-form insight can be gained.	None other than loss of insight generally associated with simulation efforts when not supported by analyses.

applicable PAS for a given design depends on the analysis objective, the accuracy desired, the type of control circuit used, whether the circuit topology is standardized, the nature of the disturbance, and, perhaps most influential, the user's analysis background.. Consequently, the PAS's implemented to date are not limited to any single approach.

Two PAS examples are given here for illustration purposes. They are all based on switching regulators employing a standardized multiple-loop control circuit. The first example analyzes the switching regulator shown in Figure 4 using the discrete-time domain analysis. The options the user can take include the following:

```
ENTER"STOP"TO DISCONTINUE PAS,OTHERWISE "NO"
? N
DO YOU WANT TO CHANGE "PARAM"? (Y OR N)
? N
DO YOU WANT TO CHANGE "COMP"? (Y OR N)
? N
DO YOU WANT NAMELIST? (Y OR N)
? N
DO YOU WANT STABILITY ANALYSIS? (Y OR N)
? N
DO YOU WANT ROOT LOCUS ANALYSIS? (Y OR N)
? N
DO YOU WANT AUDIO ANALYSIS? (Y,N)
? N
DO YOU WANT TRANSIENT ANALYSIS? (Y,N)
```

In this example, subsequent to data input, the user indicates his interest in performing the stability analysis under various line and load conditions. The computer first calculated the three eigenvalues of the regulator corresponding to a 40V input:

```
LAMBDA=     REAL          IMAGINARY
       9.561824E-01    0.
       5.320560E-01    0.
      -1.351678E+00    0.
```

It is found that one of the eigenvalues is outside the unity circle, the converter is thus unstable in this line condition. Next, the three eigenvalues of the regulator corresponding to a 50 V input are calculated as:

```
LAMBDA=     REAL          IMAGINARY
       9.562760E-01    0.
       5.074947E-01    0.
      -9.305425E-01    0.
```

Here, all three eigenvalues are inside the unity circle, signifying a stable system. The load resistance is then increased from 10 ohms to 30 ohms, and the three eigenvalues become:

```
LAMBDA=     REAL          IMAGINARY
       4.383247E-01    0.
       9.559716E-01    0.
       0.              0.
```

Notice one eigenvalue vanishes. The zero eigenvalue corresponds to the status of inductor MMF, which enters discontinuous-current operation (i.e., zero current at the beginning of on time) under light load conditions Again, the regulator is found to be stable.

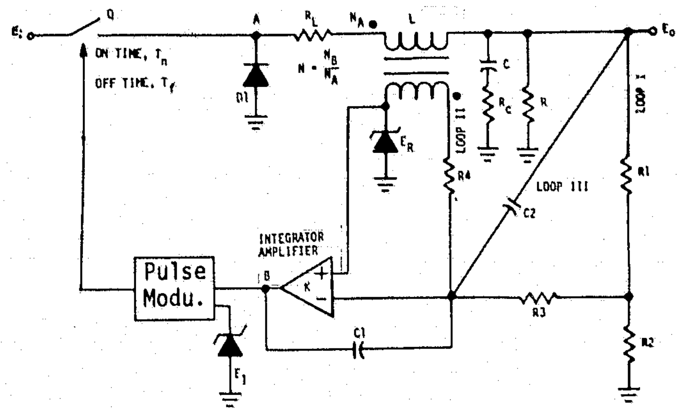

Figure 4. A Buck Regulator

The second PAS example demonstrates the discrete time-domain simulation as applied to the boost regulator shown in Figure 5. Figure 6 shows the simulated inductor current during regulator start-up. The simulation includes the circuit feature of peak-current limiting during severe transients, as is evident from the flat-top envelop at the beginning of the start-up. The measured start-up transient from the flight hardware is in good agreement with the simulation. The total computer cost for this run is $2.04.

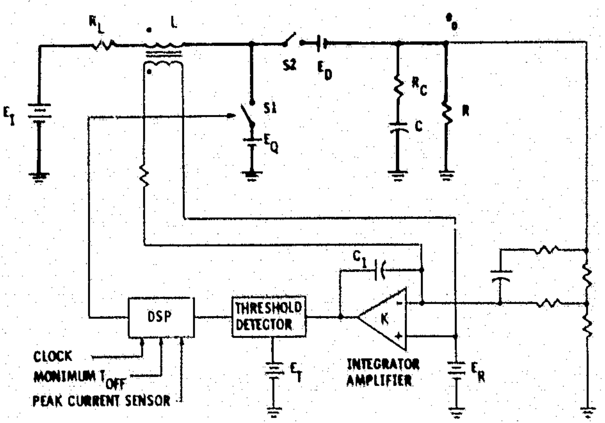

Figure 5. A Boost Regulator

7. SYSTEM ANALYSIS SUBPROGRAMS (SAS)

The SAS's represent an extension of the aforedescribed DOS's and PAS's from equipment to system level. The SAS's rely on DOS's as the basic tool for identifying the optimum system configuration, and on PAS's to address the dynamic system performances under large-signal disturbances.

An example of optimum system configuration is conveniently found in Figure 1 used in the discussion of DOS, in which the total converter weight was optimized under constraints that include a fixed total loss. The example is readily extended to include the source supplying power to the converter. Since the loss in the converter is ultimately derived from the source, what the system designers really want is: for a given source power density (watts/kilogram), how should the converter efficiency be specified so that the combined source and equipment weight can be minimized?

The new objective function thus becomes the sum of power converter weight, the heat-sink weight, and the source weight. Since both the heat-sink weight and the source weight are decreasing functions of converter efficiency while the converter component weight increases with the efficiency, obviously there exists an efficiency at which the combined source and converter weight is at its minimum. Efficiency "e" thus disappears as a design constraint. Instead, it becomes an unknown parameter to be designed by SUMT routine in order to optimize the new objective function.

Without elaboration of programming details, the computer output of optimum design of the circuit of Figure 1 to achieve a minimum combined source-converter weight is shown here. The design includes all circuit and magnetics parameters. It identifies an optimum switching frequency of 22.1 KHz, a target efficiency of 94.1% for the converter, and a minimum combined weight of 7.56 Kg. The total cost for the run is $22.18.

```
SUMT CONVERGED TO A SOLUTION

A1=    4.12993E-05    N1=    24.699
N2=    14.273         AC2=   1.13267E-06
C1=    1.32593E-04    C2=    1.90135E-05
R1=    1.83485E-02    R2=    8.05956E-03
A3=    3.95093E-05    N3=    42.611
C3=    1.34580E-03    Z3=    7.87285E-02
F=     22118          R4=    .81116
AC1=   1.13267E-06    A2=    2.35312E-05
L1=    1.52565E-04    L2=    5.12254E-05
Z1=    4.45238E-02    Z2=    3.76723E-02
D=     .75345         F1=    1114..
AL3=   2.59417E-05    L3=    1.01023E-04
R3=    1.34550E-02    G=     2.27556E-03

EFF=   .94125
R1= 1.834848444E-02
R2= 8.059554146E-03
D= 7.534468771E-01
PIF= 1.908316511E-01
PO= 1.169054381
PC= 3.633556064
PDL= 1.052713474
PT(TOTAL LOSS)= 6.24615558
EFF= 9.4125307F-01
SOURCE WEIGHT= 6.99=806549
HEAT SINK WEIGHT= 4.053000557E-01
TOTAL WEIGHT= 7.561509609
```

8. THE DATA MANAGEMENT PROGRAM

The normal use of the MAPPS involves interactive conversation between the MAPPS system and the user. The user begins by signing on to the computer operating system. The user requests that the MAPPS system be loaded and executed in the conventional program load and execute manner. A conversation then begins between the user and an executive routine through which the user instructs

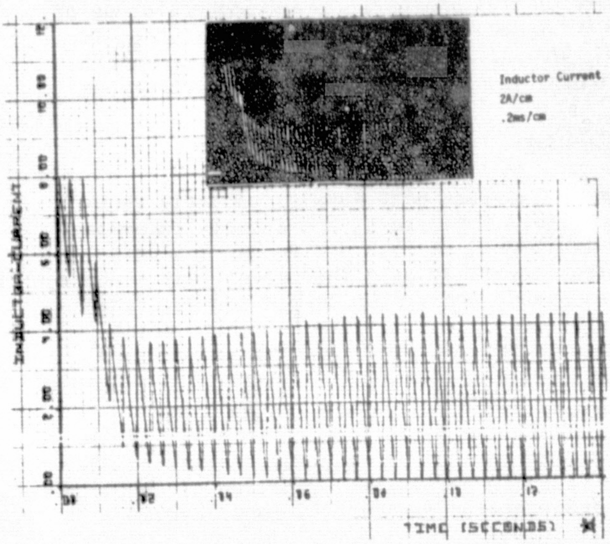

Figure 6. Boost Regulator Inductor Current Simulation

the system to attach certain external files and to perform specific analytic and/or data base manipulation functions. The MAPPS System will be sufficiently flexible to allow a sophisticated user to shortcut steps that are not needed because of the user's in-depth knowledge of the system. The new user will be presented with informative messages as processing goes forward and will also be able to retrieve some instructional text to clarify options at decision points. Upon completion of the input cycle, the MAPPS System will proceed to execute and satisfy the user's requests. The user will be able to invoke various subprograms which will aid in the equipment/system design, modeling analysis, and optimization. If intermediate results require a decision by the user, interactive conversation will again take place. During the course of an interactive session the user may display results, permanently or temporarily store results, or retrieve previously stored results from the data base.

The fusion of the various modules into a coordinated processing system is accomplished by developing appropriate control and communication routines. An Executive User Interface (EUI) routine affords the user with the means for selecting specific processes for execution. An Executive module carries out subprogram load requests and memory space allocation as well as input/output file linkage requests. Subprogram User Interface (SUI) routines provide the means for user interaction with the system. One SUI exists for each analytic subprogram integrated into the MAPPS System. Each SUI is capable of handling all of the communications relative to its respective subprogram. In addition to several analytic subprograms there will be a Data Base Manager subprogram under control of the MAPPS Executive. The Data Base Manager (DBM) will respond to, and perform all, Data Base access requests generated during any and all execution of MAPPS System analytic routines.

In the initial Phase II, a working prototype of the Data Management Program has been developed to facilitate expansion and enhancement as the MAPPS power processing subprogram capabilities increase.

9. CONCLUSIONS

To anyone working with nondissipatively regulated converters, inverters, and systems comprised of these equipment, certain design and analysis intricacies inevitably make themselves felt throughout the equipment and system design and development stage. Empirical and intuitive reliances often intercede with the designer's desire to be "more scientific" and his commitment of being "on schedule". Handicapped by a general lack of established design, modeling, analysis, and optimization tools, it has not been unusual for a power processing designer to face the perplexing situation of emerging from the intercession practically empty-handed.

Other than cost, the plight that most equipment and system designers find themselves in has to do with at least one of the following power processing characteristics: weight/efficiency, performance, and reliability. While power processing as a technology has reached the level of sophistication where the modeling, analysis, and optimization of these characteristics should have been well established, a survey of existing documents and literature has proven the contrary.

The primary content of this paper focuses the attention on the developed modeling and analysis subprograms for power processing components, equipment and systems. As is evident from the examples given here, the subprograms are entirely oriented toward the user. Four diversified subprograms including those of power circuit design optimization, control circuit design, regulator performance analysis, and power system analysis, are established. Their continued developments will undoubtedly lead to the following:

- Fully automated design for basic converter power and control circuits to meet performance specifications. Possible elimination of breadboard development stage.
- Fully automated switching-regulator performance analysis.
- Computer-aided power system configuration design and dynamic system simulation
- Significant cost saving, weight/efficiency optimization, and reliability improvement for power processing equipment or system development programs.

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