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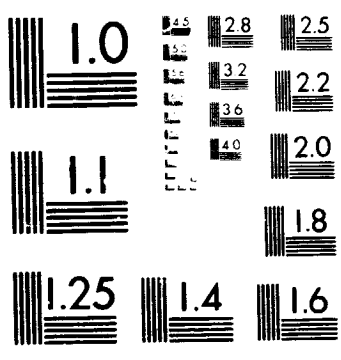

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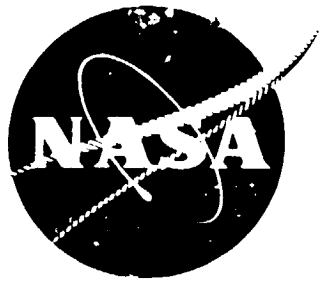

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MODELING, ANALYSIS AND DESIGN OF SWITCHING CONVERTERS

by

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Eiectrical Engineering Dept.
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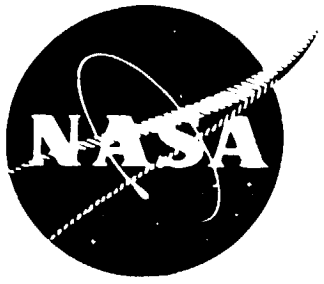

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ABSTRACT

The principal objective of this work on modelling and analysis of switching dc-to-dc converters and regulators is to obtain a linear model (either through state-space or linear circuit description), subject to appropriate restrictions, for the inherently nonlinear power stage in which the dc conversion is accomplished. A general unified approach to modelling and analysis of switching dc-to-dc converters is developed which is directly applicable to any dc-to-dc converter operating in either of two conduction modes (continuous or discontinuous inductor current), and which results in a final dynamic linear model either in terms of state-space equations or in terms of their corresponding linear circuit models. In particular, in Part I this analysis technique, called state-space averaging, is applied to the continuous conduction mode of converter operation, while in Part II appropriate extension of the method to the discontinuous conduction mode is made. In each case, the culmination of the modelling and analysis is achieved in the development of canonical circuit models which represent any such converter regardless of its detailed configuration.

The insights that emerge from the general state-space modelling approach (Parts I and II) lead in Parts III and IV to the design of new converter topologies through the study of generic properties of the cascade connection of basic buck and boost converters. This study paves the way in Part IV to the discovery of a new switching converter based upon capacitive rather than the usual inductive energy transfer. The new converter is shown to have substantial advantages over the conventional converters in its class in efficiency, performance, and also in size and weight.

Both the state-space averaged models and their corresponding circuit realizations provide the circuit designer with a powerful tool for analysis of existing converters as well as for synthesis of new converter topologies.

TABLE OF CONTENTS

INTRODUCTION

The ever increasing demand of society for new and more abundant sources of energy, as well as for means of better and more efficient conversion to a medium suitable for widespread use such as electrical energy, has provided a healthy environment for the recent growth of the new, interdisciplinary field of Power Electronics. Functions to be performed by electronic power processing systems include a wide range, from efficient conversion of dc source voltage from one voltage to another, to inversion of dc to single-phase or multiple-phase ac, and controlled conversion of ac to dc. The applications also cover a wide spectrum, from a power supply in a hand-held calculator, through a variety of spacecraft systems including solar array and battery power conditioning, to industrial process control and electric utility bulk power inversion.

However, it comes as no surprise that this new field has offered some unmatched challenges owing to its unique combination of the three major disciplines of electrical engineering: electronics, power, and control. Classical signal processing electronics, coupled with the advent of semiconductor devices capable of handling substantial amounts of power, is used to control the power (or electrical energy) flow from some raw source of electrical energy (such as solar cells, for example), to the user (load). But in distinction with signal-processing electronics, where the power efficiency is of minor concern, here, as in classical power systems, it becomes the major issue, owing to the relatively large amounts of power involved. Power

efficiency makes mandatory the use of control devices, such as transistors and SCR's (silicon controlled rectifiers) in a repetitive switching mode, thus further increasing the problems of modelling the dynamic behavior of power switching circuits because of their inherent nonlinear nature. In addition, in many instances, the power conversion or inversion function is coupled with a requirement for regulation, and stability problems naturally arise because the self-correcting feature is usually obtained by employing electronic feedback in a closed-loop system. It is in this context particularly that a fusion of viewpoints of the power, control, and electronics disciplines is most necessary and also potentially fruitful.

However, the bringing together of these disciplines in order to achieve the general understanding and consequent innovation in power processing electronics systems is not merely their accumulation, but rather requires a revised look at their specific interrelations from the component to the system level. For example, a signal-processing electronics engineer usually thinks in terms of active devices used in either linear or switching mode together with resistors and capacitors; he avoids inductors and transformers. On the other hand, a power-processing electronics engineer must think in terms of active devices used in the switching mode together with capacitors, inductors, and transformers; he must avoid resistors in the interest of maintaining high efficiency in the power path. This important distinction requires a different way of thinking about circuit function realization. From the system point of view, one has only to recognize, for example, a dc-to-dc switching regulator as a dc, wide-band, nonlinear

sampled-data control system (with the ever-present high-efficiency constraint), to appreciate the challenge of bringing together these various disciplines.

Hence, the area of modelling and analysis of power processing systems, owing to their inherent nonlinear nature, becomes an even more challenging task, particularly in view of the lack of adequate analysis tools at the disposal of the circuit designer working in this field. In connection with that, the choice of parameter values in already existing circuit topologies, as well as the design of new circuit topologies is likewise a very difficult one.

The major thrust and purpose of this work is to provide the circuit designer with analytical tools which are accurate enough for practical purposes, yet simple enough to apply to give him powerful tools for design-oriented analysis in one of the major areas of electronic power processing: switching dc-to-dc converters and/or regulators. In addition, this analysis through appropriate linear circuit models provides the necessary insight which may lead to innovative converter topologies, offering better and near optimum performance.

The structure of this work has been divided into two distinct yet firmly interconnected major divisions: general unified approach to modelling and analysis of switching dc-to-dc converters, presented in Parts I and II, and design of new converter topologies presented in Parts III and IV, which has been directly made possible by the insights gained from the analysis methods of Parts I and II. Chapter 1, which is placed outside and in front of these four parts, is

intended to familiarize the reader with the basic switching conversion concepts and at the same time to introduce both the analysis difficulties as well as to designate the possible areas of performance improvements in switching converter design.

The principal objective of the work on modelling and analysis of dc-to-dc converters and regulators (Parts I and II) is to obtain a linear model (either through state-space or linear circuit description), subject to appropraite restrictions, for the inherently nonlinear power stage in which the dc conversion is accomplished. Such converters operate in one of two modes: a two-state mode referred to as the "continuous conduction mode," in which inductor currents do not fall to zero (as modelled in Part I), and a three-state mode, "discontinuous conduction," in which an inductor current falls to zero (Part II).

The culmination of this work is a canonical circuit model for a dc-to-dc converter in the continuous conduction mode which properly represents both the line and duty ratio transfer functions and also, for the first time, correctly represents the converter input impedance. The principal advantage of the canonical model is that it represents any such converter regardless of its detailed configuration.

The corresponding canonical circuit model for a dc-to-dc converter in the discontinuous conduction mode is obtained in Part II, which not only confirms that the line and duty ratio transfer functions become first-order, in contrast to the second-order functions of the continuous conduction case, but also for the first time correctly represents the input impedance.

Both canonical models are made possible by a powerful technique called state-space averaging developed in both Parts I and II, which unifies and places in perspective what had previously been considered distinct analytic methods.

The insights gained by the state-space averaging approach of Part I and Part II leads in Part III to the study of the generic properties of a new class of buck-boost converters obtained by cascade connection of basic buck and boost converters.

Finally, this study culminates in Part IV in the discovery of a new switching converter based upon capacitive rather than the usual inductive energy transfer. The new converter is shown to have substantial advantages over conventional converters in efficiency, performance and also in size and weight.

CHAPTER 1

SWITCHING DC-TO-DC CONVERTERS AND REGULATORS

In this introductory chapter several common switching dc-to-dc converters are introduced and their physical operation briefly explained. The basic property, dc-to-dc voltage and current level conversion, is arrived at following some simplified arguments based on fundamental physical laws in order to familiarize the reader with some of the basic quantitative relationships.

Upon this initial exposure to the nature of the problems associated with the analysis of these essentially nonlinear circuits, the general, unified, and complete method of modelling and analysis of any switching dc-to-dc converters (even those yet to be invented) developed and presented in chapters to follow will be more easily grasped.

1.1 Physical operation and basic properties of switching converters

We begin with the three common switching converters (also called power stages because of their power handling capability) depicted in Fig. 1.1. While in Fig. 1.1a the topological structure of these converters independent of any particular switch realization is shown, in Fig. 1.1b a bipolar transistor, commutating diode realization of the single-pole double-throw switch S is used. It is also evident from Fig. 1.1b that transistors are used in their switching mode: either fully turned on (corresponding to the position

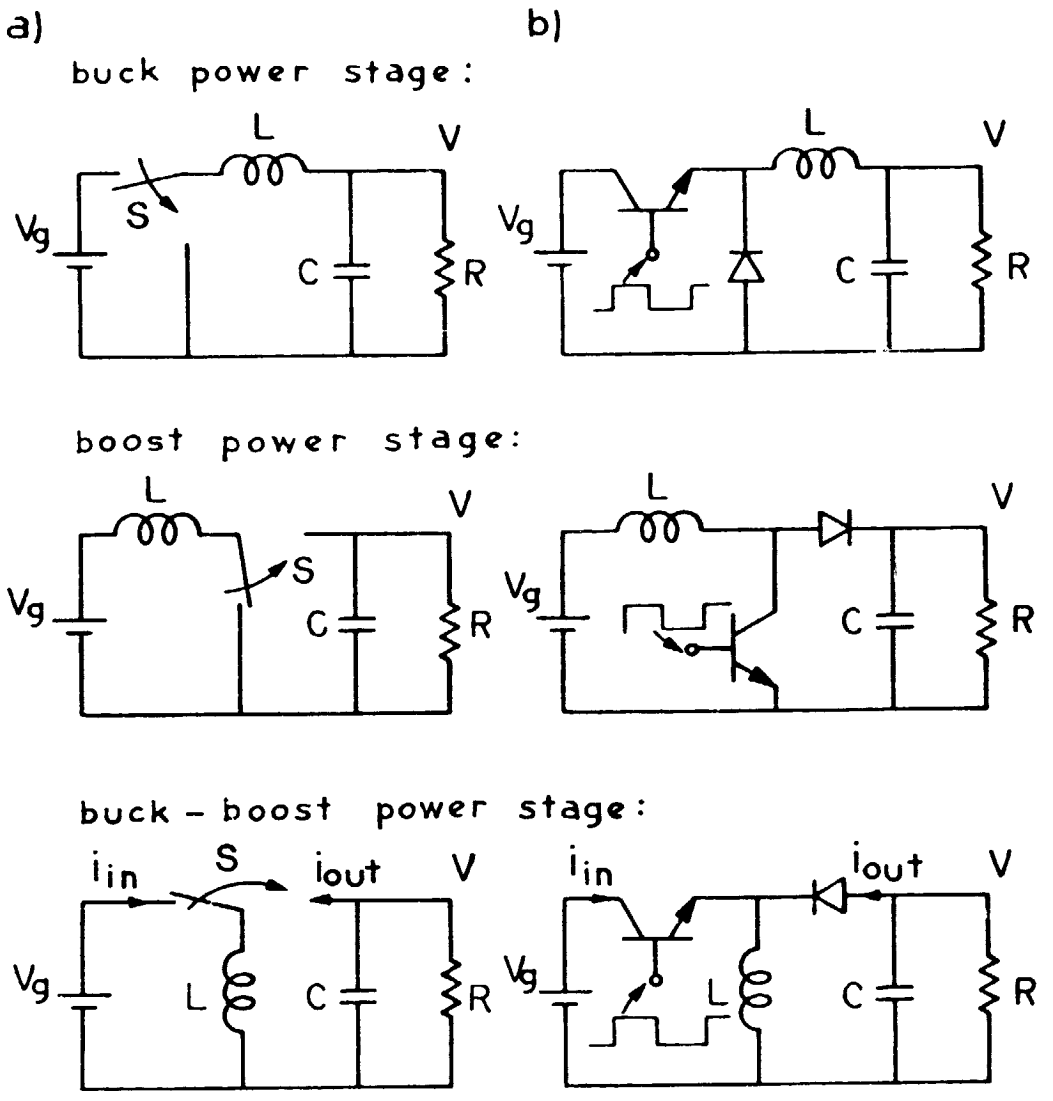


Fig. 1.1 Three common switching dc-to-dc converters: a) topological configuration independent of switch realization; b) bipolar transistor implementation of the switch S.

of switch S in Fig. 1.1a) or fully off (the other position of switch S). This is obtained by bringing a periodic switch drive signal as shown in Fig. 1.2 to the base of the transistor. The frequency of repetition of this signal is defined as the switching frequency $f_s = 1/T_s$, and for discussion purposes will be considered constant. The fraction of the complete period T_s for which the transistor is on is defined as the steady state duty ratio $D = T_N/T_s$. The diode in

each converter acts as a switch automatically synchronous with the transistor. That is, when the transistor is on, the diode is reverse biased and effectively off; as soon as the transistor becomes off, the diode is forced to conduct by the continuous inductor current, and stays on as long as there is a positive inductor current.

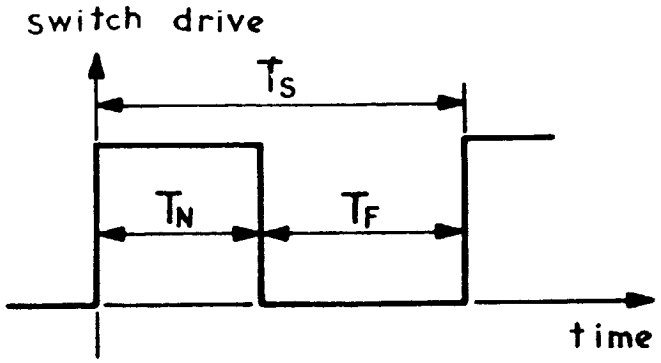


Fig. 1.2 Definition of the periodic switch drive.

Consider now more closely the simplest of these converters, the buck power stage (sometimes called the step-down or chopper converter because of its property of reducing the input dc voltage). With assumption of ideal transistor and diode switches, the buck power stage can be equivalently represented as in Fig. 1.3.

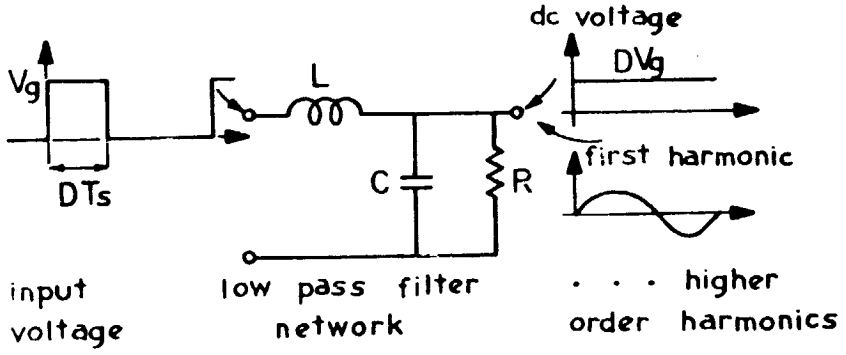


Fig. 1.3 Basic dc conversion function of buck power stage viewed through harmonic decomposition and principle of superposition.

Fourier harmonic decomposition of the periodic input voltage and the principle of superposition show that the output voltage consists of a dc voltage $V = DV_g$ and ac harmonics with fundamental at the switching frequency f_s. If the low-pass filter elements are chosen such that its corner frequency $f_c = 1/(2\pi\sqrt{LC})$ is much smaller than the switching frequency f_s ($f_c << f_s$), all harmonics are substantially attenuated leading to very small output voltage ripple. Hence, even though present, the output voltage ripple can be reduced to an arbitrarily small value by proper choice of filter elements.

A significant feature of the switching converter is that a degree of control over the output dc voltage has been introduced through its dependence on the duty ratio D. Therefore, simply by varying the switch drive duty ratio one is able to change the output dc voltage. Also, since by definition $0 \leq D \leq 1$, it is apparent that the buck power stage is capable only of reducing the dc input voltage level.

Another very important property of the converter is immediately apparent. For a properly designed filter, the ripple voltage is negligible, and the output current is dc current only $I_{out} = V/R$. However, input current flows only during the interval when the transistor is on, and hence $I_{in} = DI_{out}$. Therefore, the efficiency of the converter in this ideal case is 100% since

$$\frac{P_{out}}{P_{in}} = \frac{VI_{out}}{V_g I_{in}} = D\,\frac{1}{D} = 1$$

The key to this ideal 100% efficiency is in the fact that the control device, the transistor, is used in the switching mode, unlike its

use in a linear regulator as a linear dissipative element or variable resistance. However, in reality the voltage across a real transistor when it is turned on is not zero as for ideal switch S, but its saturation voltage V_{CEsat} is usually 0.3V-1V. Likewise, the diode has some forward voltage drop of the same order which also slightly degrades the efficiency of a real converter. Nevertheless these losses are negligible in comparison with losses present in a linear regulator.

1.2 Two operating modes and their dc relations in the steady-state regime

So far two important characteristics of switching converters have been established: a degree of control through duty ratio drive D, and high efficiency of operation. There are, however, some other features peculiar to these converters which, even though present, are not so clearly displayed in the buck power stage example. Let us therefore consider the buck-boost converter, in which these additional features are most visible.

For the two positions of the switch S in the buck-boost converter of Fig. 1.1, the two switched network configurations shown in Fig. 1.4 are obtained, from which it is clear that a topological structural change occurs within each period and the circuit configuration is changed periodically from that of Fig. 1.4a to that of Fig. 1.4b. Both switched networks in Fig. 1.4 are linear by themselves, but it is due to this periodic structural change that the converter itself is a nonlinear circuit. It is exactly here where the difficulty in modelling and analysis of these converters arises.

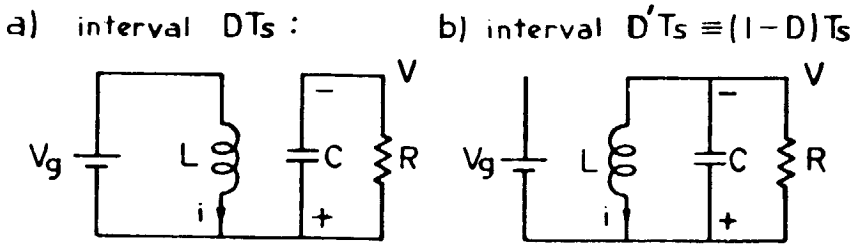


Fig. 1.4 Two switched networks for the buck-boost converter operating in the continuous conduction mode.

Another interesting observation about the role of the inductance can be made: it acts as an energy transferring device between input source voltage V_g and output load R, by accumulating the energy in the form of a magnetic field during the first interval T_sD and then releasing it to the load during the subsequent interval T_sD', thus charging the output capacitor negatively as shown in Fig. 1.4b. With assumption of LC filter values properly chosen for low (negligible) output voltage ripple, the inductor voltage and current waveforms in this steady state, so called "continuous conduction mode", are as shown in Fig. 1.5.

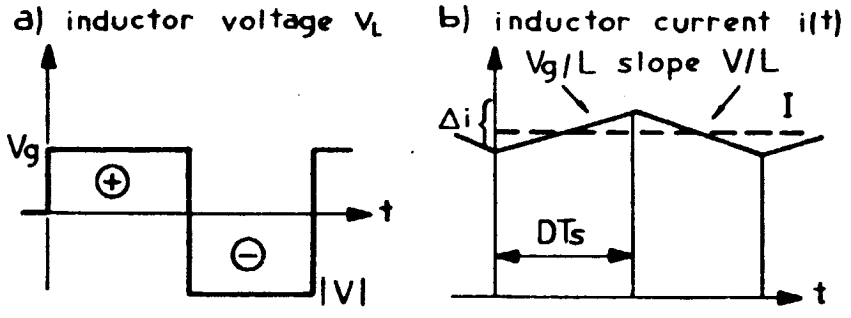


Fig. 1.5 Energy storage inductor steady-state waveforms in the continuous conduction mode.

The continuous conduction mode refers to operating conditions and converter parameter values for which the instantaneous inductor current does not fall to zero at any time during the switching cycle, as shown in Fig. 1.5b. This is directly connected with the existence of only two switched networks during each cycle, as was shown in Fig. 1.4.

Let us now find for this operating mode the static conditions, that is, the dc voltage and current level conversion relations in the steady state regime. Here "steady state regime" signifies the fact that the duty ratio D is held constant over a sequence of switching cycles, thus leading to the current and voltage periodicity requirements:

steady state
$$i(0) = i(T_s) \quad \text{for inductor current}$$
$$v(0) = v(T_s) \quad \text{for capacitor voltage}$$

Then, from Faraday's law

$$\int_0^T v_L(t)dt = L \int_{i(0)}^{i(T)} di = L[i(T_s) - i(0)] = 0 \qquad (1.1)$$

in steady state. Evaluation of the integral on left with help of Fig. 5a gives

$$V_g DT_s + V(1-D)T_s = 0$$

or

$$\frac{V}{V_g} = -\frac{D}{1-D} \qquad (1.2)$$

which is the ideal dc voltage gain for the buck-boost converter.

It is now obvious that the buck-boost power stage is capable of producing a dc output voltage which is either smaller (for $D < 0.5$) or larger (for $D > 0.5$) than the input voltage, and hence realizes

a general dc conversion function. Since none of the lossy elements has been accounted for, the dc current gain in this ideal 100% efficient case would be $I_{out}/I_{in} = D'/D$.

Consider now the case in which the energy stored in the inductor during the first interval $T_s D_1 \equiv T_s D$ is completely released to the output load before the switching cycle T_s has ended, causing the inductor current to become zero for the last portion of the period T_s. This could happen if the switching period has been sufficiently increased, or if the inductance has been substantially reduced and hence it has shortened the time interval necessary to release energy to the output. Even if neither change has occurred, but instead the load resistance R is increased sufficiently to cause lowering of the average inductor current I shown on Fig. 1.5b to the point where $i(0) = i(T_s) = 0$, the instantaneous inductor current becomes as shown in Fig. 1.6b. The converter is thus operating in the so-called "discontinuous conduction mode," in which the name clearly originates from the discontinuous inductor current waveform in Fig. 1.6b.

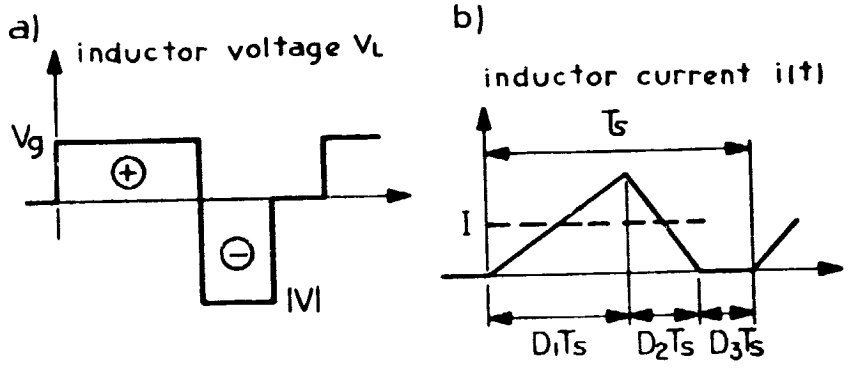


Fig. 1.6 Steady-state inductor waveforms in the discontinuous conduction mode.

The immediate consequence of operation in the discontinuous conduction mode is that there are three different switched network configurations inside each switching period T_s as shown in Fig. 1.7.

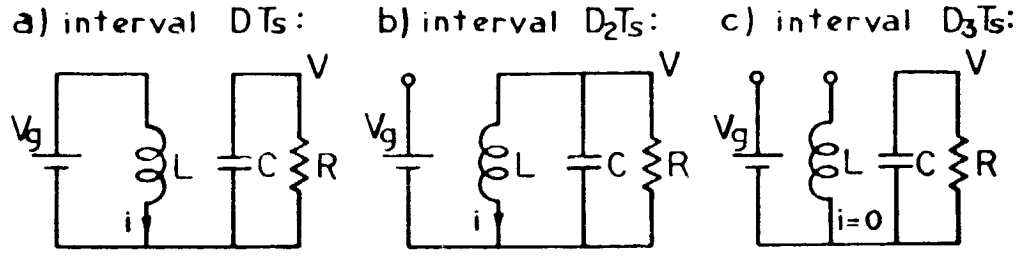


Fig. 1.7 Three switched networks for the buck-boost converter operating in the discontinuous conduction mode: a) transistor on, diode off, b) transistor off, diode on, c) transistor off, diode off.

At the end of the second interval T_sD_2, the energy stored on the inductor has been completely released to the load and inductor current vanishes. Hence, the inductor voltage becomes zero which causes the diode to become reverse biased and hence nonconducting for the last interval T_sD_3, for which interval the third switched network topology shown in Fig. 1.7c is formed. As for the continuous conduction mode topological structural changes take place within each period, but for the discontinuous conduction mode the changes are among three different switched network topologies as displayed in Fig. 1.7.

It is important to emphasize that the two properties described above for the buck-boost converter example -- inductive energy transfer principle and two modes of operation -- are not restricted to this particular example but are general in nature. They are applicable not only to the other two converters shown in Fig. 1.1 but also to any switching converter so far known.

Let us now, however, complete the comparison between the two modes of operation for the buck-boost converter example. The steady state dc voltage conversion ratio might be found as before by use of Faraday's law and Fig. 1.6a as:

$$V_g DT_s + VD_2T_s = 0$$

or

$$\frac{V}{V_g} = -\frac{D}{D_2} \tag{1.3}$$

However, the interval D_2T_s, which determines how deep in the discontinuous conduction mode the converter is operating, is yet to be determined. This can be accomplished by finding an alternative relation for the dc voltage ratio, based upon the 100% efficiency property of the ideal converter. From Fig. 1.6b, $I_{in} = DI = D^2V_gT_s/2L$ and so $P_{in} = V_gI_{in} = D^2V_g^2T_s/2L$; then, $P_{out} = V^2/R$ so from $P_{in} = P_{out}$

$$D^2 \frac{V_g^2}{2L} T_s = \frac{V^2}{R}$$

which leads to

$$\left|\frac{V}{V_g}\right| = \sqrt{\frac{TR}{2L}}\, D \tag{1.4}$$

or

where

$$\left|\frac{V}{V_g}\right| = \frac{D}{\sqrt{K}}$$

$$K = \frac{2L}{R} f_s$$

Comparison between (1.3) and (1.4) gives immediately

$$D_2 = \sqrt{K} \tag{1.5}$$

so that the dimensionless parameter K determines then the length of

the second interval D_2T_s. It is interesting to note that the second interval D_2 is determined solely by K so that, for a given converter the second interval is a constant affected only by the load resistance R. This is not true for the buck or the boost converter, in which the second interval is dependent not only upon K but also upon the duty ratio D.

For the buck-boost converter, comparison between (1.2) and (1.4) shows that in the continuous conduction mode the dc gain is a highly nonlinear function of duty ratio D only (1.2), while in the discontinuous conduction mode it is a linear function of duty ratio D but also dependent on the dimensionless parameter K (1.4).

The boundary between the two modes of operation is easily found from Fig. 1.6b as:

$$D_3 = 0 \Rightarrow D_2 = 1 - D \Rightarrow D' = \sqrt{K} \tag{1.6}$$

Furthermore, a criterion to determine in which of the two modes the converter is operating can be established in the form of an inequality relationship among circuit parameter values L,R switching frequency f_s, and duty ratio D of the switching drive as follows:

$$\begin{aligned} &\underline{\text{continuous conduction mode}} \\ &\qquad D' < \sqrt{K} \\ &\underline{\text{discontinuous conduction mode}} \\ &\qquad D' > \sqrt{K} \end{aligned} \tag{1.7}$$

where $K = 2L/RT_S$ is a dimensionless parameter.

For instance, when $K \geq 1$ the converter will <u>always</u> be operating in the continuous conduction mode regardless of the control--duty

ratio D, while for $K < 1$ it will operate in the discontinuous conduction mode for $D < 1 - \sqrt{K}$.

To illustrate this with a numerical example, let L = 1mH, f_s = 10kHz, and R = 10Ω. Then, K = 2 and the converter will always operate in the continuous conduction mode. However, if the load resistance is increased to R = 100Ω, K = 0.2 and the converter will operate in the discontinuous conduction mode for $D < 0.553$. This example also justifies why the continuous conduction mode is sometimes also called "heavy mode" (low resistance R and heavy loading) while the discontinuous conduction mode is referred to as "light mode" (higher resistance R and therefore light loading).

1.3 Switching ripple and pulsation of input and output currents

Now that the two distinct modes of operation of switching dc-to-dc converters have been clearly distinguished, the physical origin of their appearance understood and the quantitative measure describing the transition between two modes of conduction correlated with circuit physical parameters, we can proceed to expose some of the undesirable features inherent in the switching converters of Fig. 1.1 in both conduction modes.

Consider now both input and output currents (designated i_{in} and i_{out} in Fig. 1.1) for the buck-boost converter in the continuous conduction mode. Even though the converter is operating in the continuous conduction mode, owing to the switching action of the transistor and diode, both currents are as illustrated in Fig. 1.8.

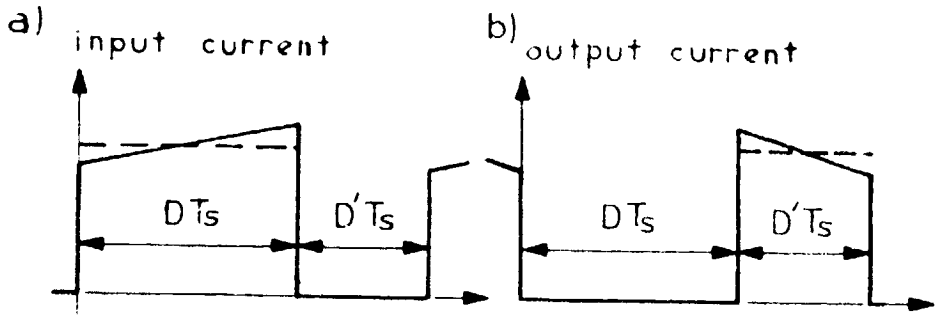


Fig. 1.8 Input and output current of the buck-boost converter operating in the continuous conduction mode.

It can easily be verified that the buck converter has the same pulsating input current as shown in Fig. 1.8a. This invariably requires that an input filter (usually a single-section low-pass L,C filter) be put in front of these two converters to smooth out the substantial current ripple component at the switching frequency drawn from the line supply. That way, electromagnetic interference (EMI) problems generated by the abrupt variation in energy flow (pulsating current) are reduced, and contamination of the environment by the undesired electromagnetic disturbances alleviated.

On the other hand, the boost converter of Fig. 1.1 has the same pulsating output current, as the buck-boost converter in Fig. 1.8b, which is primarily responsible for the much higher output voltage ripple of these two converters compared to the buck power stage with the same storage element values and operating conditions (switching frequency f_s, duty ratio D, and continuous conduction mode). The smaller voltage ripple in the buck power stage is a consequence of the nonpulsating output current (similar to that shown in Fig. 1.5a) with very small current ripple Δi_{out} which can easily be found as

$$\Delta i_{out} = \frac{V}{L} D'T \tag{1.8}$$

Consequently, the output voltage ripple Δv is obtained from

$$\Delta v(\text{peak-to-peak}) = \frac{\Delta i_{out}}{8 f_s C} = \frac{VD'}{8L\, C f_s^2} \tag{1.9}$$

and the relative output voltage ripple $\Delta v/V$ is:

$$\frac{\Delta v}{V} = \frac{\pi^2}{2} D' \left(\frac{f_c}{f_s}\right)^2 \tag{1.10}$$

where

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

Here f_c is the corner frequency of the low-pass filter formed by L and C. Since the ultimate requirement of the dc-to-dc converter is to provide dc level change and output dc voltage only, this poses a restriction on the choice of filter elements. Namely, from (1.10) output voltage ripple will be negligible if the following requirements are satisfied:

$$\begin{array}{ll} f_c \ll f_s & f_c = 1/2\pi\sqrt{LC} \\ \text{where} & \\ \omega_\alpha \ll f_s & \omega_\alpha = 1/2RC \end{array} \tag{1.11}$$

The second inequality condition in (1.11) comes from requirement of negligible output voltage change during the interval $T_s D$ (see Fig. 1.4a) when capacitance C discharges into load R.

As a numerical illustration for the typical parameter values, in continuous conduction mode, L = 6mH, C = 40μF, f_s = 20kHz,

$R = 60$, we obtain $f_c = 330Hz$, $\omega_\alpha = 21Hz$ and inequalitites (1.11) are well satisfied. Hence from (1.10) $\Delta v/V \sim (f_c/f_s)^2 \sim 10^{-4}$ or the output voltage ripple is of the order of 0.01% for the buck converter.

For the same element values but for the buck-boost converter, since the output current ripple is now from Fig. 1.8b, $\Delta i_{out} = I_{load} = V/R$, the output voltage ripple becomes load current dependent and is:

$$\Delta v = D \frac{I_{load}}{f_s C} \Rightarrow \frac{\Delta v}{V} = D \frac{1/RC}{f_s} \qquad (1.12)$$

or of the order of several percents for the given numerical example. A similar result is obtained for the boost converter.

Hence for the two converters with pulsating output current, almost two order of magnitudes higher voltage ripple is obtained. It could be reduced to an acceptable level by increase of capacitance C or by increase of the switching frequency f_s; in that case, however, the fundamental requirement (1.11) for low output voltage ripple would be even better satisfied than for the buck converter example.

It is now no surprise that both EMI and output voltage ripple would be further degraded in the discontinuous conduction mode, since then both input and output current become even more pulsating, as illustrated for the buck-boost converter in Fig. 1.9.

Suppose that the transition to the discontinuous conduction mode is made by significantly lowering the inductance from that used in the continuous conduction mode. Highly impulsive current in Fig. 1.9b would then cause an intolerable output voltage ripple, unless either

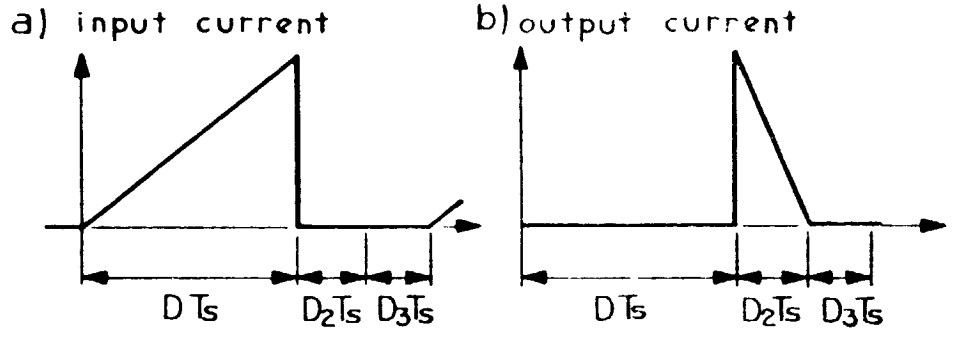


Fig. 1.9 Input and output current of the buck-boost converter operating in the discontinuous conduction mode.

the output capacitance C or switching frequency is increased, or both. In any case this has the consequence that the fundamental "small-ripple" restrictions for the "natural frequencies," $f_c \ll f_s$ and $\omega_\alpha \ll f_s$, would be even better satisfied. As an example, for the typical set of values in the discontinuous conduction mode L = 60μH, C = 400μF, f_s = 100kHz, R = 60Ω we get $f_c \simeq 1.02$kHz and $\omega_\alpha \simeq 21$Hz, thus satisfying inequalities (1.11) to a high degree. In essence, one recognizes that the burden of filtering out the switching ripple has been shifted from an equal share among inductance and capacitance in the continuous conduction mode completely to the capacitance in the discontinuous conduction mode. The inductance has retained only its energy transferring property but has lost its filtering property.

We therefore emphasize at this point the importance of the simple inequality requirements (1.11) placed as restrictions on the choice of parameter values in order to reduce the switching ripple inherent in all these converters to an acceptable level. When these relationships are properly recognized and incorporated in the model-

ling procedure a tremendous simplification of the analysis is obtained, and yet the derived results are accurate enough for all practical purposes. They are also the underlying basis of the general unified approach to modelling and analysis of switching converters which will be presented in Part I and Part II.

Besides having its importance and implication on the theoretical modelling procedure devised later, the relation (1.11) in conjunction with, for example, (1.10) exposes yet another interesting feature of switching dc-to-dc converters -- reduction of size and weight. Simple increase of switching frequency f_s would allow proportional increase of corner frequency f_c while still retaining the same switching ripple. Hence, the inductance and capacitance could be chosen smaller in value and size. However, this would not be achieved without a cost; increase in switching frequency would degrade the efficiency of the converter owing to increase in "switching losses," which become pronounced when the switching transistor rise and fall times become a substantial part of the switching period. The efficiency of conversion and quality of the switching transistor would pose the upper bound on the switching frequency.

1.4 Dynamic response of a switching converter; switching regulators

So far we have demonstrated only the steady state or static characteristics of switching converters. They would, of course, be sufficient to characterize the converter if it were used in an open loop fashion, namely, if the converter were used alone for voltage

level conversion by setting the transistor steady state duty ratio externally at some predetermined value. However, quite often the primary source of energy is unregulated and could have a wide range of voltage variation; on the other hand, a typical requirement is that the voltage (or sometimes current) supplied at the output to a user (some other electronic or electrical equipment) be maintained constant over a wide range of loading conditions. This is naturally achieved by the application of negative feedback in a closed-loop configuration, such as that shown in Fig. 1.10 depicting a typical switching regulator.

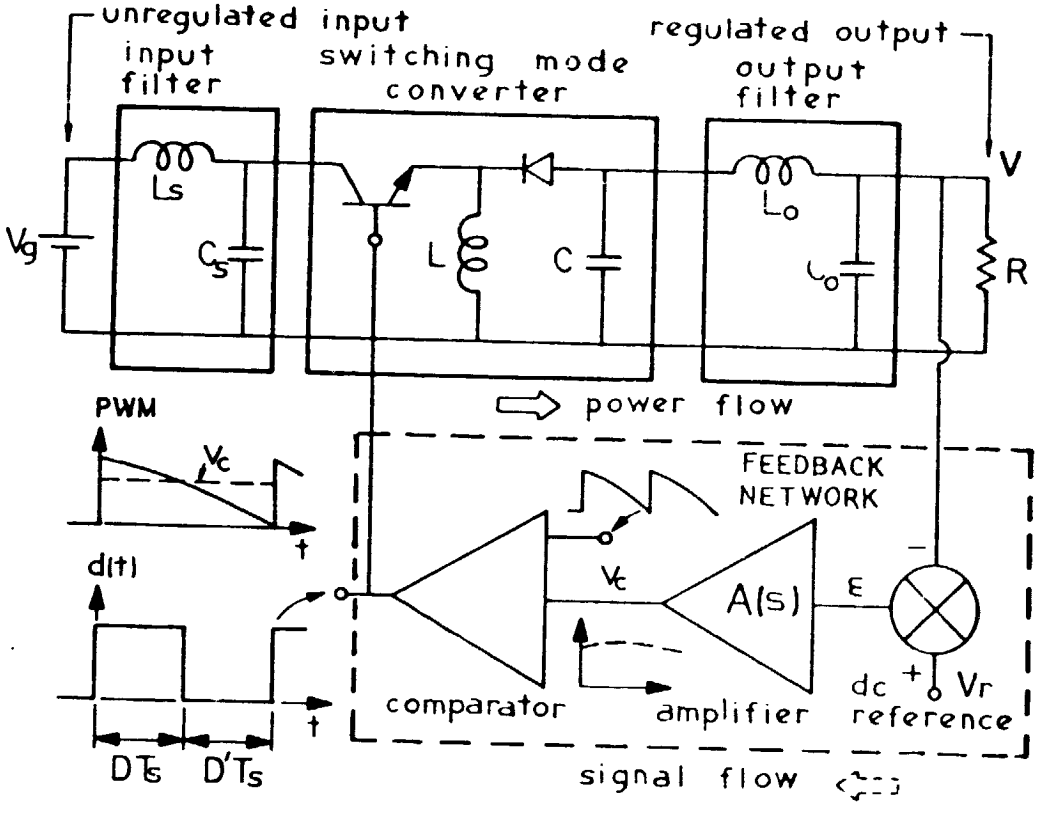


Fig. 1.10 Switching regulator: closed-loop implementation of the switching dc-to-dc converter.

For concreteness, the switching mode converter is represented by a buck-boost power stage, and the input and possible additional output filter are incorporated to smooth out the pulsating input and output currents as discussed before. Also a particular type of pulse width modulator (PWM) is used in which the on-off signal to the switch is produced by comparison of a sawtooth clocked waveform with the feedback signal as illustrated in Fig. 1.10 and sometimes referred to as a single-edge clocked pulse-width modulator.

As seen from Fig. 1.10 the error ε between the regulator output v and reference v_r is amplified (and possibly compensated) to produce an analog control signal v_c which further changes the duty ratio of the digital on-off signal d(t) as necessary to maintain a constant output voltage regardless of any source and load variations. However, as in all feedback systems, careful investigation of the closed loop is required to determine <u>stability</u> and <u>dynamic response</u>. For small-signal analysis, the problem of loop gain determination can be broken down into two parts: first, find how small-signal variations $\hat{v}_g$ and $\hat{d}$ superimposed upon the steady state, or dc, inputs V_g and D to the converter alone determine a small-signal converter output $\hat{v}$ superimposed on its steady state value V; and second, determine how this perturbation $\hat{v}$ is propagated through the feedback network to form a self-correcting modulation drive $\hat{d}$. The first problem of establishing the dynamic response of the power processing part, the

switching mode converter itself, is a very challenging problem owing to inherently nonlinear behavior of the converter, and will be thoroughly dealt with in remaining chapters. The second problem of modelling the dynamic behavior of the signal processing part, containing the modulator stage, will also be touched upon later, and hence the small-signal linear model of the complete closed loop switching regulator obtained.

Finally let us make the following simplifying observation. Even though a switching converter is nonlinear, and hence a sinusoidal test signal (such as $\hat{v}_g$) would produce a number of harmonics, all higher order harmonics may be neglected since the nonlinearity is followed by a very effective low-pass filter which attenuates them substantially with respect to the fundamental. This is the so-called describing function (DF) approximation, which can also be used experimentally to determine this linearized frequency response by observation of the output disturbance at the same frequency as the injected test sinusoidal signal.

1.5 Generalized switching dc-to-dc converter

It is now not hard on the basis of the previous discussion to visualize a general switching dc-to-dc converter, as shown in Fig. 1.11, where elements are purposely shown not interconnected in order to emphasize relative freedom of the choice of topology.

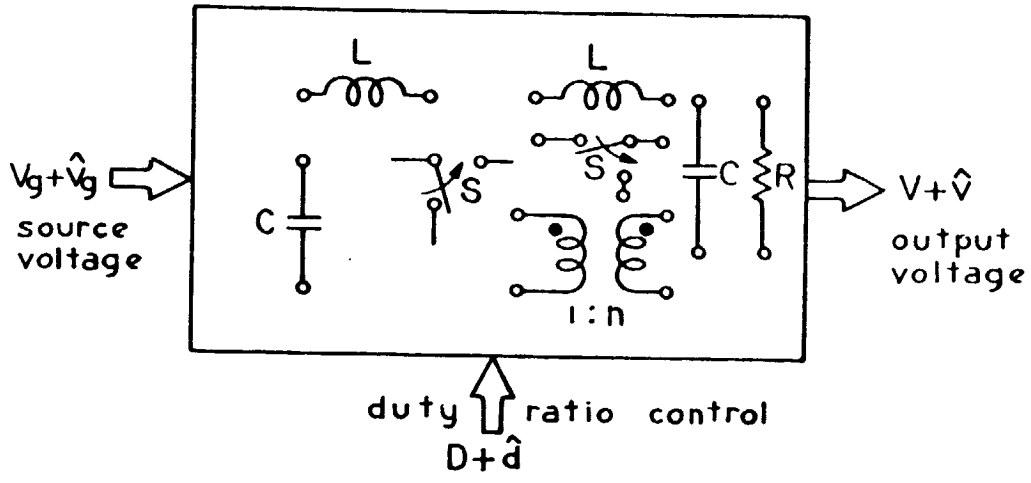


Fig. 1.11 Generalized switching dc-to-dc converter.

A generalized switching converter could consist of a number of energy storage elements (not necessarily a single inductor and capacitor as in the converters of Fig. 1.1), transformers and synchronous switches (again not restricted to the single switch as in Fig. 1.1) which are arranged in a topology such that the periodic opening and closing of the switches would guide the input power through the switching network in such a way that dc level conversion is obtained at the output.

There are, however, two general restrictions which have to be placed on the choice of interconnection of elements and their values:

1. Topology of the converter is not quite random, but the storage elements (inductors and capacitors) have to be arranged in such a way as to form effectively a low-pass filter if the prime dc input power is to be allowed to propagate to the converter output.

2. If the switching ripple caused by periodic action of the switches is to be negligible, the natural filter frequencies f_c and ω_α must be significantly smaller than the switching frequency f_s.

As seen from Fig. 1.11 the two independent inputs for the steady state (dc) static operation of the converter are line dc voltage V_g and steady state duty ratio D, while for the dynamic (ac) response, they are line voltage variation $\hat{v}_g$ and duty ratio modulation $\hat{d}$.

This generalized converter also has two modes of operation as previously illustrated on the buck-boost example. In the continuous conduction mode the topology of the converter is periodically changed between <u>two</u> switched networks (analogous to that in Fig. 1.4) while in the discontinuous conduction mode <u>three</u> switched network structures are clearly distinguished (compare with Fig. 1.7).

Note,however,that this generalized switching converter can have multistructural change (more than two switched networks) even in the continuous conduction mode (see Appendix D,for example). Likewise, the discontinuous conduction mode is not restricted to just three structural changes, though that is the minimum necessary to exhibit such behavior. Nevertheless, we will in Part I analyse the continuous conduction mode with only two structural changes, and in Part II the discontinuous conduction mode with only three structural changes because all the essential features of the two modelling methods are present in these

cases. The extension to the multistructural change is quite simple as demonstrated in Appendix D for the converters with three or four structural changes (also referred to as "three-state" and "four-state" converters, respectively) operating in the continuous conduction mode, and in Chapter 6 (Section 6.2) for the discontinuous conduction mode with more than three structural changes per switching period.

1.6 Review

It is for the generalized switching converter with the features described in Section 1.5 for which a general, unified method of modelling and analysis in both conduction modes will be developed. In particular, in Part I this general modelling technique is developed in detail for the continuous conduction mode of converter operation. In Part II, these techniques are extended with suitable modifications to include modelling of the converters operating in the discontinuous conduction mode. In both cases, a novel general and unified state space averaging technique is used to arrive at the general equations describing both static and dynamic properties of any switching dc-to-dc converter (pictorially represented in Fig. 1.11). Besides enabling some general results not previously attainable, the method lends itself easily to extraction of very useful circuit model realizations for any particular converter. Commonly used converters, shown in Fig. 1.1, are repeatedly used to demonstrate various models.

The ultimate goal and objective, however, of the modelling

procedure was not only to provide the tool for both static and dynamic analysis of existing converters, but through the circuit models and general conclusions to give additional insight and incentive to the circuit designer to devise new, better and possibly optimum converters.

In fact, it will be shown in Parts III and IV that this goal has been achieved. Indeed, Part III is a result of the search for such converter topologies which would confirm the general predictions made by the canonical circuit model of Part I, since the known existing structures failed to exhibit this generality. This has led naturally, first, to the idea of interconnecting existing converter structures into useful topologies, and cascade connection of switching converters as described in Part III turned out to be a very powerful one, from both theoretical and practical points of view. On the side of theory, it has finally confirmed the general modelling results of Part I. In addition, it has suggested a renewed look at the three "basic" converters of Fig. 1.1, through recognition that the buck-boost power stage may be considered as a buck converter cascaded with a boost converter, and thus leaving only the first two converters of Fig. 1.1 to be considered truly basic. This crucial observation paved the way for the discovery of a new switching converter which employs a novel and optimum circuit topology, and which is shown in Part IV to outperform any switching converter in its class.

Finally, after the foundations for modelling and analysis are firmly laid down in Parts I and II, and then used subsequently in

Parts III and IV to show in a rather natural and logical order how some new converter topologies could be devised, the thesis concludes with a number of research areas wide open for future investigation: discontinuous conduction mode in new converters, possible new modes of operation, and various technological implementations of synchronous switches are just a few examples.

GENERAL UNIFIED APPROACH TO MODELLING SWITCHING CONVERTERS

PART I

Continuous Conduction Mode

CHAPTER 2

REVIEW OF THE NEW STATE-SPACE MODELLING TECHNIQUE

The purpose of this chapter is to present a short, concise review of the most important interrelationships among various building blocks in the complete structure of the new modelling technique. Through this exposition of the various interconnections and procedural steps summarized in the Flowchart of Fig. 2.1 a twofold purpose will be achieved. First, the details of the modelling procedures which are presented in the remaining chapters of this Part I will be easier to grasp once it is understood how and where they fit into the complete modelling picture. Second, after the details of modelling are thoroughly explained in Chapters 3, 4 and 5, illustrated on numerous examples and fully comprehended, it will serve as a quick and easy reference guide and reminder containing all the essential information about the modelling in the continuous conduction mode.

However, because of its overview feature, this chapter will be relatively narrower in scope than, for example, Chapters 3 and 4 where the detailed development of the new modelling technique is given and the results discussed in depth.

2.1 Brief review of existing modelling techniques

In modelling of switching converters in general, and power stages in particular, two main approaches - one based on state-space modelling and the other using an averaging technique - have been developed extensively, but there has been little correlation between them. The first approach remains strictly in the domain of equation manipulations, and hence relies heavily on numerical methods and computerized implementations. Its primary advantage is in the unified description of all power stages regardless of the type (buck, boost, buck-boost or any other variation) through utilization of the exact state-space equations of the two switched models. On the other hand, the approach using an averaging technique is based on equivalent circuit manipulations, resulting in a single equivalent linear circuit model of the power stage. This has the distinct advantage of providing the circuit designer with physical insight into the behavior of the original switched circuit, and of allowing the powerful tools of linear circuit analysis and synthesis to be used to the fullest extent in design of regulators incorporating switching converters.

2.2 Proposed new state-space averaging approach

The method proposed in this work bridges the gap earlier considered to exist between the state-space technique and the averaging technique of modelling power stages by introduction of state-space averaged modelling. At the same time it offers the

advantages of both existing methods--the general unified treatment of the state-space approach, as well as an equivalent linear circuit model as its final result. Furthermore, it makes certain generalizations possible, which otherwise could not be achieved.

The proposed state-space averaging method, outlined in the Flowchart of Fig. 2.1, allows a unified treatment of a large variety of power stages currently used, since the averaging step in the state-space domain is very simple and clearly defined (compare blocks 1a and 2a). It merely consists of averaging the two exact state-space descriptions of the switched models over a single cycle T_s, where $f_s = 1/T_s$ is the switching frequency (block 2a). Hence there is no need for special "know-how" in massaging the two switched circuit models into topologically equivalent forms in order to apply circuit-oriented procedure directly, as required in [1] (block 1c). Nevertheless, through a hybrid modelling technique (block 2c), the circuit structure of the averaged circuit model (block 2b) can be readily recognized from the averaged state-space model (block 2a). Hence all the benefits of the previous averaging technique are retained. Even though this outlined process might be preferred, one can proceed from blocks 2a and 2b in two parallel but completely equivalent directions: one following path a strictly in terms of state-space equations, and the other along path b in terms of circuit models. In either case, a perturbation and linearization process required to include the duty ratio modulation effect proceeds in a very straightforward and formal manner, thus emphasizing the corner-stone character of blocks 2a and 2b. At this stage (block 2a or 2b) the steady state (dc) and line to

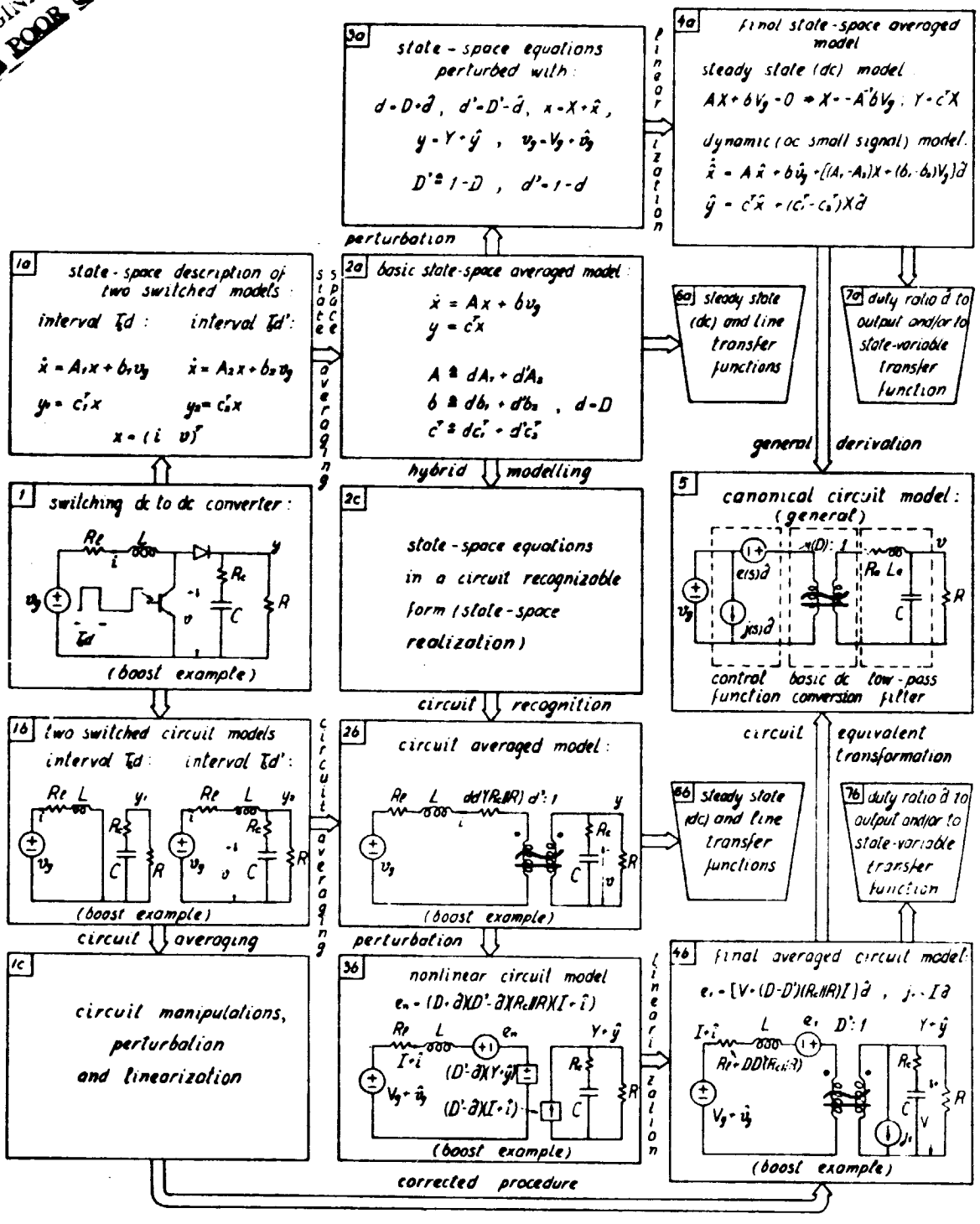


Fig. 2.1 Flowchart of averaging approaches in modelling switching dc-to-dc converters, leading to the canonical circuit model (block 5). Path a: general state-space modelling; Path b: circuit transformation method.

output transfer functions are already available, as indicated by blocks 6a and 6b respectively, while the duty ratio to output transfer function is available at the final-state model (4a or 4b) as indicated by blocks 7a and 7b. The two final state models 4a and 4b then give the complete description of the switching converter by inclusion of both independent controls, the line voltage variation and the duty ratio modulation.

Even though the circuit transformation path b might be preferred from the practical design standpoint, the state-space averaging path a is invaluable in reaching some general conclusions about the small-signal low-frequency models of any dc-to-dc switching converter (even those yet to be invented). Whereas, for path b, one has to be presented with the particular circuit in order to proceed with modelling, for path a the final state-space averaged equations (block 4a) give the complete model description through general matrices A_1, A_2 and vectors b_1, b_2, c_1^T, and c_2^T of the two starting switched models (block 1a). This is also why along path b in the Flowchart a particular example of a boost power stage with parasitic effects was chosen, while along path a general equations have been retained. Specifically, for the boost power stage $b_1 = b_2 = b$. This example will be later pursued in detail along both paths.

In addition, the state-space averaging approach offers a clear insight into the quantitative nature of the basic averaging approximation, which becomes better the further the effective low-pass filter corner frequency f_c is below the switching frequency f_s,

that is, $f_c/f_s << 1$. This is, however, shown to be equivalent to the requirement for small output voltage ripple, and hence does not pose any serious restriction or limitation on modelling of practical dc-to-dc converters.

Finally, the state-space averaging approach serves as a basis for derivation of a useful general circuit model that describes the input-output and control properties of any dc-to-dc converter.

2.3 New canonical circuit model

The culmination of any of these derivations along either path a or path b in the Flowchart of Fig. 2.1 is an equivalent circuit (block 5), valid for small-signal low-frequency variations superimposed upon a dc operating point, that represents the two transfer functions of interest for a switching converter. These are the line voltage to output and duty ratio to output transfer functions.

The equivalent circuit is a canonical model that contains the essential properties of <u>any</u> dc-to-dc switching converter, regardless of the detailed configuration. As seen in block 5 for the general case, the model includes an ideal transformer that describes the basic dc-to-dc transformation ratio from line to output; a low-pass filter whose element values depend upon the dc duty ratio; and a voltage and a current generator proportional to the duty ratio modulation input.

The canonical model in block 5 of the Flowchart can be obtained following either path a or path b, namely from block 4a or 4b, as

will be shown later. However, following the general description of the final averaged model in block 4a, certain generalizations about the canonical model are made possible, which are otherwise not achievable. Namely, even though for all currently known switching dc-to-dc converters (such as the buck, boost, buck-boost, Venable [3], Weinberg [4] and a number of others) the frequency dependence appears only in the duty-ratio dependent voltage generator but not in the current generator, and then only as a first-order (single-zero) polynomial in complex frequency s; however, neither circumstance will necessarily occur in some converter yet to be conceived. In general, switching action introduces both zeros and poles into the duty ratio to output transfer function, in addition to the zeros and poles of the effective filter network which essentially constitute the line voltage to output transfer function. Moreover, in general, both duty-ratio dependent generators, voltage and current, are frequency dependent (additional zeros and poles). That in the particular cases of the boost or buck-boost converters this dependence reduces to a first order polynomial results from the fact that the order of the system which is involved in the switching action is only two. Hence from the general result, the order of the polynomial is at most one, though it could reduce to a pure constant as in the buck or the Venable converter [3].

The significance of the new circuit model is that any switching dc-to-dc converter can be reduced to this canonical fixed topology form, at least as far as its input-output and control properties are concerned, and hence it is valuable for comparison of

various performance characteristics of different dc-to-dc converters. For example, the effective filter networks could be compared as to their effectiveness throughout the range of dc duty cycle D (in general, the effective filter elements depend on duty ratio D), and the configuration chosen which optimizes the size and weight. Also, comparison of the frequency dependence of the two duty-ratio dependent generators provides insight into the question of stability once a regulator feedback loop is closed.

2.4 Extension to complete regulator treatment

Finally, all the results obtained in modelling the converter or, more accurately, the network which effectively takes part in switching action, can easily be incorporated into more complicated systems containing dc-to-dc converters such as the switching regulator in Fig. 1.10. For example, by modelling the modulator stage along the same lines, one can obtain a linear circuit model of a closed-loop switching regulator. Standard linear feedback theory can then be used for both analysis and synthesis, stability considerations, and proper design of feedback compensating networks for multiple-loop as well as single-loop regulator configurations.

In summary, the review in this chapter has shown that the new general state-space averaging method is directly applicable to any switching dc-to-dc converter, even those whose topologies have not yet been conceived, namely to the generalized switching converter of Fig. 1.11. By simply following path a in the Flowchart of Fig. 2.1 both static (dc) and dynamic (ac) characteristics of the converter

are easily obtained. The only assumption made is that the converter operates in the continuous conduction mode, hence there exist only two switched circuit models (or their equivalent linear state-space description through triples (A_1, b_1, c_1^T) and (A_2, b_2, c_2^T) as shown in block 1a of the Flowchart in Fig. 2.1).

In addition, for any particular converter, the circuit averaged model results from following path b in the Flowchart. Finally, as a culmination of both approaches, a new canonical circuit model exhibiting fixed topology is obtained (block 5 in the Flowchart) which makes certain general conclusions possible.

After being so general in this chapter, we proceed with the specific derivations and illustrative examples in Chapters 3 and 4.

CHAPTER 3

STATE-SPACE AVERAGING, HYBRID MODELLING AND CIRCUIT AVERAGING

Several paths in the Flowchart of Fig. 2.1 are explored in detail in this chapter and are illustrated by appropriate examples. Since the justification of the basic state-space averaging step (going from block 1a to 2a in the Flowchart of Fig. 2.1) is lengthy and involved, the corresponding derivations are shown separately in Appendices A, B and C. This way they will not hide or interfere with the simple sequence of steps explained in this chapter, which are to be followed in order to arrive at the final static and dynamic model of the converter.

3.1 State-space averaging

In this section the state-space averaging method is developed first in general for any dc-to-dc switching converter, and then demonstrated in detail for the particular case of the boost power stage in which parasitic effects (esr of the capacitor and series resistance of the inductor) are included. General equations for both steady-state (dc) and dynamic performance (ac) are obtained, from which important transfer functions are derived and also applied to the special case of the boost power stage.

Basic state-space averaged model

The basic dc-to-dc level conversion function of switching converters is achieved by repetitive switching between two linear

networks consisting of ideally lossless storage elements, inductances and capacitances. In practice, this function may be obtained by use of transistors and diodes which operate as synchronous switches. On the assumption that the circuit operates in the continuous conduction mode in which the instantaneous inductor current does not fall to zero at any point in the cycle, there are only two different "states" of the circuit. Each state, however, can be represented by a linear circuit model (as shown in block 1b of Fig. 2.1) or by a corresponding set of state-space equations (block 1a). Even though any set of linearly independent variables can be chosen as the state variables, it is customary and convenient in electrical networks to adopt the inductor currents and capacitor voltages. The total number of storage elements thus determines the order of the system. Let us denote such a choice of a vector of state-variables by x.

It then follows that any switching dc-to-dc converter operating in the continuous conduction mode can be described by the state-space equations for the two switched models:

$$\begin{array}{ll} \text{(i) interval } T_s d: & \text{(ii) interval } T_s d': \\ \dot{x} = A_1 x + b_1 v_g & \dot{x} = A_2 x + b_2 v_g \\ y_1 = c_1^T x & y_2 = c_2^T x \end{array} \qquad (3.1)$$

where $T_s d$ denotes the interval when the switch is in the on state and $T_s(1-d) \equiv T_s d'$ is the interval for which it is in the off state, as shown in Fig. 1.2. The static equations $y_1 = c_1^T x$ and $y_2 = c_2^T x$ are necessary in order to account for the case when the output quantity does not coincide with any of the state variables, but is

rather a certain linear combination of the state variables.

Our objective now is to replace the state-space description of the two linear circuits emanating from the two successive phases of the switching cycle T_s by a single state-space description which represents approximately the behavior of the circuit across the whole period T_s. We therefore propose the following simple averaging step: take the average of both dynamic and static equations for the two switched intervals (3.1), by summing the equations for interval $T_s d$ multiplied by d and the equations for interval $T_s d'$ multiplied by d'. The following <u>linear continuous system</u> results;

$$\dot{x} = d(A_1 x + b_1 v_g) + d'(A_2 x + b_2 v_g)$$

$$y = dy_1 + d'y_2 = (dc_1^T + d'c_2^T)x \qquad (3.2)$$

After rearranging (3.2) into the standard linear continuous system state-space description, we obtain the basic averaged state-space description (over a single period T_s):

$$\dot{x} = (dA_1 + d'A_2)x + (db_1 + d'b_2)v_g$$

$$y = (dc_1^T + d'c_2^T)x \qquad (3.3)$$

This model is the basic averaged model which is the starting model for all other derivations (both state-space and circuit oriented).

Note that in the above equations the duty ratio d is considered constant; it is not a time dependent variable (yet), and particularly not a switched discontinuous variable which changes between 0 and 1 as

in [1] and [2], but is merely a fixed number for each cycle. This is evident from the model derivation in Appendix B. In particular, when d = 1 (switch constantly on) the averaged model (3.3) reduces to a switched model (3.1i), and when d = 0 (switch off) it reduces to switched model (3.1ii).

In essence, comparison between (3.3) and (3.1) shows that the system matrix of the averaged model is obtained by taking the average of two switched model matrices A_1 and A_2, its control is the average of two control vectors b_1 and b_2, and its output is the average of two outputs y_1 and y_2 over a period T_s.

The justification and the nature of the approximation in substitution for the two switched models of (3.1) by state-space averaged model (3.3) is indicated in the Appendices. It has already been shown in Chapter 1 that the requirement of low output switching ripple places the natural frequencies $\omega_\alpha = 1/2RC$ and $f_c = 1/2\pi\sqrt{LC}$ significantly lower than the switching frequency $f_s = 1/T_s$ (see for example (1.11)). These two restrictions on the choice of elements, namely $\omega_\alpha/f_s << 1$ and $f_c/f_s << 1$ are shown in Appendix A to lead to a very accurate approximation of the fundamental matrix e^{At} by its first-order linear term, or $e^{At} \sim I + At$. This linear approximation of the fundamental matrix is shown in Appendix B to lead directly to the state-space averaging step, namely replacement of the two linear continuous models (3.1) by a single continuous model of (3.3). In addition, in Appendix C it is shown that in the steady state regime, the exact dc conditions could be found which under the same linear approximation of fundamental matrices reduce to the dc conditions

obtained from basic averaged state-space model (3.3).

The model represented by (3.3) is an averaged model over a single period T_s. If we now assume that the duty ratio d is constant from cycle to cycle, namely, d = D (steady state dc duty ratio), we get:

$$\begin{aligned} \dot{x} &= Ax + bv_g \\ y &= c^T x \end{aligned} \tag{3.4}$$

where

$$\begin{aligned} A &= DA_1 + D'A_2 \\ b &= Db_1 + D'b_2 \\ c^T &= Dc_1^T + D'c_2^T \end{aligned} \tag{3.5}$$

Since (3.4) is a linear system, superposition holds and it can be perturbed by introduction of line voltage variations $\hat{v}_g$ as $v_g = V_g + \hat{v}_g$, where V_g is the dc line input voltage, causing a corresponding perturbation in the state vector $x = X + \hat{x}$, where again X is the dc value of the state vector and $\hat{x}$ the superimposed ac perturbation. Similarly, $y = Y + \hat{y}$, and

$$\begin{aligned} \dot{\hat{x}} &= AX + bV_g + A\hat{x} + b\hat{v}_g \\ Y + \hat{y} &= c^T X + c^T\hat{x} \end{aligned} \tag{3.6}$$

Separation of the steady-state (dc) part from the dynamic (ac) part then results in the steady state (dc) model

$$AX + bV_g = 0;\ Y = c^T X \quad Y = -c^T A^{-1} bV_g \tag{3.7}$$

and the dynamic (ac) model

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + b\hat{v}_g \\ \hat{y} &= c^T\hat{x} \end{aligned} \tag{3.8}$$

It is interesting to note that in (3.7) the steady state (dc) vector X in general depends only on the dc duty ratio D and resistances in the original model, but not on the storage element values (L's and C's). This is so because X is the solution of the linear system of equations

$$AX + bV_g = 0 \tag{3.9}$$

in which L's and C's are proportionality constants. This is in complete agreement with the first-order approximation of the exact dc conditions shown in Appendix C, which coincides with expression (3.7).

From the dynamic (ac) model, the line voltage to state-vector transfer functions can be easily derived as:

$$\frac{\hat{x}(s)}{\hat{v}_g(s)} = (sI-A)^{-1}b \tag{3.10}$$

$$\frac{\hat{y}(s)}{\hat{v}_g(s)} = c^T(sI-A)^{-1}b$$

Hence at this stage both steady state (dc) and line transfer functions are available, as shown by block 6a in the Flowchart of Fig. 2.1. We now undertake to include the duty ratio modulation effect into the basic averaged model (3.3).

Perturbation

Suppose now that the duty ratio changes from cycle to cycle, that is, $d(t) = D + \hat{d}$ where D is the steady state (dc) duty ratio as before and $\hat{d}$ is a superimposed (ac) variation. With the corresponding

perturbation definition $x = X + \hat{x}$, $y = Y + \hat{y}$, and $v_g = V_g + \hat{v}_g$ the basic model (3.3) becomes:

$$\dot{\hat{x}} = AX+bV_g + A\hat{x}+b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\hat{d} + [(A_1-A_2)\hat{x} + (b_1-b_2)\hat{v}_g]\hat{d}$$

dc term; line variation; duty ratio variation; nonlinear second-order term

$$Y + \hat{y} = c^TX + c^T\hat{x} + (c_1^T-c_2^T)X\hat{d} + (c_1^T-c_2^T)\hat{x}\hat{d} \qquad (3.11)$$

dc term; ac term; ac term; nonlinear term

The perturbed state-space description is nonlinear owing to the presence of the product of the two time-dependent quantities $\hat{x}$ and $\hat{d}$.

Linearization and final state-space averaged model

Let us now make the small-signal approximation, namely that departures from the steady state values are small compared to the steady state values themselves:

$$\frac{\hat{v}_g}{V_g} << 1, \quad \frac{\hat{d}}{D} << 1, \quad \frac{\hat{x}}{X} << 1 \qquad (3.12)$$

Then, using approximations (3.12) we neglect all nonlinear terms such as the second-order terms in (3.11) and obtain once again a linear system, but including duty-ratio modulation $\hat{d}$. After separating steady state (dc) and dynamic (ac) parts of this linearized system we arrive at the following results for the final state-space averaged model.

Steady state (dc) model:

$$X = -A^{-1}bV_g, \qquad Y = c^T X = -c^T A^{-1} b V_g \tag{3.13}$$

Dynamic (ac small-signal) model:

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\hat{d} \tag{3.14}$$

$$\hat{y} = c^T\hat{x} + (c_1^T-c_2^T)X\hat{d}$$

In these results, A, b and c^T are given as before by (3.5).

Equations (3.13) and (3.14) represent the small-signal low-frequency model of any two-state switching dc-to-dc converter working in the continuous conduction mode.

From (3.14), the duty ratio modulation $\hat{d}$ to state-variable $\hat{x}$ or to output $\hat{y}$ transfer functions are directly obtained as:

$$\frac{\hat{x}(s)}{\hat{d}(s)} = (sI-A)^{-1}[(A_1-A_2)X + (b_1-b_2)V_g] \tag{3.15}$$

$$\frac{\hat{y}(s)}{\hat{d}(s)} = c^T(sI-A)^{-1}[(A_1-A_2)X + (b_1-b_2)V_g] + (c_1^T-c_2^T)X$$

It is important to note that by neglect of the nonlinear term in (3.11) the source of harmonics is effectively removed. Therefore, the linear description (3.14) is actually a linearized describing function result that is the limit of the describing function as the amplitude of the input signals $\hat{v}_g$ and/or $\hat{d}$ becomes vanishingly small. The significance of this is that the theoretical frequency response obtained from (3.14) for line to output and duty ratio to output transfer functions can be compared with experimental describing function measurements as explained in [1], [2], or [8], in which

small-signal assumption (3.12) is preserved. Very good agreement up to close to half the switching frequency has been demonstrated repeatedly [1], [2], [3], [7].

Example: boost power stage with parasitics

We now illustrate the method for the boost power stage shown in Fig. 3.1.

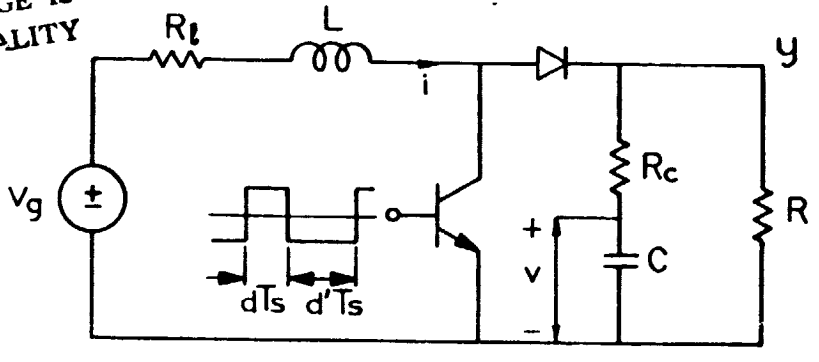


Fig. 3.1 Example for state-space averaged modelling: boost power stage with parasitics included.

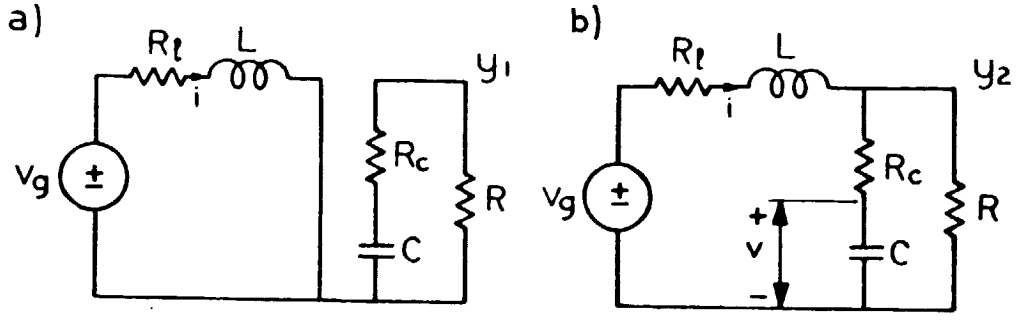


Fig. 3.2 Two switched circuit models of the circuit in Fig. 3.1 with assumption of ideal switches. All elements in the final state-space averaged model (3.13) and (3.14) are obtained: A_1, b_1, c_1^T from a) for interval dT_s, and A_2, b_2, c_2^T from b) for interval $d'T_s$.

With assumption of ideal switched, the two switched models are as shown in Fig. 3.2. For choice of state-space vector $x^T = (i\ v)$, the state-space equations become:

$$\begin{array}{ll} \text{(i) interval } T_s d: & \text{(ii) interval } T_s d': \\ \dot{x} = A_1 x + b v_g & \dot{x} = A_2 x + b v_g \\ y = c_1^T x & y_2 = c_2^T x \end{array} \tag{3.16}$$

where

$$A_1 = \begin{bmatrix} -\frac{R_\ell}{L} & 0 \\ 0 & -\frac{1}{(R+R_c)C} \end{bmatrix} \quad A_2 = \begin{bmatrix} -\frac{R_\ell + R_c \| R}{L} & -\frac{R}{L(R+R_c)} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix}$$

$$c_1^T = \begin{bmatrix} 0 & \frac{R}{R+R_c} \end{bmatrix} \quad c_2^T = \begin{bmatrix} R \| R_c & \frac{R}{R+R_c} \end{bmatrix} \tag{3.17}$$

Note that (3.16) is the special case of (3.1) in which $b_1 = b_2 = b = [1/L\ 0]^T$.

Using (3.17) and (3.5) in the general result (3.13) and (3.14), we obtain the following final state-space averaged model.

Steady-state (dc) model:

$$X = \begin{bmatrix} I \\ V \end{bmatrix} = \frac{V_g}{R'} \begin{bmatrix} 1 \\ (1-D)R \end{bmatrix}, \quad Y = \frac{V_g(1-D)R}{R'} \tag{3.18}$$

in which I is the dc inductor current, V is the dc capacitor voltage, and Y is the dc output voltage.

Dynamic (ac small signal) model:

$$\frac{d}{dt}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} = \begin{bmatrix} -\dfrac{R+(1-D)(R_c\|R)}{L} & -\dfrac{(1-D)R}{L(R+R_c)} \\ \dfrac{(1-D)R}{(R+R_c)C} & -\dfrac{1}{(R+R_c)C}\end{bmatrix}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}\hat{v}_g + \begin{bmatrix}\frac{R}{L} & \frac{(D'R+R_c)}{R+R_c}\\ -\frac{R}{(R+R_c)C}\end{bmatrix}\frac{V_g\hat{d}}{R'} \qquad (3.19)$$

$$\hat{y} = \begin{bmatrix}(1-D)(R_c\|R) & \frac{R}{R+R_c}\end{bmatrix}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} - V_g\frac{R_c\|R}{R'}\hat{d}$$

in which $R' \triangleq (1-D)^2R + R_\ell + D(1-d)(R_c\|R)$.

We now look more closely at the dc voltage transformation ratio in (3.18):

$$\frac{V}{V_g} = \frac{Y}{V_g} = \underbrace{\frac{1}{1-D}}_{\substack{\text{ideal}\\ \text{dc gain}}} \underbrace{\frac{(1-D)^2R}{(1-D)^2R + R_\ell + D(1-D)(R_c\|R)}}_{\text{correction factor}} \qquad (3.20)$$

This shows that the ideal dc voltage gain is 1/D' when all parasitics are zero ($R_\ell = 0$, $R_c = 0$) and that in their presence it is slightly reduced by a correction factor less than 1. Also we observe that nonzero esr of the capacitance ($R_c \neq 0$) (with consequent discontinuity of the output voltage) affects the dc gain and appears effectively as a resistance $DD'(R_c\|R)$ in series with the inductor resistance R_ℓ. This effect due to the discontinuity of output voltage was not included in [2], but was correctly accounted for in [1].

This is also a good example to show how even tiny parasitic resistances could significantly alter dc gain characteristics and efficiency of the converter. Just for simplicity of presentation, take $R_c = 0$ in (3.20) and consider voltage gain V/V_g as a function of duty ratio D. It is easy to see that in this more realistic case ($R\ell \neq 0$) it will have a maximum $(V/V_g)_{max} = 0.5\sqrt{R/R\ell}$ at $D_m = 1 - \sqrt{R\ell/R}$, while in the ideal case it increases without the limit, as shown in Fig. 3.3. As a numerical example, for $R = 20\Omega$, $R\ell = 0.2\Omega$ the maximum dc gain is $(V/V_g)_{max} = 5$ at $D_m = 0.9$.

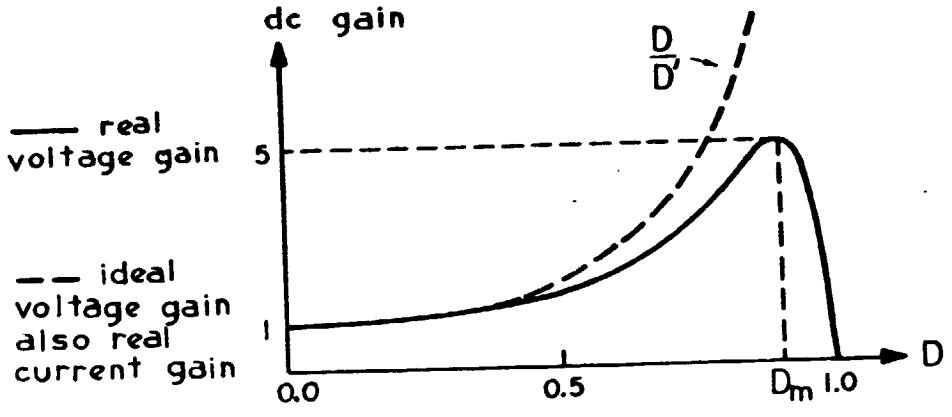


Fig. 3.3 Voltage dc gain with inductor parasitic resistance included.

It is interesting to note, however, that the dc current conversion is not affected by inclusion of parasitics and stays at $I_{in}/I_{out} = 1/D'$, or the same as the ideal dc voltage gain shown in Fig. 3.3. Therefore, the efficiency $\eta(D)$ of the converter as a function of duty ratio D could be simply obtained by dividing the two curves in Fig. 3.3 to produce Fig. 3.4. For the same numerical example $R\ell/R = 0.01$, the efficiency would drop to only 50% at the

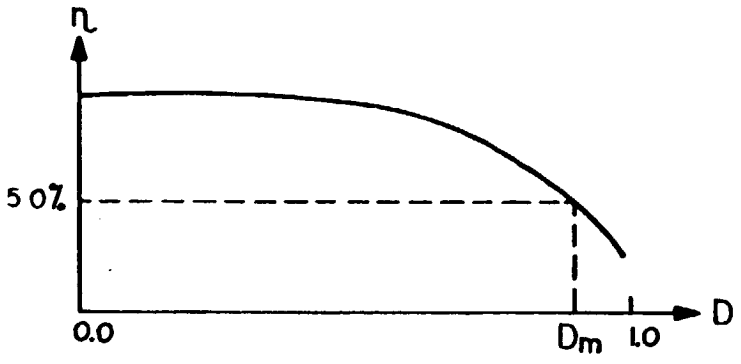


Fig. 3.4 Efficiency of the boost converter as a function of duty ratio for $R_\ell \neq 0$.

maximum dc voltage gain of 5. This illustrates in a rather dramatic fashion how even the small resistance inevitably associated with any inductor could drastically reduce efficiency and alter dc voltage conversion. One can now properly appreciate the importance of inclusion of various parasitic effects which distinguish the ideal lossless circuits from the real lossy ones.

From the dynamic model (3.19) one can find the line voltage to output and duty ratio to output transfer functions by applying (3.10) and (3.15). If we take for simplicity $R_c = 0$, the following transfer functions, which now again include the effects of nonzero R_ℓ are obtained:

$$G_{vg} = \frac{\hat{v}(s)}{\hat{v}_g(s)} = G_{og} \frac{1}{1 + \frac{s}{Q\omega_o} + (\frac{s}{\omega_o})^2}$$

$$G_{vd} = \frac{\hat{v}(s)}{\hat{d}(s)} = G_{od} \frac{1 - \frac{s}{\omega_a}}{1 + \frac{s}{Q\omega_o} + (\frac{s}{\omega_o})^2} \qquad (3.21)$$

where

$$\omega_a = (D'^2R - R_\ell)/L$$

$$\omega_o = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{R_\ell}{R}\frac{1}{D'^2}} \; ; \quad Q = \frac{D'^2R + R_\ell}{\omega_o(CRR_\ell + L)}$$

$$G_{og} = \frac{1}{D'} \frac{1}{1 + \frac{R_\ell}{R}\cdot\frac{1}{D'^2}} \; ; \quad G_{od} = \frac{V_g}{D'^2} \frac{D'^2R - R_\ell}{\left(D'^2R + R_\ell\right)^2} D'^2R$$

These results agree exactly with those obtained in [1] by following a different method of averaged model derivation based on the equivalence of circuit topologies of two switched networks.

The fundamental result of this section is the development of the general state-space averaged model represented by (3.13) and (3.14), which can be easily used to find the small-signal low-frequency model of any switching dc-to-dc converter. This was demonstrated for a boost power stage with parasitics resulting in the averaged model (3.18) and (3.19). It is important to emphasize that, unlike the transfer function description, the state-space description (3.13) and (3.14) gives the complete system behavior. This is very useful in implementing two-loop and multi-loop feedback when two or more states are used in a feedback path to modulate the duty ratio $\hat{d}$. For example, both output voltage and inductor current may be returned in a feedback loop.

3.2 Hybrid modelling

In this section it will be shown that for any specific converter a useful circuit realization of the basic averaged model given by (3.3) can always be found. Then, in the following section, the perturbation and linearization steps will be carried out on the circuit model finally to arrive at the circuit model equivalent of (3.13) and (3.14).

The circuit realization will be demonstrated for the same boost power stage example, for which the basic state-space averaged model (3.3) becomes:

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_\ell + d'(R_c \| R)}{L} & -\frac{d'R}{L(R+R_c)} \\ \\ \frac{d'R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_g$$

$$y = \begin{bmatrix} d'(R_c \| R) & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} \qquad (3.22)$$

In order to "connect" the circuit, we express the capacitor voltage v in terms of the desired output quantity y as:

$$v = \frac{R+R_c}{R} y - (1-d)R_c i$$

or, in matrix form

$$\begin{bmatrix} i \\ v \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -d'R_c & \frac{R+R_c}{R} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} \tag{3.23}$$

Substitution of (3.23) into (3.22) gives

$$\begin{bmatrix} L\frac{di}{dt} \\ C\frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -(R_\ell + dd'(R_c \| R) & d' \\ d' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_g \tag{3.24}$$

additional resistance

ideal transformer

From (3.24) one can easily reconstruct the circuit representation shown in Fig. 3.5.

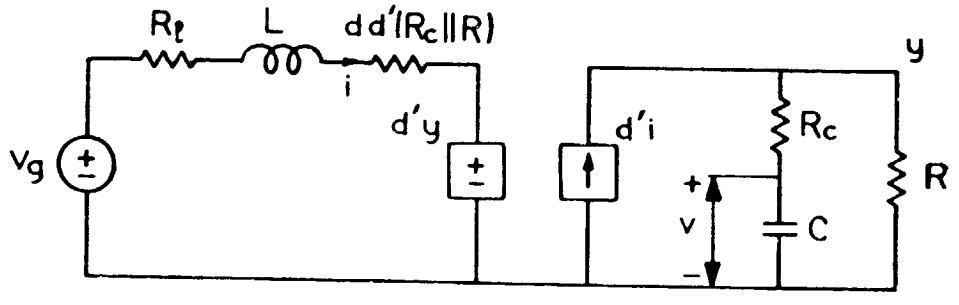


Fig. 3.5 Circuit realization of the basic state-space averaged model (3.24) through hybrid modelling.

The basic model (3.24) is valid for the dc regime, and the two dependent generators can be modeled as an ideal d':1 transformer whose range extends down to dc, as shown in Fig. 3.6.

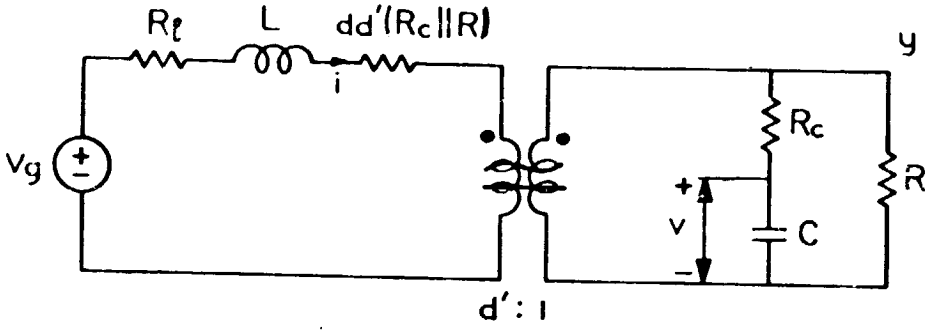


Fig. 3.6 Basic circuit averaged model for the boost circuit example in Fig. 3.1. Both dc-to-dc conversion and line variation are modelled when $d(t) = D$.

A word about the new transformer symbol introduced in Fig. 3.6 is appropriate here. In the modelling of dc-to-dc converters a need naturally arises to have as a convenient modelling tool special types of transformers: a transformer which operates for both ac and dc signals, as for example the one in Fig. 3.6, and also a transformer which only works at dc (for which the need will arise in Part II). Even though these transformers are not physically realizable they are, nevertheless, very useful in modelling the basic converter function: dc-to-dc conversion. Hence, as an indicator of their specific functions, the symbols of Fig. 3.7 are introduced. For consistency, the conventional, physically realizable, ac transformer only, is pictorially represented as in Fig. 3.7c. Later, for similar purposes, the same overprint glyphs will be used with resistance symbols.

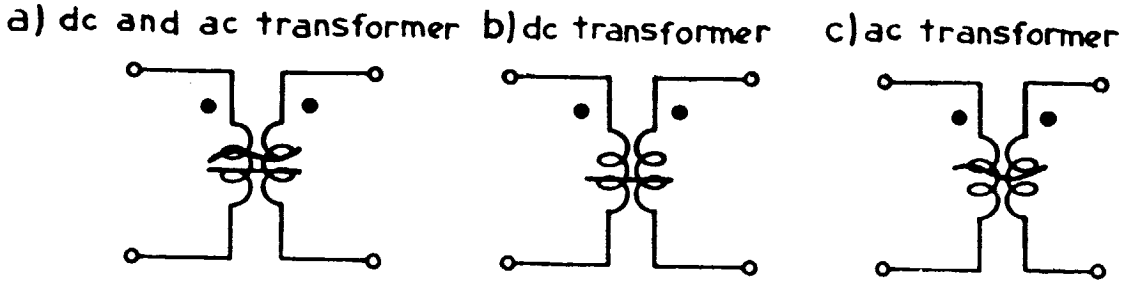


Fig. 3.7 Definition of various transformer symbols.

As before, we find that the circuit model in Fig. 3.6 reduces for d = 1 to the switched model in Fig. 3.2a, and for d = 0 to the switched model in Fig. 3.2b. In both cases the additional resistance $dd'(R_c \| R)$ disappears, as it should.

If the duty ratio is constant so d = D, the dc regime can be found easily by considering inductance L to be short and capacitance C to be open for dc, and the transformer to have a d':1 ratio. Hence the dc voltage gain (3.20) can be directly seen from Fig. 3.6 Similarly, all line transfer functions corresponding to (3.10) can be easily found from Fig. 3.6.

It is interesting now to compare this ideal d':1 transformer with the usual ac transformer. While in the latter the turns ratio is fixed, the one employed in our model has a dynamic turns ratio d':1 which changes when the duty ratio is a function of time, d(t). It is through this ideal transformer that the actual controlling function is achieved when the feedback loop is closed. In addition the ideal transformer has a dc transformation ratio d':1, while a real transformer works for ac signals only. Nevertheless, the concept of the ideal transformer in Fig. 3.6 with such properties is a very useful one, since after all, the switching converter has the overall property of a dc-to-dc transformer whose turns ratio can be dynamically adjusted by duty ratio modulation to achieve the controlling function. We will, however, see in the next section how this can be more explicitly modelled in terms of duty-ratio dependent generators only.

Following the procedure outlined in this section one can easily obtain the basic averaged circuit models of three common converter power stages, as shown in the summary of Fig.3.8 .

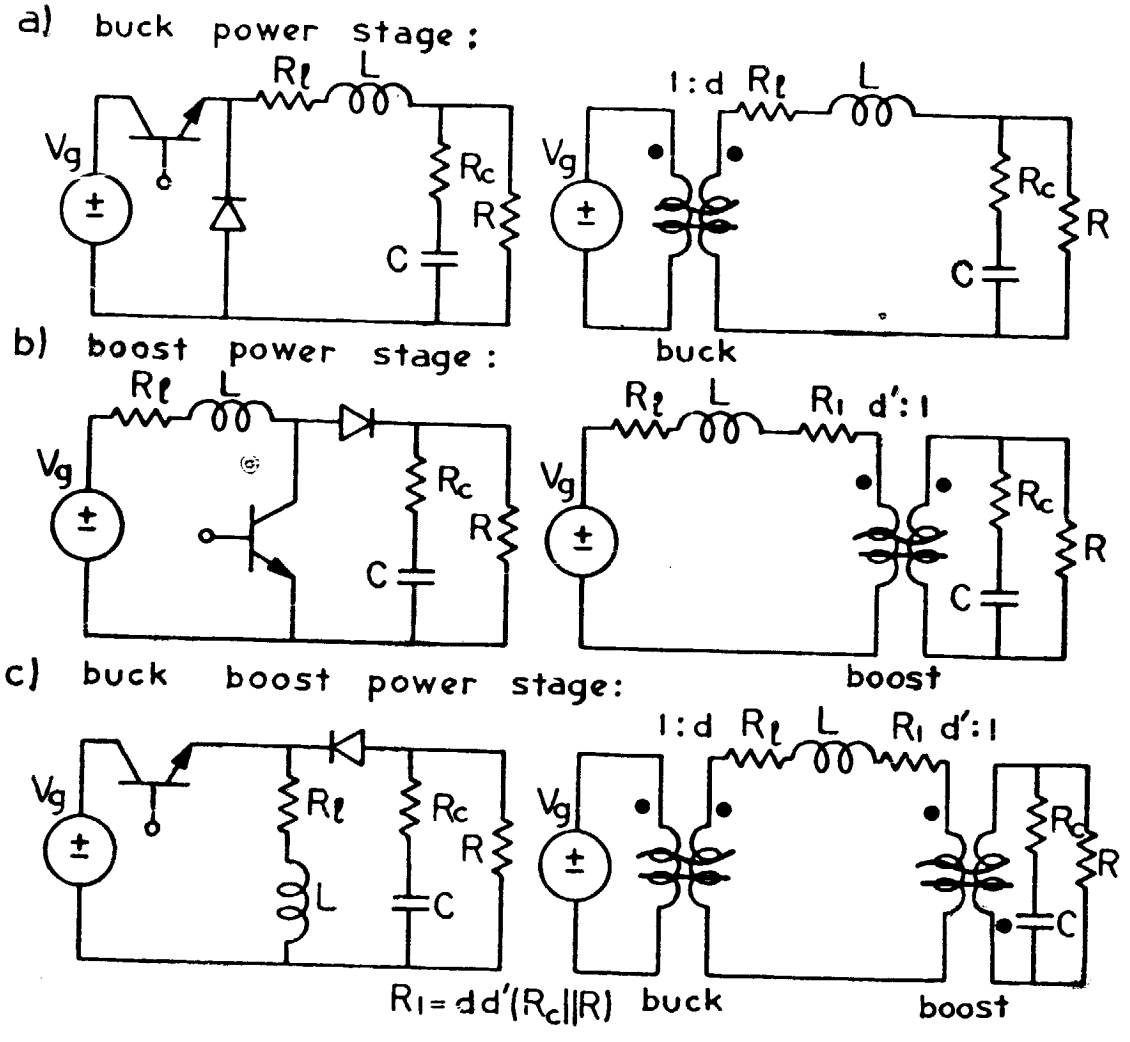


Fig. 3.8 Summary of basic circuit averaged models for three common power stages: buck, boost, and buck-boost.

The two switched circuit state-space models for the power stages in Fig.3.8 are such that the general equations (3.1) reduce to the special cases $A_1 = A_2 = A$, $b_1 \neq b_2 = 0$ (zero vector) for the buck power stage, and $A_1 \neq A_2$, $b_1 = b_2 = b$ for the boost power stage,

whereas for the buck-boost power stage $A_1 \neq A_2$ and $b_1 \neq b_2 = 0$ so that the general case is retained.

3.3 Circuit averaging

As indicated at the beginning of this chapter, in this section the alternative path b in the Flowchart of Fig. 2.1 will be followed, and equivalence with the previously developed path a firmly established. The final circuit averaged model for the same example of the boost power stage will be arrived at, which is equivalent to its corresponding state-space description given by (3.18) and (3.19).

The averaged circuit models shown in Fig. 3.8 could have been obtained as in [2] by directly averaging the corresponding components of the two switched models. However, even for some simple cases such as the buck-boost or tapped-inductor boost [1] this presents some difficulty owing to the requirement of having two switched circuit models topologically equivalent, while there is no such requirement in the outlined procedure.

In this section we proceed with the perturbation and linearization steps applied to the circuit model, continuing with the boost power stage as an example in order to include explicitly the duty ratio modulation effect.

Perturbation

If the averaged model in Fig. 3.8 is perturbed according to $v_g = V_g + \hat{v}_g$, $i = I + \hat{i}$, $d = D + \hat{d}$, $d' = D' - \hat{d}$, $v = V + \hat{v}$, $y = Y + \hat{y}$ the nonlinear model in Fig. 3.9 results.

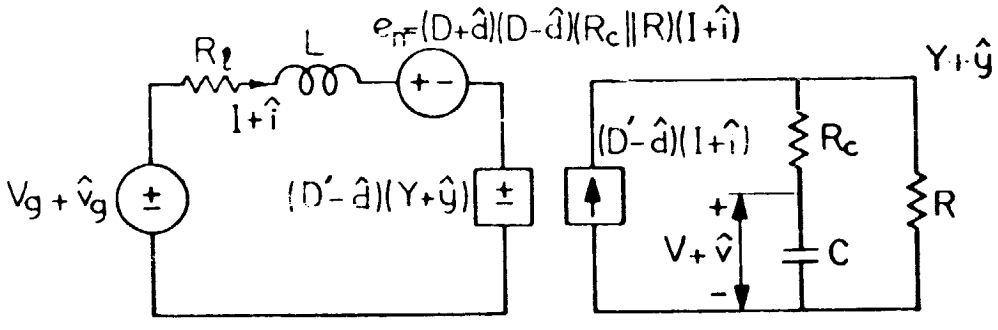


Fig. 3.9 Perturbation of the basic averaged circuit model in Fig. 3.6 includes the duty ratio modulation effect $\hat{d}$, but results in this nonlinear circuit model.

Linearization

Under the small-signal approximation (3.12), the following linear approximations are obtained:

$$e_n \approx DD'(R_c \| R)(I+\hat{i}) + \hat{d}(D'-D)(R_c \| R)I$$

$$(D'-\hat{d})(Y+\hat{y}) \approx D'(Y+\hat{y}) - \hat{d}Y$$

$$(D'-\hat{d})(I+\hat{i}) \approx D'(I+\hat{i}) - \hat{d}I$$

and the final averaged circuit model of Fig. 3.10 results. In this circuit model we have finally obtained the controlling function separated in terms of duty ratio $\hat{d}$ dependent generators e_1 and j_1, while the transformer turns ratio is dependent on the dc duty ratio D only. The circuit model obtained in Fig. 3.10 is equivalent to the state-space description given by (3.18) and (3.19).

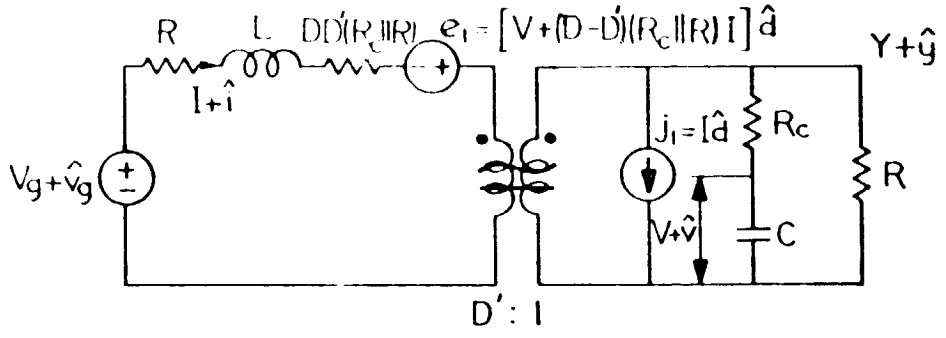


Fig. 3.10 Under small-signal assumption (3.12), the model in Fig. 3.9 is linearized and this final averaged circuit model of the boost stage in Fig. 3.1 is obtained.

This now completes the detailed investigation of all paths in the Flowchart of Fig. 2.1 except for the culminating block--the canonical circuit model, which is dealt with in the next chapter. However, before going into this final step of modelling, let us first review some of the more fundamental results obtained in this chapter.

A general method for modelling power stages of any switching dc-to-dc converter has been developed through the state-space approach. The fundamental step is in replacement of the state-space descriptions of the two switched networks by their average over the single switching period T_s, which results in a single continuous state-space equation description (3.3) designated the basic averaged state-space model. The essential approximations made are indicated in Chapter 1 and the Appendices, and are shown to be justified for any practical dc-to-dc switching converter. Their essence can be quickly summarized in the following sequence of implications:

switching ripple small $\Rightarrow$ natural frequencies $\ll$ switching frequency $\Rightarrow$ fundamental matrix $\sim$

$\sim$ linear approximation $\Rightarrow$ state-space averaging step

The subsequent perturbation and linearization step under the small-signal assumption (3.12) leads to the final state-space averaged model given by (3.13) and (3.14). These equations then serve as the basis for development of the most important qualitative result of this work, the canonical circuit model (block 5 in the Flowchart of Fig. 2.1).

In contrast with the state-space modelling approach, for any particular converter an alternative path via hybrid modelling and circuit transformation could be followed, which also arrives first at the final circuit averaged model equivalent of (3.13) and (3.14) and finally, after equivalent circuit transformations, again arrives at the canonical circuit model.

Although the state-space modelling approach has been developed in this chapter for two-state switching converters, the method can be extended to multiple-state converters. Examples of three-state converters are the familiar buck, boost and buck-boost power stages (shown in Fig. 1.1) operated in the discontinuous conduction mode (compare Chapter 1, Fig. 1.7), while dc-to-ac switching inverters in which a specific output waveform is "assembled" from discrete segments are examples of multiple-state converters.

In particular, Part II will demonstrate in detail how the extension of this state-space modelling approach can be accomplished for converters operating in the discontinuous conduction mode, where structural change takes place among three different switched network topologies as opposed to two we have treated so far in this chapter.

CHAPTER 4

CANONICAL CIRCUIT MODEL

This chapter is entirely devoted to the new canonical circuit model (see block 5 in the Flowchart of Fig. 2.1). The derivations via a general state-space model (3.13) and (3.14) are subsequently illustrated on a buck-boost example, while the results for a number of other converters are conveniently represented in the form of a table, thanks to the fixed circuit topology of the new canonical model. Finally, the significance of the new circuit model and general conclusions not otherwise available are thoroughly discussed.

Even though the general final state-space averaged model in (3.13) and (3.14) gives the complete description of the system behavior, one might still wish to derive a circuit model describing its input-output and control properties as illustrated in Fig. 4.1.

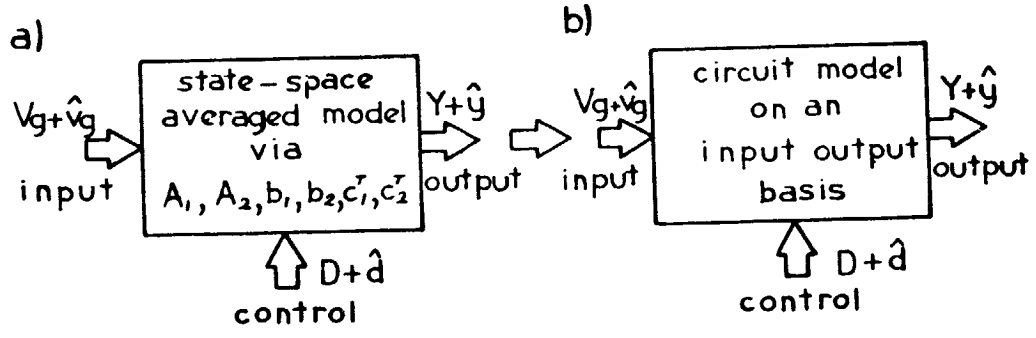


Fig. 4.1 Definition of the modelling objective: circuit averaged model describing input-output and control properties.

In going from the model of Fig. 4.1a to that of Fig. 4.1b some information about the internal behavior of some of the states will certainly be lost but, on the other hand, important advantages will be gained as were briefly outlined in Chapter 2, and as this section will illustrate.

We propose the following fixed topology circuit model, shown in Fig. 4.2 as a realization of the "black box" in Fig. 4.1b.

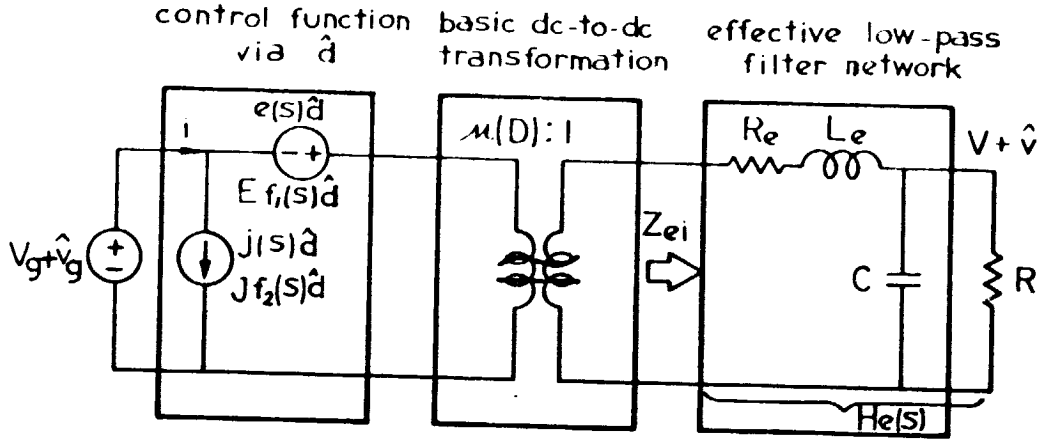


Fig. 4.2 Canonical circuit model realization of the "black box" in Fig. 4.1b, modelling the three essential functions of any dc-to-dc converter: control, basic dc conversion, and low-pass filtering.

We call this model the canonical circuit model, because any switching converter input-output model, regardless of its detailed configuration, could be represented in this form as long as the converter operates in the continuous conduction mode. Different converters are represented simply by appropriate sets of formulas for the four elements e(s), j(s), μ, $H_e(s)$ in the general equivalent circuit. The polarity of the ideal μ:1 transformer is determined by whether or not the power stage is polarity inverting. Its turns ratio μ is dependent on the dc duty ratio D, and since for modelling purposes the transformer is assumed to operate down to dc, it provides the basic dc-to-

dc level conversion. The single-section low-pass L_eC filter is shown in Fig. 4.2 only for illustration purposes, because the actual number and configuration of the L's and C's in the effective filter transfer function realization depends on the number of storage elements in the original converter.

The resistance R_e is included in the model of Fig. 4.2 to represent the damping properties of the effective low-pass filter. It is an "effective" resistance that accounts for various series ohmic resistances in the actual circuit (such as R_ℓ in the boost circuit example), the additional "switching" resistances due to discontinuity of the output voltage (such as $DD'(R_C \| R)$ in the boost circuit example), and also a "modulation" resistance that arises from a modulation of the switching transistor storage time [1].

4.1 Derivation of the canonical model through state-space

From the general state-space averaged model (3.13) and (3.14), we obtain directly using the Laplace transform:

$$\begin{aligned}\hat{x}(s) &= (sI-A)^{-1}b\hat{v}_g(s) + (sI-A)^{-1}[(A_1-A_2)X + (b_1-b_2)V_g]\hat{d}(s)\\ \hat{y}(s) &= c^T\hat{x}(s) + (c_1^T-c_2^T)X\hat{d}(s)\end{aligned} \tag{4.1}$$

Now, from the above complete set of transfer functions we single out those which describe the converter input-output properties, namely

$$\begin{aligned}\hat{y}(s) &= G_{vg}\,\hat{v}_g(s) + G_{vd}\,\hat{d}(s)\\ \hat{i}(s) &= G_{ig}\,\hat{v}_g(s) + G_{id}\,\hat{d}(s)\end{aligned} \tag{4.2}$$

in which the G's are known explicitly in terms of the matrix and vector elements in (4.1).

Equations (4.2) are analogous to the two-port network representation of the terminal properties of the network (output voltage $\hat{y}(s)$ and input current $\hat{i}(s)$). The subscripts designate the corresponding transfer functions. For example G_{vg} is the source voltage $\hat{v}_g$ to output voltage $\hat{y}$ transfer function, G_{id} is the duty ratio $\hat{d}$ to input current $\hat{i}(s)$ transfer function, and so on.

For the proposed canonical circuit model in Fig. 4.2, we directly get:

$$\begin{aligned}\hat{y}(s) &= (\hat{v}_g+e\hat{d})\,\frac{1}{\mu}\,H_e(s)\\ \hat{i}(s) &= j\,\hat{d} + (e\hat{d}+\hat{v}_g)\frac{1}{\mu^2 Z_{ei}(s)}\end{aligned} \tag{4.3}$$

or, after rearrangement into the form of (4.2):

$$\hat{y}(s) = \frac{1}{\mu} H_e(s)\, \hat{v}_g(s) + e\, \frac{1}{\mu} H_e(s)\hat{d}(s)$$

$$\hat{i}(s) = \frac{1}{\mu^2 Z_{ei}(s)}\, \hat{v}_g(s) + \left[j + \frac{e}{\mu^2 Z_{ei}(s)} \right] \hat{d}(s) \qquad (4.4)$$

Direct comparison of (4.2) and (4.4) provides the solutions for $H_e(s)$, $e(s)$, and $j(s)$ in terms of the known transfer functions G_{vg}, G_{vd}, G_{ig} and G_{id} as:

$$e(s) = \frac{G_{vd}(s)}{G_{vg}(s)}, \qquad j(s) = G_{id}(s) - e(s)G_{ig}(s)$$

$$H_e(s) = \mu G_{vg}(s) \qquad (4.5)$$

Note that in (4.5) the parameter $1/\mu$ represents the ideal dc voltage gain when all the parasitics are zero. For the previous boost power stage example, from (3.20) we get $\mu = 1\text{-}D$ and the correction factor in (3.20) is then associated with the effective filter network $H_e(s)$. However, μ could be found from

$$\frac{V}{V_g} = -c^T A^{-1} b = \frac{1}{\mu} \times (\text{correction factor}) \qquad (4.6)$$

by setting all parasitics to zero and reducing the correction factor to 1.

The physical significance of the ideal dc gain μ is that it arises as a consequence of the switching action, so it cannot be associated with the effective filter network which at dc has a gain (actually attenuation) equal to the correction factor.

The procedure for finding the four elements in the canonical model of Fig. 4.2 is now briefly reviewed. First, from (4.6) the

basic dc-to-dc conversion factor μ is found as a function of dc duty ratio D. Next, from the set of all transfer functions (4.1) only those defined by (4.2) are actually calculated. Then, by use of these four transfer functions G_{vd}, G_{vg}, G_{id}, G_{ig} in (4.5) the frequency dependent generators e(s) and j(s) as well as the low-pass filter transfer function $H_e(s)$ are obtained.

The two generators could be further put into the form

$$\begin{aligned} e(s) &= Ef_1(s) \\ j(s) &= Jf_2(s) \end{aligned} \tag{4.7}$$

where $f_1(0) = f_2(0) = 1$, such that the parameters E and J could be identified as dc gains of the frequency dependent functions e(s) and j(s).

Finally, a general synthesis procedure [10] for realization of L, C transfer functions terminated in a single load R could be used to obtain a low-pass ladder-network circuit realization of the effective low-pass network $H_e(s)$. Though for the second-order example of $H_e(s)$ this step is trivial and could be done by inspection, for higher-order transfer functions the orderly procedure of the synthesis [10] is almost mandatory.

Example: ideal buck-boost power stage

For the buck-boost circuit shown in Fig. 3.10c with $R_\ell = 0$ $R_c = 0$, the final state-space averaged model is:

$$\begin{bmatrix} \frac{d\hat{i}}{dt} \\ \\ \frac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{D'}{L} \\ \\ -\frac{D'}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \frac{D}{L} \\ \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{V_g - V}{L} \\ \\ -\frac{V}{D'RC} \end{bmatrix} \hat{d} \qquad (4.8)$$

in which the output voltage $\hat{y}$ coincides with the state-variable capacitance voltage $\hat{v}$.

From (4.6) and (4.8) one obtains $\mu = D'/D$. With use of (4.8) to derive transfer functions, and upon substitution into (4.5), there results

$$e(s) = \frac{-V}{D^2}\left(1 - s\frac{DL}{D'^2R}\right), \qquad j(s) = \frac{-V}{(1-D)^2R} \qquad (4.9)$$

$$H_e(s) = \frac{1}{1 + s/RC + s^2L_eC}, \qquad \mu = \frac{1-D}{D}$$

in which V is the dc output voltage.

The effective filter transfer function is easily seen as a low-pass LC filter with $L_e = L/D'^2$ and with load R. The two generators in the canonical model of Fig. 4.2 are identified by

$$E = \frac{-V}{D^2}, \qquad f_1(s) \equiv 1 - s\frac{DL}{D'^2R} \qquad (4.10)$$

$$J = \frac{-V}{(1-D)^2R}, \qquad f_2(s) \equiv 1$$

We now derive the same model but this time using the equivalent circuit transformations and path b in the Flowchart of Fig. 2.1.

After perturbation and linearization of the circuit averaged model in Fig. 3.8c (with $R_\ell = 0$, $R_c = 0$), the series of equivalent circuits of Fig. 4.3 is obtained.

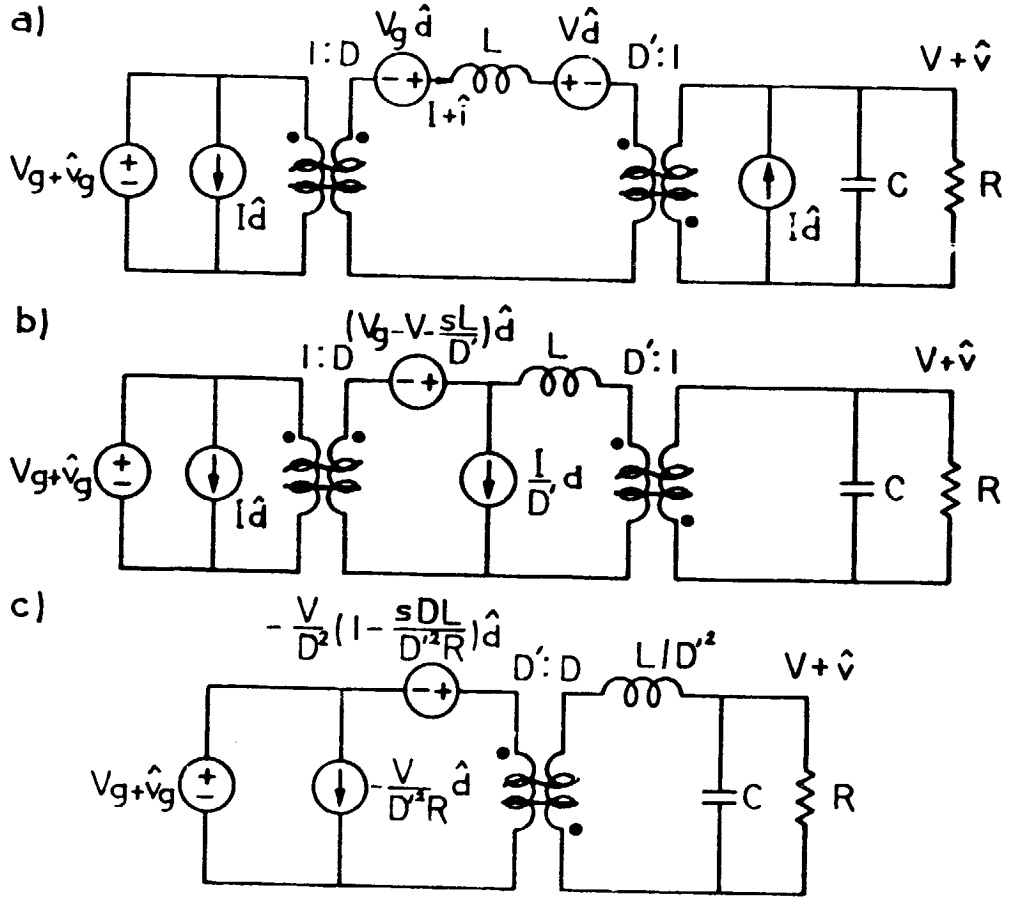


Fig. 4.3 Equivalent circuit transformations of the final circuit averaged model a) leading to its canonical circuit realization c), demonstrated on the buck-boost example of Fig. 3.8c (with $R_\ell=0$, $R_c=0$).

The objective of the transformations is to reduce the original four duty-ratio dependent generators in Fig. 4.3a to just two generators (voltage and current) in Fig. 4.3c which are at the input port of the model. As these circuit transformations unfold, one sees

how the frequency dependence in the generators arises naturally, as in Fig. 4.3b. Also, by transfer of the two generators in Fig. 4.3b from the secondary to the primary of the 1:D transformer, and the inductance L to the secondary of the D':1 transformer, the cascade of two ideal transformers is reduced to the single transformer with equivalent turns ratio D':D. At the same time the effective filter network L_e, C, R is generated.

Expressions for the elements in the canonical equivalent circuit can be found in a similar way for any converter configuration. Results for the three familiar converters, the buck, boost, and buck-boost power stages are summarized in Table I.

type	$\mathcal{M}(D)$	E	$f_1(s)$	J	$f_2(s)$	L_e
buck	$\frac{1}{D}$	$\frac{V}{D^2}$	1	$\frac{V}{R}$	1	L
boost	$1-D$	V	$1-s\frac{L_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$
buck-boost	$\frac{1-D}{D}$	$\frac{-V}{D^2}$	$1-s\frac{DL_e}{R}$	$\frac{-V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$

TABLE I Definition of the elements in the canonical circuit model of Fig. 4.2 for the three common power stages of Fig. 1.1.

It may be noted in Table I that, for the buck-boost power stage, parameters E and J have negative signs, namely $E = -V/D^2$ and $J = -V/(D'^2R)$. However, as seen from the polarity of the ideal D':D transformer in Fig. 4.3c this stage is an inverting one. Hence, for positive input dc voltage V_g, the output dc voltage V is negative

($V < 0$) since $V/V_g = -D/D'$. Therefore $E > 0$, $J > 0$ and consequently the polarity of the voltage and current duty-ratio dependent generators is not changed but is as shown in Fig. 4.3c. Moreover, this is true in general: regardless of any inversion property of the power stage, the polarity of the two generators stays the same as in Fig. 4.2. If some parasitics have been included in the original converter model (such as R_ℓ, parasitic resistance of the inductance) Table I would have had another column for R_e (effective series resistance) as seen in Fig. 4.2 with appropriate expressions.

Table I, together with the canonical circuit model of Fig. 4.2, could then conveniently be used to obtain all the important static (dc) and dynamic (ac) transfer properties of the converters listed in Table I. For example, Table II summarizing voltage gain and efficiency of three common converters could be generated in such a way. In Table II the effects of parasitics have also been included .

type	V/V_g (dc gain)	η (efficiency)
buck	$D\ \dfrac{R}{R+R_\ell}$	$\dfrac{R}{R+R_\ell}$
boost	$\dfrac{1}{D'}\ \dfrac{D'^2R}{D'^2R+R_\ell+DD'R_c\|\|R}$	$\dfrac{D'^2R}{D'^2R+R_\ell+DD'R_c\|\|R}$
buck-boost	$\dfrac{D}{D'}\ \dfrac{D'^2R}{D'^2R+R_\ell+DD'R_c\|\|R}$	$\dfrac{D'^2R}{D'^2R+R_\ell+DD'R_c\|\|R}$

TABLE II Dc transfer properties and efficiency of the three common power stages of Fig. 1.1 in the continuous conduction mode.

Similarly the dynamic (ac) transfer properties, that is, line voltage variation to output voltage and duty ratio modulation to output voltage, can be summarized for three common power stages of Fig. 1.1 in the form of Table III.

	buck	boost	buck-boost
G_{og}	$D\,\frac{R}{R+R_\ell}$	$\frac{1}{D'}\,\frac{D'^2R}{D'^2R+R_\ell}$	$\frac{D}{D'}\,\frac{D'^2R}{D'^2R+R_\ell}$
G_{od}	$V_g\,\frac{R}{R+R_\ell}$	$V_g\frac{(D'^2R-R_\ell)R}{(D'^2R+R_\ell)^2}$	$V_g\frac{D'^2R-(D-D')R_\ell}{(D'^2R+R_\ell)^2}R$
ω_o	$\frac{1}{\sqrt{LC}}\sqrt{1+\frac{R_\ell}{R}}$	$\frac{1}{\sqrt{LC}}\sqrt{D'^2+\frac{R_\ell}{R}}$	$\frac{1}{\sqrt{LC}}\sqrt{D'^2+\frac{R_\ell}{R}}$
Q	$\frac{1}{\omega_o}\,\frac{RR_\ell+L}{L+CRR_\ell}$	$\frac{1}{\omega_o}\,\frac{D'^2R+R_\ell}{L+CRR_\ell}$	$\frac{1}{\omega_o}\,\frac{D'^2R+R_\ell}{L+CRR_\ell}$
ω_a	∞	$\frac{D'^2R-R_\ell}{L}$	$\frac{D'^2R-(D-D')R_\ell}{DL}$

$$G_{vg}\triangleq\frac{\hat{v}}{\hat{v}_g}=G_{og}\,\frac{1}{1+s/Q\omega_o+(s/\omega_o)^2};\quad G_{vd}\triangleq\frac{\hat{v}}{\hat{d}}=G_{od}\,\frac{1-s/\omega_a}{1+s/Q\omega_o+(s/\omega_o)^2}$$

TABLE III Summary of the ac transfer properties of the three common power stages of Fig. 1.1 in the continuous conduction mode.

After filing the information on these converters in Tables I, II and III we can proceed to discuss the significance of the new canonical circuit model of Fig. 4.2 and related generalizations.

4.2 Significance of the canonical circuit model and related generalizations

The canonical circuit model of Fig. 4.2 incorporates all three basic properties of a dc-to-dc converter: the dc-to-dc conversion function (represented by the ideal μ:1 transformer); control (via duty ratio $\hat{d}$ dependent generators); and low-pass filtering (represented by the effective low-pass filter network $H_e(s)$). Note also that the current generator $j(s)\,\hat{d}$ in the canonical circuit model, even though superfluous when the source voltage $\hat{v}_g(s)$ is ideal, is necessary to reflect the influence of a nonideal source generator (with some internal impedance) or of an input filter [7] upon the behavior of the converter. Its presence enables one easily to include the linearized circuit model of a switching converter power stage in other linear circuits, as the next chapter will illustrate.

Another significant feature of the canonical circuit model is that any switching dc-to-dc converter can be reduced by use of (4.1), (4.2), (4.5) and (4.6) to this fixed topology form, at least as far as its input-output and control properties are concerned. Hence the possibility arises for use of this model to compare in an easy and unique way various performance characteristics of different converters. Some examples of such comparisons are given below.

1. The filter networks can be compared with respect to their effectiveness throughout the dynamic duty cycle range D, because in general the effective filter elements depend on the steady state duty ratio D. Thus, one has the

opportunity to choose the configuration and to optimize the size and weight.

2. Basic dc-to-dc conversion factors $\mu_1(D)$ and $\mu_2(D)$ can be compared as to their effective range. For some converters, traversal of the range of duty ratio D from 0 to 1 generates any conversion ratio (as in the ideal buck-boost converter), while in others the conversion ratio might be restricted (as in the Weinberg converter [4], for which $1/2 < \mu < 1$).

3. In the control section of the canonical model one can compare the frequency dependences of the generators e(s) and j(s) for different converters and select the configuration that best facilitates stabilization of a feedback regulator. For example, in the buck-boost converter e(s) is a polynomial, containing actually a real zero in the right half-plane, which undoubtedly causes some stability problems and need for proper compensation.

4. Finally, the canonical model affords a very convenient means to store and file information on various dc-to-dc converters in a computer memory in a form comparable to Table I. Then, thanks to the fixed topology of the canonical circuit model, a single computer program can be used to calculate and plot various quantities as functions of frequency (input and output impedance, audio susceptibility, duty ratio to output transfer response, and so on). Also, various input filters and/or additional output filter networks can easily be added if desired.

We now discuss an important issue which has been intentionally skipped so far. From (4.5) it is concluded that in general the duty ratio dependent generators e(s) and j(s) are rational functions of complex frequency s. Hence, in general, both some new zeros and poles are introduced into the duty ratio to output transfer function owing to the switching action, in addition to the poles and zeros of the effective filter network (or line to output transfer function). However, in special cases, as in all those shown in Table I, the frequency dependence might reduce simply to polynomials, and even further it might show up only in the voltage-dependent generators (as in the boost, or buck-boost) and reduce to a constant ($f_2(s) \equiv 1$) for the current generator. Nevertheless, this does not prevent us from modifying any of these circuits in a way that would exhibit the general result -- introduction of both additional zeros as well as poles.

Let us now illustrate this general result on a simple modification of the familiar boost circuit, with a resonant L_1, C_1 circuit in series with the input inductance L, as shown in Fig. 4.4.

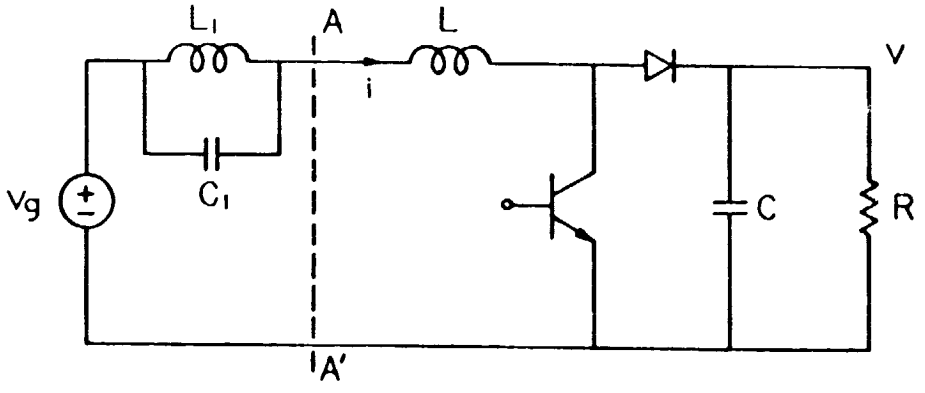


Fig. 4.4 Modified boost circuit as an illustration of general frequency behavior of the generators in the canonical circuit model of Fig. 4.2.

By introduction of the canonical circuit model for the boost power stage (for the circuit to the right of cross-section AA') and use of data from Table I. the equivalent averaged circuit model of Fig. 4.5a is obtained. Then, by application of the equivalent circuit transformation as outlined previously, the averaged model in the cancnical circuit form is obtained in Fig. 4.5b. As can be seen from Fig. 4.5b, the voltage generator has a double pole at the resonant frequency $\omega_r = 1/\sqrt{L_1C_1}$ of the parallel L_1,C_1 network. However, the effective filter transfer function has a double zero (null in magnitude) at precisely the same location such that the two pairs effectively cancel. Hence, the resonant null in the magnitude response, while present in the line voltage to output transfer function, is not seen in the duty ratio to output transfer function.

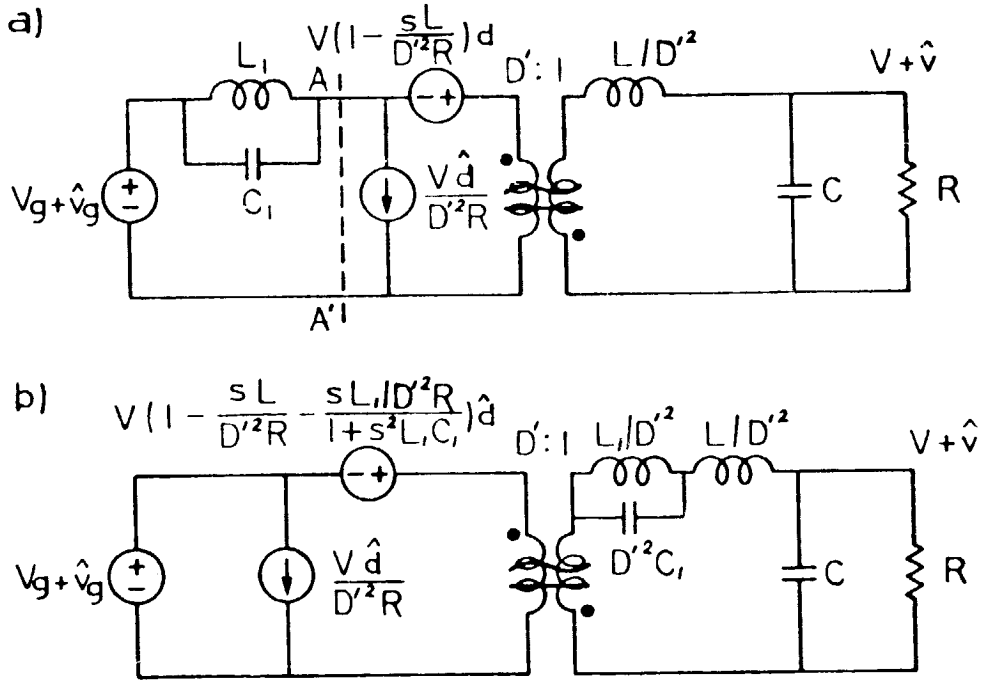


Fig. 4.5 Equivalent circuit transformation leading to the canonical circuit model b) of the circuit in Fig. 4.4.

Therefore, the positive effect of rejection of certain input frequencies around the resonant frequency ω_r is not accompanied by a detrimental effect on the loop gain, which will not contain a null in the magnitude response.

The example demonstrates yet another important aspect of modelling with use of the averaging technique. Instead of applying it directly to the whole circuit in Fig. 4.4, we have instead implemented it only with respect to the storage element network which effectively takes part in the switching action, namely L, C, and R. Upon substitution of the switched part of the network by the averaged circuit model, all other linear circuits of the complete model are retained as they appear in the original circuit (such as L_1, C_1 in Fig. 4.5a). Again, the current generator in Fig. 4.5a is the one which reflects the effect of the input resonant circuit.

After the detailed exposition we are now ready to briefly review the salient features of this new canonical circuit model (Fig. 4.2). Thanks to its fixed topology structure, different converters are represented simply by an appropriate set of formulas ((4.5) and (4.6)) for four elements in this general equivalent circuit. Besides its unified description, of which several examples are given in Table I, one of the advantages of the canonical circuit model is that various performance characteristics of different switching converters can be compared in a quick and easy manner.

Perhaps the most important consequence of the canonical circuit model derivation via the general state-space averaged model (3.13), (3.14), (4.1) and (4.2) is its prediction through (4.5) of additional zeros as well as poles in the duty ratio to output transfer function. In addition, frequency dependence is anticipated in the duty ratio dependent current generator of Fig. 4.2, even though for particular converters considered in Table I it reduces merely to a constant. Furthermore, for some switching networks which would effectively involve more than two storage elements, higher order polynomials should be expected in $f_1(s)$ and/or $f_2(s)$ of Fig. 4.2.

In fact, Part III has resulted as a consequence of the search for such switching networks which would demonstrate the predictions anticipated by this general canonical model. There, a new class of switching converters generated by the various cascade combinations of the two fundamental converters, buck and boost of Fig. 1.1, not only shows yet another topological realization of the generalized switching converter in Fig. 1.11 but also demonstrates how powerful the general equations (4.5) and (4.6) are in arriving at the canonical circuit model of Fig. 4.2. In addition, this circuit model exhibits a single zero (first-order) polynomial in complex frequency s for the duty ratio dependent current generator and a second-order polynomial for the duty ratio dependent voltage generator, besides its low-pass effective filter of fourth order (four storage elements L's and C's). Therefore, general predictions made available by the derivation of the canonical circuit model in this chapter will be confirmed by the new class of switching converters in Part III and a

new switching converter of Part IV which employs an optimum topology.

As was demonstrated in Chapter 1, the main difficulty in analyzing a switching-mode regulator (Fig. 1.10) lies in the modelling of its nonlinear part, the switching-mode converter. However, we have succeeded in previous chapters in obtaining the small-signal low-frequency circuit model of any "two-state" switching dc-to-dc converter, operating in the continuous conduction mode, in the canonical circuit form. In the next chapter it will be demonstrated how this converter circuit model can easily be incorporated in the complete regulator, and the general switching mode regulator circuit model obtained.

CHAPTER 5

SWITCHING MODE REGULATOR MODELLING

This chapter represents the culmination of the modelling procedures developed in Part I in that it demonstrates the ease with which the different converter circuit models, and the canonical circuit model in particluar, can be incorporated into more complicated systems such as a switching-mode regulator.

First a brief discussion of modelling of modulator stages (such as, for example, the single-edge clocked pulse width modulator of Fig. 1.10) in general is presented, which leads to a complete general switching-mode regulator circuit model.

This then serves as a basis for establishment of analytic quantitative expressions for the important regulator properties loop gain T, input and output impedances Z_i and Z_o, and line transmission characteristic F of the resulting linear negative feedback circuit model of a complete regulator. Knowledge of these quantitative relations and the well-known body of linear feedback theory will not only permit one to design a regulator according to the performance requirements (line and load regulation etc) but also, by proper design of the frequency shaping compensation network, to ensure stability of operation under all operating conditions.

For the same reason, an <u>in depth</u> discussion of the input properties, both open-loop and especially closed-loop input impedance, is included to reveal the source of potential instability when a switching regulator is a part of a larger system (for example, preceded

by an input filter or some other linear network or converter). This comes as a consequence of a unique behavior of a switching regulator, which at low frequencies exhibits a negative incremental input resistance R_i as will be confirmed both qualitatively and quantitatively. It is, perhaps, interesting to mention that none of the other techniques of modelling switching regulators ([11] through [17]) is able to describe such behavior, owing to the lack of an input model of the converter and/or regulator.

Consider now a switching mode regulator as shown in Fig. 5.1.

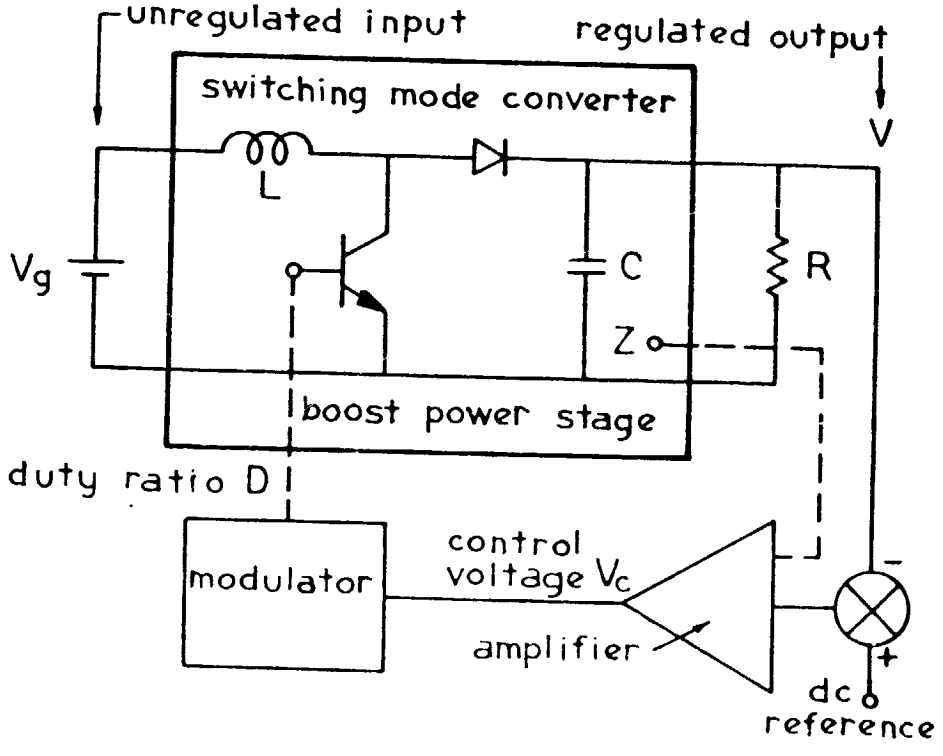


Fig. 5.1 Switching-mode regulator of Fig. 1.10 with input and output filters omitted in order to expose the properties of the converter-regulator alone.

For concreteness and in order to have the convenient illustrative example throughout derivation, the switching-mode converter is represented by a boost power stage, but the discussion applies to any converter.

5.1 Modulator stage modelling and complete regulator circuit model

So far, we have obtained the canonical circuit model for the switching-mode converter. The next step in development of the regulator equivalent circuit is to obtain a model for the modulator. This is easily done by writing an expression for the essential function of the modulator, which is to convert an (analog) control voltage V_c to the switch duty ratio D. This expression can be written $D = V_c/V_m$ in which, by definition, V_m is the range of control signal required to sweep the duty ratio over its full range from 0 to 1. A small variation $\hat{v}_c$ superimposed upon V_c therefore produces a corresponding variation $\hat{d} = \hat{v}_c/V_m$ in D, which can be generalized to account for a nonuniform frequency response as

$$\hat{d} = \frac{f_m(s)}{V_m}\,\hat{v}_c \qquad (5.1)$$

in which $f_m(0) = 1$. Thus, the control voltage to duty ratio small-signal transmission characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved. Hence, by substitution for $\hat{d}$ from (5.1) the two generators in the canonical circuit model of the switching converter can be expressed in terms of the ac control voltage $\hat{v}_c$, and the resulting model is then a linear ac equivalent circuit that represents the small-signal transfer properties of the nonlinear processes in the modulator and converter.

It remains simply to add a linear amplifier to obtain the equivalent circuit of the closed-loop regulator as shown in Fig. 5.2.

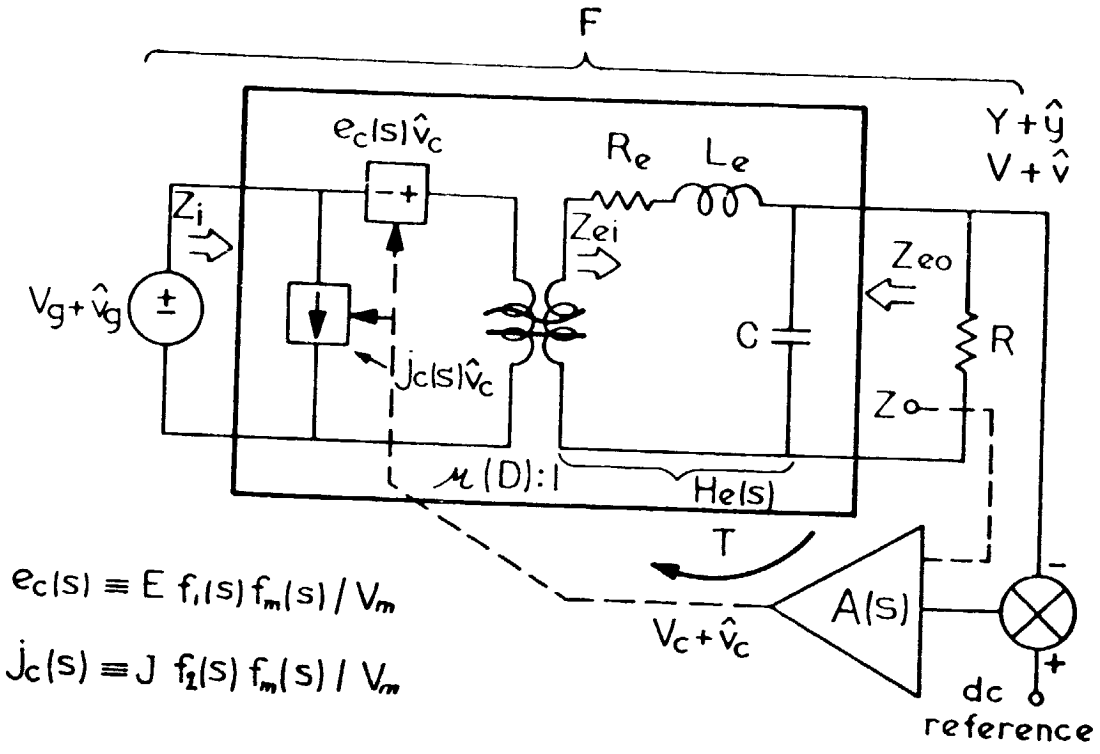


Fig. 5.2 General ac small-signal equivalent circuit for the switching-mode regulator of Fig. 5.1.

The modulator transfer function has been incorporated in the generator designations $e_c(s)$, $j_c(s)$, and the generator symbol has been changed from a circle to a square to emphasize the fact that, in the closed-loop regulator, the generators no longer are independent but are dependent on another signal in the same system. The connection from point Y to the error amplifier, via the reference voltage summing node, represents the basic voltage feedback necessary to establish the system as a voltage regulator. The dashed connection from point Z indicates a possible additional feedback sensing; this second feedback signal may be derived, for example, from the inductor flux, inductor current, or capacitor current, as in various "two-loop" configurations that are in use [9].

The current generator $j_c(s)\hat{v}_c$ in Fig. 5.2 may seem superfluous because it is shorted by the zero source impedance. However, its presence is necessary not only to reflect the influence of an input filter or nonzero source impedance, as was previously illustrated (see Fig. 4.5 for example) but, more importantly, properly to represent the switching regulator itself, namely its negative input impedance at low frequencies, as the analysis in Sections 5.2 and 5.3 will confirm.

5.2 Analysis of switching-mode regulator

A number of quantities of interest are shown explicitly in the regulator model of Fig. 5.2. The averaging filter is defined to have a voltage transfer function $H_e(s)$ in the presence of the external load R; this represents the basic low-pass filter characteristic. Also, the effective filter has an input impedance Z_{ei} and output impedance Z_{eo} at the ports indicated; these are defined for the open-loop condition of the regulator, and hence are properties of the effective low-pass filter and load resistance only, and are unaffected by any other regulator parameter. Explicitly, Z_{ei} is the impedance of R_e and L_e in series with C and R in parallel, and Z_{eo} is the impedance of C in parallel with R_e and L_e. The subscript e is employed in H_e, Z_{ei}, Z_{eo} because these are all properties of the averaging filter in terms of the "effective" inductance L_e and resistance R_e.

The remaining quantities identified in Fig. 5.2 represent properties of principal interest in the design and analysis of the regulator. The loop gain T is a fundamental parameter upon which important properties of the regulator depend; it must be designed to

have a dc value sufficient to provide the required dc regulation specification, and it must be frequency shaped to ensure stability. The closed-loop regulator output impedance Z_o is an important system specification that determines the transient response and load regulation, and the line transmission characteristic $F = \hat{v}/\hat{v}_g$ (sometimes also called audiosusceptibility characteristic) specifies the ability of the closed-loop regulator to prevent line voltage variations from appearing in the regulated output. Finally, the closed-loop regulator input impedance Z_i is important when the regulator is preceded by an input filter or some other network. Both the dc value and frequency response of each of the terminal parameters Z_o, F and Z_i are important, and are strongly influenced by the dc value and frequency response of the loop gain T.

Analysis of the equivalent circuit in Fig. 5.2 leads to the following results:

$$T = \frac{E}{V_m} f_1(s) f_m(s) H_e(s) A(s) = G_{vd} A(s) f_m(s)/V_m \tag{5.2}$$

$$Z_o = \frac{Z_{eo}}{1 + T} \tag{5.3}$$

$$F = \frac{1}{\mu} \frac{H_e}{1 + T} = \frac{G_{vg}}{1 + T} \tag{5.4}$$

$$\frac{1}{Z_i} = - \frac{T}{1 + T} \frac{1}{\mu^2 R f_1(s)} + \frac{1}{1 + T} \frac{1}{\mu^2 Z_{ei}} \tag{5.5}$$

The first three expressions are a direct consequence of the general results of linear feedback theory. Namely, the expression for loop gain T is obtained simply from Fig. 5.2 as the product of the voltage generator $e_c(s) = \frac{E}{V_m} f_1(s) f_m(s)$, effective filter transfer

function $H_e(s)$, and amplifier gain $A(s)$, while the current generator $j_c(s)$ does not enter into the result since it is effectively shorted.

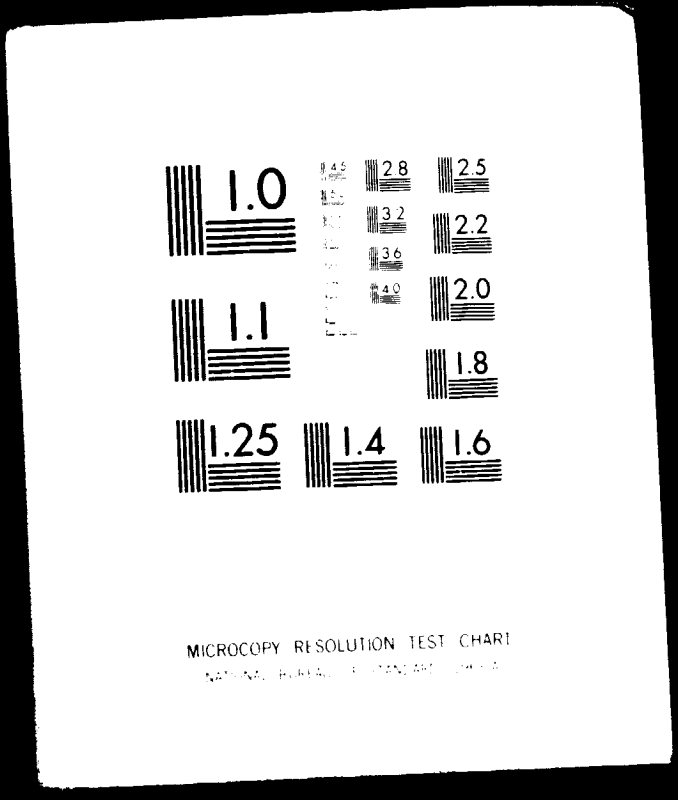
The expression for Z_o shows that the closed-loop output impedance is equal to the open-loop output impedance Z_{eo} divided by the feedback factor $1 + T$, and likewise, the expression for F shows that the closed-loop line transmission function is equal to the corresponding open-loop function H_e/μ divided by $1 + T$, both of which results are in accordance with the elementary properties of feedback.

The general model in Fig. 5.2 and expressions (5.2) through (5.5) constitute the basic representation of the switching-mode regulator operating in the continuous conduction mode and can be successfully used for both analytical or computer aided design of switching regulators.

Let us now discuss input properties represented by (5.5) in more details.

5.3 Input properties of switching regulators

The closed-loop input admittance $1/Z_i$ consists of two components as seen from (5.5). At dc and low frequencies where the loop gain T is large, the first component dominates and $Z_i \approx -\mu^2 R f_1(s)$, hence it is a negative impedance. However, above loop gain crossover where the loop gain T falls substantially below unity, the second component dominates and $Z_i \approx \mu^2 Z_{ei}$. However, from Fig. 5.2 this is the same as the open-loop input impedance, the result which should be expected when the loop gain is negligibly small. The complete



expression (5.5) shows then how the input impedance changes from negative at low frequencies to positive at high frequencies as the loop gain falls below unity.

The result that the input impedance at low frequencies is negative may seem at first surprising. Nevertheless it is inherent in switching regulators, as the following simplified analysis will demonstrate.

At low frequencies where the loop gain T is high, the feedback action maintains constant output voltage, and hence constant output power by varying duty ratio D (consequently gain $\mu(D)$), even if the input voltage V_g varies. It follows that if V_g increases, I_g must decrease since the input power also remains constant (under simplifying 100% efficiency assumption). Consequently, the regulator exhibits a negative incremental input resistance R_i given by

$$R_i = \frac{dV_g}{dI_g} = \frac{d}{dI_g}\frac{P}{I_g} = -\frac{P}{I_g^2} = -\frac{V_g}{I_g} = -\mu^2\frac{V}{I} = -\mu^2 R \qquad (5.6)$$

This is the low frequency value of the regulator input impedance Z_i given in (5.5). For example, for the boost converter example of Fig. 5.1 the closed-loop incremental resistance becomes:

$$R_i = -D'^2 R = -\left(\frac{V_g}{V}\right)^2 R \qquad (5.7)$$

while the open-loop low frequency input resistance R_{in} is:

$$R_{in} = D'^2 R = \left(\frac{V_g}{V}\right)^2 R \qquad (5.8)$$

It will be interesting later, in Part II, to compare these particular results (5.7) and (5.8) as well as the above general result (5.5) with corresponding expressions for the switching-mode regulator operating in the discontinuous conduction mode.

Another interesting interpretation of the negative input impedance at low frequency will perhaps even more illuminate the need for the presence of the current generator in the model of Fig. 5.2. When the regulator is driven by an ac voltage $\hat{v}_g$, the high loop gain at low frequencies will force the ac voltage $\hat{v}$ at the output to be vanishingly small by appropriate adjustment of the ac duty ratio $\hat{d}$; since $\hat{v}$ is the output of the filter, the voltage at the filter input and also the voltage across the current generator, is therefore vanishingly small; hence the impedance Z_i seen by the driving source $\hat{v}_g$ is simply the ratio of the voltage and current generators

$$Z_i = -\frac{e_c(s)}{j_c(s)} = -\mu^2 R \frac{f_1(s)}{f_2(s)} \qquad (5.9)$$

which is the same at low frequencies as expression (5.6) since $f_1(0) \equiv f_2(0) \equiv 1$.

As a conclusion, the regulator negative input resistance R_i in combination with the input filter can under certain conditions constitute a negative resistance oscillator, and is the origin of the system potential instability. The problem of how properly to design the input filter and to avoid performance degradation and/or stability problems is treated and solved in detail in [7]. It has been discussed here merely to demonstrate the completeness of the canonical circuit model developed in previous chapters.

PART II

Discontinuous Conduction Mode

CHAPTER 6

REVIEW OF THE NEW STATE-SPACE MODELLING TECHNIQUE IN THE DISCONTINUOUS CONDUCTION MODE

The development in Part II to a large extent resembles the same procedural order of exposition followed in Part I. This is justified for two very good reasons. First, since the procedure for modelling in discontinuous conduction mode is viewed as a special case of that applied in Part I for continuous conduction mode (provided the state-space averaging step of Part I is properly generalized to include three or more structural changes within each switching period as shown in Appendix D), the additional requirements imposed here will be immediately recognized and easy to follow in the exposition consistent with that of Part I. Second, this parallelism facilitates a direct comparison between the two modelling procedures at a number of points. While, for example, the steps common to both methods will be immediately accepted and understood on the basis of the previous in-depth explanation in Part I, those that are different will be clearly distinguished and their significance vividly displayed. This emphasizes the fact that Part II is essentially a consistent extension of the technique in Part I specially designed to model the discontinuous conduction mode of operation of switching dc-to-dc converters.

In analogy to Chapter 2 of Part I, this chapter has also a twofold purpose: to provide an extensive overview of the complete structure of the modelling of switching converters and regulators in

the discontinuous conduction mode and yet to serve post facto, after detailed exposition in later chapters, as a quick reference and reminder. In that sense, similarly to the Flowchart of Fig. 2.1 for the continuous conduction mode, the Flowchart of Fig. 6.1 summarizes all the essential information for modelling in the discontinuous conduction mode. Again, owing to the overview feature of this chapter, it will be relatively shorter than, for example, Chapters 7 and 8 where the various paths of the modelling technique are discussed at length and illustrated on several examples corresponding to those presented in Part I.

6.1 Brief review of existing modelling techniques

Owing to the relatively more complicated nature of the converter operation in the discontinuous conduction mode, dynamic (ac small signal) models have been lacking (even though valid models for continuous conduction mode have already been obtained) until recently several approaches ([11]-[17]) have been proposed. However, while all these techniques ([11]-[17]) provide through various linearization procedures the proper linearized transfer functions (duty ratio modulation $\hat{d}$ to output voltage $\hat{v}$ and line voltage $\hat{v}_g$ to output voltage $\hat{v}$ transfer functions), they are incapable of representing the input properties of the converter, and hence fail to arrive at the complete linearized converter model. This is an entirely analogous situation to that of Part I, where these methods could not model the input properties (open-and closed-loop input impedance, for example) of the converters and regulators in

continuous conduction mode of operation, as was suggested in the previous chapter. In addition, they stay throughout modelling in the domain of equation manipulations only, and thus the useful insight which can be gained from linear circuit models (as demonstrated in Part I) is lost. Hence the primary objective of the development in Part II is to overcome all these difficulties by extending the powerful state-space averaging technique of Part I, together with its circuit model realizations, to the discontinuous conduction mode of converter operation and finally to arrive at the complete linear circuit model of various converters (like, for example, those of Fig. 1.1).

6.2 New state-space and circuit averaging methods for switching converters in the discontinuous conduction mode

The state-space and circuit averaging methods presented in Part I are now to be suitably modified to account for the discontinuous conduction mode of operation, and the results are summarized in the Flowchart of Fig. 6.1. As before for the continuous conduction mode (Flowchart of Fig. 2.1), the starting model for the switching converter (block 1 in the Flowchart of Fig. 6.1) is either in terms of the state-space description of the switched networks (as in block 1a), or in terms of linear circuit models of the switched networks (as in block 1b).

The difference, however, from the previous description (compare with the Flowchart of Fig. 2.1) is not only that now there are three different structural configurations within each switching

period, but also in the fact that instantaneous inductor current is restricted in its behavior: it starts at zero at the beginning of a switching period and falls to zero current again even before the switching period has expired (see the instantaneous inductor current waveform in block 1 of Fig. 6.1).

It is actually this second difference which clearly distinguishes the discontinuous conduction mode of operation (as also demonstrated in Chapter 1 for the buck-boost converter), while the first difference, that of having three different structural configurations, appears in a way to be merely incidental. That is, in Appendix D it is shown that the state-space averaging step of Part I can be directly extended to include "three-state" converters (converters with three structural changes within each switching period), provided such converters are operated in the continuous conduction mode, and any restrictions on state-space variables (inductor currents and capacitor voltages) are avoided. Therefore, our objective in modelling converters operating in the discontinuous conduction mode (and exhibiting "three state" configuration behavior) becomes that of supplementing this generalized state-space averaging step for "three state" converters by additional constraints which reflect the special behavior of one of the state variables, the inductor current. Hence the switching-mode converter operating in the discontinuous conduction mode (and having three structural changes) may be viewed as a special case of the ordinary "three-state" converters which are free from any restrictions on state-

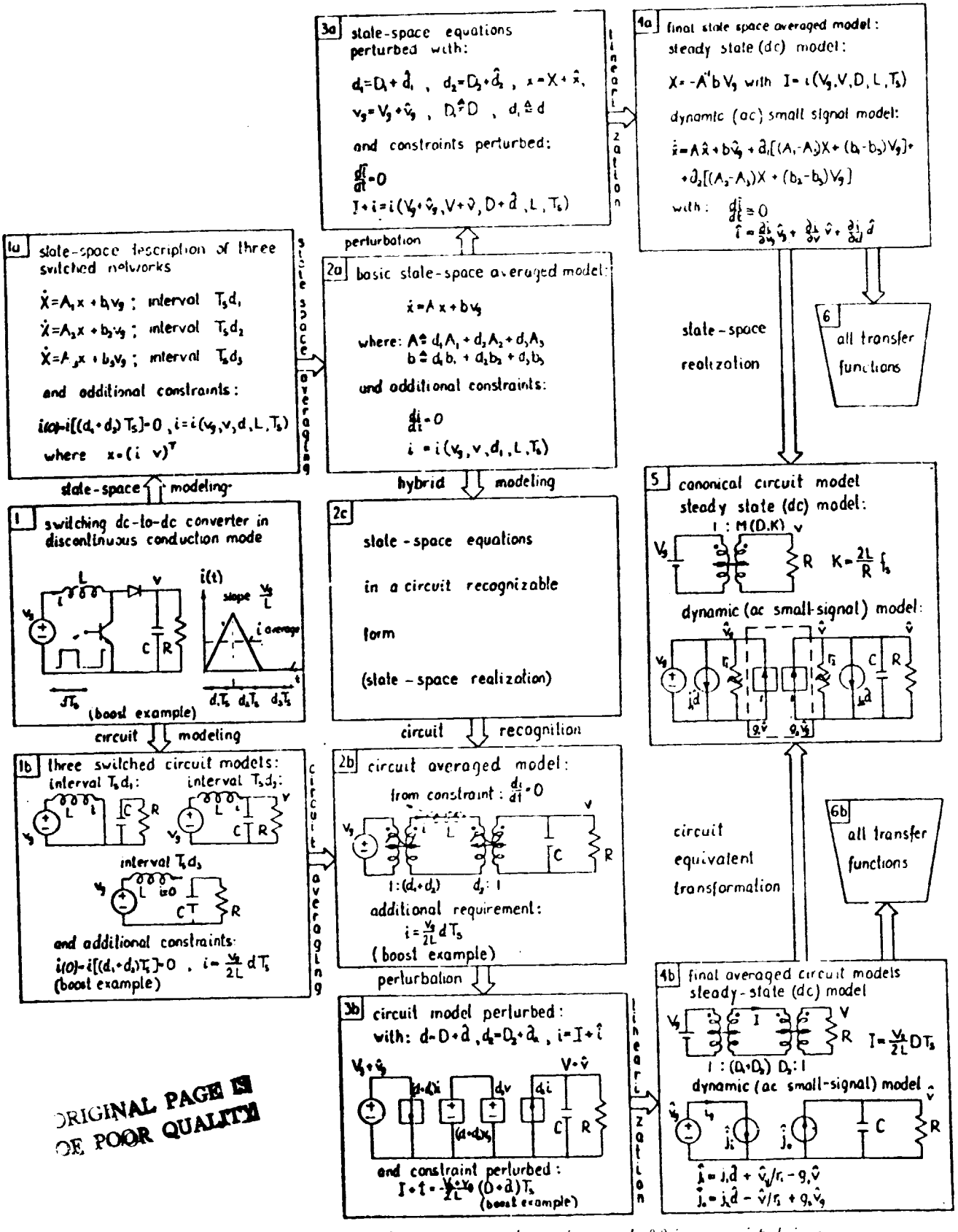


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Fig. 6.1 Flowchart of averaging approaches in modelling switching dc-to-dc converters in the discontinuous conduction mode. Path a: general state-space modelling; Path b: circuit transformation method.

variables. Thus the primary goal of this chapter (and for the whole of Part II) is properly to determine these additional constraints and to find how they propagate through various paths of the modelling (such as paths a and b on the Flowchart of Fig. 6.1).

From the Flowchart of Fig. 6.1 it is immediately clear that path a follows a development strictly in terms of state-space equations, the state-space averaged modelling technique, while the other path b proceeds in terms of circuit models, circuit averaged modelling. Moreover, as before for the continuous conduction mode, along path a the general equations (through general matrices A_1, A_2, A_3 and vectors b_1, b_2 and b_3) are retained to emphasize the fact that the outlined procedure is applicable to any "three-state" converter operating in the discontinuous conduction mode, while along path b a particular example of the boost converter is followed, owing to the requirement for the specific converter topology along that path. Specifically, for the boost power stage, $A_1 = A_3 \neq A_2$ are 2 x 2 matrices, and $b_1 = b_2 \neq 0$, $b_3 = 0$ are vectors. This example will be later pursued in detail along both paths.

We now follow path a more closely. The crucial step is made in going from block 1a to 2a in that the original description through three state-space equations (block 1a) is substituted by a single state-space averaged model (block 2a). This is justified as follows. In Chapter 1 it was demonstrated that the fundamental performance requirement of switching converters (negligible switching ripple) results in natural frequencies ω_α and f_c much lower than the switching frequency f_s. This, in turn, leads in Appendices A through D to the generalized state-space averaging step. So far

this would be the same averaging step as applied to any ordinary "three state" switching converter. However, as indicated before, the inductor current i does not behave as a true state-space variable in the discontinuous conduction mode since it does not have free boundary conditions (but fixed at zero) which is shown to lead to the following constraint:

$$\frac{di}{dt} \equiv 0 \tag{6.1}$$

This immediately reduces by one the order of the basic state-space averaged model (block 2a), since one of the dynamic equations (that for inductor current) reduces to a static equation. In addition to this, an expression describing the average inductor current i can be found directly from the converter itself (block 1) and becomes the second constraint, termed perturbation equation I, which is

$$i = i(v_g, v, d, L, T_s) \tag{6.2}$$

Thus, the two additional constraints (6.1) and (6.2), together with the generalized state-space averaging step, completely determine the converter model in the discontinuous conduction mode. It remains only to apply the standard perturbation techniques (block 3a) and (on the basis of the small-signal assumption) the linearization techniques to both state-space averaged equations and the perturbation equation of block 2a in order to arrive at the final state-space averaged model (block 4a). This model gives separately both dc and ac small-signal descriptions through general matrices A_1, A_2, A_3 and vectors b_1, b_2, b_3 of the starting switched models (block 1a) and constraints corresponding to those of (6.1) and (6.2).

Naturally, as was done before for the continuous conduction mode (compare Flowchart of Fig. 2.1 for example), we can now proceed from the basic state-space averaged model (block 2a) via hybrid modelling and circuit recognition (block 2c) to arrive at the very useful circuit realization (block 2b). Note, however, that now the constraint (6.1) effectively leads to shorting the inductance L in the circuit model since $v_L = L\, di/dt = 0$. This, for the particular boost circuit example, reduces the circuit to first order. The other constraint (6.2) is also easily specified (see additional constraint in block 2b) with the help of the inductor current waveform (block 1). The same circuit model (block 2b) could, however, be obtained directly from the switched circuit models (block 1b), by following the circuit averaging path, provided the circuit averaging step for "three-state" converters is supplemented by the aforementioned equivalents of the constraints (6.1) and (6.2). Again, the remaining circuit perturbation (block 3b) and circuit linearization steps are straightforward and result in the final circuit averaged models (block 4b) separately for dc and ac small-signal. As seen from block 4b, the dc part of the perturbation equation, current I, together with the dc circuit model, completely determines the dc conditions, while its ac part $\hat{i}$ contributes to the final ac circuit averaged model.

Finally, both models (block 4a or 4b) can be used to determine the transfer functions of interest: line voltage variation $\hat{v}_g$ and duty ratio modulation $\hat{d}$ to output voltage $\hat{v}$ (blocks 6a and 6b respectively).

6.3 New canonical circuit model for discontinuous conduction mode

As for the continuous conduction mode, the culmination of the modelling is again a canonical circuit model (block 5 of Fig. 6.1), whose fixed topology (though different from the one for continuous conduction mode) has all the features necessary to present a complete circuit model. However, this fixed topology of the model for discontinuous conduction mode came merely as a by-product, since for the three converters of Fig. 1.1 (buck, boost, and buck-boost) the ac small-signal models all resulted in the fixed topological structure of the model in block 4b of Fig. 6.1 without any need for equivalent circuit or other transformations. It does not appear that this canonical circuit topology could be directly extended to some arbitrary converter. Even though this canonical circuit model is not so general as that for two-state converters (Part I), a useful comparison between the two canonical circuit topologies can be made (at least for the common converters of Fig. 1.1 in both operating modes).

While in the continuous conduction mode the effect of duty ratio modulation $\hat{d}$ was represented by voltage and current duty ratio dependent generators at the input port (hence properly representing negative closed-loop input impedance at low frequencies as shown in Chapter 5), here in discontinuous conduction mode there are two duty ratio dependent current generators, one in the input circuit (again, properly to model converter input properties as shown later in Chapter 9), and the other in the output circuit to generate the duty ratio $\hat{d}$ to output transfer function.

The salient feature of the canonical circuit model in block 5 of the Flowchart in Fig. 6.1 is that both transfer functions are obtained using only the output port of the complete canonical circuit model, unlike the situation for continuous conduction mode (Part I), where the complete circuit model was necessary to determine them. This is also why other methods which properly represent the transfer functions in discontinuous conduction mode ([11]-[17]) have completely omitted modelling of the converter input properties.

6.4 Extension to complete regulator treatment

It has already been shown in Part I how the linear model of the modulator stage can be obtained. It remains simply to incorporate the canonical circuit model (block 5 in the Flowchart of Fig. 6.1) to arrive at the linear circuit model of a closed-loop switching regulator operating in the discontinuous conduction mode.

A word of caution, however, is appropriate here. Namely, since the very nature of the operation in the discontinuous conduction mode is that the order of the system is reduced at least by one, this would definitely change the dynamics and possible compensation networks necessary for stable operation of the closed-loop regulator. Furthermore, if both conduction modes are expected to take place for the particular application, the compensation network should be designed to ensure stability of the closed-loop and acceptable transient performance for either of the two modes. Hence canonical circuit models for both continuous and discontinuous conduction mode become an invaluable tool in the proper design of

switching regulators. In addition, the comparison of the advantages and/or disadvantages between the two modes of operation become feasible and possible trade-offs between regulator performance and choice of parameters and operating conditions is clearly displayed.

In summary, the method presented in this chapter is generally applicable to any "three state" converter operating in the discontinuous conduction mode (block 4a), even though for an arbitrary converter the final circuit model (block 4b) may have different (more complicated) topology than the canonical circuit model for the three common converters (block 5). We also emphasize the fact that the methods for finding dc and ac small-signal models are consistent with each other. Namely, for both models we need only the standard state-space or circuit averaging step (depending on whether path a or b is chosen) applicable to any converter with three switched network configurations. Then to distinguish that the converter is operating in the discontinuous conduction mode, additional restrictions (6.1) and (6.2) are imposed. Now, the dc part of perturbation equation (6.2) together with the dc state-space or circuit averaged model completely determines the final dc model, while the ac part $\hat{i}$ of (6.2) helps in complete definition of the final ac small-signal state-space or circuit averaged model.

It may seem that the method outlined in this chapter holds only for the "three-state" converters in discontinuous conduction mode. This is not so, since it can be easily generalized to include more complicated schemes of discontinuous conduction mode of operation. As an illustration of this generality, consider the new class

of switching converters of Part III, the cascade connection of ordinary buck and boost converters, which could also be classified as two-inductor converters (as opposed, for example, to the converters of Fig. 1.1 which are one-inductor converters). Suppose also that the two switches are driven synchronously with the same switch duty ratio D, thus resulting in a two-state converter for continuous conduction operation. If, however, one of the two inductor currents becomes discontinuous, a three-state converter operating in the discontinuous conduction mode is obtained. But now the matrices A_1, A_2, A_3 and A would be of 4-th order (as opposed to 2-nd order for the converters of Fig. 1.1) and the final state-space or circuit averaged model would be of the 3-rd order (reduction of order by one due to discontinuity of one of the two inductor currents). Moreover, there is also the possibility that both inductor currents could become discontinuous under certain operating conditions in which case four-state converters are generated. Therefore, the generalized state-space averaging step (Appendix D) applicable to four-state converters is supplemented with additional constraints: for each discontinuous current there will be two constraints imposed analogous to (6.1) and (6.2). The immediate consequence of these constraints is that the fourth order original converter model becomes only a second-order final state-space or circuit averaged model (with two inductances effectively disappearing from the final circuit averaged model).

Despite this demonstration of the generality of the method, we will restrict ourselves in the remaining chapters of Part II to the "three-state" converters in the discontinuous conduction mode

since all the essential features of the method are present there. Likewise, in Part III and also Part IV we will consider the cascade connection of converters only in the two-state continuous conduction mode, since the emphasis of these two parts is on the intelligent choice of converter topologies rather than on the particular mode of their operation.

CHAPTER 7

STATE-SPACE AVERAGING, HYBRID MODELLING AND CIRCUIT AVERAGING IN DISCONTINUOUS CONDUCTION MODE

In this chapter various paths on the Flowchart of Fig. 6.1 are followed in detail, first with general derivation and then illustrated by examples corresponding to those of Chapter 3. The detailed exposition will follow that of Chatper 3 as much as possible in order to make direct comparison easier and also to emphasize the significant differences. But, in order to obtain clear insight into the first-order effects, and to avoid cumbersome algebraic expressions, this time throughout the presentation it is assumed that the output quantity (voltage) coincides with one of the state variables, the capacitor voltage (esr of the capacitance neglected). The same assumption was also used throughout the Flowchart of Fig. 6.1. However, if desired, this effect can be incorporated along lines similar to those already presented in Part I.

7.1 State-space averaging

In this section, the final state-space averaged model (block 4a of Fig. 6.1) is derived, first in general for any three-state switching converter in discontinuous conduction mode, and then demonstrated on the idealized boost circuit example (parasitic effects not included). Steady state (dc) conditions are obtained for this particular example and discussed in depth, including determination of the boundary between the two modes of converter operation. From the dynamic (ac small-signal) model, the two transfer functions of interest ($\hat{v}(s)/\hat{v}_g(s)$ and $\hat{v}(s)/\hat{d}(s)$) are also

determined to enable comparison with the corresponding transfer functions derived from the final circuit averaged model for the boost converter presented in Section 7.3.

Basic state-space averaged model

We first define the time-domain description of an arbitrary three-state switching converter operating in the discontinuous conduction mode with the help of Fig. 7.1, which displays the switch drive (Fig. 7.1a) and instantaneous inductor current (Fig. 7.1b) which becomes discontinuous. The definition of the three intervals $T_s d_1$, $T_s d_2$, and $T_s d_3$ (or corresponding steady-state quantities $T_s D_1$, $T_s D_2$, and $T_s D_3$) is also clearly visible on Fig. 7.1.

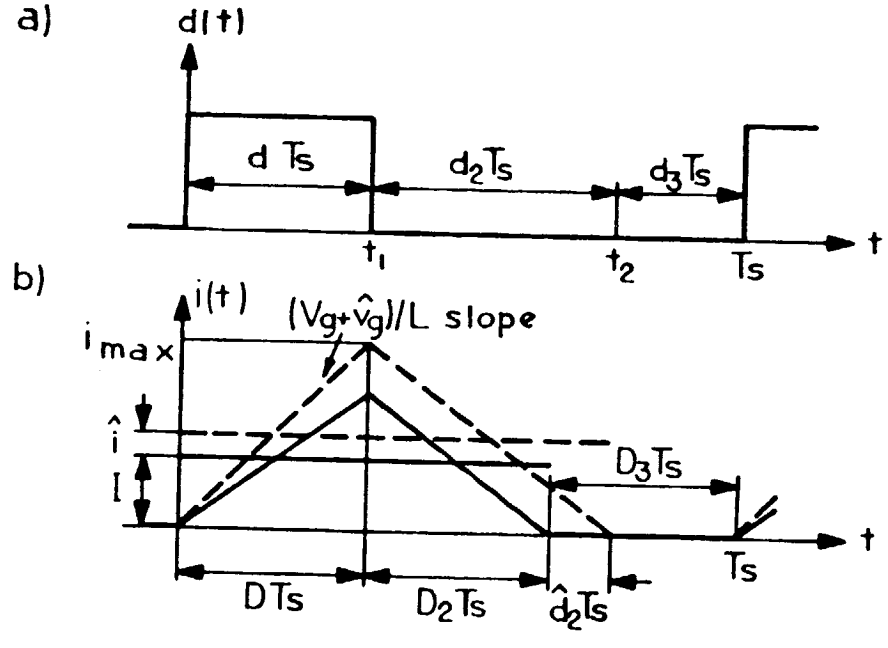


Fig. 7.1 Definition of the time intervals and perturbation quantities: a) transistor switch drive ; b) instantaneous inductor current.

As seen from Fig. 7.1, the "on" interval $T_s d_1 \equiv T_s d \equiv T_s D$ coincides with the previous "on" interval T_N in Fig. 1.2, while the "off" interval T_F of Fig. 1.2 or $T_s d' = T_s D'$ of Fig. 7.1a is now subdivided into two intervals $T_s d_2$ and $T_s d_3$ (or $T_s D_2$ and $T_s D_3$). While the first "on" interval $T_s D$ is dictated by the switch drive and is a known quantity (at least in open-loop converter usage), the second interval $T_s d_2$ (or $T_s D_2$) is as yet unknown and depends in general on both the length of the first interval and some circuit parameters, and describes how deep in the discontinuous conduction mode the converter is operating (see, for example, the simplified analysis of the buck-boost converter in discontinuous conduction mode as shown in Chapter 1). Nevertheless we assume that the interval $T_s D_2$ exists (hence discontinuous conduction follows) and leave it to the modelling procedure itself to reveal how it is actually determined.

For each of the three intervals in Fig. 7.1, there exists in general a different switched network (compare with Fig. 1.7 for the buck-boost converter example), which can be described by a corresponding state-space equation as follows:

$$\begin{aligned}
\dot{x} &= A_1 x + b_1 v_g \qquad \text{for interval } d_1 T_s, \qquad (0 \leq t \leq t_1) \\
\dot{x} &= A_2 x + b_2 v_g \qquad \text{for interval } d_2 T_s, \qquad (t_1 \leq t \leq t_2) \qquad (7.1) \\
\dot{x} &= A_3 x + b_3 v_g \qquad \text{for interval } d_3 T_s, \qquad (t_2 \leq t \leq T_s)
\end{aligned}$$

While the similar expression (3.1) for continuous conduction mode was sufficient to describe the converter, here in discontinuous

conduction mode, (7.1) does not describe the switching converter completely. Namely, the instantaneous inductor current is restricted in its evolution since from Fig. 7.1:

$$i(0) = i[(d_1+d_2)T_s] = 0 \quad \text{and} \quad i(t) \equiv 0 \text{ for } t \in [t_2, T_s] \qquad (7.2)$$

Therefore (7.1) together with (7.2) completely determine the behavior of the switching converter. However, directly from this description, even the determination of the steady-state (dc) conditions on an <u>exact</u> basis might be a very difficult (if not insurmountable) task, as was demonstrated for the simpler continuous conduction mode description (3.1) in Appendix C. Moreover, the tremendous complexity of the result may be unnecessary (compare (C.4), (C.5), (C.7) and (C.8) with the much simpler result (C.10)). In addition, the direct perturbation of (7.1) and (7.2) to obtain the dynamic response of the converter would become by an order of magnitude more difficult if not virtually impossible. Our objective then becomes, as it was in Part I for the continuous conduction mode, to replace the original converter description through three state-space equations (7.1) by a single state-space description which will very accurately represent the evolution of the state-vector at the switching instants. It is also desirable that the additional constraint (7.2) is appropriately accounted for to modify this averaging equivalent, but in such a way as to interfere the least possible with its orderly procedure.

The first task is accomplished by application of the generalized state-space averaging step for three-state converters (Appendix D) to (7.1), which results in a single state-space description

$$\dot{x} = (d_1A_1+d_2A_2+d_3A_3)x + (d_1b_1+d_2b_2+d_3b_3)v_g \qquad (7.3)$$

Note, however, that this continuous description ((7.3) and previously (3.3) for two-state converters) is a <u>continuous equivalent</u> to the originally derived approximate discrete system (see (B.8) in Appendix B). Hence the definition of derivative (B.9) from Appendix B transforms the constraint (7.2) into

$$\frac{di}{dt}(nT_s) = \frac{i(T_s) - i(0)}{T_s} = 0 \qquad (7.4)$$

It follows that the inductor current in the equivalent continuous system (7.3) <u>ceases to be a true state-space variable</u>, since according to (7.4) it has lost its dynamic properties. Nevertheless, despite the zero constraints $i(nT_s) = 0$ and $di/dt(nT_s) = 0$ for $n = 0,1,\ldots$, a line voltage perturbation $\hat{v}_g$ (as seen in Fig. 7.1b) <u>does</u> cause a perturbation of the instantaneous inductor current (shown in dotted lines on Fig. 7.1b) from its steady-state waveform (heavy line in Fig. 7.1b), which in turn results in a corresponding perturbation $\hat{v}$ of the output steady-state voltage. Note that there is also perturbation of the average inductor current i (defined in Fig. 7.1b for interval $(d_1+d_2)T_s$ when instantaneous inductor current i(t) is different from zero)

from its steady-state average current I. This is in sharp contrast to the situation in the continuous conduction mode where the average inductor current does not change under any small-signal perturbation, but rather initial and final conditions $i(0)$ and $i(T_s)$ change accordingly to accommodate perturbation. Here, $i(0)$ and $i(T_s)$ are fixed at zero, and the average inductor current is the quantity which reflects the effect of introduced perturbation.

Since the objective in modelling the dynamic performance of the converter is faithfully to represent departure from the steady-state, we introduce the average inductor current as a substitute for the "lost" state-variable (the instantaneous inductor current). But, rather than change the symbol, we assign to the same designation i this new meaning. Then from Fig. 7.1b we obtain

$$i = \frac{i_{max}}{2} = i(v_g, v, d, L, T_s) \tag{7.5}$$

and designate it perturbation equation I, for reasons which will become apparent later. Naturally, the other constraint (7.4) for this average inductor current i is maintained (as seen also from Fig. 7.1b) and we finally obtain the basic state-space averaged model for discontinuous conduction mode:

$$\dot{x} = (d_1A_1+d_2A_2+d_3A_3)x + (d_1b_1+d_2b_2+d_3b_3)v_g \tag{7.6}$$

with additional constraints

$$\frac{di}{dt} = 0 \tag{7.7}$$

$$i = i(v_g, v, d_1, L, T_s) \tag{7.8}$$

The two additional constraints (7.7) and (7.8) modify the ordinary averaged model (7.6) to account for the discontinuity of the inductor current. This model (block 2a in the Flowchart of Fig. 6.1) is the starting point for all other derivations (both state space and circuit oriented) and represents an averaged model over a single period T_s.

Note, also from (7.5) that the calculation of the average inductor current i is actually based on the assumption of the linearity of the inductor current waveform (triangular waveshape in Fig. 7.1). However, this does not pose any limitations at all, since the linearity of the inductor waveform is again a consequence of the small switching ripple requirement and therefore consistent with the same basic assumption made in the continuous conduction mode.

We now consider first the simplest possible case, determination of the basic dc conditions in the steady state regime. In the steady state all quantities become dc quantities and are denoted by capital letters, that is, $d_1 = D_1 = D$, $d_2 = D_2$, $d_3 = D_3$, $v_g = V_g$, $x = X$. The average inductor current i becomes the steady state average inductor current I (see Fig. 7.1b, for example) and the steady-state vector $X = (I \quad V \ldots)$. Since then $dX/dt \equiv 0$, the state-space equation (7.6) reduces to the linear algebraic system

$$AX + bV_g = 0 \tag{7.9}$$

where

$$\begin{aligned} A &= D_1A_1 + D_2A_2 + D_3A_3 \\ b &= D_1b_1 + D_2b_2 + D_3b_3 \end{aligned} \tag{7.10}$$

while the first constraint (7.7) is automatically satisfied and the second constraint becomes

$$I = i(V_g, V, D_1, L, T_s) \tag{7.11}$$

It is now interesting to compare these results for dc conditions ((7.9) and (7.11)) with those of Part I (3.9). For easier correlation of these results, the notation $d_1 = d$ and $D_1 = D$ henceforth will be used interchangeably. The steady state vector X is the solution of the linear system (7.9) as it was before in (3.9). Hence storage elements (L's and C's) are proportionality constants in the linear system (7.9) and it appears as though solution X of (7.9) is independent of them and dependent on dc duty ratios and resistances in the original model. However, since $D_1 + D_2 + D_3 \equiv 1$ or $D_3 = 1 - (D+D_2)$ from (7.9) and (7.10) it follows that steady state vector X is now dependent on two duty ratios D (given) and D_2 (as yet undetermined) as opposed to only D in (3.9). The additional constraint (7.11) which expresses the average steady state inductor current I in terms of circuit parameter values can now be used together with (7.9) to solve for the unknown duty ratio D_2, and hence to determine the length of the second interval D_2T_s. In general, then, D_2 is dependent on circuit parameters (such as L and T_s, for example) and hence dc conditions are also substantially dependent on switching frequency f_s and inductance L (compare with (1.4) and (1.5)). This is in sharp contrast to the continuous conduction mode (see Fig. C.2), where dc conditions were dependent on duty ratio D and resistances only.

In summary, expressions (7.9) and (7.11) completely determine the dc conditions in the discontinuous conduction mode, and at the same time help to determine the length of the second interval D_2T_s, which was unknown at the beginning of this analysis.

We now undertake to obtain the dynamic model for the line voltage variation $\hat{v}_g$ only, in order to compare it with the corresponding result (3.8) in Part I and to emphasize the significant differences. From Fig. 7.1b it becomes obvious that the superimposed variation $\hat{v}_g$ causes the perturbation of the instantaneous inductor current (dotted lines) and hence modulation of the second interval d_2T_s and the third interval d_3T_s as well. Therefore only the switch drive duty ratio d is constant (d = D) as it was also in Part I, while the other two duty ratios are modulated. After the perturbation equations

$$d = D, \qquad d_2 = D_2+\hat{d}_2, \qquad d_3 = D_3-\hat{d}_2,$$
$$v_g = V_g+\hat{v}_g, \qquad x = X+\hat{x} \qquad \text{and} \qquad i = I+\hat{i} \tag{7.12}$$

are introduced, the basic state-space averaged model given by (7.6), (7.7) and (7.8) becomes

$$\dot{\hat{x}} = [DA_1+(D_2+\hat{d}_2)A_2 + (D_3-\hat{d}_2)A_3](X+\hat{x}) + [Db_1+(D_2+\hat{d}_2)b_2 + (D_3-\hat{d}_2)b_3](V_g+\hat{v}_g) \tag{7.13}$$

with additional constraints

$$\frac{d\hat{i}}{dt} = 0 \tag{7.14}$$

$$I + \hat{i} = i(V_g+\hat{v}_g, V+\hat{v}, D, L, T_s) \tag{7.15}$$

Note that the perturbations (7.12) are now applied not only to the state-space equations (7.6) but to the constraints (7.7) and (7.8) as well. Upon the usual small-signal assumption, the second-order terms are neglected and linear state-space equations with linearized constraints (7.15) are obtained. The separation of the dc and ac models then results in the steady-state dc model as given before by (7.9) and (7.11) and the dynamic (ac small-signal) model for line variations $\hat{v}_g$ only, given by

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + \hat{d}_2[(A_2-A_3)X + (b_2-b_3)V_g] \tag{7.16}$$

subject to constraints

$$\frac{d\hat{i}}{dt} = 0 \tag{7.17}$$

$$\hat{i} = \frac{\partial i}{\partial v_g}\hat{v}_g + \frac{\partial i}{\partial v}\hat{v} \tag{7.18}$$

where A and b are as given before in (7.10).

From (7.18) it also becomes obvious why (7.5) was originally called "perturbation equation I". In addition, since $\dot{\hat{x}} = [d\hat{i}/dt\ d\hat{v}/dt\ \ldots]^T$ the introduction of constraint (7.17) into (7.16) reduces the first dynamic equation to a static one, from which the unknown modulation $\hat{d}_2$ can be determined in terms of $\hat{v}_g$ and $\hat{i}$ modulations and circuit parameters.

The dynamic state-space equation which, because of (7.17), became a static one, can now be designated "perturbation equation II", since it helps to determine the other unknown perturbation quantity $\hat{d}_2$. Together with (7.18) this uniquely defines the line transfer

function, $\hat{v}(s)/\hat{v}_g(s)$. However, owing to the presence of constraints (7.17) and (7.18) we cannot give the closed-form expression for this transfer function as we could in (3.10) for continuous conduction mode.

We turn next to the most general case and allow both modulations (line voltage variation $\hat{v}_g$ and duty ratio modulation $\hat{d}$) to occur concurrently.

Perturbation

We now suppose that the switch drive duty ratio d changes from cycle to cycle, in addition to the line voltage variation. Hence, the general perturbation equations

$$\begin{aligned} d &= D+\hat{d}, & d_2 &= D_2+\hat{d}_2, & d_3 &= D_3+\hat{d}_3, \\ v_g &= V_g+\hat{v}_g, & x &= X+\hat{x}, \quad \text{and} & i &= I+\hat{i} \end{aligned} \tag{7.19}$$

introduced into the basic-state space averaged model given by (7.6), (7.7) and (7.8) result in

$$\begin{aligned} \dot{\hat{x}} = &[(D+\hat{d})A_1 + (D_2+\hat{d}_2)A_2 + (D_3-\hat{d}-\hat{d}_2)A_3](X+\hat{x}) + \\ &+ [(D+\hat{d})b_1 + (D_2+\hat{d})b_2 + (D_3-\hat{d}-\hat{d}_2)b_3](V_g+\hat{v}_g) \end{aligned} \tag{7.20}$$

with additional constraints

$$\frac{d\hat{i}}{dt} = 0 \tag{7.21}$$

$$I + \hat{i} = i(V_g+\hat{v}_g, V+v, D+\hat{d}, L, T_s) \tag{7.22}$$

From $d + d_2 + d_3 \equiv 1$, when perturbed by (7.19), we got $D + \hat{d} + D_2 + \hat{d}_2 + D_3 + \hat{d}_3 \equiv 1$ or, since also $D + D_2 + D_3 \equiv 1$, we finally arrive at

$$\hat{d}_3 = -(\hat{d}+\hat{d}_2) \tag{7.23}$$

which was then used in (7.20).

The perturbed model given by (7.20), (7.21) and (7.22) is nonlinear owing to the presence of at least second-order terms.

Linearization and final state-space averaged model for discontinuous conduction mode

We now make the small-signal approximation, namely that the departures from the steady-state values are small compared to the steady-state values themselves:

$$\frac{\hat{v}_g}{V_g} << 1, \qquad \frac{\hat{d}}{D} << 1, \qquad \frac{\hat{d}_2}{D_2} << 1, \qquad \frac{\hat{x}}{X} << 1 \tag{7.24}$$

Using approximations (7.24) we neglect all second (or higher) order terms, and obtain once again a linear system but including duty-ratio modulation $\hat{d}$. After separating the steady-state (dc) and dynamic (ac) parts of both state-space equations (7.20) and constraints (7.21) and (7.22) we arrive at the following results for the final state-space averaged model.

Steady state (dc) model:

$$X = -A^{-1}bV_g \tag{7.25}$$

subject to constraint

$$I = i(V_g,V,D,L,T_s) \tag{7.26}$$

Dynamic (ac small-signal) model:

$$\dot{\hat{x}} = A\hat{x}+b\hat{v}_g+\hat{d}[(A_1-A_3)X+(b_1-b_3)V_g]+\hat{d}_2[(A_2-A_3)X+(b_2-b_3)V_g] \qquad (7.27)$$

subject to constraints

$$\frac{d\hat{i}}{dt} = 0 \qquad (7.28)$$

$$\hat{i} = \frac{\partial i}{\partial v_g}\hat{v}_g + \frac{\partial i}{\partial v}\hat{v} + \frac{\partial i}{\partial d}\hat{d} \qquad (7.29)$$

where A and b are as given before by (7.10). Note how duty ratio modulation $\hat{d}$ is now included in constraint (7.29).

We conclude this section with illustration of these general results on the boost converter. Both dc and ac small-signal models are then analyzed in detail and some unique insights into the operation of the boost converter in the discontinuous conduction mode are obtained. Dc conditions and the determination of the boundary of the two modes of operation are particularly thoroughly analyzed.

Example: ideal boost power stage in discontinuous conduction mode

For the ideal boost power stage of Fig. 1.1 (or Fig. 3.1 with $R_\ell = 0$, $R_c = 0$) the three switched networks in the discontinuous conduction mode of operation are shown in Fig. 7.2.

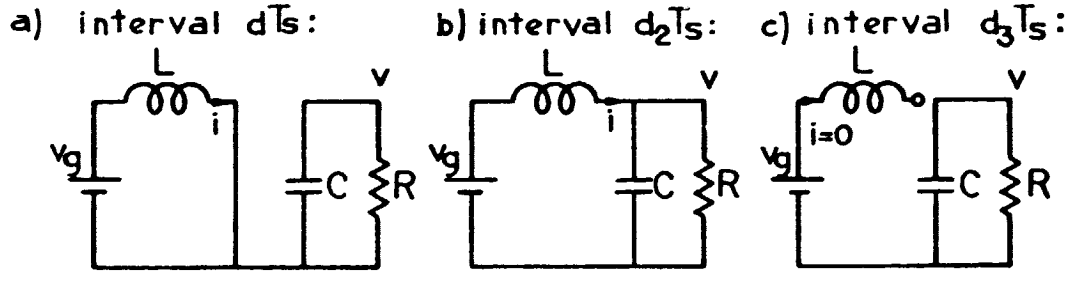


Fig. 7.2 Three switched networks of the ideal boost converter of Fig. 1.1 operating in the discontinuous conduction mode.

For the choice of state-space vector $x = (i \quad v)^T$, the state-space equations of the three linear switched networks in Fig. 7.2 become:

$$\begin{aligned} \dot{x} &= A_1 x + b_1 v_g && \text{for interval } dT_s \\ \dot{x} &= A_2 x + b_2 v_g && \text{for interval } d_2 T_2 \\ \dot{x} &= A_3 x + b_3 v_g && \text{for interval } d_3 T_s \end{aligned} \qquad (7.30)$$

where

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \tag{7.31}$$

$$b_1 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T \quad b_2 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T \quad b_3 = \begin{bmatrix} 0 & 0 \end{bmatrix}^T$$

In addition to this, perturbation equation I (7.5) is needed. However, it can easily be found from Fig. 7.2a as

$$i = \frac{i_{max}}{2} = \frac{v_g}{2L} dT_s = i(v_g, d, L, T_s) \tag{7.32}$$

The same result could have been concluded also from Fig. 7.1b, which actually represented instantaneous inductor current for the boost converter (or buck-boost converter since both have the same slope during interval dT_s).

Equations (7.31) and (7.32) contain now all that is needed to determine both dc and ac small-signal models by application of the general result, equations (7.25) through (7.29). We first analyze in greater depth the steady-state (dc) model.

Steady state (dc) model analysis

By use of (7.31) in (7.25) the following linear algebraic system results

$$\underline{A} \qquad\qquad \underline{X} \qquad\qquad \underline{b}$$

$$\begin{bmatrix} 0 & -\frac{D_2}{L} \\ \frac{D_2}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} \frac{D+D_2}{L} \\ 0 \end{bmatrix} V_g = 0 \qquad (7.33)$$

in which the quantities A, X and b are clearly identified and obtained by use of their definition (7.10). The general remark made previously about the solution of this linear algebraic system (7.33) becomes clearly visible. Storage elements (L's and C's) are indeed proportionality constants, and the solution of (7.33) is

$$\frac{V}{V_g} = 1 + \frac{D}{D_2} \qquad (7.34)$$

$$I = \frac{V}{D_2 R} \qquad (7.35)$$

Hence, the dc conditions depend only on duty ratios D and D_2 and resistance R. From (7.34) we conclude also that the boost converter has even in the discontinuous conduction mode the boosting property (dc gain $V/V_g \geq 1$), since D, D_2 are by definition positive quantities. However, the dc conditions are not quite determined since D_2 is as yet unknown. But, by use of the additional constraint (7.26), as further specified in (7.32) as

$$I = \frac{V_g D T_s}{2L} \qquad (7.36)$$

together with (7.34) and (7.35), dc conditions (and also D_2) are <u>completely</u> determined. For example, substitution of (7.36) into (7.35) results in

$$D_2 = \frac{V}{RI} = \frac{V}{R}\frac{2L}{DT_s V_g} = \frac{V}{V_g}\frac{K}{D} = \frac{MK}{D} \tag{7.37}$$

where the very important dimensionless quantity K is defined as

$$K \triangleq \frac{2L}{RT_s} \triangleq \frac{2L}{R} f_s \tag{7.38}$$

This dimensionless parameter K plays a key role in the discontinuous conduction mode since it combines uniquely all the parameters responsible for such behavior. Another quantity which will frequently appear is the dc voltage gain V/V_g, so we define also another dimensionless parameter M as

$$M \triangleq \frac{V}{V_g} \tag{7.39}$$

Finally, by use of (7.37) and (7.39) in yet unused dc relation (7.34), the quadratic equation for dc gain M is obtained

$$M^2 - M - D^2/K = 0 \tag{7.40}$$

Since from (7.34) the dc gain M is positive, only the positive solution of (7.40) is meaningful and we obtain

$$M = \frac{1 + \sqrt{1 + 4D^2/K}}{2} \tag{7.41}$$

Finally, the substitution of (7.41) in (7.37) determines the previously unknown duty ratio D_2 as

$$D_2 = \frac{K}{D}\frac{1 + \sqrt{1 + 4D^2/K}}{2} \tag{7.42}$$

Hence, we have succeeded in expressing, through (7.41) and (7.42), two important quantities, the dc gain M and duty ratio D_2, in terms of the driving condition (duty ratio D of the transistor switch), and the single dimensionless quantity K which solely reflects the

effect of circuit parameter values (L and R) and the other operating condition, the switching frequency f_s, upon the dc conditions in the discontinuous conduction mode. If desired, the remaining dc quantity, the steady-state average inductor current I, may be found in terms of D and K by use of (7.42) in (7.35).

All these expressions (7.41), (7.42), and (7.35) are very useful in predicting the dc conditions when the switching converter is used alone, that is in an open-loop fashion, since then the duty ratio D is given (independently generated) and the constant K may be calculated from element values with use of (7.38). However, if the converter is used in a closed-loop switching regulator (such as, for example, those of Fig. 1.10 or Fig. 5.1), the output dc voltage V is predetermined by the choice of the reference voltage and kept constant regardless of any variation of input dc voltage V_g, by appropriate self-adjustment of the dc duty ratio D (internally generated) in a negative feedback manner. Hence in closed-loop operation, D and D_2 become dependent on the external dc gain M and the dimensionless parameter K. These dependences can easily be found from (7.41) and (7.42) to get, for closed-loop consideration:

$$D = \sqrt{KM(M-1)} \tag{7.43}$$

$$D_2 = \sqrt{\frac{KM}{M-1}} \tag{7.44}$$

Hence, (7.41) and (7.42) conveniently determine dc quantities for open-loop considerations, while (7.43) and (7.44) are likewise useful for closed-loop considerations.

It is now very interesting to compare the open-loop dc gain in the discontinuous conduction mode given by (7.41) with the corresponding dc gain in the continuous conduction mode, which, for ideal boost converter (see for example (3.20)), is

$$M = \frac{1}{1 - D} \tag{7.45}$$

Hence, the ideal dc gain (7.45) is dependent on duty ratio D only and not on circuit parameters (such as L, R) or switching frequency f_s. Even the exact dc analysis of Appendix C (with parasitics $R_\ell \neq 0$, $R_c \neq 0$ also included) demonstrated in a very convincing manner (see, for example, Fig. C.2) that for all practical purposes (small switching ripple) dc gain is independent of switching frequency f_s (and L, C, R as well) in the continuous conduction mode. In sharp contrast to this, the dc gain M in the discontinuous conduction mode (7.41) is dependent also on K in addition to D and hence is a strong function of switching frequency f_s, inductance L, and load R. Nevertheless, when the converter is used in this mode in a closed-loop regulator, the self-correcting feature of the duty ratio D would compensate any possible changes of load R or switching frequency f_s and still keep output voltage relatively constant.

Another question naturally arises in comparison of the two dc gains: when do we calculate dc gain from one (7.41) or the other formula (7.45) or, what is the criterion to determine in which of the two modes (continuous or discontinuous) the converter is operating? The answer is provided easily with reference to Fig. 7.1. When the second interval D_2T_s is smaller than interval $(1-D)T_s$, the converter is

operating in the discontinuous conduction mode, and in continuous otherwise, so the criterion becomes

continuous conduction mode

$$D_2 > 1 - D \tag{7.46}$$

discontinuous conduction mode

$$D_2 < 1 - D \tag{7.47}$$

To obtain a convenient quantitative measure we find, first, what happens exactly on the boundary between the two modes of converter operation, or

boundary between two conduction modes

$$D_2 = 1 - D \tag{7.48}$$

By use of (7.42) in (7.48), the equation to determine the critical value of parameter K, that is, K_{crit} for which this happens, is

$$\sqrt{K_{crit}^2 + 4K_{crit}D^2} = 2DD' - K_{crit} \tag{7.49}$$

from which

$$K_{crit} = DD'^2 \tag{7.50}$$

The solution (7.50) is the proper solution of (7.49) since $2DD' - K_{crit} = 2DD' - DD'^2 = 2DD'(2-D') = 2DD'(1+D)$ is always positive regardless of D, resulting in a proper positive right hand side of (7.49). With this, the criteria (7.46) and (7.47) for determination of the operating mode become

continuous conduction mode $K > K_{crit}$ (7.51)

discontinuous conduction mode $K < K_{crit}$ (7.52)

boundary between two conduction modes $K = K_{crit}$ (7.53)

where K, as given before by (7.38), is a function of parameters L, R, and f_s, while K_{crit} is a function of the duty ratio D only.

We now investigate how these criteria, (7.51) through (7.53), behave throughout the duty ratio range D ϵ[0,1]. To facilitate this insight, K_{crit} is plotted as a function of duty ratio D in Fig. 7.3a.

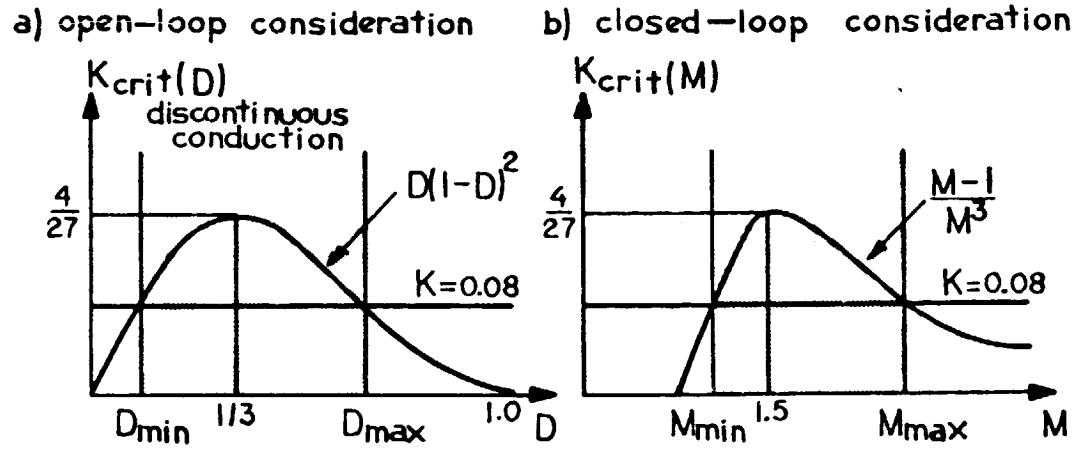


Fig. 7.3 Determination of the operating mode (continuous or discontinuous) for the ideal boost converter of Fig. 1.1.

As seen in Fig. 7.3a, $K_{crit}(D)$ has a maximum of 4/27 at D = 1/3. This now enables a very important conclusion about operating mode to be made. Namely, if the parameters L, R, and f_s are such that the computed parameter K is greater than 4/27, expression (7.51) is satisfied

regardless of duty ratio D. Hence for $K > 4/27$ the converter always operates in the continuous conduction mode, no matter what the operating condition (duty ratio D) is. However, if parameters L, R, and f_s are such that $K < 4/27 \sim 0.15$ the situation becomes as shown in Fig. 7.3a, where the particular example of $K = 0.08 < 0.15$ was chosen. For a certain range of duty ratio D, that is $D_{min} < D < D_{max}$ (as shown by the shaded area in Fig. 7.3a), the condition (7.52) is satisfied and the converter operates in the discontinuous conduction mode, while for the remaining portions of the operating range ($0 < D < D_{min}$ and $D_{max} < D < 1.0$) it again operates in the continuous conduction mode, since then inequality (7.51) holds.

This discussion has been in terms of open-loop considerations, when duty ratio D is given and externally controlled. However, as before for dc conditions, it is desirable to have the boundary condition (7.50) in terms of the dc gain M, which is a more suitable quantity for the closed-loop considerations. This can easily be done since the dc gain M is continuous across the boundary (as seen by use of (7.48) in (7.34) resulting in (7.45)), and thus substitution $D = (M-1)/M$ in (7.50) gives

$$K_{crit} = \frac{M-1}{M^3} \tag{7.54}$$

This function $K_{crit}(M)$ is plotted in Fig. 7.3b, and a similar discussion applies. However, now the maximum of $K_{crit}(M)$ of 4/27 is obtained for gain $M = 1.5$. As before, for $K < 4/27$, the converter is in the

discontinuous conduction mode, but now for dc gain M in the range $M_{min} < M < M_{max}$ as shown by the shaded area in Fig. 7.3b. This reveals a potentially serious problem if the boost regulator were designed (and compensated) to operate in the discontinuous conduction mode only. Namely, during the initial turn-on process, the output voltage starts from zero, and the converter would have to pass through the continuous conduction region <u>first</u> (for $1 < M < M_{min}$), before coming to the discontinuous conduction region (shaded area in Fig. 7.3b). This would suggest possible stability problems, if the closed-loop was not compensated to assure <u>stable</u> operation in the continuous conduction mode as well.

From the standpoint of the dc gains (as a function of duty ratio D), the situation corresponding to that of Fig. 7.3 is shown in Fig. 7.4 for some $K < 4/27$.

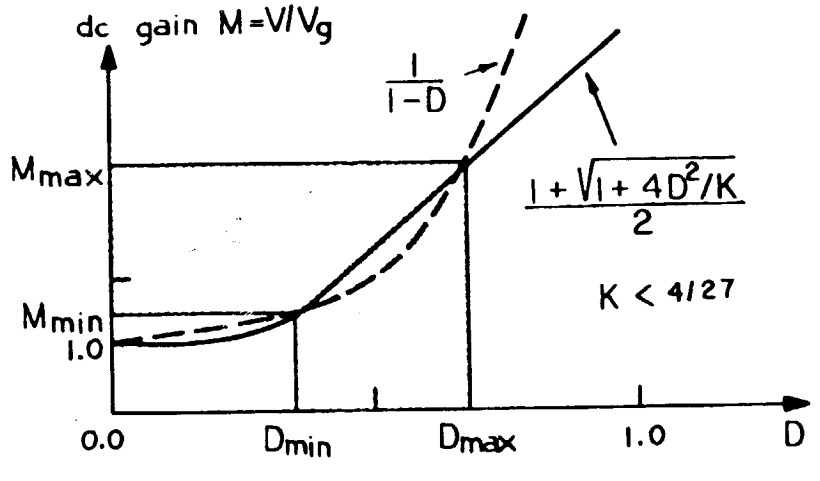


Fig. 7.4 Boost converter dc voltage gains in continuous and discontinuous conduction modes as a function of duty ratio D.

From the dc gains for both conduction modes shown in Fig. 7.4, it becomes obvious that the actual dc gain will follow the larger of the two gains, thus the mode of operation will change accordingly as the duty ratio changes from 0 to 1. Also in the close vicinity of gain M = 1 ($1 \leq M \leq M_{min}$), the converter is always operating in the continuous conduction mode. Thus, the problem of having, for example, D_2 infinite when M→1 from (7.44) is only a fictitious one, since (7.44) is for the discontinuous conduction mode and hence not applicable in the vicinity of gain M=1.

We conclude this dc analysis with some numerical examples and related quantitative and qualitative significance of the dimensionless parameter K. For example, for the set of parameters L = 880μH, R = 220Ω and f_s = 20kHz, we compute $K = 2Lf_s/R = 0.16$. Therefore, since K = 0.16 > 4/27, the converter will with this set of parameters always operate in the continuous conduction mode. However if, for example, the switching frequency is reduced to f_s= 10 kHz, this results in K 0.08 < 4/27 and some range of discontinuous conduction operation should be expected (see Figs. 7.3 and 7.4). Therefore, the reduction of parameter K below 4/27 causes this transition. From the definition of K in (7.38) this reduction and change to the discontinuous conduction mode is qualitatively achieved by three means: increase of load R, decrease of the inductance L or switching frequency f_s. There is also a fourth way to enter the discontinuous conduction mode, and that is to change the operating condition, the duty ratio D, as illustrated in Fig. 7.3 and Fig. 7.4, but only if the condition K < 4/27 is met.

Very often, however, out of all these four possibilities, one is mostly interested in how the change of load R affects the operating mode. Namely, the parameters L and f_s are usually design parameters whose choice may depend on the size and efficiency requirements of the converter or regulator. On the other hand, the range of variation of duty ratio D, or equivalently gain M, is a design requirement in a closed-loop implementation since the output voltage V is maintained constant against the range of variation of input voltage V_g (hence range of $M = V/V_g$) by the action of negative feedback. The load R also can have a wide range of change depending on the user of the regulator, and is often out of the designer's control. Hence, determination of the converter operating mode with respect to changes of load R becomes important. This can be easily accomplished by finding an equivalent of (7.50) and (7.54) respectively, as

$$R_{crit} = \frac{1}{DD'^2} R_{nom} \tag{7.55}$$

$$R_{crit} = \frac{M^3}{M-1} R_{nom} \tag{7.56}$$

where R_{nom} is a design parameter defined by

$$R_{nom} \triangleq 2Lf_s \tag{7.57}$$

The criteria for determination of the operating mode, (7.51), (7.52), and (7.53), then become

<u>continuous conduction mode</u>

$$R < R_{crit} \tag{7.58}$$

discontinuous conduction mode

$$R > R_{crit} \tag{7.59}$$

boundary between two modes

$$R = R_{crit} \tag{7.60}$$

Let us now illustrate this on a numerical example. For L = 880μF, f_s = 20kHz we calculate R_{nom} = 35.2Ω. By the same argument as before (see Figs. 7.3 and 7.4, for example), the converter will always operate in the continuous conduction mode if

$$R < \frac{27}{4} R_{nom} \tag{7.61}$$

or for the given numerical example for R < 238Ω. When R > 238Ω there will be a range of gain M (see Fig. 7.4) for which the converter operates in the discontinuous conduction mode.

This concludes the extensive dc analysis and we now turn to the dynamic (ac small-signal) model analysis of this ideal boost converter example.

Dynamic (ac small-signal) model analysis

Before we apply the general result to this ideal boost converter example, let us first put the constraint (7.32) into a more suitable form by using the steady-state average inductor current I of (7.36) to get

$$i = \frac{v_g dT_s}{2L} = \frac{v_g d}{V_g D} I \tag{7.62}$$

By use of perturbation equation (7.62), model description (7.31) and

definition (7.10) in the general result given by (7.27) through (7.29), we obtain

dynamic (ac small-signal) model

$$\begin{bmatrix} \frac{d\hat{i}}{dt} \\ \frac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D_2}{L} \\ \frac{D_2}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \frac{D+D_2}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{V_g - V}{L} \\ \frac{I}{C} \end{bmatrix} \hat{d}_2 \quad (7.63)$$

with additional constraints

$$\frac{d\hat{i}}{dt} = 0 \quad (7.64)$$

$$\hat{i} = \frac{I}{V_g} \hat{v}_g + \frac{I}{D} \hat{d} \quad (7.65)$$

As opposed to the general result, we can now for this specific example enter the constraints (7.64) and (7.65) into dynamic model description (7.63). The introduction of (7.64) reduces the first dynamic equation in (7.63) to a static one, and after proportionality constant L is removed the dynamic model becomes

$$0 = -D_2\hat{v} + (D+D_2)\hat{v}_g + V_g\hat{d} + (V_g - V)\hat{d}_2 \quad (7.66)$$

$$C\frac{d\hat{v}}{dt} = D_2\hat{i} - \hat{v}/R + I\hat{d}_2 \quad (7.67)$$

with additional constraint (7.65). Note, however, that now the first static equation (7.66) actually determines the <u>unknown</u> modulation quantity $\hat{d}_2$ (modulation of the second interval d_2T_s as shown in Fig. 7.1, for example) in terms of the other dc and ac quantitites. In the remaining dynamic equation (7.67), besides this modulation $\hat{d}_2$ which we can now express from (7.66), current modulation $\hat{i}$ also appears. But, from the perturbation equation I (7.65)

it is also determined in terms of the known ac quantities (forced modulations $\hat{v}_g$ and $\hat{d}$). In general, both equations (7.65) and (7.66) could have both modulation quantities $\hat{i}$ and $\hat{d}_2$ for some arbitrary converter. But, they are linear algebraic equations and could be solved for $\hat{i}$ and $\hat{d}_2$ in terms of other ac quantities and then substituted in the remaining dynamic description (which could be, for some converter with more than two storage elements, higher than the first order model given by (7.67)).

Another general feature, which is in this model hidden, is that (7.66) can be considered as a consequence of the equation

$$(d+d_2)v_g = d_2 v \tag{7.68}$$

which after usual perturbation and linearization steps and subtraction of dc terms reduces to (7.66). Hence, in analogy to (7.62), equation (7.68) can now be designated perturbation equation II. The appearance of (7.68) in the modelling will become more apparent later in the hybrid modelling and circuit averaging techniques. But in any case, the unknown modulation quantities $\hat{i}$ and $\hat{d}_2$ come as the solution of two linear algebraic equations, which are essentially linearized versions of perturbation equations I and II, (7.62) and (7.68) respectively.

To complete the dynamic model description we simply substitute (7.65) and the solution of $\hat{d}_2$ from (7.66) in (7.67) to get

$$C\frac{d\hat{v}}{dt} = -\left(\frac{D_2 I}{V-V_g} + \frac{1}{R}\right)\hat{v} + \left(\frac{D_2}{V_g} + \frac{D+D_2}{V-V_g}\right)I\hat{v}_g + \left(\frac{D_2}{D} + \frac{V_g}{V-V_g}\right)I\hat{d}$$

Since this dynamic model has significance only for the closed-loop regulator, it is convenient to express all dc quantities in terms of M, K, R and output voltage V, as was explained before in the dc analysis. Hence by use of (7.43), (7.44) and (7.35) we obtain

$$C\frac{d\hat{v}}{dt} = -\frac{2M-1}{M-1}\frac{1}{R}\hat{v} + \frac{M}{M-1}\frac{2M-1}{R}\hat{v}_g + \frac{2V}{R}\frac{1}{\sqrt{KM(M-1)}}\hat{d} \qquad (7.69)$$

In (7.69) all proportionality constants would become infinite and meaningless when M = 1. However, it was explained in the dc analysis that in the vicinity and at gain M = 1, the boost converter always operates in the <u>continuous conduction</u> mode, hence a different dynamic model (that of (3.19) with $R_\ell = R_c = 0$ in Part I) applies.

It is now easy to obtain from (7.69) two transfer functions of interest

$$G_{vg} = \frac{\hat{v}(s)}{\hat{v}_g(s)} = G_{og}\frac{1}{1 + s/\omega_p}$$
$$G_{vd} = \frac{\hat{v}(s)}{\hat{d}(s)} = G_{od}\frac{1}{1 + s/\omega_p} \qquad (7.70)$$

where

$$\omega_p = \frac{2M-1}{M-1}\frac{1}{RC} \qquad (7.71)$$

and

$$G_{og} = M, \qquad G_{od} = \frac{2V}{2M-1}\sqrt{\frac{KM}{M-1}} \qquad (7.72)$$

As seen from (7.70) both transfer functions have a single pole ω_p and no zeros. This is qualitatively completely different dynamic behavior than in the continuous conduction mode (compare with the corresponding transfer functions in (3.21)) where two poles and even a right half-plane zero are obtained (for the G_{vd} transfer function

only). This in turn suggests easier compensation (even no compensation at all) and reduced stability problems if the converter as a part of switching regulator is operating consistently in the discontinuous conduction mode. But, a potential danger exists there: any significant transient changes (such as sudden change of input voltage or temporary substantial change of load R) could move the operating point to the continuous conduction region (see Fig. 7.4) and cause instability. Another problem is inherent to the discontinuous conduction mode. In addition to the output current, now the input current becomes pulsating as well (as shown in Fig. 7.1) which increases electromagnetic interference problems. Hence, a decision on the choice of operating mode becomes a complex one, depending on the particular design requirements. To facilitate that decision, we now undertake the task of developing useful circuit models of the switching converter operating in the discontinuous conduction mode.

7.2 Hybrid modelling in the discontinuous conduction mode

In analogy to Section 3.2, we demonstrate in this section how for any specific converter a useful circuit model of the basic state-space averaged model (7.6) can be found, appropriately modified by inclusion of the constraint (7.7), and supplemented by the additional constraint (7.8). In terms of the Flowchart of Fig. 6.1 we will proceed from block 2a through 2c to arrive at the circuit model in block 2b. Again this is illustrated on the same ideal boost converter example as in the previous section.

When the boost converter description (7.31) and (7.32) is applied to (7.6), (7.7) and (7.8) the following basic state-space averaged model results:

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{d_2}{L} \\ \\ \frac{d_2}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix} + \begin{bmatrix} \frac{d+d_2}{L} \\ \\ 0 \end{bmatrix} v_g \qquad (7.73)$$

with additional constraints

$$\frac{di}{dt} = 0 \qquad (7.74)$$

$$i = \frac{v_g dT_s}{2L} \qquad (7.75)$$

It now becomes clear that introduction of (7.74) into (7.73) reduces the first dynamic equation to perturbation equation II as given before by (7.68). But, instead of introducing this substitution, let us first find the circuit realization of the state-space equations (7.73) as shown in Fig. 7.5.

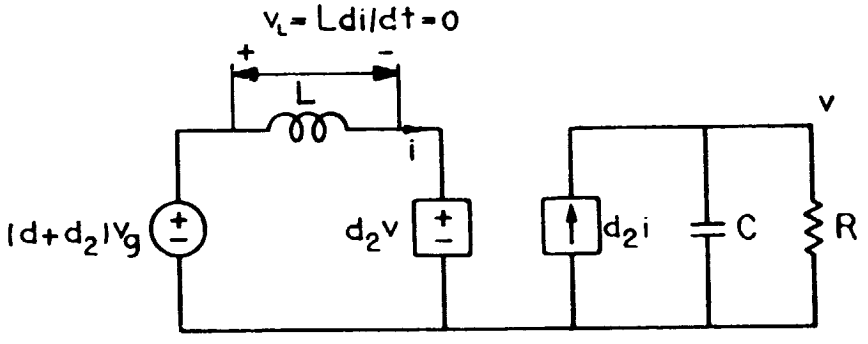


Fig. 7.5 Circuit realization of the state-space model (7.73), with constraint (7.74) also included.

The constraint (7.74) leads, in the circuit model of Fig. 7.5, to effective disappearance of the inductance L, since $v_L = Ldi/dt = 0$. The resulting equality of the two voltage generators produces again

the perturbation equation II given before by (7.68). At the same time shorting of the inductance causes reduction of system order by one, and effectively a single pole transfer function result (7.70) becomes apparent.

Let us now put the circuit of Fig. 7.5 into more elegant form, by introducing a dc and ac transformer in place of the two dependent generators in Fig. 7.5. Also, it is desirable to have source voltage v_g effectively at the input of the converter, rather than as some modified quantity as $(d+d_2)v_g$ in Fig. 7.5. However, this is easily accomplished by introduction of another dc and ac transformer at the input of the converter. In addition, the true input current into the converter becomes properly exposed as seen in the basic circuit-averaged model of Fig. 7.6. In addition to the circuit model in Fig. 7.6 we need the remaining constraint (7.75) to complete the description of the converter in discontinuous conduction mode (as also displayed in Fig. 7.6). As before, the circuit model and the additional perturbation equation are valid for both dc and ac conditions. Hence the two transformers in Fig. 7.6 are operating both at ac and dc and the appropriate symbol introduced in Part I to expose that fact is also used.

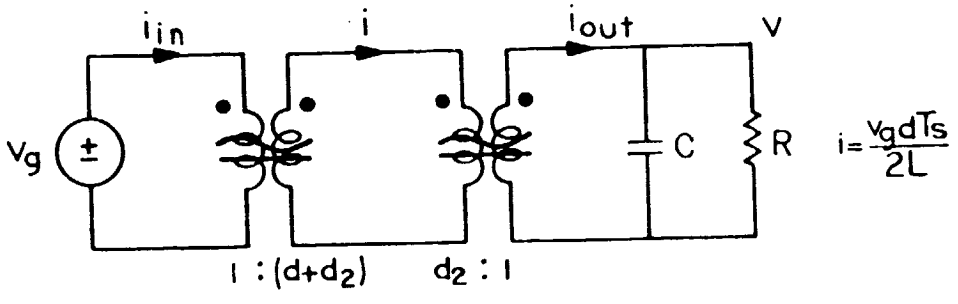


Fig. 7.6 Basic circuit averaged model for the ideal boost converter in the discontinuous conduction mode.

Following the procedure outlined in this section one can easily obtain the basic averaged circuit models of three common power stages of Fig. 1.1. These models for discontinuous conduction mode are summarized in Fig. 7.7.

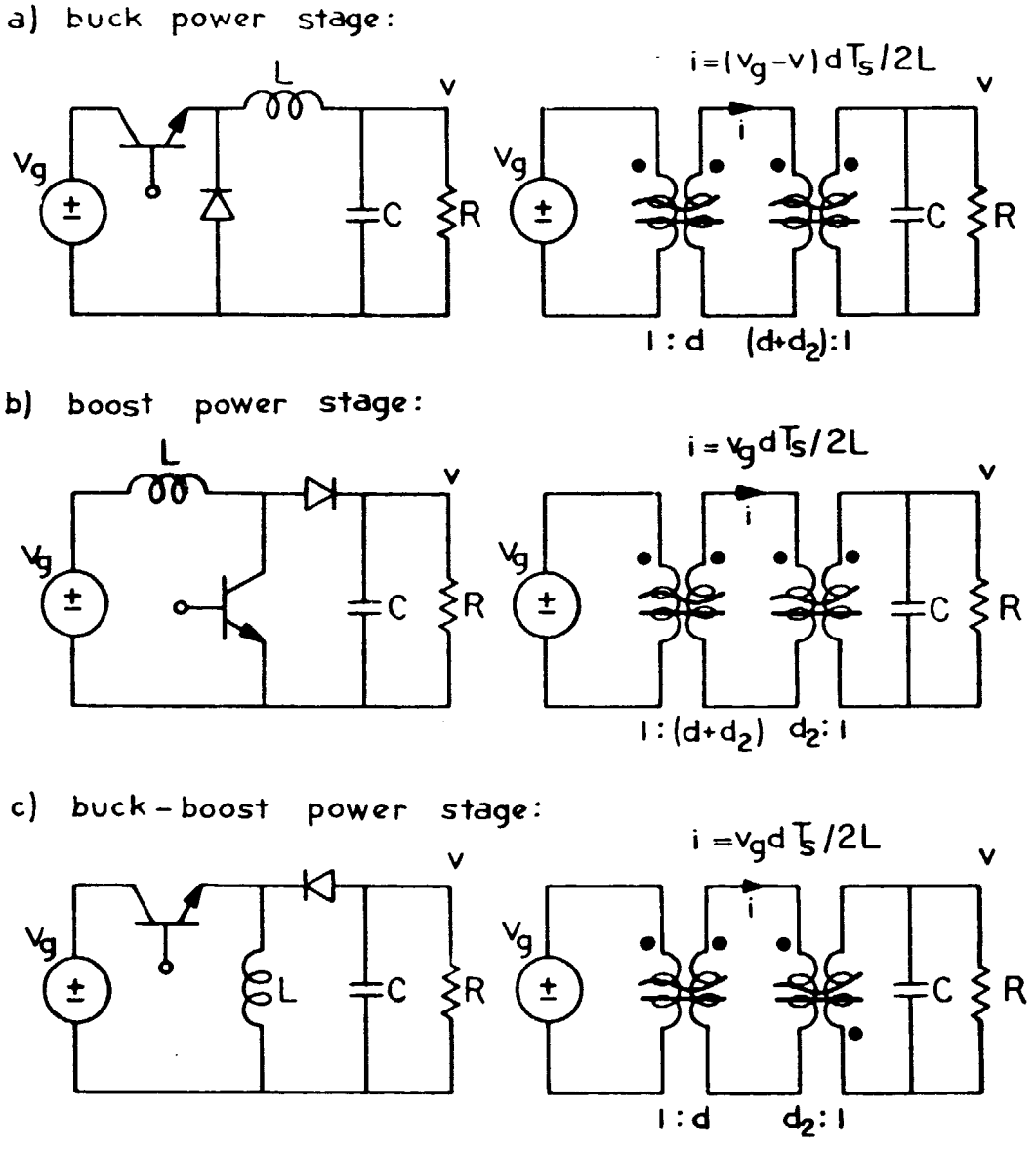


Fig. 7.7 Summary of the basic circuit averaged models for three common power stages in discontinuous conduction mode.

An interesting comparison with the corresponding summary of Fig. 3.8 can be made. While the topologies of circuit models in Fig. 3.8 are different from each other owing to the presence of inductance L, the converter models of Fig. 7.7 already have the same topology. This suggests that the circuit averaging procedure (circuit perturbation and linearization steps) presented in the next section will directly result in the fixed circuit topology of the final linearized model, without a need for any circuit equivalent transformations that were necessary in Part I in order to arrive at the canonical circuit model. This conjecture will be confirmed in the next chapter in which the canonical circuit model for discontinuous conduction mode for the three converters of Fig. 7.7 is arrived at.

Another distinction between the two circuit models is that the circuit models in Fig. 3.8 are already in a topological form which directly accounts for line voltage variation $\hat{v}_g$, while those in Fig. 7.7 are not, because of the additional constraint, the perturbation equation I, which should be also incorporated into the dynamic model as the next section will illustrate. However, Fig. 7.7 does represent dc circuit models directly (as Fig. 3.8 also did) as the next section will also verify.

7.3 Circuit averaging in the discontinuous conduction mode

In this section the alternative path b in the Flowchart of Fig. 6.1 is followed and the perturbation and linearization steps corresponding to those in state-space averaging path a are applied to the circuit model to arrive at the final circuit averaged models, separately for steady-state (dc) and dynamic (ac) response.

We continue with the same ideal boost converter example and hence use as a starting model the circuit model of Fig. 7.6. Even though that circuit model was obtained by following hybrid modelling, we emphasize also the other possibility. Namely, it could have been obtained directly by averaging the three switched circuit models of Fig. 7.2 using the standard circuit averaging technique and supplementing it by the appropriate constraints (7.74) and (7.75).

Perturbation

If the averaged circuit model of Fig. 7.6 is perturbed together with its perturbation equation I according to

$$v_g = V_g+\hat{v}_g, \quad i = I+\hat{i}, \quad d = D+\hat{d}, \quad d_2 = D_2+\hat{d}_2, \quad v = V+\hat{v} \qquad (7.76)$$

the nonlinear model of Fig. 7.8 results.

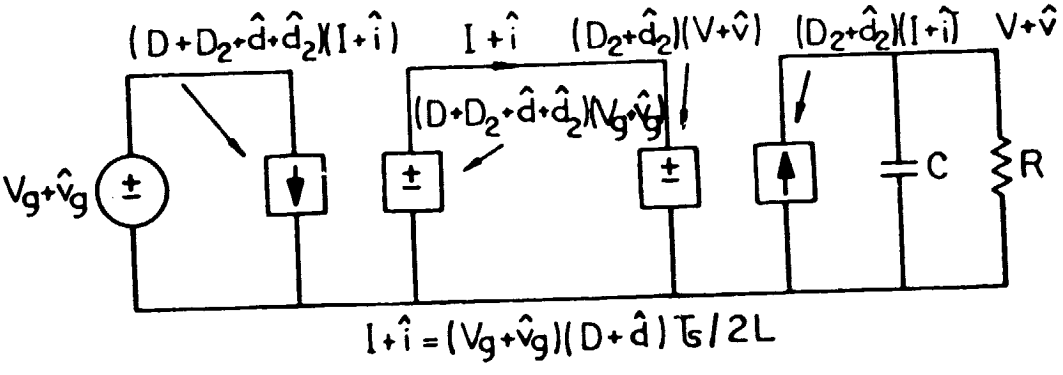


Fig. 7.8 Perturbation of the basic averaged circuit model in Fig. 7.6 results in this nonlinear circuit model.

Linearization

With the small-signal assumption on perturbation, that is

$$\hat{d} \ll D, \quad \hat{d}_2 \ll D_2, \quad \hat{i} \ll I, \quad \hat{v} \ll V, \quad \hat{v}_g \ll V_g \tag{7.77}$$

the second order terms in Fig. 7.8 can be neglected and the linearized model of Fig. 7.9 obtained.

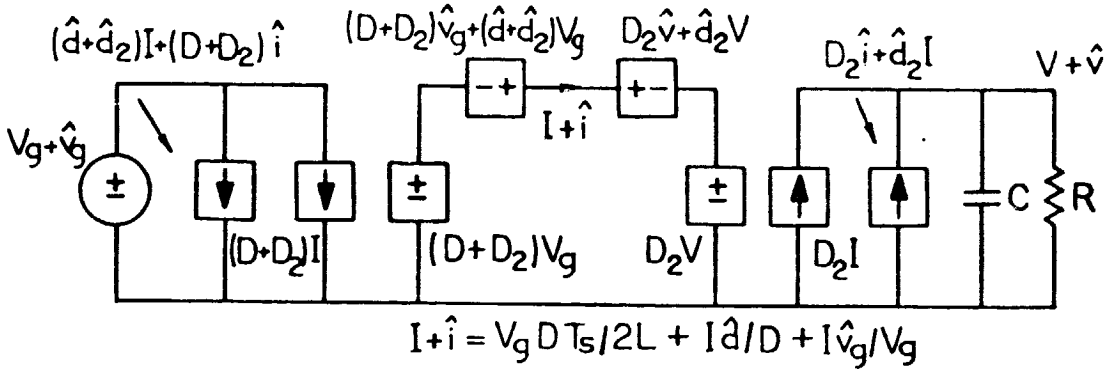


Fig. 7.9 Model of Fig. 7.8 linearized to include dc and ac small-signal models.

The circuit model in Fig. 7.9 together with the dc and ac part of the perturbation equation I (also shown in Fig. 7.9) completely determines both models. At this point, we continue to develop separately the two circuit models -- the steady-state (dc) circuit model and the dynamic (ac small-signal) model.

Steady-state (dc) circuit model

With all ac quantities set to zero, the dc circuit model is obtained directly from Fig. 7.9, and upon substitution of dc dependent generators by the dc transformer symbols, the circuit model in Fig. 7.10 results.

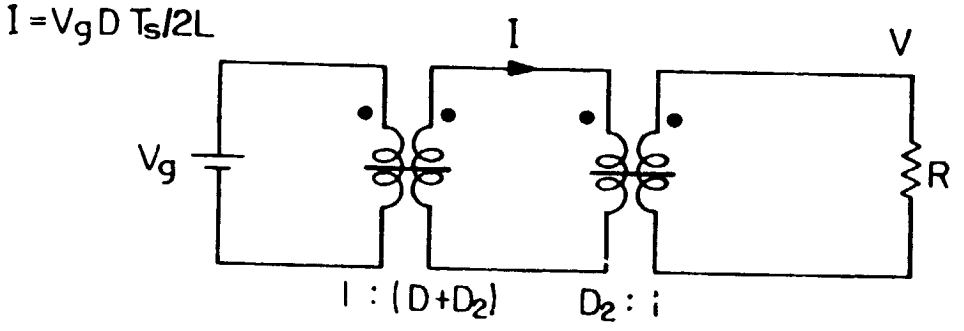


Fig. 7.10 Final dc circuit model for the boost converter in the discontinuous conduction mode.

This circuit model is also supplemented by the dc part of the perturbation equation I, which is, of course, the same as (7.36). From the circuit model in Fig. 7.10 the other two dc relations (7.34) and (7.35) are obtained. Hence the dc circuit model leads to the same dc conditions and results discussed at length in Section 7.1 on state-space averaging.

We now turn to the development of the dynamic (ac) circuit model.

Dynamic (ac) circuit model

After the steady-state (dc) quantities are subtracted from the circuit model in Fig. 7.9 (and perturbation equation as well) the ac circuit model in Fig. 7.11 is obtained.

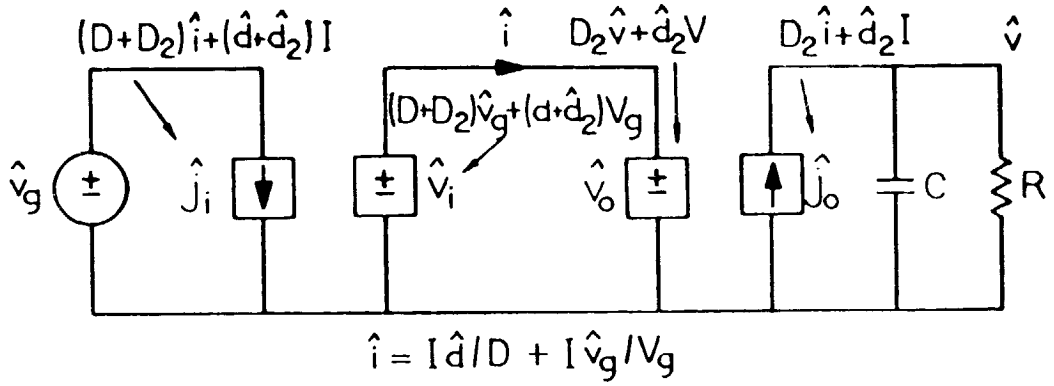


Fig. 7.11 Dynamic (ac small-signal) circuit model for the boost converter with the constraint on modulation $\hat{i}$ (perturbation equation I) not yet included in the circuit model.

From Fig. 7.11 it is obvious that the two dependent current generators are functions of two yet undetermined modulation quantities $\hat{d}_2$ and $\hat{i}$, since the other quantities are either already determined from the dc circuit model (such as D_2, I) or are known driving quantities (as D and $\hat{d}$). While the current modulation is already available through the linearized perturbation equation I (see Fig. 7.11), the other modulation quantity $\hat{d}_2$ can easily be obtained from the inside loop of Fig. 7.11. Namely, since the two voltage generators in Fig. 7.11 must be equal, we get

$$(D+D_2)\hat{v}_g + (d+\hat{d}_2)V_g = D_2\hat{v} + \hat{d}_2V \tag{7.78}$$

Note that this is the same equation as the first (static) equation (7.66) of the state-space averaged model. Now it is easy to see that (7.78) and (7.66) came out actually as a consequence of the perturbation and linearization steps applied to the perturbation equation II (7.68), since the voltage generators in Fig. 7.11 resulted from the perturbation and linearization of the voltage generators in Fig. 7.5, which have been shown to be equal for discontinuous conduction mode

(owing to di/dt = 0 constraint).

The equation (7.78) can now be solved for the unknown modulation $\hat{d}_2$ and, together with the perturbation equation defining $\hat{i}$, determines the two current generators in terms of the known modulation quantities as follows:

$$\hat{j}_i = (\hat{d}+\hat{d}_2)I + (D+D_2)\hat{i} = \frac{2VI}{V-V_g}\hat{d} + \frac{V}{V_g}\frac{(D+D_2)I}{V-V_g}\hat{v}_g - \frac{D_2 I}{V-V_g}\hat{v} \qquad (7.79)$$

$$\hat{j}_o = \hat{d}_2 I + D_2\hat{i} = \frac{2V_g I}{V-V_g}\hat{d} + \frac{V}{V_g}\frac{2V-V_g}{V-V_g}\frac{1}{R}\hat{v}_g - \frac{V}{V-V_g}\frac{1}{R}\hat{v} \qquad (7.80)$$

Since the converter dynamic model is solely used in closed-loop regulator applications, we conveniently express all dc quantities in terms of M, K, R and output regulated voltage V (as explained before) to arrive at

$$\hat{j}_i = \frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}\hat{d} + \frac{M^3}{M-1}\frac{1}{R}\hat{v}_g - \frac{M}{M-1}\frac{1}{R}\hat{v} \qquad (7.81)$$

$$\hat{j}_o = \frac{2V}{R}\frac{1}{\sqrt{KM(M-1)}}\hat{d} + \frac{M(2M-1)}{M-1}\frac{1}{R}\hat{v}_g - \frac{M}{M-1}\frac{1}{R}\hat{v} \qquad (7.82)$$

By use of (7.81) and (7.82) in the circuit model of Fig. 7.11, the circuit model in Fig. 7.12 is generated.

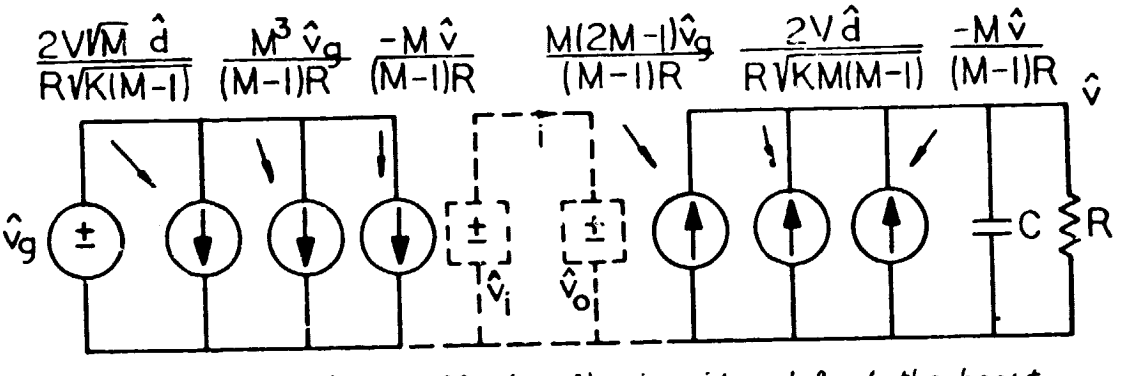


Fig. 7.12 Dynamic (ac small-signal) circuit model of the boost converter with perturbation equation I (for modulation $\hat{i}$) and perturbation equation II (equality of the voltage generators v_i and $\hat{v}_o$) included in the circuit model.

The two voltage generators $\hat{v}_i$ and $\hat{v}_o$ in Fig. 7.12 are purposely shown in dotted lines to emphasize the fact that they are no longer essential, since the information provided by them (7.78) has already been used to find modulation $\hat{d}_2$ and substituted elsewhere in the circuit model. Therefore they can now be omitted from the circuit model. Finally, by modelling the current generators in Fig. 7.12 which are proportional to voltages across them as ac resistors only, the final circuit model of Fig. 7.13 is obtained.

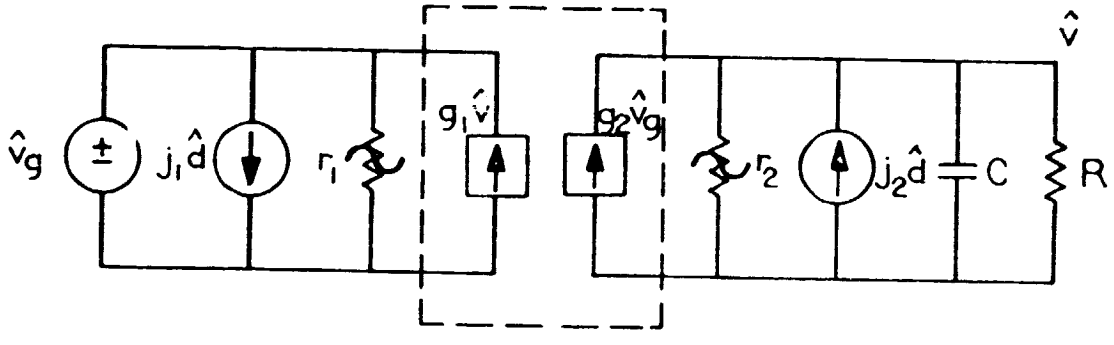


Fig. 7.13 Final ac small-signal circuit model for boost converter in the discontinuous conduction mode.

The element values in Fig. 7.13 are defined as

$$j_1 = \frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}\,, \qquad r_1 = \frac{M-1}{M^3}R\,, \qquad g_1 = \frac{M}{M-1}\frac{1}{R} \tag{7.83}$$

$$j_2 = \frac{2V}{R}\frac{1}{\sqrt{KM(M-1)}}\,, \qquad r_2 = \frac{M-1}{M}R\,, \qquad g_2 = \frac{M(2M-1)}{M-1}\frac{1}{R} \tag{7.84}$$

Also since r_1 and r_2 are ac resistances only, the appropriate symbol consistent with that adopted for the ideal transformer designation (see Fig. 3.7, for example) is used in Fig. 7.13. The two current generators inside the dotted-line box in Fig. 7.13 are used with square symbols to emphasize the fact that they are dependent current generators (on some other quantities in the circuit).

From the circuit model in Fig. 7.13 and by use of element definitions (7.83) and (7.84), the two transfer functions G_{vd} and G_{vg} can be derived. It can easily be verified that they agree exactly with those obtained before,((7.70), (7.71) and (7.72)), using the state-space averaging. An interesting observation with regard to the topology of the circuit model in Fig. 7.13 can be made. Namely, to arrive at these two transfer functions, only the elements in the output port j_2, r_2 and g_2 have been used, without any need for input port description. However, the input port description becomes mandatory if the determination of the complete circuit model is desired, since it properly models the important input properties (both open- and closed-loop input impedances, for example), as will be illustrated in Chapter 9. Moreover, the output port model now does affect the input properties through the dependent current generator $g_1\hat{v}$ in Fig. 7.13.

An interesting comparison with the circuit model topologies for the continuous conduction mode (Fig. 3.10 or Fig. 4.2) seems appropriate here. While in the continuous conduction mode the effect of duty ratio modulation $\hat{d}$ was expressed through duty ratio dependent voltage and current generators, here two duty ratio

dependent current generators (one at the input and the other at the output port) appropriately account for both input and transfer properties (and output properties, as well). Another distinction and unique feature of the circuit model of Fig. 7.13 is the presence of ac resistances only (which are in general dependent on an operating condition, the gain M), a characteristic not present in the continuous conduction mode. But despite these topological and qualitative differences, the circuit models for continuous conduction mode (Fig. 4.2) and discontinuous conduction mode (Fig. 7.13) have something very important in common: they both represent a complete linearized circuit model which accurately represents not only transfer properties but input and output properties as well.

In summary, this chapter has provided detailed insight into the various paths in the Flowchart of Fig. 6.1. A general method for modelling any three-state switching converter operating in the discontinuous conduction mode has been presented first. The fundamental step is in replacement of the state-space descriptions of the three switched networks (7.1) by their average (7.6) over the single period T_s, the same step as taken for any ordinary three-state converter. This is then supplemented by additional constraints (7.7) and (7.8) which properly account for the discontinuous conduction mode of operation.

The subsequent perturbation and linearization steps are applied not only to the state-space or circuit averaged models but also to the constraints, which then provide the additional information needed to define completely both dc and ac small-signal models.

An extensive analysis of the dc conditions in the discontinuous conduction mode has been given, which then enabled the definition of the boundary between the two operating modes for specific boost converter example. An easily interpretable formula ((7.50) or (7.54)) led to simple criteria ((7.51), (7.52) and (7.53)) for determination of the converter mode of operation.

Analysis of the dynamic (ac small-signal) model confirmed the general modelling prediction-reduction of the system order by one. Thus, common converters of Fig. 1.1 showed a single-pole frequency response in the discontinuous conduction mode, as opposed to their two pole response in the continuous conduction mode.

Finally, a new circuit model (Fig. 7.13) with a rather unusual topological structure is obtained, which provides a complete model for dynamic (ac small-signal) behavior.

The method outlined in this section, and illustrated for the boost converter, is applied to the other two converters of Fig. 1.1 and results are presented in various tabular forms (including the boost circuit example) in the next chapter on a canonical circuit model.

CHAPTER 8

CANONICAL CIRCUIT MODEL FOR DISCONTINUOUS CONDUCTION MODE

In this chapter the canonical circuit model for discontinuous conduction mode (block 5 in the Flowchart of Fig. 6.1 or Fig. 7.13) is obtained for the three common switching converters of Fig. 1.1 and, thanks to its fixed circuit topology, the results are conveniently summarized in the form of various tables, separately for dc and for ac small-signal circuit models.

From the dc conditions and by following the derivations presented in Section 7.1, the simple formulas for determination of the boundary between the two conduction modes may also be found for the buck and buck-boost converters. These results, analogous to (7.50) and (7.54) through (7.56) for the boost converter, are again tabulated for all three common converters of Fig. 1.1. This then ultimately determines which of the circuit models (those of Part I or those of Part II) should be chosen for given parameter values and operating conditions of a closed-loop switching regulator. An interesting pictorial interpretation facilitating this decision is given in terms of the frequency scale and position of another "inherent" frequency ω_β (frequency defined by converter element values, like ω_α and f_c before) with respect to switching frequency f_s.

Finally, both dc and ac transfer properties are experimentally verified on a particular buck-boost converter breadboard and excellent agreement with the predictions is observed, thus confirming

the high accuracy of the circuit models for the discontinuous conduction mode.

8.1 Derivation of the canonical circuit models for discontinuous conduction mode

In this section the canonical circuit models (both dc and ac small-signal circuit models) for the two remaining converters of Fig. 1.1 are derived from the basic circuit averaged models in Fig. 7.7.

Buck converter in discontinuous conduction mode

With regard to the dc circuit model derivation, a general observation seems appropriate here. Namely, the dc circuit model of the boost converter (Fig. 7.7) could have been obtained directly from the unperturbed circuit model in Fig. 7.7b by simply taking all quantities to be dc quantities and as usual considering the capacitance C to be open for dc signals. Hence, as should have been expected, the circuit models in Fig. 7.7 together with the additional expressions for the average inductor current i are valid dc models. But this is exactly why it was previously emphasized that the presented methods for finding dc and ac models are consistent with each other. After all, ac small-signal models really represent the linearized perturbation around some steady-state (dc) conditions. Hence, by perturbation and linearization of the circuit models in Fig. 7.7, the ac circuit models consistent with the superimposed dc circuit models result. Therefore, the dc circuit model for the buck converter is as in Fig. 7.7a with dc quantities $d = D$, $d_2 = D_2$,

$i = I$, $v_g = V_g$, $v = V$ and dc transformers only.

After usual perturbation and linearization steps are applied to circuit model of Fig. 7.7a, the dynamic (ac) circuit model in Fig. 8.1 is obtained.

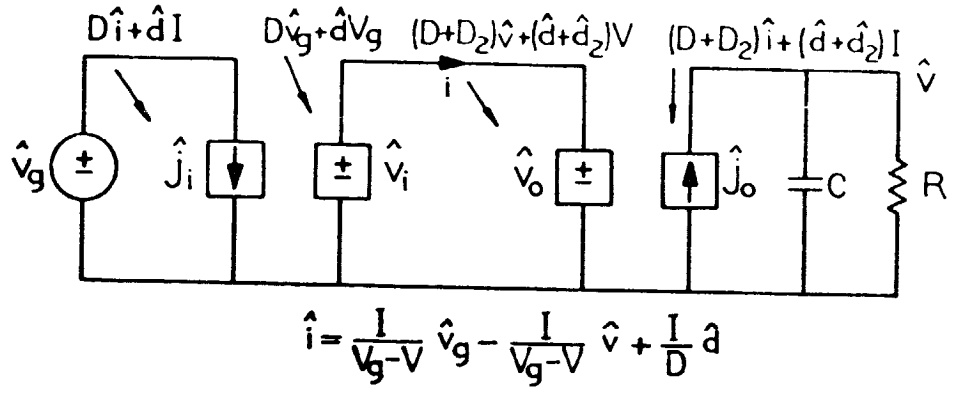


Fig. 8.1 Dynamic (ac small-signal) circuit model for the buck converter in discontinuous conduction mode with corresponding perturbation equation I for modulation $\hat{i}$.

The perturbation equation I is different from that for the boost converter and is

$$i = \frac{(v_g-v)dT_s}{2L} = \frac{(v_g-v)d}{(V_g-V)D} I \tag{8.1}$$

After perturbation and linearization of (8.1) we get

$$\hat{i} = \frac{I}{V_g-V}\hat{v}_g + \frac{I}{D}\hat{d} - \frac{I}{V_g-V}\hat{v} \tag{8.2}$$

When the unknown modulation quantity $\hat{d}_2$ is found from equality of the two voltage generators in Fig. 8.1 , and by use of (8.2), the two current generators in Fig. 8.1 , after expression of dc quantities in terms of closed-loop parameters M, K, R and V, become

$$\hat{j}_i = j_1\hat{d} + \hat{v}_g/r_1 - g_1\hat{v}; \qquad \hat{j}_o = j_2\hat{d} + g_2\hat{v}_g - \hat{v}/r_2 \tag{8.3}$$

where

$$j_1 = \frac{2V}{R}\sqrt{\frac{1-M}{K}}, \qquad r_1 = \frac{1-M}{M^2}R, \qquad g_1 = \frac{M^2}{1-M}\frac{1}{R} \tag{8.4}$$

$$j_2 = \frac{2V}{R}\frac{1}{M}\sqrt{\frac{1-M}{K}}, \qquad r_2 = (1-M)R, \qquad g_2 = \frac{M(2-M)}{1-M}\frac{1}{R} \tag{8.5}$$

Hence the same topology of the dynamic (ac) model for the boost converter shown in Fig. 7.13 is also obtained for the buck converter in the discontinuous conduction mode, but with the model element values defined by (8.4) and (8.5).

Buck-boost converter in the discontinuous conduction mode

The dc circuit model for the buck-boost converter is obtained directly from the circuit model in Fig. 7.7c. After perturbation and linearization of the model, the dynamic (ac) circuit model, in Fig. 8.2 is obtained.

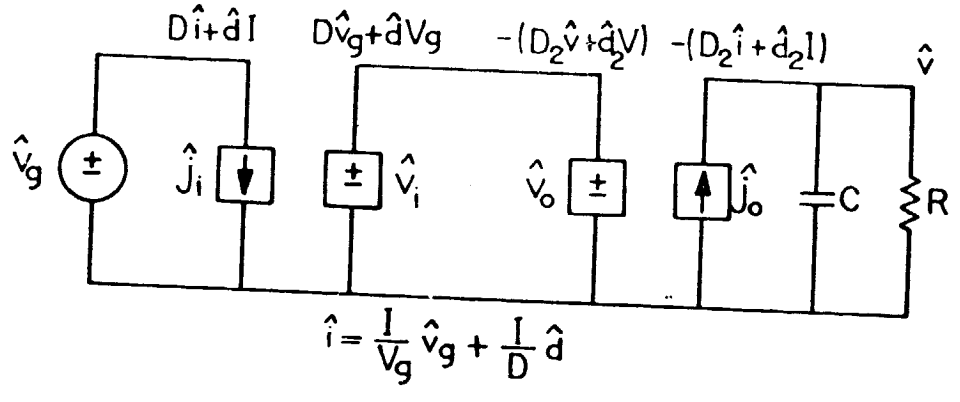


Fig. 8.2 Dynamic (ac small-signal) circuit model for the buck-boost converter in discontinuous conduction mode with perturbation equation I (for $\hat{i}$) shown explicitly.

The perturbation equation I is now the same as for the boost converter (7.75) and the two current generators $\hat{j}_i$ and $\hat{j}_o$ in Fig. 8.2 are as defined in (8.3) but with the following element values for the buck-boost converter:

$$j_1 = \frac{2|V|}{\sqrt{KR}}, \qquad r_1 = \frac{R}{M^2}, \qquad g_1 = 0 \tag{8.6}$$

$$j_2 = 2\,\frac{|V|}{\sqrt{KR}}\,\frac{1}{M}, \qquad r_2 = R, \qquad g_2 = \frac{2M}{R} \tag{8.7}$$

Again the same circuit topology of Fig. 7.13 results, but with element values (8.6) and (8.7). However, there is a small distinction from the previous two models since now, as seen in (8.6), $g_1 = 0$. Therefore there is no feedback effect from the output port to the input circuit model as in the other two converters, and the open-loop input impedance is just r_1. But, this is reasonable to expect for the buck-boost converter, since it is the only converter in which the energy transferring inductance is present either solely in the input circuit (interval DT_s) or solely in the output circuit (interval D_2T_s). In the other two converters (buck and boost), on the other hand, the output circuit (including C and R) is at least for a portion of period T_s connected to the input and represents a loading effect on it. Hence the feedback action through current generator $g_1\hat{v}$ is to be expected in these two converters.

The results for all three converters (buck, boost and buck-boost) are summarized in the next section.

8.2 Summary of the canonical circuit model results for three common converters

In this section the results for both dc and dynamic (ac) canonical circuit models for buck, boost and buck-boost converter are summarized and, owing to the fixed circuit model topology, conveniently listed in several tables.

STEADY STATE (DC) CIRCUIT MODEL

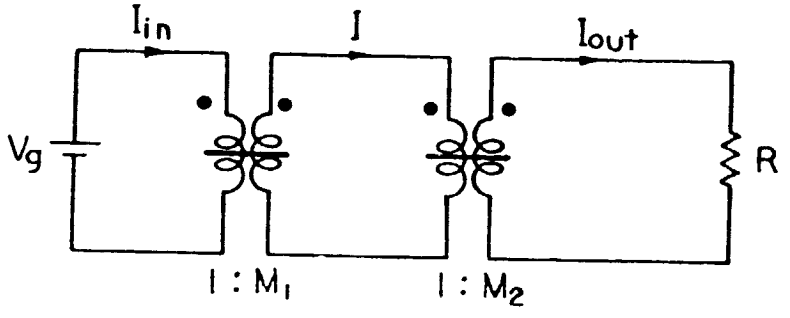


Fig. 8.3 Steady-state (dc) circuit model for the converters of Fig. 1.1 in the discontinuous conduction mode.

In Fig. 8.3 the polarity of the second transformer $1:M_2$ is inverting for the buck-boost converter and otherwise as shown. The parameters in the dc circuit model of Fig. 8.3 are defined in the first three columns of Table IV, while the remaining two columns tabulate the dc relations derived from this circuit model. Note, however, that this circuit model can be used to determine other dc quantities as well, such as the dc input current I_{in} in terms of the defining parameters.

converter type	definition of dc model			derived quantities	
	M_1	M_2	I(average)	$I = M_2 V/R$	$M = M_1 M_2$
buck	D	$\frac{1}{D+D_2}$	$\frac{(V_g - V)DT_s}{2L}$	$\frac{V}{(D+D_2)R}$	$\frac{D}{D+D_2}$
boost	$D+D_2$	$\frac{1}{D_2}$	$\frac{V_g D T_s}{2L}$	$\frac{V}{D_2 R}$	$\frac{D+D_2}{D_2}$
buck-boost	D	$\frac{1}{D_2}$	$\frac{V_g D T_s}{2L}$	$\frac{V}{D_2 R}$	$\frac{D}{D_2}$

TABLE IV Definition of the dc circuit model in Fig. 8.3 for the three common converters of Fig. 1.1 operating in the discontinuous conduction mode.

With use now of the last three columns of Table IV and the procedures outlined in Chapter 7 in Section 7.1, the very useful Table V can be generated, in which the dimensionless parameter K is defined as before with $K = 2L/RT_s = 2Lf_s/R$.

converter type	open-loop consideration		closed-loop consideration	
	$M(D,K)$	$D_2(D,K)$	$D(M,K)$	$D_2(M,K)$
buck	$\frac{2}{1+\sqrt{1+4K/D^2}}$	$\frac{K}{D}\frac{2}{1+\sqrt{1+4K/D^2}}$	$\sqrt{\frac{KM^2}{1-M}}$	$\sqrt{K(1-M)}$
boost	$\frac{1+\sqrt{1+4D^2/K}}{2}$	$\frac{K}{D}\frac{1+\sqrt{1+4D^2/K}}{2}$	$\sqrt{KM(M-1)}$	$\sqrt{\frac{KM}{M-1}}$
buck-boost	$\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$M\sqrt{K}$	$\sqrt{K}$

TABLE V Summary of dc transfer properties of the three common converters of Fig. 1.1 in the discontinuous conduction mode expressed for open-loop as well as for closed-loop considerations.

DYNAMIC (AC SMALL-SIGNAL) CIRCUIT MODEL

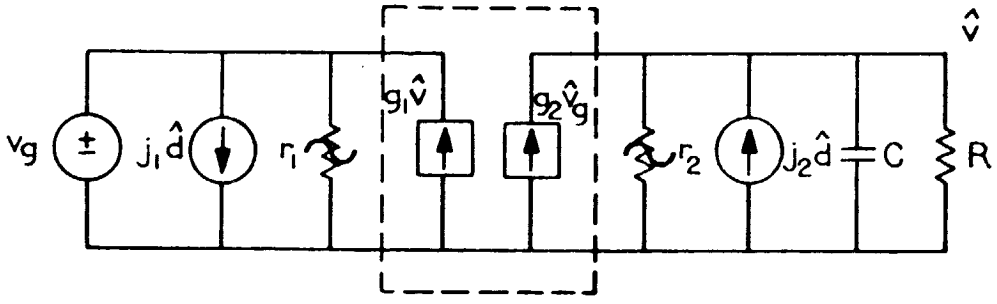


Fig. 8.4 Final ac small-signal circuit model for converters of Fig. 1.1 in the discontinuous conduction mode.

The element values of the dynamic (ac) circuit model in Fig. 8.4 for the three converters are shown in Table VI.

type	j_1	r_1	g_1	j_2	r_2	g_2
buck	$\frac{2V}{R}\sqrt{\frac{1-M}{K}}$	$\frac{1-M}{M^2}R$	$\frac{M^2}{1-M}\frac{1}{R}$	$\frac{2V}{RM}\sqrt{\frac{1-M}{K}}$	$(1-M)R$	$\frac{M(2-M)}{1-M}\frac{1}{R}$
boost	$\frac{2V}{R}\sqrt{\frac{M}{K(M-1)}}$	$\frac{M-1}{M^3}R$	$\frac{M}{M-1}\frac{1}{R}$	$\frac{2V}{R\sqrt{KM(M-1)}}$	$\frac{M-1}{M}R$	$\frac{M(2M-1)}{M-1}\frac{1}{R}$
buck-boost	$\frac{2\lvert V\rvert}{R\sqrt{K}}$	$\frac{R}{M^2}$	0	$\frac{2\lvert V\rvert}{R\sqrt{K}M}$	R	$\frac{2M}{R}$

TABLE VI Definition of the elements in the canonical circuit model of Fig. 8.4 for the three common converters of Fig. 1.1 operating in the discontinuous conduction mode.

Again, as Table V was generated from Table IV and only input-output dc transfer properties obtained, we can similarly generate from Table VI another Table VII in which only input-output ac transfer properties (transfer functions G_{vg} and G_{vd}) are listed for the three converters.

type	G_{og}	G_{od}	ω_p
buck	M	$\frac{2V(1-M)^{3/2}}{\sqrt{K}\,M(2-M)}$	$\frac{2-M}{1-M}\,\frac{1}{RC}$
boost	M	$\frac{2V}{2M-1}\sqrt{\frac{M-1}{KM}}$	$\frac{2M-1}{M-1}\,\frac{1}{RC}$
buck-boost	M	$\frac{V}{\sqrt{K}\,M}$	$\frac{2}{RC}$
$G_{vg}=\frac{\hat{v}}{\hat{v}_g}=G_{og}\frac{1}{1+s/\omega_p}$; $G_{vd}=\frac{\hat{v}}{\hat{d}}=G_{od}\frac{1}{1+s/\omega_p}$			

TABLE VII Summary of the ac transfer properties of the three common converters of Fig. 1.1 operating in the discontinuous conduction mode.

All the results presented in this section are applicable only to the discontinuous conduction mode of operation of these three switching converters. To determine when these results ought to be applied and when those presented in Chapter 4 for continuous conduction mode, the boundary between the two modes of operation is determined for these three converters and tabulated in the next section.

8.3 Determination of the boundary between two conduction modes

As explained in detail in Section 7.1 the criteria for determination of the converter conduction mode are

boundary between the two conduction modes

$$K = K_{crit} \qquad \text{or} \qquad R = R_{crit} \tag{8.8}$$

continuous conduction mode

$$K > K_{crit} \qquad \text{or} \qquad R < R_{crit} \tag{8.9}$$

discontinuous conduction mode

$$K < K_{crit} \qquad \text{or} \qquad R > R_{crit} \tag{8.10}$$

where K is as defined before $K = 2L/RT_s = 2Lf_s/R$. Following the same procedure outlined in Section 7.1 for the boost converter example, the parameters K_{crit} and R_{crit} can easily be found for the other two converters and all results are shown tabulated in Table VIII.

converter type	open-loop consideration		closed-loop consideration	
	$K_{crit}(D)$	$R_{crit}(D, R_{nom})$	$K_{crit}(M)$	$R_{crit}(M, R_{nom})$
buck	$1 - D$	$\frac{R_{nom}}{1-D}$	$1 - M$	$\frac{R_{nom}}{1-M}$
boost	$D(1-D)^2$	$\frac{R_{nom}}{D(1-D)^2}$	$\frac{M-1}{M^3}$	$\frac{M^3}{M-1} R_{nom}$
buck-boost	$(1-D)^2$	$\frac{R_{nom}}{(1-D)^2}$	$\frac{1}{(M+1)^2}$	$(M+1)^2 R_{nom}$

TABLE VIII Determination of the boundary between the two conduction modes, expressed for open-loop as well as for closed-loop considerations.

In Table VIII nominal resistance R_{nom} is a design parameter defined by

$$R_{nom} = 2Lf_s \tag{8.11}$$

It has already been demonstrated in Section 7.1 for the boost converter that parameter K can be chosen ($K > 4/27$), such that the converter is <u>always</u> operating in the continuous conduction mode regardless of the operating point, that is dc duty ratio D, while the discontinuous conduction mode can occur only for $K < 4/27$, and then only for a portion of the dynamic range of duty ratio D. The same holds true for the other two converters, and the following criteria can be set:

a) when $K > K_M$ converter is always in continuous conduction mode regardless of D.

b) when $K < K_M$ discontinuous conduction mode can occur, but only for limited range of duty ratio D.

Parameter K_M is actually the maximum of the duty ratio D dependent function of first column in Table VIII, and is for comparison purposes listed in Table IX.

	buck	boost	buck-boost
K_M	1	$\frac{4}{27}$	1

TABLE IX Summary of the parameter K_M determining the region of unconditional continuous conduction for three common converters of Fig. 1.1.

From Table IX it is obvious that when K > 1 any of the three converters listed will always operate in the continuous conduction mode, and when K < 4/27 each of them will operate in the discontinuous conduction mode for a portion of the duty ratio range. With this, and the first column in Table V, the dc voltage gain as a function of duty ratio can be shown as in Fig. 8.5b for K < 4/27, while the corresponding result for continuous conduction mode is illustrated for comparison purposes in Fig. 8.5a for K > 1.

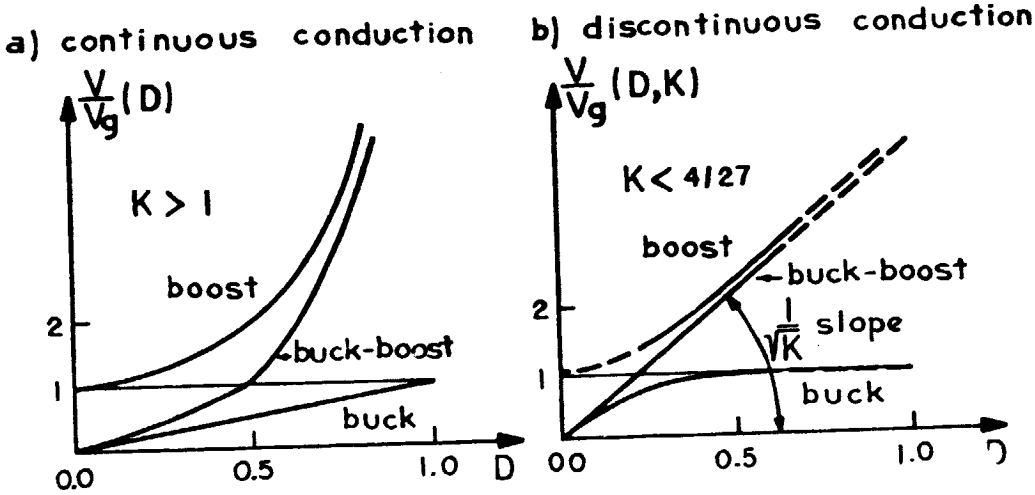


Fig. 8.5 Comparison of the dc voltage gain characteristics in the two conduction modes for the common converters of Fig. 1.1.

In Fig. 8.5b heavy lines designate the region of actual discontinuous conduction operation, whereas dotted lines signify that the continuous conduction mode takes over and the dc gain characteristics begin to follow those for the continuous conduction mode (see for comparison Fig. 7.4). From Fig. 8.5b it is also evident that in the buck and the buck-boost converter, the transition between the two conduction modes occurs only once at higher duty ratio D, and not

also at the lower end as it does in the boost converter. Therefore, during initial start-up of the converter, when the duty ratio changes from zero to the value required by the steady-state gain M, the two converters (buck and buck-boost) can be designed to stay in the discontinuous conduction mode only, even in this transitional period.

We now present another viewpoint, which in an interesting pictorial way and a unique frequency interpretation, illuminates the determination of the converter operating mode and the basic small-switching-ripple requirement. Namely, from Fig. 1.1 it is apparent that the three common converters essentially consist of the single switch S positioned differently among the source voltage V_g and three elements, inductance L, capacitance C, and load R. With only these three elements three different "inherent" frequencies can be defined regardless of the converter type. Two of them, ω_α and f_c, termed natural frequencies, have previously been defined (1.11) and are repeated here for completeness:

$$\omega_\alpha = \frac{1}{2RC}, \qquad f_c = \frac{1}{2\pi\sqrt{LC}} \tag{8.12}$$

However, yet another "inherent" frequency ω_β can be defined by these three elements as

$$\omega_\beta = \frac{R}{2L} \tag{8.13}$$

The dimensionsless parameter K, which plays a crucial role in the determination of the conduction mode, can now be expressed as

$$K = \frac{f_s}{\omega_\beta} \tag{8.14}$$

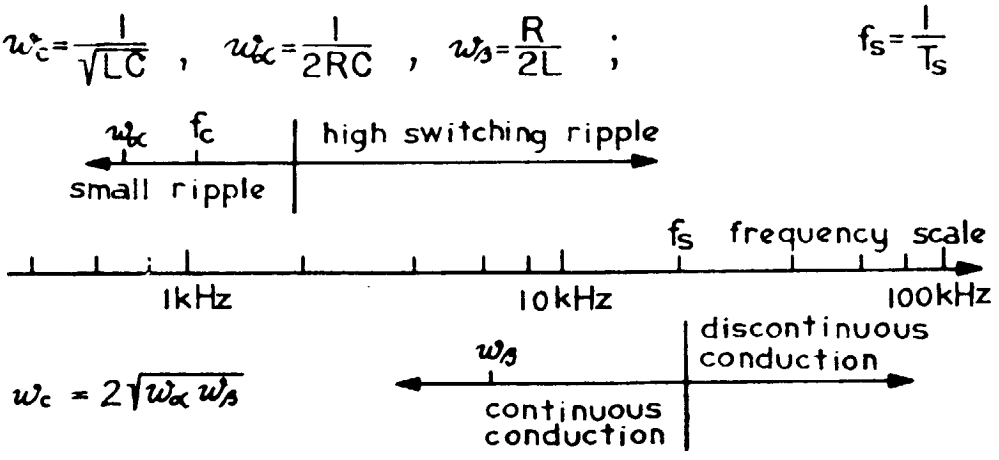


Fig. 8.6 Frequency interpretation of the conduction mode type and small switching ripple requirement.

Therefore, the position of this new frequency ω_β with respect to the switching frequency f_s determines the conduction mode. Hence for $K > 1$ or $\omega_\beta < f_s$, each of the three converters will always be in continuous conduction mode regardless of D. Also it was shown before (1.11) that $\omega_\alpha << f_s$ and $f_c << f_s$ are requirements for small switching ripple. The information contained in the position of these three "inherent" frequencies ω_α, ω_β and f_c with respect to the switching frequency f_s is concisely summarized in Fig. 8.6. The diagram in Fig. 8.6, with the help of definitions (8.12) and (8.13), displays in a convincing manner the interplay between conduction mode types, switching ripple requirement and choice of parameter values L, C, R and f_s. For example, increase of load R can cause change to discontinuous conduction mode without deterioration in switching ripple. However, if inductance L or switching frequency is reduced, change to discontinuous conduction mode can occur, but at the price of higher switching ripple since separation between f_c and f_s is also reduced. One would have to

increase capacitance C to remain at an acceptable switching ripple level. Thus the frequency diagram of Fig. 8.6 gives valuable insight, both qualitative and quantitative, into the basic relationships inherent to switching converters. It is interesting that from (8.12) and (8.13) a very simple relationship follows

$$\omega_c = 2\sqrt{\omega_\alpha \omega_\beta} \qquad (8.15)$$

which may further facilitate quantitative analysis.

8.4 Experimental verification of the transfer properties

Both dc and ac transfer properties have been experimentally verified on a circuit breadboard of the buck-boost converter shown in Fig. 7.7c.

The buck-boost converter was chosen because of several unique features which clearly distinguish it from the other two converters, and which are easy to check. A quick look at Table V, for example, reveals that it is the only converter whose second interval D_2T_s is independent of the operating conditions (duty ratio D or gain M), but rather is fixed determined by the parameter K only.

Likewise, a look at Table VI shows that the ac resistance r_2 is also independent of steady-state operating condition (gain M). Therefore, the single pole of the two transfer functions G_{vg} and G_{vd} does not move with change of operating condition (gain M) as it does in the other two converters.

Finally, the open-loop input impedance of the buck-boost converter is $R_i = R/M^2$ since there is no internal feedback ($g_1 = 0$). Hence the input impedance is purely resistive, which is not the case for the other two converters.

The transfer properties have been verified on the test buck-boost converter with the following switching components: transistor 2N2880 and diode TRW7342.

Dc gain measurements

For the choice of element values L = 890μH, C = 12μF, R = 220Ω, f_s = 10kHz and V_g = 6V we compute $K = 2Lf_s/R = 0.81$ and $D_2 = \sqrt{K} = 0.28$. Therefore, the buck-boost converter operates in the discontinuous conduction mode from D = 0 until $D = 1-D_2 = 0.72$, and the experimental dc gain characteristic is shown in this duty ratio range on Fig. 8.7.

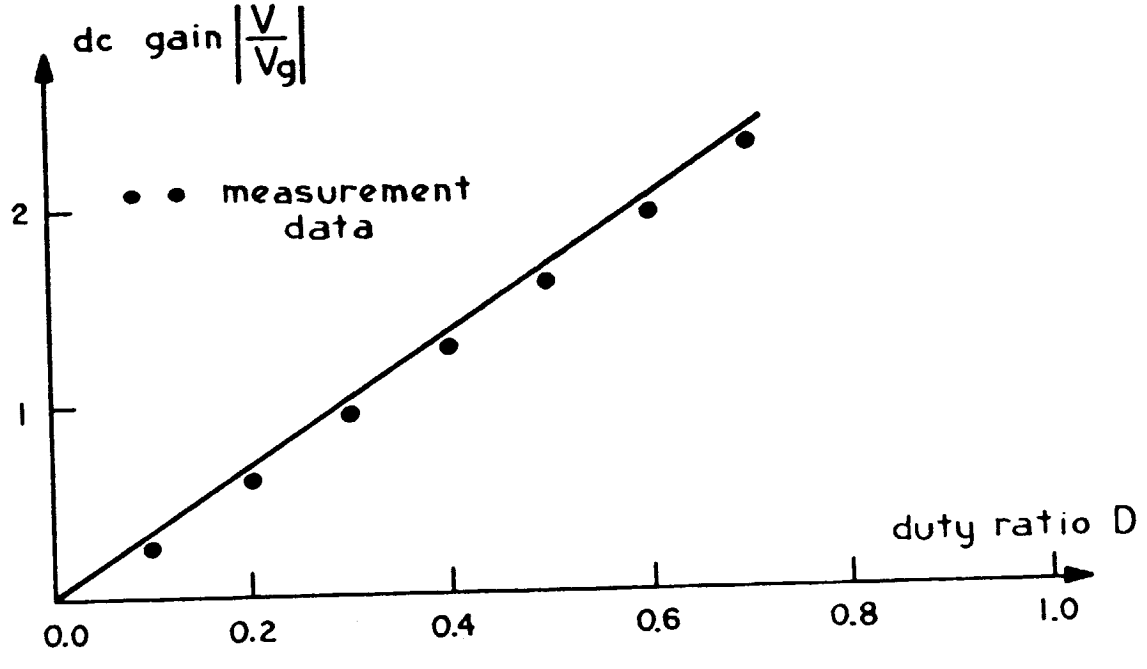


Fig. 8.7 Dc voltage gain measurements for the buck-boost converter in the discontinuous conduction mode.

As seen in Fig. 8.7, experimental points follow very closely the theoretical straight line characteristic. The experimental data, however, are slightly lower than the theoretical curve since

the transistor saturation voltage and diode drop have not been accounted for in the theoretical model, although this can easily be accomplished. The inductor current waveform was monitored, and confirmed discontinuous conduction operation for D ε[0,0.72] while D_2 measured was constant as predicted at D_2 = 0.28.

Ac transfer function measurements

The duty ratio modulation $\hat{d}$ to output voltage $\hat{v}$ transfer function G_{vd} is now measured using the describing function measurement technique [20].

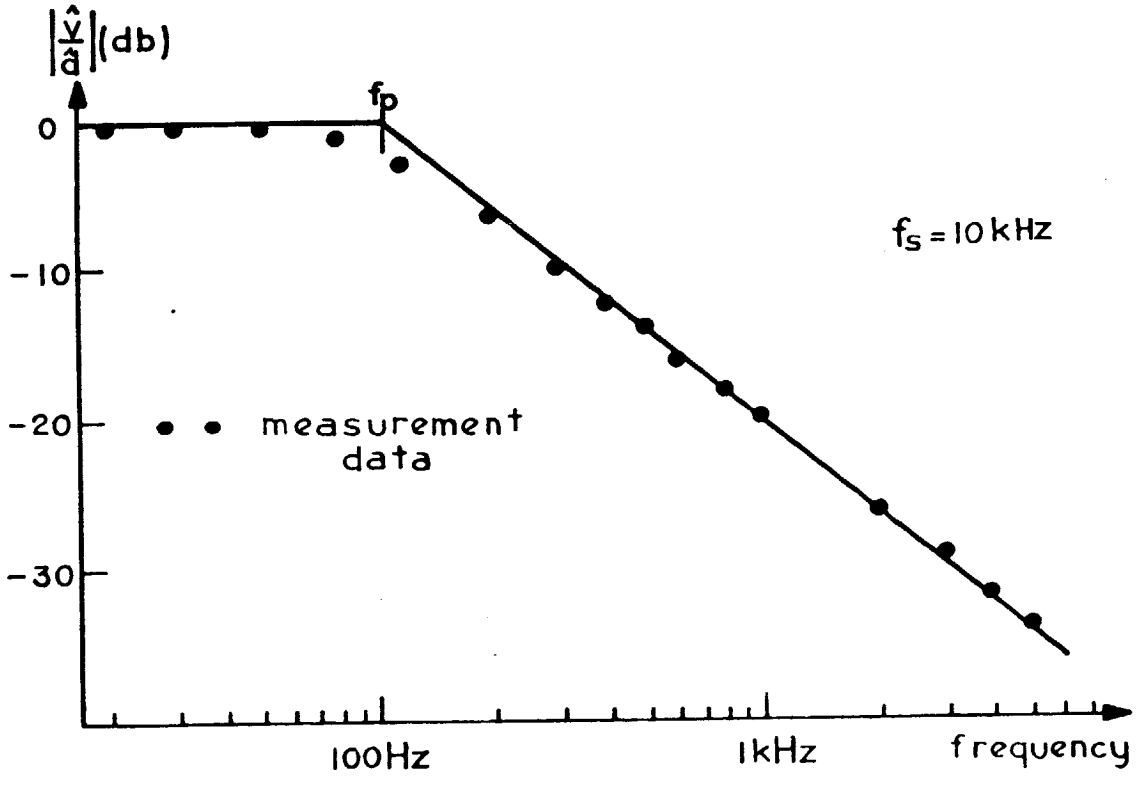


Fig. 8.8 Experimental magnitude-frequency response of $G_{vd} = \hat{v}/\hat{d}$ transfer function for buck-boost converter in the discontinuous conduction mode.

The element values used are the same as for the dc measurements, except that the inductance was increased four times to L = 3.5mH to reduce the superimposed switching ripple and to reduce the ringing effect in the D_3T_s interval. Hence for L = 3.5mH, C = 12μF, R = 220Ω, f_s = 10kHz, V_g = 6V we calculate K = 1.62 and D_2 = 0.56. The range of discontinuous conduction operation is then reduced to D ε [0,0.44]. The single pole of the transfer functions G_{vg} and G_{vd} (see Table VII) becomes $f_p = 1/\pi RC$ = 120Hz, which is in excellent agreement with the experimental data shown in Fig. 8.8.

The measurements were repeated for several operating points in the discontinuous conduction region, namely, for D = 0.1, 0.2, 0.3, and 0.4 but the single pole at f_p, as predicted, did not move.

The experimental measurements therefore have confirmed the high degree of accuracy of the canonical circuit model (Fig. 8.4) for the discontinuous conduction mode of operation.

In summary, the canonical circuit model for discontinuous conduction mode (Fig. 8.4) retains all the advantages of the fixed topology structure, previously mentioned in Section 4.2 in connection with the canonical circuit model for continuous conduction mode. The culmination of the modelling in discontinuous conduction mode is given by Section 8.2, where the results for several converters are conveniently summarized in various tables for later quick reference and use. This further enables an easy method of determination of the conduction mode type through Section 8.3, where the results for several converters have been summarized. Common features of the three

standard converters (buck, boost, and buck-boost) have been extracted via an interesting frequency interpretation. Finally, in Section 8.4, the transfer properties predicted by the canonical circuit model have been experimentally confirmed for the buck-boost converter. The single-pole frequency response (Fig. 8.8) for discontinuous conduction mode is in sharp contrast with the two pole, right half-plane zero frequency response (Table III) for continuous conduction mode, and verifies the general prediction of different converter dynamics in the two conduction modes.

Only one issue has not been covered in this chapter. It is the question of converter input properties, and particularly of open- and closed-loop input impedances, which are left to the next chapter on modelling of a switching mode regulator in discontinuous conduction mode.

CHAPTER 9

MODELLING OF SWITCHING REGULATOR IN DISCONTINUOUS CONDUCTION MODE

This chapter, in an analogous way to Chapter 5, demonstrates how the canonical circuit model for a switching converter operating in the discontinuous conduction mode can easily be incorporated into the complete switching-mode regulator model. The modelling of the modulator stage has already been given in Section 5.1, so it will be directly included here and a complete linear negative feedback circuit model of the regulator will be obtained. This model is subsequently used to derive the important regulator properties loop gain T, input and output impedances Z_i and Z_o, and line transmission characteristic F, but this time for discontinuous conduction mode. The obtained general expressions are then compared with the corresponding results ((5.2) through (5.5)) for the continuous conduction mode.

Again, the input properties, both open-loop and especially closed-loop input impedance, are of special importance when the regulator is a part of a more complex network. Owing to the very nature of the switching regulator operation, its closed-loop incremental input resistance R_i is negative at low frequencies, even in the discontinuous conduction mode, since the simplified reasoning (5.6) of Section 5.3 applies equally well. It is then demonstrated that the duty ratio dependent current generator $j_1(s)\hat{d}$ at the input of the canonical circuit model (Fig. 8.4) is the one whose presence properly models such behavior in much the same way as the $j(s)\hat{d}$ current generator did for the continuous conduction mode canonical

circuit model (see Fig. 5.2, for example).

Again as before, the modelling techniques ([11] through [17]) are not capable of describing such behavior, because of the total absence of the input model of the converter and/or regulator. This then once more stresses the completeness of the canonical circuit models of Part I and Part II for either conduction mode of operation.

9.1 Analysis of switching regulator in discontinuous conduction mode

The inclusion of the canonical circuit model (Fig. 8.4) and an appropriate model for the modulator stage (5.1) into the switching regulator (Fig. 5.1) results in a complete circuit model of a switching regulator in the discontinuous conduction mode, as shown in Fig. 9.1.

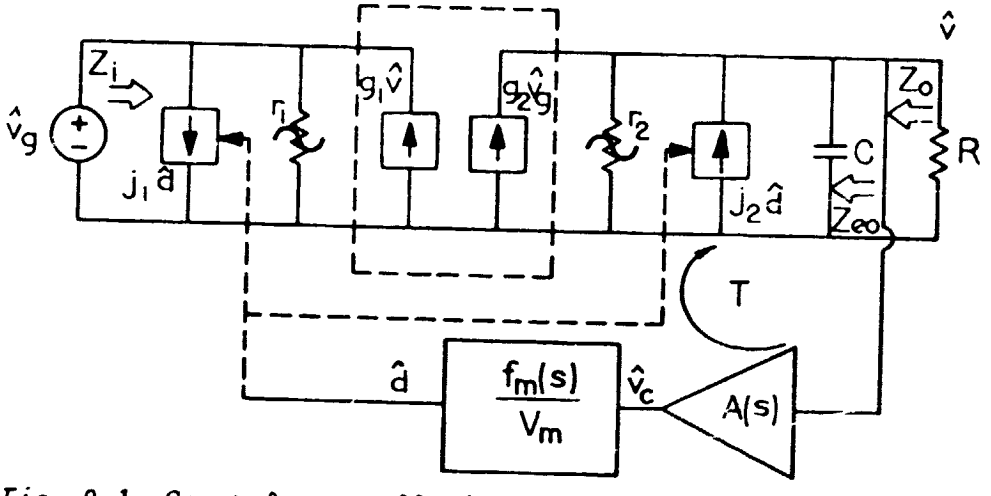


Fig. 9.1 General ac small-signal circuit model for the switching regulator of Fig. 5.1 operating in the discontinuous conduction mode.

The generator symbol for the current generators $j_1(s)\hat{d}$ and $j_2(s)\hat{d}$ at the input and output ports, respectively, has been changed from a circle to a square to emphasize that in the closed-loop regulator they have become dependent generators (on output voltage modulation $\hat{v}$ in particular). A closer look at the circuit model in Fig. 9.1 reveals some unique properties of this negative feedback circuit. Namely, it has been previously shown in Section 7.3 that only the output port network (consisting of current generators $g_2\hat{v}_g$, $j_2\hat{d}$, resistances r_2 and R and capacitance C) effectively takes part in determination of the open-loop transfer functions G_{vg} and G_{vd}. The immediate implication of this is that for ideal source voltage $\hat{v}_g$, the loop gain T is defined only with respect to the output port as shown in Fig. 9.1. Likewise, the output impedance Z_o

and line transmission characteristic F (audio-susceptibility) become solely defined in terms of the output port elements, while the input port takes part only in determination of the input impedance Z_i. This is easily confirmed by analysis of the equivalent circuit in Fig. 9.1, which leads to

$$T = G_{vd}(s)A(s)f_m(s)/V_m \tag{9.1}$$

$$Z_o = \frac{Z_{eo}(s)}{1+T} \tag{9.2}$$

$$F = \frac{G_{vg}(s)}{1+T} \tag{9.3}$$

$$\frac{1}{Z_i} = -\frac{T}{1+T}\left(\frac{G_{vg}}{G_{vd}}j_1 - \frac{1}{r_1}\right) + \frac{1}{1+T}\left(\frac{1}{r_1} - g_1 G_{vg}\right) \tag{9.4}$$

The first three expressions are rather obvious and are a consequence of the general results of linear feedback theory. They also confirm that T, Z_o, and F are functions of the output port elements only, since the open-loop transfer functions G_{vg} and G_{vd} are independent of input port elements. These results are actually the same analytical expressions as the corresponding expressions for the continuous conduction mode ((5.2), (5.3) and (5.4)), except that the open-loop quantities G_{vg}, G_{vd} and Z_{eo} in discontinuous conduction mode are different from those in continuous conduction mode as, for example, the analysis of transfer functions G_{vg} and G_{vd} in previous sections clearly demonstrated.

The fourth expression (9.4) for closed-loop input impedance is rather complicated and will be derived in the next section. However, it does clearly demonstrate that the input impedance is dependent

also on the input quantities j_1, r_1 and g_1.

It should be noted, however, that this peculiar dependence of some feedback quantities T, Z_o, and F on output port elements only, is a quite special case, which is a consequence of the ideal source voltage $\hat{v}_g$. If the source voltage had an internal impedance, or an input filter were included in front of the converter, even the open-loop transfer functions G_{vg} and G_{vd} would become dependent on all circuit elements, the feedback quantities even more so, and this special feature would disappear. This once again demonstrates how powerful these converter equivalent circuit models are, since any of such additional effects can be directly included in the circuit model of Fig. 9.1, owing to its complete circuit representation of the converter properties.

We now investigate in more detail the important input properties of the circuit model in Fig. 9.1, and make appropriate comparisons with the corresponding result (5.5) for continuous conduction mode.

9.2 Input properties of switching regulators in discontinuous conduction mode

Let us first derive the input impedance formula (9.4) by use of the circuit model in Fig. 9.1. The input current $\hat{i}_g$ can be expressed as

$$\hat{i}_g = \frac{\hat{v}_g}{Z_i} = j_1\hat{d} + \hat{v}_g/r_1 - g_1\hat{v} \qquad (9.5)$$

The objective is now to express $\hat{d}$ and $\hat{v}$ modulation quantities in terms of $\hat{v}_g$. From the feedback network description

$$\hat{d} = -\frac{f_m(s)}{V_m} A(s)\hat{v} \tag{9.6}$$

Note that the negative sign in (9.6) expresses the negative feedback effect: increase of output voltage is corrected by decrease of dc duty ratio, hence $\hat{d}$ is negative. By use of (9.1) in (9.6) we get

$$\hat{d} = -\frac{T}{G_{vd}} \hat{v} \tag{9.7}$$

From (9.3) we obtain directly

$$\hat{v} = \frac{G_{vg}}{1+T} \hat{v}_g \tag{9.8}$$

Finally, substitution of (9.7) and (9.8) in (9.5) results in the input impedance for discontinuous conduction mode:

$$\frac{1}{Z_i} = -\frac{T}{1+T}\left(\frac{G_{vg}}{G_{vd}} j_1 - \frac{1}{r_1}\right) + \frac{1}{1+T}\left(\frac{1}{r_1} - g_1 G_{vg}\right) \tag{9.9}$$

It is interesting that the corresponding result (5.5) for continuous conduction mode can be put in a very similar form, as

$$\frac{1}{Z_i} = -\frac{T}{1+T}\frac{G_{vg}}{G_{vd}} j + \frac{1}{1+T}\frac{1}{\mu^2 Z_{ei}} \tag{9.10}$$

where G_{vg} and G_{vd} are open-loop transfer functions for the continuous conduction mode.

Comparison of (9.9) and (9.10) clearly shows that, for both canonical circuit models, the input duty ratio dependent current generators $j_1\hat{d}$ (in Fig. 9.1) and $j\hat{d}$ (in Fig. 4.2) are responsible for the negative input impedance at low frequencies. If they were not present in the model, $j_1 = 0$ and $j = 0$, and since at low frequencies

$T \to \infty$, the input resistance R_i would appear to be positive, in obvious conflict with the actual physical requirement (5.6).

Let us now verify this for the discontinuous conduction mode, and consider first the limiting case of (9.9) for high loop gain $T \to \infty$ (at low frequencies)

$$\frac{1}{R_i} = -\left(\frac{G_{vg}}{G_{vd}} j_1 - \frac{1}{r_1}\right) \tag{9.11}$$

From the circuit model in Fig. 9.1 the converter open-loop transfer functions G_{vg} and G_{vd} are easily found as

$$G_{vg} = g_2(r_2 \| R)\frac{1}{1 + sC(r_2 \| R)}$$

$$G_{vd} = j_2(r_2 \| R)\frac{1}{1 + sC(r_2 \| R)} \tag{9.12}$$

By use of (9.12) in (9.11) we finally obtain the closed-loop incremental resistance R_i as

$$R_i = -\left(\frac{j_1}{j_2} g_2 - \frac{1}{r_1}\right) \tag{9.13}$$

Using now the definitions of element values j_1, j_2, g_2, and r_1 from Table VI in (9.13), we obtain for all three converters (buck, boost and buck-boost) that

$$R_i = -\frac{R}{M^2} = -\left(\frac{V_g}{V}\right)^2 R \tag{9.14}$$

However, this is the same as the closed-loop incremental resistance R_i for continuous conduction mode given previously in (5.7).

From (9.13) it is also evident that despite the presence of the positive term, the negative term has prevailed, correctly

predicting the negative closed-loop input resistance.

Let us now consider the other extreme when the loop gain is very small, that is T→0 (or equivalently at high frequencies). Then, the input impedance approaches the open-loop input impedance Z_{in} obtained from (9.9) as

$$\frac{1}{Z_{in}} = \frac{1}{r_1} - g_1 G_{vg} \tag{9.15}$$

The same result could be obtained directly from the open-loop converter model in Fig. 8.4. From (9.15) it seems as though Z_{in} could be negative owing to this negative internal effect of the current generator $g_1\hat{v}$ in the model of Fig. 8.4. However, this is not true, since the low-frequency value of the open-loop input impedance R_{in} becomes from (9.15)

$$R_{in} = \frac{r_1}{1 - g_1 r_1 g_2 (r_2 \| R)} \tag{9.16}$$

Again by using element definitions from Table VI in (9.16) we get for <u>all</u> three converters

$$R_{in} = \frac{R}{M^2} = \left(\frac{V_g}{V}\right)^2 R \tag{9.17}$$

which correctly predicts open-loop low-frequency input resistance to be positive. This is actually also the same result as the one obtained previously for the continuous conduction mode in (5.8).

From these derivations and the corresponding one in Chapter 5, it follows that the closed-loop low-frequency input resistance R_i is given by (9.14) <u>regardless</u> of the conduction mode type and switching converter type (buck, boost or buck-boost). The same is also true for the open-loop low-frequency input resistance R_{in} given by (9.17).

In summary, this chapter has confirmed that the canonical circuit model for discontinuous conduction mode (Fig. 9.1) properly models the regulator input properties (closed-loop input impedance) in much the same way as the canonical circuit model for continuous conduction mode (Fig. 5.2) did, through the presence of duty ratio dependent current generators at the input of the converter model. The immediate consequence of this is that the regulator circuit model (Fig. 9.1) is a complete circuit model which correctly represents all essential properties; input, output and transfer properties.

GENERAL THEORY AND DESIGN OF BUCK-BOOST CONVERTERS

PART III

CASCADE CONNECTION OF BUCK AND BOOST CONVERTERS

CHAPTER 10

GENERIC PROPERTIES OF CASCADE CONNECTIONS OF POWER STAGES

A twofold purpose is intended for this Part III. First, a new class of switching converters generated by the cascade connection of common power stages is introduced. It demonstrates the feasibility of various realizations of the generalized switching converter (Fig. 1.11) but at the same time provides verification of some of the general modelling predictions made through the canonical circuit model of Part I, which could not have been illustrated there owing to the lack of the appropriate converter topology (converters with more than two storage elements and a single switch). Second, a closer look at these converters and some of their unique features paves the way for the discovery of a new optimum topology switching converter superior to existing converters in its class, which will be presented in Part IV. The new converter will at the same time fill the gap previously existing in the complete theory of buck-boost converters by establishing the remaining missing link.

Since the emphasis in the remaining parts is on the converter topology and <u>not</u> on its particular mode of operation, it will be assumed throughout, unless otherwise specified, that all converters operate as two-state converters, hence also in a continuous conduction mode.

In this chapter, a valuable insight into the generic properties of the cascade connection of buck and boost power stages is gained,

which allows a renewed look at the common converters of Fig. 1.1. In particular, it is demonstrated that the buck-boost converter of Fig. 1.1 (or conventional buck-boost converter as it will be referred to in the future) may be viewed as a special case derived from one kind of cascade connection between buck and boost converters (buck converter followed by a boost converter) rather than a completely independent circuit. The other two converters (buck and boost) are then regarded as truly basic converters. In connection with that an important conclusion is arrived at: the reduction of number of switches in this cascade connection from two to one (and therefore reduction of both dc and switching losses) can be achieved by sacrifice of the original noninverting property (both input and output dc voltage of the same polarity) for the inverting one (as in the conventional buck-boost converter of Fig. 1.1).

However, this does not exhaust all the possibilities of interconnecting buck and boost converters in order to achieve a general dc transfer function (both increase or decrease of input dc voltage), since a boost converter cascaded by a buck converter is proven to be a much superior topology. It is shown to have all the good properties of buck and boost power stages alone, without acquiring any of their bad properties. It is this connection from which a new optimum topology switching converter is developed in Part IV.

Let us, however, before actually going into the various detailed aspects of the cascade connections, review first the three common converters (buck, boost and conventional buck-boost) to provide proper motivation for this investigation.

10.1 Three common converters revisited

A closer look at the topological structure of the three common converters (buck, boost, and buck-boost) shown in Fig. 1.1a reveals that all of them could be generated from the circuit model in Fig. 10.1.

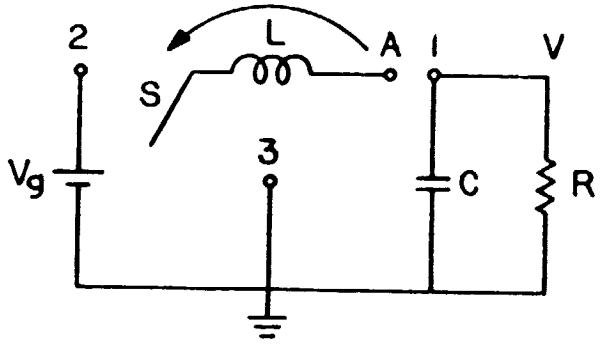


Fig. 10.1 Generation of the buck, boost, and buck-boost converters by cyclic rotation of the series connection of inductance L and switch S.

As seen in Fig. 10.1 a cyclic counterclockwise rotation of the series connection of inductance L and switch S between the input port (source voltage V_g) and the output port (parallel combination of C and R) generates respectively the three converters of Fig. 1.1a. Namely, when inductance node A coincides with node 1 and the switch S operates between the other two nodes (2 and 3), the buck power stage is generated. However, if the series connection of L and S is rotated such that A now coincides with node 2, while switch S operates between other two nodes (1 and 3), the boost converter

results. The only remaining possibility is that A coincides with node 3 which is, of course, the conventional buck-boost converter. This then exhausts all the possibilities of placing the series connection of L and S between input and output nodes (three terminal network, hence only three nodes).

This at the same time exhausts all the ways in which inductance is used as an energy transferring device between the input and output ports: either solely in the input circuit, solely in the output circuit, or connecting them. It is then no surprise that the basic dc conversion functions for these three converters are different from each other, both qualitatively and quantitatively as was demonstrated in previous chapters. For example, one only reduces the input voltage (buck), the other increases (boost), while only buck-boost is capable of the general conversion function (increase or decrease of input voltage).

These dc conversion properties and the method of generation of these converters depicted in Fig. 10.1 tend to suggest that all three converters are completely independent of each other, and are nonlinear circuits in their own right. This is probably why they are often referred to as "basic" power stages, meaning they cannot be derived from each other by some sequence of well-defined steps.

However, they are not so unrelated and independent as it may seem at first sight, since a strong correlation exists among their

basic dc conversion relations. Namely, the ideal dc gain for the buck-boost converter $V/V_g = D/D'$ is just the product of the dc gains for the buck ($V/V_g = D$) and boost converter ($V/V_g = 1/D'$). The same fact can also be observed in the basic circuit models of Fig. 3.8 (with $R_\ell = R_c = 0$) which are also valid at dc. For the buck-boost converter, the first ideal 1:d transformer effectively reduces the input dc voltage (buck), while the second d':1 transformer increases (boost) the resulting voltage and leads to d/d', or D/D' for the overall dc gain. From the other two converter models in Fig. 3.8 it appears as though the buck-boost converter model is just their simple merger. In fact, it becomes obvious that the same dc gain would be achieved by cascading the buck power stage with the boost power stage. Let us therefore investigate in more detail this particular connection.

7.2 Buck converter cascaded by a boost converter

When the buck power stage is cascaded by the boost power stage the converter in Fig. 10.2 is obtained. In Fig. 10.2 switching action is represented by the ideal switches S_1 and S_2, which can be replaced by the bipolar transistors and diodes by use of Fig. 1.1b. Here ideal switches are used to facilitate discussion and enhance the converter topology. For the same reason we assume that the two

switches S_1 and S_2 operate synchronously, such that only two switched networks are distinguished: one for interval DT_s when both switches are at position 1 and the other for interval $D'T_s$ when they are at position 2. In other words, the circuit operates as a two-state converter (hence also in the continuous conduction mode). Note that even though the first buck power stage does not contain explicitly the load R, it is effectively loaded by the dc input resistance $R_i = R/M^2$ to the second, boost power stage.

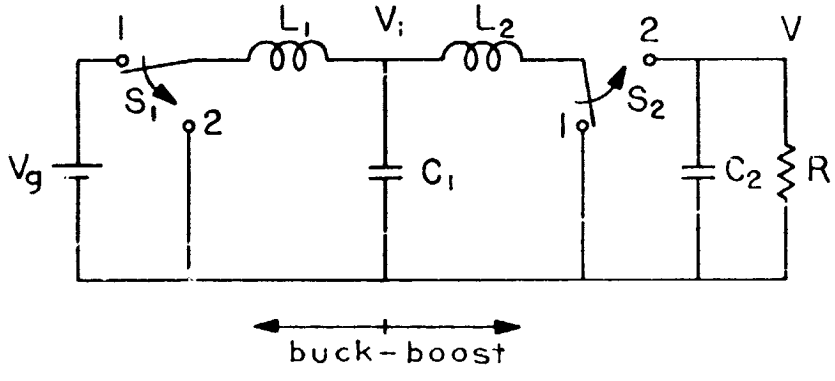


Fig. 10.2 Buck power stage cascaded by the boost power stage.

An interesting observation about the energy transferring mechanism of the converter in Fig. 10.2 can now be made. The T shaped network consisting of storage elements L_1, L_2 and C_1 is, through the switching action, first <u>completely</u> switched into the input network (to source voltage V_g), and then during the subsequent interval $D'T_s$ <u>completely</u> transferred to the output network thus feeding the load R with the energy stored in the previous interval. Hence in

this converter the energy transferring role is assigned to the complete T network (L_1,C_1,L_2) while in the conventional buck-boost this role belonged to the single inductor. We have here, therefore, the case of mixed energy transferring mechanism consisting of both inductive and capacitive energy storage.

By use of the technique described in Part I, the basic circuit averaged model of the converter in Fig. 10.2 is obtained as shown in Fig. 10.3.

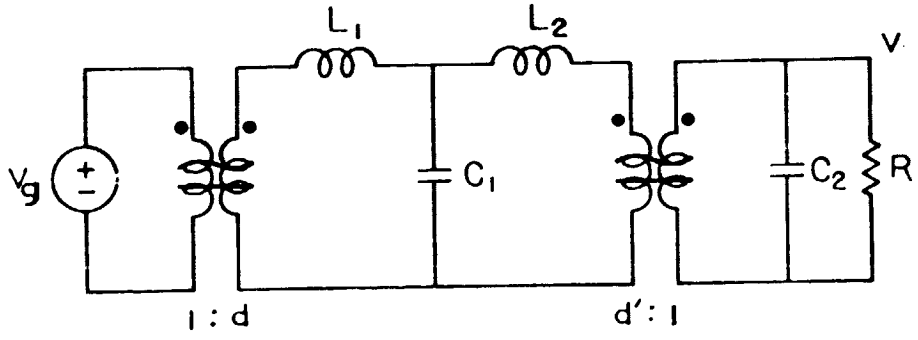


Fig. 10.3 Basic circuit averaged model for cascade connection of buck and boost converter shown in Fig. 10.2.

From the circuit model in Fig. 10.3 the dc conditions are obtained as usual by considering the inductances short and capacitances open, and hence the converter dc gain D/D' and noninverting property are easily established.

Since the capacitance C_1 does not affect the dc conditions let us now simplify the converter in Fig. 10.2 by simply taking it out of the circuit (or $C_1 = 0$) to obtain the converter in Fig. 10.4a.

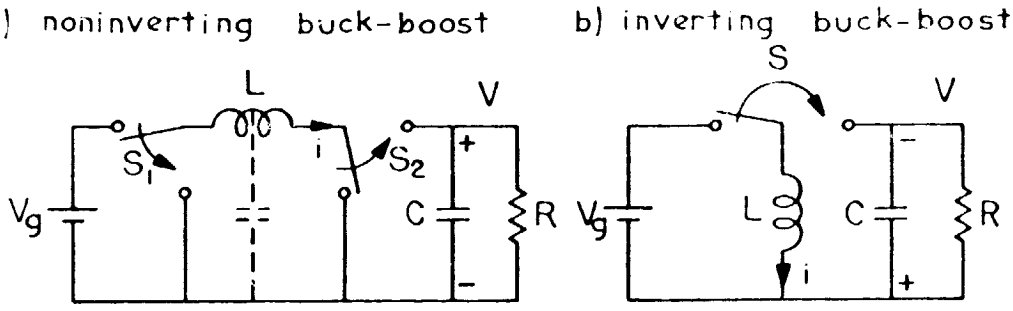


Fig. 10.4 Reduction of the two switches S_1 and S_2 in the noninverting converter in a) to a single switch S in the corresponding inverting converter (conventional buck-boost) in b).

A significant simplification has been achieved, since the original converter of Fig. 10.2 with <u>four</u> storage elements has been transformed to the converter of Fig. 10.4a with only two storage elements, and yet the basic dc conversion relations are preserved. The mixed energy transferring network (L_1,C_1,L_2) has been reduced to a single inductance with $L = L_1+L_2$. This then stresses the importance of <u>the way</u> in which the energy storage network is switched between input and output circuits in determining the dc conversion relation, and diminishes the importance of the particular storage element content. In essence, we have achieved the same basic dc conversion function but with a smaller number of storage components (only two) and simpler dynamics, when this special choice (C_1=0) is used in the general cascade connection of the buck and boost power stages. With this specific choice, the circuit model in Fig. 10.3 becomes the same as that in Fig. 3.8c (with $R_\ell = R_c = 0$) for the conventional buck-boost converter except for the difference in polarity of the second d':1 ideal transformer.

Even though the obtained converter in Fig. 10.4 is already greatly simplified, let us see if it can be still further reduced. Namely, the converter in Fig.10.4a still has two switches which in terms of hardware realizations with transistor and diodes means higher switching and dc losses, hence lower efficiency. The important question then becomes how these two switches could be reduced to a single one, and yet the dc conversion properties preserved.

As seen in Fig. 10.4a, inductor L appears to be "floating" and switching action (through S_1 and S_2) periodically grounds one and then the other inductor lead, thus producing an output voltage of positive polarity. If one of the inductor leads is grounded as in Fig. 10.4b, then single switch S performs the same action as previously S_1 and S_2, except that now inversion of the output voltage is obtained. Therefore, if one is willing to sacrifice the noninverting property of the converter in Fig. 10.4a, the reduction of two switches S_1 and S_2 to a single switch S can be achieved as illustrated in Fig. 10.4b. In fact, the converter in Fig. 10.4b is the conventional buck-boost converter.

This has now brought us to an important conclusion: the conventional buck-boost converter is not an independent circuit, but rather may be considered as a special case of the cascade combination of the buck and boost power stage (special case with $C_1 = 0$) in which the inversion of output voltage allowed reduction of the number of switches to one. This then leaves the other two converters, the buck and boost power stages, to be considered as the only really basic power stages, since the buck-boost converter could be derived from

them by following the aforementioned sequence of steps.

Note, however, that this sequence of steps is not to be understood in the usual linear circuits and linear dependence sense. Namely, even though the cascade combination in itself is a linear combination (provided the elementary circuits themselves are linear), the circuit elements here (buck and boost converter) are extremely nonlinear as also is their cascade connection. However, this difference is alleviated since we are using linear circuit models for both dc and ac small-signal models of the converters, as presented in the previous two parts. It is therefore the last step, that of replacing a number of switches for the inverting property of the converter which is highly nonlinear (and, of course, cannot be linearized!), which distinguished this process from the conventional linear equivalent circuit transformation steps, for example. However, despite that, the linear circuit models (both dc and ac small-signal) of the two converters in Fig. 10.4 are the same (compare the model in Fig. 10.3 for $C_1 = 0$, with that of Fig. 3.8c with $R_\ell = R_c = 0$) except one is inverting while the other (Fig. 10.3) is not. This may even appear to be a general result (of course assuming that all the switches are ideal, zero on resistance and infinite off resistance).

This view of the conventional buck-boost converter being just a special case of one kind of cascade connection of buck and boost converters, as opposed to the conventional view of Section 10.1, might seem artificial at present. Nevertheless, this view is later shown to be a very fruitful one, since it led naturally to the discovery of the new optimum topology switching converter and completion

of the general theory of buck-boost converters.

As seen in Fig. 10.2, the cascade connection of buck and boost converters provided a variety of converters (for different values of energy storage elements L_1, L_2, C_1), not just one for the special choice $C_1=0$, and each of them realized a general buck-boost dc conversion function. However, the particular choice $C_1=0$ had the desirable feature that it could be reduced to the single-switch circuit by sacrifice of its originally noninverting property for the inverting one, which still further simplifies the complexity of the converter.

It may seem now that with this conventional buck-boost converter, the ultimate goal of optimum topology (minimum complexity with maximum performance) has been achieved. This is, however, not so since the conventional buck-boost converter has two very important drawbacks. It has been demonstrated in Chapter 1 that the conventional buck-boost converter has both input and output currents pulsating (see Fig. 1.8, for example), which further cause severe EMI (electromagnetic interference) problem and significantly large output voltage ripple compared to the buck power stage (which has continuous, nonpulsating output current). But, this was to be expected. Namely, at the very beginning, the cascade connection of the buck power stage first, followed by the boost power stage (Fig. 10.2) combined only the bad properties of the two original converters: the pulsating input current of the buck converter and the pulsating output current of the boost converter. To alleviate these problems, one usually resorts to a one-two-section input filter to smooth out the input

current ripple, and larger output capacitance to reduce the increased output voltage ripple.

But there is a much better and more elegant method to resolve these performance degradation problems. Note that all the possibilities of producing the general dc-to-dc conversion function (both increase or decrease of dc input voltage) have not been exhausted by combination of the buck and boost converters. Namely, we can put the boost power stage first and then cascade it by the buck power stage, and still produce the same dc conversion function. In this way, the good properties of both of the two elementary converters are combined: the continuous input current of the boost converter and the continuous output current of the buck converter. Let us investigate this possibility.

10.3 Boost converter cascaded by buck converter

By cascading the boost power stage with buck power stage, the converter in Fig. 10.5 is obtained.

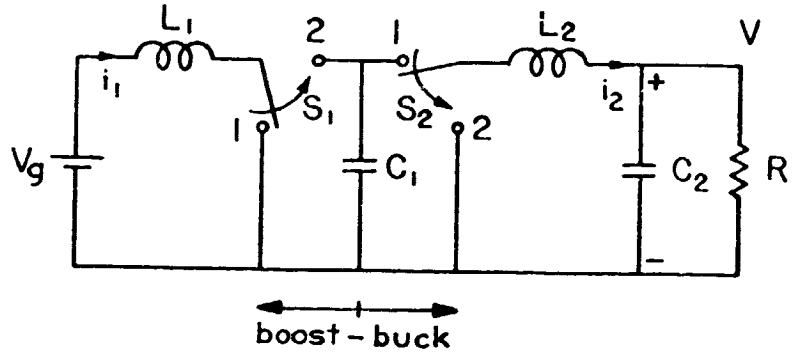


Fig. 10.5 Boost power stage cascaded by a buck power stage .

Again, as before, the two switches S_1 and S_2 operate as for the two-state converter: one switched network is generated with switches in position 1 (for interval DT_s) and the other in position 2 (for interval $D'T_s$). This converter will be referred to as a boost-buck noninverting converter, in distinction to the converter of Fig. 10.4 which will be termed the buck-boost noninverting converter.

Let us now see how the energy transferring mechanism is affected by this particular choice of cascade connection. As seen in Fig. 10.5 the switches S_1 and S_2 are now embedded inside the T-shaped network consisting of L_1, L_2, and C_1, while in the buck-boost configuration (Fig. 10.2) they are outside of this T network of storage elements. It now becomes obvious that the capacitance C_1 is the only energy

transferring device. Namely, during the interval $D'T_s$ the capacitance C_1 enters the input circuit (series connection of source voltage and inductance L_1) and accumulates energy in the form of stored charge. For the subsequent interval DT_s, capacitance C_1 is completely transferred to the output circuit to which it then releases the energy stored in the previous interval. Therefore, in distinction with the previous two cases, we have now a purely capacitive energy transfer, since a single capacitance has taken the role of the energy transferring network, as did the single inductance in the conventional buck-boost converter employing purely inductive energy transfer.

It is now clear that we cannot simplify the energy transferring network in this case, (as we did for buck converter cascaded by the boost converter (Fig. 10.2)), since it is already in the simplest possible form, consisting of a single storage element, capacitance C_1. Therefore we cannot reduce the number of storage elements as we could before and all four storage elements are necessary.

However, in order to make a fair comparison, we compare this converter with the buck-boost converter of Fig. 10.4a to which an input LC filter has been added. Then, both converters have the same number of storage elements (four) and the same number of switches. From the performance standpoint, both possess a continuous input current (because an input filter was added to the converter in Fig. 10.4a) similar to that shown in Fig. 1.5b. However, the boost-buck converter of Fig. 10.5 also has continuous output current, and thus significantly lower switching ripple voltage for the same storage elements, than does the converter of Fig. 10.4a with added input filter (see comparison in Section 1.3).

In conclusion, the boost-buck converter of Fig. 10.5 retains the good input properties of the boost converter and the good output property of the buck converter, which to a large extent offset its higher complexity in having four storage elements. In addition, in the next chapter on modelling and experimental verification of this converter, it will be shown that even its frequency response resembles the desirable characteristic of the buck converter, and not the quite undesirable frequency response of the boost power stage (which has a right half-plane zero).

Let us now review the various forms the energy transferring network, consisting of storage elements only (inductors and capacitors), can take in order to realize the general buck-boost dc conversion function.

10.4 Energy transfer principles for general dc conversion

The general dc conversion function (both increase and decrease of input dc voltage) can be achieved by switching the storage element network (consisting of inductances and capacitances only) between the input and output circuit as illustrated in Fig. 10.6.

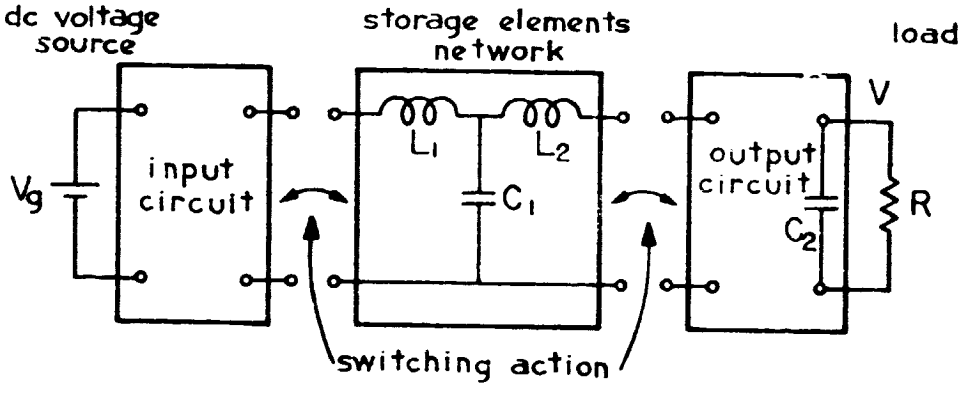


Fig. 10.6 Energy transferring networks and mechanism for general (buck-boost) dc conversion.

It was demonstrated in previous sections that for achieving the general dc conversion function, the particular storage-element content of the energy transferring network is not so important as the <u>way</u> the complete network is switched between input and output circuits: being <u>completely</u> in the input circuit during one interval (DT_s), and then <u>completely</u> in the output circuit during the subsequent interval. Hence, ideally at no time is it connecting the input and output circuits. This is in clear distinction with the ordinary buck and

boost power stages in which the energy transferring network connects the input and output circuits for a portion of the switching period.

In Fig. 10.6 the energy transferring network employs both inductive and capacitive energy storage, an example of which is the buck-boost converter of Fig. 10.2. However, if $C_1=0$, purely inductive storage and energy transfer takes place as in the converters of Fig. 10.4. Finally, when $L_1 = L_2 = 0$, purely capacitive energy transfer is employed as in boost-buck converter of Fig. 10.5.

It seems now appropriate to compare the inductive energy transfer principle which is used in all so far known converters (such as the Weinberg, Venable, and a number of others), with the capacitive energy transfer principle first encountered in the boost-buck converter of Fig. 10.5. While in the first kind the energy is accumulated in the inductor in the form of a magnetic field, in the second the energy is stored on the capacitor in the form of an electric field. We can now compare easily their storage capabilities. Electrostatic energy stored in capacitance C with voltage V is $E_c = CV^2/2$, while the electromagnetic energy stored in inductor L with current I is $E_L = LI^2/2$. For example, for C = 1μF and V = 50V, E_c = 1.25mJ, while for L = 2.5mH and I = 1A, E_L is also E_L = 1.25 mJ. However, the physical size and weight of a 1μF, 50V capacitor is negligible compared to those of a 2.5mH, 1A inductor. Therefore, capacitive energy storage has much better storage capability per unit size or weight than does inductive energy storage. This becomes of prime importance for switching converters, since their weight and size reduction is sometimes the primary goal (aerospace applications, for example).

Let us now summarize the main results of this chapter. First, it has provided a different and unconventional view of the three "basic" converters (Fig. 10.1). Then, the useful generic properties of the cascade connection of buck and boost power stages led to a better understanding of the energy transferring mechanism through various storage element networks. At the same time, the conventional buck-boost converter was viewed as merely a special case of the particular cascade connection by observing an important fact: the number of switches of the noninverting converter (Fig. 10.4a) can be reduced to one, if output voltage inversion is allowed (Fig. 10.4b), without even changing the dynamics (ac small-signal model).

While in this chapter the cascade connection was assumed to operate as a two-state converter, this is by no means a requirement. For example, it is illustrated in Appendix D (Figs. D.1 and D.2) that the boost-buck converter (Fig. 10.5) can under appropriate driving conditions (switches S_1 and S_2 out of synchronism) act as a three-state or even a four-state converter. In addition, while we have considered only the cascade combinations which would produce the general buck-boost dc conversion function (from nongeneral buck and boost functions), one might study the other combinations as well (buck-buck, boost-boost, buck-conventional buck-boost and so on). However, for all the other combinations to become useful, they have to be related to a rather specialized problem. Just recently and concurrently with this work, such cascade connections have been studied for the first time ([21] and [22]) but in a quite different context, in connection with one specialized problem-reduction of the surge current in switching regulators for color television applications.

Since the boost-buck converter of Fig. 10.5 was judged to have more promising performance than the buck-boost converter of Fig. 10.2, we pursue in the next chapter the modelling of that particular converter, following the modelling procedures of Part I, and verify some of the general predictions made earlier in Part I.

CHAPTER 11

MODELLING AND EXPERIMENTAL VERIFICATION OF CASCADED BOOST-BUCK CONVERTER

In this chapter, the general predictions made available by the derivation of the canonical circuit model in Part I (Chapter 4) are confirmed on the model of the boost-buck noninverting converter (Fig. 10.5). It is demonstrated that the current generator $j(s)\hat{d}$ in the canonical circuit model (Fig. 4.2) of this converter contains a single right-half plane zero, while the voltage generator $e(s)\hat{d}$ has two complex zeros (second order frequency dependent polynomial) in complete agreement with the general predictions. In addition, the effective low-pass filter network is now of fourth order, with the effective filter elements being again dependent on the steady-state duty ratio D.

This boost-buck noninverting converter is also a very good example of the generalized switching converter (Section 1.5) with more storage elements (four) and more switches (two) than the common converters of Fig. 1.1. Its model derived in this chapter for continuous conduction mode by use of both circuit and state-space averaging technique, illustrates the general applicability of the modelling techniques presented in Part I. Even its model in the discontinuous conduction mode could be easily obtained, as was suggested at the end of Chapter 6.

This chapter concludes with the experimental verifications of the dc and ac small-signal models of this converter, which once again confirm the high accuracy of the presented modelling techniques.

11.1 Modelling of the boost-buck noninverting converter

Since we assume that the converter in Fig. 10.5 is operating as a two-state converter (continuous conduction mode), the two switched networks of Fig. 11.1 are obtained.

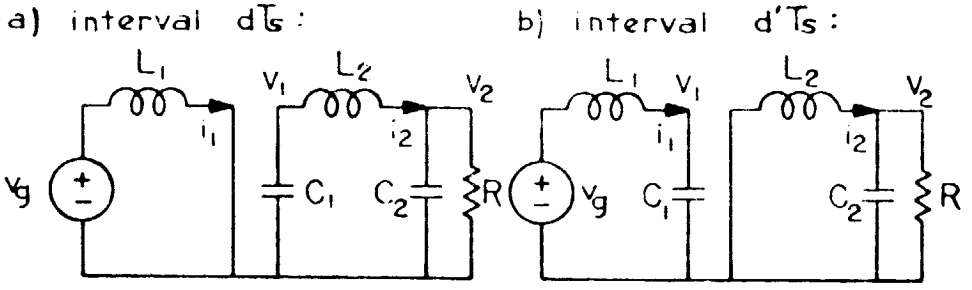


Fig. 11.1 Two switched circuit models of the boost-buck converter in Fig. 10.5.

By use of the converter description in Fig. 11.1 and the hybrid modelling or the circuit averaging technique of Part I, the basic circuit averaged model of this converter results as shown in Fig. 11.2.

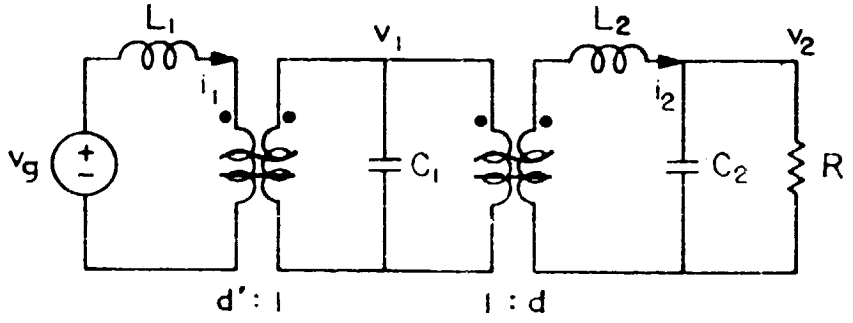


Fig. 11.2 Basic circuit averaged model of the boost-buck converter in Fig. 10.5.

The usual perturbation and linearization steps lead to the linear circuit model (both dc and ac small-signal) of this converter in Fig. 11.3.

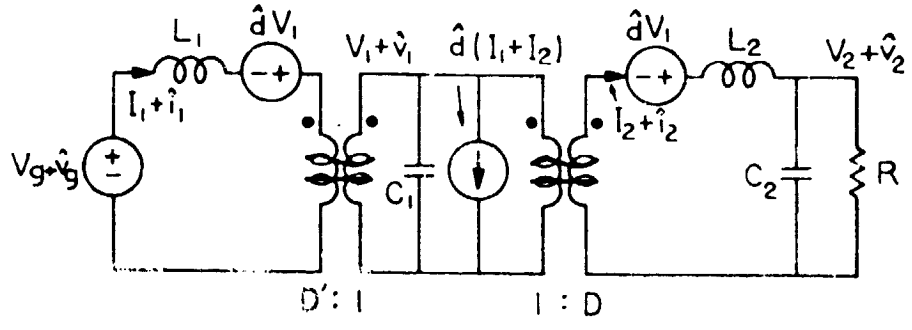


Fig. 11.3 Linear circuit model (both dc and ac small-signal) of the boost-buck converter in Fig. 10.5.

From the circuit model in Fig. 11.3 one can easily obtain the complete dc relations as

$$\frac{V_2}{V_g} = \frac{D}{D'}, \quad \frac{V_2}{V_1} = D, \quad \frac{I_2}{I_1} = \frac{D'}{D}, \quad \frac{V_2}{I_2} = R \tag{11.1}$$

By use of the equivalent circuit transformations and with help of dc relations (11.1), the circuit model of Fig. 11.3 can be transformed into the canonical circuit form shown in Fig. 11.4.

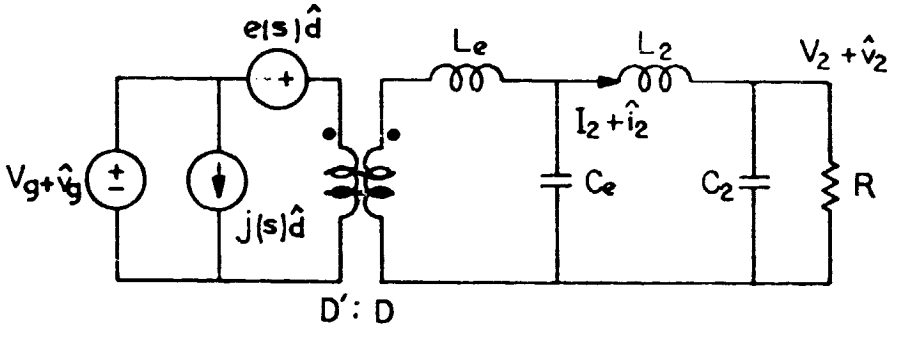


Fig. 11.4 Canonical circuit model of the boost-buck converter in Fig. 10.5 with none of the parasitic elements included.

The element values in Fig. 11.4 are defined as

$$L_e = \left(\frac{D}{D'}\right)^2 L_1; \qquad C_e = \frac{C_1}{D^2} \tag{11.2}$$

$$e(s) = \frac{V_2}{D^2}\left(1 - s\frac{L_e}{R} + s^2 L_e C_e D'\right) \tag{11.3}$$

$$j(s) = \frac{V_2}{D'^2 R}(1 - sC_e RD') \tag{11.4}$$

Let us now discuss the significance of this result. First, the effective filter network consists of <u>two low-pass</u> LC filter sections, whose element values are now duty ratio dependent as seen in

(11.2). Second, for the first time in the configurations considered in this work, frequency dependence appears in the current generator $\hat{jd}$ (11.4), while the voltage generator (11.3) exhibits a second order frequency dependence in contrast to the first-order dependence in some of the previous converter examples. Both of these results, (11.3) and (11.4), directly confirm modelling predictions made possible by the canonical circuit model formulas (4.5).

As a matter of fact, the canonical circuit model of Fig. 11.4 could have been obtained directly by use of these formulas in a way analogous to that for the buck-boost example of Chapter 4. The only difference is that now the matrices A_1 and A_2 are of the fourth order, and are obtained from the switched networks in Fig. 11.1 as

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 \\ 0 & \frac{1}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \tag{11.5}$$

with the corresponding vector definition $x^T = (i_1\ v_1\ i_2\ v_2)$. Therefore, by use of (11.5) in (3.14) to find the transfer functions required by (4.5), the two generators are directly determined, while the transformer turns ratio $\mu = D'/D$ is obtained from (4.6). Note, however, that from (4.5) we will actually obtain the transfer function $H_e(s)$ of the effective filter network, rather than the network itself. Synthesis procedure [10] for realization of a ladder type network

structure from its transfer function description could then be used to obtain the effective low-pass filter network as in Fig. 11.4.

However, if frequency response is desired, $H_e(s)$ and $e(s)$ are needed to find the open-loop transfer functions G_{vg} and G_{vd}. By applying either this general procedure, or from the circuit model in Fig. 11.4, we obtain

$$H_e(s) = \frac{1}{P(s)} \tag{11.6}$$

where

$$P(s) = 1 + \frac{L_e+L_2}{R} s + (L_eC_e+L_2C_2+L_eC_2)s^2 + \frac{C_eL_eL_2}{R} s^3 + L_eC_eL_2C_2s^4 \tag{11.7}$$

It is now of some practical interest (as will be demonstrated on the experimental test circuit) to find what conditions should be satisfied that this 4th order polynomial can be <u>analytically</u> separated in terms of two second-order polynomials.

Suppose now that $P(s)$ is approximated by the product of two second order polynomials as

$$P(s) = (1 + \frac{L_e}{R} s + L_eC_es^2)(1 + \frac{L_2}{R} s + L_2C_2s^2) \tag{11.8}$$

Comparison of (11.7) and (11.8) reveals that (11.7) is well approximated by (11.8) if the following inequality conditions are satisfied

$$C_e \gg C_2$$

$$C_e \gg L_2/R^2 \tag{11.9}$$

If, in addition, the inductances L_e and L_2 are of the same order of magnitude, the two pairs of complex poles of $H_e(s)$ resulting from (11.8) are <u>well separated</u>, with their respective corner frequencies and Q factors given by

$$f_{c1} = \frac{1}{2\pi\sqrt{L_e C_e}}, \qquad Q_1 = \frac{R}{\omega_{c1} L_e}$$

$$f_{c2} = \frac{1}{2\pi\sqrt{L_2 C_2}}, \qquad Q_2 = \frac{R}{\omega_{c2} L_2} \tag{11.10}$$

Therefore, if the conditions (11.9) are met, the frequency response of the open-loop transfer functions G_{vg} and G_{vd} can be easily sketched by inspection with the help of (11.10), since the two pairs of complex poles of (11.6) are well separated.

Note that the switching action now introduces into the duty ratio to output transfer function G_{vd} a pair of complex zeros given by (11.3), in addition to the poles of the effective filter network $H_e(s)$ given by (11.8), since $G_{vd}(s) = e(s)\, G_{vg}(s)$. Moreover, the complex zeros are in the <u>right half-plane</u>, owing to the <u>negative</u> linear term in s in e(s) given by (11.3). This should be compared with the single real <u>right half-plane</u> zero for the conventional buck-boost converter (see (4.9) for example).

As discussed in Part I, even only a single right half-plane zero (nonminimum phase network) poses significant problems in stabilizing the loop gain T, which directly depends on this open-loop transfer function $G_{vd}(s)$ as seen in (5.2). Then, the complex pair in the right half-plane would even more enhance this problem.

Nevertheless, for practical applications the situation is not so unfavorable as it may look at first sight. Namely, in the model of Fig. 11.4 the inductances have been considered ideal, and their parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ which are always associated with them have not been included. These parasitic resistances, however, being

the only dissipative elements besides load R, can significantly affect converter properties. It has been demonstrated earlier (Fig. 3.3) that they can have a profound effect upon the dc properties; here, besides confirmation of the same effect for dc properties, their positive (stabilizing) effect upon the ac properties will be demonstrated.

The inclusion of the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ is easily incorporated in the previously outlined modelling procedure, and leads to the canonical circuit model of Fig. 11.5.

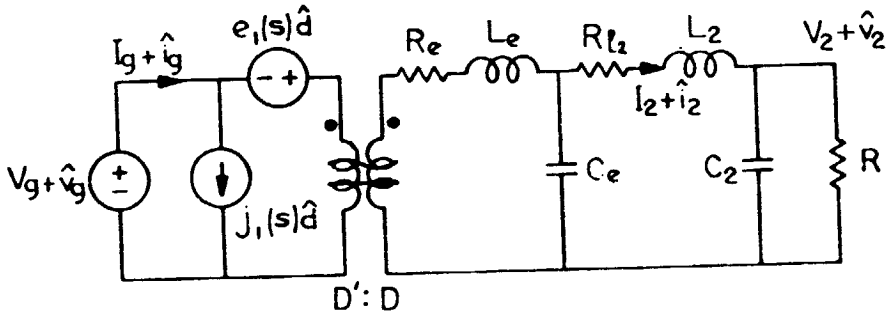


Fig. 11.5 Canonical circuit model of the boost-buck converter in Fig. 10.5 with the series parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ of the two inductors included.

The element values in Fig. 11.5 are defined as

$$R_e = \left(\frac{D}{D'}\right)^2 R_{\ell 1}, \qquad L_e = \left(\frac{D}{D'}\right)^2 L_1, \qquad C_e = \frac{C_1}{D^2} \tag{11.11}$$

$$e_1(s) = \frac{V_2}{D^2}\left\{1 + \frac{R_{\ell 2}-R_e}{R} - s\left[\frac{L_e}{R} - R_e C_e D'\left(1+\frac{R_{\ell 2}}{R}\right)\right] + s^2 L_e C_e D'\left(1+\frac{R_{\ell 2}}{R}\right)\right\} \tag{11.12}$$

$$j_1(s) = \frac{V_2}{D'^2 R}\left\{1 - s\, C_e R D'\left(1+\frac{R_{\ell 2}}{R}\right)\right\} \tag{11.13}$$

From the circuit model in Fig. 11.5 and by use of (11.11) the dc voltage gain, which now includes the effect of parasitics, is obtained as

$$\frac{V_2}{V_g} = \frac{D}{D'} \frac{1}{1 + \frac{R_{\ell 1}}{R}\left(\frac{D}{D'}\right)^2 + \frac{R_{\ell 2}}{R}} \tag{11.14}$$

while similarly as before, the dc current gain is not affected and remains

$$\frac{I_2}{I_g} = \frac{D'}{D} \tag{11.15}$$

thus leading to the efficiency η defined by

$$\eta = \frac{1}{1 + \frac{R_{\ell 1}}{R}\left(\frac{D}{D'}\right)^2 + \frac{R_{\ell 2}}{R}} \tag{11.16}$$

The dc voltage and current gain dependence on duty ratio D is shown in Fig. 11.7.

Let us now examine more closely what consequences the inclusion of parasitics has upon the frequency response. Since the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ are in reality small compared to load R, that is

$$R_{\ell 1} << R, \qquad R_{\ell 2} << R \tag{11.17}$$

their effect upon the position of the two corner frequencies f_{c1} and f_{c2} is negligible and they are still very accurately predicted by (11.10). However, their Q factors will be appreciably affected. The same is true for the numerator polynomial $e_1(s)$ which is under (11.17) approximated by

$$e_1(s) \simeq \frac{V_2}{D^2}\left[1 - s\left(\frac{L_e}{R} - R_e C_e D'\right) + s^2 L_e C_e D'\right] \tag{11.18}$$

As seen from (11.18) two complex zeros of $e_1(s)$ can now become left half-plane zeros if the following condition is met:

$$\frac{L_e}{R} - R_e C_e D' < 0 \tag{11.19}$$

Therefore, owing to the corrective term $R_e C_e D'$ originating from the parasitic resistance $R_{\ell 1}$, the frequency response may be qualitatively changed to a minimum phase frequency response and stabilization problems substantially reduced. This is, however, what should have been expected, since the input series resistance $R_{\ell 1}$ effectively adds more damping to the converter.

As before, the corner frequency remains virtually unaffected and the same as in (11.3), that is

$$f_{z1} = \frac{1}{2\pi\sqrt{L_e C_e D'}} \tag{11.20}$$

Comparison of (11.20) and (11.10) now shows that complex zeros at f_{z1} almost completely cancel the influence of complex poles at f_{c1}, since they are very little separated ($f_{z1} = f_{c1}/\sqrt{D'}$), thus giving a second-order response with effective complex poles at f_{c2} for the G_{vd} transfer function (see computer generated graph in Fig. 11.9). Note also that the first pole at f_{c1} is dependent on duty ratio D, since $L_e C_e = L_1 C_1 / D'^2$, while the pole at f_{c2} is not.

Therefore, once again it is confirmed that this converter (Fig. 10.5) has acquired the desirable dynamic properties of the buck converter in having second-order behavior with corner frequency $f_{c2} = 1/2\pi\sqrt{L_2 C_2}$ independent of duty ratio D, and in not having any

right half-plane zeros as do the boost and buck-boost converters. Nevertheless, the line to output transfer function is still of the fourth order (Fig. 11.8) giving an excellent audio-susceptibility characteristic. Thus, this converter has a very desirable frequency response, which is easy to stabilize once the feedback loop is closed in switching regulator applications.

Let us now confirm these theoretical analytical predictions with exact computer generated dc gain and frequency plots, and with experimental data obtained from the test circuit.

11.2 Experimental verification of the modelling predictions

A boost-buck noninverting switching converter (Fig. 10.5) was constructed as shown in Fig. 11.6 with the following switching elements: transistors 2N2880 and diodes TRW 7342. Since series parasitic resistances have been shown to have a profound effect upon the converter characteristics, they are measured and included in the model (and circuit description in Fig. 11.6 as well).

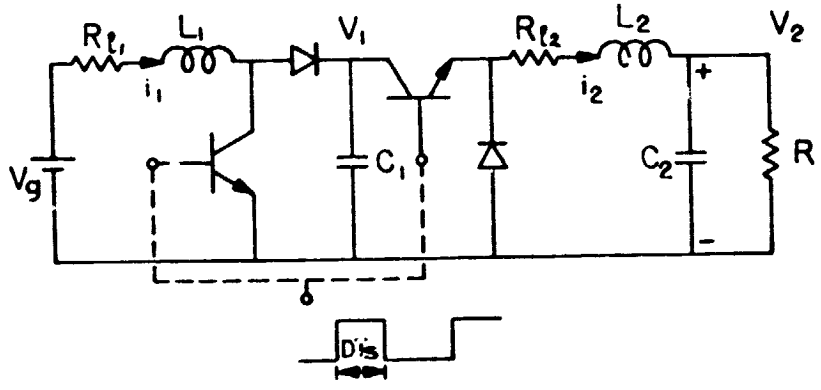


Fig. 11.6 Experimental test circuit for the boost-buck converter of Fig. 10.5.

Two separate "floating" switch drive circuits are used to drive the two transistors in synchronism with the same duty ratio D (and switching frequency f_s as well), as indicated in Fig. 11.6 by dotted lines.

For purpose of experimental verification the following values were used:

$$\begin{aligned} V_g &= 5V, & R_{\ell 1} &= 1.0\Omega, & L_1 &= 3.5mH, \\ C_1 &= 100\mu F, & f_s &= 40kHz, & R_{\ell 2} &= 0.4\Omega, \\ L_2 &= 6.5mH, & C_2 &= 0.47\mu F & R &= 75\Omega \end{aligned} \qquad (11.21)$$

Note that for these experimental values, the converter operates in the continuous conduction mode (for the range of duty ratios D involved), as can easily be checked using the results of Part II (Section 8.3). Hence it will behave as a two-state converter, and the modelling results of Part I and Section 11.1 apply.

DC gain measurements

First, the dc conditions are verified. By use of experimental values (11.21) in (11.14) and (11.15), both dc voltage and current gain are plotted as a function of duty ratio D via a computer program DCGAIN, as shown in Fig. 11.7.

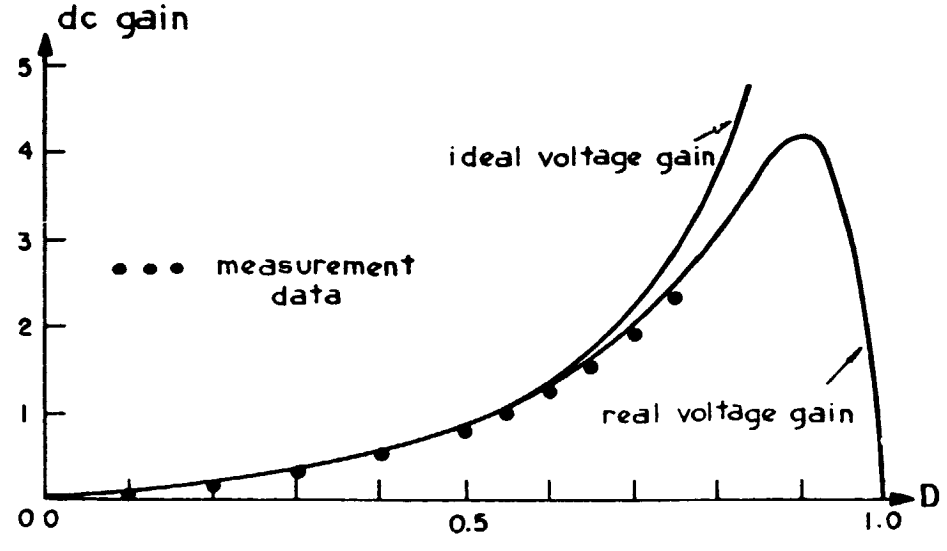


Fig. 11.7 Theoretical and experimental dc gain characteristics of the boost-buck converter of Fig. 11.6.

As seen in Fig. 11.7, the experimental data for the dc voltage gain measured on the circuit of Fig. 11.6 are in good agreement with the theoretical predictions.

Frequency response measurements

For ac small-signal frequency measurements, the steady-state operating point was chosen to be at D = 0.5. With this and definitions (11.1), inequality conditions (11.9) become 400μF >> 0.47μF and 400μF >> 1.15μF respectively, and are well satisfied. Hence the two pairs of complex poles are well-separated and can be calculated from (11.10) as

$$f_{c1} = 133\text{Hz}, \qquad f_{c2} = 2.8\text{kHz} \tag{11.22}$$

The condition (11.19) for complex zeros to be in the left half-plane is also satisfied since $L_e/R - R_e C_e D' = -154\mu\text{sec}$ is negative, and its corner frequency f_{z1} given by (11.20) becomes

$$f_{z1} = 190\text{Hz} \tag{11.23}$$

The computer program NEW was used to generate the exact frequency response for line transfer function G_{vg} obtained from Fig. 11.5, and is plotted in Fig. 11.8 by use of experimental values in (11.21). As seen in Fig. 11.8, the two pairs of complex poles are well-separated (more than a decade apart) and the corner frequencies obtained from the plot agree very well with their computed estimates (11.22).

The same computer program was then used to plot the duty ratio modulation transfer function $G_{vd} = e_1(s)G_{vg}$ as shown in Fig. 11.9.

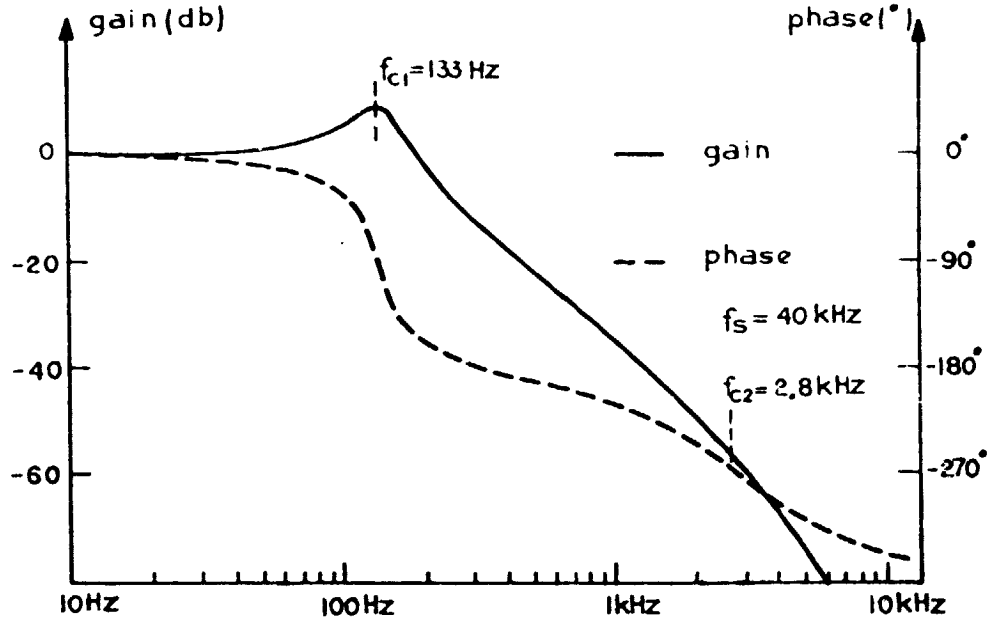


Fig. 11.8 Theoretical magnitude and phase frequency response of the line transfer function $G_{vg} = \hat{v}/\hat{v}_g$ for the boost-buck converter of Fig. 11.6.

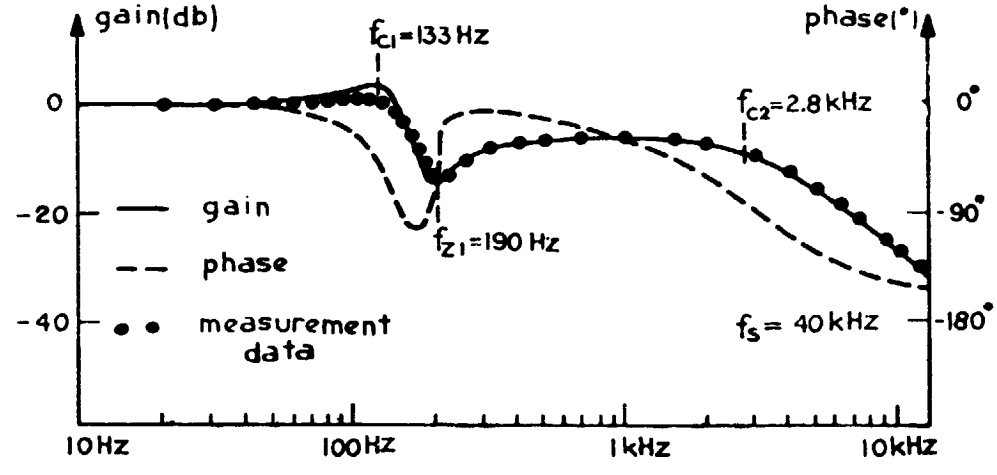


Fig. 11.9 Theoretical and experimental frequency response of the duty ratio modulation transfer function $G_{vd} = \hat{v}/\hat{d}$ for the boost-buck converter of Fig. 11.6.

As seen from the phase plot, the complex zeros are indeed in the left half-plane (minimum phase response) as was predicted by the satisfaction of inequality condition (11.19). In addition, the corner frequency f_{z1}, whose position is accurately predicted by (11.23), is indeed very close to f_{c1} and causes almost complete cancellation of their effects on both magnitude and phase characteristics. Note, however, that when the parasitic resistance $R_{\ell 1}$ is reduced from 1.0Ω to 0.2Ω, the inequality condition (11.19) is violated and the complex zeros become right half-plane zeros. This fact has also been confirmed on the phase response of G_{vd} by use of the same computer program NEW, but with $R_{\ell 1} = 0.2\Omega$.

Finally, the duty ratio modulation transfer function G_{vd} was measured using the familiar describing function measurements [20], and excellent agreement with the theoretical frequency response is observed (see Fig. 11.9).

In conclusion, this chapter has for the first time verified the prediction made by the general modelling method of Part I, that the current generator $j(s)\hat{d}$ in the canonical circuit model may also be frequency dependent, while the voltage generator $e(s)\hat{d}$ could have frequency dependence higher than the first order. None of the two events has occurred in modelling any of the previously known converters. Also it was demonstrated that the effective filter network is of low-pass nature (as postulated in Section 1.5 on generalized switching converters) and that it could be of higher order, four in this particular example.

Even though it seems that this fourth-order model is much more difficult to analyze than the corresponding second-order models

of converters in Fig. 1.1, it has been shown how, under the appropriate choice of circuit element values, the analytical analysis is considerably simplified and the favorable frequency response of the converter obtained.

Both dc transfer properties and ac small-signal frequency response for this particular design have been shown to be in very good agreement with experimental measurements made on the converter test circuit, thus verifying the high accuracy of the converter circuit model in Fig. 11.5 and the subsequent analysis results.

It is now appropriate to mention that the same procedure, outlined in this chapter, can be used to obtain the canonical circuit model of Fig. 11.4 or Fig. 11.5 for the buck converter cascaded by a boost converter (Fig. 10.2). Then the results for these two types of converters (Fig. 10.2 and Fig. 10.5) can be tabulated and used to supplement TABLE I (Chapter 4) with some more converter model examples.

The cascade connection of buck and boost converters becomes then fruitful for two very good reasons:

1) for modelling and analysis, it offered a converter topology more representative of the generalized switching converter (Fig. 1.11) and consequently resulted in converter models more general in nature .

2) in the study of converter topologies (how to interconnect the components of the generalized switching converter in order to form a useful dc conversion function), the generic properties of the cascade connection lead naturally to the discovery of the new optimum topology switching converter presented in Part IV, and to the completion of the general theory of buck-boost converters.

PART IV

NEW OPTIMUM TOPOLOGY SWITCHING CONVERTER

CHAPTER 12

DISCOVERY OF A NEW OPTIMUM TOPOLOGY SWITCHING CONVERTER

This Part IV represents a culmination of the investigations made in the previous three parts. Through the exceptional insights gained by the modelling techniques of Part I and II, and the canonical circuit models in particular, the outstanding generic properties of the cascade combination of power stages have been recognized in Part III and they all lead in a genuine way in this Part IV to the achievement of the ultimate goal -- the optimum topology switching dc-to-dc converter. Part IV is thus entirely devoted to the discovery of the new switching converter and consists of several major topics covered in three chapters.

First, the novel converter topology based upon capacitive rather than inductive energy transfer is conceived by reduction of the number of switches in the only other so-far known converter based upon the capacitive energy transfer (Fig. 10.5). The practical bipolar transistor-diode realization of the single switch leads to experimental verification of the converter operation.

Then, the new converter is extensively compared with a number of other known converters, and especially with the conventional buck-boost converter to which an input filter has been added. Both theoretical and experimental comparisons show the superior performance, higher efficiency, smaller size, lighter weight, and reduced switching ripple of the new capacitive energy transfer dc-to-dc converter. However, this is no surprise, since the new converter is

recognized to have the optimum topology, which realizes the maximum performance with minimum number of components.

Finally, several areas of investigation ar clearly designated. On the practical side of the technological implementation, they include various technological realizations of the switching action besides the conventional bipolar transistor and diode, and closed-loop regulator implementation using the recent state-of-the art integrated circuits with feedback control circuitry on a single chip. On the theoretical and modelling side, they include modelling of the new converter in the discontinuous conduction mode and, for closed-loop regulator applications, multiloop feedback control with several additional loops (three) to choose from besides the usual one involving the output voltage. Suitable modifications of the new converter are being sought to include the desirable isolation property and its corollary, the multi-output possibility.

This chapter, however, in addition to introduction of the novel converter topology, gives the exposition of the complete structure of all converters performing the buck-boost function, in which the new converter has filled in the missing element. An interesting method of generating the buck, boost and the new converter analogous, and in fact dual, to the one in Fig. 10.1 is also given. The chapter then concludes with the experimental verification of the canonical circuit model of the new converter.

12.1 Topological reduction of number of switches

We now recall that in a cascade connection where a buck power stage is followed by a boost power stage (Fig. 10.2), reduction of the number of storage elements to two is possible and results in the non-inverting converter of Fig. 10.4a. Moreover, it was demonstrated that further reduction of the number of switches from two in the converter of Fig. 10.4a to a single one in that of Fig. 10.4b (conventional buck-boost converter) is possible if inversion of the output dc voltage is allowed.

Then, it was concluded that the other cascade connection, a boost converter followed by a buck converter (Fig. 10.5), combines the good properties of both converters alone, unlike the first cascade connection. However , it was also determined that reduction of the number of storage elements is not possible in this otherwise favorable cascade connection, since the single capacitance performs the energy transferring role (Fig. 10.5). However, one fundamental question remained unanswered for this favorable cascade connection, and it is:

Is it possible to reduce the number of switches in the converter of Fig. 10.5 from two to one, and at the same time achieve inversion of the output dc voltage?

The answer to this question may be surprising, since it is affirmative as will now be demonstrated. The same question, when slightly rephrased, leads easily to the answer: we ask what actually should be done in the converter of Fig. 10.5 to cause inversion

of output dc voltage. Both boost and buck power stages are by themselves inherently noninverting and therefore the only way the output voltage could be inverted is that the switching action causes the polarity of the energy transferring capacitance C_1 to be inverted when presented to the output (buck) circuit, and then inverted back to positive polarity when in the input (boost) circuit. Therefore, if we concentrate only on the capacitance C_1 and the two switches S_1 and S_2 in the converter of Fig. 10.5, we quickly realize that the stated goal can easily be obtained as shown in Fig. 12.1.

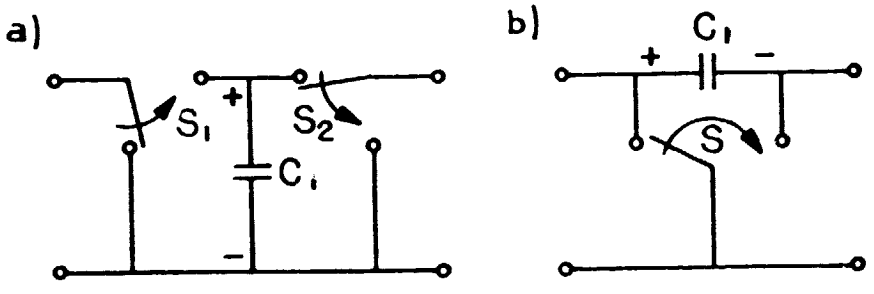


Fig. 12.1 Topological reduction of the number of switches:
a) two switches and noninversion of capacitance voltage
b) single switch and inversion of capacitance voltage

Hence, at the same time that the voltage polarity inversion of the capacitance C_1 is obtained, the reduction of the two switches S_1 and S_2 in Fig. 12.1a to a single switch S in Fig. 12.1b has been achieved.

In this capacitive energy transfer, the originally grounded capacitance C_1 and the two switches (Fig. 12.1a) have been transformed into the "floating" capacitance C_1 and single switch S (Fig. 12.1b), which periodically grounds one and then the other end of the capacitance. Note, however, that the opposite is true for the inductive

energy transfer configuration in Fig. 10.4. There, the originally "floating" inductance with two switches (Fig. 10.4a) is transformed into a grounded inductance with a single switch (Fig. 10.4b). This comparison can be carried even further. For inductive energy transfer, inversion of the inductor current (but not the polarity of the inductor) is necessary to achieve output voltage inversion (Fig. 10.4), while for capacitive energy transfer, inversion of the capacitor voltage is necessary to realize the same goal. Furthermore the capacitance C_1 and switch S in Fig. 12.1b can be considered to be in parallel, while in Fig. 10.4b the inductance L and switch S are in series. A general principle, the dual nature of the two storage elements, capacitors and inductors, and even the duality of the accompanying switching network, has been once again confirmed on the example of Fig. 10.4 and Fig. 12.1.

Let us now introduce the topological transformation of Fig. 12.1 into the converter of Fig. 10.5 to obtain finally, the new switching converter shown in Fig. 12.2.

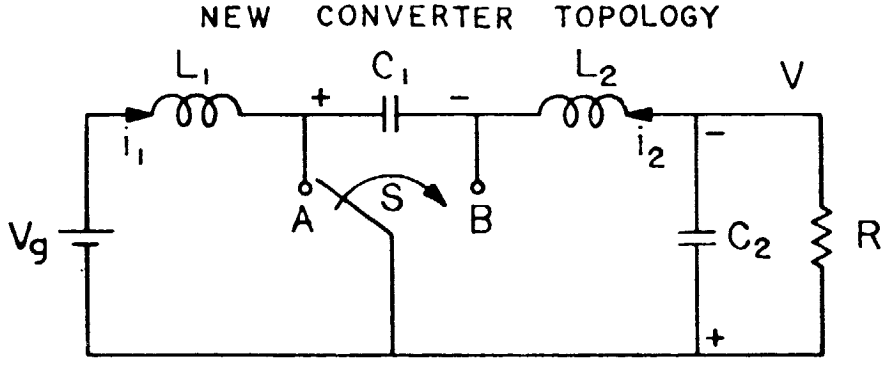


Fig. 12.2 Novel converter topology employing capacitive energy transfer and independent of any particular hardware realization of the switch S.

The novel converter topology of Fig. 12.2 has never previously been reported, so a patent disclosure on this new converter has been made [23], in which the outstanding features, presented in this Part IV in detail, have been concisely summarized.

A closer look at the interconnection of the storage elements in this new converter (Fig. 12.2) might for a moment cause a concern that the low-pass nature of the storage element interconnections postulated for the generalized switching converter in Section 1.5 is being violated here. However, this is not so, even though the capacitance C_1 appears in a series branch (in series with inductances L_1 and L_2) because it effectively acts as a parallel branch either in the input circuit (for interval $D'T_s$) or in the output circuit (for interval DT_s). This is further confirmed later, by the canonical circuit model (Fig. 12.8) of this new converter, which clearly exhibits low-pass nature, or by the experimental converter which does perform the basic dc conversion function.

Another interesting property of the converter becomes immediately apparent. Note that the output capacitance C_2 is not essential for proper converter operation (dc-to-dc conversion), but is merely included further to reduce the switching ripple. Then, the remaining part, which effectively realizes the dc conversion function (consisting of L_1, C_1, L_2 and switch S) is completely symmetrical from the input-output viewpoint. Hence, the input source V_g and

output load R (or load R and capacitance C_2 if present) could be interchanged without effect upon the proper operation of the converter. Very often the input dc source voltage has capacitance across it (to reduce undesired fluctuations, or if it comes from rectified ac source), such that complete symmetry including the output capacitance C_2 is obtained. While the same holds true for the other buck-boost converters (Fig. 10.2 or Fig. 10.4), this is not so for the basic power stages, buck and boost converters (Fig. 1.1). However, this symmetry is not necessarily preserved when the particular hardware realization of the switching action is made by use of various semiconductor devices, as will be shown later.

Another observation about the polarity of the output voltage can be made: it is not restricted to be negative with respect to ground. Namely if the input source voltage is of negative polarity (opposite to that shown in Fig. 1 2.2), the output voltage becomes positive owing to the inverting property of the power stage. Note, however, that this is also possible because the ideal switch S is a representation of the true bipolar switch -- it allows current to be drawn through it in either direction. In a particular implementation this may require appropriate choice of semiconductor devices, as will be illustrated in Chapter 14.

The representation of the new converter topology in Fig. 12.2 with the ideal switch S is essential, since it is independent of any particular realization of switch S. However, for practical implementation, nonideal hardware realization of the switch is used. Let us now investigate one such practical converter realization.

12.2 Physical realization and basic operation of the new converter

We now pose the task of implementing the switch S in Fig. 12.2 by a bipolar transistor, diode combination in a way analogous to that used in Fig. 1.1 for the three common power stages. The transistor is once again used in the switching mode, and the diode is used to supplement its switching action and in turn works in synchronism with it: when the transistor is on, the diode is off, and vice versa. It is, then, now not difficult to see that the switch S in Fig. 12.2 can be substituted by the bipolar transistor, diode combination as shown in Fig. 12.3.

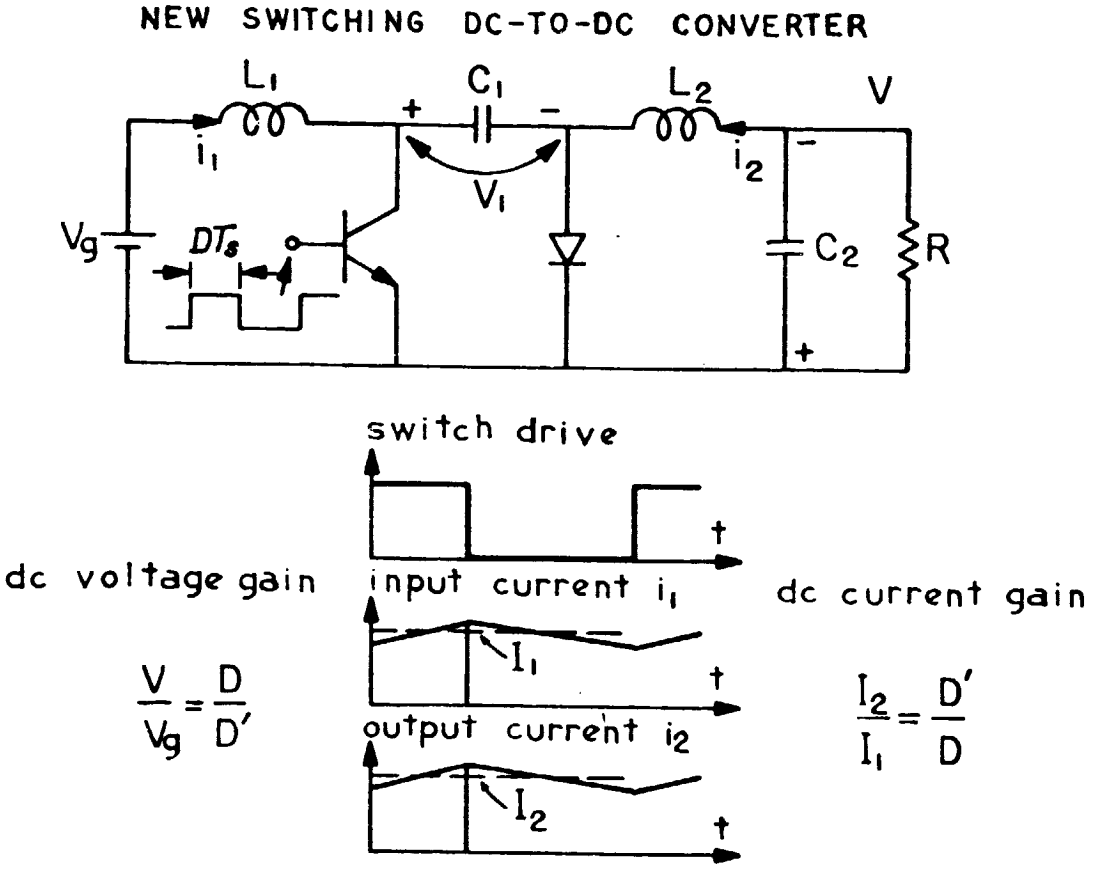


Fig. 12.3 Hardware realization of the new switching converter using bipolar transistor and diode to replace switch S in Fig. 12.2.

Let us now describe the operation of the circuit in Fig. 12.3. During the interval $D'T_s = (1-D)T_s$ when the transistor is off, the diode is forward biased and capacitance C_1 is charging in the positive direction as seen in Fig. 12.4b (switched network for interval $D'T_s$ assuming negligible diode drop). The collector-to-emitter voltage of the transistor is therefore positive, and it can be turned on for the subsequent interval DT_s. However, as soon as it turns on, capacitance C_1 becomes connected across the diode, thus reverse-biasing and effectively disconnecting it from the circuit as in Fig. 12.4a (switched network for interval DT_s assuming negligible saturation voltage of the transistor). During this interval DT_s, the capacitance C_1 discharges through the load R and inductance L_2, thus charging the output capacitance to a negative voltage as shown in Fig. 12.4a. Finally, to close the complete cycle, when the transistor again turns off, the diode conducts again, thus providing the path for current i_2 to charge the output capacitor C_2, using stored energy in the inductance L_2 as the energy source. This is the reason why this converter, owing to its continuous output current (Fig. 12.3), has inherently much smaller switching ripple than the converters with pulsating output current (such as the boost or buck-boost converters of Fig. 1.1).

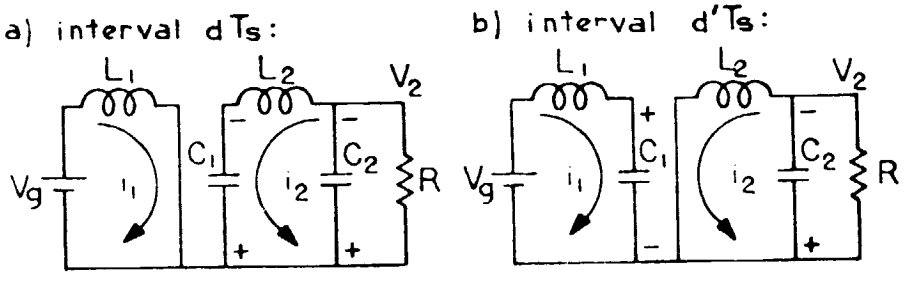


Fig. 12.4 Two switched circuit models of the new converter.

The synchronous action of the transistor and diode can be compared with a see-saw. Namely, when the transistor is turning on, it is pulling down the capacitor end (potential) on its side, while at the same time pulling up (in magnitude) the other capacitor end (on the diode side). The opposite is true when the transistor is turning off. Thus, owing to this automatic see-saw action, the danger in having both transistor and diode on at the same time is eliminated. Note also that the symmetry does not hold any more, and that interchange of the diode and transistor in Fig. 12.3 would not function in the required see-saw manner.

Even though the new converter in Fig. 12.3 contains only one transistor switch, Figs. 12.3 and 12.4 reveal how it effectively behaves as a cascade combination of a boost stage followed by a buck power stage, in which output voltage inversion is obtained at the same time. The energy transferring capacitance C_1 plays a double role: it is the output capacitance of the input boost-like circuit (consisting of transistor, V_g, L_1, C_1 and diode) and also the negative voltage supply to the second stage (consisting of diode, C_1, L_2, C_2, and R) which acts as a buck power stage. The same is true for the diode D, which performs the function of the diode in both power stages.

It looks as though during the interval DT_s, the second nonexistent transistor switch of the buck power stage (see Fig. 11.6 for

comparison) connected the voltage source (here capacitance C_1) to its L_2, C_2 filter and load R, while at the same time the real transistor switch connected inductance L_1 to ground as is usual in a boost converter. Then, during the next interval, it looks as though the nonexistent transistor switch of buck power stage turned off, thus disconnecting voltage source (capacitance C_1) from its L_2, C_2 filter and connecting L_2 through the diode to ground as is always the case in a buck power stage. It appears as though the two switches are functioning, even though in reality only a single transistor and diode are used. This is probably why, owing to this merging of functions, it is not easy to recognize directly from Fig. 12.3 that the new converter is effectively working as a cascade of boost and buck converters. As a matter of fact, the canonical circuit model in Section 12.6 will confirm that the new converter has, except for the inversion, the same dc and dynamic (ac small-signal) properties as the converter in Fig. 11.6 (assuming of course ideal transistors and diodes).

Let us now, before the extensive theoretical and experimental comparison with other converters in the next chapter, review first some of the outstanding features and advantages of the new converter, which are immediately apparent.

12.3 Advantages of the new optimum topology converter

As seen in Fig. 12.3, this converter employs a new circuit topology which enables it to have both input and output current continuous. Hence, none of the problems present in the conventional

converters (buck, boost, buck-boost) due to discontinuity of either input or output current (or both) are present in the new converter. The new converter actually combines the desirable input properties of the boost power stage and the desirable output properties of the buck power stage (without acquiring any of their undesirable properties), and yet performs the general conversion function (increase or decrease of input voltage) of a conventional buck-boost power stage with considerably higher efficiency, as will be proven in the next chapter.

Even though there is no such thing as a dc-to-dc transformer (not physically realizable) the new converter can be functionally considered as a true dc-to-dc transformer, since both its input and output voltages and currents are very close to true dc quantities, owing to the negligible switching ripple.

The new converter uses capacitive energy transfer, which was shown earlier to have much better energy storage and transfer capabilities than the conventional inductive energy transfer.

So far these were the same advantages brought by the favorable cascade connection of a boost followed by a buck discussed in the previous chapter (see Fig. 11.6 also). However, the new converter of Fig. 12.3 has a number of additional advantages over it. First, the number of switching components has been cut in half (one transistor and diode less). This immediately eliminates the need for the additional "floating" drive circuitry for the buck part of the converter in Fig. 11.6, and leaves only the transistor referred to ground in Fig. 12.3 which does not need any special "floating" drive circuitry. Moreover, the switching losses, which represent an important

part of the overall losses, are cut in half in the new converter, hence boosting the efficiency of the converter operation significantly. Hence the switching losses in the new converter become even equal to (or lower than, as demonstrated in the next chapter) the losses in the single-switch converters of Fig. 1.1.

Once again, the new converter of Fig. 12.3 has acquired a good property of the boost converter in not requiring special drive circuitry , since its transistor is with grounded emitter, and not the unfavorable one of buck and conventional buck-boost converters in requiring "floating" drive circuitry.

From the analysis in Chapter 1, it follows that the continuous input and output currents are the most desirable characteristics, and lead alone to the outstanding converter performance. Thus, the following conclusion can be made.

The new dc-to-dc converter (Fig. 12.2 or 12.3) has an optimum topology (maximum performance for the minimum number of components). Namely, to have both input and output current continuous, one needs two inductances, one in series with the input source, the other in series with the load. To obtain a dc level conversion, an energy transferring network with storage capabilities must be used. Here it is a single capacitance. To enable it to serve as an energy transferring device, at least one switch is necessary. Here it is the single switch S in Fig. 12.2 or bipolar transistor, diode combination in Fig. 12.3. Finally, an output capacitance, even though not essential for proper operation of the converter, is put across the load further to reduce output voltage ripple.

It is rather surprising that just this new optimum topology switching converter (Fig. 12.2 or Fig. 12.3) was the only one missing in the complete structure of the buck-boost converters. Let us therefore now review the structure of all converters performing the buck-boost function and generated by two different cascade connections of basic buck and boost power stages, and include the new converter in it.

12.4 General theory of buck-boost converters

With the invention of the new converter, the previously incomplete picture of buck-boost and boost-buck switching converters can be completed as shown in Fig. 12.5.

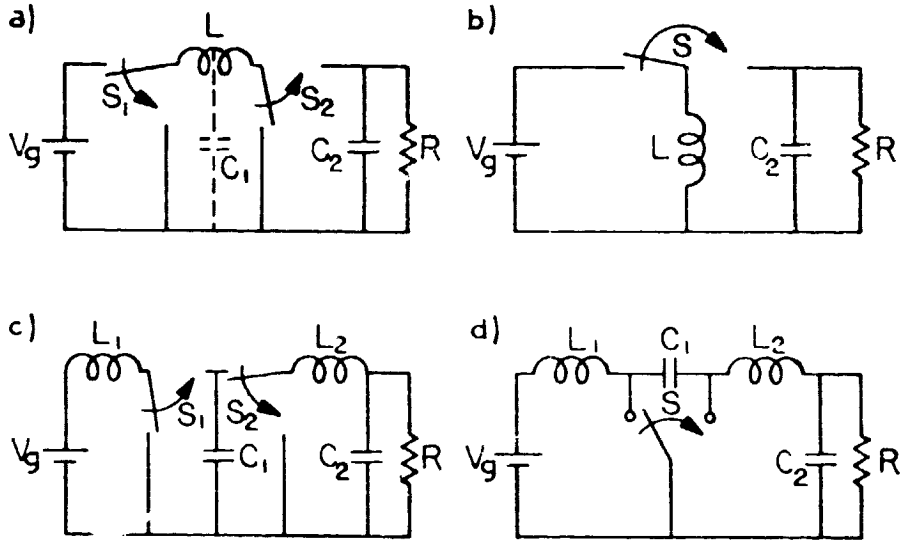


Fig. 12.5 Complete topological structure of buck-boost and boost-buck converters: a) buck-boost noninverting b) buck-boost inverting c) boost-buck noninverting d) boost-buck inverting (new converter).

Fig. 12.5 shows all four possible different topologies to realize the buck-boost function, either in noninverting or in the inverting form. The new converter in Fig. 12.5d has filled in the gap previously existing, and has completed the topological view of these converters.

A good summary of the three possible energy transferring mechanisms is also transparent in Fig. 12.5, which shows mixed energy transfer employing both inductive and capacitive energy transfer (Fig. 12.5a with $C_1 \neq 0$), purely inductive (Fig. 12.5a with $C_1 = 0$ and Fig. 12.5b) or purely capacitive (Fig. 12.5c and d).

Comparison of the complexity of these converters shows those with inductive energy transfer to be of second-order (two storage elements), while those based on capacitive energy transfer are of the fourth order (four storage elements). Nevertheless, their higher complexity is outweighed by their superior performance, since converters in Fig. 12.5a and b require at least one section of input L,C filter and still have a much worse output characteristic because of pulsating output current (as discussed in Chapter 1 and in extensive comparison of next chapter).

Since the resulting dc and ac small-signal circuit models of all converters in Fig. 12.5 are linear models, a very good analogy with linear vector fields can be made as shown in Fig. 12.6, which also emphasizes the generic properties of the cascade connection of buck and boost converters.

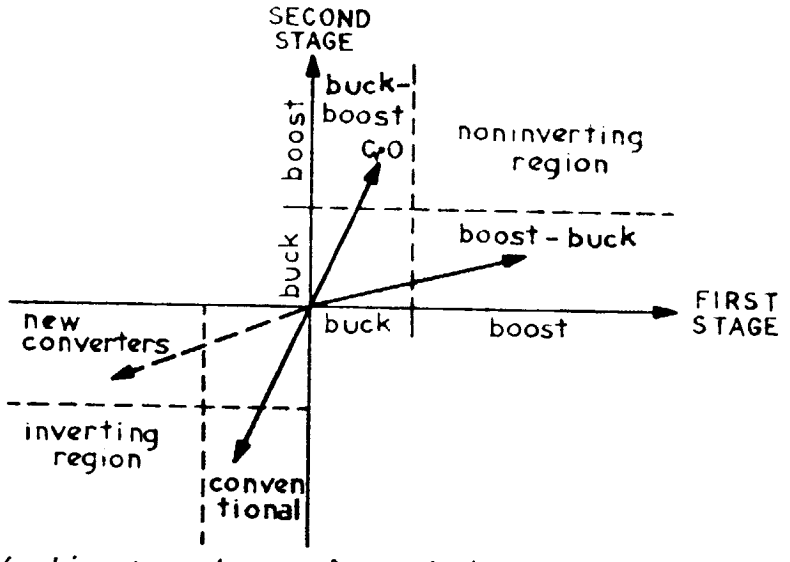


Fig. 12.6 Linear vector analogy of the generation of converters in Fig. 12.5 by cascading the basic buck and boost converters.

As seen in Fig. 12.6, the basic buck and boost converters are considered as abstract entities: the elementary vectors are defined along coordinates representing the first and second stage of the cascade connection. Then, the noninverting converters (buck-boost and boost-buck) of Fig. 12.5a and Fig. 12.5c are obtained as their linear combination, while the corresponding inverting converters (Fig. 12.5b and Fig. 12.5d) are defined as the vectors of same magnitude but opposite sign (direction), thus in the third quadrant on Fig. 12.6. In particular, a previously missing link establishing new converters of Fig. 12.5d is shown in Fig. 12.6 by a dotted line vector, which generates a whole new field of converters (for variety of storage element values in its configuration).

Note, however, that this analogy even becomes an accurate one, if the converter models, instead of the converters themselves, are considered as abstract vectors in Fig. 12.5. Namely, both inverting converters (Fig. 12.5b and d) have the same dc and dynamic (ac small-signal) models as their noninverting counterparts, except

for the inversion property. The same fact is clearly marked on Fig. 12.6 in having the same magnitude but opposite sign, for their abstract representations. The fact that the new converter (Fig. 12.5d) has the same dc and dynamic properties as its counterpart (Fig. 12.5c) except for the inversion property is demonstrated later in Section 12.6.

The region defining the general buck-boost function in Fig. 12.6 was shown shaded. The remaining unshaded region in the first quadrant defines specialized functions: buck (obtained by buck-buck cascade connection) and boost (obtained by boost-boost cascade connection). Besides their special function, they also do not have their corresponding inverting counterparts as does the buck-boost connection.

The position of the new converter topology within buck-boost converters has now been firmly established, and we can turn to a very interesting correlation between the new converter topology and that of its building blocks, buck and boost converters.

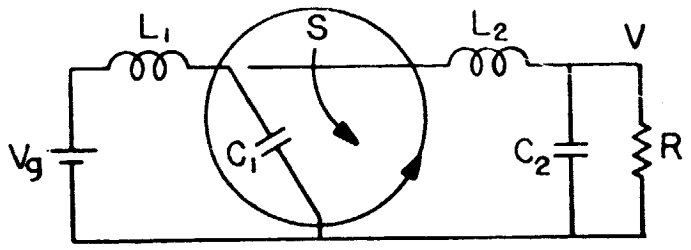
12.5 Correlation among buck, boost and new converter topologies

We now recall that the three common converters (buck, boost and buck-boost) of Fig. 1.1 may be considered as generated by cyclic rotation of the series connection of the energy transferring inductance L and a single-pole double-throw switch S, between input (source) and output (load) circuit, as was explained in Section 10.1 and shown in Fig. 10.1.

Let us now find a similar interpretation for the generation of the new converter topology, along with that for the two basic

converters, the buck and boost. But in distinction with the previous method, and in order to enhance common features of the latter three converters, we now look at: the buck converter with input filter, the boost converter with output filter, and the new converter as shown in Fig. 12.7.

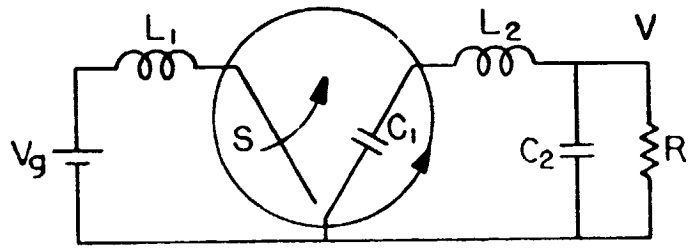
a) buck converter with input filter:



noninverting

$$\frac{V}{V_g} = D$$

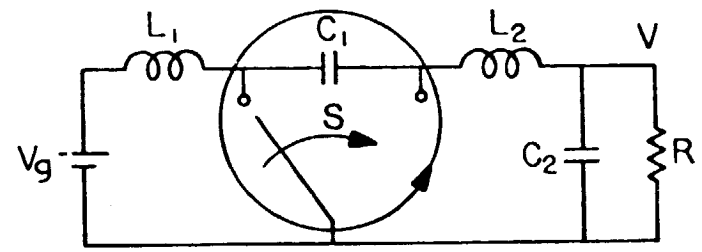
b) boost converter with output filter:



noninverting

$$\frac{V}{V_g} = \frac{1}{D'}$$

c) new converter:



inverting

$$\frac{V}{V_g} = -\frac{D}{D'}$$

Fig. 12.7 Generation of the three converters: buck with input filter, boost with output filter, and new converter by cyclic rotation of the parallel connection of capacitance C and switch S.

It now becomes apparent that all three converters in Fig. 12.7 may be generated by cyclic rotation (counterclockwise) of the parallel connection of capacitance C_1 and single-pole double-throw switch S between the input circuit (now consisting of a voltage source in series with inductance L_1) and the output circuit (now consisting of inductance L_2 in series with load R). Once again the striking dual nature of the two generating procedures becomes transparent: the cyclic rotation of the series combination of inductance and switch is substituted here by the parallel combination of the capacitance C_1 and switch S.

When comparing the new converter with the buck or boost converter, it seems appropriate to make the comparison with their versions in Fig. 12.7a and 12.7b. This way, all three converters in Fig. 12.7 have the same number of storage elements (four) and similar performance characteristics, both input and output currents continuous. However, the new converter is still superior in that it is capable of both increasing and decreasing the input dc voltage, while the other two converters are not. In a practical realization with a transistor and diode, there could be some additional advantages. For example, the buck converter, unlike the new converter, needs special drive circuitry, and the boost converter may have less favorable frequency response than the new converter.

After this in-depth theoretical explanation of the new converter, the development and the experimental confirmation of its linearized circuit model predictions seem now appropriate.

12.6 Modelling and experimental verification of the new converter

By application of the same procedure outlined in Chapter 11, the canonical circuit model of the new converter (Fig. 12.3) can be obtained as in Fig. 12.8. Again, the series parasitic resistances of the two inductors have been included, because of their significant effect on converter performance, and the transistor and diode are assumed ideal.

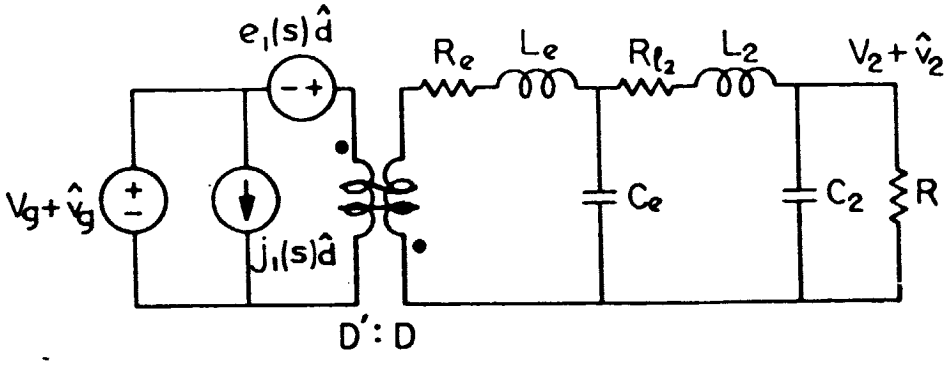


Fig. 12.8 Canonical circuit model of the new converter in Fig. 10.2

The element values in Fig. 12.8 are defined as

$$R_e = \left(\frac{D}{D'}\right)^2 R_{\ell 1}, \qquad L_e = \left(\frac{D}{D'}\right)^2 L_1, \qquad C_e = \left(\frac{C_1}{D^2}\right) \tag{12.1}$$

$$e_1(s) = -\frac{V_2}{D^2}\left\{1 + \frac{R_{\ell 2}-R_e}{R} - s\left[\frac{L_e}{R} - R_e C_e D'\left(1+\frac{R_{\ell 2}}{R}\right)\right] + s^2 L_e C_e D'\left(1+\frac{R_{\ell 2}}{R}\right)\right\} \tag{12.2}$$

$$j_1(s) = -\frac{V_2}{D'^2 R}\left\{1 - sC_e RD'\left(1+\frac{R_{\ell 2}}{R}\right)\right\} \tag{12.3}$$

Comparison of this model and the canonical circuit model in Fig. 11.5 for the boost-buck noninverting converter, shows that they are identical except for the polarity of the D':D transformer: in the new converter it is inverting, while in Fig. 11.5 it is noninverting. Because of this inverting property, the output dc voltage V_2 is negative in the new converter and equations (12.2) and (12.3) are

identical to (11.12) and (11.13) for the other converter.

An important conclusion can now be drawn: except for the inversion, the new converter has the same dc and dynamic properties as the boost-buck noninverting converter of Fig. 10.5. Hence, the complete analysis of Chapter 11 is equally valid for the new converter.

For the purpose of experimental verification, the new converter of Fig. 12.3 was built with the following switching elements: transistor General Electric D44H10 and diode TRW PD9050.

For easier comparison, the same components and operating conditions as for experimental verification of the boost-buck noninverting converter (Section 11.2) were used, that is as in (11.21).

It is not surprising that dc voltage gain measurement followed very closely that in Fig. 11.7, thus confirming the equality of the dc conditions. Another verification, of the dc voltage V_1 of the energy transferring capacitance C_1, confirmed that it does change according to $V_1/V_g = 1/D'$, or the same as the gain of the boost converter. This confirms that capacitance C_1 is indeed to be considered as the output capacitance of the boost converter, the fact which may not be so obvious from the converter circuit in Fig. 12.3.

For the same operating condition as before in Chapter 11 ($D = 0.5$, $f_s = 40kHz$), the duty ratio modulation to output voltage frequency response measurements agreed very well with those of Fig. 11.9, thus confirming the equality of their dynamic models. Hence all the benefits of the favorable frequency response discussed in Chapter 11 apply equally well to this new converter.

We now summarize the major results accomplished in this chapter. First, it has been demonstrated how the topological reduction of the number of switches and the recognition of the duality nature of the storage element networks with switches, led to the discovery of the new converter topology (Fig. 12.2) based upon capacitive rather than inductive energy transfer. The new converter topology in Fig. 12.2 is independent of any particular hardware realization of the single switch S.

Then, it was shown how a single bipolar transistor and diode can be used in practical implementation of the switching action (Fig. 12.3), and an in-depth explanation of the physical operation of that circuit is given. A number of advantages of the new converter over the other known converters, emerged as a consequence of its optimum topology (maximum performance for minimum number of components).

It has also been demonstrated that the new converter topology was the only one previously missing in the complete structure of all buck-boost and boost-buck converters (Fig. 12.5). In connection with that, an interesting abstract analogy with linear vectors was given (Fig. 12.6).

Another view of the generation of the new converter, dual to that in Fig. 10.1, arrived at the new converter topology by cyclic rotation of the parallel combination of the capacitance and switch S between the input and the output circuit, with buck and boost converters obtained alongside.

Finally, the canonical circuit model of the new converter was obtained (Fig. 12.8) which, except for inversion, is identical with

that for the boost-buck noninverting converter (Fig. 11.5). The subsequent experimental measurements confirmed these modelling predictions.

Several of the outstanding features of the new converter are further exposed when it is compared in the next chapter with the only other converter having the general dc conversion function and the simplest possible structure, the conventional buck-boost converter.

CHAPTER 13

COMPARISON OF THE NEW CONVERTER AND CONVENTIONAL BUCK-BOOST CONVERTER

In this chapter an extensive theoretical as well as experimental comparison is made between the new converter and the conventional buck-boost converter to which an input filter has been added. This, and the same component element values as well as operating conditions for the two converters, enable a convenient common ground for comparison. The two converters are then compared with respect to the most important performance parameters, namely: switching ripple, efficiency (with separate analysis of transistor switching and dc losses as well as parasitic resistance losses), electromagnetic interference (EMI) problems, complexity of the transistor drive circuitry, effect of the effective series resistance (ESR) of the output capacitor, and converter size and weight reductions resulting from potential increase of the switching frequency f_s. At all these comparison points, the new converter is shown to be superior.

After the detailed theoretical and experimental comparisons, the important advantages of the new converter are concisely summarized at the end of the chapter.

13.1 Experimental test circuits of the two converters

Two experimental test circuits have been built, one employing the new converter topology and the other the conventional buck-boost converter with an input filter as shown in Fig. 13.1.

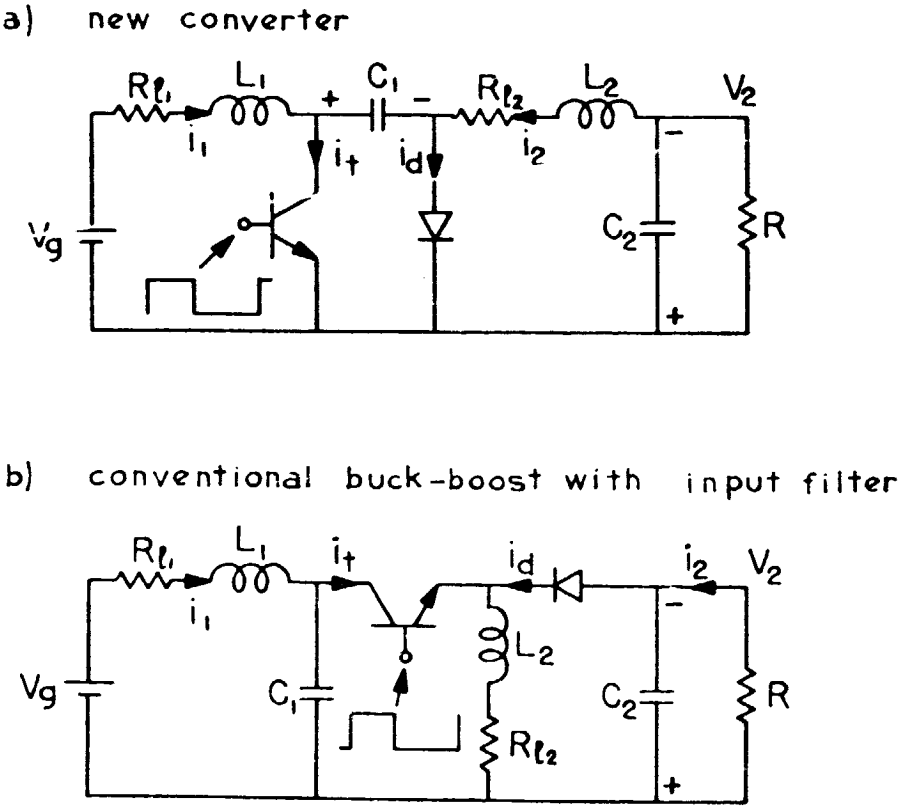


Fig. 13.1 Two converters used for experimental and theoretical comparison employ the same components but different topologies.

The addition of the input L_1,C_1 filter to the conventional buck-boost converter is invariably required to smooth out the input current switching ripple. This then provides a convenient comparison ground for the two converters in Fig. 13.1. Now both converters have continuous input current in addition to performing the same general dc conversion function with output dc voltage inversion. Moreover, both now consist of the same components. They, however, differ in the way these components are interconnected. Therefore the effect of two different converter topologies upon the performance characteristics can now be extracted.

For comparison purposes, the same component element values are used for both converters, and are

$$R_{\ell 1} = 1.0\Omega, \quad L_1 = 3.5\text{mH}, \quad C_1 = 100\mu\text{F}, \quad R = 75\Omega$$
$$R_{\ell 2} = 0.4\Omega, \quad L_2 = 6.5\text{mH}, \quad C_2 = 0.47\mu\text{F} \tag{13.1}$$

The same operating conditions are also used:

$$V_g = 5\text{V}, \quad D = 0.6, \quad f_s = 40\text{kHz} \tag{13.2}$$

With the two converters now completely defined, we turn to detailed experimental and theoretical comparison.

13.2 Switching ripple comparison

Since the output stage of the new converter in Fig. 13.1a represents essentially a buck power stage, the output current ripple Δi_2 can be computed as for the buck converter in Chapter 1 from equation (1.8), that is $\Delta i_2 = V_2 D' T_s / L$, or for values given in (13.1)

and (13.2), as Δi_2 = 14.5mA. The output voltage ripple Δv_2 is similarly obtained as in (1.9), that is

$$\Delta v_2 = \frac{V_2 D'}{8 L_2 C_2} \frac{1}{f_s^2} \tag{13.3}$$

Numerically, Δv_2 = 95.5mV in a close agreement with the actual output voltage ripple shown in Fig. 13.2a displaying the actual oscilloscope waveforms of the new converter. Again, the new converter has retained the good ripple properties of the buck converter: output voltage ripple is <u>independent</u> of the load current, and decreases sharply with increase in switching frequency (as $1/f_s^2$). This is a consequence of the <u>continuous output current</u> i_2, also shown in Fig. 13.2a.

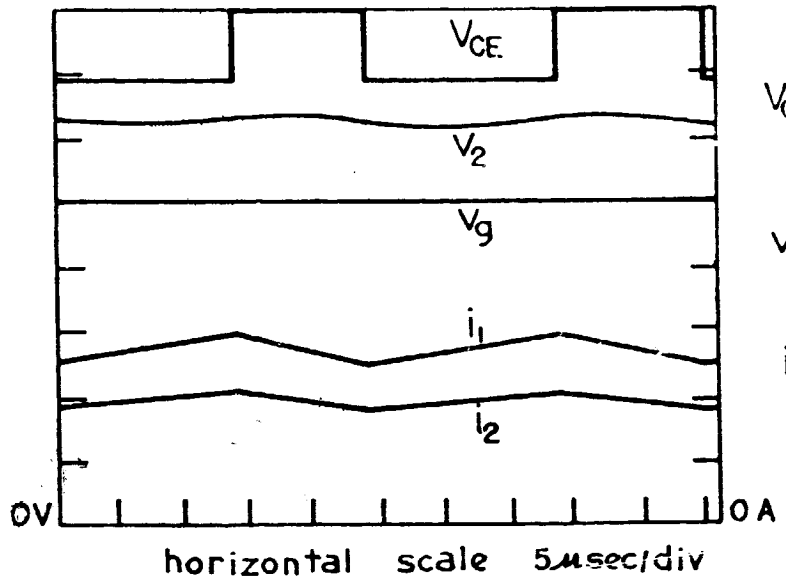
However, the buck-boost converter still has <u>discontinuous output</u> current i_d (diode current) as shown in Fig. 13.2b. The immediate consequence is that the output voltage ripple Δv_2 is <u>load-current dependent</u> and obtained as before in (1.12) as

$$\Delta v_2 = D \frac{V_2}{RC_2} \frac{1}{f_s} \tag{13.4}$$

For the same element values (13.1) and (13.2) as in the new converter, the output voltage ripple from (13.4) becomes Δv_2 = 3V (here $v_2(0^+)$ = 7.6V from Fig. 13.2b is used instead of V_2 = 6.3V since ripple is large and (13.4) is strictly applicable for small ripple). This is quite close to the actual measured ripple of Δv_2 = 2.8V from the output voltage waveform in Fig. 13.2b.

Therefore, with use of the same element values in both

a) new converter



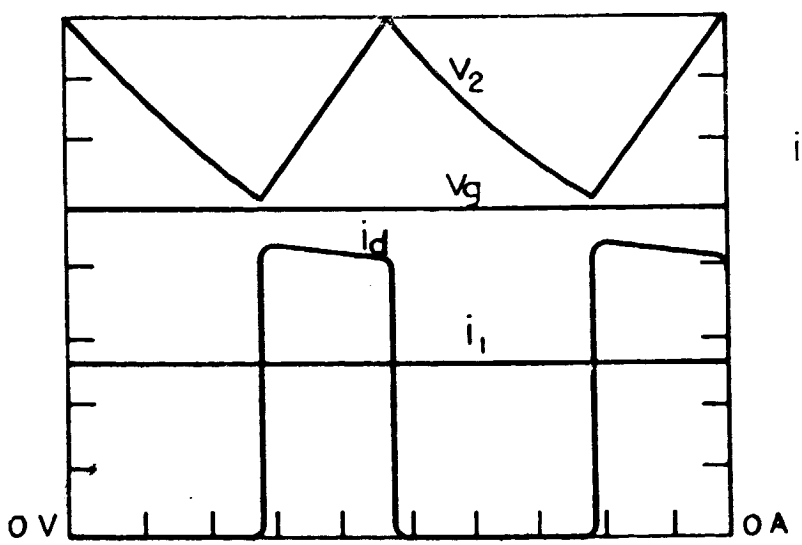
vertical scales :

V_{CE} - collector emitter voltage (10V/div)

V_g, V_2 - 1V/div

i_1, i_2 - 50 mA/div

b) conventional buck-boost with input filter



i_d - 50 mA/div

Fig. 13.2 Comparison of the output voltage and current switching ripple of the two converters of Fig. 13.1.

converters, the output voltage ripple was reduced from a totally unacceptable 44% in the conventional buck-boost converter (Fig. 13.2b) to less than 1.5% in the new converter (13.2a). Hence a 30:1 ripple reduction has been achieved just by use of the new converter topology. Moreover, this ratio becomes even proportionally much bigger with increased switching frequency f_s, duty ratio D and increased loads ($R < 75\Omega$).

Since the voltage ripple in Fig. 13.2 is completely unacceptable, one would have to resort to some means of reducing it. As seen in (13.4) the ripple would be reduced by substantial increase of capacitance C_2, but at the same time size and weight would be proportionally increased. The other possibility, the increase of switching frequency f_s, would, because of increased switching losses, degrade further the efficiency of the conventional buck-boost converter in Fig. 13.1b. Moreover, by increase of switching frequency, the output voltage ripple Δv_2 in the new converter would decrease at a much higher rate, owing to the $1/f_s^2$ dependence in (13.3) as compared to the $1/f_s$ dependence in (13.4).

As a conclusion, the new converter (Fig. 13.1a) outperforms in every respect the conventional buck-boost converter (Fig. 13.1b) as far as the output switching ripple is concerned.

13.3 Comparison of the transistor and diode dc losses and transistor switching losses for the idealized case ($R_{\ell 1}=R_{\ell 2}=0$)

A substantial part of the total converter losses is due to the dc losses in the transistor and diode, which come from their non-ideal nature. Namely, when the transistor is on, the collector-emitter voltage V_{CE} is not zero (as it is for an ideal switch S), but some saturation voltage V_{CEsat} on the order of 0.3V-1V. Likewise, the diode has some forward voltage drop V_F of the same order. Since V_{CEsat} and V_F increase very little with increase of dc current, the dc losses are approximately proportional to the dc currents. Hence we compare the dc transistor and diode losses of the two converters by comparing their respective dc currents (when they are on, since their dc losses are negligible in the off state).

Let us for the moment assume that the inductors in the two converters of Fig. 13.1 are ideal ($R_{\ell 1}=R_{\ell 2}=0$) because we will return to the real case ($R_{\ell 1}\neq R_{\ell 2}\neq 0$) in Section 13.5.

At first sight, it seems that the transistor and diode dc losses are higher in the new converter (Fig. 13.1a), since the sum of the input and output currents (i_1+i_2) passes through its transistor when it is on, while in the conventional buck-boost converter (Fig. 13.1b) only the input current passes through its transistor. Likewise, when the transistor is off, both input and output currents (i_1+i_2) pass through the diode in the new converter, while only output current passes through the diode in the conventional buck-boost converter. However, this is only an illusion as clearly illustrated on the actual oscilloscope waveforms of the four currents

i_1, i_2, i_t, and i_d shown in Fig. 13.3 for the new converter, and in Fig. 13.4 for the conventional buck-boost converter. As a matter of fact the actual comparison of Figs. 13.3 and 13.4 shows that the transistor and diode currents are higher for the conventional buck-boost converter than for the new converter. This is, however, not a mere coincidence, but a consequence of the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ (which, of course, cannot be excluded from the actual measurements as they can from the analysis) as will be explained in Section 13.5. Let us, now, go back to the ideal case $R_{\ell 1}=R_{\ell 2}=0$, to clarify this result.

Consider first the conventional buck-boost converter of Fig. 13.1b. Its transistor current during the interval when the transistor is on must be proportionally higher than the input current i_1 (and its dc value I_1) in order to have the same dc average value I_1 over the whole period T_s (see Fig. 13.4a). Also, through the action of the inductance L_2, transistor dc current I_t (when it is on) is equal to the diode dc current I_d (when the diode is on) since they are both equal to the dc current of inductance L_2. Hence

$$I_t = I_d = I_1/D \tag{13.5}$$

where I_1 is the dc input current. Note that for the conventional buck-boost converter, I_2 is defined as the dc load current (dotted line in Fig. 13.4b) and not as the dc current of inductance L_2, in order to conform with the dc input and output current notation for the new converter.

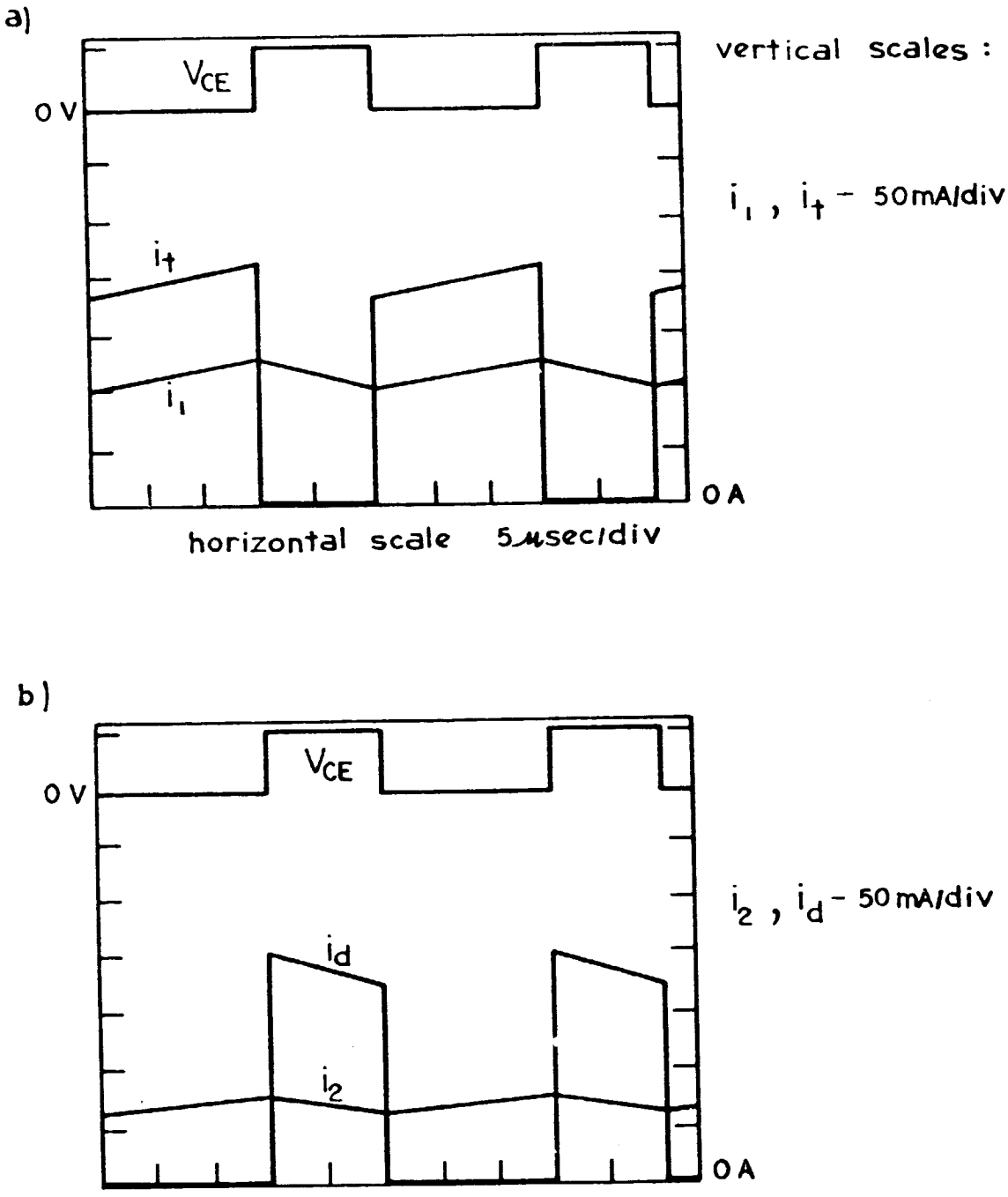


Fig. 13.3 Comparison of input and output currents with transistor and diode currents for the new converter: a) input current and transistor current; b) output current and diode current.

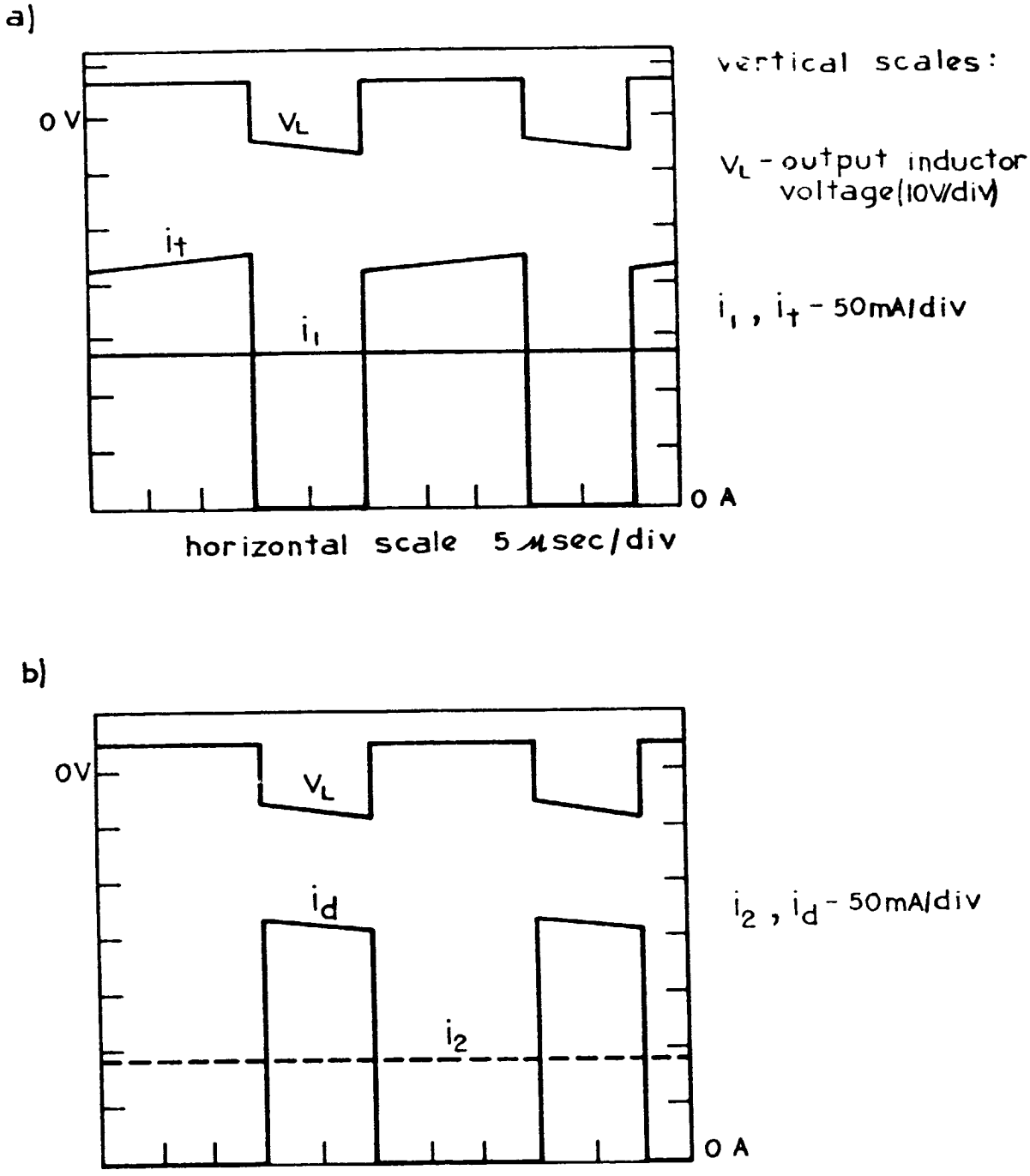


Fig. 13.4 Comparison of input and output currents with transistor and diode currents for conventional buck-boost converter: a) input current and transistor current; b) output current and diode current.

For the new converter in Fig. 13.1a, transistor and diode dc currents I_t and I_d are equal to the sum of input and output dc currents, that is

$$I_t = I_d = I_1 + I_2 \tag{13.6}$$

However, upon substitution of the dc current relations $I_2/I_1 = D'/D$ for this converter, in (13.6) the same result as (13.5) is obtained. Hence, the dc transistor and diode currents I_t and I_d are the same for both converters in this ideal case ($R_{\ell 1}=R_{\ell 2}=0$), and consequently their respective dc losses are also equal.

Since the on currents I_t of the switching transistors are the same for the two converters, so are the corresponding saturation voltages V_{CEsat}. From Fig. 13.1 the collector-emitter voltages of the transistors when they are off (V_{CEoff}) are also the same and equal to $V_{CEoff} = V_g/D'$. Hence, during switching the transistor operating point traverses the region between the same points (V_{CEsat},I_t) and (V_{CEoff},0). Therefore the transistor switching losses are also the same for two converters of Fig. 13.1 in the ideal case $R_{\ell 1}=R_{\ell 2}=0$.

13.4 Comparison of the resistive dc losses only

We now make the opposite assumption from the one in the previous section, that is, the transistor and diode are ideal with no dc losses, and instead include the effect of the parasitic resistances only by considering $R_{\ell 1}$,$R_{\ell 2}\neq 0$.

From the canonical circuit models for the two converters (or by solving for the dc conditions using state-space averaging), the efficiency and dc conversion relations are obtained as

new converter:

$$\eta_1 = \frac{R}{R + \left(\frac{D}{D'}\right)^2 R_{\ell 1} + R_{\ell 2}} \quad ; \quad \left|\frac{V_2}{V_g}\right| = \frac{D}{D'}\eta_1 \qquad \frac{I_1}{I_2} = \frac{D}{D'} \tag{13.7}$$

conventional buck-boost with input filter:

$$\eta_2 = \frac{R}{R + \left(\frac{D}{D'}\right)^2 R\ell_1 + \frac{R_{\ell 2}}{D'^2}} \quad ; \quad \left|\frac{V_2}{V_g}\right| = \frac{D}{D'}\eta_2 \qquad \frac{I_1}{I_2} = \frac{D}{D'} \tag{13.8}$$

Comparison of (13.7) and (13.8) now reveals that both the dc voltage gain and efficiency are higher in the new converter than in the conventional buck-boost throughout the duty ratio D range because of the difference in terms dependent on $R_{\ell 2}$, the parasitic resistance of inductance L_2.

In order to enhance this difference, the inductances in the experimental models of Fig. 13 1 have been interchanged such that now $R_{\ell 1} = 0.4\Omega$ and $R_{\ell 2} = 1.0\Omega$, but $R = 75\Omega$ as before. With these element values and by use of (13.7) and (13.8), the dc gain characteristics for the two converters are as shown in Fig. 13.5, while efficiency is plotted in Fig. 13.6.

Let us now with the help of these graphs illustrate the comparison of the efficiencies between the two converters. Suppose that it is required that the nominal input voltage $V_g = 5V$ is boosted 3 times. This would result in the establishment of the steady-state (dc) duty ratio D = 0.82, or operation at point A in Fig. 13.5, if the conventional buck-boost converter of Fig. 13.1b was used. However, the same gain of 3 can be achieved with the new converter by operation at point B, with substantially smaller duty ratio D = 0.76 as seen

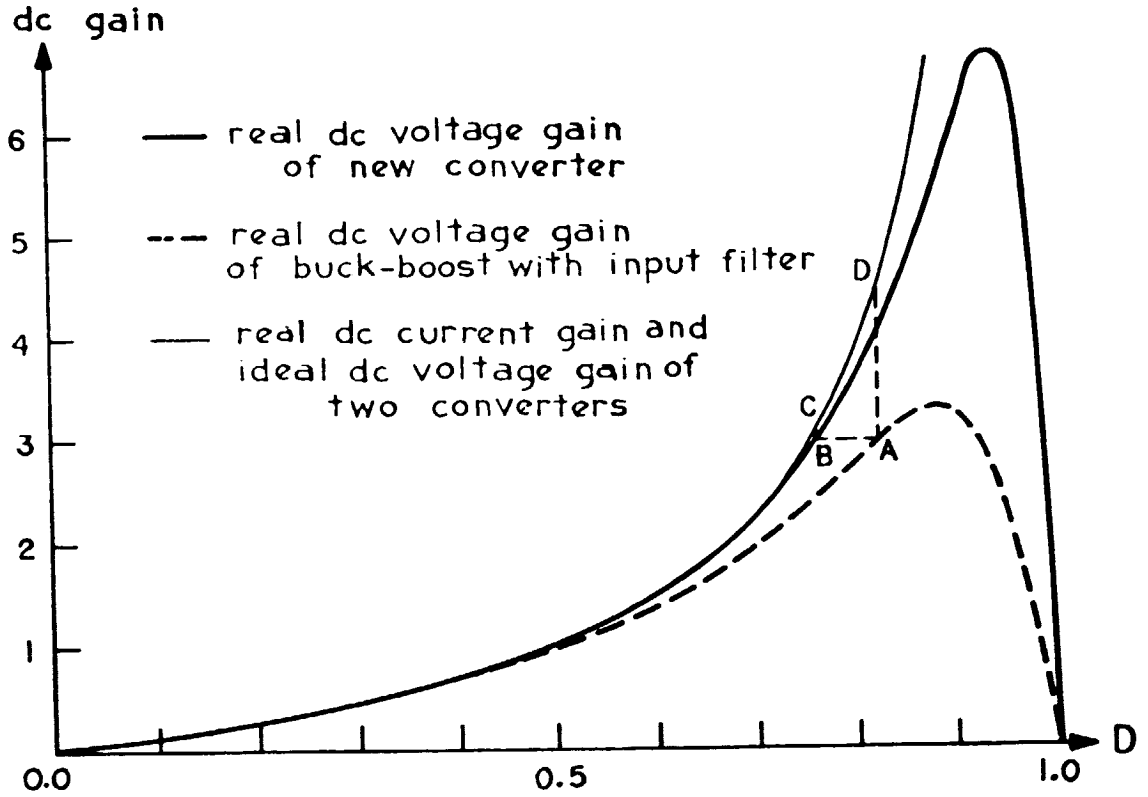


Fig. 13.5 Steady-state (dc) characteristics for the two converters of Fig. 13.1.

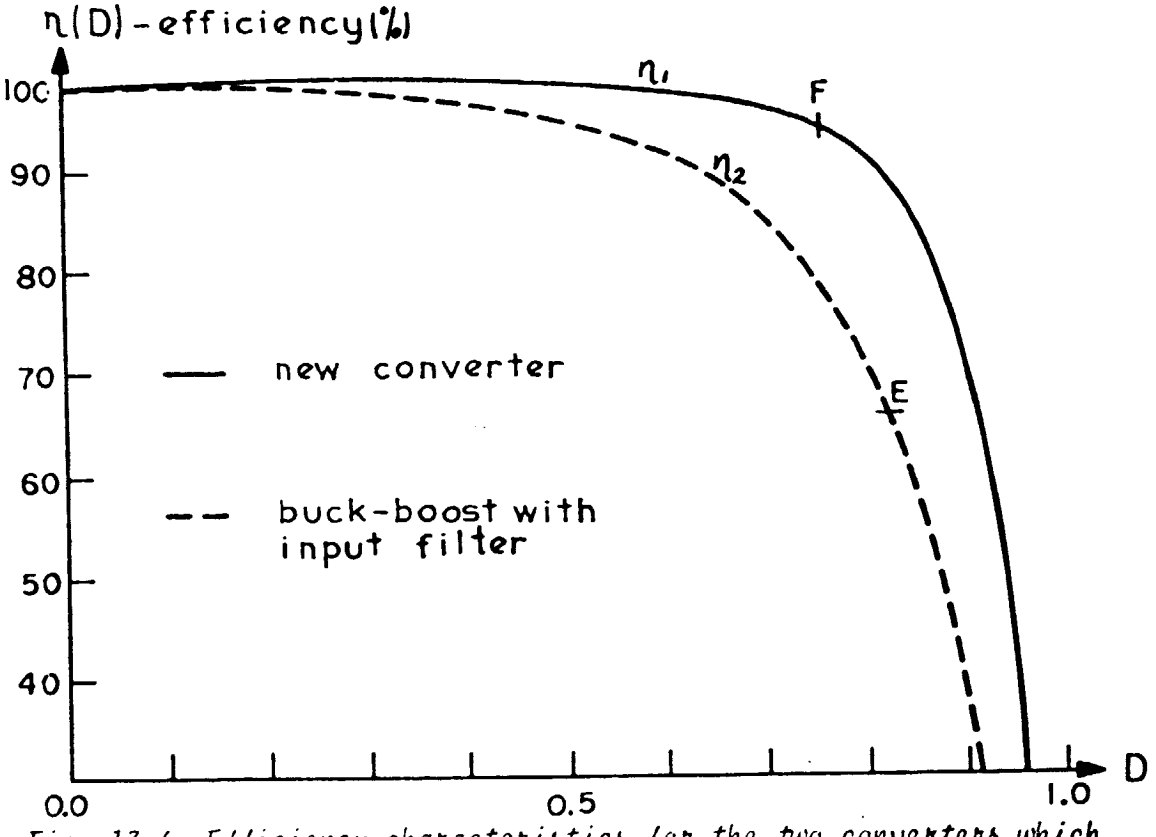


Fig. 13.6 Efficiency characteristics for the two converters which include effect of parasitic resistances only ($R_{\ell 1} \neq 0$, $R_{\ell 2} \neq 0$).

in Fig. 13.5. From Fig. 13.6 we find that operation at point A (D = 0.82) would mean only 65.5% efficiency (point E) while operating at point B would give an excellent 93.5% efficiency (point F). Hence, use of the same storage element values (inductors) in the novel circuit topology of the new converter (Fig. 13.1a) would boost the efficiency by 28% over the conventional solution (Fig. 13.1b). But as surprising as it may seem, this is only a conservative estimate, as the following section verifies.

13.5 Real transistor and diode dc losses and transistor switching losses ($R_{\ell 1}, R_{\ell 2} \neq 0$)

We now consider what effect inclusion of the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ has upon the real transistor and diode losses. For the same numerical example as in the previous section, the output dc voltage $|V_2| = 15V$ (dc gain of 3) and the output dc current $I_2 = |V_2|/R = 200mA$ are the same for both converters (operating points A and B in Fig. 13.5). However, the input dc currents corresponding to these operating points are substantially different, owing to the significant difference in their efficiencies.

For the conventional buck-boost converter we find from Fig. 13.5 for D = 0.82 the dc current gain of $I_1/I_2 = 4.55$ or $I_1 = 910mA$. By use of the expression (13.5) for the dc transistor and diode current, that is, $I_t = I_d = I_1/D$ we finally obtain $I_t = I_d = 1110mA$.

For the new converter, however, operating at D = 0.76 (point C on the dc current gain characteristic in Fig. 13.5) gives only $I_1/I_2 = 3.15$ or $I_1 = 630mA$. Then, by use of (13.6) to find the transistor and diode dc losses for this converter, we get

$I_t = I_d = I_1 + I_2 = 830mA.$

Consequently, when the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ are taken into account, the transistor and diode dc currents are not the same but, for the particular example, are about 34% larger in the conventional topology compared to the new converter topology. This now explains very well why the actual measured transistor and diode dc currents for the conventional buck-boost converter (Fig. 13.4) are higher than those for the new converter (Fig. 13.3). Hence, in reality ($R_{\ell 1}$, $R_{\ell 2} \neq 0$) the new converter has lower transistor and diode dc losses than has the conventional solution.

In addition to the higher dc losses, the switching losses now become higher for the conventional buck-boost converter, since its transistor is operating at a higher (V_{CEsat},I_t) point and traverses, during switching, a region of higher dissipation.

In conclusion, both transistor and diode dc losses and transistor switching losses are substantially higher in the conventional solution, in addition to already higher resistive losses. Hence, for the same element values and output requirements (constant dc voltage) as in the conventional topology, the new converter topology offers unmatched increase in efficiency.

13.6 Comparison of ESR losses of the output capacitance

So far we have considered only the inductors as the nonideal elements, with their corresponding modelling representation which includes their series parasitic resistances. The real capacitors are, likewise, better modelled by inclusion of their effectives series resistance (ESR), which signifies the ac losses present in the real

capacitor. Let us, therefore, now find out what consequences its inclusion in the model would have upon the two converters in Fig. 13.1.

The effect of ESR is particularly pronounced at the output capacitor C_2, so for purpose of numerical comparison we assume that it has ESR = 1Ω. As shown before (Fig. 13.3b) output current ripple (ac) of the new converter is small, at Δi_2 = 14.5mA, hence the capacitance ac losses P_c are $P_c = (\Delta i_2)^2/12$ ESR = 17.5μW = 17.5×10^{-6}W. For the conventional buck-boost, however, the output current is pulsating with Δi_2 = 210mA (Fig. 13.4b), hence the ac losses are P_c = 3.68mW, which amounts to a 210:1 increase in power loss in the conventional solution. This becomes even the dominant power loss in the conventional buck-boost at higher load currents. For example when Δi_2 = 10A (much higher load current) losses in the conventional converter become P_c = 8.3W, while in the new converter, owing to its ac ripple independence of the load current, they stay the same as before at P_c = 17.5μW. Not only would this still further degrade the efficiency of the conventional solution at higher load currents, but one would have difficulty in finding a capacitor which can dissipate so much power. Moreover, in order to obtain acceptable output voltage ripple, larger capacitances have to be used in the conventional solution and hence ESR problems would be further enhanced. None of these problems is present in the new converter of Fig. 13.1a.

13.7 Size and weight reduction in the new converter

It has been demonstrated both theoretically and experimentally that the value of the output capacitance C_2 can be very small in the new converter of Fig. 13.1a (C_2 = 0.47μF) and still achieve reasonably small switching ripple. A small value of output capacitance thus eliminates the need for bulky, electrolytic capacitors of high capacitance value. Moreover, it is very significant that the value of the energy transferring capacitance C_1 does not enter the ripple calculations in (13.3). Hence it is no surprise that the output voltage ripple remains essentially unaffected (as observed on the scope waveform) even when the capacitance C_1 is reduced 1000 times from C_1 = 100μF to C_1 = 0.1μF, while all other conditions remain unchanged as in (13.1) and (13.2). This once again confirms the very significant energy transferring capabilities per unit size and weight of the capacitive storage.

However, the voltage across the capacitance C_1 is no longer constant (dc) as for C_1 =100μF, but has a triangular waveform (as observed on the scope) with substantial magnitude. But, according to the duality principle, this is to be compared with the triangular current waveform of the energy transferring inductance in the conventional buck-boost converter.

In conclusion, for all practical purposes, the physical size and weight of the two capacitors C_1 and C_2 in this new converter (Fig. 13.1a) can be completely neglected. In addition, the two inductors, which independently control input and output current

ripple, can be significantly reduced in size (and weight) by further increase of the switching frequency.

The important advantages of the new converter topology, covered extensively in Chapters 12 and 13, are now concisely summarized in the next section.

13.8 Summary of the advantages of the new switching converter

A novel switching dc-to-dc converter (Fig. 12.3) is developed which offers higher efficiency, lower output voltage ripple, reduced EMI, smaller size, and yet at the same time achieves the general conversion function: it is capable of both increasing or decreasing the input dc voltage depending on the duty ratio of the switching transistor. This converter employs a new topology (Fig. 12.3) which enables it to have both input and output current continuous. The converter uses capacitive energy transfer rather than the inductive energy transfer employed in the other converters. In addition, when it is incorporated into a switching regulator, stabilization problems are reduced owing to the favorable frequency response of the new converter (Figs. 11.8 and 11.9).

Some of the important advantages of the new converter over the other existing converters are:

1) Provides true general (increase or decrease) dc level conversion of both dc voltage and current
2) Offers much higher efficiency.
3) Both output voltage and current ripple are much smaller
4) No dissipation problems in the ESR of the output capacitance

5) Substantial weight and size reduction due to smaller output filter and smaller energy transferring device (capacitance C_1)

6) Electromagnetic interference (EMI) problems are substantially reduced, thanks to the small ac input current ripple, without need for additional input filters

7) Excellent dynamic response enables simple compensation in a switching regulator implementation

8) Can be used as a constant-current as well as a constant-voltage source

9) Much simpler transistor drive circuitry, since the switching transistor is referenced to ground (grounded emitter)

10) Various technological implementations of the switching action are possible (see Chapter 14).

In conclusion, the new switching dc-to-dc converter is superior to any of the currently known dc-to-dc converters in its category, outperforming them in every respect.

CHAPTER 14

IMPLEMENTATION OF THE NEW SWITCHING CONVERTER AND FUTURE AREAS OF INVESTIGATIONS

The investigations made so far have opened up several new avenues for future research. The primary intention of this chapter is to outline briefly some of the leads which may be followed. For that reason, this chapter will be relatively short in scope, but nevertheless quite important in setting up the major thrust of future efforts.

These efforts may be classified in two main categories: theoretical and practical. From the practical viewpoint, various possibilities exist for the actual hardware implementation of the new converter topology (Fig. 12.2) besides the one already presented using a bipolar transistor and diode for the realization of the switch. The recent advent of switching power devices (transistors) in the metal-oxide-semiconductor (MOS) technology gives an alternative hardware realization, which looks very promising. Further study is necessary, however, to investigate the various trade-offs between the two technological implementations. The recent availability of the complete, signal processing (feedback control) part of the switching regulator (see Fig. 1.10 or Fig. 14.2), in a single integrated circuit makes the closed-loop regulator implementation of the new converter extremely convenient and further reduces the total size and weight of the regulator.

From the theoretical viewpoint, several areas are now immediately open for detailed analysis. The basic foundations are already firmly laid out for modelling of the new converter in the

discontinuous conduction mode and only the detailed work remains. Then, analysis and design of switching regulators incorporating the new converter and also several feedback loops becomes feasible for both conduction modes.

Finally, the search for new, innovative converter topologies can be continued. Possible modifications of the new converter or some other converter topologies are being sought which could include some desirable properties, such as input-output isolation and its corollary, the multi-output feature.

14.1 Implementation of the new converter with VMOS power transistors

Metal-oxide-semiconductor technology was considered until recently only applicable to small-signal, low-power devices, but it is now making inroads into the high-power field through the family of VMOS (vertical MOS) power field-effect transistors. While bipolar transistors are current-controlled minority-carrier devices, the VMOS power field-effect transistors are voltage-controlled majority-carrier devices, which has many advantages. They have much higher input impedance, fast switching speed because of absence of minority carrier storage, and no secondary breakdown because of the negative temperature coefficient. Their switching speed (4 nsec typical) is one or two orders of magnitude faster than in comparable bipolar (200 nsec), hence the switching losses are significantly reduced. Therefore, the circuit hardware realization of the new converter topology (Fig. 12.2) using VMOS power transistor as shown in Fig. 14.1a

may have some advantages over the bipolar transistor implementation in Fig. 12.3.

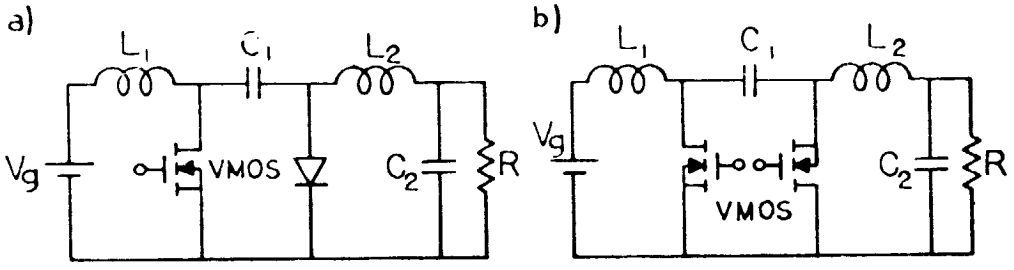


Fig. 14.1 Implementation of the new converter in Fig. 10.2 by different technological realization of the switch S using VMOSFET power transistors.

As seen in Fig. 14.1b there is also the possibility of replacing the diode by another VMOS power transistor. The two transistors are then voltage driven oppositely, when one transistor is on, the other is off and vice versa. The converters in Fig. 14.1 can be implemented by use of the state-of-the-art VMOS power transistor VMP1 (25 watts) from Siliconix, Inc.

14.2 Closed-loop switching regulator implementing the new converter

In Fig. 14.2 it is shown how this new converter can be incorporated in the complete closed-loop switching regulator. For a further reduction in size, the integrated circuit incorporating a pulse-width-modulator (PWM), feedback circuitry, power transistor and diode on a single integrated circuit (Texas Instruments TL 497C) is used.

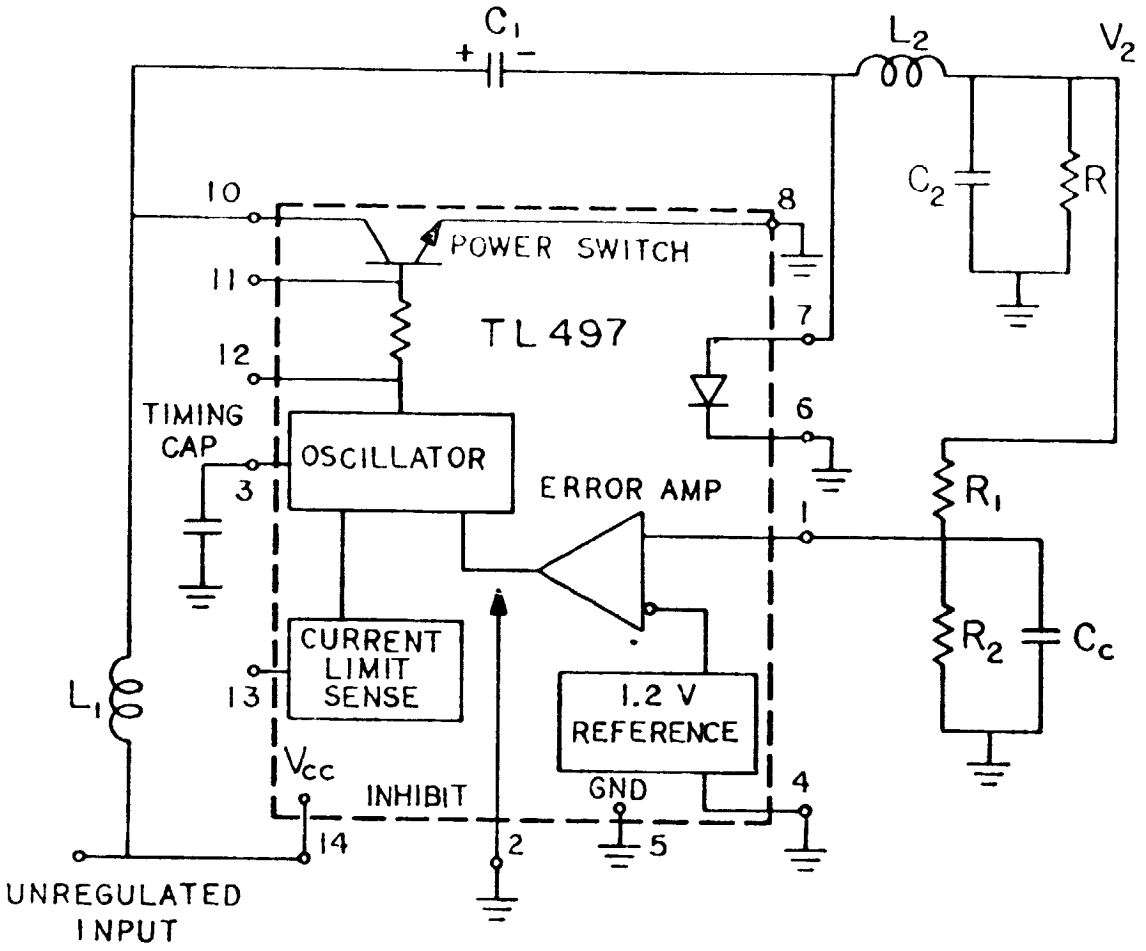


Fig. 14.2 Closed-loop switching regulator implementing new converter and integrated feedback control circuitry.

The output dc voltage V_2 is then determined by

$$V_2 = \left(1 + \frac{R_1}{R_2}\right) V_{REF} \tag{14.1}$$

where V_{REF} is the internal reference voltage of $V_{REF} = 1.2V$. By use of the modelling technique of Part I and Part II, the converter canonical circuit model can be obtained and the proper feedback compensation designed with the help of feedback analysis in Chapters 5 and 9. Two or more feedback loops may be considered also.

14.3 Discontinuous conduction mode in the new converter

The new converter (Fig. 12.3) may be considered as consisting of a boost power stage followed by a buck power stage, as was explained in Chapter 12. Then, we can define the dimensionless parameter K_2 for the output (buck) power stage as

$$K_2 = \frac{2L_2}{R} f_s \qquad (14.2)$$

which will determine with the help of Table VIII (Chapter 8) whether or not the output buck power stage is in discontinuous conduction mode. If it is, Table VI is instructive in defining the model of the output (buck) power stage.

It has been shown (Chapters 5 and 9) that the open-loop low-frequency input impedance R_{in} of a buck converter is

$$R_{in} = \frac{R}{M^2} \qquad (14.2)$$

where M is the dc gain of buck power stage. Since R_{in} is now the dc load for the input boost converter, we can define another dimensionless parameter K_1 for the boost power stage as

$$K_1 = \frac{2L_1}{R_{in}} f_s \qquad (14.3)$$

which will now determine when the input boost power stage is operating in discontinuous conduction mode and will define its model, by use of Table VIII and Table VI respectively.

This now illustrates how the analysis of complex problems can be broken down into analysis of simpler ones, and at the same time

demonstrates the power of the complete model representation, which also includes the converter input properties.

14.4 Search toward new, innovative converter topologies

There are some desirable converter properties, which have not yet been discussed. Namely, all the converters considered so far, including the new converter, have common ground for both input (source voltage) and output (load) circuit. However, there are some converters having the so-called isolation property, which allows the unregulated source voltage ground to be isolated from the load ground. For example, a simple modification of the conventional buck-boost converter in Fig. 1.1b can be made to include this isolation property between the input and output, and is shown in Fig. 14.3.

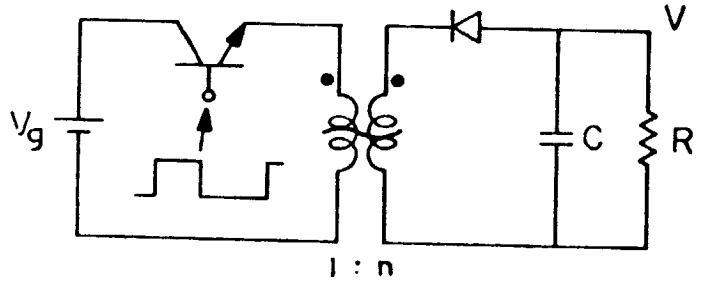


Fig. 14.3 Conventional buck-boost modified to include the isolation property.

Comparison of Fig. 14.3 with Fig. 1.1b shows that the modification consists only in replacing the original energy transferring inductance by a transformer with 1:n turns ratio. Moreover this turns ratio now proportionally affects the dc gain and appears as another controlling factor besides duty ratio D. Hence, by adding another

secondary circuit, two converter outputs at different dc level could be obtained. Then, this multi-output feature comes almost as a by-product of the isolation property of the converter. Both of these properties are very desirable for some applications.

The natural question now arises: is it possible to build this desirable isolation property into the new converter of Fig. 12.3 by some appropriate modification of (or addition to) its topology? If it is not possible, could some other converter topology based also on the capacitive energy transfer (for basic dc conversion realization) be devised which includes the isolation property? Perhaps, the less ambitious goal of achieving only the multi-output feature without the isolation property in the new converter is feasible.

The search for new innovative switching converter topologies continues...

CONCLUSION

A general unified approach to modelling switching converters has been developed which is directly applicable to any dc-to-dc converter operating in either of the two conduction modes. Despite its remarkable simplicity, the method is shown to be accurate enough for all practical purposes, since its primary assumption of small switching ripple is also the main requirement for acceptable converter performance. Both state-space averaged models and their corresponding circuit realizations provide the circuit designer with a powerful tool for both analysis (as demonstrated in Parts I and II) and synthesis (as demonstrated in Parts III and IV) of existing as well as new converter topologies.

The importance of the completeness of the circuit model realization, versus its representation through transfer functions only, cannot be overemphasized since it may be compared, for example, with complete linear circuit model of a transistor (which besides transfer properties, properly represents both input and output properties as well), versus its gain-frequency response only.

The benefits of the state-space averaging technique can now be applied in several areas:

(1) development of comparative criteria and design tools based upon the canonical models;

(2) extension and development towards modelling and analysis of dc-to-ac and ac-to-dc inverters;

(3) search for innovations in power processing techniques.

By use of canonical circuit models to represent the input and the transfer properties of a general class of dc-to-dc converters in both continuous and discontinuous conduction modes, the way is now clear to apply these models in development of design optimization tools and comparative criteria for a wide range of switching regulators.

In particular, it is now possible to make an informed selection of the optimal conduction mode for a given application. It is sometimes suggested that the discontinuous conduction mode has a number of advantages with respect to frequency response; however, the new canonical models indicate that this is only part of the story in that the benefits might be outweighed by other disadvantages.

Again as a consequence of the canonical models, it is now possible to make a comparative classification of all known dc-to-dc converters, regardless of their apparent complexity. Since some configurations have undesirable factors in their duty ratio frequency response (right half-plane zeros), it is important to know whether the resulting much more severe regulator stability conditions are outweighed by other performance advantages.

Finally, in direct application of the canonical models, system optimization of switching regulators can be investigated, in that the relative merits of fixed and variable frequency operation, and one- or two-loop feedback, can be also evaluated.

In the area of dc-to-ac and ac-to-dc inverters, much work remains to be done, but there is a strong expectation that the present state-space averaging techniques can be extended to include their analysis

and design.

In Parts III and IV it has been demonstrated how these modelling techniques can effectively be used in the search for new, innovative converter topologies.

The insights that have emerged from the general state-space modelling approach suggest (as illustrated in Chapter 14, for example) that there are still some features yet to be desired in switching converters not realized by the new optimum topology converter. Hence, there is a whole field of new switching dc-to-dc converters yet to be discovered. This encourages a renewed search for innovative circuit designs (or modification of existing ones) in a field which is yet young, and promises to yield a significant number of inventions in the stream of its full development. This progress will naturally be fully supported by new technologies coming at an ever-increasing pace. However, even though the efficiency and performance of currently existing converters will increase through better, faster transistors, more ideal capacitors (with low ESR) and so on, it will be primarily the responsibility of the circuit designer and inventor to put these components to best use in a topology which is optimal with respect to the given performance requirements. Search for new converters, and how best to use present and future technologies, will be of prime importance in achieving the ultimate goal of near-ideal general switching dc-to-dc converters.

APPENDICES

APPENDICES

In the sequence of Appendices A, B and C several of the questions related to substitution of the two switched models (3.1) by the state-space averaged description (3.3) for the continuous conduction operation in which two structural changes occur within each period are thoroughly discussed. Then, in Appendix D the state-space averaging step is naturally extended to include the multi-structural change (three or more different topological configurations) within each period. This also serves as a basis for development in Part II of modelling procedures for switching converters operating in the discontinuous conduction mode.

It has already been shown in Chapter 1 that the requirement on negligible switching ripple imposes inequality restrictions (1.11) on the choice of parameter values, namely $f_c << f_s$ and $\omega_\alpha << f_s$. In Appendix A it is demonstrated that under the same inequality conditions (1.11) the fundamental matrix e^{AT_s} can be approximated to a very high degree of accuracy by its first-order linear term $I + AT_s$. This is confirmed both analytically and quantitatively (numerically), for a typical set of parameter values and operating conditions for a boost converter, though it is readily applicable to any other converter configuration.

These linear approximations of the fundamental matrices $e^{A_1T_s}$ and $e^{A_2T_s}$ lead naturally in Appendix B to the state-space averaging step (3.2) or (3.3). The evolution of the state-variables during each period T_s, originally governed by two linear system descriptions (3.1) is with the help of these linear approximations substituted by

a single linear description (3.2) which very accurately models the overall dynamics (with switching ripple being neglected and "smoothed out").

Appendix C provides an excellent theoretical confirmation of the validity of the state-space averaging step and the high accuracy of the derived results. Namely, through a rather elaborate procedure and quite cumbersome expressions, the steady-state (dc) conditions can be found exactly by proper matching of the boundary conditions as shown in Appendix C. In general, besides depending on steady-state duty ratio D, load R and parasitic resistances, the exact dc conditions also depend on the storage element values and switching frequency f_s in a rather complicated fashion. However, under the linear approximation of the exponential matrices, these additional dependencies disappear, the dc conditions become dependent on duty ratio D, load R and parasitic resistances only, and reduce analytically to the same expressions as those predicted by the state-space averaged model. In addition, the exact dc conditions serve as a good quantitative measure of the high accuracy of the results obtained via state-space averaging and offer a quantitative insight into its basic underlying requirement, inequalities (1.11).

In Appendix D the state-space averaging step is generalized to multistructural converter configurations. In particular, the state-space averaged model for converters with three structural changes within each period is derived analogously as in Appendix B. As an example, the cascade connection of boost and buck converters (both operating in continuous conduction mode) is shown to generate,

under special driving conditions of the two switches, either three or four different topological configurations. Finally, the state-space averaging step is demonstrated for the generalized switching converter with n topological structural changes within each switching period.

APPENDIX A

On the linear approximation of the fundamental matrix

From the well-known body of linear system theory the exponential (fundamental) matrix e^{AT_s} can be expressed in terms of an infinite convergent series as:

$$e^{AT_s} = I + AT_s + A^2T_s^2/2! + A^3T_s^3/3! + \ldots \qquad (A.1)$$

which in form very much resembles its scalar counterpart (expansion of $e^{\alpha t}$ in an infinite series). The fundamental question we now ask is: when can this exponential matrix be satisfactorily approximated by its first-order term (linear in T_s)? Note that it is not enough merely to specify T_s being very small, but rather small in comparison with some other quantities dependent on matrix A (compare with the simple scalar case). In addition, the question of how good the linear approximation will be for a given T_s and A ought to be answered quantitatively.

We now demonstrate the answer to these questions on a boost circuit example (see Fig. 3.1 and Fig. 3.2), in which for simplicity of presentation $R_\ell = 0$ and $R_c = 0$ is assumed. The two matrices A_1 and A_2 of (3.17) then become:

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \qquad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad (A.2)$$

The exponential matrix e^{AT_s} can be found in a closed form using an alternative definition to (A.1), that is

$$e^{AT_s} = \mathcal{L}^{-1}[(sI-A)^{-1}] \tag{A.3}$$

where operator $\mathcal{L}^{-1}$ denotes inverse Laplace transformation, while s is complex frequency. By applying (A.3) to (A.2) we obtain <u>closed form</u> expressions for the exponential matrices $e^{A_1DT_s}$ and $e^{A_2D'T_s}$ as shown in (A.4).

$$e^{A_1DT_s} = \begin{bmatrix} 1 & 0 \\ 0 & e^{-2\omega_\alpha DT_s} \end{bmatrix} =$$

$$e^{A_sD'T_s} = e^{-\omega_\alpha D'T_s}\begin{bmatrix} \cos\omega_o D'T_s + \frac{\omega_\alpha}{\omega_o}\sin\omega_o D'T_s & -\frac{\sin\omega_o D'T_s}{\omega_o L} \\ \frac{\sin\omega_o D'T_s}{\omega_o C} & \cos\omega_o D'T_s - \frac{\omega_\alpha}{\omega_o}\sin\omega_o D'T_s \end{bmatrix} \tag{A.4}$$

where

$$\omega_\alpha = \frac{1}{2RC}, \qquad \omega_o = \sqrt{\frac{1}{LC} - \omega_\alpha^2} \tag{A.5}$$

Suppose now that the switching frequency $f_s = 1/T_s$ is sufficiently greater than the natural frequencies ω_α and ω_o of the converter, such that

$$\omega_o D'T_s << 1 \qquad \text{and} \qquad \omega_\alpha D'T_s << 1 \tag{A.6}$$

Then, by introduction of the linear approximations

$$e^{-2\omega_\alpha DT_s} \sim 1-2\omega_\alpha DT_s, \quad \cos\omega_o D'T_s \sim 1, \quad \sin\omega_o D'T_s \sim \omega_o D'T_s \tag{A.7}$$

matrices in (A.4) reduce to:

$$I + A_1 DT_s = \begin{bmatrix} 1 & 0 \\ 0 & 1 - \frac{DT_s}{RC} \end{bmatrix} \qquad I + A_2 D'T_s = \begin{bmatrix} 1 & -\frac{D'T_s}{L} \\ \frac{D'T_s}{C} & 1 - \frac{D'T_s}{RC} \end{bmatrix} \tag{A.8}$$

Let us now calculate the exact exponential matrices (A.4) and the approximate ones (A.8) for the typical numerical values used in a practical boost converter

$$L = 6\text{mH}, \quad C = 45\mu\text{F}, \quad R = 30\Omega, \quad D = 0.25, \quad V_g = 37.5\text{V} \tag{A.9}$$

and with constant switching frequency $f_s = 10\text{kHz}$. The following results are obtained:

$$e^{A_1 DT_s} = \begin{bmatrix} 1.0 & 0 \\ 0 & .982 \end{bmatrix} \qquad e^{A_2 D'T_s} = \begin{bmatrix} 0.99 & -1.21\times10^{-2} \\ 1.616 & 0.936 \end{bmatrix} \tag{A.10}$$

$$I + A_1 DT_s = \begin{bmatrix} 1.0 & 0 \\ 0 & 0.982 \end{bmatrix} \qquad I + A_2 D'T_s = \begin{bmatrix} 1.0 & -1.25\times10^{-2} \\ 1.667\Omega & 0.944 \end{bmatrix}$$

while natural frequencies f_α and f_o computed from (A.5) are $f_\alpha = 370/2\pi\text{Hz}$ and $f_o = 306\text{Hz}$. Note also that $f_c = 1/2\pi\sqrt{LC} \sim 306\text{Hz}$ is very closely approximated by f_o.

From (A.10) it becomes obvious that the linear approximations for the fundamental matrices

$$e^{A_1 DT_s} \sim I + A_1 DT_s \qquad e^{A_2 D'T_s} \sim I + A_2 D'T_s \tag{A.11}$$

will introduce insignificant error (less than 2%) since the following inequality conditions are well satisfied:

$$\frac{\omega_\alpha}{f_s} = 0\ 037 << 1 \qquad \text{and} \qquad \frac{f_c}{f_s} = 0.0306 << 1 \tag{A.12}$$

Hence, even for the natural frequencies ω_α and f_c slightly more than a decade apart from the switching frequency f_s, satisfactory results are obtained using linear approximations for the exponential matrices.

APPENDIX B

The fundamental approximation in the state-space averaging approach

Consider now that a switching dc-to-dc converter operating in the continuous conduction mode is described by the following state-space equations for the two switched models:

$$\begin{aligned} \dot{x}_1 &= A_1 x_1 + b_1 v_g \quad \text{for interval } T_s d, \ (0 \leq t \leq t_1) \\ \dot{x}_2 &= A_2 x_2 + b_2 v_g \quad \text{for interval } T_s d', \ (t_1 \leq t \leq T_s) \end{aligned} \tag{B.1}$$

Here the state-variable vector x is denoted by x_1 for interval $T_s d$ $(0 \leq t \leq t_1)$, and by x_2 for interval $T_s d' (t_1 \leq t \leq T_s)$ to distinguish clearly the solutions in the two regions and to make their connection by matching boundary conditions at $t = t_1$ more visible.

The solutions of (B.1) can easily be found in terms of exponential matrices and convolution integrals as

$$\begin{aligned} x_1(t) &= e^{A_1 t} x_1(0) + \int_0^t e^{A_1(t-\tau)} b_1 v_g d\tau \qquad \text{for } (0 \leq t \leq t_1) \\ x_2(t) &= e^{A_2(t-t_1)} x_2(t_1) + \int_{t_1}^t e^{A_2(t-\tau)} b_2 v_g d\tau \qquad \text{for } (t_1 \leq t \leq T_s) \end{aligned} \tag{B.2}$$

With the assumption that v_g is almost constant (small signal assumption on $v_g = V_g + \hat{v}_g$ where $\hat{v}_g \ll V_g$) so that it can be taken outside the integrals, and by introduction of the substitutions

$$B_i(t) = \int_0^t e^{A_i \tau} d\tau = A_i^{-1}(e^{A_i \tau} - I) \qquad \text{for } i = 1,2 \tag{B.3}$$

into (B.2), the solutions become:

$$x_1(t) = e^{A_1 t} x_1(0) + v_g B_1(t) b_1 \qquad \text{for } t \in [0, t_1]$$
$$x_2(t) = e^{A_2(t-t_1)} x_2(t_1) + v_g B_2(t-t_1) b_2 \qquad \text{for } t \in [t_1, T_s] \tag{B.4}$$

This is pictorially represented in Fig. B.1, which shows how the first equation in (B.4) carries initial state-vector $x_1(0)$ across interval $T_s d$ into the $x_1(t_1)$ state-vector and how the second equation carries it further into $x_2(T_s)$ during the subsequent interval $T_s d'$.

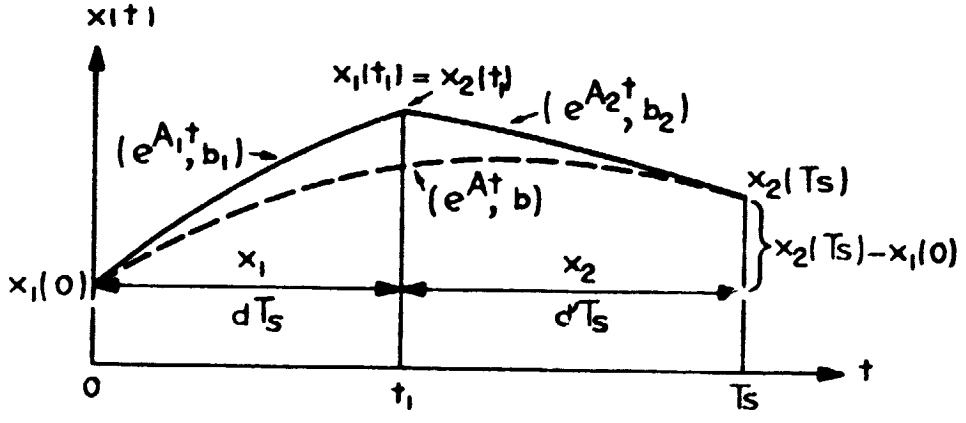


Fig. B.1 Pictorial representation of the evolution of the state vector x(t) from the original switched network description (heavy line) and its state-space averaged model description (dotted line).

By definition, state variables cannot change instantaneously (like inductor currents and capacitor voltages), hence the vector of state-variables is continuous across the switching instant t_1, or

$$x_1(t_1) = x_2(t_1) \tag{B.5}$$

which has also been displayed in Fig. B.1. With use of (B.5) in (B.4), the state-vector $x_2(T_s)$ is determined as:

$$x_2(T_s) = e^{A_2 d' T_s} e^{A_1 d T_s} x_1(0) + v_g [e^{A_2 d' T_s} B_1(dT_s) b_1 + B_2(d'T_s) b_2] \tag{B.6}$$

Introduction of linear approximations (A.11) and retention of only the first-order terms transforms (B.6) into:

$$x_2(T_s) \sim (I + dA_1T_s + d'A_2T_s)x_1(0) + v_g[db_1T_s + d'b_2T_s] \qquad (B.7)$$

However, the same equation could be obtained for any switching period, say n-th by simple substitutions $x_1(0) = x(nT_s)$, $x_2(T_s) = x[(n+1)T_s]$ which, after suitable rearrangement of (B.7), produce:

$$\frac{x[(n+1)T_s] - x(nT_s)}{T_s} = (dA_1+d'A_2)x(nT_s) + v_g(db_1+d'b_2) \qquad (B.8)$$

With the definition of the derivative

$$\dot{x}(nT_s) = \frac{x[(n+1)T_s] - x(nT_s)}{T_s} \qquad (B.9)$$

we define a <u>continuous</u> system corresponding to (B.8):

$$\dot{x} = Ax + bv_g \quad \text{where} \quad \begin{cases} A = dA_1 + d'A_2 \\ b = db_1 + d'b_2 \end{cases} \qquad (B.10)$$

We have, finally, succeeded in substituting the original two state-space models (B.1) by a single continuous state-space averaged model (B.10) using only linear approximations of the exponential matrices (A.11) which are shown in Appendix A to be very accurate.

The meaning of the state-space averaged model (B.10) should be understood in the following way. Even though its instantaneous state-vector x(t) (shown by dotted lines in Fig. B.1) may differ from the evolu tion of the state vector in the original system (B.1) (shown in heavy lines in Fig. B.1) inside the switching period T_s,

it very accurately carries the starting state $x(nT)$ into final state $x[(n+1)T]$. In essence it effectively "smooths out" the switching ripple superimposed on its dynamic motion, as clearly displayed in an exaggerated fashion in Fig. B.1. The actual switching ripple, however, is much smaller than that shown in Fig. B.1 since it is dictated by tight performance requirements in practical converters (switching ripple usually on the order of 0.01%). This negligible switching ripple is in fact what justifies the state-space averaged model (B.10) (shown in dotted lines in Fig. B.1) which assumes zero switching ripple.

It is interesting to point out that in going from (B.6) to (B.7) some second order terms (proportional to T_s^2) could have been retained. However, the very marginal added accuracy would not justify the tremendous complexity introduced into the model. All the desirable properties of the model (B.10) (equivalent circuit interpretations, general state-space averaged model, canonical circuit model) as well as simplicity of the procedure would have been lost -- sacrificed merely for the sake of a tiny correction term which is negligible anyway (its effect being much smaller than even component tolerances effect).

Another property of model (B.10) quickly arises. If we had considered first the "off" interval and then the "on" interval in matching boundary conditions, the following equation corresponding to (B.6) would have been obtained:

$$x(T_s) = e^{A_1 dT_s} e^{A_2 d'T_s} x(0) + v_g[e^{A_1 dT_s} B_2(d'T_s)b_2 + B_1(dT_s)b_1] \quad (B.11)$$

However, use of linear approximations (A.11) and retention of only the first-order terms again results in (B.7). Hence, the state-space averaged model (B.10) is indistinguishable with respect to which interval was considered to be first, whether interval (dT_s) was followed by interval ($d'T_s$), or vice versa. However, if the second-order terms are retained, a distinction between models derived from (B.6) and (B.11) would exist.

From comparison of the solution of (B.10)

$$x(T_s) = e^{AT_s}x(0) + \int_0^{T_s} e^{A(T_s-\tau)} bv_g d\tau$$

with (B.6) or (B.11), the problem of modelling can be partly stated in the following way: can a matrix A be found such that

$$e^{AT_s} = e^{A_2 d'T_s} e^{A_1 dT_s} \tag{B.12}$$

The general result is provided by the Baker-Campbell-Hausdorff series [5] for the matrix A:

$$AT_s = (dA_1+d'A_2)T_s + dd'(A_1A_2-A_2A_1)T_s^2+\ldots \tag{B.13}$$

For switching converter applications, the second-order term is negligible, resulting in

$$A = dA_1 + d'A_2 \tag{B.14}$$

as obtained before using linear approximations (A.11). The result (B.14) even becomes exact when the matrices involved are commutative, that is when $A_1A_2 = A_2A_1$. This is the case, for example, for the buck converter in which $A_1 = A_2 = A$.

It remains, finally, to incorporate into model (B.10) the cases when the output quantity does not coincide with any of the state variables (as in, for example, the boost converter of Fig. 3.1). Since, during the interval $T_s d$ the output quantity becomes $y_1 = c_1^T x$ while during the interval $T_s d'$ it is $y_2 = c_2^T x$, the output quantity y over the whole period T_s is taken to be their average, or

$$y = dy_1 + d'y_2 = (dc_1^T + d'c_2^T)x \tag{B.15}$$

and with (B.10) completes the state-space averaging step (3.2) or (3.3).

APPENDIX C

Derivation of the exact dc conditions and their simplification under linear approximation of the exponential matrices

We now derive the exact steady-state (dc) conditions from the general state-space description (B.1) of the two switched circuit models. Since for steady-state $v_g = V_g$ (dc voltage only) and $d = D$, the exact solutions analogous to (B.4) are obtained as

$$x_1(t) = e^{A_1 t} x_1(0) + V_g B_1(t) b_1 \qquad \text{for } t \in [0, t_1] \tag{C.1}$$

$$x_2(t) = e^{A_2(t-t_1)} x_2(t_1) + V_g B_2(t-t_1) b_2 \qquad \text{for } t \in [t_1, T_s]$$

where $$B_i(t) = \int_0^t e^{A\tau} d\tau$$

Solutions (C.1) contain two yet undetermined constants, $x_1(0)$ and $x_2(t_1)$. We therefore impose two boundary conditions:

(a) the vector of state variables is continuous across the switching instant t_1, since the inductor currents and capacitor voltages cannot change instantaneously.

Hence
$$x_1(t_1) = x_2(t_1) \tag{C.2}$$

(b) from the steady state requirement, all the state variables should returr after period T_s to their initial values. Hence:

$$x_1(0) = x_2(T_s) \tag{C.3}$$

The boundary conditions (C.2) and (C.3) are illustrated in Fig. C.1, where $v(0) = v(T_s)$, $i(0) = i(T_s)$ and $i(t)$ and $v(t)$ are continuous across the switching instant t_1.

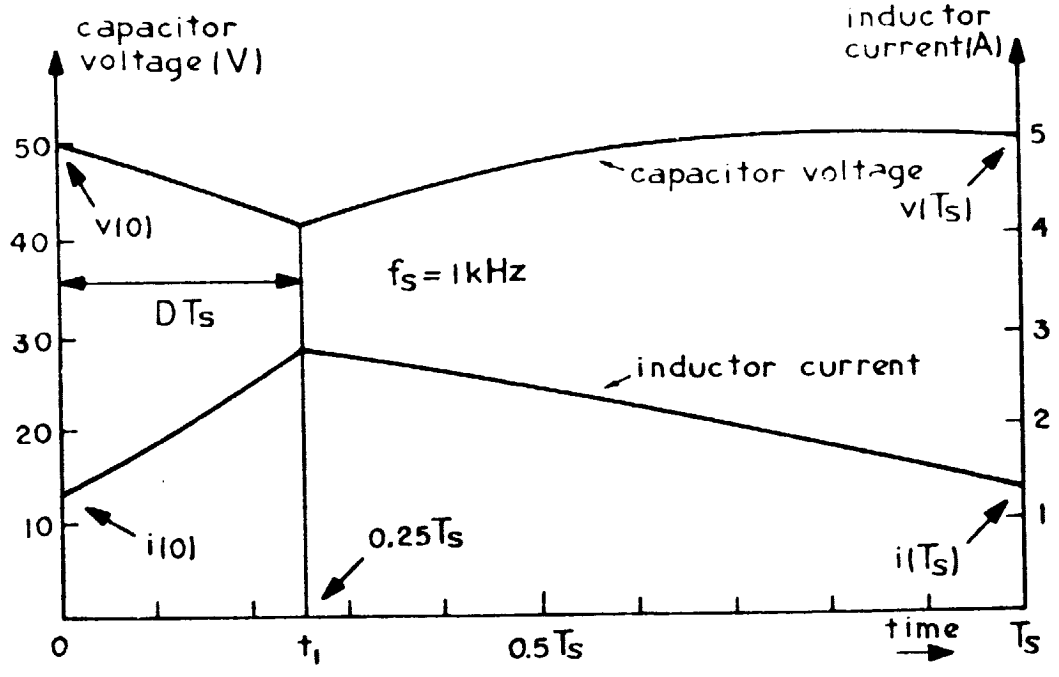


Fig. C.1 Typical state-variable time dependence over a single period T_s in the steady-state, for the boost circuit numerical example with f_s = 1kHz.

Insertion of (C.2) and (C.3) into (C.1) results in solution for the initial condition $x_1(0)$ as well as the other constant $x_2(t_1)$:

$$x_1(0) = x_2(T_s) = V_g(I - e^{D'A_2T_s}e^{DA_1T_s})^{-1}(e^{D'A_2T_s}B_1(DT_s)b_1 + B_2(D'T_s)b_2) \tag{C.4}$$

$$x_2(t_1) = x_1(t_1) = e^{A_1DT_s}x_1(0) + V_gB_1(DT_s)b_1$$

It was already demonstrated in Appendix A that closed-form exp ssions for the fundamental matrices can be found, as in (A.3).

Moreover, the same is true for $B_i(t)$ since

$$B_i(t) = \int_0^t e^{A_i\tau} d\tau = A_i^{-1}(e^{A_i t} - I), \qquad i = 1,2 \tag{C.5}$$

provided inverse matrices A_i^{-1} (i=1,2) exist. Hence a closed form solution for initial conditions is obtained. Then, with use of (C.1) and (C.4), the instantaneous state-vectors $x_1(t)$ and $x_2(t)$ can be plotted via a computer program.

In particular, for the boost circuit example of Fig. 3.1,a computer program RIPPLE (attached to the Appendices) was made. In addition to the parameter values shown in (A.9), $R_\ell = 0.46\Omega$ and $R_c = 0.28\Omega$ were adopted and for switching frequency $f_s = 1$kHz the inductor current and capacitance voltage waveforms of Fig. C.1 were generated using this program. The waveforms reveal a substantial output voltage ripple (almost 15%) since the inequality conditions (1.11) or (A.6) are not very well met.

We now proceed with derivation of the dc conditions. As seen from Fig. C.1, the average values of inductor current and capacitor voltage could be found by integration over the period T_s, and in general the steady-state vector X is found from:

$$X = \frac{1}{T_s}\left[\int_0^{t_1} x_1(\tau)d\tau + \int_{t_1}^{T_s} x_2(\tau)d\tau\right] \tag{C.6}$$

Even though the integration (C.6) using (C.1) and (C.4) seems complicated, it can actually be carried out with repeated use of result (C.5) to obtain

$$X(T_s) = \frac{1}{T_s}\left[B_1(DT_s)x_1(0)+B_2(D'T_s)x_2(t_1)+V_g\int_0^{DT_s} B_1(\tau)\,d\tau\, b_1+\int_0^{D'T_s} B_2(\tau)\,d\tau\, b_2\right] \tag{C.7}$$

where

$$\int_0^t B_i(\tau)\,d\tau = A_i^{-2}(e^{A_i t}-I) - tA_i^{-1} \quad \text{for } i = 1,2 \tag{C.8}$$

Equation (C.7) with the help of (C.4), (C.5) and (C.8) now completely determines the steady-state vector X(T) through the multiplication and inversion of the known matrices A_1 and A_2, vectors b_1 and b_2 and the exponential matrices $e^{A_1DT_s}$ and $e^{A_2D'T_s}$.

It is obvious from the complexity of (C.7) that $X(T_s)$ <u>in general</u> depends not only on D and various resistive elements, but also on all parameter values including storage elements L and C and on switching frequency f_s as well. Since the <u>exact</u> dc conditions represented by (C.7) appear to be quite complicated functions of switching frequency $f_s = 1/T_s$, one has to resort to the computer to obtain insight into that functional dependence. A computer program PBOOST (attached to these Appendices) was used to plot the output dc voltage obtained from (C.7) and the initial inductor current i(0) from (C.4) as functions of switching frequency $f_s = 1/T_s$ for the boost circuit example of Fig. 3.1. For the same parameter values used before, that is:

$$L = 6\text{mH}, \quad C = 45\mu\text{F}, \quad R = 30\Omega, \quad D = 0.25, \quad V_g = 37.5\text{V}, \quad R_\ell = 0.46\Omega, \quad R_c = 0.28\Omega \tag{C.9}$$

the computerized plot of Fig. C.2 results.

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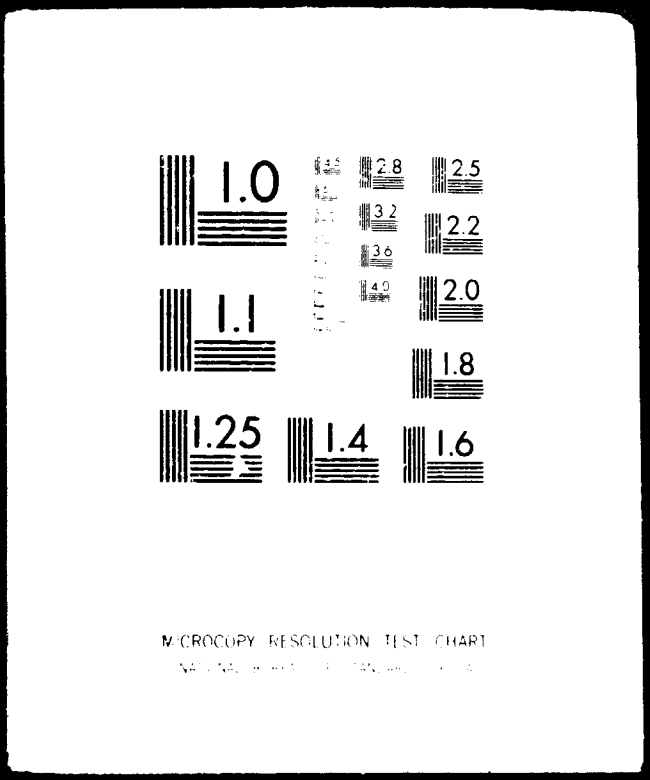

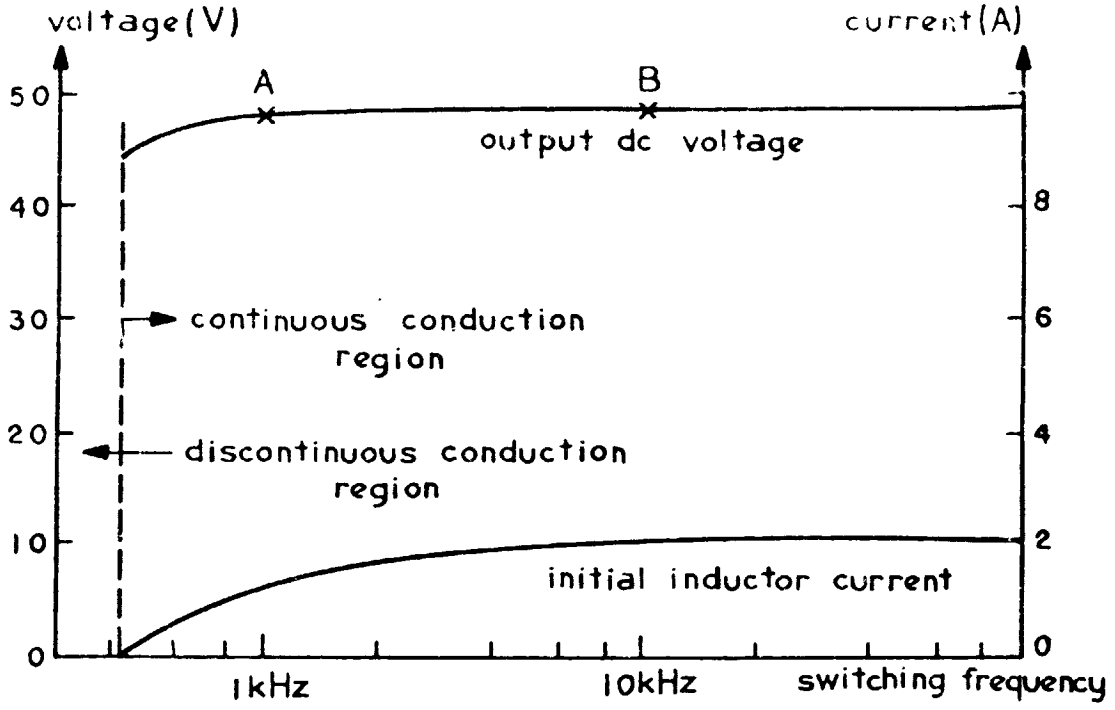

Fig. C.2 Typical dependence of the steady-state (dc) conditions (output voltage) on the switching frequency f_s in the continuous conduction region (to the right of the dotted line).

As seen from Fig. C.2, the point where the initial inductor current i(0) becomes zero determines the boundary between continuous and discontinuous conduction regions. Since the exact dc conditions (C.7) are implicitly applicable to the continuous conduction region only, this helps to contain the functional dependence (C.7) within region of its applicability. The actual dependence of dc conditions on switching frequency f_s in discontinuous conduction region shows grossly different behavior, as was shown in Part II.

From Fig. C.2 it is evident that the output dc voltage changes appreciably only when switching frequency f_s becomes close to the

filter corner frequency $f_c = 1/2\pi\sqrt{LC} = 306Hz$ or the effective filter corner frequency $f_o = D'f_c = 230Hz$, while for higher switching frequencies (to the right of point A in Fig. C.2) it becomes almost constant and for all practical purposes independent of f_s. Also at point A in Fig. C.2 ($f_s = 1kHz$) substantial ripples in the instantaneous output voltage and inductor current are observed, as was demonstrated by Fig. C.1. However, if all conditions (C.9) are retained but the switching frequency is increased to $f_s = 10kHz$ (point B on Fig. C.2), the plot of Fig. C.3 is obtained via a computer program RIPPLE.

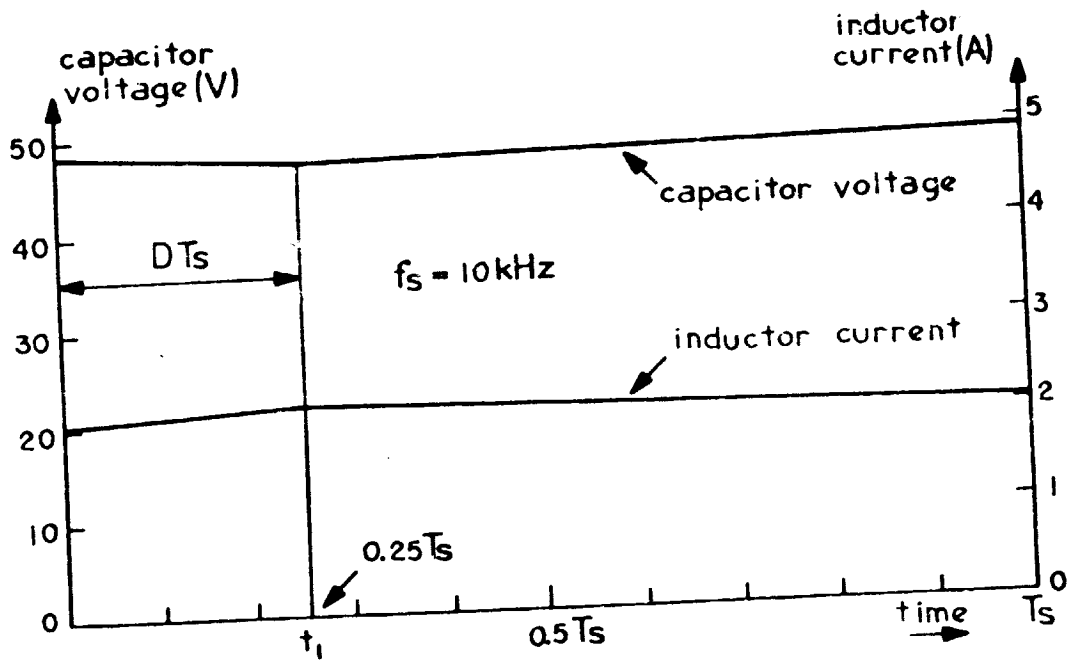

Fig. C.3 Same as Fig. C.1 but with $f_s = 10kHz$. Strong linearity and small ripple exhibited by the curves are consequences of $e^{AT_s} \approx 1 + AT_s$, since $f_c/f_s \ll 1$.

From Fig. C.3 it is clear that the switching ripple is substantially reduced and has become negligible since the inequality requirements (A.12) or (1.11) are well satisfied. Moreover the state variables show very strong linearity in the two intervals T_sD and T_sD' on Fig. C.3. This is by no means an accident, but a consequence of the fact that linear approximations of the fundamental matrices (A.11) are well satisfied at point B in Fig. C.2, as was verified in Appendix A. Hence the introduction of these linear approximations into (C.1) would bring a linear time-dependence of state variables and show as straight lines in Fig. C.3. Furthermore, the same linear approximations (A.11) when introduced into exact dc conditions (C.7), and upon retention of first order terms only, greatly simplify the steady state (dc) vector $X(T_s)$ to:

$$X = -A^{-1}bV_g \qquad \text{where} \qquad \begin{aligned} A &= DA_1 + D'A_2 \\ b &= Db_1 + D'b_2 \end{aligned} \tag{C.10}$$

It may seem surprising that the steady state vector X came out to be independent of period T_s or switching frequency f_s. However, it is exactly this equation (C.10) which models very accurately the most interesting region for practical purposes-- the flat portion of the dc output voltage shown in Fig. C.2 to the right of point A, where switching ripple becomes negligible and whicn is also practically independent of switching frequency f_s. It is interesting that (C.10) becomes an <u>exact</u> result when the limit $T_s \to 0$ is used on (C.7), that is

$$X = \lim_{T_s \to 0} X(T_s) \tag{C.11}$$

However, one does not have to go to infinite switching frequency, since the separation of the switching frequency from the natural frequencies f_α and f_c by more than a decade would lead to essentially constant steady state vector X given by (C.10), as illustrated in Fig. C.2.

Now a very interesting comparison with state space averaged model (B.10) developed in previous Appendix B can be made. Since in the steady state $x[(n+1)T_s] = x(nT_s)$, from (B.9) we obtain $\dot{x}(nT_s) = 0$ and (B.10) gives exactly the same result for steady state vector X as (C.10) (with, of course, substitutions $v_g = V_g$ and $d = D$ for dc regime) and also coincides with result (3.7) in Chapter 3.

After deriving the quite cumbersome exact dc conditions (C.7), one can truly appreciate the tremendous simplification achieved by using the simple result (C.10), which is shown to be justified for all cases of practical interest (negligible switching ripple). Moreover one can now fully recognize how powerful is the state-space averaged model (B.10) or (3.2). It not only serves to determine very accurately the dc conditions (steady state vector X) in a rather simple way, but also is the basis for development of a dynamic model of the switching converter as demonstrated in Chapters 3 and 4. In addition, both dc and ac small signal models are <u>consistent</u> with each other since they are obtained with the same degree of accuracy owing to the same crucial approximation (A.1).

The results of the sequence of Appendices A, B and C can now be very briefly and concisely summarized. The basic performance requirement for switching dc-to-dc converters of small (negligible) switching ripple is shown to be the underlying motive for the following sequence of cause and effect:

switching ripple small $\Rightarrow$ natural frequencies $\ll$ switching frequency $\Rightarrow$ fundamental matrices $\sim$

$\sim$ linear approximation $\Rightarrow$ state-space averaging step $\Rightarrow$ dc and ac small signal state-space averaged model

In conclusion, the recognition of this sequence of implications enabled extremely simple, powerful and very accurate scheme for modelling and analysis of switching converters to be devised. This scheme is now generalized in Appendix D to switching converters with multistructural topological change.

APPENDIX D

State-space averaging step extended to converters with multistructural (three or more) topological changes within each period

We now derive the state-space averaging step for switching converters characterized by three structural changes within each switching period. Each topological structure can be described as before by linear state-space equations, hence

$$\begin{aligned}
\dot{x}_1 &= A_1x_1 + b_1v_g \qquad \text{for interval } d_1T_s, \quad (0 \le t \le t_1) \\
\dot{x}_2 &= A_2x_2 + b_2v_g \qquad \text{for interval } d_2T_s, \quad (t_1 \le t \le t_2) \\
\dot{x}_3 &= A_3x_3 + b_3v_g \qquad \text{for interval } d_3T_s, \quad (t_2 \le t \le T_s)
\end{aligned} \tag{D.1}$$

In contrast to the previous derivation, two boundary conditions are now imposed. Since the state-space vector is continuous in transition from first to second and from second to third regions

$$\begin{aligned}
x_2(t_1) &= x_1(t_1) \\
x_3(t_2) &= x_2(t_2)
\end{aligned} \tag{D.2}$$

Solution of (D.1) under the small signal assumption for $\hat{v}_g$ (where $v_g = V_g + \hat{v}_g$ and $\hat{v}_g << V_g$) yields

$$\begin{aligned}
x_1(t) &= e^{A_1t}x_1(0) + v_gB_1(t)b_1 && \text{for } t \in [0,t_1] \\
x_2(t) &= e^{A_2(t-t_1)}x_2(t_1) + v_gB_2(t-t_1)b_2 && \text{for } t \in [t_1,t_2] \\
x_3(t) &= e^{A_3(t-t_2)}x_2(t_2) + v_gB_3(t-t_2)b_3 && \text{for } t \in [t_2,T_s]
\end{aligned} \tag{D.3}$$

where

$$B_i(t) = \int_0^t e^{A_i\tau} d\tau , \qquad i = 1,2,3 \tag{D.4}$$

Use of boundary conditions (D.2) in (D.3) gives

$$x_3(T_s) = e^{A_3d_3T_s}e^{A_2d_2T_s}e^{A_1d_1T_s}\, x_1(0) + v_g[e^{A_3d_3T_s}e^{A_2d_2T_s}B_1(d_1T_s)b_1 + e^{A_3d_3T_s}B_2(d_2T_s)b_2 + B_3(d_3T_s)b_3] \tag{D.5}$$

With introduction of the linear approximations

$$e^{A_id_iT_s} \sim I + A_id_iT_s , \qquad i = 1,2,3 \tag{D.6}$$

into (D.4) and (D.5), and after retention of only first-order terms (linear in T_s), (D.5) reduces to

$$x_3(T_s) = (I+d_1A_1+d_2A_2+d_3A_3)x_1(0) + (d_1b_1+d_2b_2+d_3b_3)v_g \tag{D.7}$$

This, as explained before in Appendix B, leads to a single continuous linear system

$$\dot{x} = Ax + bv_g \quad \text{where} \quad \begin{aligned} A &= d_1A_1 + d_2A_2 + d_3A_3 \\ b &= d_1b_1 + d_2b_2 + d_3b_3 \end{aligned} \tag{D.8}$$

which, within the accuracy of approximations (D.6), models the dynamic and static behavior of the system originally described by periodic change among the three linear systems (D.1).

As an illustration of a switching converter with such multi-structural change, consider the converter shown in Fig. D.1a whose two switches S_1 and S_2 are driven as specified in Fig. D.1b. The two switches S_1 and S_2 are shown in their "on" position in Fig. D.1a.

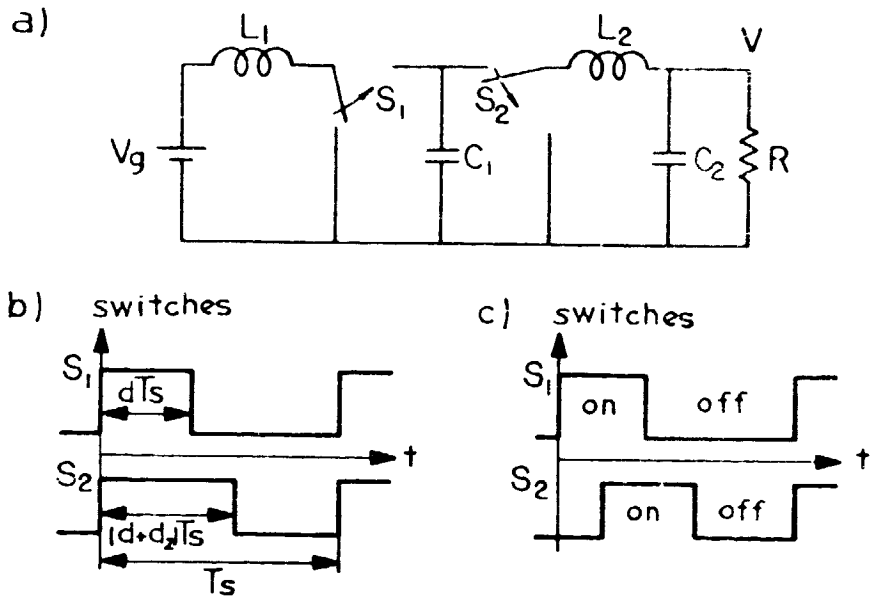

Fig. D.1 Switching converter exhibiting multistructural change: a) boost converter cascaded by a buck converter b) switch drive for "three state" behavior c) switch drive for "four state" behavior.

It can easily be recognized that this converter is actually a boost converter cascaded by a buck converter whose switches are driven synchronously but with different duty ratios, d_1 and d_1+d_2 respectively. This is in contrast to the case discussed at length in Part III, where both switches have the same duty ratio and for which only two switched networks need be distinguished.

However, if this converter is looked upon as single system, the switching action of Fig. D.1b would produce periodic sequential change among three different structures (shown in Fig. D.2 b,c, and d), while that of Fig. D.1c would produce periodic sequential change among all four different switched networks of Fig. D.2. In any case, it demonstrates the feasibility of realization of the generalized

switching converter of Fig. 1.11 having three or more switched network configurations, even in the continuous conduction mode of operation. Naturally, result (D.8) is then directly applicable to the situation in Fig. D.1b provided the converter is operating as a whole in the continuous conduction mode of operation (ensuring that only those switched networks of Fig. D.2 b,c and d actually exist).

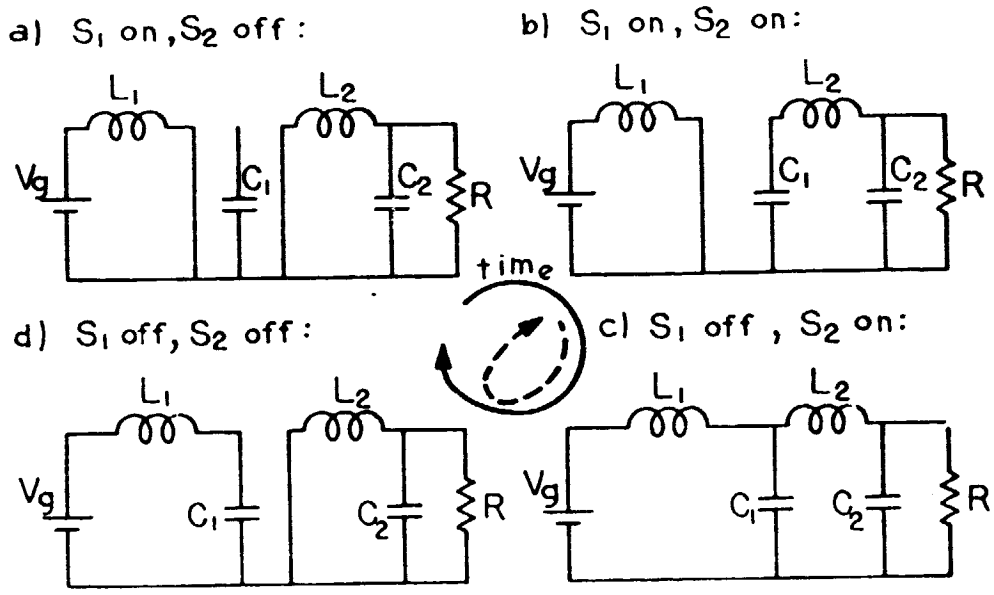

Fig. D.2 Various switched networks for the converter in Fig. D.1a.

On the other hand if the converter is looked upon as consisting of cascaded boost and buck converters and each of them has been modelled separately as a "two-state" converter following Part I, and their models put together, the same result would have been obtained.

Other examples of "three-state" switching converters are the familiar common power stages (buck, boost and buck-boost of Fig. 1.1) operating in the discontinuous conduction mode as demonstrated in Chapter 1. However, even though the three different switched

networks are also clearly distinguished (compare with Fig. 1.7 for example) the discontinuous conduction mode represents a rather special case of the "three-state" converter. While in ordinary "three-state" converters (like that demonstrated by Fig. D.1a, b and Fig. D.2b, c and d) all the state variables (inductor currents and capacitor voltages) retain their essential properties which characterize them as state-space quantities (free, independent initial and final conditions) this is not so for discontinuous conduction operation. Namely, the inductor current is forced to have zero initial and final condition (compare Fig. 1.6 for example). Hence, inductor current which becomes discontinuous ceases to be a true state-variable. Therefore, in addition to the state-space averaging step (D.8) for "three-state" converters, some other restrictions are imposed to reflect this limited behavior of inductor current with fixed (zero) boundary values. What these additional requirements are is shown in Part II, where they naturally lead to the reduction of system order (discontinuous inductor current becoming a removed state-variable) and transform the basic averaged model (D.8) into a linear circuit model of such converters.

In Chapter 1 it has already been demonstrated that the inequality requirements (1.11)(natural frequencies << switching frequency) are well satisfied even for the discontinuous conduction operation. Hence, because of the results in Appendix A, the linear approximations (D.6) are excellent and the basic averaged model (D.8) is a very accurate starting model for modelling converters in the discontinuous conduction mode.

We have therefore established that the state-space averaging step (D.8) is generally applicable to "three-state" switching converters: directly to the converters operating in continuous conduction mode (along procedures outlined in Part I), and with some additional restrictions to converters operating in discontinuous conduction mode (as specified in detail in Part II).

It remains, finally, to characterize the state-space averaging step for the generalized switching converter with n structural changes within each switching period, namely, one described by

$$\dot{x} = A_i x + b_i v_g, \qquad \begin{matrix} d_i T_s = t_i - t_{i-1} \\ t \in [t_{i-1}, t_i] \end{matrix} \qquad i = 1,2,\ldots,n \tag{D.9}$$

for which the corresponding basic state-space averaged model is

$$\dot{x} = Ax + bv_g \; ; \qquad \begin{matrix} A = \sum_{i=1}^{n} d_i A_i \\ b = \sum_{i=1}^{n} d_i b_i \end{matrix} \tag{D.10}$$

The average of possible output equations can be taken as well in analogy with (B.15).

COMPUTER PROGRAMS

Short description of computer programs

PROGRAM RIPPLE — is used to calculate and plot exact instantaneous waveforms (inductor current and capacitor voltage) for the boost converter example of Fig. 3.1 operating in the continuous conduction mode.

PROGRAM PBOOST — is used to calculate and plot the frequency dependence of the exact dc conditions for the boost converter example of Fig. 3.1 operating in the continuous conduction mode.

PROGRAM DCGAIN — is used to calculate and plot dc gain dependence on duty ratio D for the boost-buck converter in Fig. 11.6 and converters in Fig. 13.1 operating in the continuous conduction mode.

PROGRAM NEW — is used to calculate and plot frequency response of the new converter of Fig 12.3 operating in the continuous conduction mode.

PROGRAM RIPPLE

```
TYPE RIPPLE.F4
      COMMON /HPPLOT/HPPLOT
      DIMENSION VOLRIP(510),CURRIP(510),VTIME(510)
      DIMENSION DOC(3),XTIME(2)
      DIMENSION XP(2),X(2),L(2),M(2),D2(4),XTEMP(2),XDT(2)
      DIMENSION A1INV(4),A2INV(4),U(4)
      DIMENSION A1(4),A2(4),F1(4),F2(4),TEMP(4),D1(4)
      HPPLOT=-1
      WRITE(5,99)
   99 FORMAT(1X,'INPUT N')
      READ(5,100) N
  100 FORMAT(I1)
      WRITE(5,199)
  199 FORMAT(1X,'INPUT VG,D,RL,RC,R,L,C')
      READ(5,210) VG,D,RL,RC,R,Q,C
  210 FORMAT(7F)
      WRITE(5,400) VG,D,RL,RC,R,Q,C
  400 FORMAT(1X,'PARAMETAR VALUES ARE ',/,1X,'VG=',F6.2,4X,'D=',F4.2,
     1 4X,'RL=',F6.2,4X,'RC=',F6.2,4X,'R=',F6.2,4X,'L=',E10.4,
     2 4X,'C=',E10.4,4X,///)
      NN=N*N
      XP(1)=VG/Q
      XP(2)=0.0
      A1(2)=0.0
      A1(1)=-RL/Q
      A1(3)=0.0
      A1(4)=-1./((R+RC)*C)
      A2(1)=-(RL+RC*R/(R+RC))/Q
      A2(2)=R/((R+RC)*C)
      A2(3)=-R/((R+RC)*Q)
      A2(4)=-1./((R+RC)*C)
      DO 16 I=1,NN
   16 U(I)=0.0
      DO 17 I=1,N
      II=(N+1)*(I-1)+1
   17 U(II)=1.0
      DO 56 I=1,NN
   56 A1INV(I)=A1(I)
      DO 57 I=1,NN
   57 A2INV(I)=A2(I)
      CALL MINV(A1INV,N,DET1,L,M)
      IF(DET1) 59,58,59
   58 WRITE(5, 01)
  401 FORMAT(1X,'DET1 IS ZERO')
      GO TO 3
   59 CALL MINV(A2INV,N,DET2,L,M)
      IF(DET2) 91,92,91
   92 WRITE(5,402)
  402 FORMAT(1X,'DET2 IS ZERO')
      GO TO 3
   91 WRITE(5,304)
  304 FORMAT(1X,'READ NPOINT NUMBER OF POINTS PER PLOT')
      READ(5,350) NPOINT
  350 FORMAT(I)
    1 WRITE(5,600)
  600 FORMAT(1X,'WHAT IS THE SWITCHING FREQUENCY?')
      READ(5,601) FS
  601 FORMAT(F)
      IF(FS) 2,3,2
    2 T=1./FS
      DT=D*T
      CALL ONN(F1,N,DT,R,RC,RL,Q,C)
      DNT=(1-D)*T
```

```
      CALL OFF(F2,N,DNT,R,RC,RL,Q,C)
      DO 71 I=1,NN
 71   TEMP(I)=F1(I)-U(I)
      CALL GMPRD(A1INV,TEMP,B1,N,N,N)
      DO 72 I=1,NN
 72   TEMP(I)=F2(I)-U(I)
      CALL GMPRD(A2INV,TEMP,B2,N,N,N)
      CALL GMPRD(F2,B1,TEMP,N,N,N)
      DO 73 I=1,NN
 73   TEMP(I)=TEMP(I)+B2(I)
      CALL GMPRD(TEMP,XP,X,N,N,1)
      CALL GMPRD(F2,F1,TEMP,N,N,N)
      DO 74 I=1,NN
 74   TEMP(I)=U(I)-TEMP(I)
      CALL SIMQ(TEMP,X,N,KS)
      IF(KS-1) 76,77,76
 77   WRITE(5,106)
106   FORMAT(1X,'SINGULAR SET OF EQUATIONS')
      GO TO 3
 76   CALL GMPRD(F1,X,XDT,N,N,1)
      CALL GMPRD(B1,XP,XTEMP,N,N,1)
      DO 78 I=1,N
 78   XDT(I)=XDT(I)+XTEMP(I)
      DELTA=T/NPOINT
      DO 50 K=1,NPOINT+1
      TIME=DELTA*(K-1)
      IF(TIME-DT) 41,42,42
 41   CALL ONN(F1,N,TIME,R,RC,RL,Q,C)
      DO 79 I=1,NN
 79   TEMP(I)=F1(I)-U(I)
      CALL GMPRD(A1INV,TEMP,B1,N,N,N)
      CALL GMPRD(F1,X,XTIME,N,N,1)
      CALL GMPRD(B1,XP,XTEMP,N,N,1)
      DO 31 I=1,N
 31   XTIME(I)=XTIME(I)+XTEMP(I)
      VOLRIP(K)=XTIME(2)
      CURRIP(K)=XTIME(1)
      VTIME(K)=TIME
      GO TO 50
 42   TIMEN=TIME-DT
      CALL OFF(F2,N,TIMEN,R,RC,RL,Q,C)
      DO 81 I=1,NN
 81   TEMP(I)=F2(I)-U(I)
      CALL GMPRD(A2INV,TEMP,B2,N,N,N)
      CALL GMPRD(F2,XDT,XTIME,N,N,1)
      CALL GMPRD(B2,XP,XTEMP,N,N,1)
      DO 32 I=1,N
 32   XTIME(I)=XTIME(I)+XTEMP(I)
      VOLRIP(K)=XTIME(2)
      CURRIP(K)=XTIME(1)
      VTIME(K)=TIME
 50   CONTINUE
      WRITE(5,500)
500   FORMAT(1X,'READ PLOTTING SCALES VOLMIN,VOLMAX,CURMIN,CURMAX')
      READ(5,200) VOLMIN,VOLMAX,CURMIN,CURMAX
200   FORMAT(4F)
      LAB=-1
      DOC(1)='BOOST'
      DOC(2)=' CASE'
      DOC(3)=1.0
      CALL XYPLOT(NPOINT+1,VTIME,VOLRIP,0.,T,VOLMIN,VOLMAX,DOC,LAB)
      DOC(1)=0.0
      CALL XYPLOT(NPOINT+1,VTIME,CURRIP,0.,T,CURMIN,CURMAX,DOC,LAB)
      GO TO 1
   3  CALL EXIT
      END
```

PROGRAM PBOOST

```
TYPE PBOOST.F4
      COMMON /HPPLOT/HPPLOT
      DIMENSION FREQ(500),DCCUR(500),DCVOL(500),CURIN(500),VOLIN(500)
      DIMENSION DOC(3)
      DIMENSION XP(2),XD(2),XF(2),X(2),XDC(2),L(2),M(2),D2(4)
      DIMENSION A1INV(4),A2INV(4),U(4)
      DIMENSION A1(4),A2(4),F1(4),F2(4),TEMP(4),SAVE(4),D1(4)
      HPPLOT=-1
      WRITE(5,99)
   99 FORMAT(1X,'INPUT N')
      READ(5,100) N
  100 FORMAT(I )
      WRITE(5,199)
  199 FORMAT(1X,'INPUT VG,D,RL,RC')
      READ(5,200) VG,D,RL,RC
  200 FORMAT(4F)
    1 WRITE(5,299)
  299 FORMAT(1X,'INPUT R,L,C,FMIN,FMAX')
      READ(5,300) R,Q,C,FMIN,FMAX
  300 FORMAT(5F)
      WRITE(5,304)
  304 FORMAT(1X,'READ NPOINT NUMBER OF POINTS PER PLOT')
      READ(5,350) NPOINT
  350 FORMAT(I)
      IF(R) 2,3,2
    2 WRITE(5,400) VG,D,RL,RC,R,Q,C
  400 FORMAT(1X,'PARAMETAR VALUES ARE ',/,1X,'VG=',F6.2,4X,'D=',F4.2,
     1 4X,'RL=',F6.2,4X,'RC=',F6.2,4X,'R=',F6.2,4X,'L=',E10.4,
     2 4X,'C=',E10.4,4X,///)
      NN=N*N
      XP(1)=VG/Q
      XP(2)=0.0
      A1(2)=0.0
      A1(1)=-RL/Q
      A1(3)=0.0
      A1(4)=-1./((R+RC)*C)
      A2(1)=-(RL+RC*R/(R+RC))/Q
      A2(2)=R/((R+RC)*C)
      A2(3)=-R/((R+RC)*Q)
      A2(4)=-1./((R+RC)*C)
      DO 16 I=1,NN
   16 U(I)=0.0
      DO 17 I=1,N
      II=(N+1)*(I-1)+1
   17 U(II)=1.0
      DO 56 I=1,NN
   56 A1INV(I)=A1(I)
      DO 57 I=1,NN
   57 A2INV(I)=A2(I)
      CALL MINV(A1INV,N,DET1,L,M)
      IF(DET1) 59,58,59
   58 WRITE(5,401)
  401 FORMAT(1X,'DET1 IS ZERO')
      GO TO 3
   59 CALL MINV(A2INV,N,DET2,L,M)
      IF(DET2) 91,92,91
   92 WRITE(5,402)
  402 FORMAT(1X,'DET2 IS ZERO')
      GO TO 3
   91 DO 61 I=1,NN
   61 TEMP(I)=-D*A1INV(I)-(1-D)*A2INV(I)
      CALL GMPRD(TEMP,XP,XD,N,N,1)
      WRITE(5,301) XD(1),XD(2)
  301 FORMAT(1X,'BEGINNING CONDITIONS ARE',/,1X,'DC INDUCTOR CURRENT
```

```
      DO 62 I=1,NN
   62 TEMP(I)=-D*A1(I)-(1-D)*A2(I)
      CALL MINV(TEMP,N,DET3,L,M)
      IF(DET3) 93,94,93
   94 WRITE(5,403)
  403 FORMAT(1X,'DET3 IS ZERO')
      GO TO 3
   93 CALL GMPRD(TEMP,XP,XF,N,N,1)
      WRITE(5,302) XF(1),XF(2)
  302 FORMAT(1X,'FINAL CONDITIONS ARE',//,'DC INDUCTOR CURRENT IS',
     1 F8.4,6X,'DC OUTPUT VOLTAGE IS',F8.4,///)
      XMIN=ALOG10(FMIN)
      XMAX=ALOG10(FMAX)
      XDELT=(XMAX-XMIN)/NPOINT
      DO 50 K=1,NPOINT+1
      XORD=XMIN+(K-1)*XDELT
      FREQ(K)=XORD
      FS=(10.0)**XORD
      T=1.0/FS
      DT=D*T
      CALL ONN(F1,N,DT,R,RC,RL,Q,C)
      DNT=(1-D)*T
      CALL OFF(F2,N,DNT,R,RC,RL,Q,C)
      DO 71 I=1,NN
   71 TEMP(I)=F1(I)-U(I)
      CALL GMPRD(A1INV,TEMP,B1,N,N,N)
      DO 72 I=1,NN
   72 TEMP(I)=F2(I)-U(I)
      CALL GMPRD(A2INV,TEMP,D2,N,N,N)
      CALL GMPRD(F2,B1,TEMP,N,N,N)
      DO 73 I=1,NN
   73 TEMP(I)=TEMP(I)+D2(I)
      CALL GMPRD(TEMP,XP,X,N,N,1)
      CALL GMPRD(F2,F1,TEMP,N,N,N)
      DO 74 I=1,NN
   74 TEMP(I)=U(I)-TEMP(I)
      CALL SIMQ(TEMP,X,N,KS)
      IF(KS-1) 76,77,76
   77 WRITE(5,106)
  106 FORMAT(1X,'SINGULAR SET OF EQUATIONS')
      GO TO 3
   76 CALL GMPRD(B2,F1,TEMP,N,N,N)
      DO 78 I=1,NN
   78 TEMP(I)=TEMP(I)+D1(I)
      CALL GMPRD(TEMP,X,XF,N,N,1)
      CALL GMPRD(A1INV,B1,TEMP,N,N,N)
      CALL GMPRD(A2INV,B2,SAVE,N,N,N)
      DO 79 I=1,NN
   79 SAVE(I)=SAVE(I)+TEMP(I)
      CALL GMPRD(B2,B1,TEMP,N,N,N)
      DO 81 I=1,NN
   81 SAVE(I)=SAVE(I)+TEMP(I)
      CALL GMPRD(SAVE,XP,XDC,N,N,1)
      DO 82 I=1,N
   82 XDC(I)=(XDC(I)+XF(I))/T+XD(I)
      DCCUR(K)=XDC(1)
      DCVOL(K)=XDC(2)
      CURIN(K)=X(1)
      VOLIN(K)=X(2)
   50 CONTINUE
      WRITE(5,500)
  500 FORMAT(1X,'READ PLOTTING SCALES VOLMIN,VOLMAX,CURMIN,CURMAX',/)
      READ(5,200) VOLMIN,VOLMAX,CURMIN,CURMAX
      LAB=-1
```

```
      DOC(3)=1.0
      CALL XYPLOT(NPOINT+1,FREQ,DCVOL,XMIN,XMAX,VOLMIN,VOLMAX,DOC,LAB)
      DOC(1)=0.0
      CALL XYPLOT(NPOINT+1,FREQ,VOLIN,XMIN,XMAX,VOLMIN,VOLMAX,DOC,LAB)
      CALL XYPLOT(NPOINT+1,FREQ,DCCUR,XMIN,XMAX,CURMIN,CURMAX,DOC,LAB)
      CALL XYPLOT(NPOINT+1,FREQ,CURIN,XMIN,XMAX,CURMIN,CURMAX,DOR,LAB)
      GO TO 1
    3 CALL EXIT
      END
```

```
TYPE ONN.FA
      SUBROUTINE ONN(F,N,T,R,RC,RL,Q,C)
      DIMENSION F(1)
      F(1)=EXP(-RL*T/Q)
      F(2)=0.0
      F(3)=0.0
      F(4)=EXP(-T/((R+RC)*C))
      RETURN
      END
```



```
TYPE OFF.FA
      SUBROUTINE OFF(F,N,T,R,RC,RL,Q,C)
      DIMENSION F(1)
      TC=1.0/((R+RC)*C)
      TL=(RL+RC*R/(R+RC))/Q
      A=0.5*(TC+TL)
      W=SQRT((R+RL)/((R+RC)*Q*C)-A*A)
      B=0.5*(TC-TL)/W
      AL=EXP(-A*T)*COS(W*T)
      BE=EXP(-A*T)*SIN(W*T)
      F(1)=AL+BE*B
      F(2)=R*BE/((R+RC)*W*C)
      F(3)=-R*BE/((R+RC)*W*Q)
      F(4)=AL-BE*B
      RETURN
      END
```

PROGRAM DCGAIN

```
TYPE DCGAIN.F4
      COMMON /HPPLOT/ HPPLOT
      DIMENSION DUTY(500),GAIN(500),OGAIN(500),CGAIN(500)
      DIMENSION DEFIC(500),EFIC(500),DOC(3)
      HPPLOT=-1
      WRITE(5,100)
100   FORMAT(1X,'INPUT RESISTANCES RL1,RL2,R AND NPOINT')
      READ(5,200) RL1,RL2,R,NPOINT
200   FORMAT(3F,I)
      XDELT=1.0/NPOINT
      DO 50 K=1,NPOINT
      XORD=(K-1)*XDELT
      DUTY(K)=XORD
      D=XORD/(1.0-XORD)
      DNOT=1./(1.-XORD)
      FACT1=R/(R+RL2+D*D*RL1)
      FACT2=R/(R+DNOT*DNOT*RL2+D*D*RL1)
      GAIN(K)=D*FACT1
      OGAIN(K)=D*FACT2
      EFIC(K)=FACT1*100.
      DEFIC(K)=FACT2*100.
      CGAIN(K)=D
50    CONTINUE
      DOC(3)=1.0
      DOC(1)=0.0
      LAB=1
      CALL XYPLOT(NPOINT,DUTY,GAIN,0.0,1.0,0.0,7.0,DOC,LAB)
      CALL XYPLOT(NPOINT,DUTY,OGAIN,0.0,1.0,0.0,7.0,DOC,LAB)
      CALL XYPLOT(NPOINT,DUTY,CGAIN,0.0,1.0,0.0,7.0,DOC,LAB)
      CALL XYPLOT(NPOINT,DUTY,EFIC,0.0,1.0,30.,100.,DOC,LAB)
      CALL XYPLOT(NPOINT,DUTY,DEFIC,0.0,1.0,30.,100.,DOC,LAB)
      CALL EXIT
      END
```

PROGRAM NEW

```
TYPE NEW.FA
      COMMON /HPPLOT/ HPPLOT
      COMPLEX S,P,Q,G,H
      DIMENSION FREQ(500),GDUTY(500),FDUTY(500),GLINE(500),PLINE(500)
      DIMENSION DOC(3)
      HPPLOT=-1
      PI=3.14159
    1 WRITE(5,99)
   99 FORMAT(1X,'INPUT PARAMETARS  L1,L2,C1,C2,R,D',/)
      READ(5,100)Q1,Q2,C1,C2,R,D
  100 FORMAT(6F)
      WRITE(5,199)
  199 FORMAT(1X,'INPUT PARASITICS RL1,RL2 AND FS',/)
      READ(5,200) RL1,RL2,FS
  200 FORMAT(3F)
      WRITE(5,299)
  299 FORMAT(1X,'INPUT FMIN,FMAX,NPOINT',/)
      READ(5,300) FMIN,FMAX,NPOINT
  300 FORMAT(2F,I)
      WRITE(5,400) Q1,Q2,C1,C2,R,RL1,RL2,D,FS
  400 FORMAT(1X,'PARAMETAR VALUES ARE',/,1X,'L1=',E10.4,
     1 4X,'L2=',E10.4,4X,'C1=',E10.4,4X,'C2=',E10.4,4X,/,1X,'R=',
     2 F6.2,4X,'RL1=',F6.2,4X,'RL2=',F6.2,4X,'D=',F6.2,4X,'FS=',
     3 F6.2,//)
      DE=(D/(1.-D))**2
      RE=DE*RL1
      QE=DE*Q1
      CE=C1/(D*D)
      A0=1.+(RE+RL2)/R
      A1=CE*RE*(1.+RL2/R)+C2*(RE+RL2)+(Q2+QE)/R
      A2=QE*C2+Q2*C2+QE*CE*(1.+RL2/R)+Q2*CE*RE/R+CE*RE*C2*RL2
      A3=CE*QE*Q2/R+(QE*RL2+Q2*RE)*CE*C2
      A4=QE*CE*Q2*C2
      B0=1.+(RL2-RE)/R
      B1=RE*CE*(1.-D)*(1.+RL2/R)-QE/R
      B2=QE*CE*(1.-D)*(1.+RL2/R)
      IF(B1) 9,9,10
   10 WRITE(5,600)
  600 FORMAT(1X,'LEFT HALF PLANE COMPLEX ZEROS')
      GO TO 11
    9 WRITE(5,700)
  700 FORMAT(1X,'RIGHT HALF PLANE ZEROS')
   11 WRITE(5,800) B1
  800 FORMAT(1X,'B1=',E10.4,/)
      XMIN=ALOG10(FMIN)
      XMAX=ALOG10(FMAX)
      XDELT=(XMAX-XMIN)/NPOINT
      DO 30 K=1,NPOINT+1
      XORD=XMIN+(K-1)*XDELT
      FREQ(K)=XORD
      F=(10.0)**XORD
      W=6.28318*F
      S=CMPLX(0.0,W)
      P=B0+B1*S+B2*S*S
      Q=A0+A1*S+A2*S*S+A3*S*S*S+A4*S*S*S*S
      G=P/Q
      H=1./Q
      GAIN=CABS(G)
      GDUTY(K)=20.0*ALOG10(GAIN)
      GAIN=CABS(H)
      GLINE(K)=20.0*ALOG10(GAIN)
      AR=REAL(G)
      AI=AIMAG(G)
```

```
      ARG=AI/AR
      PRAD=ATAN(ARG)
      IF(ARG) 26,27,27
   27 IF(AR) 18,19,19
   19 PRAD=PRAD-2*PI
      GO TO 21
   18 PRAD=PRAD-PI
      GO TO 21
   26 IF(AR) 22,21,21
   22 PRAD=PRAD-PI
   21 PDUTY(K)=180.*PRAD/PI
      AR=REAL(H)
      AI=AIMAG(H)
      ARG=AI/AR
      PRAD=ATAN(ARG)
      IF(ARG) 36,37,37
   37 IF(AR) 38,39,39
   39 PRAD=PRAD-2*PI
      GO TO 41
   38 PRAD=PRAD-PI
      GO TO 41
   36 IF(AR) 32,41,41
   32 PRAD=PRAD-PI
   41 PLINE(K)=180.*PRAD/PI
   50 CONTINUE
      WRITE(5,500)
  500 FORMAT(1X,'INPUT SCALES FOR DUTY TR FUNC  GMIN,GMAX,PMIN,PMAX')
      READ(5,201) GMIN,GMAX,PMIN,PMAX
  201 FORMAT(4F)
      LAB=1
      IF(B1) 12,13,13
   13 DOC(1)='LHP  '
      DOC(2)='ZEROS'
      GO TO 14
   12 DOC(1)='RHP  '
      DOC(2)='ZEROS'
   14 DOC(3)=1.0
      CALL XYPLOT(NPOINT+1,FREQ,GDUTY,XMIN,XMAX,GMIN,GMAX,DOC,LAB)
      DOC(1)=0.0
      CALL XYPLOT(NPOINT+1,FREQ,PDUTY,XMIN,XMAX,PMIN,PMAX,DOC,LAB)
      WRITE(5,860)
  860 FORMAT(1X,'INPUT SCALES FOR LINE TR FUNC  GMIN, GMAX,PMIN,PMAX')
      READ(5,201) GMIN,GMAX,PMIN,PMAX
      DOC(1)='LINE '
      DOC(2)='TRANS'
      CALL XYPLOT(NPOINT+1,FREQ,GLINE,XMIN,XMAX,GMIN,GMAX,DOC,LAB)
      DOC(1)=0.0
      CALL XYPLOT(NPOINT+1,FREQ,PLINE,XMIN,XMAX,PMIN,PMAX,DOC,LAB)
      READ(5,850) KRAJ
  850 FORMAT(F)
      IF(KRAJ) 17,16,17
   16 GO TO 1
   17 CALL EXIT
      END
```

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