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Preliminary Study of the Reliability of Imaging Charge Coupled Devices

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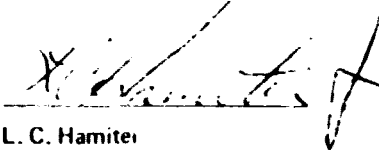
**PRELIMINARY STUDY OF THE
RELIABILITY OF IMAGING
CHARGE COUPLED DEVICES**

Authors:

J. R. Beali, M. D. Borenstein,
R. A. Homan, D. L. Johnson,
D. D. Wilson, V. F. Young

Approved:


V. F. Young
Program Manager


L. C. Hamiter
NASA/MSFC Technical Monitor

Prepared for:

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama

MARTIN MARIETTA CORPORATION
DENVER DIVISION
Denver, Colorado 80201

FOREWORD

The objective of this preliminary study of Imaging Charge Coupled Devices (ICCDs) was to evaluate the reliability of one particular device, the Fairchild CCD121H, for use in imaging applications. The device was selected because of considerable experience gained in usage on a separate program and because it is representative of CCD processing using N-channel silicon gate MOS technology.

The short term objectives for the period of performance of November 1977 through June 1978 was to identify failure modes and to measure the performance as related to packaging, chip construction, and electro-optical parameters. The longer range objective was to define a test program to evaluate ICCDs in general.

The work was performed under contract NAS8-32641 for the National Aeronautics and Space Administration, Marshall Space Flight Center. The NASA Technical Monitor was Mr. Leon Hamiter. All work was performed at the Denver Division of the Martin Marietta Corporation by the Microelectronics and Failure Analysis Laboratories.

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ABSTRACT

Imaging CCDs are capable of low light level response and high signal-to-noise ratios. In space applications they offer the user the ability to achieve extremely high resolution imaging with minimum circuitry in the photo sensor array. This work relates the CCD121H Fairchild device to the fundamentals of CCDs and the representative technologies. Several failure modes are described, construction is analyzed and test results are reported. In addition, the relationship of the device reliability to packaging principles is analyzed and test data presented. Finally, a test program is defined for more general reliability evaluation of CCDs.

I. INTRODUCTION

The Charge Coupled Device (CCD) is an important advancement in the semiconductor field. Its relatively short period of existence (from 1970 to present) is characterized by rapid development in improvement of fundamental MOS technology in materials and innovative process techniques. The references contain extensive descriptions of the different methods and principles used in manufacturing and applying CCDs but, as is often the case with rapidly growing technologies, there is little information on the subject of reliability.

The work reported herein combines an introduction to CCDs with an evaluation of the construction and performance of the Fairchild CCD121H Linear Imaging Array.

The CCD121H was selected because of the experience gained with it on a separate high reliability program. The data, as a whole, must not be looked upon as representative of all CCDs. Certain fundamental properties of the CCD121H are common to CCDs in general. These will be presented as such. The report will show that the CCD121H is capable of high reliability applications. When screen tested for initially defective parts and applied properly, the device operates with excellent electro-optical performance and reliability.

II. PROGRAM DEFINITION

This program was performed with the primary objective of obtaining reliability data on one type of CCD. This data, in part, was expected to relate to CCDs in general. It is considered a preliminary study on CCD reliability because of limited scope. A second objective is to define a reliability test and evaluation program for CCDs that would encompass the most important processes and CCD classes. This is difficult to perform without large expenditures since each device requires unique driving and signal processing circuitry and each device requires a considerable amount of construction analysis. The task that is defined in Section VI of this report recommends work on devices which, along with the work performed on the CCD121H, provides a study of some of the most important aspects of CCD reliability.

A. TASK DESCRIPTIONS.

1. Provide an introduction to CCDs from a user's point of view. This task was intended to describe the CCD121H where possible while relating to device fundamentals.
2. Research available literature on CCD reliability.
3. Report on electrical and optical performance tests of the CCD121H.
4. Analyze the packaging constraints especially with respect to large silicon chips.
5. Perform an in-depth construction analysis to determine location of diffusions, polysilicon layers, metal layers, interconnect reliability and other device characteristics that relate to reliability.
6. Identify potential failure modes of the CCD121H.
7. Provide conclusions about the device reliability and, where applicable, describe methods that would help screen for high reliability applications.
8. Recommend a test program to more quantitatively evaluate the reliability of CCDs.

B. TEST METHODS

1. Construction Analysis.

This work was performed in the Failure Analysis Laboratory on sample chips using the Scanning Electron Microscope along with etch back techniques and precision sectioning. By successively removing layers down to the diffusions at the CCD surface, an accurate diagram of the circuit was generated. Observations of the degree of gate overlaps, oxide thicknesses, depth of diffusions and types of diffusions are all required in order to understand the operation of a CCD. Many of these physical properties have a direct relationship on electro-optical and electrical properties.

2. Electrical Tests.

Six commercially packaged devices were tested and included with test data obtained on about 200 similar devices. The following test methods were used in obtaining the data.

- a) Responsivity. This parameter was measured by illuminating the CCD with a calibrated light source with a color temperature of 5000°K. The photosites accumulate electrons in the potential wells for a time period called the integration time. For these tests, the integration time was 80 milliseconds. The signal is transferred to the shift register every 80 milliseconds and read out in units of volts per unit of light energy density or volts/joule/meter².

$$R = \text{Volts per joule/meter}^2$$

where R = the responsivity,

joules = light intensity times integration time,

area = the size of the photosite, which is 13 x 17 microns.

The test was performed at 25°C and -10°C. The dark signal background is first stored and then subtracted from the illuminated readings.

The sensitivity of the CCD is directly proportional to the integration time. An 80 millisecond integration time results in a very high sensitivity but allows proportionally more dark signal to accumulate.

- b) Response Uniformity. The uniformity of the response of one pixel (picture element) compared to the next was measured by recording the line readout of the CCD on an oscilloscope for both dark and illuminated conditions. The double-exposed photograph was analyzed for variations in pixel response. Individual pixels with nonuniformity that exceeds +10% of the average response of the line were identified.
- c) Linearity. The response of three selected pixels was measured at various illumination levels. This is accomplished by placing fixed and variable neutral density filters in the light path. The voltage response versus incident illumination is plotted in the log-log domain, and a

least-squares best fit straight line is calculated from the data. The slope of the line is called gamma and is a measure of linearity. An ideal slope is equal to 1.0. The deviation from the best fit line of all of the measured values was also calculated.

- d) **Dynamic Range.** The dynamic range was determined by increasing the illumination until the output response begins deviating from the best fit line determined in the linearity test. The point at which the output response begins to saturate is a measure of the dynamic range.
- e) **Transfer Efficiency.** The ability of the charge to be completely transferred from one register element to the next will be measured. This is done by electrically injecting a packet of charge at one of the register and observing it as it comes out the other end. The ratio of the output at the n th transfer to the $n + 1$ th transfer on an N -element array can be mathematically converted into transfer efficiency as a fraction. A typical value for the CCD121H is 0.99999.
- f) **Noise.** The equivalent irradiance of the noise was determined by first measuring the uncertainty of 125 consecutive readouts of each test pixel. A pixel near each end of the line and one near the middle was selected. The rms value of the noise was and then converted into equivalent irradiance by using the measured under dark and illuminated conditions.
- g) **Dark Signal.** The value of the electrical output of the CCD with no illumination was documented by photographing the CCD readout on the oscilloscope. The voltage output was then converted into equivalent dark irradiance using values of measured responsivity. The nonuniformity of the dark signal was displayed on the photograph and the maximum dark signal recorded. "Bad" pixels which exceed the continuous dark readout are individual documented.
- h) **Spectral Response.** The spectral response of the photo elements was measured by placing calibrated optical bandpass filters in front of the spectrally calibrated light source. The resulting response was plotted over a spectrum on 0.4 to 1.1 microns.
- i) **Crosstalk.** The response of a pixel due to light falling on areas other than that pixel was evaluated. A spot of light was focused on the channel stop between two pixels. The response of the adjacent two pixels was compared with the summed response of the two illuminated pixels and the two adjacent pixels. Also, the response of the fifth removed pixels in both directions was compared to the response of the center four pixels. The effect of a spot focused over the aluminum shield which covers the shift register, input parts, and output amplifier was checked. Response due to this stray illumination was documented.
- j) **Test Equipment Description.** The electronic test tool provides

the proper bias voltages and clock signals to the unit under test. In addition, timing circuitry was provided for selecting the output of any individual element of the CCD. Two basic control tools are used for complete characterization of a CCD.

- 1) Variable Frequency and Temperature Test Set-Up. The block diagram of Figure II-1 shows the test configuration used when performing variable frequency tests and temperature tests. The controller is capable of providing the proper waveforms to the CCD at frequencies from 100 KHz to about 1 MHz. The adaptor contains high speed drivers capable of driving the high capacitance clock lines.
- 2) Optical Test-Up. The block diagram of Figure II-2 shows the test set-up for performing room ambient and optical tests. The electronic controller provides bias and clock signals to the unit under test and operates at a frequency of 129.6 KHz with an integration time of 80 milliseconds. Bias and clock signals are provided to inject background charge to reduce the effects of trapping loss. Controls are provided to perform transfer efficiency and trapping loss tests. The controller also contains a double-correlated sample and hold circuit, which samples the video output of the CCD and allows accurate measurement of individual pixel outputs. The pixel output voltage is used to perform responsivity, linearity, dynamic range and noise equivalent signal measurements. A radiometer diode is mounted in the adaptor for accurate measurement of light intensities.

The optical bench provides a collimated beam of light to the unit under test. The color temperature of the source has been adjusted to simulate a 5000°K black body. A neutral density wedge and several selectable neutral density filters are used to control the light intensity in the range from less than 10 to greater than 3000 $\mu\text{j}/\text{m}^2$. In addition, various color filters can be inserted to change the spectral content of the light.

- 3) Data Acquisition and Reduction. An HP9830 programmable calculator was used to automatically collect and reduce test data. Responsivity, linearity, and noise equivalent signal were calculated as the data was taken. The linearity is further determined by manually plotting the calculated points on log-log paper.

3. Mechanical Test Description.

A test was designed and implemented to measure dark signal performance versus strain in the silicon. It is intended that this test simulate some of the effects found when large chips are bonded to dissimilar materials. The test is described in detail along with

the test results in Section IV. Briefly, the test consisted of a CCD bonded to a zirconium pull test specimen using gold filled epoxy cured at 125°C (to limit the initial chip strain). Zirconium was selected because of the close temperature coefficient of expansion match to silicon also for minimization of initial built-in stresses. The assembly was then pull tested while measuring dark signal as a function of chip strain. As a calibration test, a thin film strain gage was first mounted to a similar sample on the CCD surface to verify the degree of strain transmitted to the CCD up to the point of bond failure.

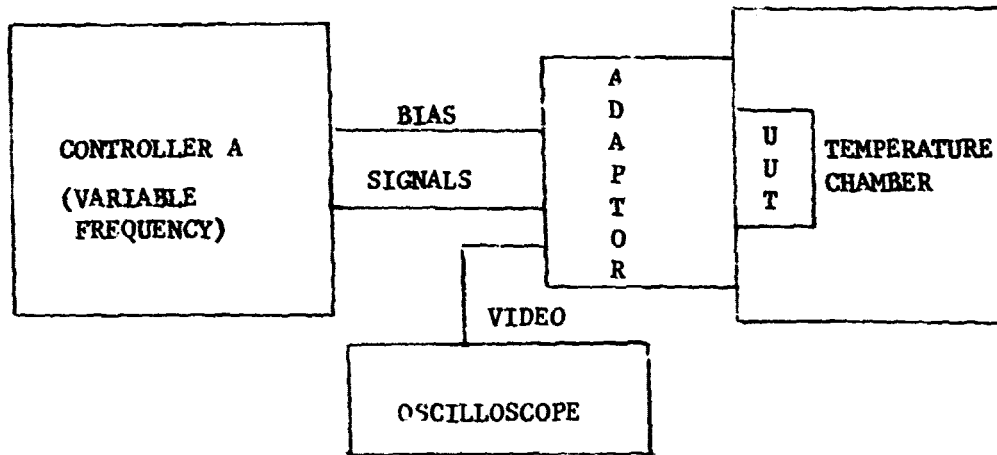


FIGURE II-1 Variable Frequency Test Set-Up

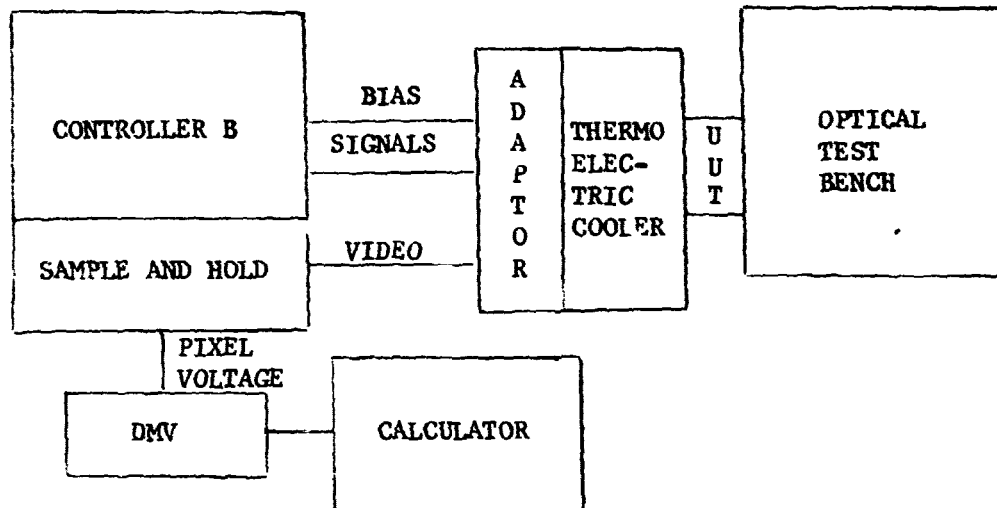


FIGURE II-2 Optical Test Set-Up

III. INTRODUCTION TO CCDS

This section serves a dual purpose: to introduce CCD concepts as well as to describe the CCD121H circuit. Where practical this has been accomplished without attempting a detailed analysis of physical science of CCDs. The references offer an extensive and in-depth study of CCDs.

The study of the reliability of the CCD121H should be introduced with a description of CCD principles and applications in order that the reader may effectively understand the data reported. The following introduction will present fundamental characteristics, processes, and applications.

A. CCD PRINCIPLES

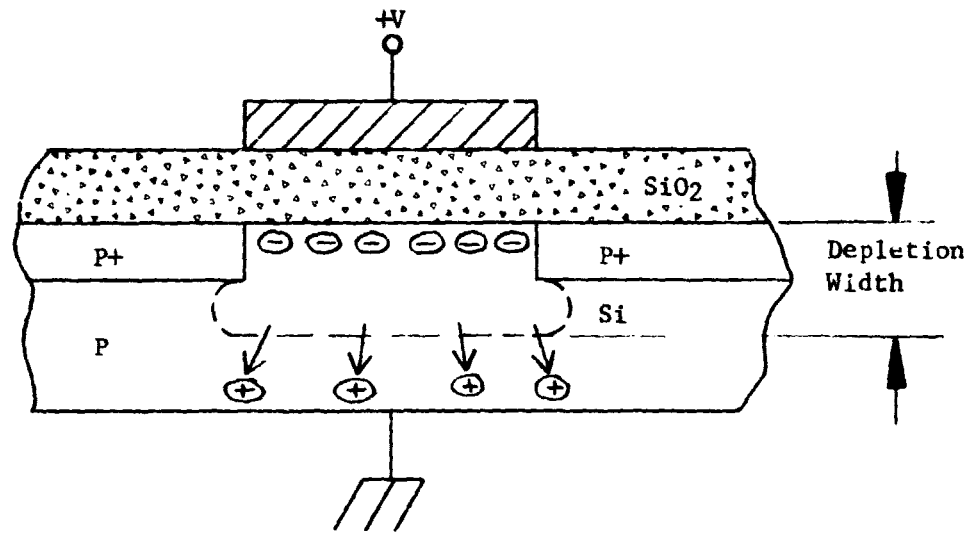
Probably the earliest formulated concept of charge transfer devices was presented by Weimer in 1948 in the discussion of the telegraph repeater which employed serial transmission of charge stored on a condenser. Later, various investigators reported on devices called Bucket Brigade Devices (BBDs) which used electronic switches and amplifiers to move the charge from one capacitor to another. The first CCD concept is attributed to Boyle and Smith in 1969. They proposed that plates, or electrodes, closely spaced on a silicon surface could be used to move a charge along the surface of silicon by pulsing the electrodes in a three-phase manner. The voltage on the electrode creates an inversion layer in the silicon thus forming a capacitor. The inversion layer is discussed as a potential well that is capable of storing charge. By properly shaping the potential wells along the silicon surface the charge can be made to flow, or transfer, from one electrode area to another. The characteristics of the potential well are examined in the next section.

1. The MOS Capacitor.

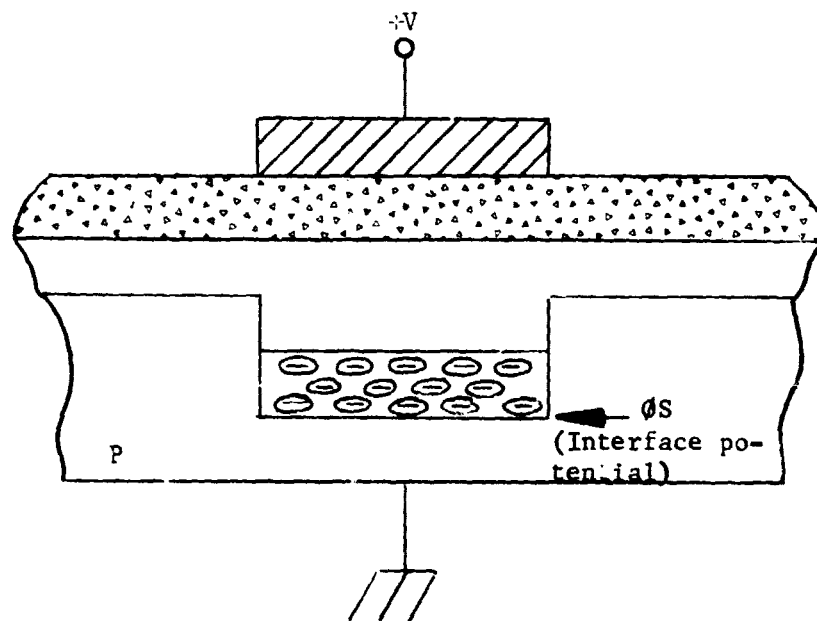
The metal-oxide-semiconductor (MOS) capacitor provides the basic principle for CCDs. Figure III-1a illustrates the sectional view of a p-type MOS capacitor. When positive voltage is applied, the positive charge (majority carriers) near the surface is repelled forming a depleted region that is capable of storing electrons (minority carriers). This region will fill up with thermally generated electrons (later called dark current) or the depletion region may be used to store signal charge temporarily. Figure III-1b shows the commonly used schematic of a potential well. It is convenient, but incorrect, to think of the charge as filling the well from the bottom up. Charge actually resides near the surface at the point of maximum potential.

The two fundamental classes of CCDs are surface CCDs (SCCDs), in

which the charge is transported along the surface at the silicon to silicon dioxide interface, and buried channel CCDs (BCCDs), in which the charge is transported below the interface. Under normal operation, the BCCD is operated with all signal charge contained within the buried channel.



A) Metal - Oxide - Semiconductor Structure



B) Schematic Representation of Potential Well

Figure III-1 The MOS Capacitor

The discussion of the MOS capacitor characteristics is important in later examining the types of CCDs used in imaging applications. Figure III-2 shows the energy band diagram for an MOS capacitor. This diagram depicts the different energy bands for the material. The valence band energy level, E_v , is the energy of the highest valence band electrons in the silicon. The conduction band energy levels, E_c , is the energy of the lowest conduction band electrons in the silicon. The diagram shows an energy gap between E_v and E_c that exists for silicon. This energy, E_g , is 1.1 eV and is often described as a forbidden energy region because no allowed states can exist (i.e., electrons are either in the valence band or if 1.1 eV of energy is added to the electron, it is broken loose from the valence band for conduction). The significance of this energy gap is important in understanding CCD operation. The Fermi level, E_f , in the energy gap shown in Figure III-2 represents the energy level at which the probability of an electron existing is 50%. The intrinsic energy level, E_i , in the energy gap is the energy at which charge neutrality exists in nondoped or intrinsic silicon. This energy lies midway in the energy gap for intrinsic silicon as does the Fermi energy level. The significance of these two energy levels emerges when one examines doped, or extrinsic silicon. For N-doped silicon, the Fermi level lies higher than the intrinsic energy level as shown in Figure III-2. When the bands in N-type silicon are bent by the presence of an applied negative voltage, as in Figure III-2b, the majority carriers (electrons) are repelled, forming a depleted region or a potential well that is capable of storing minority carriers (holes).

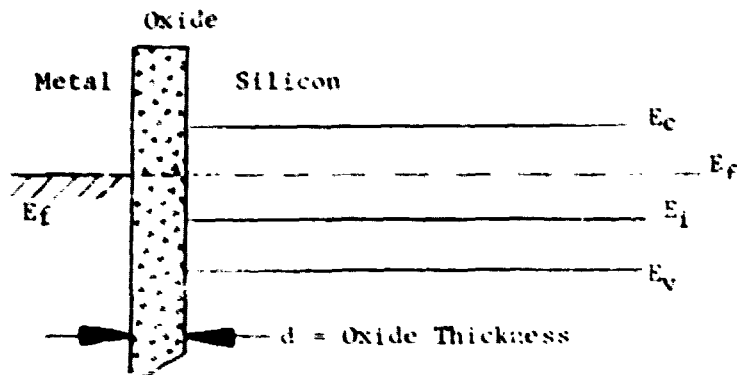
2. Charge Coupled Devices.

The CCD can be looked at as an array of closely spaced MOS capacitors. The principles of the previous section apply directly. In this section we will describe the functional requirements to implement an imaging CCD using the principle of an MOS capacitor. The elements needed are:

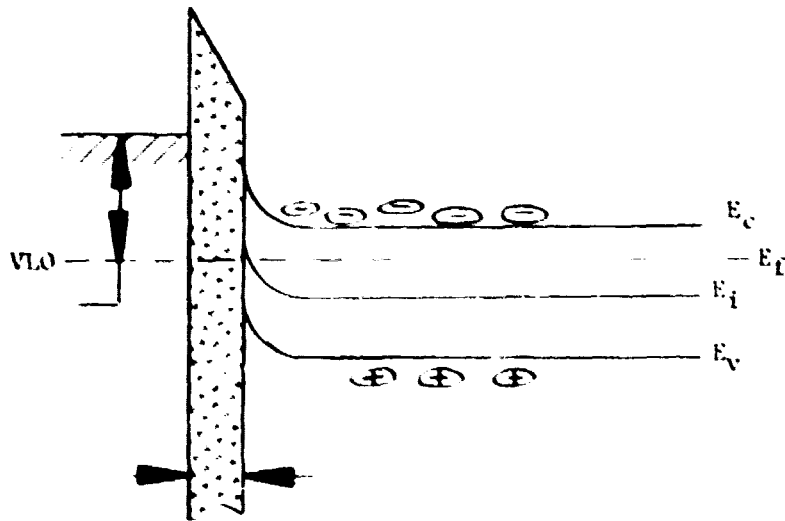
- a) A method for optical signal input (conversion of photons to electron-hole pairs).
- b) A method for electrical signal input.
- c) A method of moving the input signal to the CCD shift register.
- d) A method of transferring the charge along the shift register.
- e) A method of collecting the charge and amplifying it.

Since the above methods are comprehensively presented in several references, we shall present a single approach that relates closely to the CCD121H circuit. This approach will be for a linear array, meaning a single row of N-elements (called pixels, or picture elements) in length commonly described as an $N \times 1$ array. The other geometries are called area arrays of N pixels by M rows.

Figure III-3 shows a functional schematic of a linear array of 8 x 1 pixels. This schematic is applicable to either an SCCD or a BCCD (the CCD121H is a 1728 x 1 BCCD). Fairchild uses a functional diagram



A) Zero Biased N-Type. No band bending due to applied voltage. Charges do not accumulate.



B) Negative Biased N-Type. Majority carriers (electrons) have been repelled forming depletion region at the surface for storing minority carriers (holes).

Figure III-2 Energy Band Diagram of the MDS Capacitor

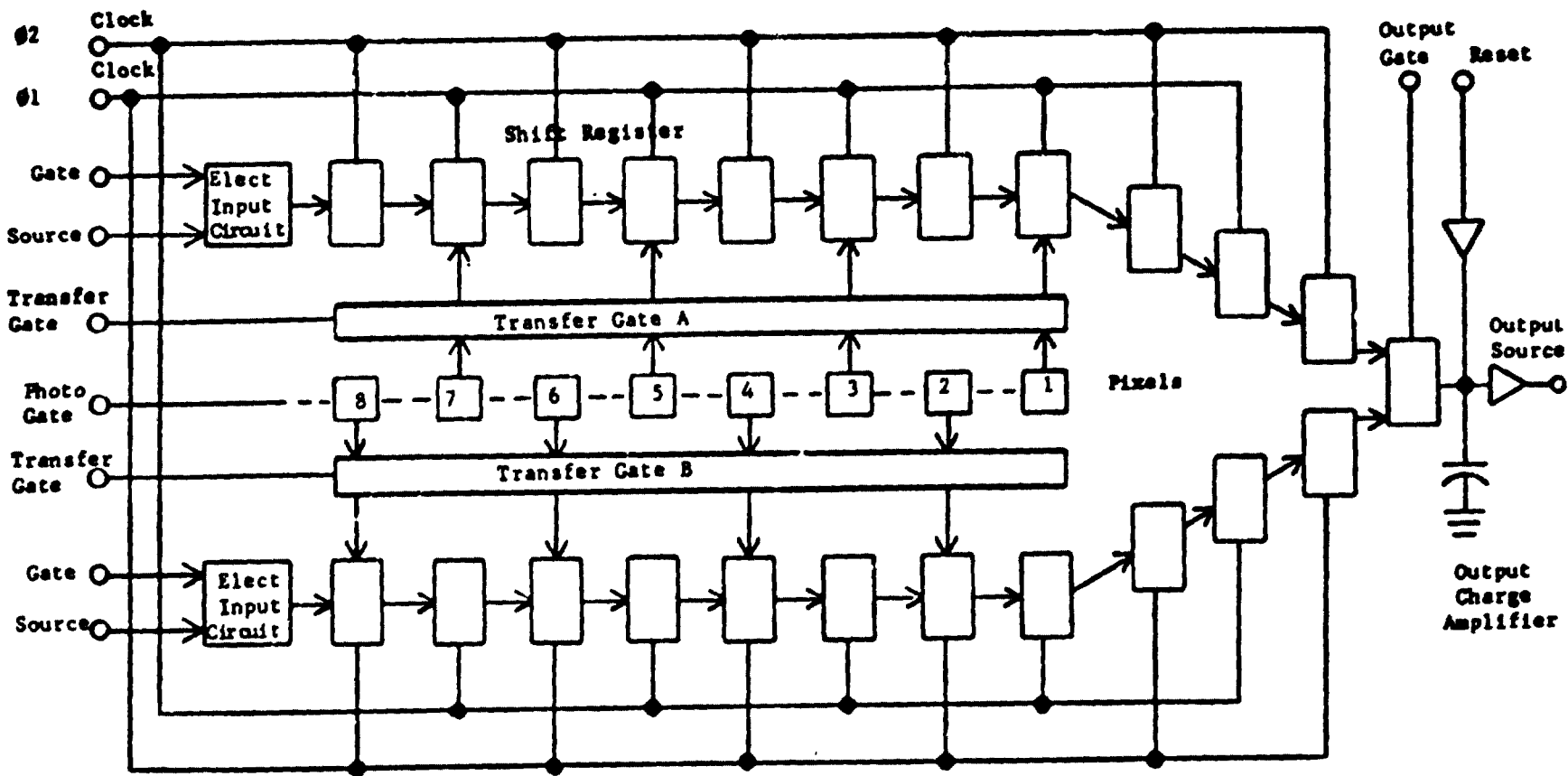


FIGURE III-3 Functional Diagram of 8 x 1 Pixel CCD Array

organized similar to that shown in Figure III-3. As we examine each of the functions in the diagram, we will be describing the CCD121H circuitry except where the differences between surface and buried channel CCD's conflict.

3. Description of the Shift Register.

Figure III-4 shows a two-phase CCD register that builds in directionality to the charge flow. One cell consists of four electrodes wired in pairs to Phase 1 and Phase 2 drive signals. The figure initiates a convention that will occur later in this report. Notice that electrodes P1 and P2 are identified by different shading (hatching). This is to illustrate that the well potential under electrodes P1 and P2 are different even though both are connected to the same applied gate voltage. This difference in interface potential can be achieved in several ways:

- a) Ion implanting the silicon after one electrode is deposited which would be self-aligning to the second electrode.
- b) Varying the thickness of the insulator beneath each of the two electrodes.
- c) Changing the work function of the two electrodes.

The spacing of the electrodes can influence the charge transfer efficiency severely. The region under an electrode gap represents a small barrier, or reduction of the schematically represented well potential profile. The exposed gap region SiO_2 can collect ionic charge and create a small work function well voltage because the silicon must "mirror" the surface charge. The different schemes in use for fabricating CCDs each try to achieve a sealed channel, that is, a zero gap condition between the electrodes. Multiple electrode structures overlap one another to achieve this. The following discussion will be limited to the process used in fabricating the CCD121H. Later, other commonly employed processes for fabricating overlapped electrode structures will be presented.

The well potential profile shown in Figure III-4 illustrates a stepped deeper well in the direction of charge transfer. Electrons (minority carriers) will "flow" as the region with the deepest well potential in a similar manner to fluid flow. The timing is shown at time t_1 . At the next clock change, t_2 , the electrodes under the Phase 2 clock line will cause V3 and V4 to switch levels with V1 and V2, respectively. This will produce forward flow to the next electrode pair. The process is carried out until the charge is shifted to the end of the register for gating out to a collection/amplification circuit. The actual implementation of the electrode structure is shown in a simplified view in Figure III-5. The electrodes labeled P1 are polysilicon deposition number 1. This layer is deposited on a thin layer of silicon nitride, doped and etched back to define P1 electrodes. Subsequently, the surface is oxidized which grows a thermally generated oxide layer over the polysilicon electrodes.

The P2 electrodes are formed in a similar manner by depositing a second polysilicon layer. The etching alignment (masking) defines the electrode overlap. Another level of doping occurs which defines a different built-in well potential than produced by P1 electrodes. The second oxidation isolates P2 from the third polysilicon layer which is deposited and etched next.

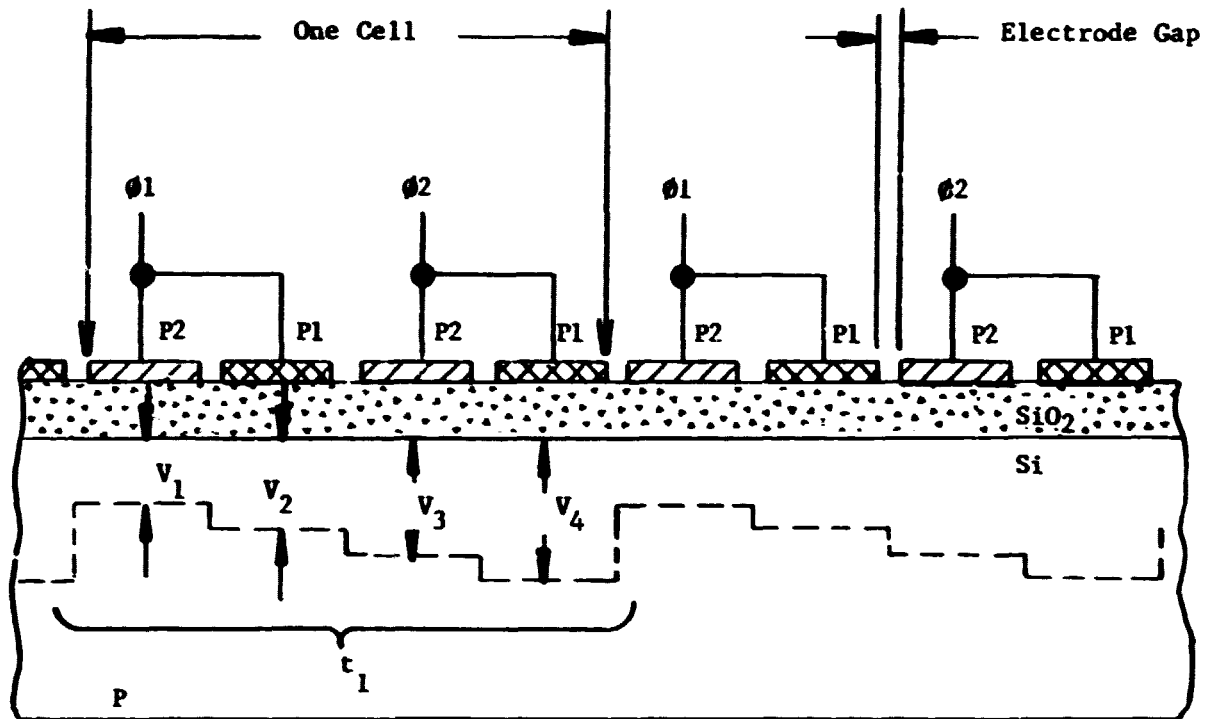


Figure III-4 Two-Phase CCD Shift Register

The diagram shown in Figure III-5 is a simplification of the CCD121H circuit in that it does not show surface or buried channel details.

4. Surface and Buried Channel CCDs.

The characteristics of SCCDs and BCCDs are most appropriately discussed along with the shift register description. They are applicable, however, to most of the CCD circuit components.

The SCCD principles are very similar to the MOS charge potential well discussed earlier. The fundamental difference between an SCCD and a BCCD is that for an SCCD minority charge is moved beneath the closely spaced electrodes at the surface along the SiO_2 -Si interface. This produces the following general advantages and disadvantages:

- a) The signal charge can interact with interface states and is generally affected by significant charge trapping loss due to ions in the SiO_2 . The BCCD has significantly improved trapping losses and less trapping noise because the charge is transported through the silicon rather than at the interface.
- b) The speed is somewhat limited by the higher electrode capacitance of the SCCD.

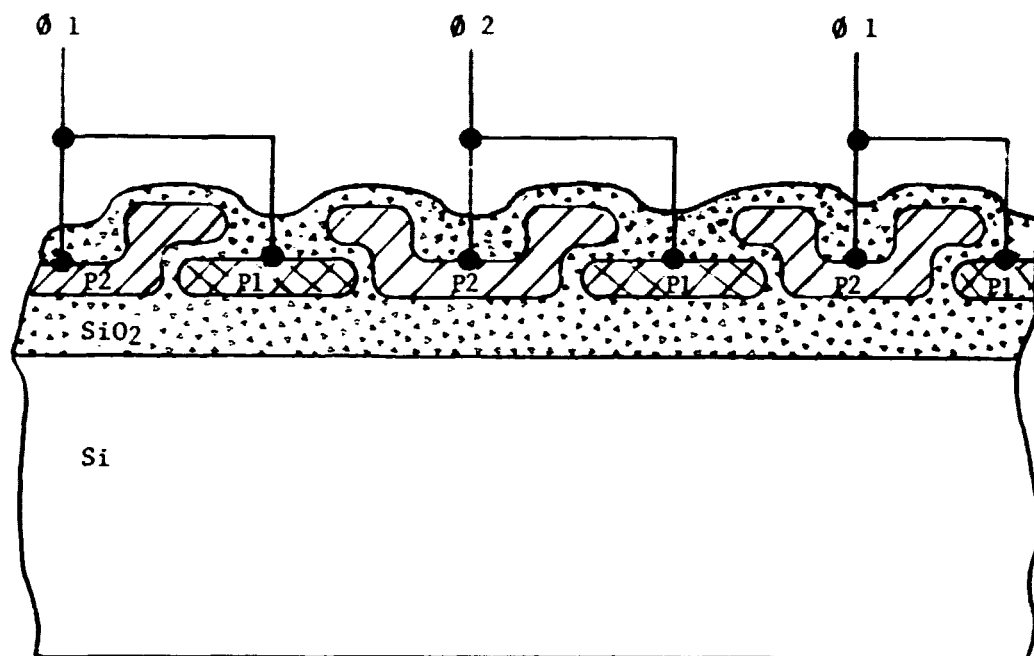
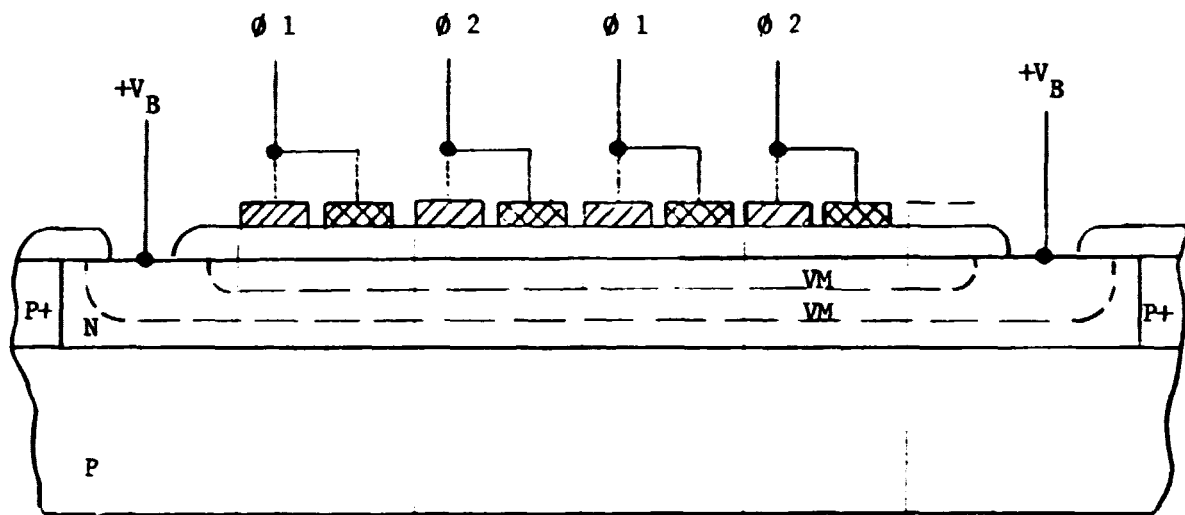


Figure III-5 CCD121H Shift Register

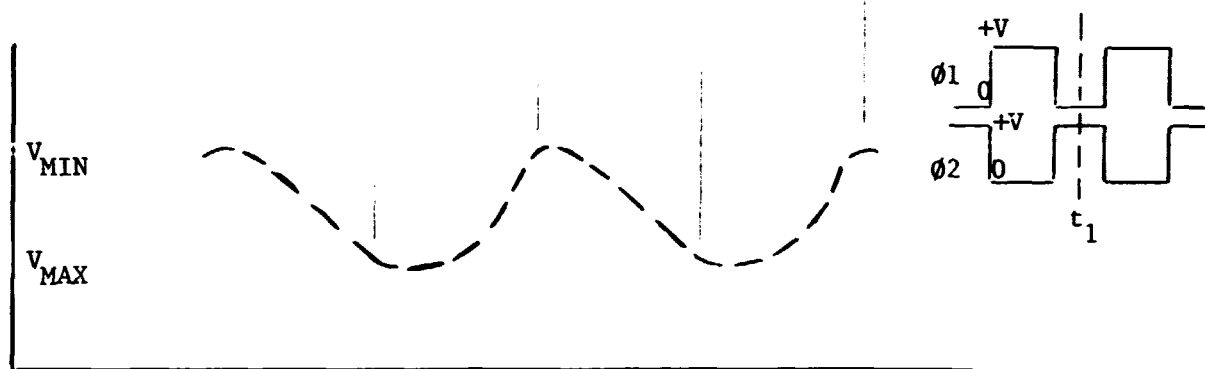
- c) The dynamic range is increased for the SCCD since charge builds from the surface downward. The BCCD channel is limited in thickness and can contain less charge than for an equivalent SCCD.

The discussion of BCCDs is significant in that the CCD121H is a BCCD and the basic principle departs from the devices described so far in this report. Some of the disadvantages of the SCCD can be overcome with the buried channel device. The BCCD has been called peristaltic CCD (Esser, 1972) due to its similarity to the peristalsis process of moving something in wavelike constrictions along an enclosed canal. The buried channel is confined laterally by channel stops and vertically by equal potential maximums in the bulk silicon. Clocking voltages applied as described in Figure III-4 constrict or open this channel thus moving the charge along the register. Up to this point the SCCD energy levels were described by the band bending diagrams of the MOS capacitor.

The CCD121H BCCD is shown in cross section in Figure III-6a. The figure shows the resulting equipotential field lines resulting when sufficient reverse bias is applied to the input and output diodes to drain out the mobile carriers (electrons) in the N region. The region between the equipotential lines is depleted forming a channel for signal charge. This channel is "peristaltically" modulated by applying two-phase clocks to the gate electrode structure. Figure III-6b shows the resulting potential well profile for the two-phase register with two electrodes at different flatband potential per phase. The BCCD has increased electron mobility because the charge is away from the surface interface states. It also has an increased fringing field created by the adjacent electrodes and higher basic field strength than with the SCCD. The longitudinal effect of the fringing field is illustrated in Figure III-6b by the smoothing of the well potential profile.



A) Cross Section Showing Potential Minima of Channel Without Gate Voltage



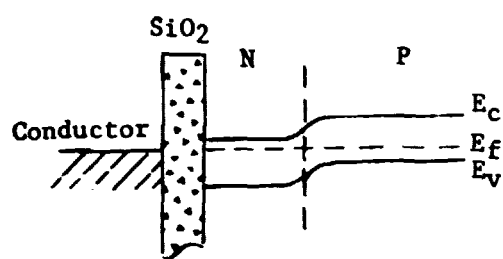
B) Corresponding Channel Potential Well with $\phi 1$ and $\phi 2$ Gate Voltage at t_1

Figure III-6 BCCD Two-Phase Shift Register

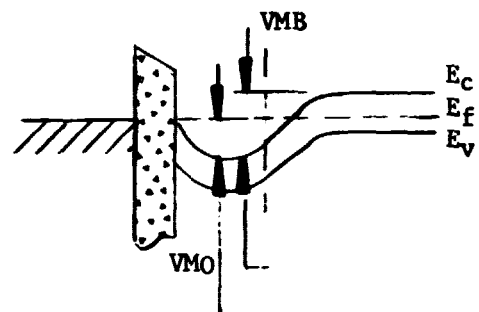
Figure III-7 shows the energy band diagrams for the BCCD structure. When the N region is unbiased, no space charge region, or channel, is formed as shown in Figure III-7a. This shows the band bending due to the N and P regions and assumes equally doped regions with the Fermi level located accordingly from the center of the respective band gaps. When the N region is reverse biased as shown in Figure III-7b, but without gate voltage applied, band bending occurs as the space charge region changes from N doped to depleted. An effective charge distribution is created within the N region which has two equipotential levels (as depicted also in Figure III-6a). The potential well varies from the minimum to the oxide, V_{MO} , and from the minimum to the bulk, V_{MB} . Under zero gate voltage, $V_{MB}-V_{MO}$ is approximately the energy difference from the N to P regions. As positive gate voltage is applied, as shown in Figure III-7c, the band is bent further, reducing V_{MO} and increasing V_{MB} thus deepening the well potential (widening the depleted channel). This is described as "modulating" the channel potential well in the references. An additional condition is examined in Figure III-7d where signal charge is present. Charge (electrons) in the well tends to flatten the band bending because the depth is a function of charge level. This occurs because the charge increases the potential energy level at the interface. The drop across the oxide is therefore increased equal to the potential drop in the silicon (since the gate voltage, V_G , stays constant). As the well begins to flatten with signal charge increase, the minimum V_{MO} , moves closer to the surface thus spreading out the signal charge. The limiting condition is felt in signal saturation as the charge reaches the surface. Dynamic range is limited, trapping losses begin to occur and increased noise due to interface state noise occurs.

5. Description of the Optical Signal Input Photosites.

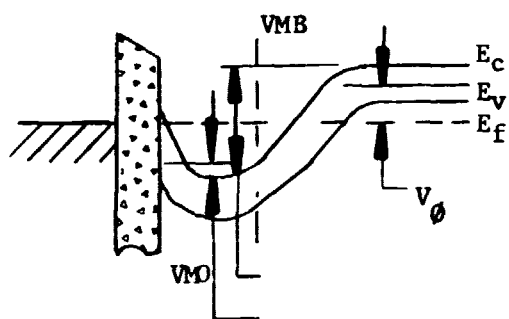
The photosites, called pixels, are created much in the same manner as a typical MOS capacitor is created as shown in Figure III-1. The photosites are illustrated again in Figure III-8. The CCD121H has an implanted N region (the same as described in the previous BCCD description). Diffusion stops (P+) isolate the photosites longitudinally along the linear CCD while the lateral confinement (not shown) is provided by lateral potential well barriers produced by the transfer gates shown in Figure III-3. The photosites contain a buried depletion as shown in Figure III-8 because the N-regions are part of the same N-region that makes up the CCD shift register (shown in Figure III-6a). These N-regions are all formed by the same phosphorous implant. The potential well under the photogate is deepened (depletion region widened) by the application of a positive photogate voltage. The photogate is transparent polysilicon created during the second polysilicon deposition, doping and etching. It has the same work function, or flatband voltage, V_{FB} , as depicted in Figure III-4 for the well potential, V_1 , when the gate voltage is zero volts. Arriving photons penetrate into the photosite and create electron-hole pairs. The holes diffuse away in the bulk silicon. The electrons are collected in the depletion region near the center



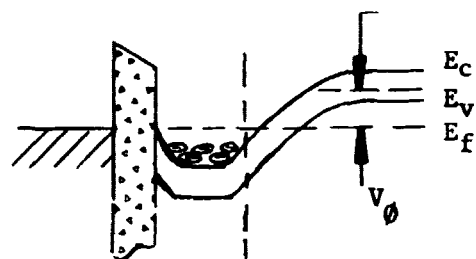
A) Unbiased, no gate voltage.



B) Reverse Biased with no gate voltage.



C) Reverse Biased with positive gate voltage.



D) Biased with full well of signal charge.

Figure III-7 Energy Band Diagrams for the BCCD

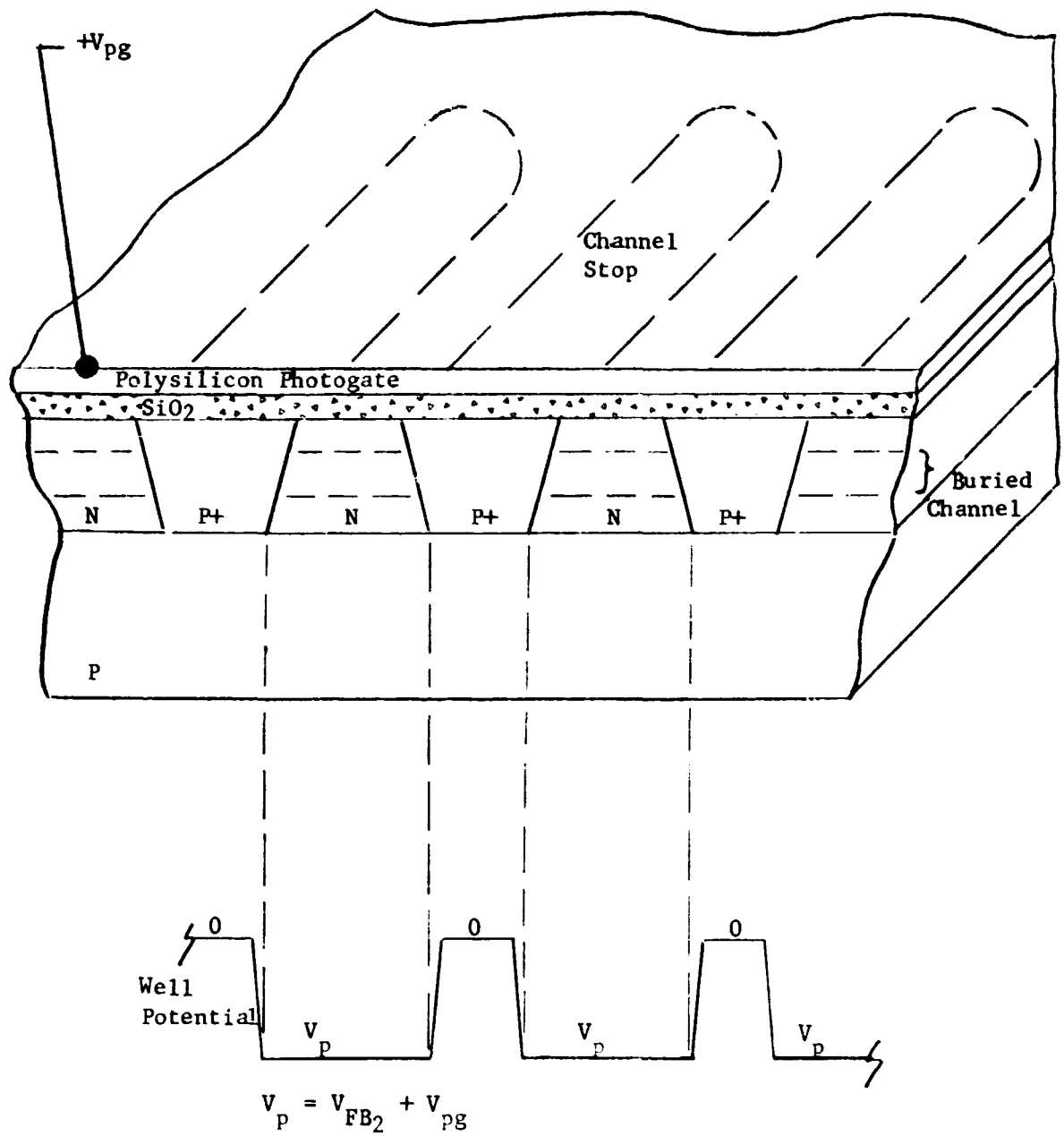


Figure III-8 Photosite Diagram

of the buried channel. The density is highest in the center since the depletion boundaries are N type and the like charge repels the photo generated electrons.

The spectral response to light is primarily determined by the absorption coefficient of the silicon. This coefficient is a strong function of the wavelength. Longer wavelength photons penetrate the photosite deeper and have a tendency to increase the crosstalk or unwanted photo response in neighboring photosites. Another factor which influences the photo response is the characteristics of the photogate. As will be shown in the test results later in this report, there are peaks and valleys in the spectral response. These are caused by interference in the polysilicon and in the silicon dioxide at the surface of the photosite.

Generally, the spectral response of a silicon imaging CCD is similar to that of silicon photodiodes. The effective short wavelength response begins at about .35 microns and the long wavelength cutoff is at 1.1 microns in the near infrared.

6. Description of the Transfer Gate.

Signal from the photosites must be transferred to the shift register in order to be brought out for external chip processing. Figure III-9 shows the transfer gates on either side of the photosites looking at an end section of the linear chip. As previously described, the photogate creates a well potential, V_p , which is equal to the flatband voltage plus the voltage on the photogate. This is the photosite shown in end view. Recall that the side view shown in Figure III-8 illustrates that the photosites are separated by diffusion stops along the length of the chip. The lateral confinement, to establish an individual element, is created by the well potential barrier due to the transfer gate flatband voltage. Figure III-9 shows the lateral view of well potential across the CCD at time t_1 when transfer is taking place from the photosites through the transfer gate to the shift register. The section is drawn through a point showing the polysilicon 1 portion of the shift register. From the previous discussion, the shift register well at this point is deepest because the flatband voltage for polysilicon 1 is largest. If one examines the functional diagram shown in Figure III-3, it can be seen that the transfer shown in Figure III-9 is for even numbered pixels. Previously, during the ϕ_{XA} cycle, all odd numbered pixels were transferred to shift register A. Photosite transfer can be considered a lateral one-stage CCD. Voltage levels must be carefully chosen to have complete transfer. For example, if the photogate voltage is set too high, the well could be deeper than the adjacent portion of the well, V_T . This would cause transfer of large signals that exceed the small inadvertent barrier between V_p and V_T . Too small a photogate voltage limits the dynamic range. The same discussion applies for the rest of the transfer into the shift register.

The transfer gate is formed with the third polysilicon deposition for the CCD121H so that it can overlap the photogate and both depositions of the shift register forming a sealed electrode structure. As previously discussed this is critical to avoid the interelectrode gap well barriers produced by unbiased exposed silicon nitride.

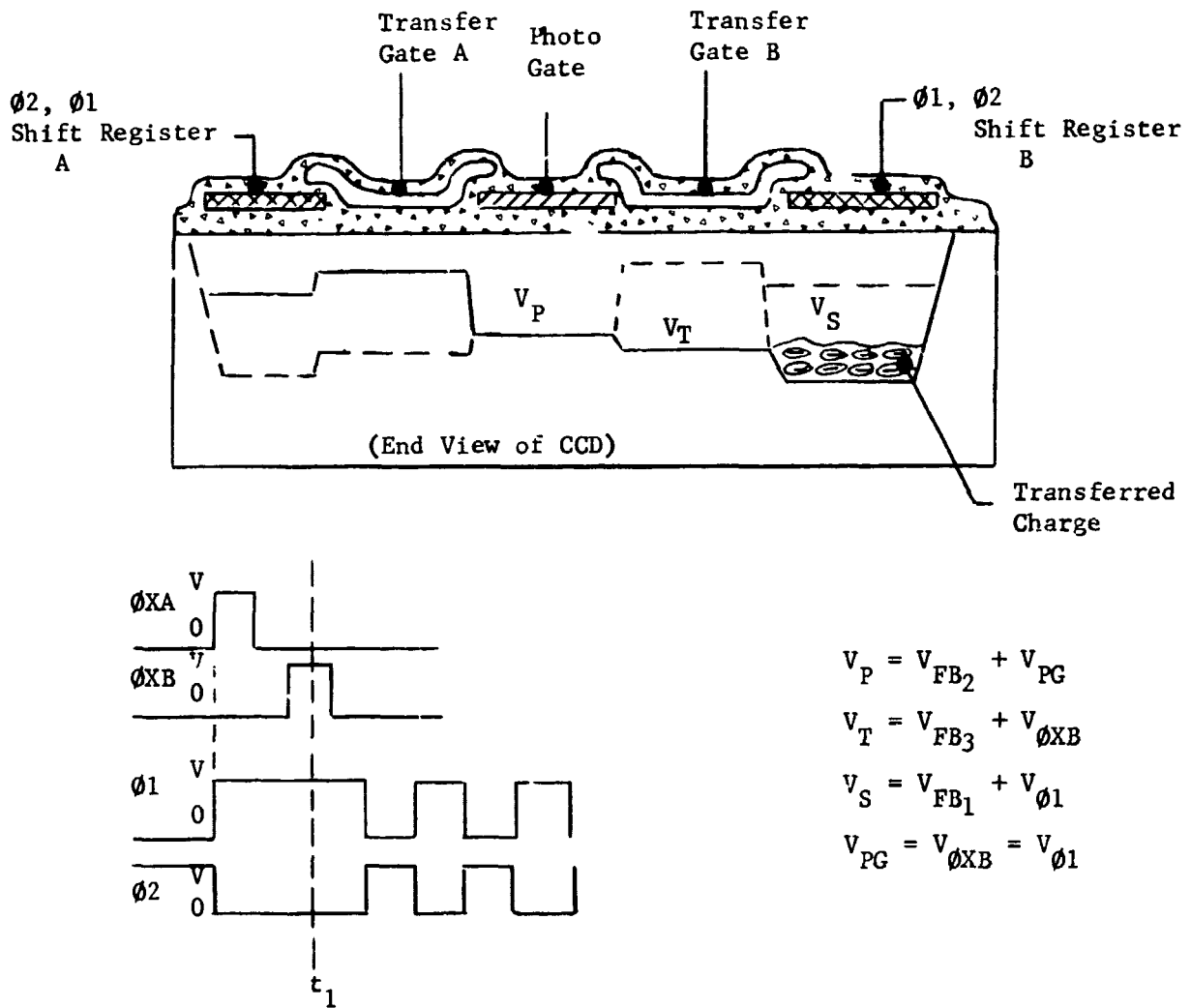


Figure III-9 Transfer Gate Structure

Not shown in Figure III-9 is the fact that over the shift register, there are now three polysilicon layers (Poly 2 overlaps Poly 1 which is overlapped by the transfer gate, Poly 3).

7. Description of the Input Circuit.

The discussion on CCD principles and the CCD121H has not previously mentioned an electrical input network. The circuit is needed for two primary reasons:

- a) Trapping losses for SCCDs are high. The traps take electrons from the signal charge as it is shifted along the CCD. If the traps are satisfied from a background charge that is electrically injected, thermally generated or optically generated, the signal can be mostly preserved. Since thermal background charge (dark signal) affects the photosites and output amplifier it is undesirable from a noise standpoint for several reasons. Optical generation is difficult to achieve but, with the proper electrical network, it is straightforward to inject a background charge. In SCCDs this charge is relatively high due to a large amount of surface states. It is often called a "fat zero" charge. For BCCDs with lower trapping losses, it is called a "slim zero" charge.
- b) For applications other than imaging, the electrical network is needed to input either digital levels or varying analog levels.

Input circuits must convert either an electrical current or voltage to a precisely controllable amount of electronic charge. The references include several discussions of these networks. The most common is called a "fill and spill" circuit which is used on the CCD121H and shown in Figure III-10. This method uses a fixed gate and a control gate to overfill a well under the control gate and spill the excess charge back to the input source well. Figure III-11 shows the sequence for injecting one level of charge, Q_1 , and following with an injection of a higher level of charge, Q_2 . This circuit is often called a voltage preset method since the floating diffusion potential between the fixed gate and control gate is switched between the two gate levels. Consider that at time, t_2 , the floating diffusion is at the level of the control gate then after the input source is pulsed, at t_4 , the floating diffusion is now at the level of the fixed gate.

The floating diffusion is effectively an infinite supply of electrons and acts as a capacitive node between the two gate voltage levels which is set and reset. By changing the control gate, one can meter in a given charge level to the shift register. As Figure III-11 shows, the input source voltage is not particularly critical so long as its low voltage switch point barrier is higher than the barrier at the fixed gate. The diagram shows flatband voltage (zero gate voltage well potential*) at three volts for Poly 2 and six volts for Poly 1.

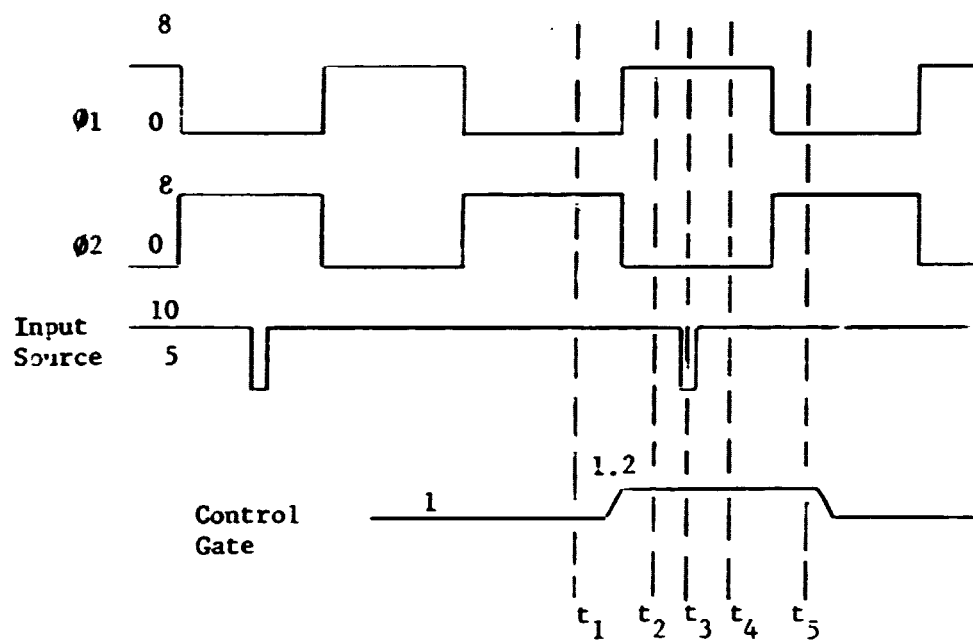
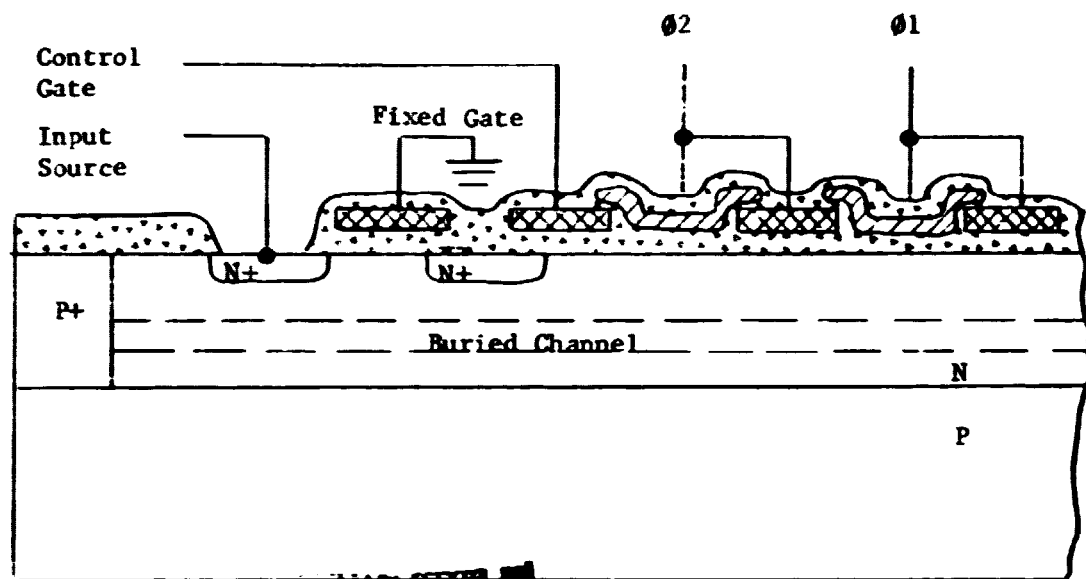


Figure III-10 Input Network

8. Description of the Output Circuit.

To complete the CCD shown in Figure III-3 there must be a method of integrating the two shift registers into one serial output charge,

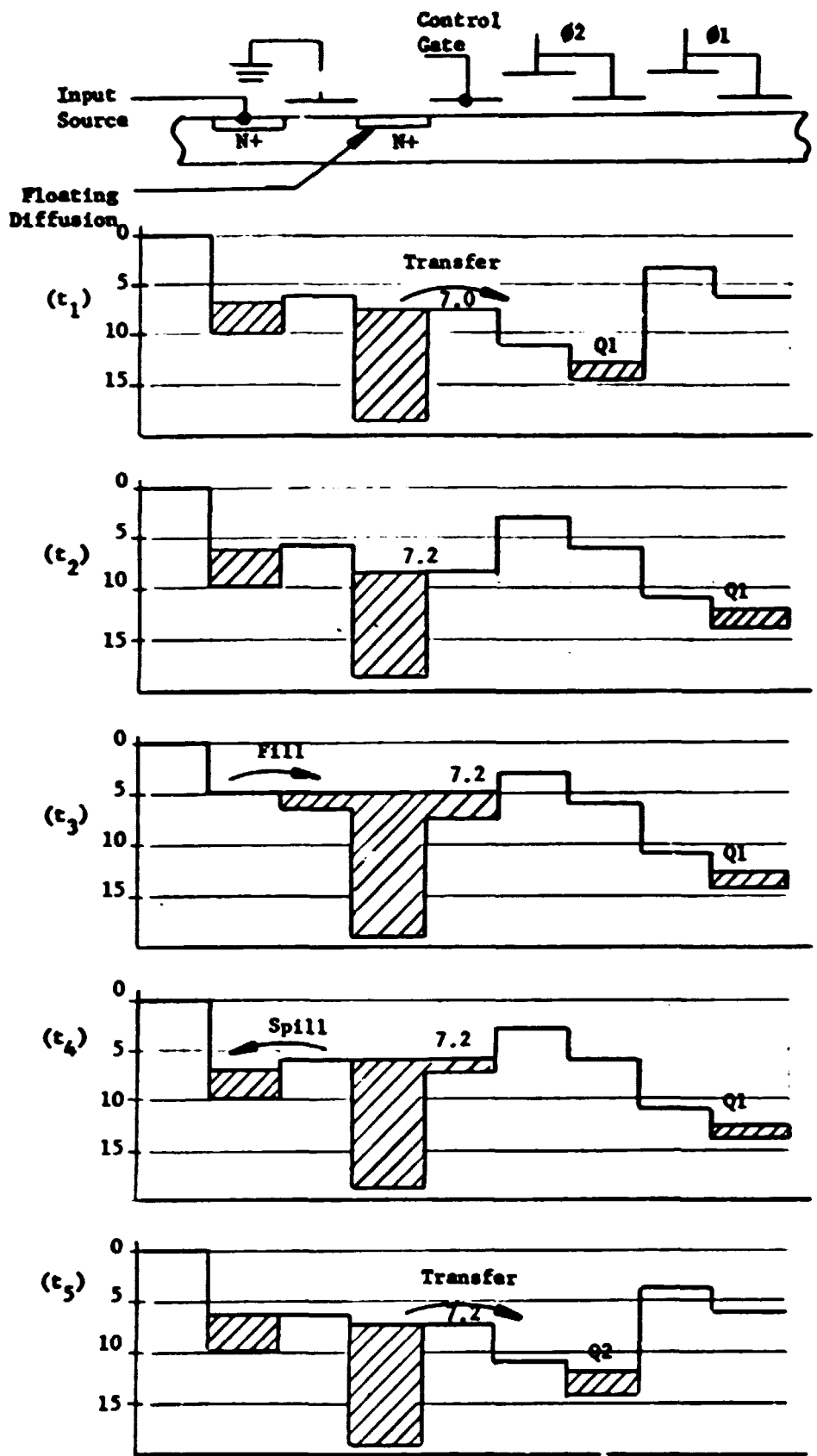


Figure III-11 Well Potentials for Input Circuit Operation

collecting the charge and amplifying it. Figure III-3 shows three extra shift register stages past the end of the line of pixels before the two registers are gated onto a charge collection capacitor. The purpose is to gradually move the charge across the chip to the output gate. This prevents losses due to larger cells that would be needed to merge the signals. The output gate shown in Figure III-3 operates as an adjustable barrier that alternately allows the signal charge from either register to be gated onto a collection capacitor. The output gate voltage must be set so that the voltage waveform appearing on the capacitor has no rising tilt or decaying tilt due to capacitor charge interaction with the registers.

Figure III-3 shows only the functional characteristics of the output circuit. The complete circuit in simplified form is shown in Figure III-12.

There are two identical amplifiers on the CCD121H. The circuits can be used with off-chip differential amplification to subtract the reset clock feedthrough signals at VOS and VCS. Each circuit consists of a capacitor, a transistor to reset the charge level on the capacitor (shown as a series resistor and switch) and a Darlington connected source follower circuit with a voltage gain of about .6.

The reset clock, ϕ_R , closes the switch, setting the voltage level on the capacitor to the reset drain voltage. After the switch opens and a shift register clock transition occurs, some electron charge is gated onto the capacitor. The voltage level changes by:

$$(1) \Delta V = \frac{\Delta Q}{C} \text{ where } \Delta Q \text{ is the charge from the output gate.}$$

The circuit is characterized by several noise sources but is dominated by the noise produced in the reset circuit. Most users eliminate this source of noise by correlated double sampling of the OS output thus ignoring the CS output. The CS output amplifier noise is eliminated as well as correlation of the noise due to the reset amplifier. The rms value of the noise due to charging capacitor C through channel resistance R is given by:

$$(2) V_C^2 = \frac{KT}{C} (1 - e^{-2t/RC})$$

where K is Boltzman's constant, T is temperature in degrees Kelvin, C is the collection capacitance and R is either the ON or OFF resistance of the FET switch.

The change is small for short intervals where $t \ll RC$. It is equal to KT/C for $t \gg RC$. One can make the time, t, be very small by sampling the OS waveform just before and just after the signal level transition occurs on the OS signal.

The reset feedthrough "porch" level is stored and electronically

subtracted from the second sample which occurs just after the shift register clock has made a transition. This transition sets the video level (charge packet) onto the collection capacitor.

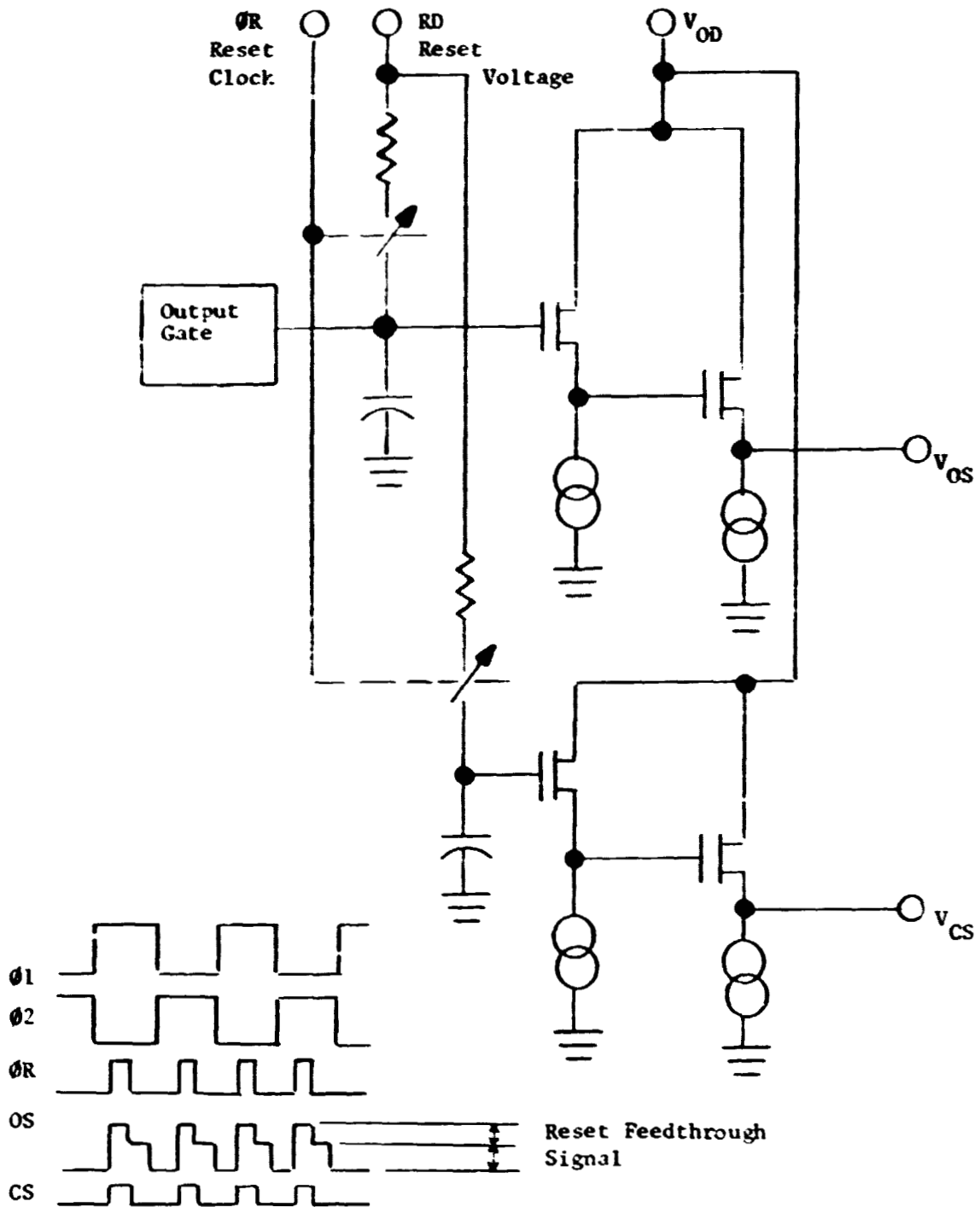


Figure III-12 Output Circuit

B. APPLICATIONS

Several important applications are presented in this section from the general viewpoint. The references contain detailed descriptions of most of the applications discussed.

The classes of applications can be separated by considering functional categories. Because the CCD is basically an analog serial shift register, it can be adapted to perform circuit functions that usually require much additional support circuitry. It also can be arranged to perform two dimensional (area array) storage and processing functions. We will separate the application classes as:

- a) Imaging
- b) Processing
- c) Memory

To give the reader some idea of the applications, we will list several in each class and comment on some of the salient features and advantages or disadvantages.

1. Image Sensors.

Linear arrays feature a self-scanning function in one direction while area arrays provide self-scanning in both directions. This, of course, reduces mechanical scanning apparatus.

a) Television Cameras

- 1) Provision of automatic, or self, scanning is accomplished with area arrays. The signal to noise ratio and resolution can be very high. Also, weight and power can be reduced.
- 2) Cooling of the array may be required to reduce the dark signal background for high quality pictures. Also, blooming due to high light intensities is a problem with most CCDs. Charge packets may reach saturation in a photosite and diffuse into adjacent photosites. Several schemes are discussed by manufacturers to reduce this effect.

b) Low Level Imaging: Cameras, Telescopes, and Other Devices

- 1) Very high signal to noise ratios can be achieved especially with cooling. Typical numbers for noise can be as low as 20 to 30 electrons equivalent charge. Self-scanning also is a significant advantage.
- 2) Cooling requires considerable input power in many cases. Circuit (CCDs) yield is still low when it is desired to have defect-free devices; e.g., no bad pixels due to high dark signal or nonuniform response.
- 3) Production inspection on assembly lines. Counting.

self-scanned dimensional measurements, visual quality (inspection of currency), specific types of flaw inspection.

- 4) Facsimile page readers.
- 5) Infrared Imagers. Both hybrid and monolithic approaches are available. Hybrid approaches combine separate detectors with CCDs while monolithic devices can be fabricated so that spectral sensitivities extend past normal silicon wavelength cutoff (1.1 microns).

C. SIGNAL PROCESSING

The CCD can be used in a variety of ways to store, delay, recirculate, filter and process analog signals.

1. Analog Delay Lines. Tapped delay lines.
2. Frame Subtractors. Subtraction of one analog frame from another.
3. Time Division Multiplexing.
4. Fourier Transform of an Optical Image.
5. Recursive and Transversal Filters.
6. Waveform Generation.

D. DIGITAL AND ANALOG MEMORIES

In digital memories there is very high competition to reduce the cost per bit. The CCD is very competitive although the access time is slower due to its serial nature. The CCD competes well with devices used for serial storage such as drum, disc, and other serial storage mediums using one head per track approaches.

The disadvantages are that the CCD memory is volatile and must be refreshed periodically due to the thermal buildup of dark signal. Manufacturers are now producing 65K bits on a single chip with excellent yields.

E. PROCESSES

The introduction to CCD principles included the CCD121H description without discussing various other methods or processes for polyphase clocking schemes now being used in manufacturing CCDs. In practice several approaches are used for providing multiple phase clocking to

achieve directional transfer of charge through the CCD. Three-phase and two-phase are most often used. When three, or more, phases are employed, the processing can be simpler because the electrodes can be of a simple structure with the gate voltage and timing producing the stepped well. The two-phase structure described for the CCD121H requires additional processing steps because for each cell, four electrodes are required with alternate electrodes having a different flatband voltage. The two-phase CCD could be considered a four-phase structure because the four electrodes of a cell are all operated at a different well potential during a given clock period. Adjacent Poly 2 and Poly 1 electrodes are connected to the same clock phase as shown in the introduction section. Three-phase systems were developed first because of the simple electrode structure requiring only a simple flatband voltage in the process. The primary disadvantage of the three phase structure is that conductor crossovers are more complicated to connect the drive signals to the electrodes. Because the wafer processing is more representative for two-phase systems and also being used more widely, this discussion will be limited in scope to these processes that implement the two-phase structure.

1. Two-Polysilicon CCD121H Process.

The process already described for the CCD121H uses two polysilicon depositions that are doped differently to produce about a 2:1 variation in the flatband voltage as shown in Figure III-13.

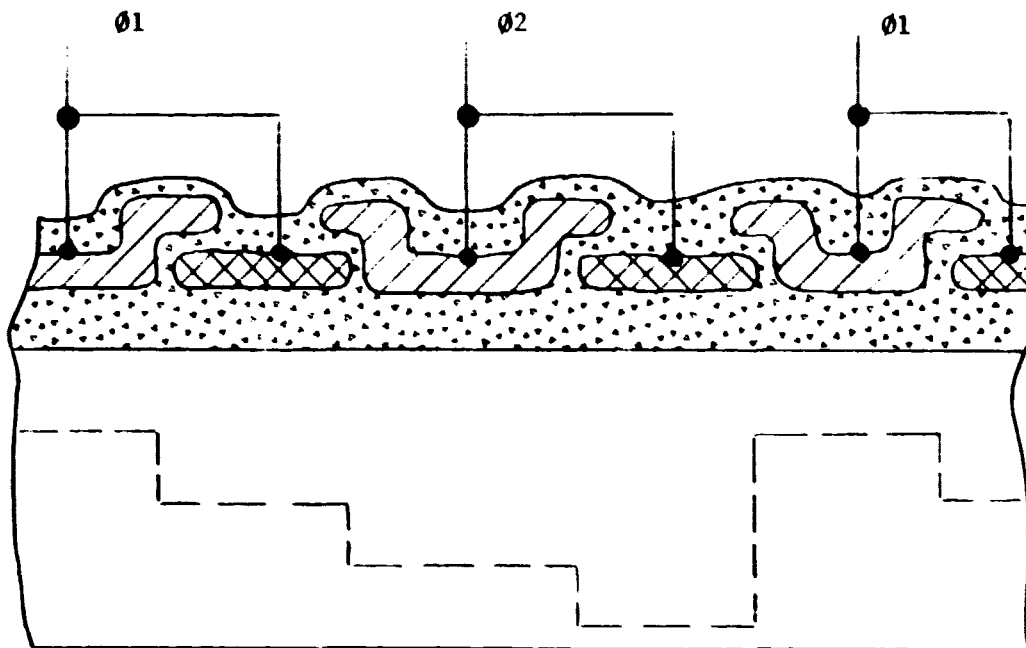


FIGURE III-13. Two-Polysilicon CCD121H Process

2. Stepped Oxide Process.

The work function can be varied between the transfer and storage electrode by depositing the electrode conductors on two different thicknesses of silicon dioxide as illustrated in Figure III-14. In an SCCD the deepest well potential occurs beneath the electrode on the thinnest oxide. The opposite occurs for a BCCD because as the oxide thickness increases, the positive buried layer charge at the N diffusion to P interface is opposed less by the surface charge. More of the charge is neutralized by the depletion region in the substrate. A measure of well depth is illustrated by term V_{MB} in the energy band diagram shown in Figure III-7. Several methods are described in the references for achieving stepped oxide directionality of charge transfer.

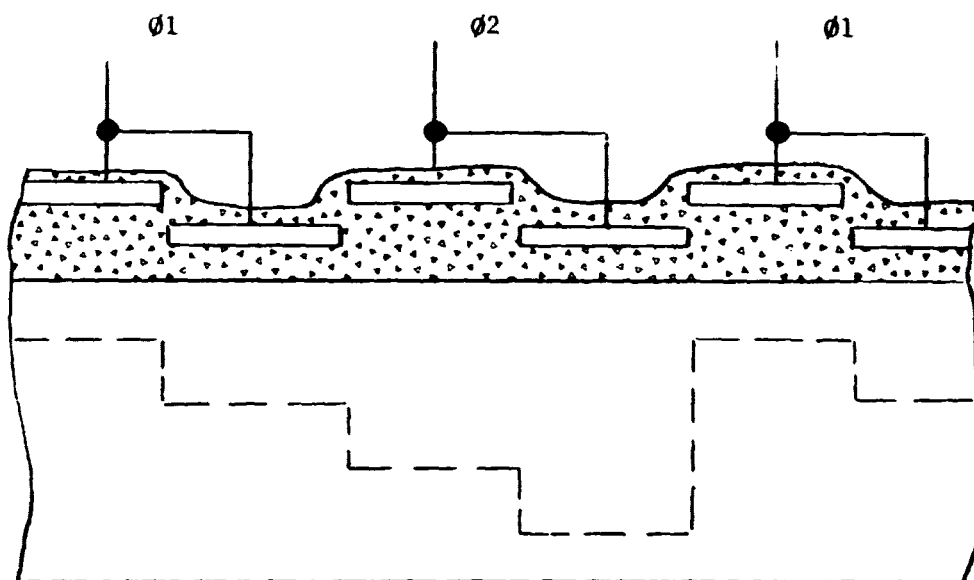


FIGURE III-14. Stepped Oxide Process

The simple stepped oxide approach shown in Figure III-14 is usually combined with other techniques to minimize interelectrode gaps and to enhance the work functions. One approach is to combine a polysilicon storage electrode with an aluminum transfer electrode. The work function is 3.2 eV for aluminum and about 4.5 eV for polysilicon (a function of the polysilicon doping).

3. Stepped Oxide Combined with Different Work Functions.

Figure III-15 shows an aluminum storage electrode with the work function reduced further by a positive ion implant combined with a polysilicon storage electrode and stepped oxide.

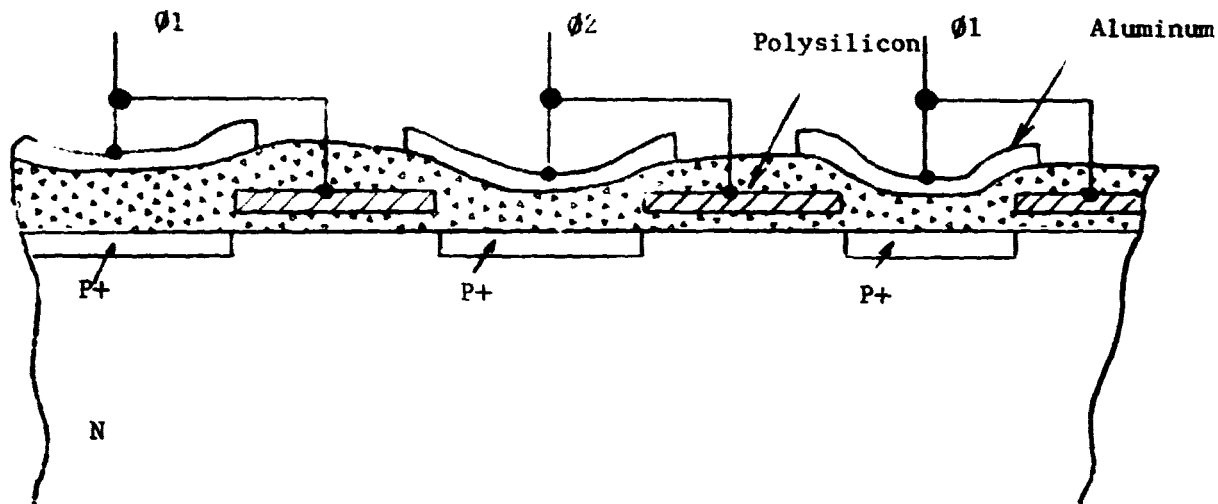


FIGURE III-15. Stepped Oxide Combined with Two Different Work Functions

4. Aluminum-Aluminum Oxide-Aluminum.

Figure III-16 shows a three-phase structure which employs anodized aluminum as the insulating layer between the electrodes.

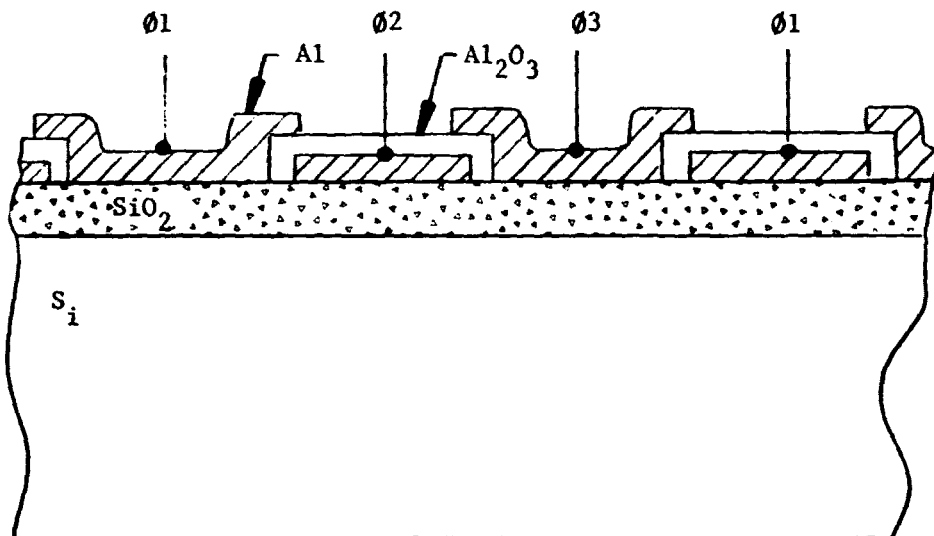


FIGURE III-16. Three-Phase Al-Al₂O₃-Al Structure

This process is usually implemented with three- or four-phase devices since adjacent electrodes have the same work function and cannot, therefore, be connected together to make the double electrode two-phased CCD.

In addition to the processes listed in this section for fabricating CCDs, many innovative techniques have been reported. Some of these are listed below:

- a) Stepped oxide combined with undercutting to create gate overlaps.
- b) Stepped oxide with an effective electrode pair created by depositing aluminum at an angle to the surface. Adjacent pairs are separated by shadow effects during aluminum deposition.
- c) VMOS combined with N⁺ conductive coupling between electrodes.
- d) Stepped oxide created by a deposited oxide layer on a grown oxide layer.
- e) Three-phase triple-polysilicon electrode structures.
- f) Shadow etch techniques to reduce interelectrode gaps.
- g) Buried positive trapped charge in silicon nitride to create variations in work functions.

IV. PROGRAM RESULTS

Data is presented that will describe how the CCD121H is constructed and its electro-optical performance. The final section analyzes the packaging stress that results in bonding two dissimilar materials especially when dealing with large semiconductor chips. The CCD121H is .9 inches long by .06 inches wide. This can result in severe built in stresses as well as environmentally sensitive stress levels.

In each of the following sections the intent is to relate to the reliability of the device when presenting the data.

A. PHYSICAL CONSTRUCTION

1. Functional Schematic.

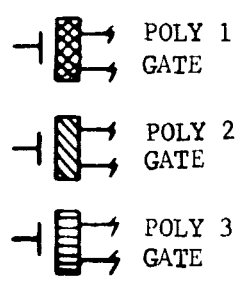
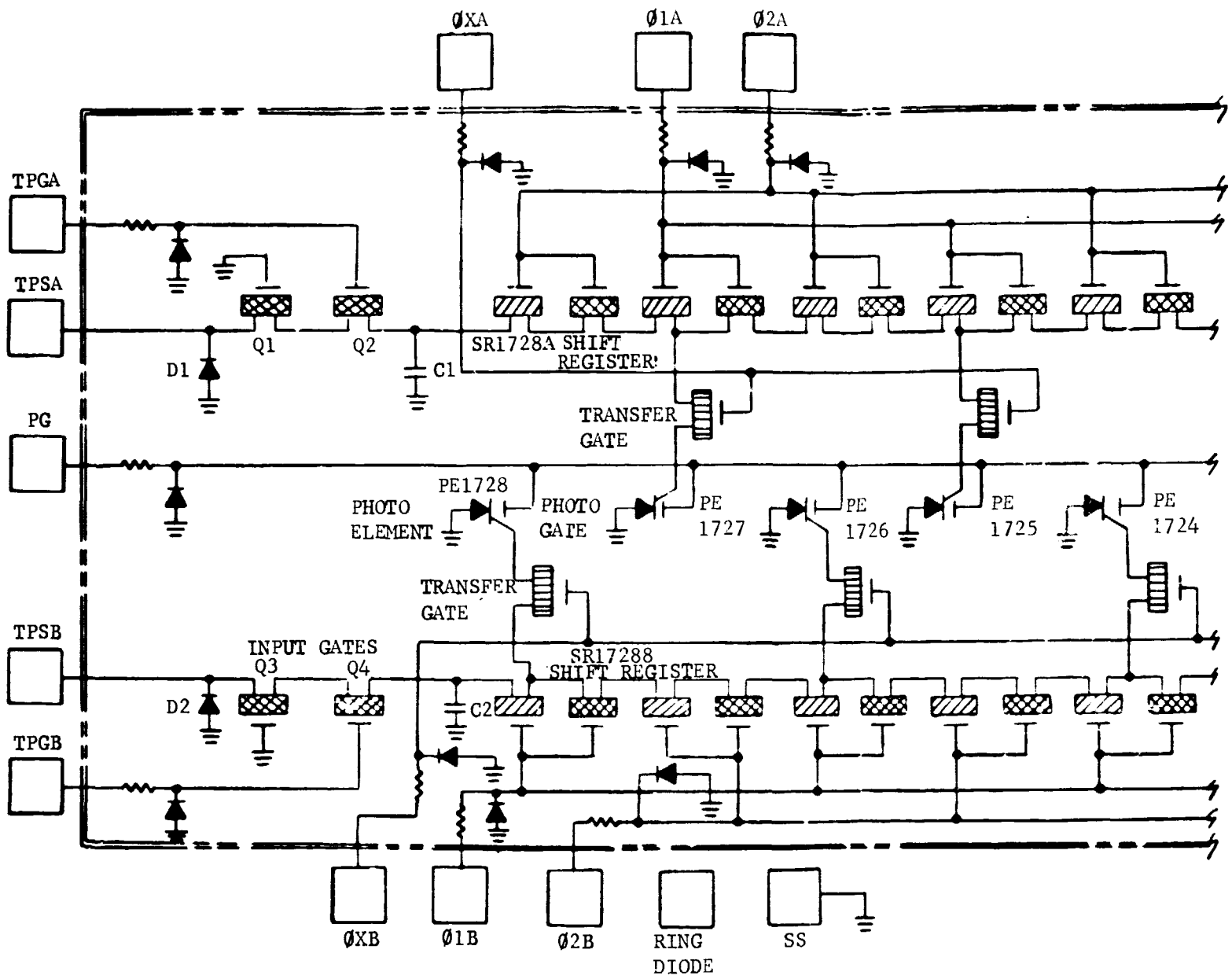
A simplified schematic diagram of the CCD chip was generated to provide a conceptual overview of the total circuit and for use in relating the chip location of the functional components. The schematic diagram is shown in Figure IV-1.

The input gate circuits (D1, Q1, Q2, C1 and D2, Q3, Q4, C2) provide the means for charge injection into the shift registers. A negative going pulse applied to the test point source (TPS) injects a charge through Q1 and Q2 and charges (fills) capacitor C1. When the input (TPS) returns positive the charge amplitude at C1 is determined by the potential barrier height "spills" back through Q2 and Q1 equilibrating the C1 charge to a specific amplitude. The injected charge amplitude is adjusted by the applied gate voltage of Q2. The injected charge is transferred from C1 into the shift register by the Phase 1 and Phase 2 clock signals. The injected charge provides a specific zero signal compensation or "slim zero" in the shift register potential wells. The physical location of the input gate components are identified in Figure IV-2. Diodes D1 and D2 and capacitors C1 and C2 are intrinsic to the chip structure.

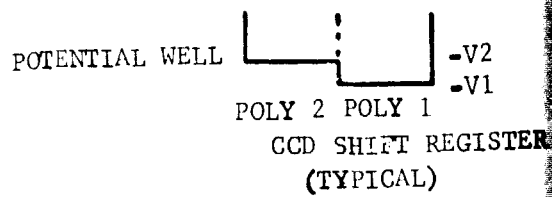
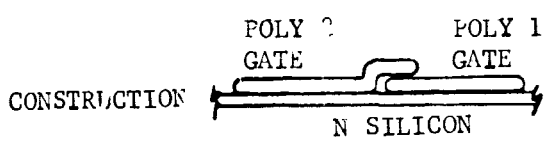
The photo element, transfer gate, and shift register are formed by a single rectangular N doped diffusion. The physical location of these devices is shown in Figure IV-3. The photo elements and transfer gates are isolated from adjacent pixel channels by P+ doped channel stops. The gate and shift register electrodes are formed by three separate polysilicon films. The modified work functions produce different intrinsic potential well depths for equal gate oxide thicknesses. Refer to Figure IV-4. These differences in potential well depths are especially important to the shift register operation.

The photo element has a transparent polysilicon gate overlay. This gate is called the photogate. The voltage applied to the photogate adjusts the potential well for the photo element. The photo element

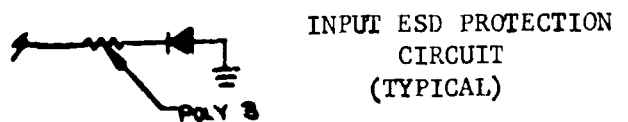
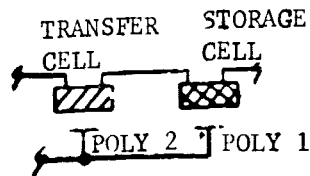
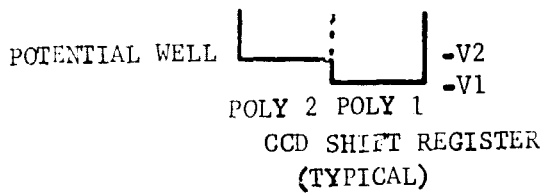
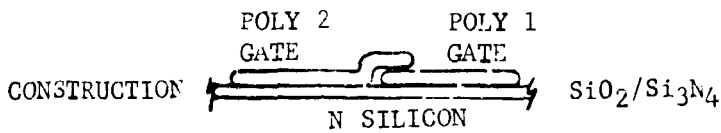
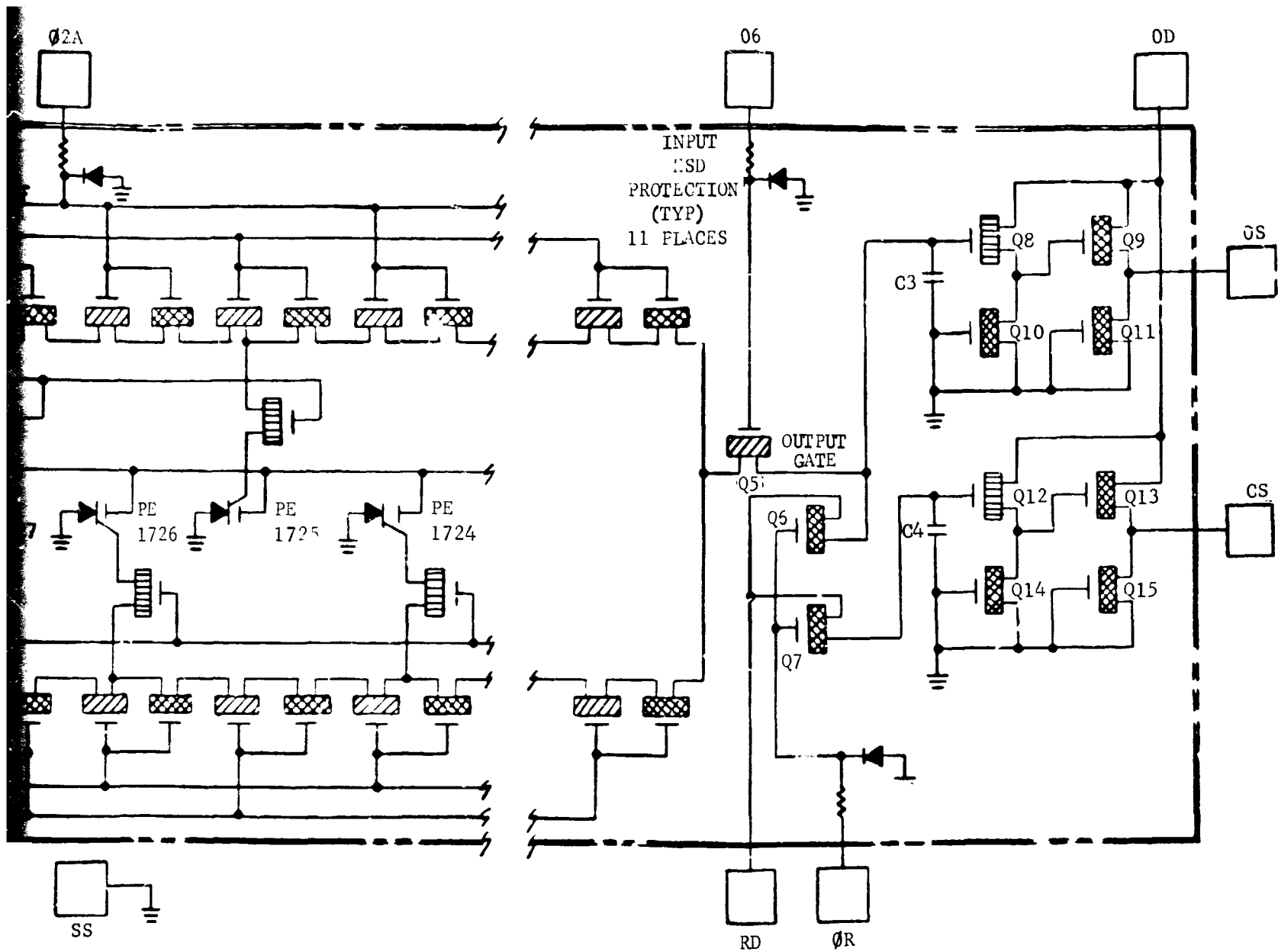
potential well depth determines two basic factors, the electron storage capacity of the cell and the quantity of stored electrons accessible for transfer from the cell. When the potential well depth is inadequate the cell will saturate and image contrast will be lost.



SCHEMATIC DESIGNATION



FOLDOUT FRAME



FOLDOUT FRAME

Figure IV-1 Functional Schematic, CCD121

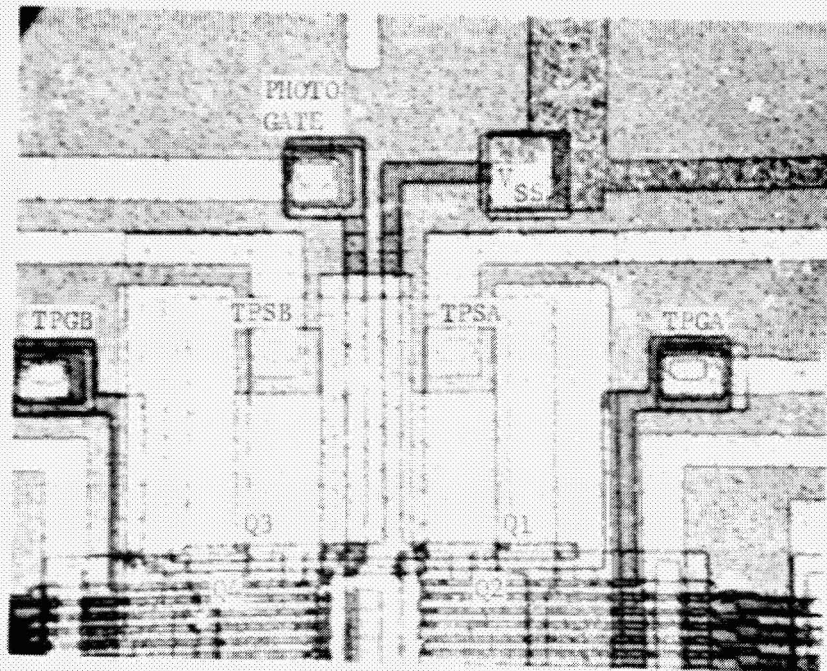


Figure IV-2 Photograph showing the input gate components and signal lines. Mag. 500X

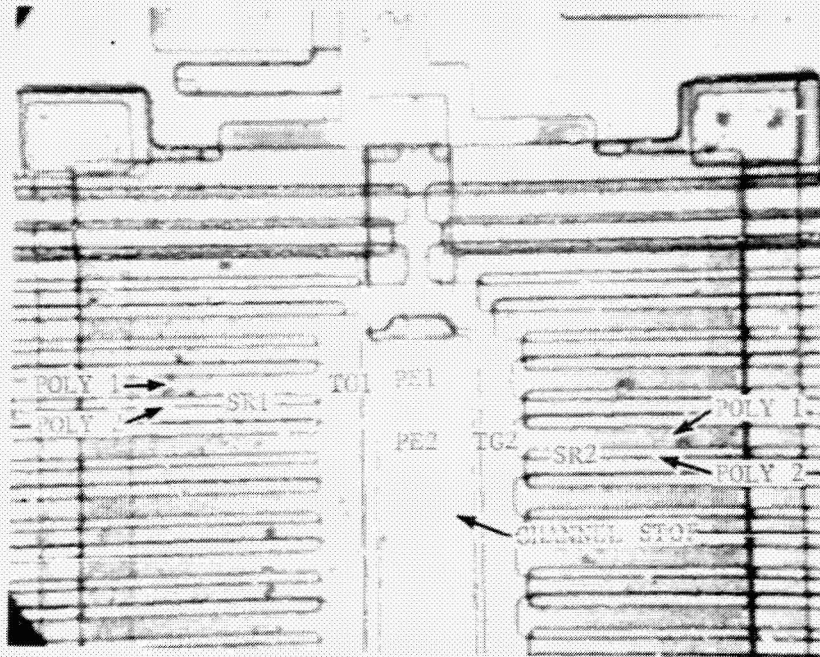


Figure IV-3 Photograph showing photo element, transfer gate, and shift register locations. Mag. 500X

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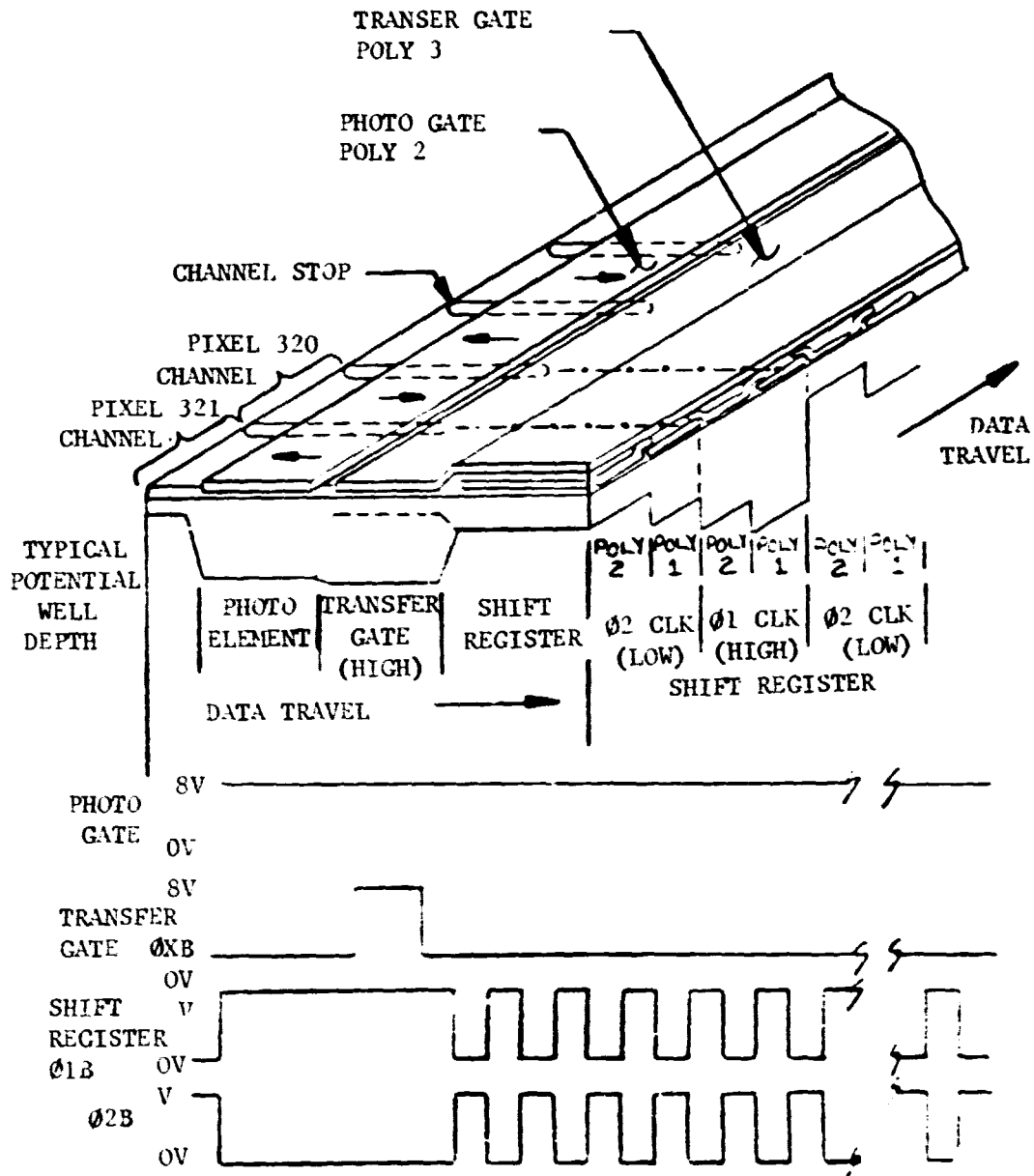


Figure IV-4 Cross Section Diagram

The potential well depth requirement is dependent upon the cell acquisition time or array integration time and the image brightness or signal intensity. When the potential well depth is excessive only the stored electrons in excess of the transfer gate potential well will transfer from the photo element potential well.

Figure IV-4 shows an isometric cross section of the CCD array. This figure shows one side of the array. The photo elements are located along the centerline of the die and this figure describes the array operation to the right of center. The potential well depth for the transfer gate is determined by the transfer gate voltage and as described earlier, the potential well depth for the transfer gate may prohibit total transfer of the electrons from the photo element to the shift registers. Typically the transfer gate potential well level should be between the shift register Poly 1 and Poly 2 potential well levels, with a high clock state present for both the transfer gate and the shift register gates. Signal generation, transfer and shifting to the output amplifier occurs as follows:

- a) Light energy dissipated in the photo element produces electron-hole pairs. The holes diffuse across the P-N junction created by the channel stop diffusion. Electrons accumulate in proportion to the dissipated light energy.
- b) Transfer gate :XA and shift register clocks Phase 1A and Phase 1B are switched high and shift register clocks Phase 2A and Phase 2B are switched low. Stored electrons are transferred from odd numbered photo elements to the left side shift register as illustrated in Figure IV-4. Stored electrons for even numbered photo elements cannot be transferred because the respective shift register gates are low and this presents a high potential barrier for these transfer channels. The transfer gate :XA is switched low, transfer gate :XB is switched high and shift register clocks are maintained in the same states. When :XA is switched low the signal integration time for the odd numbered photo elements begins. When :XB is switched high the stored electrons for the even numbered photo elements are transferred to the right side shift registers. As :XB is switched low the signal integration time for the even numbered photo elements begins. Next, the transferred signals (electron packets) are shifted down the shift registers. This is accomplished by the two-phase clocks Phase 1 and Phase 2. As the shift register clocks are switched the electron packets are moved down the registers on the potential well wave front. This is illustrated in Figure IV-4. The electron packets reside at the lowest potential level. As one clock voltage decreases the respective potential level rises. Simultaneously, the opposite phase clock voltage increases and the respective potential level falls allowing the electron packets to spill forward in the direction of data shift. Note that adjacent electron packet isolation is maintained by a high potential barrier in front and back. As described earlier, the potential staircase is generated by the difference in work functions between Poly 1 and

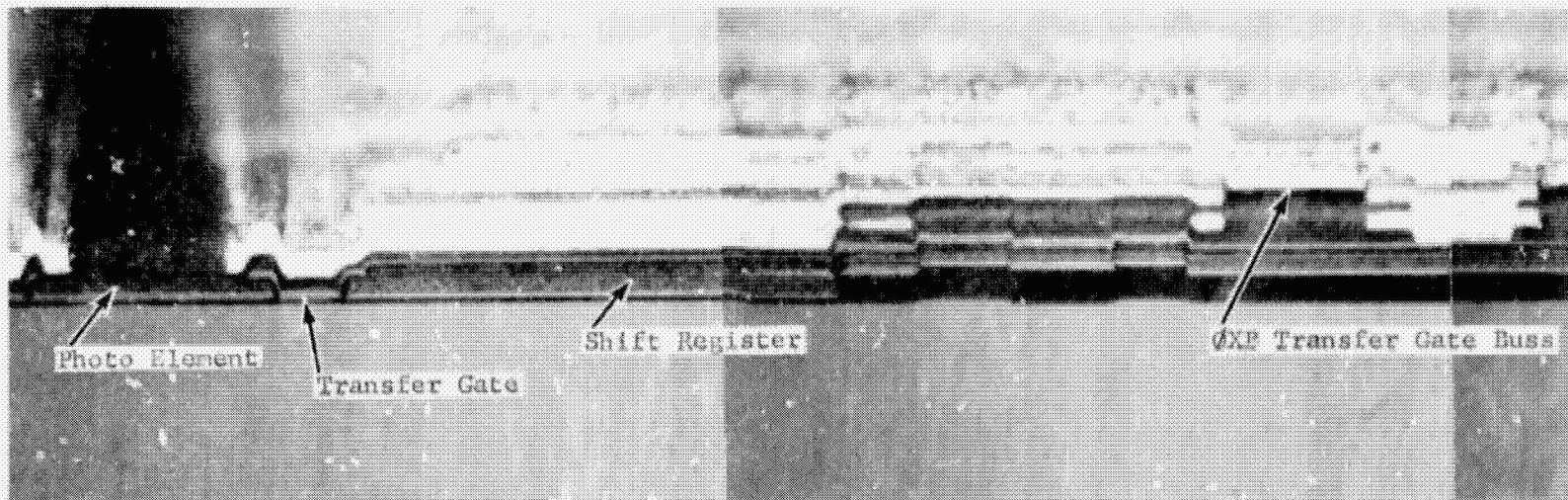
Poly 2. Odd and even electron packets merge at the output gate/gated charge detector (Q5, C3) in serial form beginning with photo element 1 and ending with photo element 1728. (Reference Figure IV-3.) These serial data travel through the output amplifier (Q8-Q11) and arrive at terminal OS. When the electron packet for photo element 1728 arrives at the gated charge detector the next serial data sequence begins by setting the shift registers and enabling the transfer gates. The gated charge detector is precharged through OR and RD. The variations in quantity produces a linear change in voltage at the gate of Q8. The on-chip output amplifier has a typical gain of 0.6 and provides isolation for the gated charge detector. A second on-chip amplifier, having the same characteristics as the output amplifier, is provided (Q12-Q15) for compensation of the reset transient that is also present in the OS output signal. These outputs can be applied to an external differential amplifier to subtract the reset transient noise.

2. Aluminum and Polysilicon Conductors.

The CCD:21H array utilizes three polysilicon conductive layers, one aluminum metal conductor layer and an aluminum metal light shield. The complexity of five conductive layers required multiple cross sections from the side and end of chips to determine the interconnection configurations. The cross section data were compared (side view to end view) and correlated to a top view. This provided a three dimensional correlation.

An end view cross section of the photo element, transfer gate and shift register regions are shown in Figure IV-5. This view shows a typical signal flow path as it travels from the photo element through the transfer gate into the shift register. The Poly 2 photogate is shown over the photo element. Electrical connection to the photogate is made at the input end of the chip. Adjacent to the photo element is the Poly 3 transfer gate. This poly layer continues out and terminates with the aluminum transfer buss conductor. Adjacent to the transfer gate is one of two adjacent shift register electrodes. This is a Poly 1 electrode which continues out and terminates with the Phase 1 clock buss. The plane of this section does not show the second Poly 2 shift register electrode. The first level aluminum conductor which extends between the photo element and just short of the X transfer buss provides a light shield for the array. It is the primary light shield between the edge of the photo element and the shift register and the secondary light shield between the shift register out to the die edge.

A side view cross section of the array is shown in a sequence of Figures IV-6 through IV-12. Figure IV-6 shows the transition region between the transfer gate and shift register. This photo shows the first level aluminum light shield, the Poly 3 transfer gate, and the Poly 1/Poly 2 shift register overlap scheme. Continuing away from the transfer gate into the shift register Figure IV-7 shows the start of the second level metal light shield. This photo shows the shift register structure of Poly 1/Poly 2 electrodes with a transfer gate



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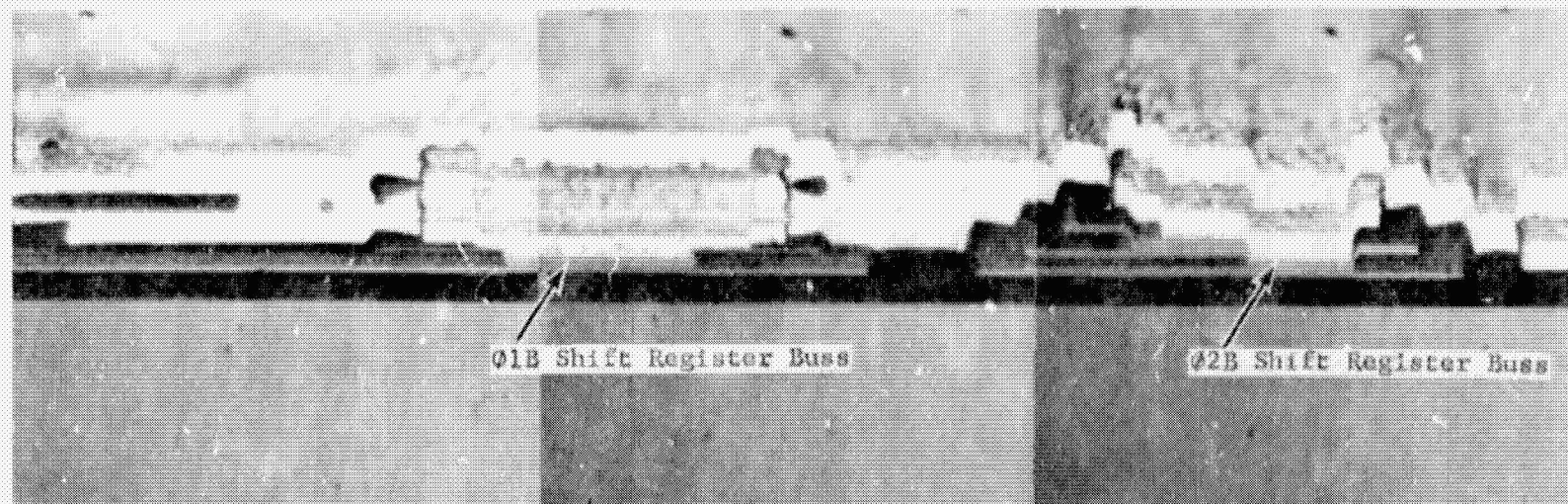


Figure IV-5 Cross Section, End View, Showing The Photo Element, Transfer Gate and Shift Register Regends. Mag. 1200X

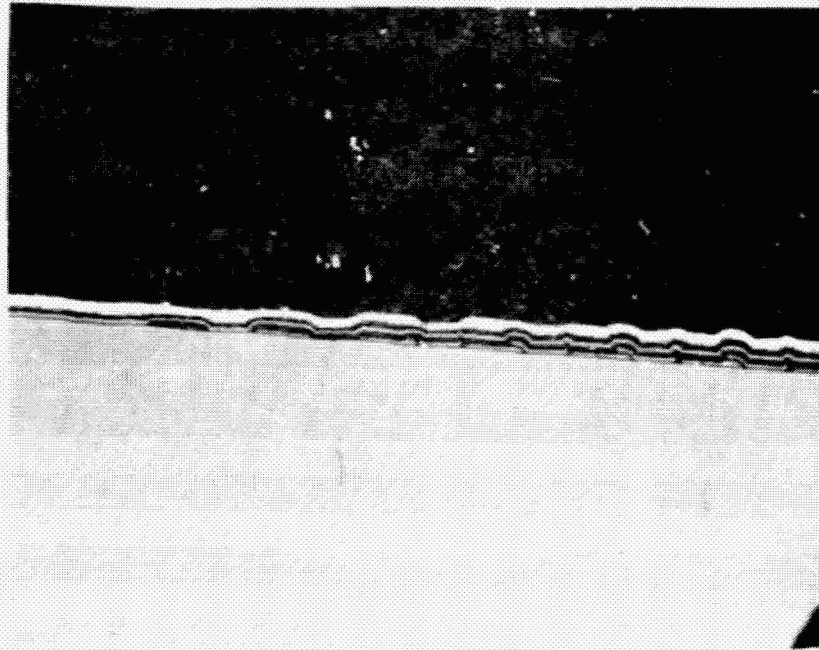


Figure IV-6 Photograph of a side view cross section showing the transition between transfer gate and shift register. Mag. 1200X

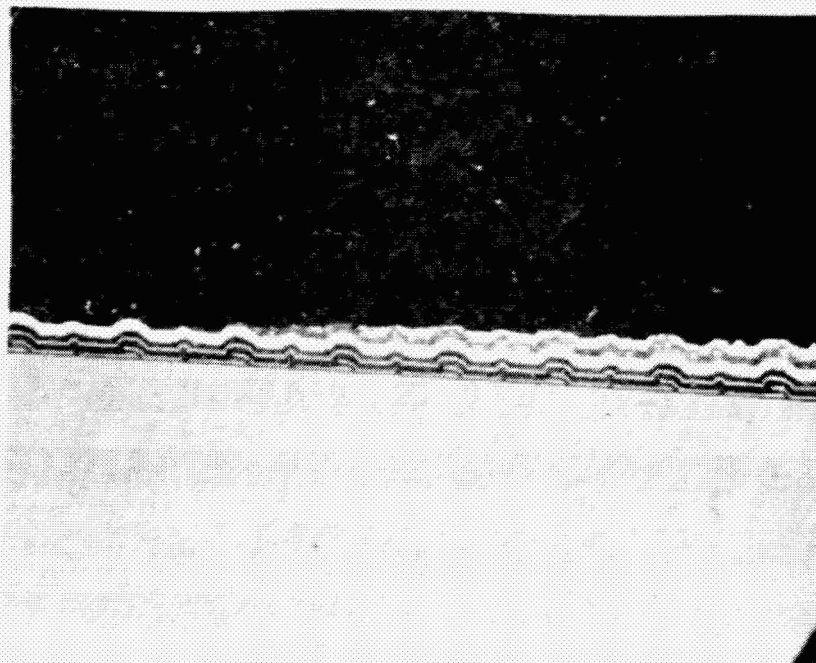


Figure IV-7 Photograph showing the shift register electrodes. Mag. 1200X

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Poly 3 overlaying these electrodes. These three layers are covered by first level aluminum which is serving as a light shield. All five layers are electrically isolated by silicon oxide. Figure IV-8 shows the area where the shift register electrodes further separate from the silicon surface. At this point the electrodes are beyond the active area of the shift register. There appear to be circular voids in the passivation between first and second level aluminum. This is believed to be crack sites which occur during sectioning due to the poor support provided by the aluminum film on both sides. Figure IV-9 shows the contact region between the Poly 3 transfer gate and the first level aluminum transfer buss. The Poly 3 film stops shortly beyond this contact region. Figure IV-10 shows that the remaining Poly 1 and Poly 2 films begin to form pairs. Figure IV-11 shows the Poly 2 film positioned directly over the Poly 1 film. Figure IV-12 shows the contact region for the alternate Poly 1/Poly 2 pair through a Poly 3 film to the first level aluminum Phase 1 clock buss. The remaining Poly 1/Poly 2 pair continue out where they likewise make contact to the Phase 2 clock buss.

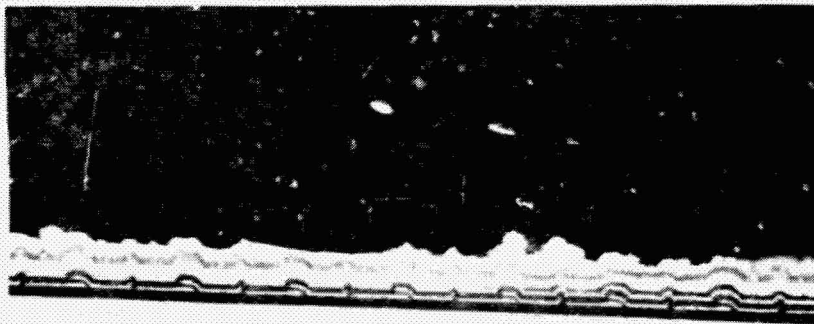
From these cross section data and surface photographs a composite isometric view was generated to further describe the array. The composite isometric is shown in Figure IV-13. At this point it becomes possible to appreciate the complexity of the conductor interconnect system for this array. The CCD array chip is approximately .9 inches long and 0.06 inches wide. At the magnification shown (250X) this chip would be 250 inches long. The polysilicon oxidation process is a combination of thermal oxidation and deposited glass. The thermal oxidation of the polysilicon produces an integral passivation around the conductor. This eliminates the possibility of voids in the passivation which could later lead to interconductor shorting. One concern indicated by the cross section (Figure IV-7) is the lack of Poly 2 overlap of Poly 1 for the shift register electrodes. This lack of overlap is probably the cause for the previous rejection of the CCD during wafer tests. It is not representative of CCD121H CCDs. The cross section shows good overlap on one side and minimal to no overlap on the opposite side. This raises the possibility for trapping wells to occur in these areas. All devices used for evaluation of physical construction were mechanical samples which had failed electrical die probe. This was necessitated by the cost of electrically good chips. Examination of the aluminum to polysilicon contact via's showed that all aluminum to Poly 1 and Poly 2 interconnections were made through a Poly 3 layer.

3. Scanning Electron Microscope Examination.

Scanning Electron Microscope (SEM) examination of the Fairchild CCD121H was performed with a Cambridge S-180 SEM. The integrity of the first level metallization and the polycrystalline silicon was judged utilizing MIL-STD-883B, Method 201E, as the criteria. The various layers were selectively removed with as little damage to



Figure IV-8 Photograph showing the shift register electrodes leaving the surface. This area is beyond the active shift register region. Mag. 1200X



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Figure IV-9 Photograph showing the transfer gate (Poly 3) to aluminum (ØX Buss) interconnection. Mag. 1200X

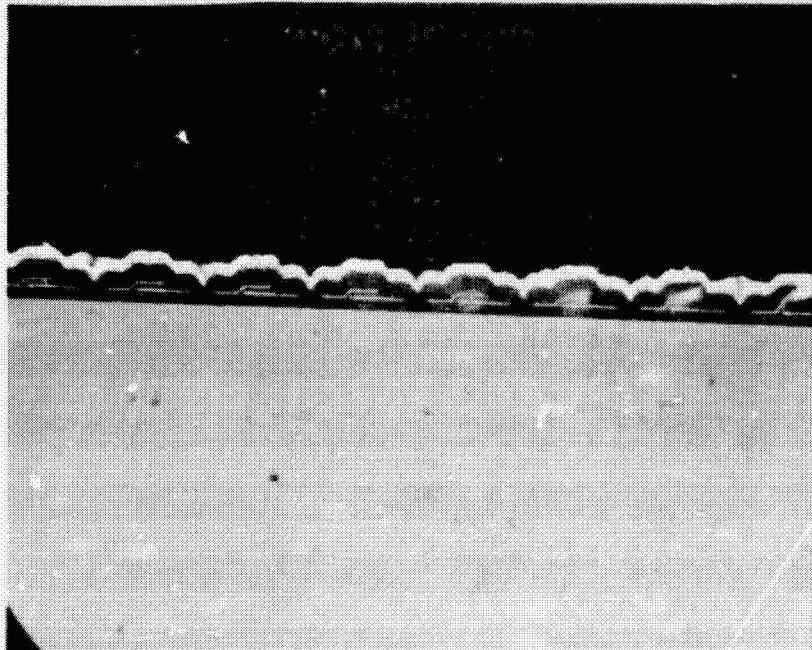


Figure IV-10 Photograph showing the transition of Poly 2 moving top of Poly 1. Mag. 1200X

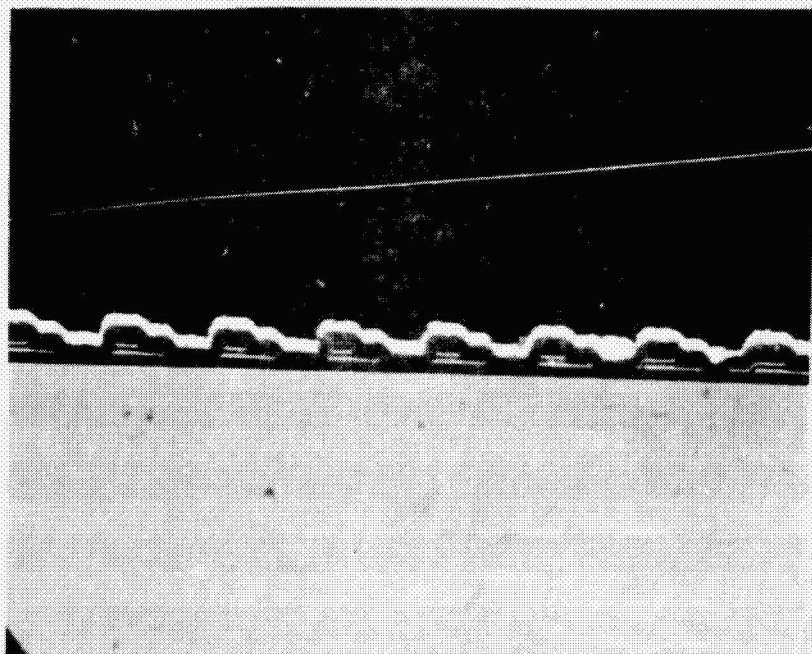


Figure IV-11 Photograph showing Poly 2 laying on top of Poly 1. Mag 1200X

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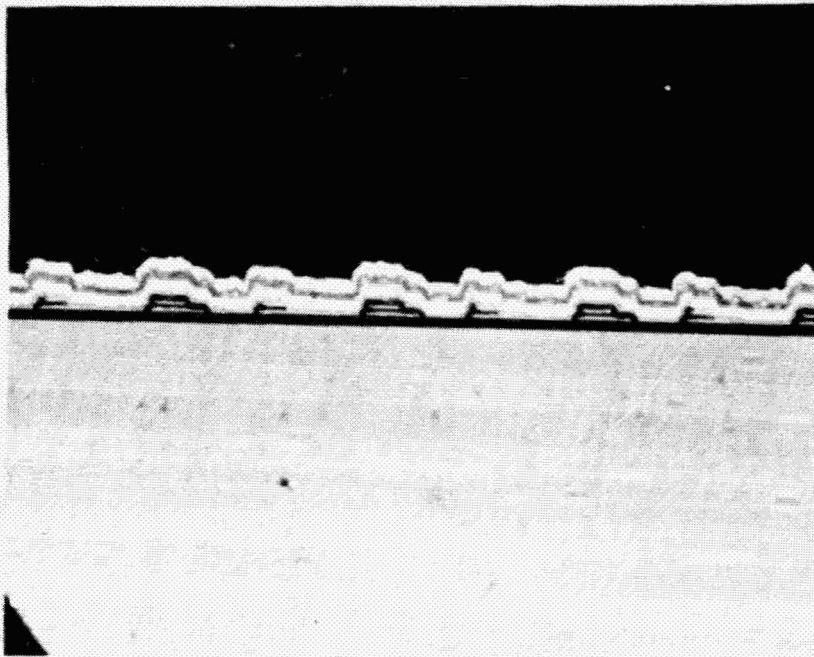
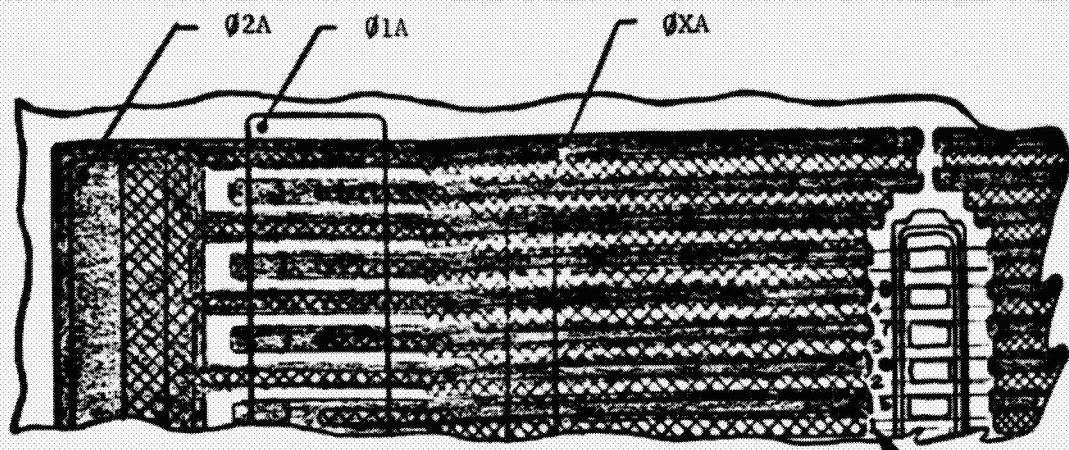
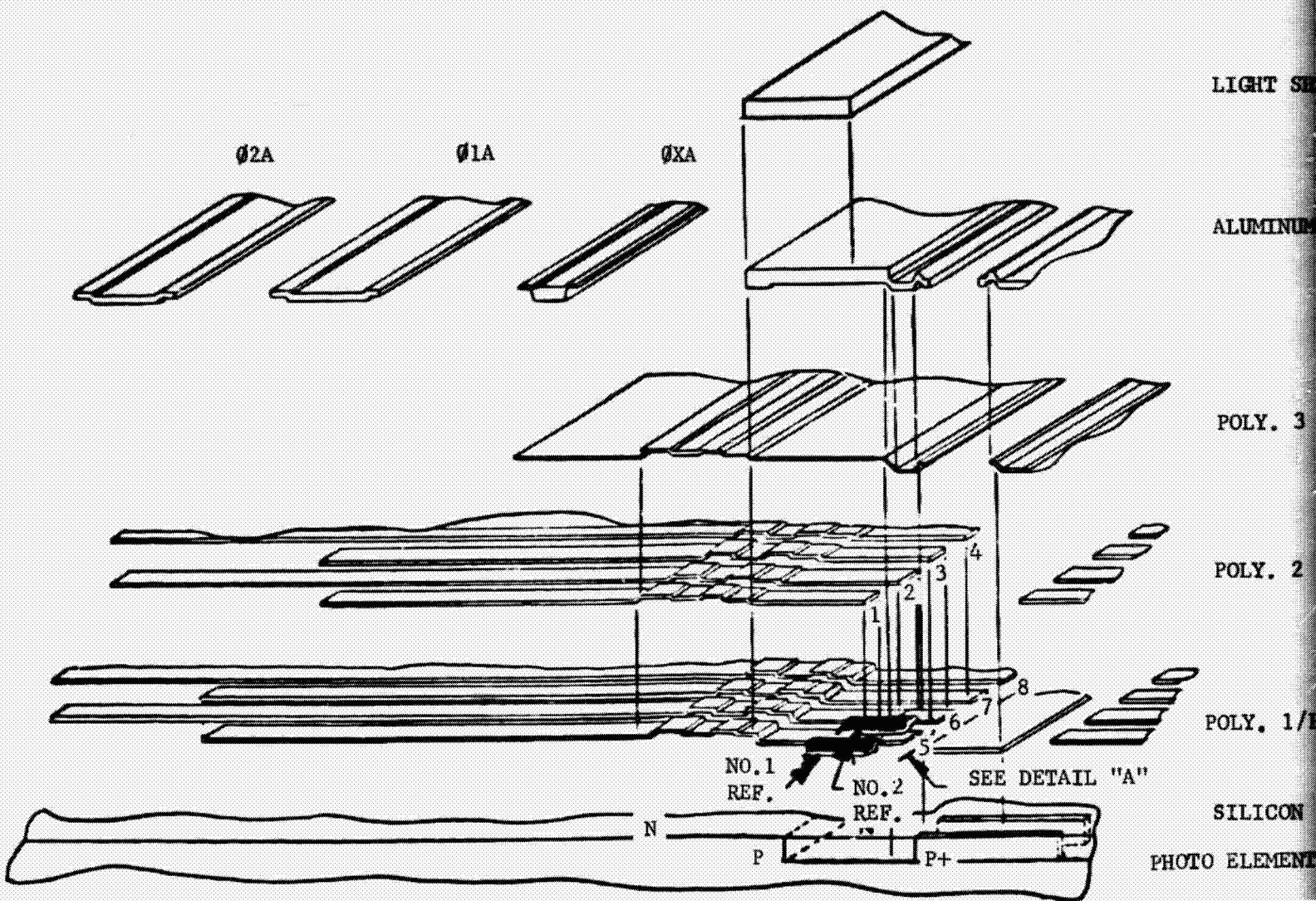


Figure IV-12 Photograph showing aluminum (\emptyset 1) to Poly 3 and alternate pairs of poly 1 & 2. Mag. 1200X

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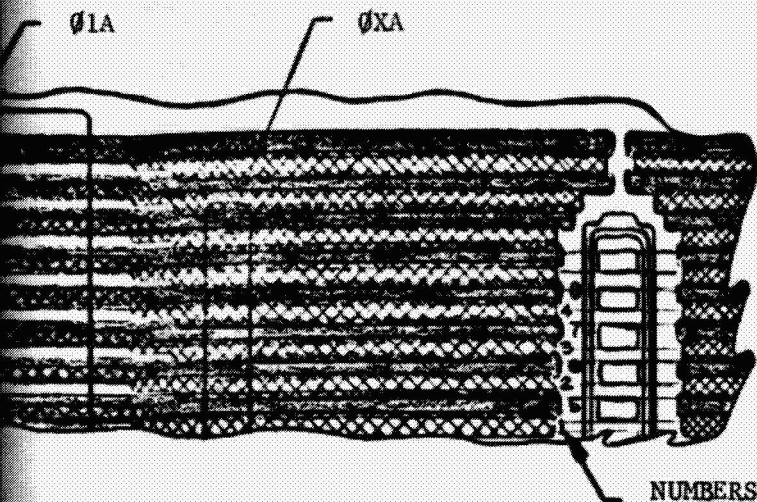


NUMBERS SHOWN
REF. ONLY
(1-4) POLY. LA
(5-8) POLY. LA





NO. 1
REF.
NO. 2
REF.
SEE DETAIL "A"

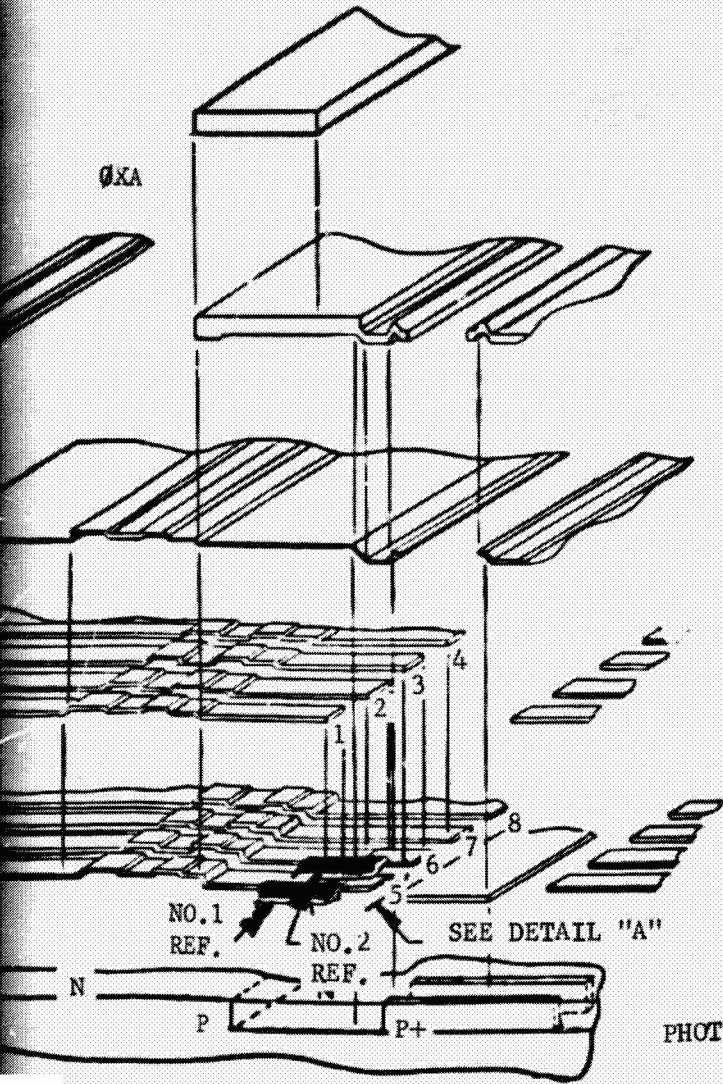
FRAME



NOTES:

1.  1ST LEVEL (POLY.1)
2.  2ND LEVEL (POLY.2)
3. LAYERS ARE ISOLATED BY AN OXIDE FILM LAYER (TYP.)

NUMBERS SHOWN FOR REF. ONLY
 (1-4) POLY. LAYER 2
 (5-8) POLY. LAYER 1



LIGHT SHIELD

ALUMINUM

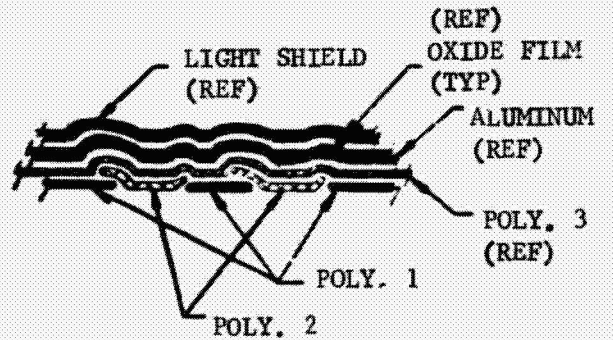
POLY. 3

POLY. 2

POLY. 1/PHOTOGATE




SILICON

PHOTO ELEMENT/TRANSFERGATE/SHIFT REGISTER DIFFUSION



DETAIL A

SCALE: NONE

-  POLY. 1
-  POLY. 2
-  POLY. 3

OLDOUT ERASE

Figure IV-13 Exposed view of conductive layers, CCD121H

lower levels as possible. Due to the number of layers involved this examination is an integral part of a reliability assessment for this device. The layers examined in order are:

- a) Light Shield (second level metallization);
- b) CVD Passivation;
- c) First Level Metallization;
- d) CVD Passivation; and,
- e) Three Polycrystalline Silicon Layers.

The integrity of the layers, the interconnections between layers, the possibility of electrical shorts between layers and other reliability considerations will be discussed.

The entire die surface, with the exception of the photogate area and the bond pads are covered with an aluminum light shield. The purpose of the shield is to prevent incident light from reaching the die surface and creating unwanted light signal indications. The critical area of coverage is the shift register region between the ring diode and the photogate. This criticality is minimized since first level metallization also covers this region.

The shield metallization is normally connected to V_{SS} . If shorts occur to other points, electrical failure can result. Shorts could occur to the bond pads if metal is smeared across the 0.5 mil passivation around the pad or if a bond is poorly placed (Figure IV-14 and Figure IV-15). Shorts can be produced through the passivation by mechanical damage in other areas of the chip. The CVD passivation is relatively brittle and can be cracked; therefore, more care needs to be exercised in handling these parts than devices without light shields.

Pitting of the shield metallization was found in many areas (Figures IV-16, IV-17). This is primarily due to the photoresist not adequately protecting these areas during light shield removal in the photogate and bond pad areas. The continuity of the photoresist is aggravated by the unusual variation in surface topograph created by the five layer conductor system (Figure IV-18). This in itself is not a reliability concern; however, following the selective metallization etch the CVD passivation is removed above the bond pad and immediately over the photogate. If during this step there is coincidence between the pitted aluminum and poor photoresist coverage, the CVD passivation in these areas will be etched. This could leave a possible path for a short to occur between conductor and the shield metallization. For a short to occur an external conductive contaminant would be required and is therefore not believed to be a serious reliability risk. It does indicate a need for better photoresist coverage.

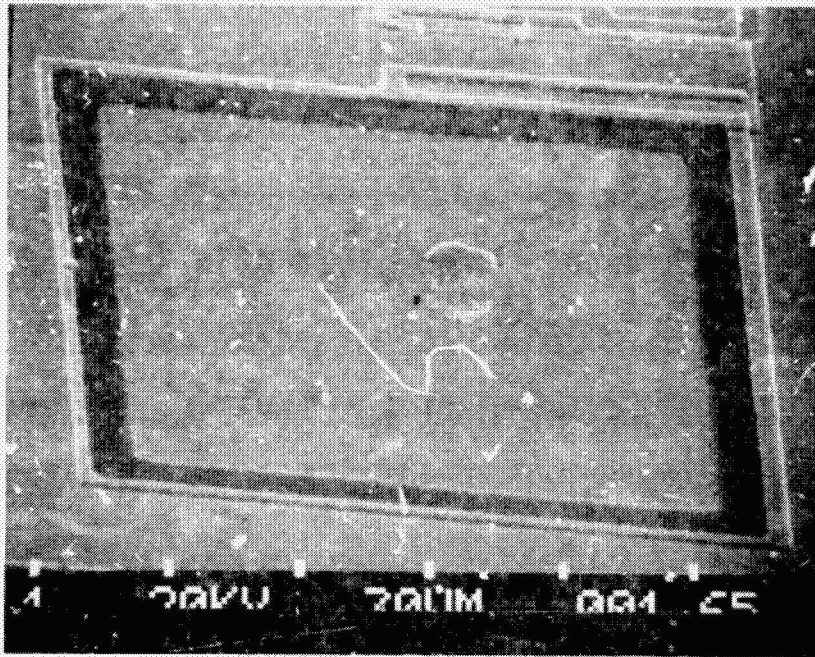


Figure IV-14 Micrograph showing bond pad. Mag. 600X



Figure IV-15 Micrograph showing CVD glass between bond pad and shield metalization. Mag. 6300X

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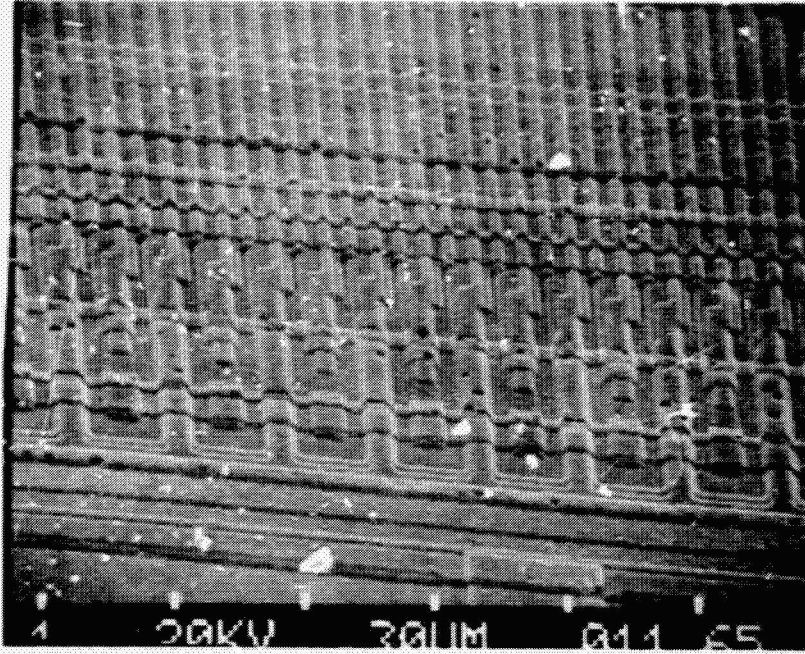


Figure IV-16 Micrograph showing pitting of shield metalization.
Mag. 630X

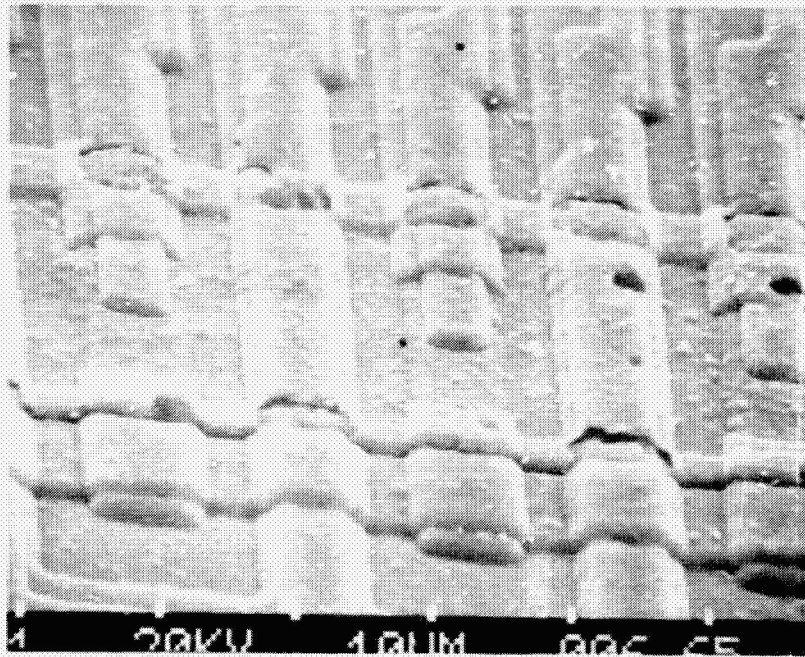


Figure IV-17 Micrograph showing pitting of shield metalization.
Mag. 2000X

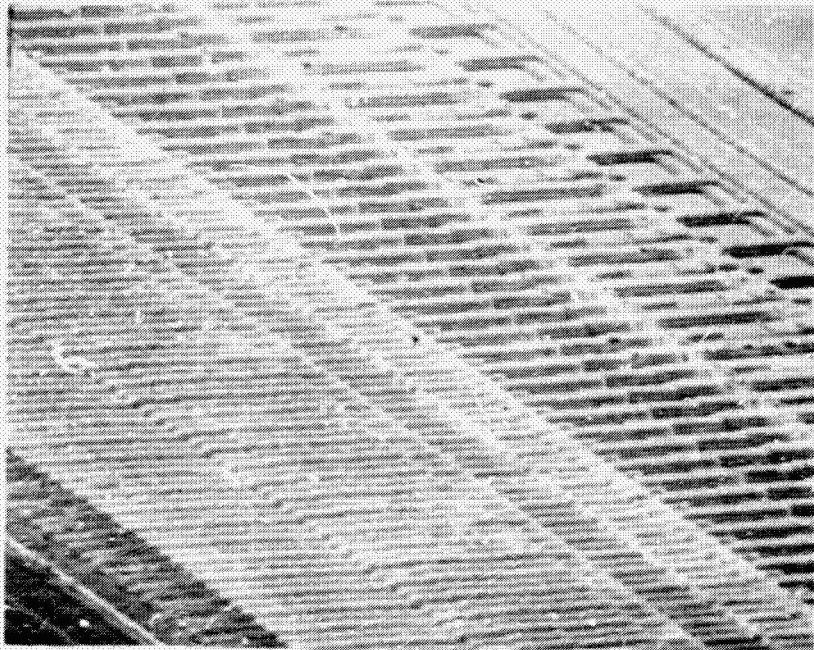


Figure IV-18 Micrograph showing surface topography. Mag. 730X

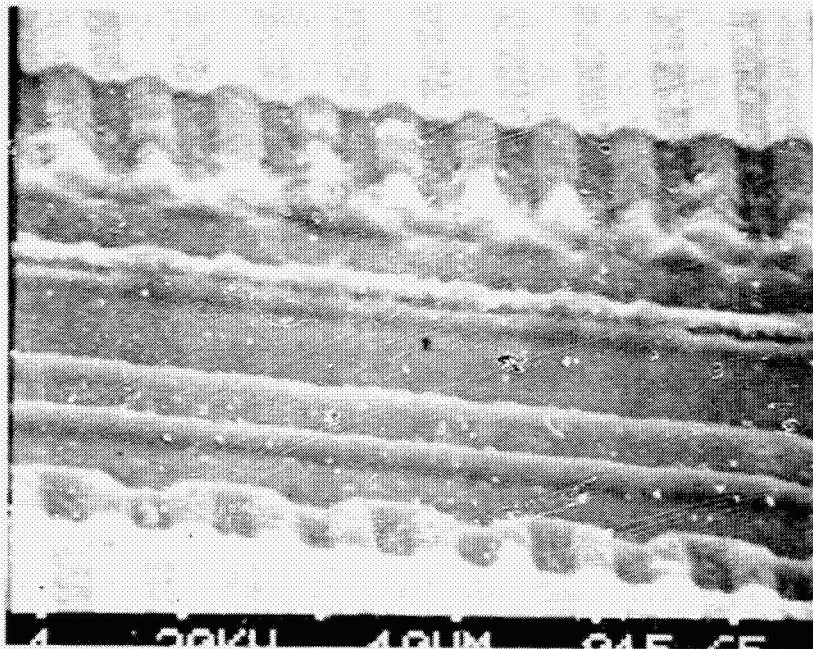


Figure IV-19 Micrograph showing etching of CVD passivation adjacent to photo gate. Mag. 2000X

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During this CVD passivation etch the area between the photogate and the edge of the shield metallization is also being etched in several areas (Figure IV-19). This does not represent a reliability risk but is another indication of an inadequate photoresist process for a device with this amount of surface variation.

To facilitate further examination of the CVD passivation layer the shield metallization was removed using aluminum etchant. There was evidence of pitting of the passivation layer due to the reasons noted above (Figures IV-20, IV-21). The pitted areas in the passivation adjacent to the photogate were more evident due to the etching of the exposed first level metallization (Figure IV-21).

The passivation was then removed using a plasma stripper and fluorocarbon gas. This method allows removal of the passivation without causing further damage to the first level metal. Examination of the first level metal found one metallization stripe, ϕR , to be unacceptable (Figure IV-22). The area appears to have been etched and it is likely that the line was acceptable prior to stripping the shield metallization. The general metallization was adequate (Figures IV-23 through IV-26). The largest step located on the CCD was the ring diode contact (Figures IV-25, IV-26). As can be seen there was adequate coverage. Figure IV-27 shows an aluminum to Poly 3 contact on transistor Q10 drain to V_{SS} . The Poly 3 is then in direct contact with the Poly 1 layer. Figure IV-28 shows an input protect circuit with a series Poly 3 resistor and diode to substrate. The interconnections made on this device are aluminum to Poly 3 and silicon, Poly 3 to Poly 2 and Poly 1 and Poly 2 to Poly 1. There is no electrical contact between the aluminum and Poly 2 or Poly 1. No evidence of adhesion or contact problems were visible.

The first level aluminum was next stripped with aluminum etchant and the die surface re-examined on the SEM. The CVD passivation layer appeared adequate. The first level metal does not cross Poly 1 or Poly 2 except where contact is made to it through Poly 3 and over the Poly 1 V_{SS} line in the output amplifier. Beneath the remainder of the areas where there is first level metal there is CVD passivation and thermal oxide. This makes the possibility of a short remote.

The CVD passivation layer was then stripped with siloxide etchant and the polycrystalline silicon layers examined. All poly layer step coverages were excellent (Figures IV-29 through IV-36). Poly 3 step coverage is shown in Figures IV-29 through IV-31; Poly 2 coverage is shown in Figures IV-32 through IV-34 and Poly 1 coverage is shown in Figures IV-35, IV-36. Figures IV-31 and IV-36 are Poly 3 and Poly 1 over the same step in the output amplifier. The polycrystalline silicon layers are approximately 0.5 μm thick and quite uniform. Poly 1 and Poly 2 layers are oxidized during processing which provides good dielectric isolation between layers and should prevent shorts. No indication of inadequate isolation was seen.

SEM examination found only one condition which might be a reliability concern. This is the pitting in the shield metallization and the CVD

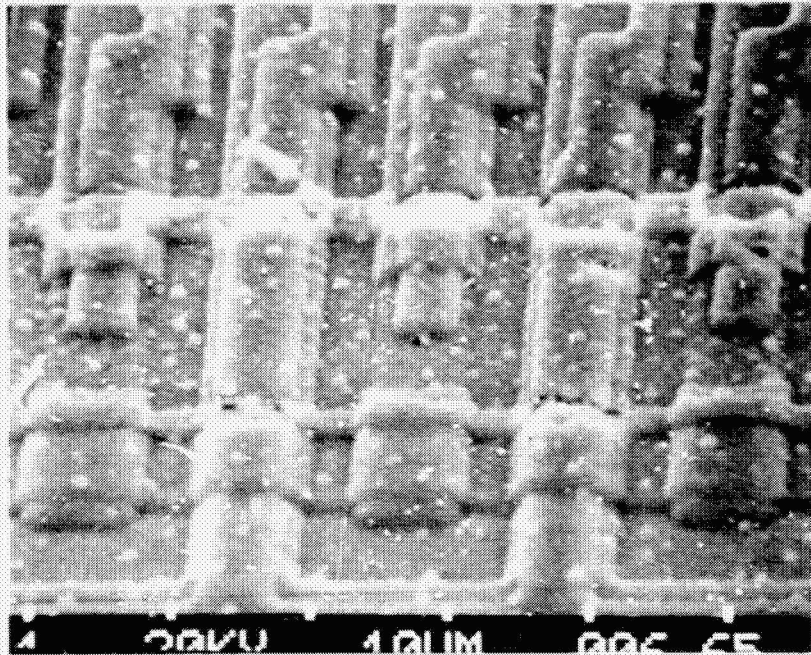


Figure IV-20 Micrograph showing pitting of the passivation layer beneath the metallization. Mag. 2000X

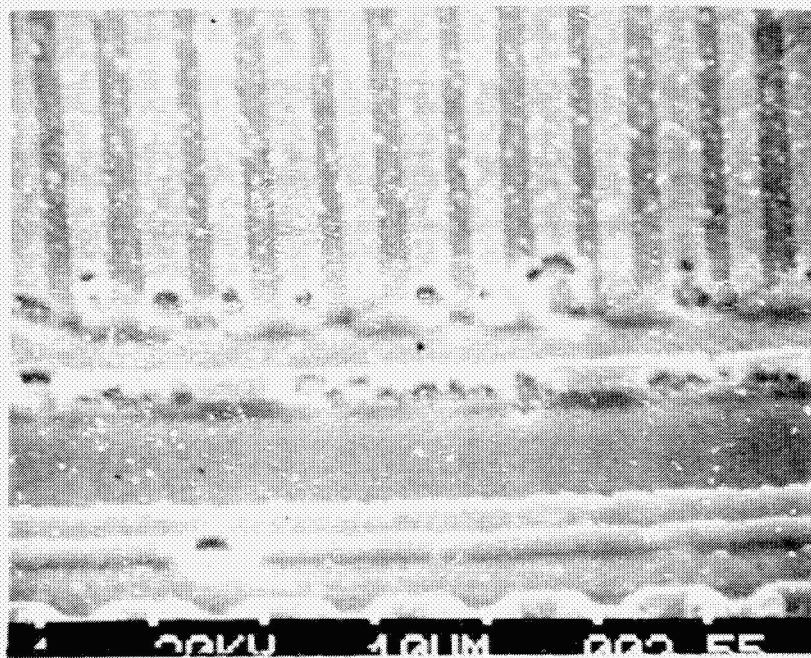


Figure IV-21 Micrograph with passivation pitting adjacent to the photogate evident. Mag. 1600X

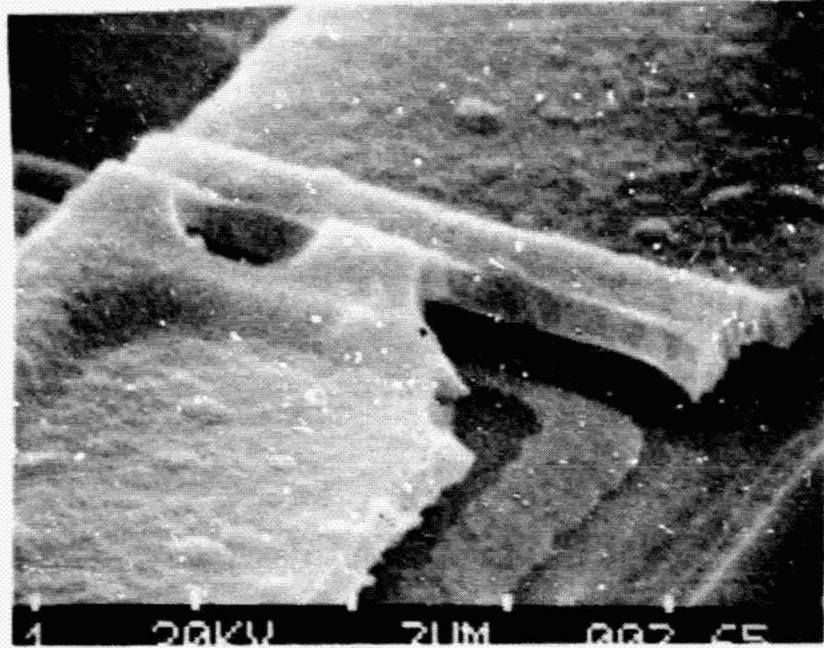


Figure IV-22 Micrograph showing unacceptable metalization stripe on ØR. Mag. 7500X

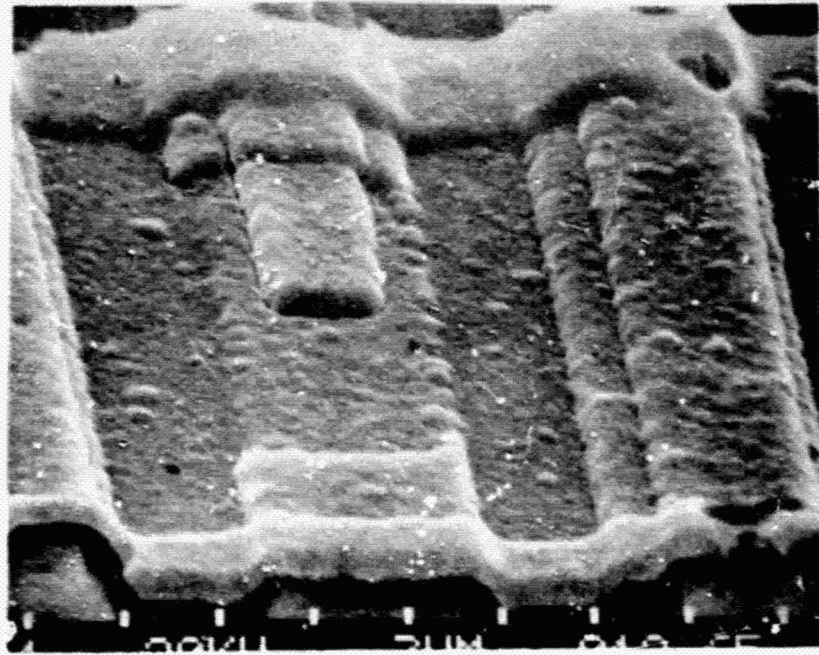


Figure IV-23 Micrograph showing Ø 1 metalization coverage. Mag. 4500X

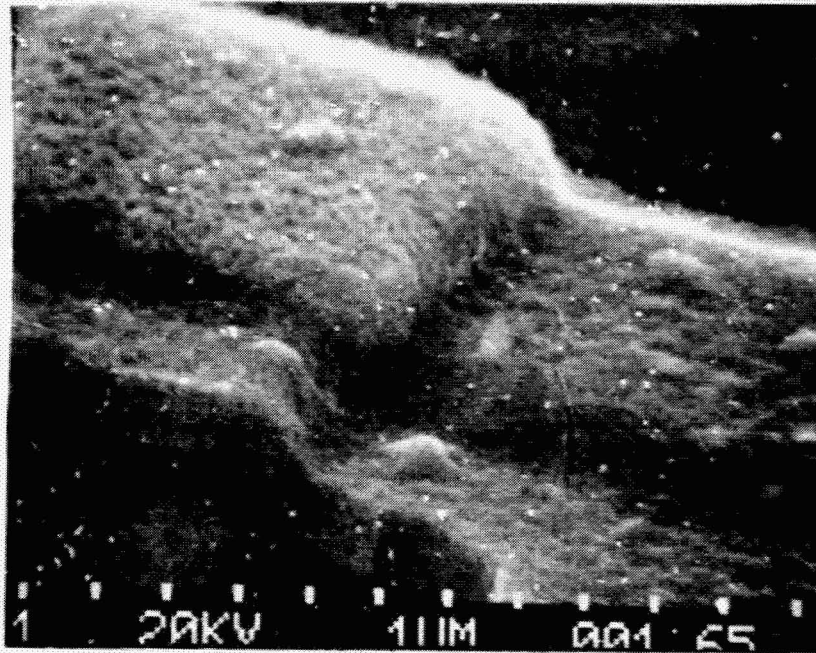


Figure IV-24 Micrograph showing output amplifier step coverage.
Mag. 10,000X

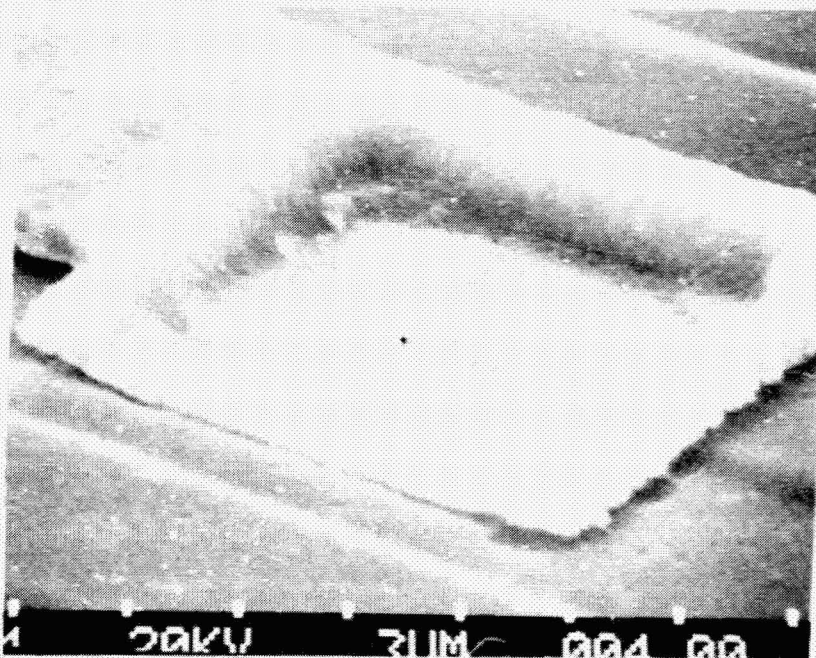


Figure IV-25 Micrograph showing ring diode contact window.
Mag. 5200X

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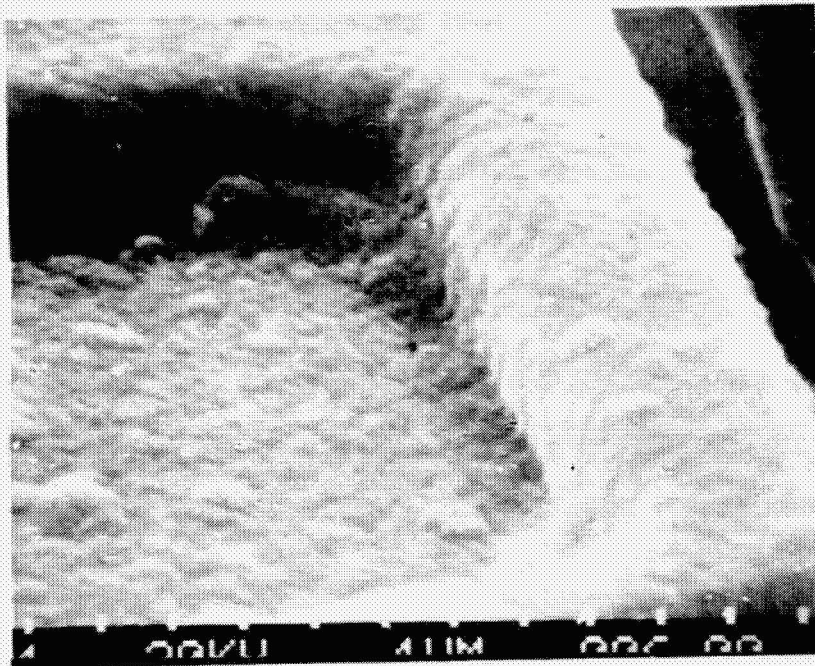


Figure IV-26 Micrograph showing ring diode contact window step coverage. Mag. 10,000X

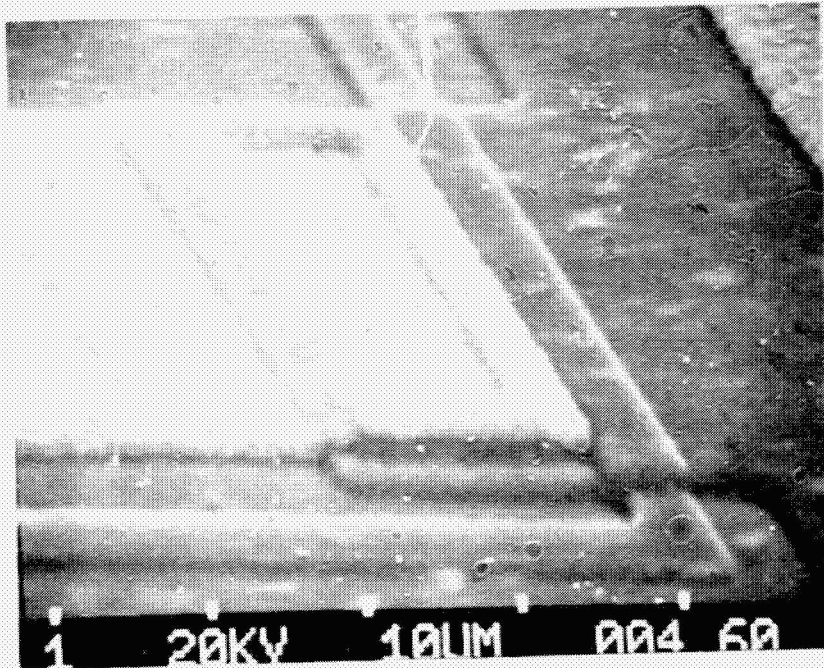


Figure IV-27 Micrograph of aluminum to Poly 3 to Poly 1 contact in output amplifier. Mag 2200X

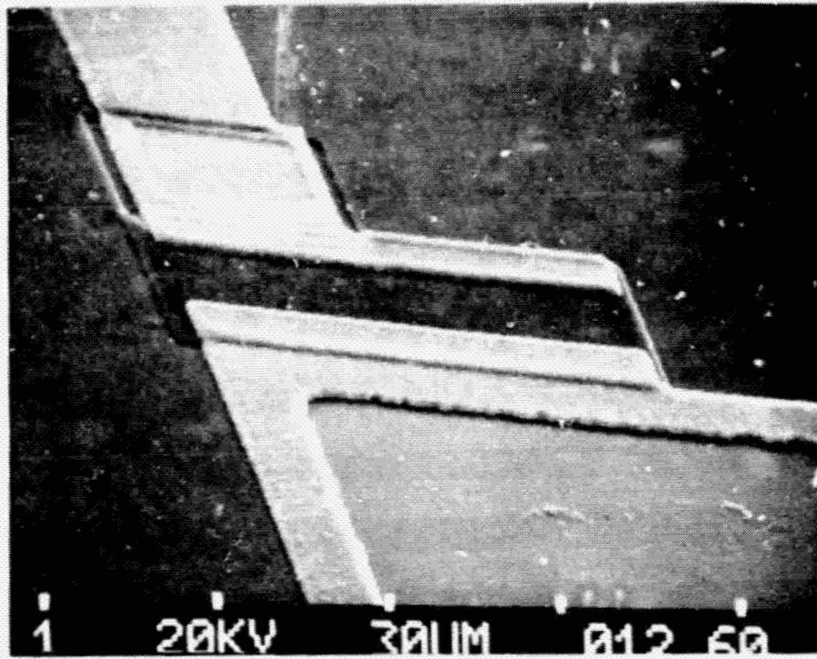


Figure IV-28 Micrograph of input protect resistor and diode contact. Mag. 800X

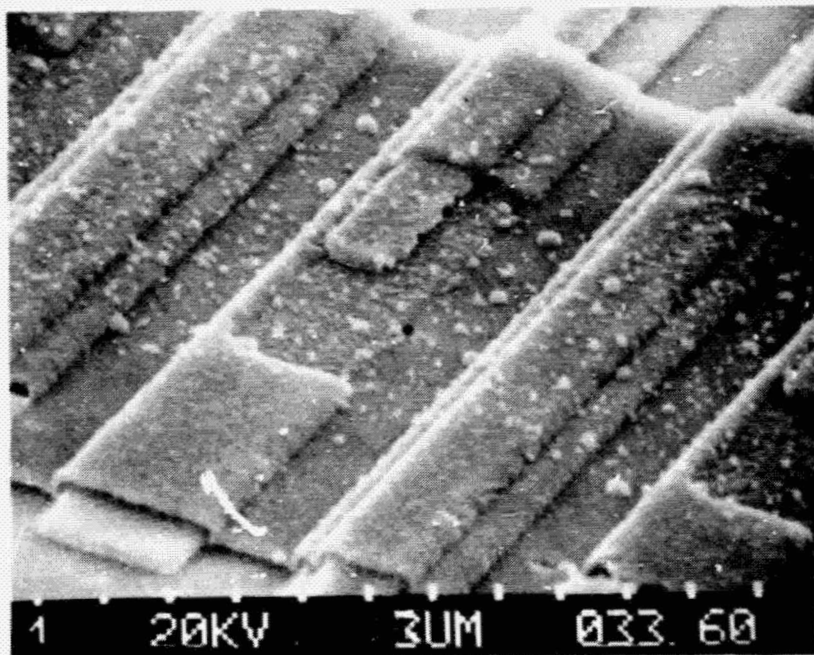


Figure IV-29 Micrograph of Poly 3 step coverage. Mag. 3200X

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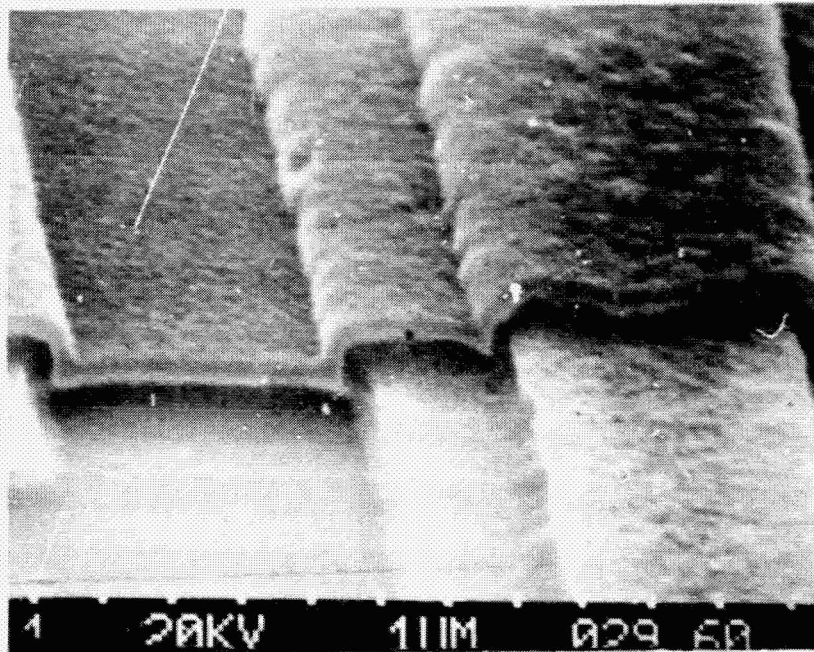


Figure IV-30 Micrograph of Poly 3 step coverage. Mag. 10,000X

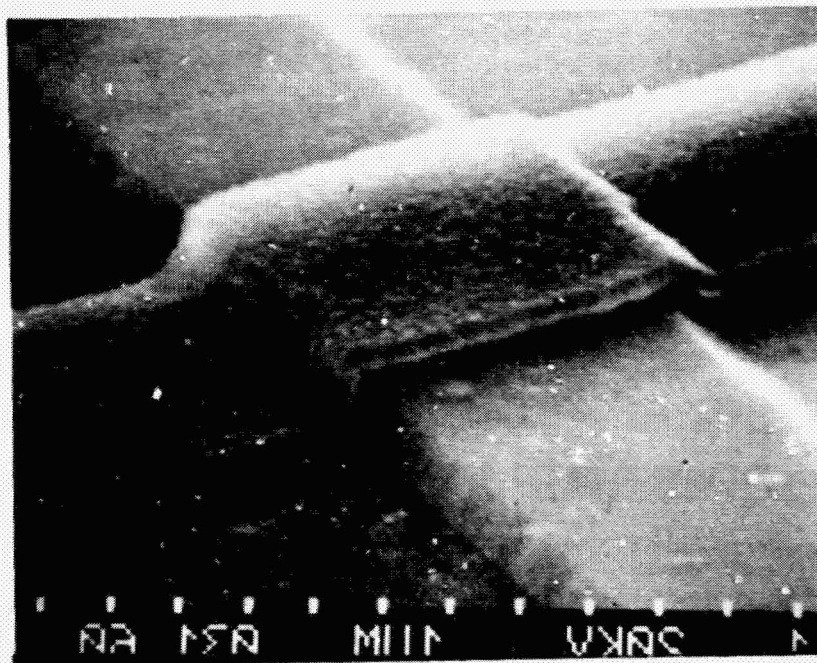


Figure IV-31 Micrograph of Poly 3 step coverage in output amplifier. Mag. 10,000X

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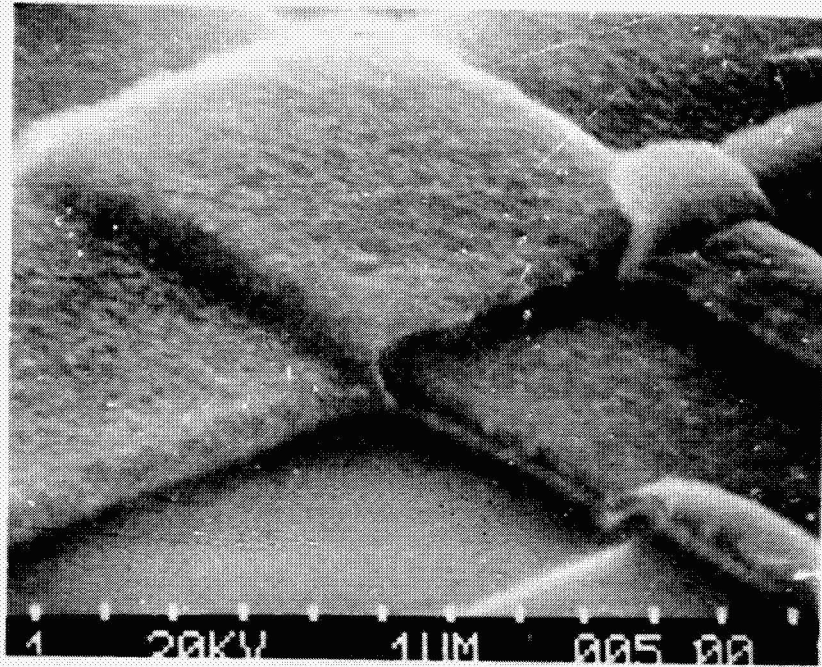


Figure IV-32 Micrograph of Poly 2 step coverage over Poly 1. Mag. 10,000X

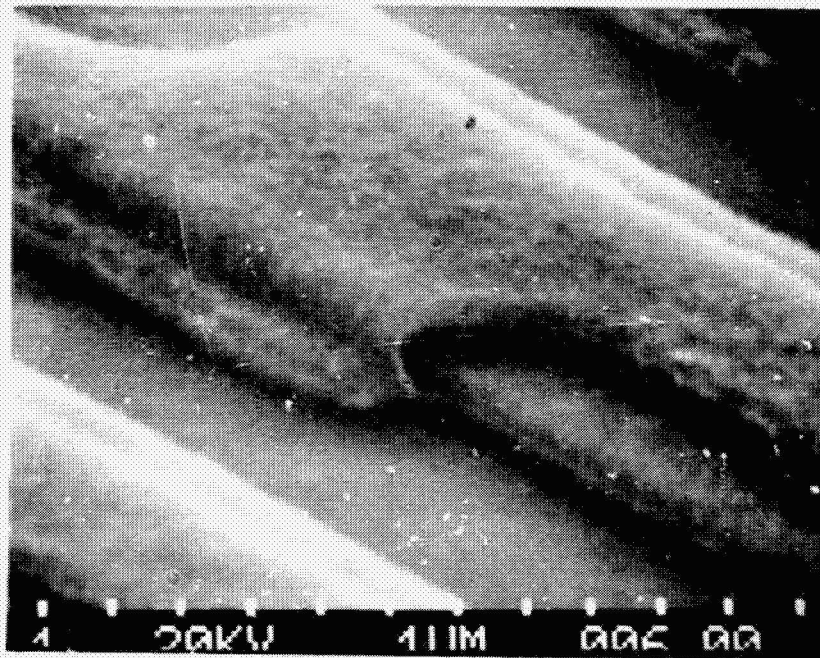


Figure IV-33 Micrograph of Poly 2 over Poly 1. Mag. 10,000X

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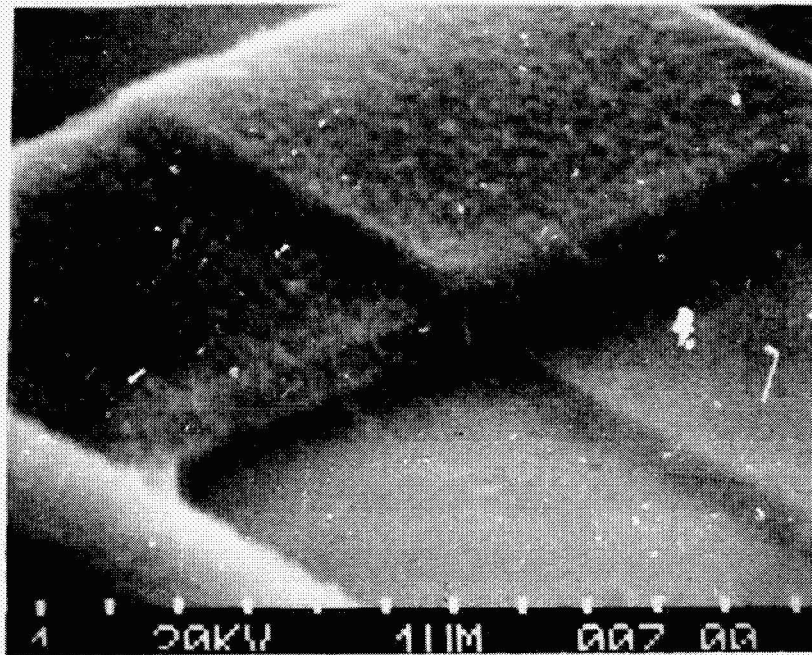


Figure IV-34 Micrograph of Poly 2 step coverage. Mag. 10,000X

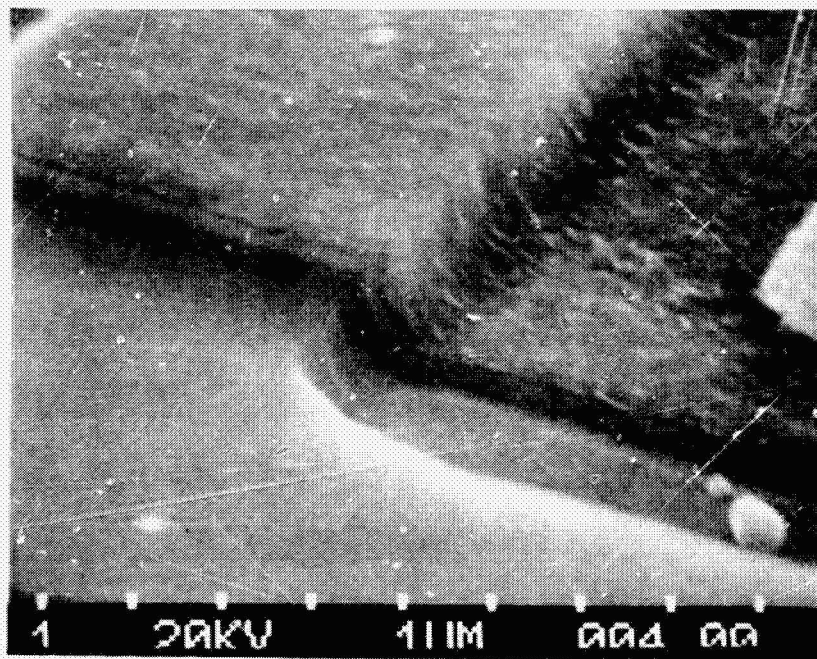


Figure IV-35 Micrograph of Poly 1 step coverage. Mag. 13,000X

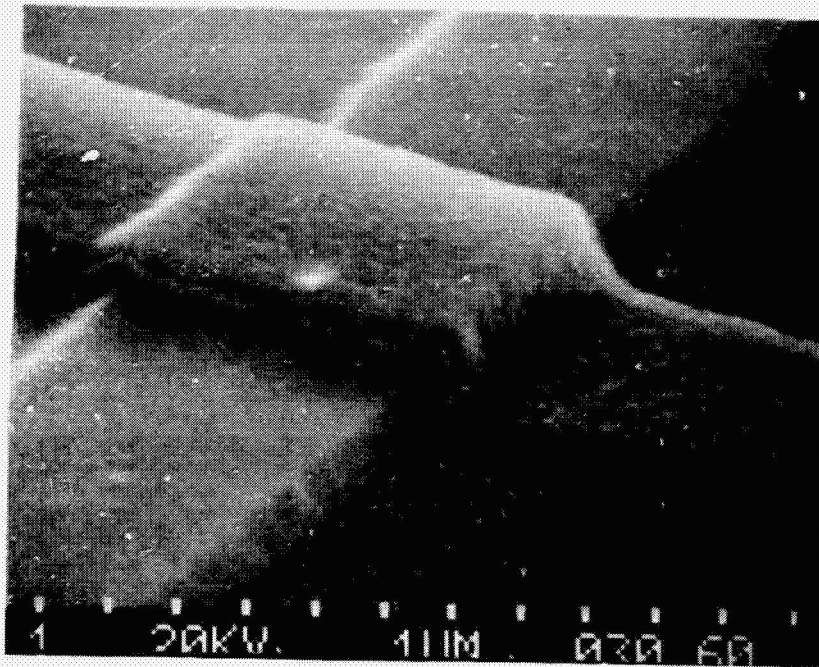


Figure IV-36 Micrograph of Poly 1 step coverage in output section. Mag. 10,000X

passivation caused by inadequate photoresist coverage. This is a processing problem and not a generic part problem.

The aluminum step coverage was good and the polysilicon layers were very uniform and provided good coverage. There were no visible problems with the interconnections between the layers. Care does need to be taken during the handling and bonding of parts with second level metallization to avoid shorts.

4. Diffusions.

The Fairchild CCD121H was microsectioned and stained to identify and characterize the different diffusions. These diffusions were:

- a) N+ Ring Diode;
- b) P+ for isolating the photo elements, and transfer gates, providing lateral confinement of the shift register, isolating the output amplifier sections and for all areas outside of the ring diode;
- c) N ion-implant for the photo elements, transfer gates and shift register; and,
- d) N+ source and drain diffusion.

The starting material is p-type silicon. A deep (approximately 3.5 μm) N+ diffusion is then made which surrounds all of the active areas on the chip (Figures IV-37 through IV-39). This is the ring diode.

The next diffusion is a P+ diffusion approximately 1.6 μm deep. This diffusion is in all areas outside of the ring diode except for the input protect diodes. In addition, this diffusion provides isolation between the photo elements and transfer gates, separates the shift register and the ring diode, surrounds the output amplifier sections and separates transistors in the output section (Figures IV-40 through IV-43).

Ion-implantation is used to make shallow (approximately 0.4 μm) N-type diffusion. The photo elements, transfer gate, shift register, and output amplifier diffusions are generated in this step (Figure IV-39, IV-44).

The final diffusion is N+ approximately 1.1 μm deep. This step uses the polysilicon gates for masking and produces the sources and drains (Figures IV-41, IV-45, IV-46).

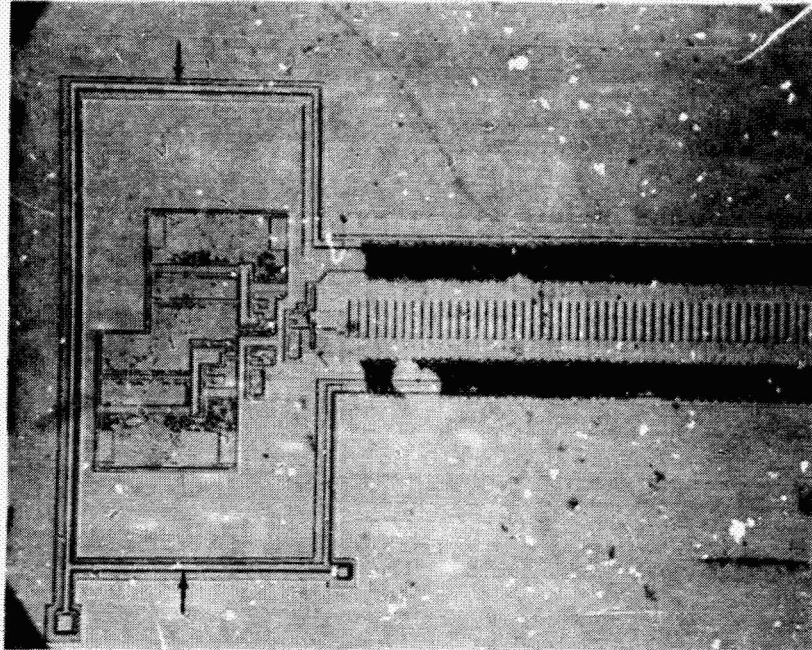


Figure IV-37 Photograph showing ring diode diffusion (at arrows) around output section. Mag. 100X

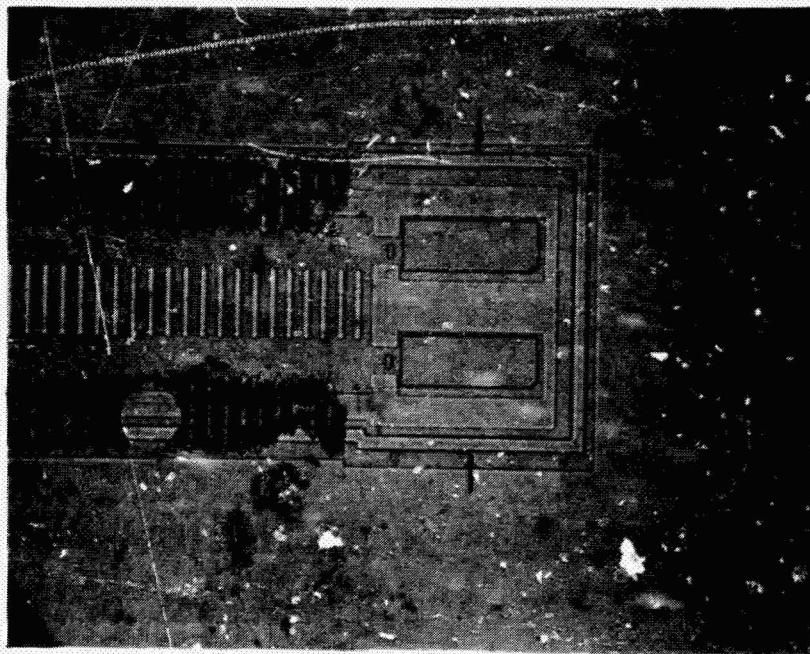


Figure IV-38 Photograph showing ring diode diffusion (at arrows) around input section. Mag. 200X

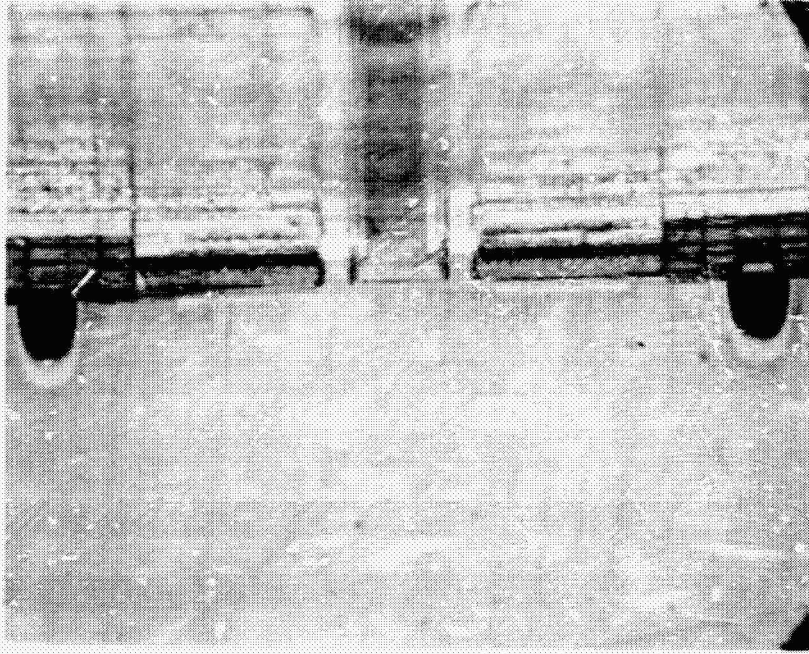


Figure IV-39 Photograph of microsection showing ring diode diffusion on outside edges and shallow shift register diffusion in outer. Mag. 500X

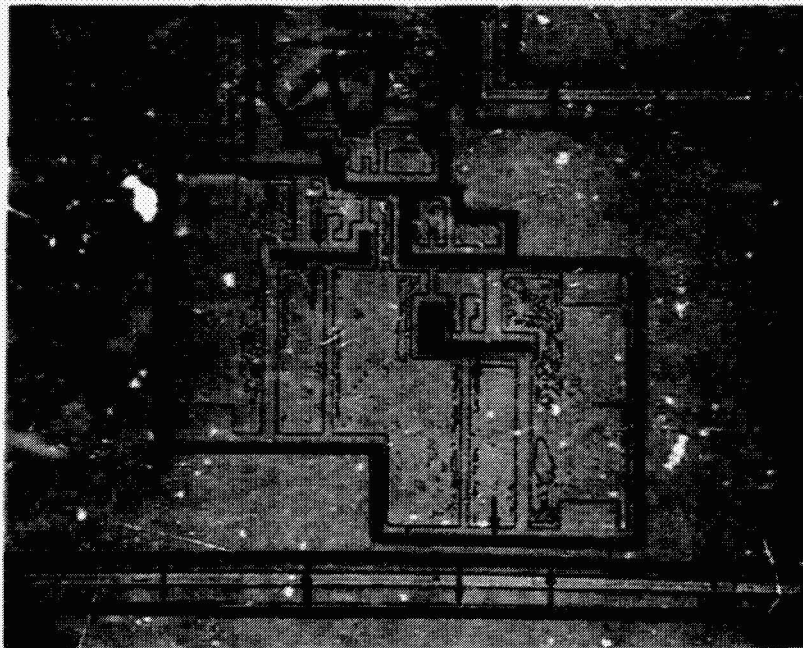


Figure IV-40 Photograph showing P+ diffusion areas at tips of arrows. Mag. 200X

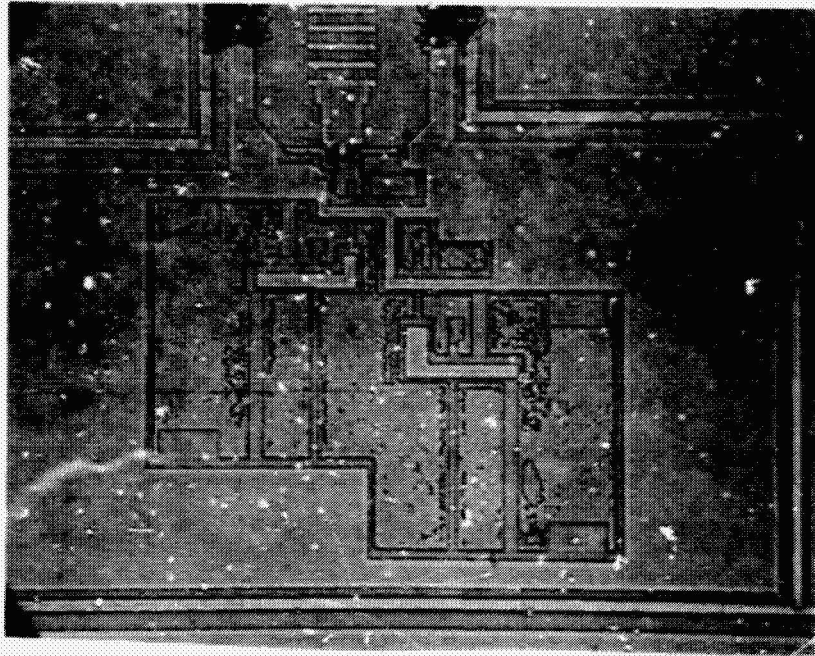


Figure IV-41 Photograph showing area as Fig. IV-40 without arrows and output section source and drain diffusion. Mag. 200X

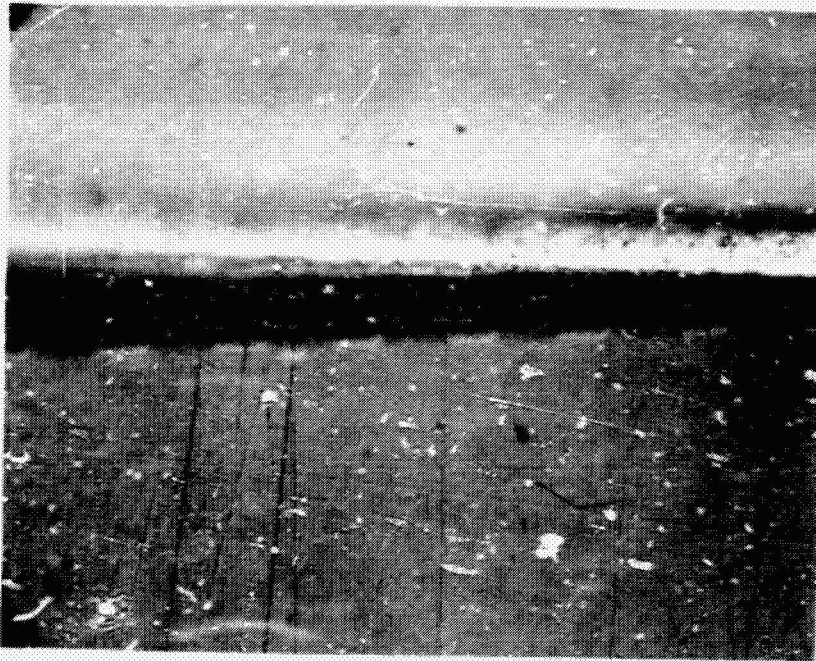


Figure IV-42 Photograph of microsection showing P+ channel stop diffusions. Mag. 1200X

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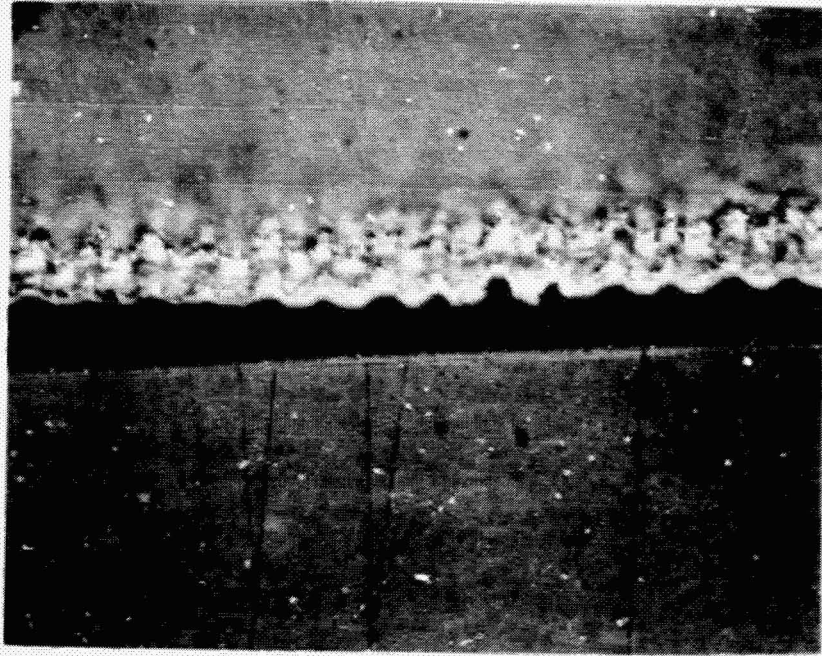


Figure IV-43 Photograph of microsection showing P+ diffusion outside of ring diode. Mag. 1200X

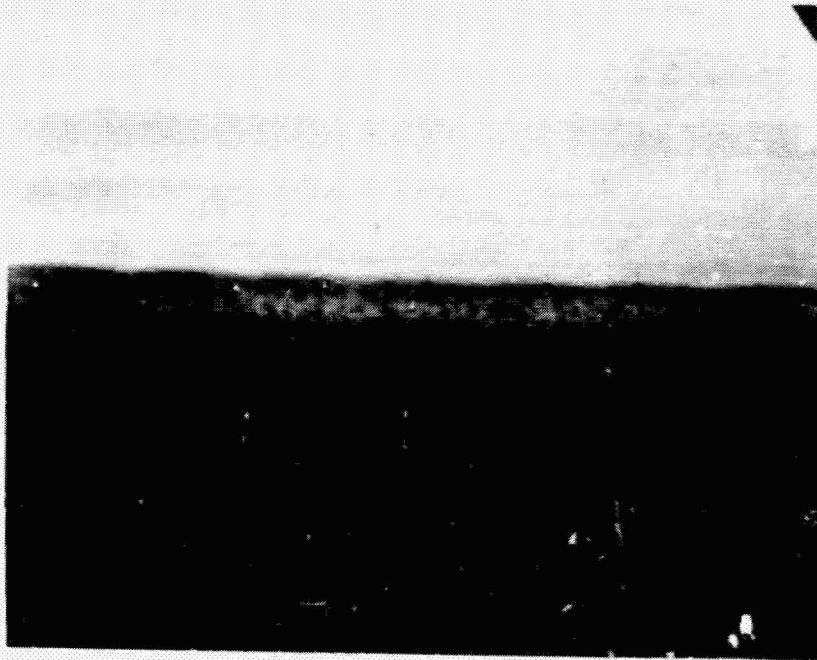


Figure IV-44 Photograph of microsection showing shallow photo element diffusion. Mag. 1200X

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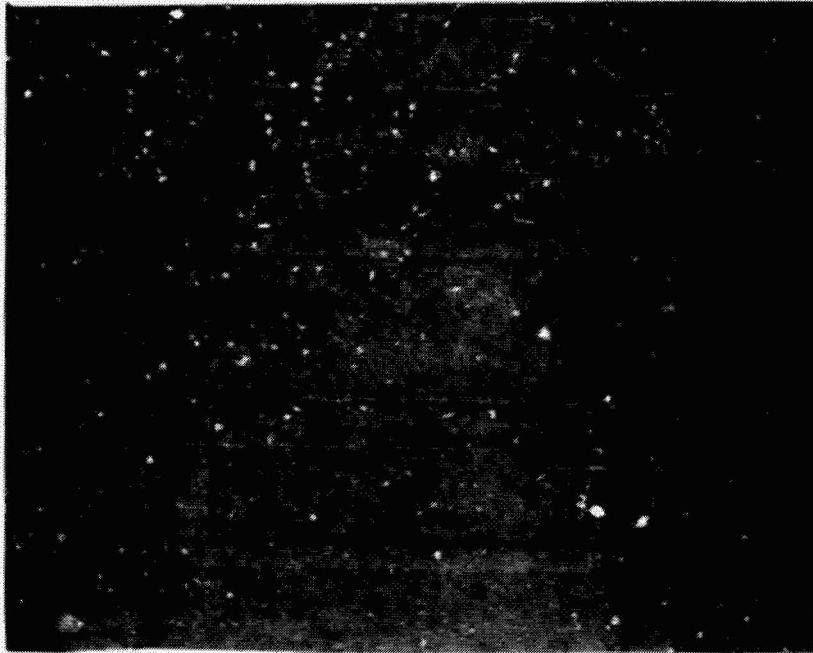


Figure IV-45 Photograph showing input section source and drain diffusions (dark outlined rectangular areas). Mag. 500X

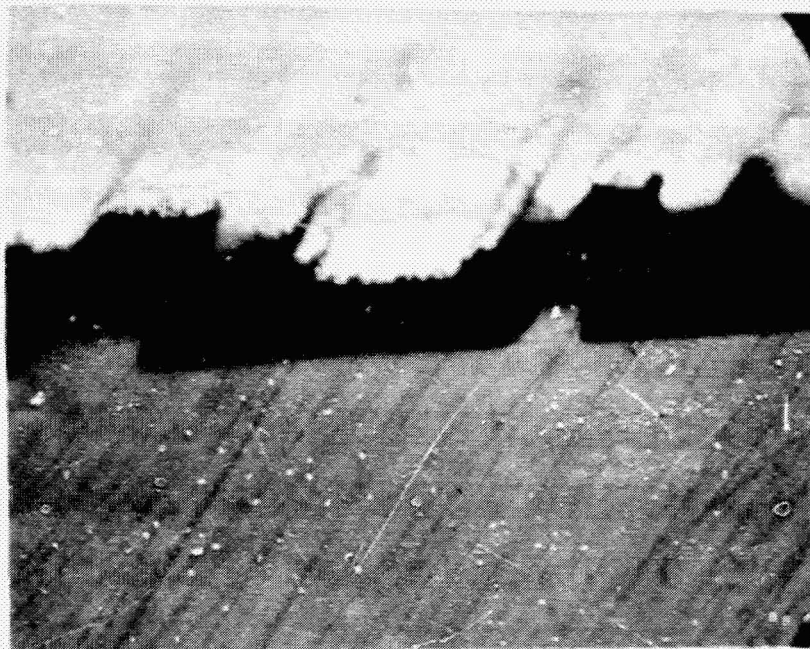


Figure IV-46 Photograph of microsection showing source and drain diffusion. Mag. 1200X

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B. ELECTRO-OPTICAL TESTS AND ANALYSIS

The electrical and optical characteristics of the Fairchild CCD121H are described in this section. Much of the data is taken from production testing records of a number of devices used on a High Reliability Program. In addition, several independent tests were performed to gather data on various parameters of interest. In order to be able to use the CCD121H for a particular application the device's performance must be understood as a function of temperature, clock frequency, and integration time. In addition, the characteristics of the electrical input and output networks should be understood.

The test conditions, unless otherwise specified, are as follows:

$V_{OD} = 15V$
 $V_{RD} = 12V$
 $V_{OG} = 5.5V$
 $V_{PG} = 8.0V$
Phase 1, 2, ϕ_{XA} , ϕ_{XB} , ϕ_R Clocks = 8V (High State)
= 0 to 0.5V (Low State)
 $t_{int} = 80 \mu\text{sec}$
 $f_{reset} = 128.6 \text{ KHz}$
TPSA,B = 10V High State; 5V Low State

OS Load: 100K ohms minimum, parallel with 30 pF maximum.

Figure IV-47 shows waveform timing both pictorially and graphically.

Pixel voltages were measured using the system shown in Figure IV-48. The OS signal is passed through an amplifier with a 2 MHz bandwidth. The waveform is then measured using a double-correlated sampling technique which removes low frequency noise and DC offset drift.

1. Responsivity

- a) **Spectral Response.** The spectral response is to a great extent a function of the polysilicon gate which covers the photosites. The silicon response characteristics of the photosites is altered by the transmission characteristics of the polysilicon gate material. Since the exact thickness and composition of this material does vary, the spectral response varies from device to device. Even devices from the same wafer, and pixel elements from the same device, can exhibit differences in spectral response. Figure IV-49 shows the average spectral response characteristics of devices from the same wafer run. The maximum variation of the individual curves are also plotted in the figure.
- b) **Absolute Responsivity.** Wide variations in voltage response to illumination have been experienced. Most values range from 80 $V/j/m^2$ to 200 $V/j/m^2$, using a 5000°K simulated source.

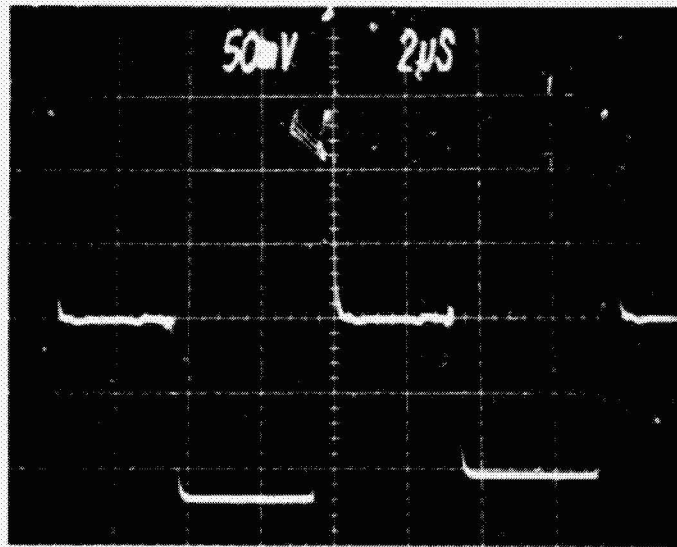
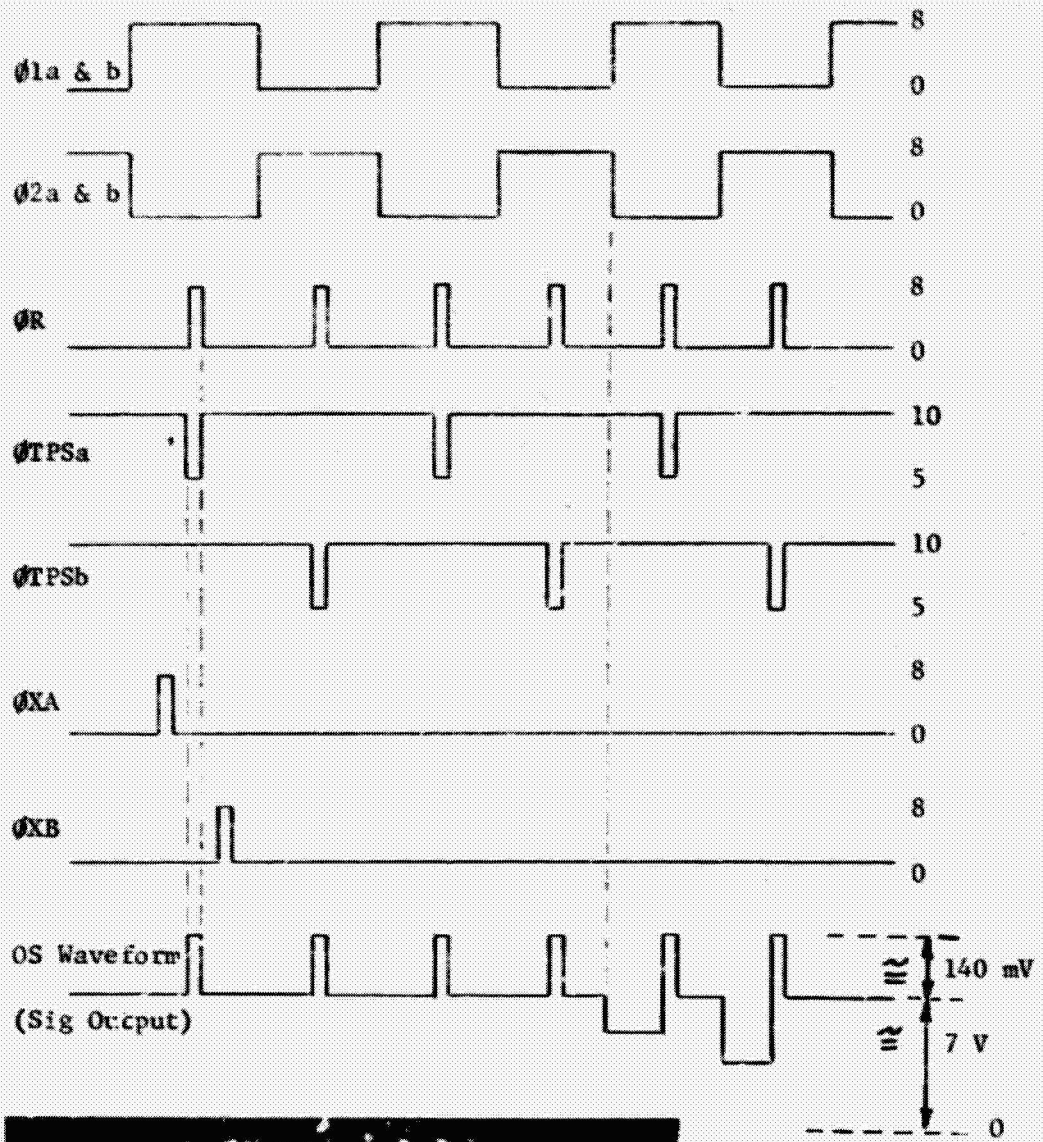
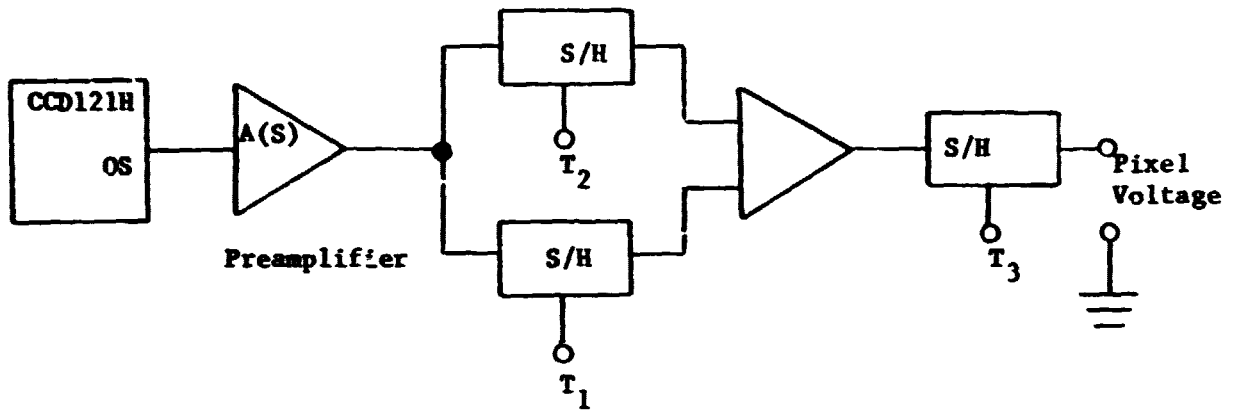


Figure IV-47 Waveform timing

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Preamplifier Characteristics:

$$A(S) = \frac{10}{1 + \frac{S}{4\pi \times 10^6}}$$

$$V_n \text{ (input noise voltage)} = 25 \text{ nV}/\sqrt{\text{Hz}}$$

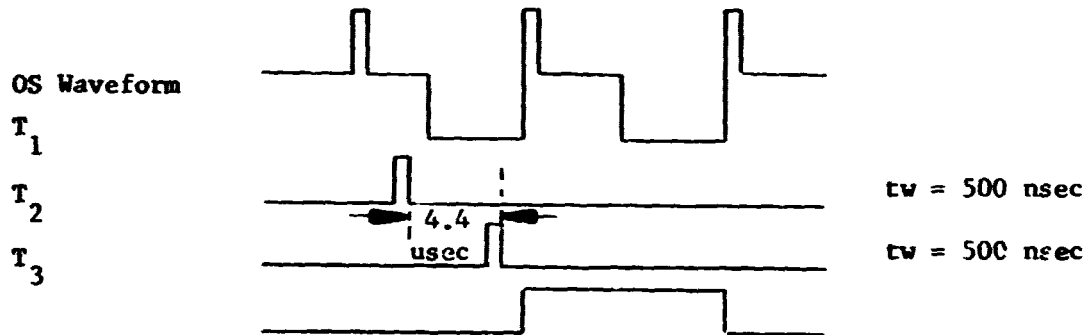


Figure IV-48 Pixel Voltage Test Circuit

REPRODUCTION PROHIBITED
EXCEPT BY AUTHORITY OF
THE QUALITY CONTROL DEPARTMENT

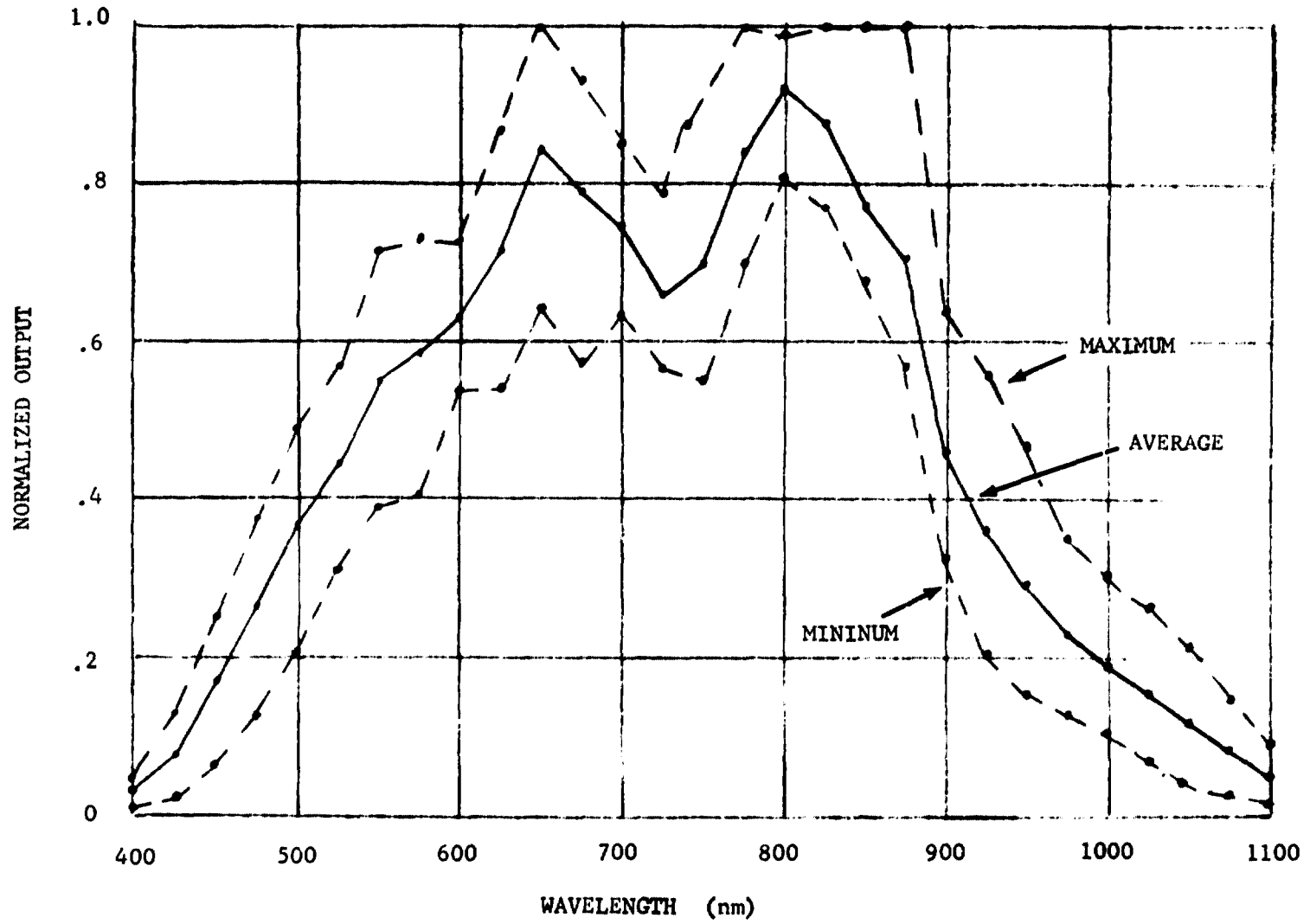


Figure IV-49 Averaged Spectral Responsivity for 6 CCD121H Devices

The responsivity was calculated over a spectral band from 400 nm to 1100 nm. Responsivity is affected somewhat by temperature. A decrease of 5% in responsivity can be expected at -10°C compared to +25°C. A number of comparison values of responsivity at +25°C and -10°C are listed.

	25°C		-10°C	
#1	123	uV/uj/m ²	115	uV/uj/m ²
#2	124	"	115	"
#3	181	"	174	"
#4	184	"	183	"
#5	115	"	106	"

- c) **Linearity.** Although all devices tested are quite linear, in general, the voltage responsivity has a voltage gamma slightly greater than unity. That is, as the illumination increases the responsivity increases. Voltage gammas of 1.03 are typical when tested to approximately 50% of saturation.
- d) **Optical Crosstalk.** Depending upon the wavelength of light striking a photosite, there is a certain amount of crosstalk to adjacent pixels. Figures IV-50, IV-51, show optical crosstalk for 5000°K broadband light and for narrow band light at .53 micrometers. At 500 nm wavelength, the crosstalk is only 3% to the adjacent pixels, and negligible to the second pixel away. At 1000 nm, however, there is 36% crosstalk to the adjacent pixel, and 1 1/2% to the fifth pixel away. Figure IV-52 plots the optical crosstalk as a function of wavelength.
- e) **Photoresponse Non-Uniformity.** The CCD121H was intended for usage in near saturation conditions for commercial applications such as facsimile page readers. The testing on this program was mostly at low light levels where uniformity of response can become a problem that requires screening of parts. A significant non-uniformity problem has been observed in a number of devices at low temperature and low light levels. When the photo current is low enough to produce less than approximately 10 mV of output (including dark signal), the uniformity of the photo response of the 1728 pixels becomes quite poor. With the photogate voltage recommended by the manufacturer of 10.25 volts, the response of the individual pixels becomes very irregular; each element responding from 0% to 200% of the average. Much improvement is seen by reducing the photogate voltage to 8.0 volts, the same voltage as the transfer clocks. At this condition, the response of an even or an odd register becomes more uniform with respect to itself, but often the average responsivity of the odd register may be substantially greater than the even register. Figure IV-53 illustrates this phenomenon by plotting the voltage response of the even and odd registers separately as a function of illumination. Figure IV-54a shows the normal oscilloscope display of the OS signal which results from a double exposure

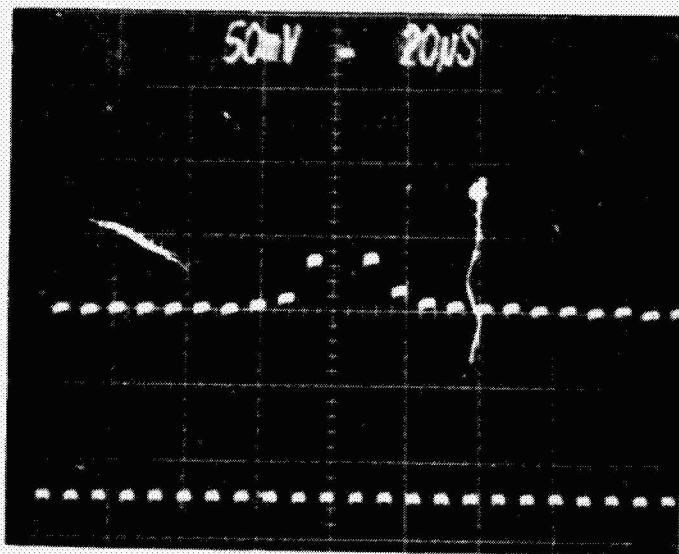


Figure IV-50 Optical Crosstalk Due to 10 μ m Diameter Spot and 5000 K Broadband Source

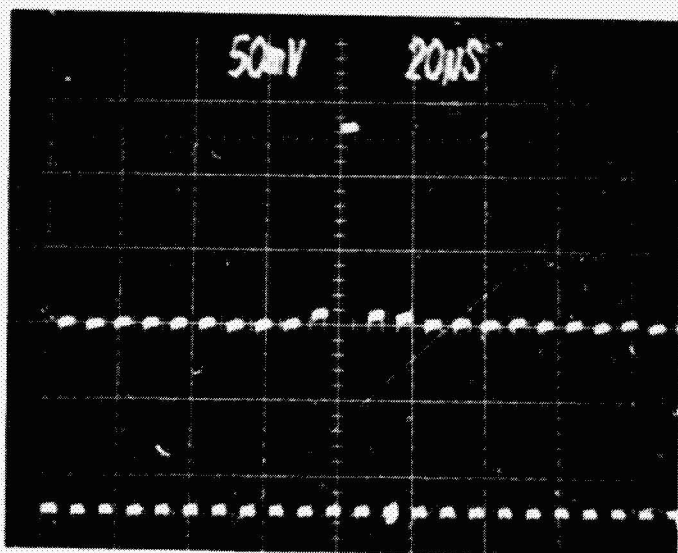


Figure IV-51 Optical Crosstalk Due to 10 μ m Diameter Spot With 0.53 μ m Narrow Band Illumination

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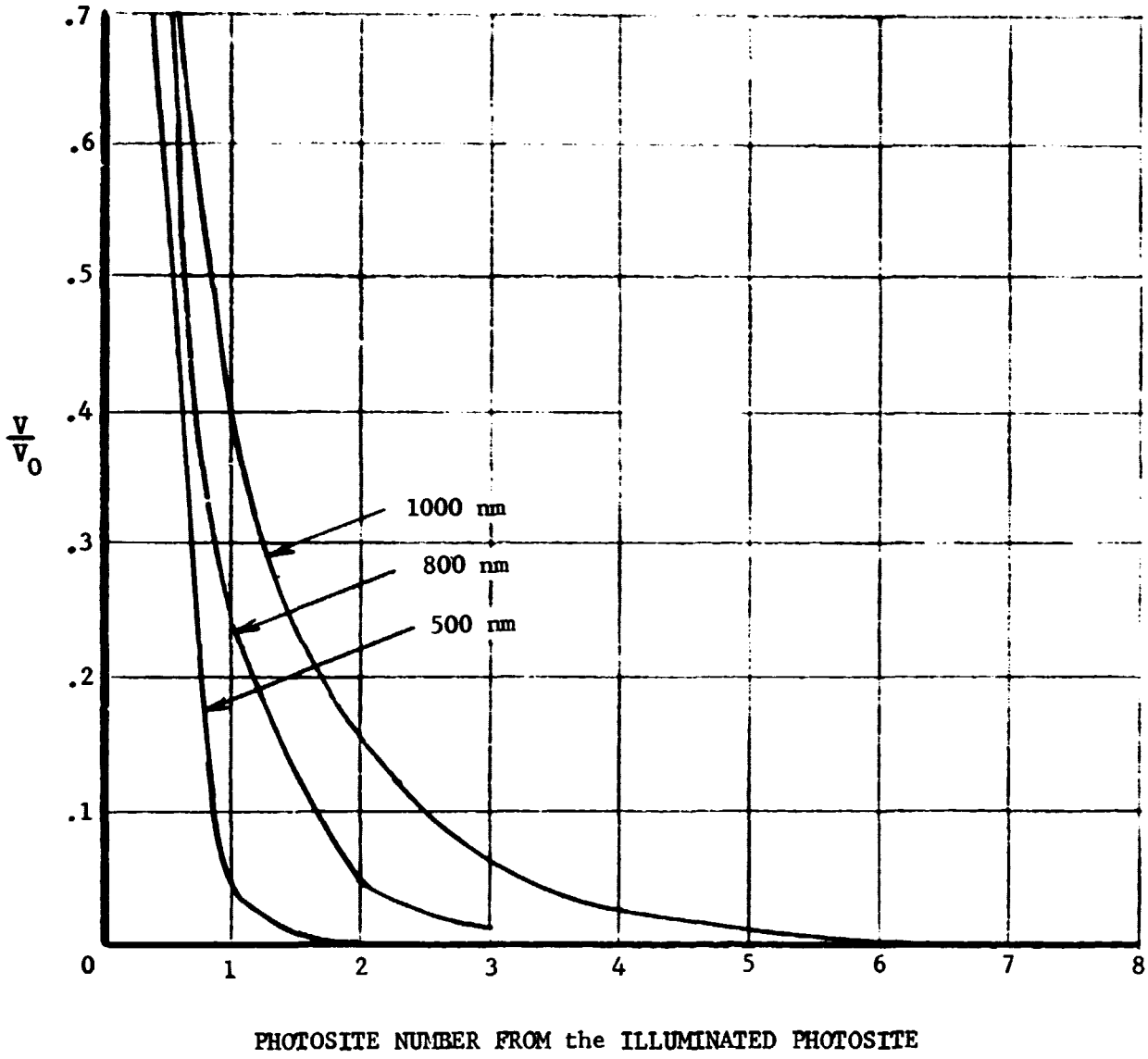


Figure IV-52 CCD121H, Crosstalk vs Wavelength

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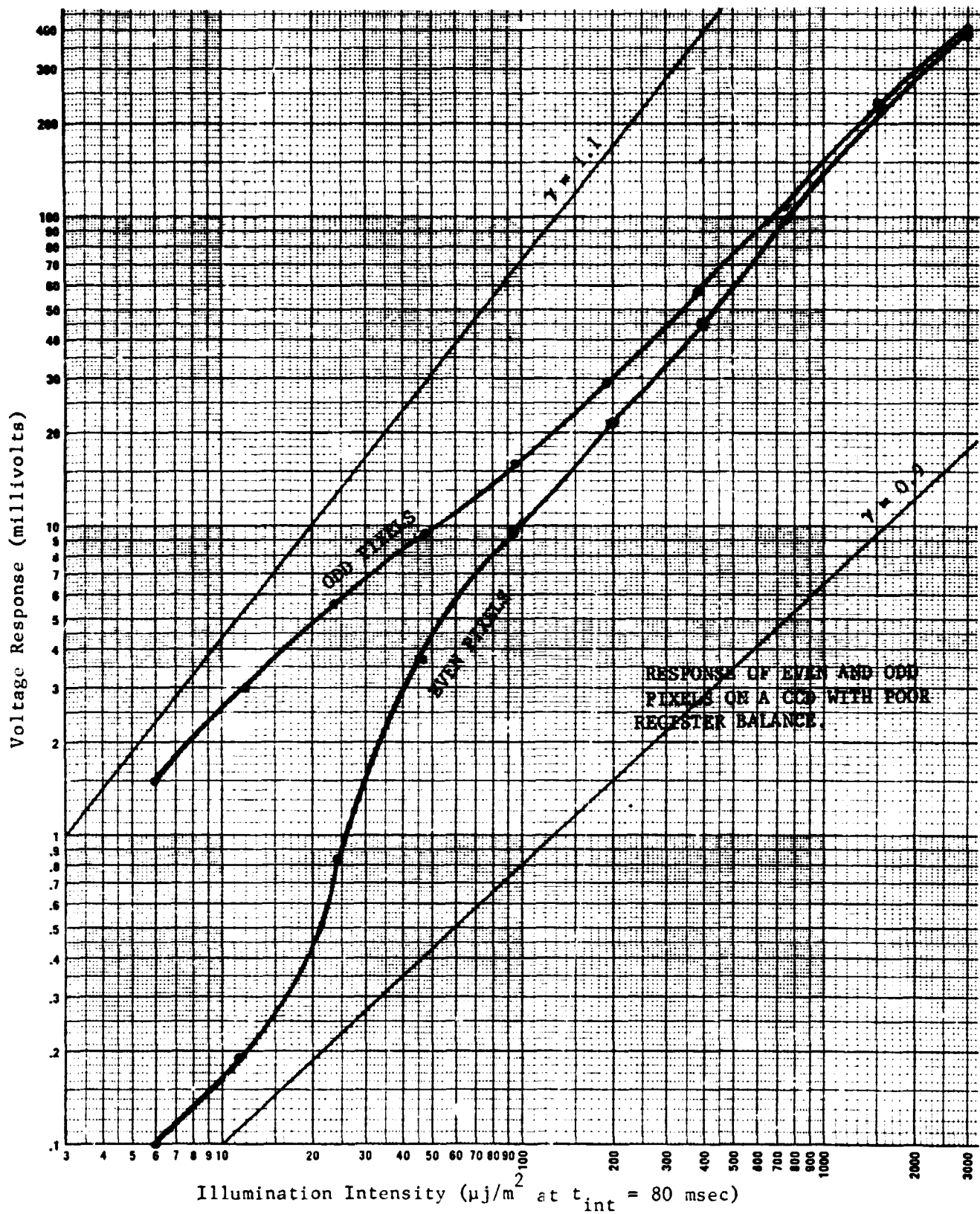
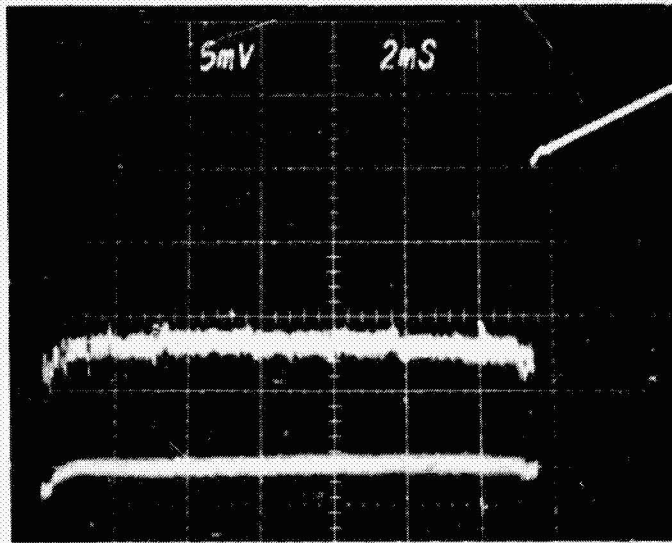
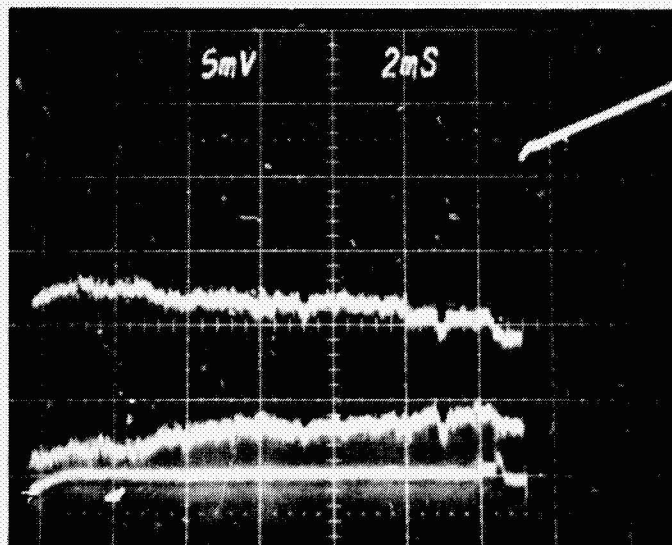


Figure IV-53 Voltage Gamma of CCD121H with Odd-Even Unbalance

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A) Normal Response to $53 \mu\text{j}/\text{m}^2$ Illumination
 PG = 8 V, T = -10°C



B) Response to $53 \mu\text{j}/\text{m}^2$ Illumination With
 Odd-Even Unbalance, PG = 8 V, T = -10°C

Figure IV-54 Oscilloscope Display of the OS Signal

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of dark and illuminated conditions. Figure IV-54b shows the display which results from a device with odd-even imbalance. Figures IV-54c and IV-54d show the results of increasing or decreasing the photogate voltage from 8.0 volts. This characteristic seems to be most prevalent on earlier wafer runs and is wafer related.

2. Dark Signal.

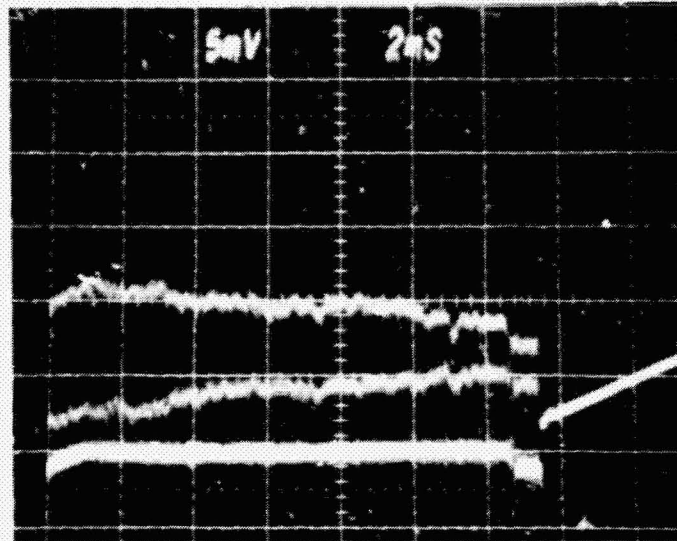
The amount of signal transferred into the output amplifier with no illumination to the device is called the dark signal. The dark signal is caused by thermal generation of electrons within the silicon which are accumulated into a potential well. Since dark current appears in the photo elements as well as in the shift register, there are two parts which make up the total dark signal. The register dark current is made up of the sum of the contributions from each shift register element, and therefore appears as a constant level for all pixels readout. The photo element dark current is different for each pixel since it is parallel loaded into the shift register. This component causes a variation from one pixel to the next. The two components of the 25°C dark signal of a device are illustrated in Figure IV-55. The first photo shows the OS waveform with the transfer gates turned off, preventing photo element data from being loaded into the shift registers. The second photo shows the same device with the transfer gates activated.

Since the dark current generates charge which increases linearly with respect to time, the register dark current increases as the shift register phase clock frequency decreases. Also, the photosite dark current increases in proportion to integration time. Figure IV-56 shows experimental results of the effect of clock frequency on register dark signal, and of integration time on photosite dark signal.

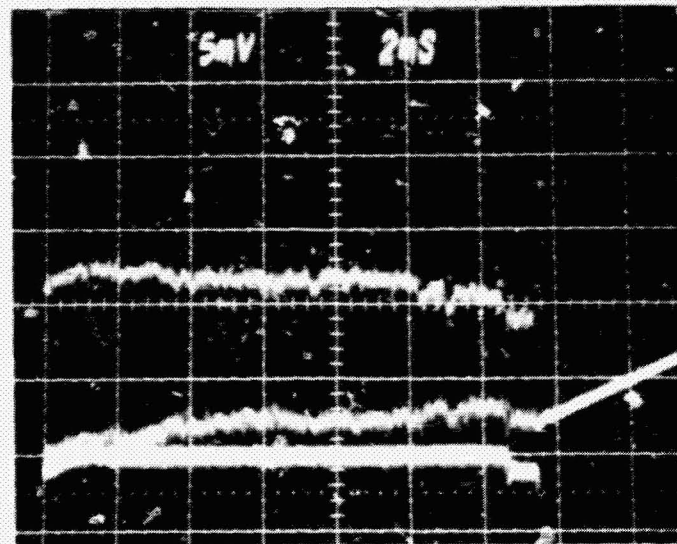
Localized defects in the photosite area can cause an increased dark current in a single pixel. Most devices tested have some isolated pixels with high dark signals, or "spikes." Quite often, if the defect appears in the channel stop junction, a pair of pixels is affected. The amplitude of a spike follows the same integration time relationship as a normal pixel, but does not necessarily follow the normal temperature dependence.

Dark signal is greatly affected by temperature. Figure IV-57 shows experimental data of this dependence. In general, dark signal drops in half for each 8°C decrease in temperature in the range from 25°C to -20°C. Some spikes follow this same dependence, but some have a sudden increase as a particular temperature is exceeded.

The effects of device self-heating can be seen in the pixel response. Nearly all of the 200 mW dissipated by the device is in the output amplifier transistors. The amplifier is located at the end of the chip closest to Pixel 1. A test was performed to measure the temperature rise of the photo elements on the chip. The amplifier power was pulsed on for 30 usec once every 80 msec while the



C) Response to $53 \mu\text{j}/\text{m}^2$ Illumination With
 Odd-Even Unbalance, PG = 10 V, T = -10°C

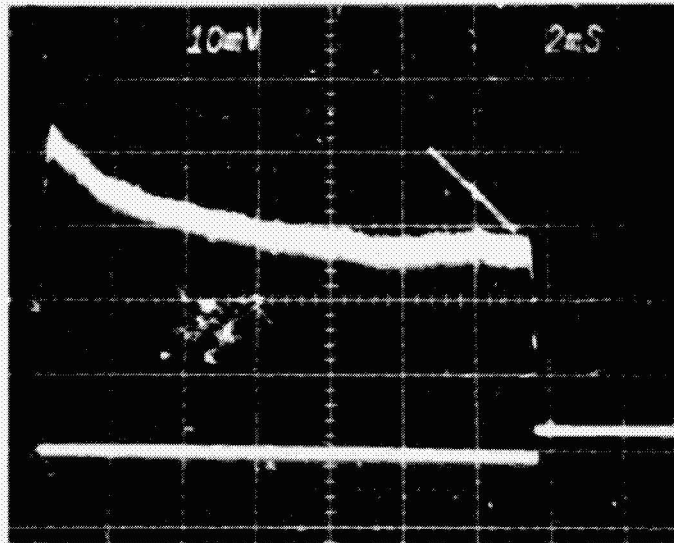


D) Response to $53 \mu\text{j}/\text{m}^2$ Illumination With
 Odd-Even Unbalance, PG = 7 V, T = -10°C

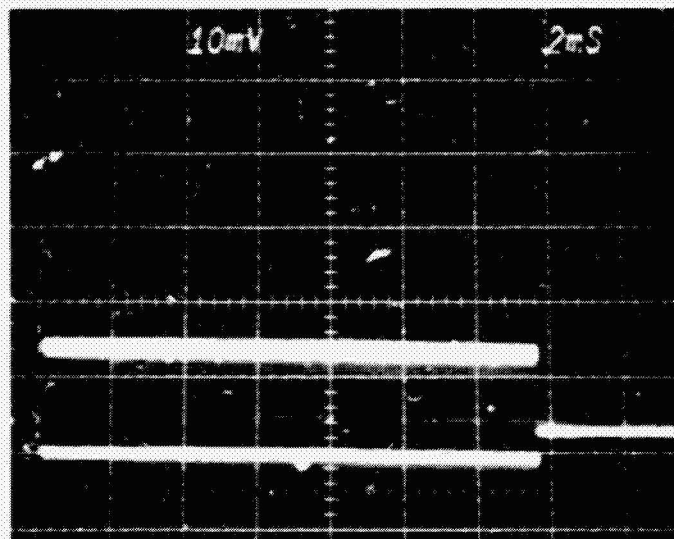
Figure IV-54 (cont)

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A) 25°C Dark Signal With Transfer Gates OFF



B) 25°C Dark Signal With Transfer Gates ON

Figure IV-55 CCD121H Dark Signal

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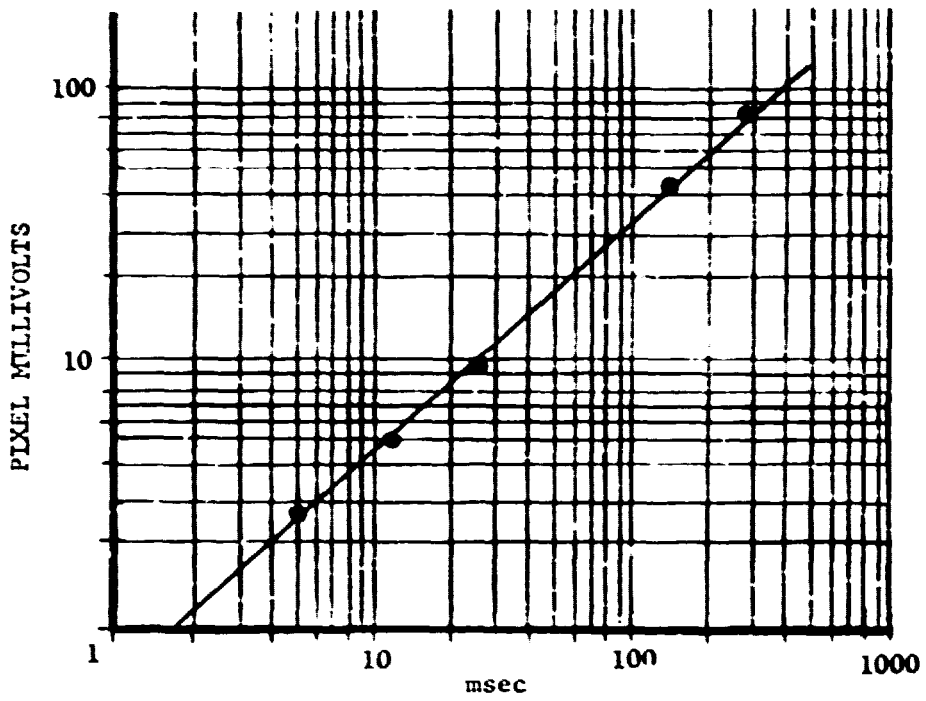
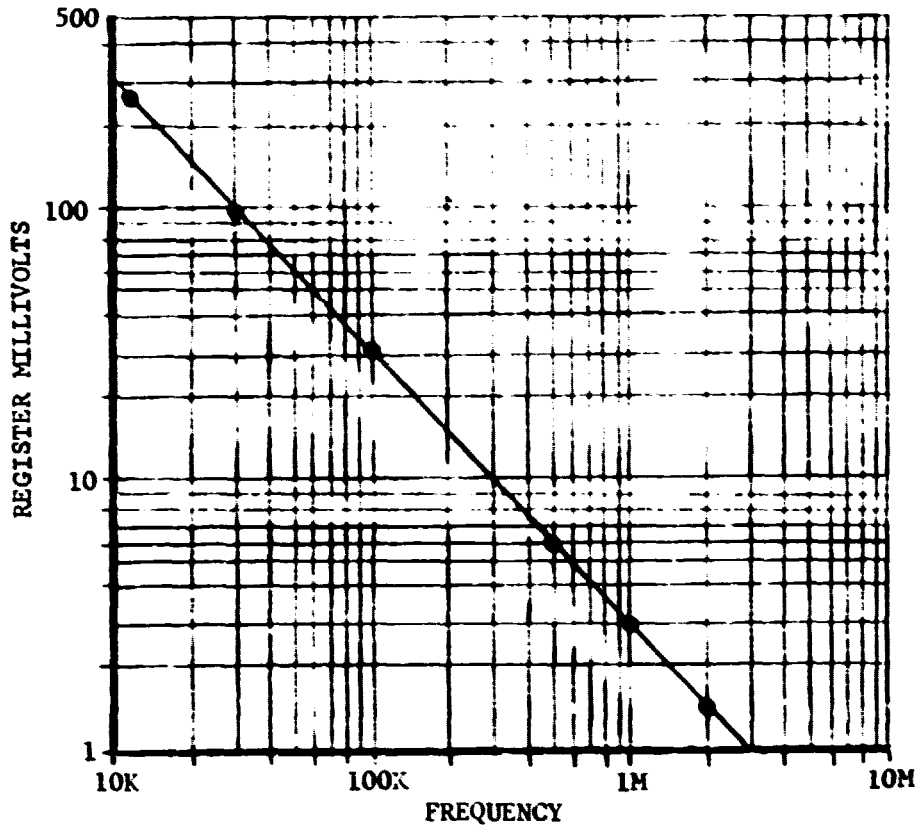


Figure IV-56 Dark Signal vs Frequency, Integration Time

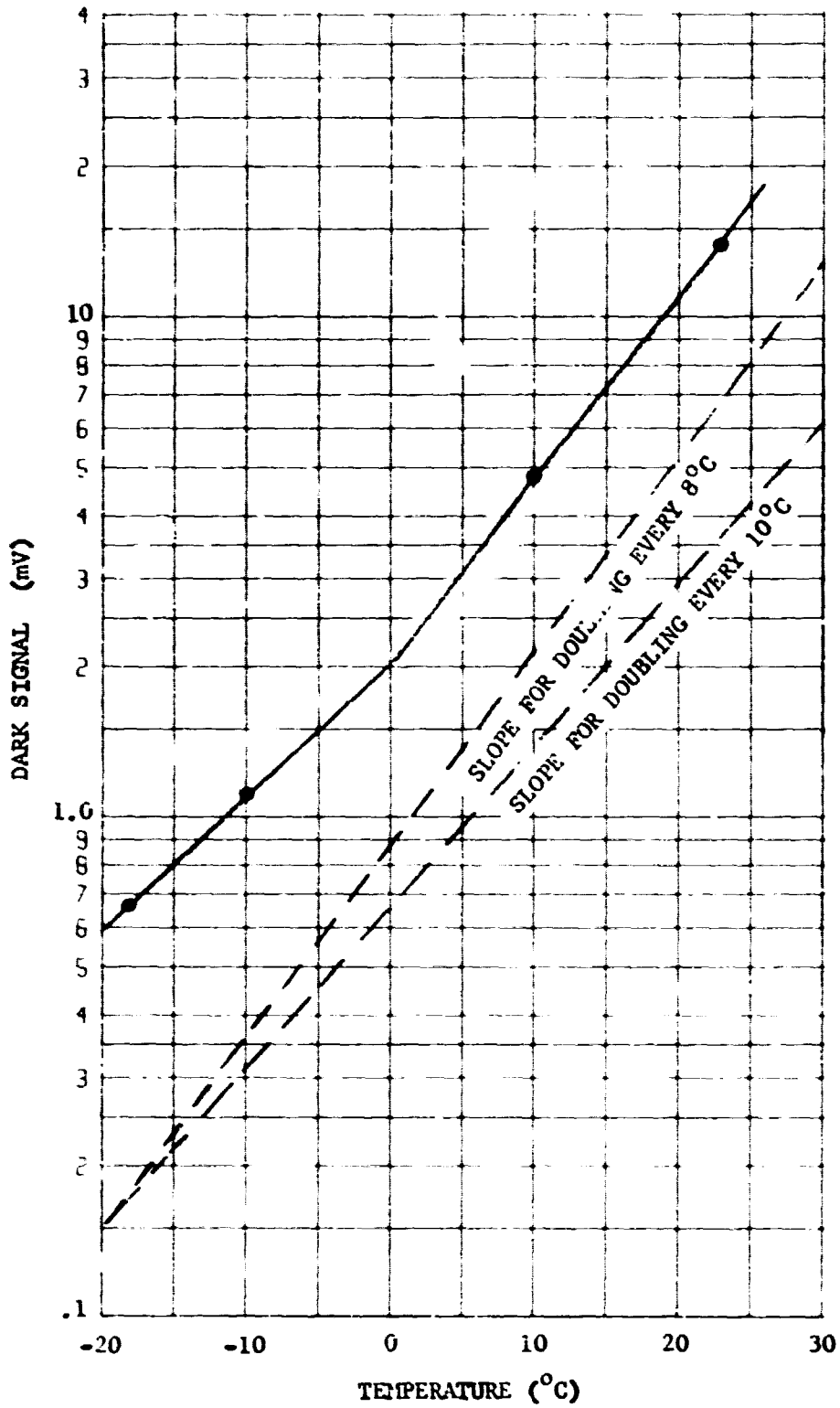


Figure IV-57 Dark Signal Temperature Dependence

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device temperature was varied. Thus, a zero power calibration was made of amplifier DC output level, and selected pixel voltages versus temperature. Then the amplifier was powered continuously at a power level of 220 mW. The results of the test are shown in Figure IV-58. The thermal resistance (θ_{JC}) of the test configuration was found to be 39°C/W, but would be considerably lower in the commercially supplied package. A photograph of the pixel readout showing the increased dark signal near the amplifier end (Pixel 1) is also shown in Figure IV-59.

3. Noise.

Noise tests were performed using the conditions and double-correlated sampling technique shown in Section IV-B. The noise is measured by calculating the RMS value of 125 consecutive samples of the same pixels. Since there is a variation among devices in voltage responsivity and amplifier gain, the noise is converted into noise equivalent irradiance by dividing the RMS noise signal by the measured responsivity. Typical results are as follows:

NEH Dark, +25°C = 1.5 $\mu\text{j}/\text{m}^2$
 NEH Dark, -10°C = 1.0 $\mu\text{j}/\text{m}^2$
 NEH 1400 $\mu\text{j}/\text{m}^2$, +25°C = 2.5 $\mu\text{j}/\text{m}^2$
 NEH 1400 $\mu\text{j}/\text{m}^2$, -10°C = 2.4 $\mu\text{j}/\text{m}^2$

The noise increases with light due to the light-generated photosite current. The decrease in NEH at -10°C as compared to +25°C is mainly due to the decrease in dark signal, since thermal generation in the photosites produces the same noise as an equivalent amount of light. Reducing the temperature of the device, therefore, improves the useful sensitivity to light at longer integration times.

The noise characteristics of the on-chip amplifier itself was measured. All clock signals were held still, and the reset transistor was held on. The amplifier output was connected to an HP model 310 wave analyzer with a measured noise bandwidth of 2.7 KHz, and to an HP model 302 wave analyzer with a measured noise bandwidth of 5.5 Hz. The model 310 was used above 10 KHz, and the model 302 was used below 10 KHz. The results are plotted in Figure IV-60.

4. Output Amplifier Tests.

Output amplifier characteristics were measured to provide design curves and data which may be useful in some applications. The schematic diagram is shown in Figure IV-61. Figure IV-62 plots I_{OD} and V_{OS} as a function of V_{RD} . V_{OD} was biased at +15V for this test. I_{OD} is the total drain current for both amplifiers on the chip. The plot shows that the amplifier voltage gain (V_{OS}/V_{RD}) increases to about 0.55 up to $V_{RD} = 10\text{V}$, and then remains steady above 10V. The amplifier is not useful for V_{RD} less than 7 volts because this is the voltage at which the reset transistor cannot be turned off with 0 volts on ϕ_R .

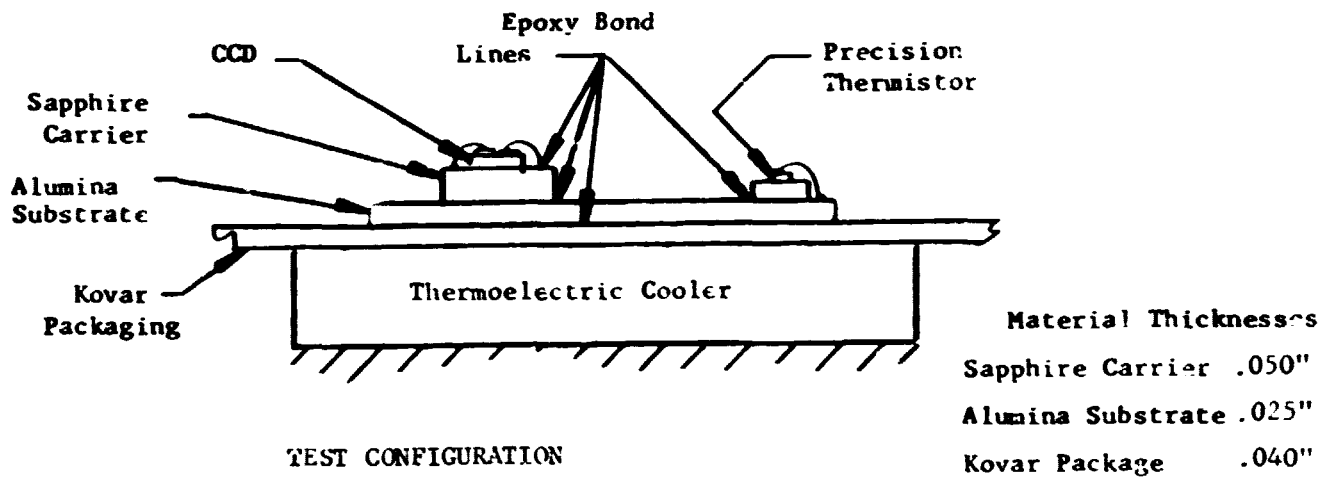
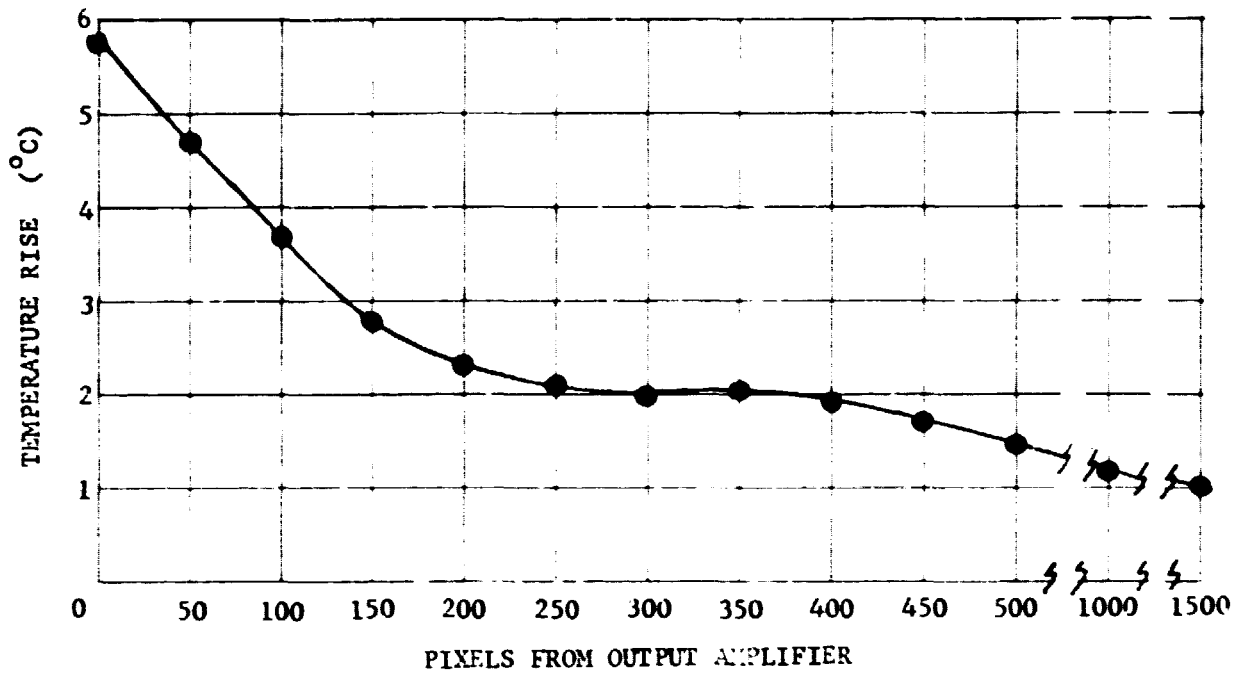


Figure IV-58 Dark Signal vs Pixel Position (Temperature Effects)

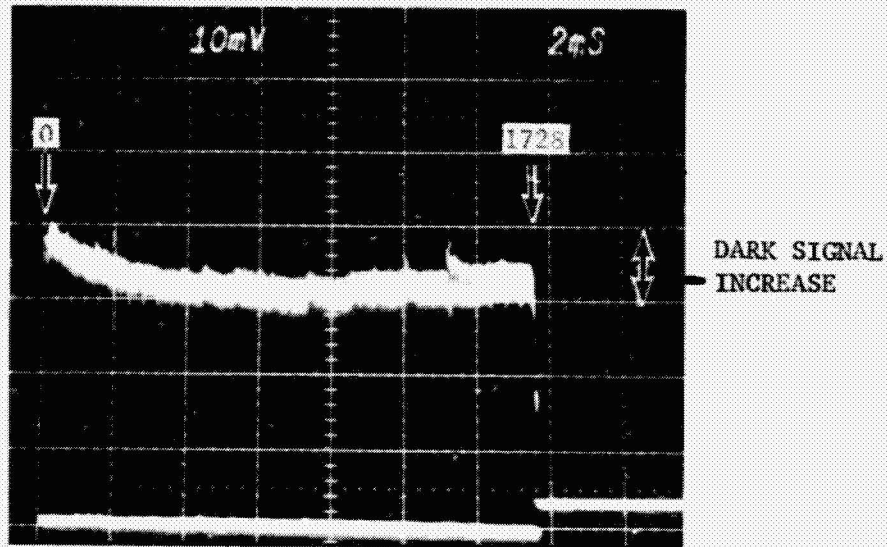


Figure IV-59 Effect of Temperature Rise at Output Amplifier End On Dark Signal Output.
 $T_A = 25^{\circ}\text{C}$

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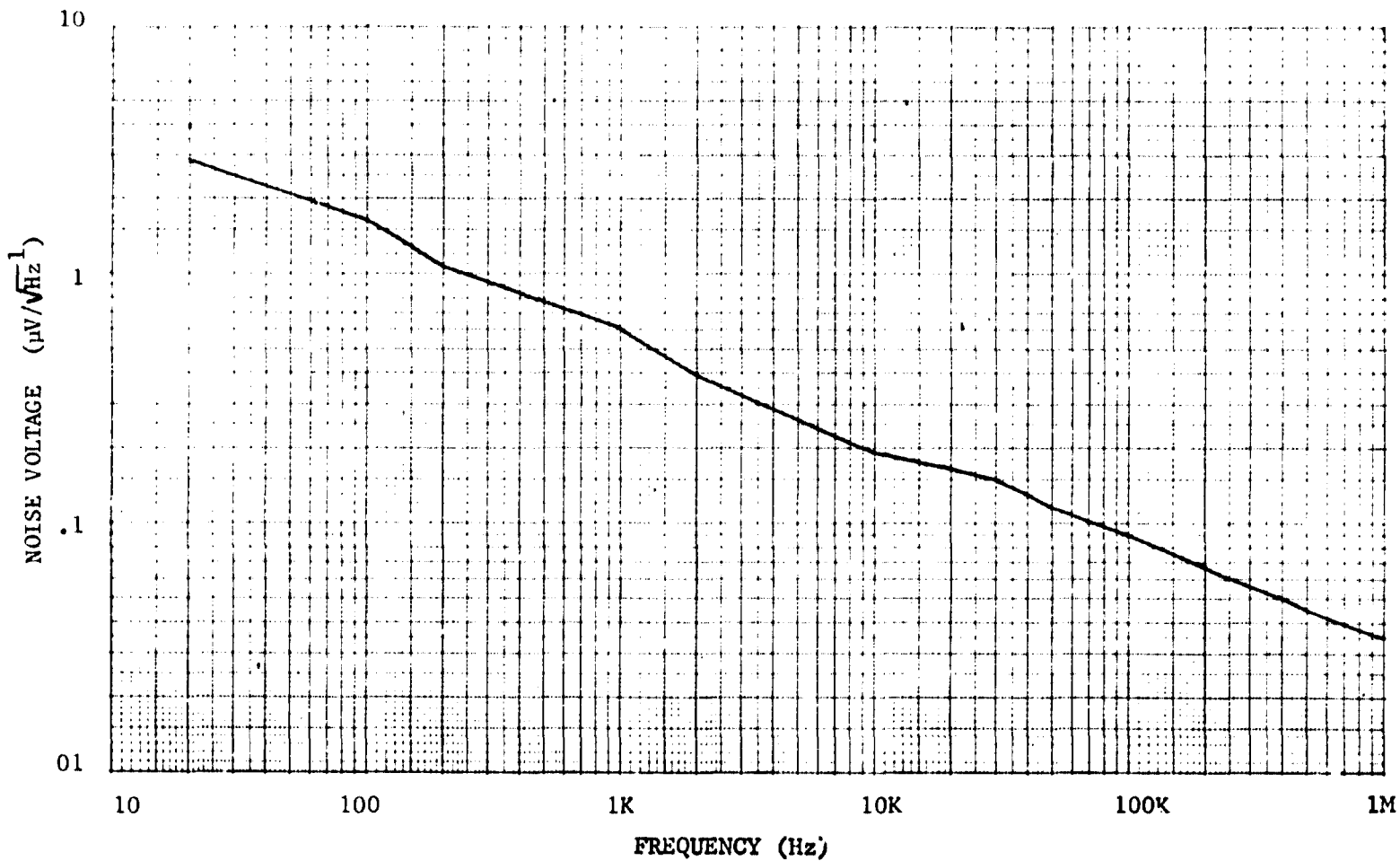


Figure IV-60 Output Amplifier Noise Spectral Density

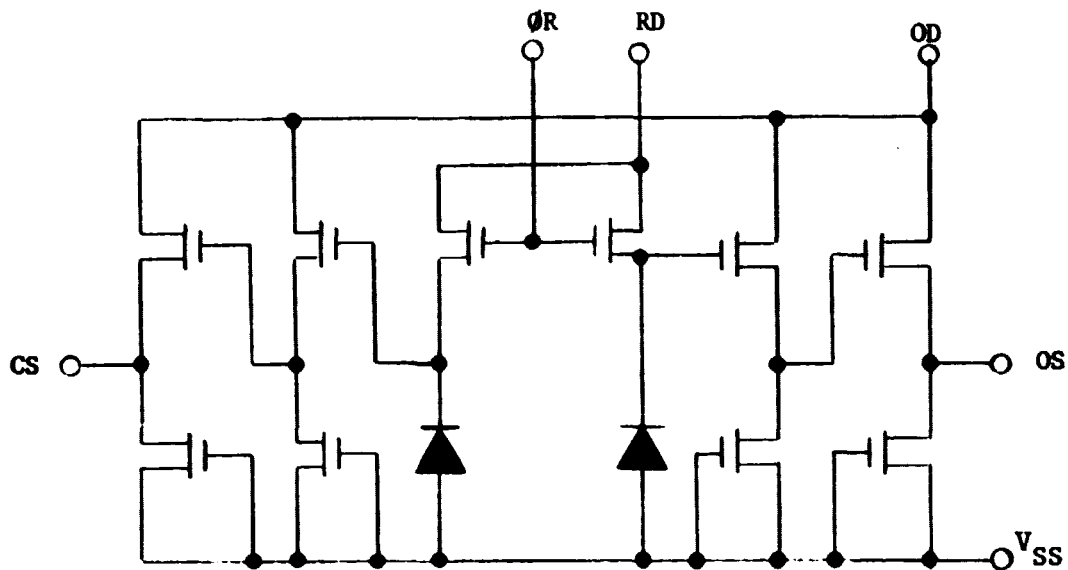


FIGURE IV-61. Amplifier Schematic

5. Electrical Input Circuit.

As described earlier, the electrical input network can be used to inject charge into the end of the shift register furthest from the amplifier. The linearity of these inputs was tested by comparing TPG input voltage to OS pixel voltage. The results are shown in Figure IV-63. An increasing amount of nonlinearity was noted at low injection voltages.

If the injected signal is to be other than a steady DC level, some attention must be paid to the timing relationships. The input signal must be at the proper level at the time of the TPS pulse. The level must remain steady throughout the pixel period following the pixel period of the transfer. The timing requirements are shown in Figure IV-64.

6. Transfer Losses.

Transfer losses can be classified into two categories; charge transfer efficiency refers to the percentage of charge that shifts for each transfer. Trapping loss refers to charge which is absorbed into traps in silicon bulk, and then released slowly.

- a) Transfer Efficiency. Transfer efficiency has been measured both optically and electrically using the input networks. The optical method uses a single spot focused on the 1727th or 1728th pixels. The electrical method uses a single pulse injected into the TPGA or TPGB inputs. The output, observed 1731 transfers later, compared to the output observed 1733 transfers later can be converted to transfer efficiency using the following formula:

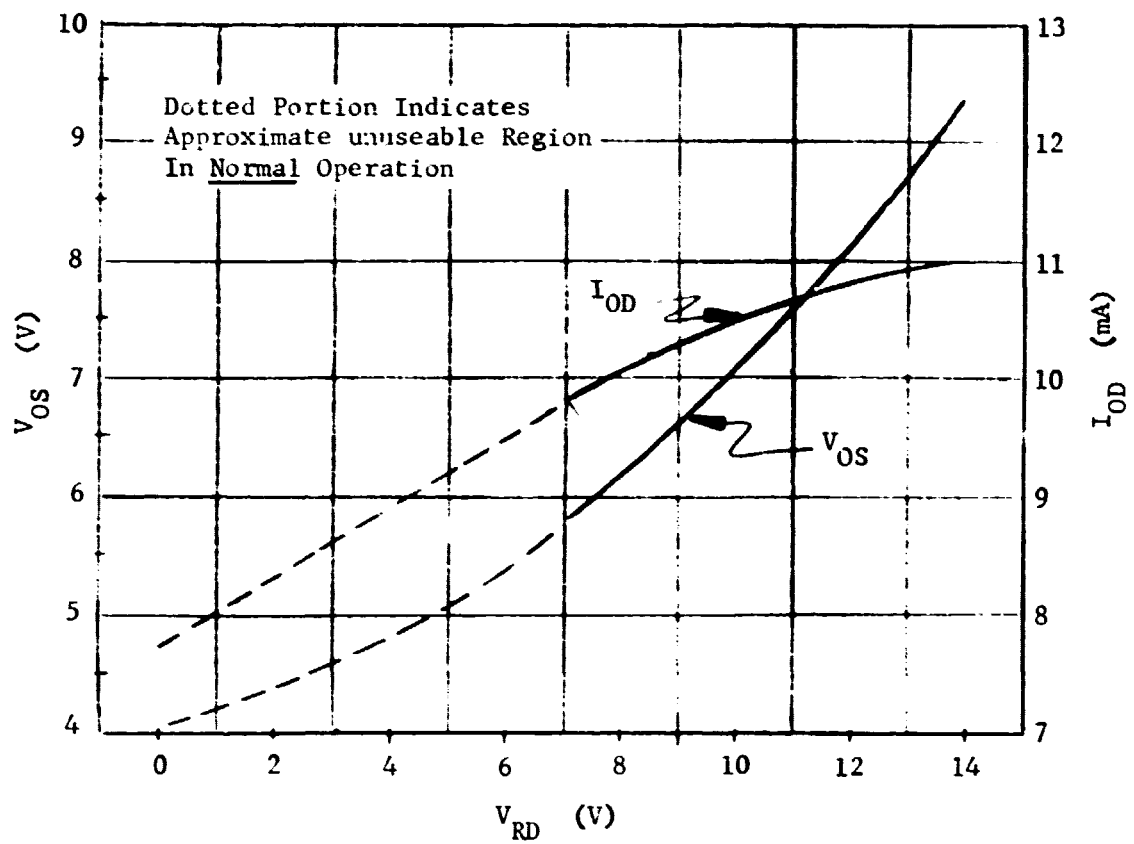
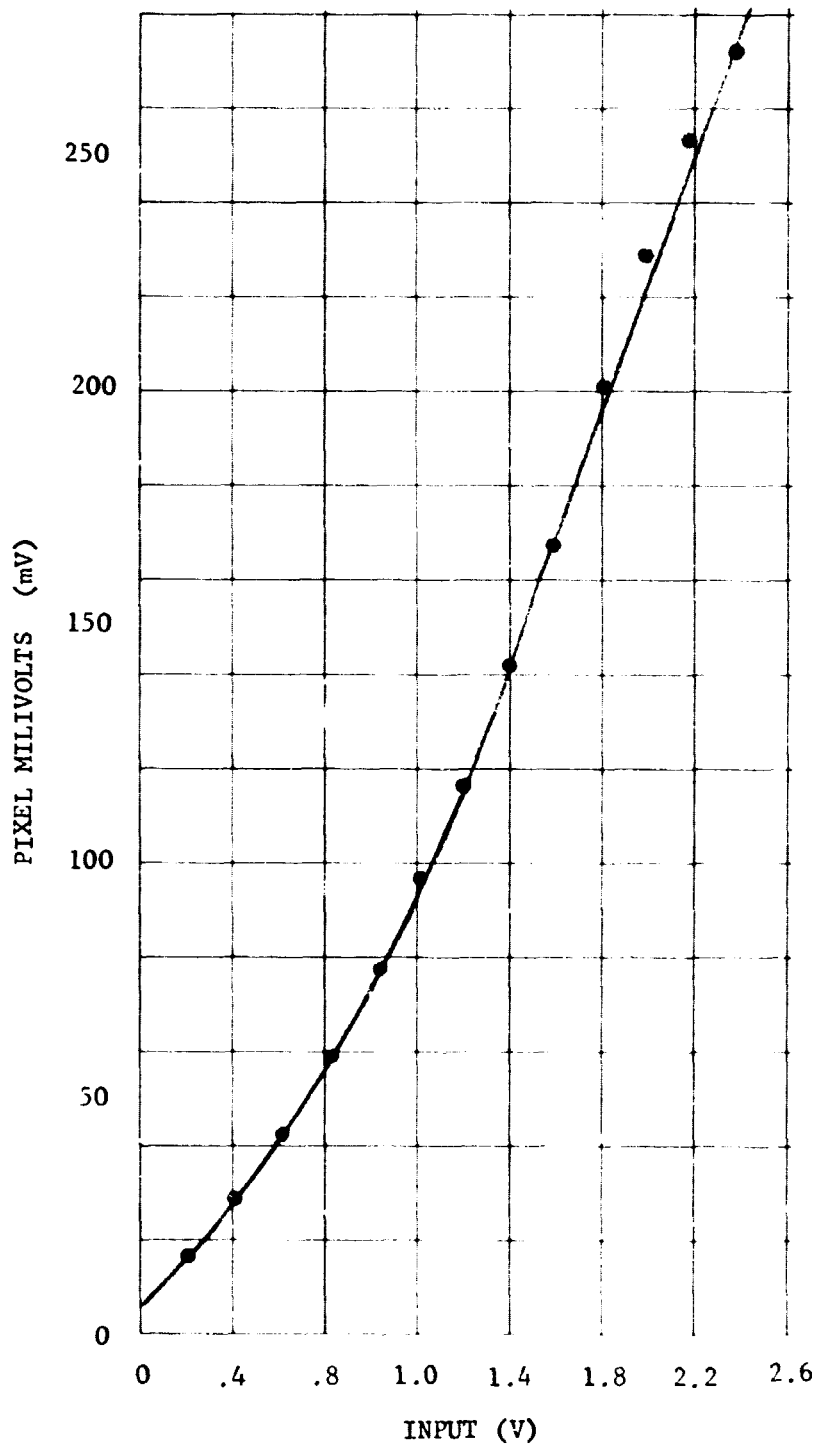


Figure IV-62 Output Amplifier Characteristics

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Figure IV-63 Average Input-Output Transfer Function

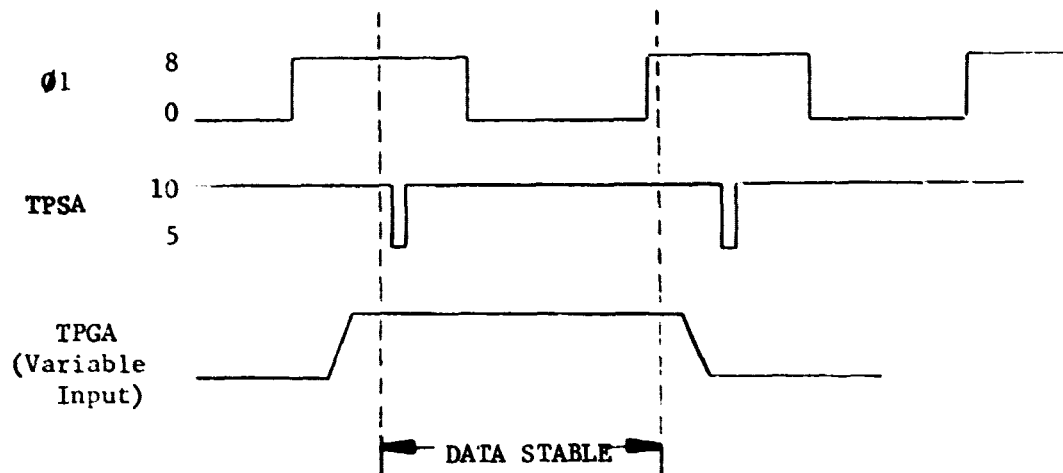


FIGURE IV-64. Input Timing

$$\text{Transfer Efficiency} = 1 - \frac{V_{\text{After 1733 shifts}} - 1}{V_{\text{After 1731 shifts}} - 1732}$$

where V is the difference in the pixel voltage with and without an injection pulse or a light spot.

Typical values measured for transfer efficiency are 0.999990 to 0.999999. The efficiency varies slightly with temperature, improving with decreasing temperature. The following data illustrates the temperature effect on some sample devices:

	CTE 25°C	CTE -10°C
#1	.9999777	.9999719
#2	.9999914	.9999974
#3	.9999938	.9999966
#4	.9999910	.9999954
#5	.9999919	.9999954

- b) **Trapping Loss.** It is difficult to separate losses due to trapping from transfer efficiency losses. The transfer efficiency must be measured first, and then considered when calculating trapping loss. Again, trapping loss has been measured both electrically and optically.

Cumulative trapping loss along the entire shift register without any background charge due to "slim zero" injection, dark signal.

or light can be as high as 50%. Applying the equivalent of 400 $\mu\text{j}/\text{m}^2$ of injection satisfies most of the traps and reduces the loss to the 5 to 10% range.

C. MECHANICAL TESTS AND ANALYSES

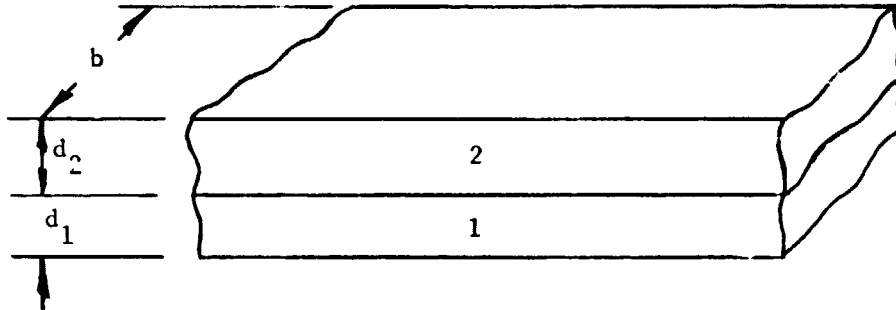
1. Package Effects

Common applications of integrated circuit chips (including ICCDs) involve bonding the chips to a dissimilar material. Mechanical stresses and deformations result if: 1) the chip and its companion material have different thermal coefficients of expansion; and, 2) the combined assembly is at equilibrium at a temperature other than that at which the bonding medium became essentially non-compliant. These stresses and deformations are usually described as thermally induced stresses and deformations, although a more accurate term would be thermal expansion difference induced stresses and deformations.

The first condition for thermal expansion induced effects is very common since most of the materials used in packaging IC chips are selected for properties other than a thermal expansion coefficient which closely matches the IC chip (typically silicon, with $\alpha = 2.6 \times 10^{-6}/^\circ\text{C}$). Following is a tabulation of materials (and their properties) which are commonly used as package or substrate materials in conjunction with ICCD chips:

Material	T.C.E. $\left[\frac{1}{^\circ\text{C}} \right]$	Elastic Modulus $\left[\frac{\text{lbf}}{\text{in}^2} \right]$
Aluminum	23×10^{-6}	10×10^6
Alumina	6.3×10^{-6}	48×10^6
Beryllia	6.4×10^{-6}	51×10^6
Copper	17.6×10^{-6}	17×10^6
Glass	7.5×10^{-6}	11.8×10^6
Kovar	4.8×10^{-6}	21.6×10^6
Quartz (Fused)	0.5×10^{-6}	55×10^6
Sapphire	$5.8-6.7 \times 10^{-6}$	55×10^6
Silicon	2.6×10^{-6}	16×10^6
Zirconium	5.4×10^{-6}	14×10^6

To determine the stress and deformation resulting from bonding two dissimilar materials, consider the following model of a two material beam of width b :



For simplified analysis the beam will be assumed to be composed of homogeneous, isotropic materials. Additionally, it will be assumed that the bond line is thin and rigid and that the beam is long (end effects will be ignored, and shear stress in the bond is zero).

For a classical beam of this type the strain in the longitudinal (X) direction is linear function of distance from the neutral axis:

$$\varepsilon_{XX}(Y) = \varepsilon_{XX}(0) + \frac{Y \Delta \varepsilon_{XX}}{d_1 + d_2} \quad 1)$$

Equilibrium requires that:

$$\int \sigma dA = P = \text{externally applied axial load} \quad 2)$$

and,

$$\int \sigma y dA = M = \text{externally applied bending moment} \quad 3)$$

The stress distribution is:

$$(\sigma_{XX})_1 = E_1 \varepsilon_{XX}(Y) \text{ for } 0 < Y < d_1 \quad 4)$$

$$(\sigma_{XX})_2 = E_2 \varepsilon_{XX}(Y) \text{ for } d_1 < Y < d_2 \quad 5)$$

For the case of an applied bending moment (no axial loads or thermal effects),

$$\int_0^{d_1+d_2} b\sigma_{XX}(Y) dY = 0, \quad \int_0^{d_1+d_2} b\sigma_{XX}(Y) YdY = M \quad 6)$$

Substituting 1), 4), and 5) into the equations of 6) we find the strain at $y = 0$.

$$\epsilon_{XX}(0) = -\frac{\Delta\epsilon_{XX}}{2} \left[\frac{1 + 2\frac{E_2d_2}{E_1d_1} + \frac{E_2d_2^2}{E_1d_1^2}}{\left(1 + \frac{d_2}{d_1}\right)\left(1 + \frac{E_2d_2}{E_1d_1}\right)} \right] \quad 7)$$

Substituting 1), 4), and 5) into equation 6) to get an expression for M in terms of the strain variation across the beam,

$$\frac{M}{b} = \int_0^{d_1} E_1 \left(\epsilon_{XX}(0) + \frac{Y\Delta\epsilon_{XX}}{d_1+d_2} \right) YdY + \int_{d_1}^{d_1+d_2} E_2 \left(\epsilon_{XX}(0) + \frac{Y\Delta\epsilon_{XX}}{d_1+d_2} \right) YdY \quad 8)$$

Substituting 7) into 8) and combining terms,

$$\frac{M}{b} = \frac{\Delta\epsilon_{XX} E_1 d_1^3}{12 (d_1+d_2) \left(1 + \frac{E_2 d_2}{E_1 d_1}\right)} \left(1 + 4 \frac{E_2 d_2}{E_1 d_1} - 6 \frac{E_2 d_2^2}{E_1 d_1^2} + 4 \frac{E_2 d_2^3}{E_1 d_1^3} \right) \quad 9)$$

$$+ 12 \frac{E_2 d_2^2}{E_1 d_1^2} + \frac{E_2 d_2^4}{E_1 d_1^4}$$

From simplified beam theory (for small deflections),

$$\frac{1}{R} = \frac{\Delta\epsilon_{XX}}{d_1+d_2}, \quad \text{and } M = \frac{E_1 I_{EFF}}{R} \quad 10)$$

Therefore, for the beam in question, the effective moment of inertia is,

$$I_{EFF} = \frac{bd_1^3}{12 \left(1 + \frac{E_2 d_2}{E_1 d_1}\right)} \left(1 + 4 \frac{E_2 d_2}{E_1 d_1} - 6 \frac{E_2 d_2^2}{E_1 d_2^2} + 4 \frac{E_2 d_2^3}{E_1 d_1^3} \right) \quad (11)$$

$$+ 12 \frac{E_2 d_2^2}{E_1 d_1^2} + \frac{E_2 d_2^4}{E_1 d_1^4}$$

Now the thermal strain problem can be solved.

If materials 1 and 2 of the beam are not bonded together, a temperature change, ΔT would result in the beam sections changing length by $\alpha_1 \Delta T$ and $\alpha_2 \Delta T$ (for a unit length of the beam). To restore the beam to its bonded configuration, external axial loads P_1 and P_2 can be applied to the two beam segments. To provide compatibility the strains imposed by the temperature expansion and by the external load must satisfy,

(12)

$$(\epsilon_{XX})_1 + \alpha_1 \Delta T = (\epsilon_{XX})_2 + \alpha_2 \Delta T$$

where,

$$(\epsilon_{XX})_1 = \frac{P_1}{E_1 d_1 b}, \text{ and } (\epsilon_{XX})_2 = \frac{P_2}{E_2 d_2 b} = \frac{-P_1}{E_2 d_2 b}$$

The axial load, P_1 , then is

(13)

$$P_1 = \frac{(\alpha_2 - \alpha_1) \Delta T E_2 d_2 b}{\left(1 + \frac{E_2 d_2}{E_1 d_1}\right)}$$

The axial loads act as an externally applied moment (since they are applied to the center of their material thickness) of size,

(14)

$$M = \frac{1}{2} P_1 (d_1 + d_2)$$

An opposing moment must be externally applied to return the beam to its uncurved configuration,

15)

$$M = -M' = -\frac{1}{2} (\alpha_2 - \alpha_1) \Delta T \left[\frac{E_2 d_2 b (d_1 + d_2)}{\left(1 + \frac{E_2 d_2}{E_1 d_1}\right)} \right]$$

Substituting 15) into 10) to find the curvature that would result from this externally applied moment,

16)

$$\frac{1}{R} = -\frac{1}{2} (\alpha_2 - \alpha_1) \Delta T d_1^2 \left[\frac{\left(\frac{d_2}{d_1} + 1\right) \frac{E_2 d_2}{E_1 d_1} b}{I_{EFF} \left(1 + \frac{E_2 d_2}{E_1 d_1}\right)} \right]$$

Substituting 10) into 16) to find $\Delta \epsilon_{XX}$,

17)

$$\Delta \epsilon_{XX} = -\frac{1}{2} (\alpha_2 - \alpha_1) \Delta T d_1^2 \left[\frac{\left(\frac{d_2}{d_1} + 1\right) \frac{E_2 d_2}{E_1 d_1} b}{I_{EFF} \left(1 + \frac{E_2 d_2}{E_1 d_1}\right)} \right]$$

which may be substituted into 7) to find $\epsilon_{XX}(0)$, then the appropriate substitutions may be made in 4) and 5) to find the strains in the materials:

18)

$$\epsilon_{XX}(Y) = \frac{3 (\alpha_2 - \alpha_1) \Delta T \left(\frac{d_1 + d_2}{d_1}\right) \left[1 - 2 \frac{Y}{d_1} + 2 \frac{E_2 d_2}{E_1 d_1} \left(1 - \frac{Y}{d_1}\right) + \frac{E_2 d_2^2}{E_1 d_1^2} \right]}{\left(1 + 4 \frac{E_2 d_2}{E_1 d_1} - 6 \frac{E_2 d_2^2}{E_1 d_1^2} + 4 \frac{E_2 d_2^3}{E_1 d_1^3} + 12 \frac{E_2^2 d_2^2}{E_1^2 d_1^2} + \frac{E_2^2 d_2^4}{E_1^2 d_1^4} \right) \left(1 + \frac{E_1 d_1}{E_2 d_2}\right)}$$

For some applications, the stresses in the materials are less significant than are the deformations from a flat surface. An obvious example of this is the non-flatness of the focal plane of a hybrid (or monolithic) circuit using large ICCDs. For large curvatures, the deviation of the mid-point of a beam from the straight line connecting its ends is:

19)

$$\Delta Z = \frac{l^2}{8R}$$

where l is the length of the beam and R is the previously derived radius of curvature.

For area CCDs the previous analysis for a beam may be modified simplistically to a plate mode as follows:

20)

$$\sigma_{XX} = \frac{E}{(1-\nu^2)} (\epsilon_{XX} + \nu \epsilon_{YY})$$

21)

$$\sigma_{YY} = \frac{E}{(1-\nu^2)} (\epsilon_{YY} + \nu \epsilon_{XX})$$

ϵ_{XX} and ϵ_{YY} are assumed to be equal and a linear function of the depth, Z , so that,

22)

$$M_X = \int_0^{d_1+d_2} Z \sigma_{XX} (Z) dZ$$

Also from equilibrium of forces,

23)

$$0 = \int_0^{d_1+d_2} \sigma_{XX} (Z) dZ$$

simplifying 20) since $\epsilon_{XX} = \epsilon_{YY}$ and substituting into 22) and 23),

24)

$$M_X = \int_0^{d_1} E_1 \left(\epsilon_{XX}(0) + \frac{Z \Delta \epsilon_{XX}}{d_1 + d_2} \right) Z dz + \int_{d_1}^{d_2} E_2 \left(\epsilon_{XX}(0) + \frac{Z \Delta \epsilon_{XX}}{d_1 + d_2} \right) Z dz$$

25)

$$0 = \int_0^{d_1} \frac{E_1}{1-\nu_1} \left(\epsilon_{XX}(0) + \frac{Z \Delta \epsilon_{XX}}{d_1 + d_2} \right) dz + \int_{d_1}^{d_2} \frac{E_2}{1-\nu_2} \left(\epsilon_{XX}(0) + \frac{Z \Delta \epsilon_{XX}}{d_1 + d_2} \right) dz$$

Equation 25) can be solved for $\epsilon_{XX}(0)$,

26)

$$\epsilon_{XX}(0) = - \frac{\Delta \epsilon_{XX}}{2} \left[\frac{E_1 d_1^2}{1-\nu_1} + \frac{E_2 (d_2^2 - d_1^2)}{1-\nu_2} \right] \left[\frac{E_1 d_1}{1-\nu_1} + \frac{E_2 (d_2 - d_1)}{1-\nu_2} \right]$$

Substituting 26) into 24) and solving in terms of $\Delta \epsilon_{XX}$,

27)

$$M_X = \frac{E_1 \Delta \epsilon_{XX} d_1^3}{12 (d_1 + d_2) \left(\frac{1-\nu_2}{1-\nu_1} + \frac{E_2 d_2}{E_1 d_1} - \frac{E_2}{E_1} \right)} \left\{ \begin{aligned} & -3 \left[\frac{1-\nu_2}{1-\nu_1} + \frac{E_2 d_2}{E_1 d_1} - \frac{E_2}{E_1} \right] \left[1 + \frac{E_2 d_2^2}{E_1 d_1^3} - \frac{E_2}{E_1} \right] \\ & + 4 \left[\frac{1-\nu_2}{1-\nu_1} + \frac{E_2 d_2}{E_1 d_1} - \frac{E_2}{E_1} \right] \left[1 + \frac{E_2 d_2^2}{E_1 d_1^3} - \frac{E_2}{E_1} \right] \end{aligned} \right\}$$

from 10), $M_X = \frac{EI_{EFF} \Delta \epsilon_{XX}}{d_1 + d_2}$ we find that,

$$I_{EFF} = \frac{d_1^3}{12 \left(\frac{1-\nu_2}{1-\nu_1} + \frac{E_2 d_2}{E_1 d_1} - \frac{E_2}{E_1} \right)} \left\{ \begin{array}{l} -3 \left[\frac{1-\nu_2}{1-\nu_1} + \frac{E_2 d_2^2}{E_1 d_1^2} - \frac{E_2}{E_1} \right] \left[1 + \frac{E_2 d_2^2}{E_1 d_1^2} - \frac{E_2}{E_1} \right] \\ +4 \left[\frac{1-\nu_2}{1-\nu_1} + \frac{E_2 d_2}{E_1 d_1} - \frac{E_2}{E_1} \right] \left[1 + \frac{E_2 d_2^3}{E_1 d_1^3} - \frac{E_2}{E_1} \right] \end{array} \right\} \quad (28)$$

consider this plate in the same fashion that the beam was previously, the axial load required is,

$$P_1 = -P_2 = \frac{(\alpha_2 - \alpha_1) \Delta T d_1 E_1}{(1-\nu_1) \left(1 + \frac{d_1 E_1 (1-\nu_2)}{d_2 E_2 (1-\nu_1)} \right)} \quad (29)$$

and the resulting curvature is

$$\frac{1}{R} = -\frac{1}{2} (\alpha_2 - \alpha_1) \Delta T \left[\frac{d_1^2 \left(1 + \frac{d_2}{d_1} \right)}{I_{EFF} \left[1 + \frac{d_1 E_1 (1-\nu_2)}{d_2 E_2 (1-\nu_1)} \right]} \right] \quad (30)$$

from 10) the strain increment is

$$\Delta \epsilon_{XX} = -\frac{1}{2} (\alpha_2 - \alpha_1) \Delta T \left[\frac{d_1 (d_1 + d_2)^2}{I_{EFF} \left[1 + \left(\frac{d_1 E_1 (1-\nu_2)}{d_2 E_2 (1-\nu_1)} \right) \right]} \right] \quad (31)$$

This may be substituted into 26) to find the strain as a function of Z.

32)

$$\epsilon_{XX}(Z) = \epsilon_{YY}(Z) = -\frac{\alpha_2 \alpha_1 \Delta T}{2} \frac{d_1 (d_1 + d_2)^2}{I_{EFF} \left(1 + \frac{d_1 E_1 (1 - \nu_2)}{d_2 E_2 (1 - \nu_1)}\right)} \left[Z - \left(\frac{\frac{E_1 d_1^2}{1 - \nu_1} + \frac{E_2 (d_2^2 - d_1^2)}{1 - \nu_2}}{2 (d_1 + d_2) \left(\frac{E_1 d_1}{1 - \nu_1} + \frac{E_2 (d_2 - d_1)}{1 - \nu_2} \right)} \right) \right]$$

Examples:

Case I -- Linear imaging CCD eutectically bonded to alumina dual inline package. (For long, narrow CCD the beam model will be used).

Alumina: $d_1 = .025$ in., $E_1 = 48 \times 10^6$ psi,
 $\alpha_1 = 6.3 \times 10^{-6}/^\circ\text{C}$;

Silicon: $d_2 = .008$ in., $E_2 = 16 \times 10^6$ psi,
 $\alpha_2 = 2.6 \times 10^{-6}/^\circ\text{C}$;

Gold-silicon eutectic melting point = 377°C , so $\Delta T = -352^\circ\text{C}$.

For $Y/d_1 = 0$ (i.e., maximum stress in alumina), $\sigma_{XX} = 330,000$ psi (Tension);

For $Y/d_1 = 1 + d_2/d_1$ (i.e., maximum stress in silicon),
 $\sigma_{XX} = -138,000$ psi (Compression).

Case II - Similar ICCD, epoxy mounted to multilayer sapphire substrate.

Sapphire: $d_1 = .050$ in., $E_1 = 55 \times 10^6$ psi,
 $\alpha_1 = 6.3 \times 10^{-6}/^\circ\text{C}$; Epoxy cures at 125°C ,
so $\Delta T = -100^\circ\text{C}$.

For $Y/d_1 = 0$ (i.e., maximum stress in sapphire), $\sigma_{XX} = 77,938$ psi (Tension);

For $Y/d_1 = 1 + d_2/d_1$ (i.e., maximum stress in silicon),
 $\sigma_{XX} = -27,350$ psi (Compression).

2. Dark Signal vs. Mechanical Strain

A Fairchild CCD121W ICCD was epoxy attached to a tensile test bar. The ICCD was strained at the following strain levels: 50, 100, 200, 400, 600, 800, and 1000 microinches/inch. At each strain level the dark signal from six pixels was measured (pixels 14, 15, 874, 875, 1714, and 1715) and the ambient temperature (to 0.5°C) was recorded. The table below is a summary of the average normalized 80°C doubling, divided by zero load dark signal at the start of testing, and averaged for the six test pixels).

Strain X10 ⁶	0	50	100	200	400	600	800	0
Relative Dark Signal	1.00	.95	1.02	1.07	1.02	1.01	.94	.94

There is no apparent correlation between strain and dark signal. Any relationship is concealed by the uncertainty of the temperature (0.5°C uncertainty being equivalent to a 5% uncertainty in dark signal).

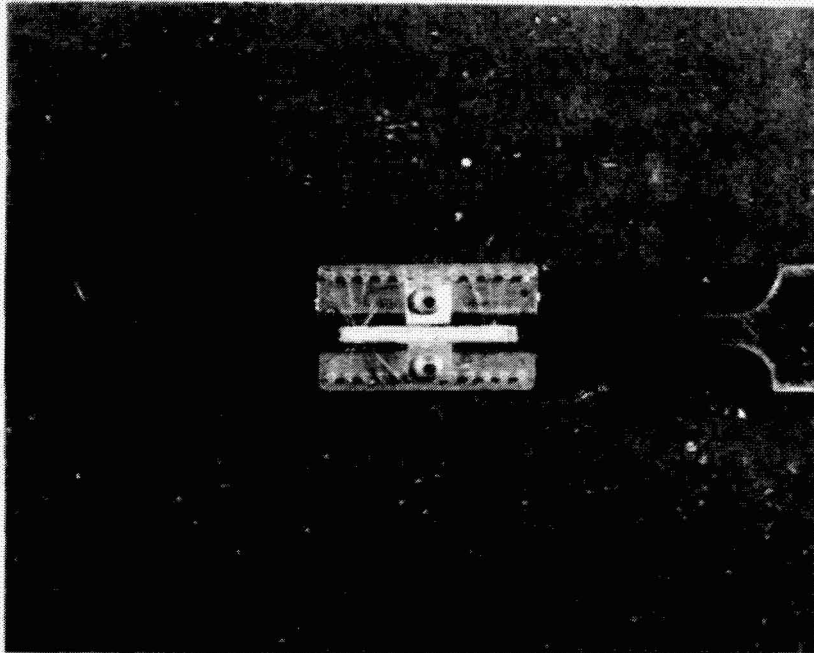
At the same time that dark signal measurements were made, the transfer efficiency of the even and odd registers was measured. Again, there was no correlation between strain and the measured transfer efficiency.

At a strain level of 1000 microinch/inch, the CCD broke from the mechanical stress. The CCD continued to respond to light (odd register only transferring charge) back to pixel number 1189.

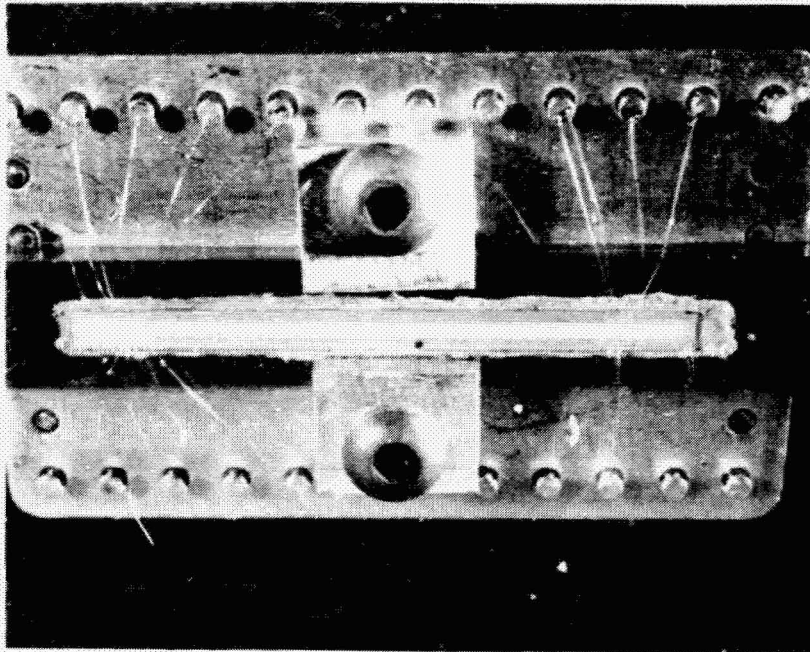
Figures IV-65a and 65b are photographs of the test CCD and tensile test bar used for the strain vs. ICCD performance tests described above.

The strain on the ICCD under test was determined indirectly. A nonworking ICCD was mounted to a tensile test bar with the same epoxy used to attach the functional ICCD (Epotek H-40, gold-filled epoxy cured two hours at 125°C). All samples were attached to a reactor grade zirconium test bar with a 0 inch x .200 inch x 4.00 inch long test section. A thin-film strain gage was then attached to the surface of the ICCD (a .030 inch x .030 inch gaging element) with Eastman 910 cyanoacrylate adhesive. This "calibration" specimen was then pull tested to get a tensile load to ICCD strain factor. The tensile load was normalized to a tensile stress (in the zirconium test bar) by dividing the load by the cross-sectional area of the zirconium bar. After each 50×10^{-6} in./in. increment of ICCD strain, the load on the tensile test bar was relaxed to zero and the residual strain was measured. Up to a 1000×10^{-6} in./in. strain application, the residual strain was 40×10^{-6} in./in. or less. This low residual strain indicates that the ICCD, test bar and epoxy bond line were not experiencing plastic deformation.

At an ICCD strain of 1050×10^{-6} in./in. the epoxy bond between the ICCD and the zirconium test bar failed near the ends of the ICCD during the "calibration" testing. This failure mode is the one expected because of shear stress concentration at the end of the composite beam (zirconium and silicon). The epoxy bond failed instantaneously



A) Circuit Including Zirconium Bar



B) Circuit Showing Test Wires

Figure IV-65 Dark Signal vs Strain Test Configuration

(with an audible snap) and resulted in a visibly bad bond and non-repeatable test measurements. Inspection of the dark signal test specimen. After straining up to 800×10^{-6} in./in. showed no evidence of epoxy bond failure, giving a high degree of confidence that the strain computed from the "calibration" data is correct within instrumentation and material relaxation uncertainties (approximately $\pm 20 \times 10^{-6}$ in./in.).

3. Packaging Conclusions.

Careful analysis of the materials being considered for use as a substrate with an ICCD will make it relatively easy to avoid mechanical stress related anomalies. The two ICCDs tested exhibited no measurable stress related problems until the stress levels were high enough to fracture the bulk silicon. Normal applications would not require more detailed analysis of the thermally induced stresses in the "bi-metallic" system than is presented in Section IV.C.1. A safety margin of three (i.e., limiting thermally induced strain to 300 μ in./in.) is certainly adequate to ensure satisfactory short-term device operation. In view of the non-ductile nature of silicon, this safety margin is probably adequate to avoid long-term degradation (creep, defect propagation, etc).

V. RELIABILITY DISCUSSION

The program test and analysis results show few failures that result from device degradation after initial screening tests. This program evaluates only six devices but the data discussion includes approximately 200 devices. The number of failures that were not related to handling was less than 2% when a failure is described as a catastrophic dropout or one which produced significant performance drift.

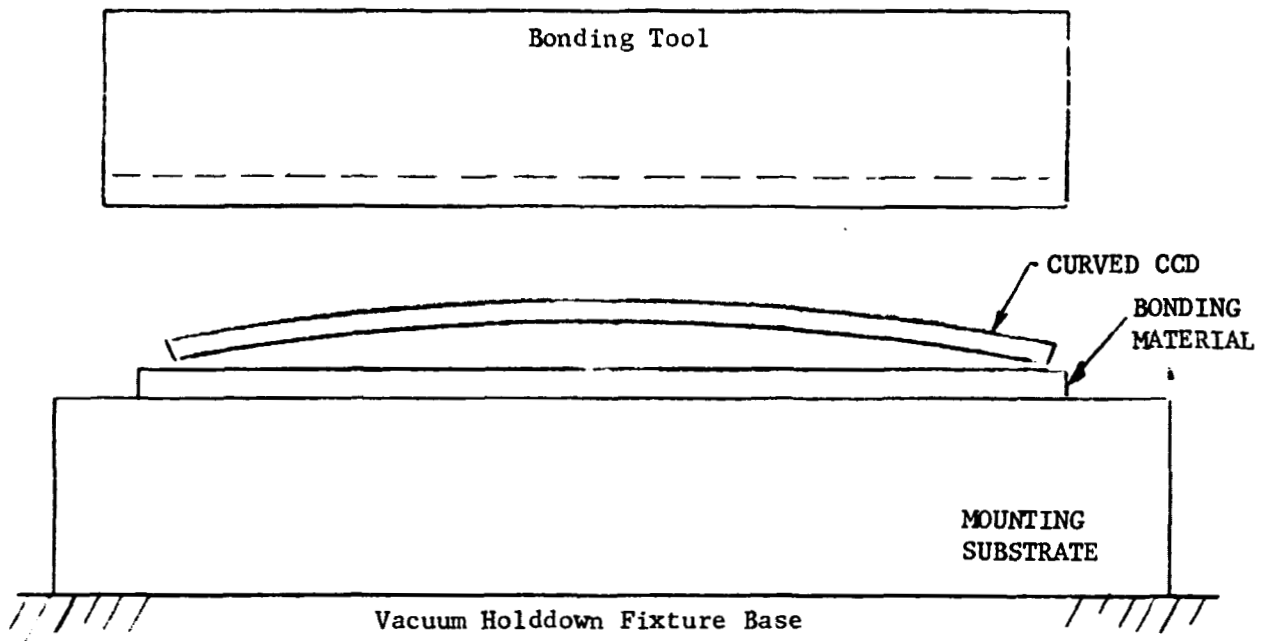
Much of the discussion in this section relates to defects that are produced in handling due to surface contact damage, improper application of drive signals and voltage levels and static discharge sensitivity.

A. FAILURE MODES

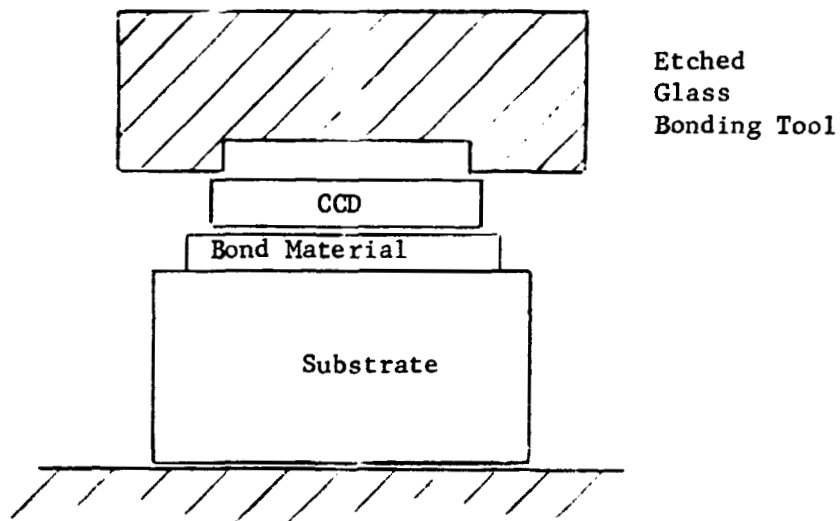
1. Mechanical Failure Modes.

- a) Excessive stress due to coefficient of expansion mismatch between the CCD and substrate (or header). This can become a serious problem especially with large CCD chips. The failure mode can be as extreme as chip microcracking but the most likely effects are conductor fracture, increased dark signal due to lattice structure strain and layer-to-layer shorts or leakage paths. Section IV addresses this subject in detail.
- b) Layer-to-Layer Shorting Due to Handling. The CCD121H has five conductive layers, which result in a relatively high degree of topographic variation. Normal handling practices for semiconductor chips allow the use of vacuum tweezers for picking up the die and allow the die to be laid upside down without concern. The CCD121H cannot be handled with vacuum tweezers. Several layer-to-layer shorts, especially between the first and second metal conductors, resulted from contact pressure from the tweezers. A soft rubber tip was added to the vacuum tweezer which significantly reduces the risk of damage.

Another interlayer shorting failure mode resulted because the long slender chips have about .002" to .004" curvature after scribe and break. When the device is used for imaging it is usually required to be flat to within a few microns of total curvature for optical focal plane reasons. This must be accomplished with tooling that flattens the device during die bonding yet does not contact the surface of the chip. A solution for this is shown in Figure V-1. The bonding material is screen printed gold-filled epoxy. The bonding tool is optically aligned to the CCD in a fixture that also registers the parts together. The glass tool only contacts the edge of



A. Side View



B. End View

Figure V-1 Die Bonding Tool; To Produce a Flat CCD

the CCD along both sides. Unfortunately, the CCD121H wire bonding pads are very close to the edge of the chip and also consist of two metal layers. A light shield over the chip is etched back to expose the wire bonding pads. The possibility of shorting is still present but to a much lower degree with fixturing of this type.

- c) **Wire Bonding Damage.** The multilayer shorting problem discussed above can also be aggravated by wire bonding processes. If the circuit uses wedge bonding, the machine capillary can easily contact the edge of the bonding pad (as shown in Figure IV-14) creating a multilayer short. Also, Fairchild has reported a historical concern for ultrasonic wire bonding due to what was believed to be microfractures or stress concentrations that produced added dark current. This has not been found to be a problem at Martin Marietta in special tests to evaluate the problem. Capillary tip damage has resulted several times, however, and is controlled by operator care in placing the wire bond.
- d) **Sensitivity to Moisture.** No failures have occurred due to this but it has remained a technical concern. The CCD light shield often can have small pinholes exposing underlying deposited glass. Moisture along with ionic contamination is considered a reliability concern especially since this device is very large with five layers of conductors. Problems such as leakage current, corrosion and migrated resistive shorts are all possible. Also, the dark signal performance can be affected by mobile ions in the silicon dioxide at the surface. This device is a sealed channel CCD but moisture along with pinholes could result in inversion layer and dark signal increases. In Section IV, several photos show surface metal pinholes which resulted from the top metal photoresist step. Inadequate coverage allowed undesirable pinholes to be etched in the light shield. As earlier stated, pinholes in the light shield are not a reliability concern except when moisture may be present.

2. Electrical Failure Modes.

- a) **Output Amplifier Shorts.** Several shorting problems have been examined and traced to a multiplicity of causes. These include shorts due to static discharge, handling damage and gate to-drain and gate-to-source shorting by a mechanism that is described as dendritic-like growth of polysilicon down through the silicon dioxide to the bulk silicon.

The CCD is generally considered very static sensitive due to its MOS type construction. The CCD121H has adequate protection networks for normal levels of static discharge energy on all the input gates. The output amplifier, however, is not fully protected. Terminals RD, OD, OS, and CS are all susceptible to low levels (see the functional schematic, Figure IV-13. Several failures have occurred where a high impedance short is created

between the output drain, OD, and the gate of either Q8 or Q12. These transistors have exhibited the highest degree of susceptibility for reasons not clearly understood. The conductive path is measured by setting OR to a positive voltage thus turning Q6 and Q7 on. The resistance may then be measured for a shorted Q8 or Q12 gate to drain. Scanning Electron Microscope photos have shown a clear indication of voltage breakdown. These and other static failures have occurred while operators were wearing conductive wriststraps and working on conductive surfaces. Extreme measures have been implemented to reduce this type of damage since earlier failures.

Another gate-to-drain failure mode is described as a "dendritic" polysilicon growth. This name is probably incorrect but because of the visual nature of the short, it has been likened to a dendritic growth. In at least three occurrences out of about 200 devices this mechanism for failure has shown up. It has not been traced to the actual failure cause. The circuits in each case have been operating in a normal manner prior to failing. It was thought that burn-in under reverse bias would enhance and activate this type of failure but this has not occurred. The failure cause is still being investigated.

- b) Polysilicon Shorts. This is a failure mode that has not occurred with the CCD121H after the devices have been previously operating normally. The process of thermally growing oxide on one polysilicon layer for insulation from the next polysilicon layer has been found to be highly reliable. No failures have occurred either in burn-in or other testing that were related to polysilicon layer shorting. In part, we believe that this is due to the fairly in-depth electro-optical testing that is performed by Fairchild on the devices at the wafer level. Additional performance tests were added over standard commercial wafer tests that have proved to be very effective screens.
- c) Dark Signal Change After Burn-In. Only five devices out of about 200 have shown a significant shift due to burn-in at 125°C for 168 hours. These devices may be normal devices that were incorrectly measured prior to burn-in. Subsequent retests have shown a reduction in the dark signal shift which would indicate the shift is real. To date this has not been explained. High temperature reverse bias testing should effectively screen this type of problem especially if it is related to mobile ions in the SiO₂ on the CCD. In general, the devices have exhibited exceptional stability after burn-in tests up to 1000 hours. This is true of responsivity, dark signal and noise. Section V.C addresses performance test data in detail.
- d) Voltage Overstressing. Input gates are 100% tested at 18 volts during wafer tests. The breakdown voltage exceeds 18 volts. No failures have resulted on this program from such overstressing. The mode must always be considered on multilayer devices,

For high reliability programs it is recommended that pin-to-pin and pin-to-substrate leakage current be measured and monitored for delta shifts. Several devices have been screened out due to leakage current on input gates.

3. Electro-Optical Failure Modes.

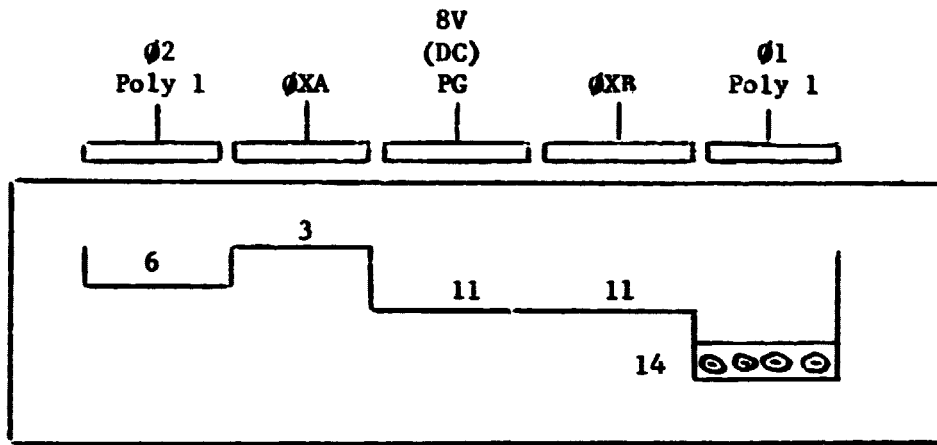
Some of the modes discussed in this section are the result of incorrect operating voltages and are not to be confused with reliability problems. The CCD121H will fail to perform in a given application if drive signal voltages and timing is incorrect.

- a) **Poor Low Light Level Response.** Figure V-2 shows the result if the photogate voltage is set too high (usually with the intent of increasing the signal handling capability). The figure shows a well under the photogate that is deeper than the well under the transfer gate. Some of the charge does not transfer to the shift register. A slow buildup in responsivity occurs for low light level as the photosites accumulate a background charge to fill the partial or residual well. The effects are most noticeable when the array is cooled when dark signal does not contribute as much to the background charge. The same effect can occur if other voltages are set incorrectly or if the flatband voltage or polysilicon work function voltage is not well controlled.
- b) **Odd-Even Unbalance.** This condition usually shows when the odd register, which transfers first, shows lower response than the even register response. It was determined that the odd register is missing some charge which finds its way into the even register. Figure V-2 would seem to indicate that a low photogate voltage should operate acceptably but with reduced dynamic range. However, this is not the case. Experiments show that with the photogate dropped to seven volts the first transfer will be incomplete with the second transfer taking the excess charge.

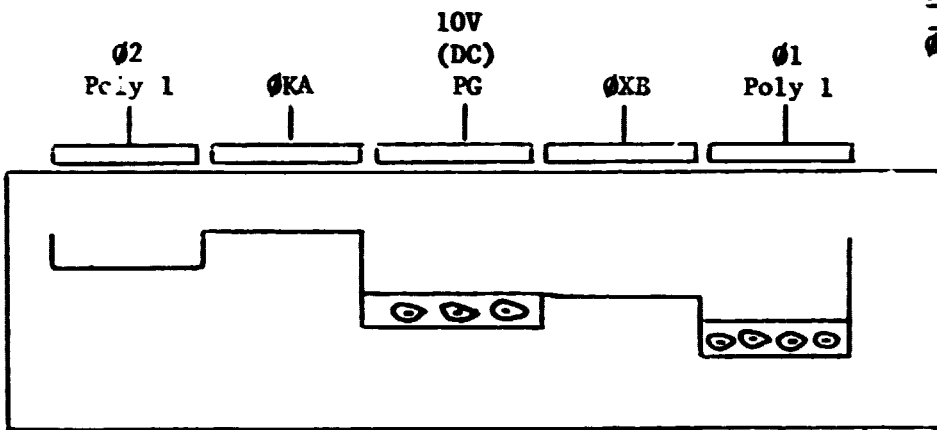
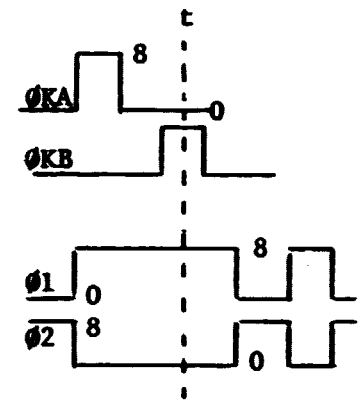
It is also believed that misalignment of the shift register overlap over the pixel channel stops will allow charge to bleed, or flow, around the stop and into the adjacent photosite.

The circuit designer should provide flexibility to allow trimming the operating voltages for optimum performance. The conditions often are normal and typified by existing CCD manufacturing tolerances.

- c) **Response Non-Uniformity.** This is often related to the previous two discussions but can be caused by other factors. For example, variations in the uniformity of the photogate can change the photon transmission. Also, defects such as ionic contamination in the silicon dioxide, bulk traps, silicon lattice defects, doping concentration variations and other causes can effect the response non-uniformity. The size of the



A. Correct Operating Voltages



B. Photogate Voltage Too High
(Incomplete Transfer Over Barrier)

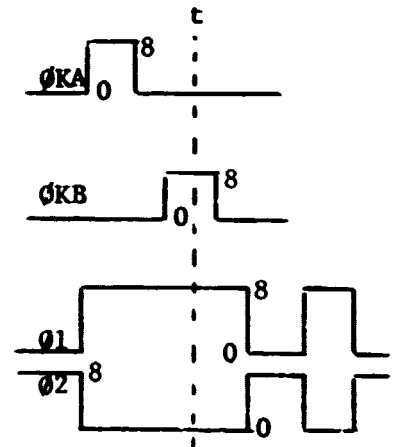


Figure V-2 Well Potential for Photosite Charge Transfer

CCD makes these variables more pronounced.

Typical performance data along with anomalous performance is discussed in Section IV including photographs of the various signal performance. Experience to date with the CCD121H has shown very few optical problems. From wafer-to-wafer and from run-to-run the variations occur as expected in a complex device.

In addition to the problem areas discussed in this section, other reliability concerns are presented in Section IV on construction analysis. CCDs are subject to typical problems such as contact window step coverage when aluminum is interconnected to polysilicon conductors. Some evidence of this is found on the CCD121H device. We have included failure mode concerns of this nature in the construction analysis that resulted from an examination per the criteria of MIL-STD-883B, Method 2018.

B. RELIABILITY CONCLUSIONS

The CCD121H, when properly screened for initially defective devices, can be characterized as a highly stable and environmentally resistant device suitable for use in the aerospace industry. The following conclusions have been drawn from this study program:

1. Metallization interconnects would generally meet MIL-STD-883, Level B, criteria exhibiting good adhesion, fair to good step coverage in contact windows and well controlled delineation.
2. Polysilicon layer-to-layer shorting is not a problem. Because of the very high density of conductors, however, it is recommended that for high reliability applications, screen testing be evaluated carefully to effectively separate out weak parts. Specifically, burn-in should be increased from 168 hours to 240 hours and if possible, be performed at 150°C. More detailed examination of the burn-in circuit must be performed to identify worst case reverse bias combinations. This should occur with heavy emphasis on the chip construction and layout to achieve maximum layer-to-layer bias effects during the burn-in.
3. Eutectic die attach is recommended only when the coefficient of expansion differences between the chip and header or substrate are carefully evaluated. Also, operating and nonoperating temperature extremes for each application should be evaluated prior to selecting a eutectic die attach.
4. Metal-to-metal shorting is a serious yield problem in that the chip is so large (approximately 1 inch long) that is essentially not inspectable for micro damage due to handling. Microfractures on the chip surface can occur during many final wafer processing steps, wafer testing, scribe and break, cleaning, inspection, die bonding and wire bonding. The parts often short with no visible damage to

the top light shield aluminum because the topography has many high spots for contact stress concentrations. In many cases failures existed that were not evident during detailed high magnification examination of the surface aluminum.

This problem is reduced to one of handling controls and in-depth screening. Its effect is on yield and not reliability if the screen testing is thorough.

A significant improvement would be to change the upper light shield to a non-conductive material. This is recognized as a difficult task in that this shield must be opaque to essentially all light in the visible and near infrared wavelengths. It also must be suitable to normal photolithographic processes for delineation.

5. Electrical and optical parameter stability is excellent.
6. Variables in wafer processing result in the inability to use fixed level voltages on clocks and other control gates. This should not be a problem except in particular applications requiring high resolution at very low light levels. The necessary work-around is to provide voltage trimming capability for at least the photogate, the output gate and transfer gate clocks.
7. Surface oxidation resulting from an unknown process variable producing wire bonding problems. The problem was corrected by a buffered etch cleanup of the oxide contamination. A recommendation for high reliability applications is to incorporate some degree of wafer discoloration (stain) inspection and to subsequently store wafers or chips under well controlled, dry nitrogen conditions.
8. The user should incorporate external electrostatic discharge protection networks for the RD, OD, OS, and CS outputs. The results of this program indicate that extreme measures must be taken to protect the output amplifier circuit.
9. The user requiring long life and high reliability should incorporate a sampling plan for SEM analysis of conductor interconnects, step coverage and general mask alignment evidence. In many cases, the requirements of MIL-STD-883 for SEM inspection are not related to CCDs with regard to mask alignment. If shift register electrodes are poorly aligned, transfer efficiency problems and response nonuniformity can result.
10. High reliability users should strive for a representative electro-optical wafer test program at application frequencies or be prepared to screen devices for application particular characteristics.
11. Applications for use in hybrid circuits require special emphasis on parameter versus temperature relationships. Wafer testing is practical only at room temperatures. Actual applications are often at cooled temperatures. Our experience shows that an occasional

circuit will not perform per an expected temperature relationship which constitutes another packaging yield factor. The optimum program would include an interim or temporary packaging and testing program prior to hybrid packaging.

VI. RECOMMENDATIONS FOR ADDITIONAL RELIABILITY EVALUATION

This preliminary study of CCDs has provided considerable insight into the construction and performance of commercial imaging device. It is recommended that this information be expanded to include reliability data resulting from stress tests of longer term duration similar to MIL-STD-883, Method 1016. The predominant failure mechanism encountered in this study has been metallization layer-to-layer shorting. However, these devices are certainly subject to the usual MOS failure mechanisms as well, which are related to the materials, processes, handling, and applications involved. Unique failures may be induced additionally by high stress testing, which would be peculiar to the device processing and construction. Table VI-1 lists failure mechanisms which may be encountered and the stresses which induce them. It is noted that the principal stresses are high temperature operation and temperature cycling.

Approximately 40 devices should be entered into the program in order to obtain statistical significance and confidence in the results. This would be very costly for a device such as the CCD121H. It is suggested that a device such as the CCD321 shift register be utilized. This device is a logical choice in the interest of economy and it is fabricated with the same types of processes and techniques as the CCD121H. It is believed, therefore, that the same inherent failure mechanisms will be evident in both devices.

It is important that baselines be established on the test items in order to document the performance and quality level as well as the process/design configuration being evaluated. Therefore, the parts should be screened to a standard level such as MIL-STD-883, Method 5004, Class B. The process/design baseline should also be documented by a construction analysis which should be enhanced by manufacturer supplied information to the extent possible.

The purpose of this evaluation is to induce and accelerate the mechanisms of failure. In this manner the design strengths and weaknesses can be assessed. When the strengths and weaknesses have been established, it will be possible to identify the tests (such as burn-in circuits and temperatures) suitable to properly apply in accepting, selecting, and specifying high quality devices. The weaknesses may suggest recommended changes to device design and construction which would upgrade reliability. Also, the weaknesses or capability limits would provide information useful for applications, such as derating guidelines. Characterization and preliminary temperature characteristics test are recommended for the purpose of identifying test parameters and limits in the program and to identify circuit conditions and temperature levels in the ensuing high temperature life test.

In addition to high temperature operation and temperature cycling tests, a number of parts should be subjected to overvoltage tests to

Table VI-1

PROBABLE FAILURE MECHANISMS

FAILURE MECHANISM	TYPE OF FAILURE	INDUCING STRESS
Drift	Infant/Wearout	High temperature bias, electrical, electro-optical, and operating life
Oxide Defects (including contamination)	Infant/Random	High temperature bias, electrical, and operating life.
Electromigration	Wearout	High temperature bias, electrical, and operating life.
Microcracks	Random/Handling	Temperature cycling and SEM.
Shorts between Electrodes (surface and interlevel)	Random/Wearout/ Handling	Temperature cycling destructive physical analysis, operating life and SEM.
Metal Shield to Electrode Shorts through Passivation	Random/Handling	Temperature cycling and operating life.
Polysilicon Shorts	Random	Temperature cycling and operating life, and voltage overstressing.

assess the capability to withstand voltage overstressing.

It is also important that failure analyses be performed at each stage in the test sequence in sufficient depth that all mechanisms are understood. It may not be necessary to analyze every failure or to analyze to the same degree of depth in every case, but the mechanisms must be understood and the likely modes established.

The existing study, when supplemented by this recommended reliability study, will provide a data base for BCCDs in general and the CCD121/CCD321 types in particular. It is suggested that SCCDs be evaluated also for the purpose of comparison of these two technologies.