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(NASA-CR-159439) ADAPTATION OF ION BEAM TECHNOLOGY TO MICROFABRICATION OF SOLID STATE DEVICES AND TRANSDUCERS (Case Western Reserve Univ.) 40 p HC A03/MF A01 CSCL 20L

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ADAPTATION OF ION BEAM TECHNOLOGY TO MICROFABRICATION OF SOLID STATE DEVICES AND TRANSDUCERS

PREPARED FOR NASA LEWIS RESEARCH CENTER

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16. Abstract

A number of areas have been investigated to determine the potential uses of ion beam techniques in the construction of solid state devices and transducers and the packaging of implantable electronics for biomedical applications. The five areas investigated during the past year are:

A. Tests were performed on diode like devices fabricated on textured silicon.
B. A photolithographic technique was developed for patterning ion beam sputtered PVC.
C. The use of sputtered teflon as a protective coating for implantable pressure sensors was investigated.
D. Work has been initiated on the sputtering of Macor to seal implantable hybrid circuits.
E. Preliminary studies on the use of sputtered teflon to immobilize enzymes has begun.

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ADAPTATION OF ION BEAM TECHNOLOGY TO MICROFABRICATION OF SOLID STATE DEVICES AND TRANSDUCERS

I. Introduction

In the microelectronics field, ion beam milling systems are seeing greater use due to the potentially improved control over line widths and the reduction of undercutting as compared to conventional wet chemical etching. Another indication of the growing interest in this fabrication technique is the increase in the number of commercially available ion beam milling systems. Some of the companies now offering such equipment are Veeco, Commonwealth Scientific, Ion Tech Inc., and Technics.

The work being pursued under this grant can be classified into two categories which are of a different nature than the commonly used ion milling technique. They are (1) a study of textured silicon surfaces and how their properties can be used for the fabrication of semiconductor devices, and (2) the sputtering of unconventional materials, as far as solid state processing is concerned, such as teflon, polyvinylchloride, and Macor (a machinable ceramic developed by Corning) for use as protective coatings for microelectronic biological implants or as membranes for chemical sensitive electrodes.

The characterization of the silicon texturing process is being carried out at NASA Lewis and is not a part of the work reported here.

In addition, the development of the ion beam sputtering technique for the various materials has been or is being carried out by NASA Lewis personnel.

This report will cover the following areas:

A. Tests on diode like devices fabricated on textured silicon.

B. The development of a photolithographic process for sputtered PVC.

C. The use of sputtered teflon as a protective coating for implantable pressure sensors.

D. The sputtering of Macor to seal implantable hybrid circuits.

E. The use of sputtered teflon to immobilize enzymes.

Progress in the various areas which will be covered has been slower than one would like due to the fact that we have to rely on the personnel at NASA Lewis for all of the ion beam sputtering that is done. Because of the many projects with which they are involved the turn around time for our work is understandably delayed. In order to overcome this problem we intend to purchase a commercial ion beam etching and sputtering system. The funds for this equipment will be provided from other grants which stand to benefit from the development of these ion beam techniques.

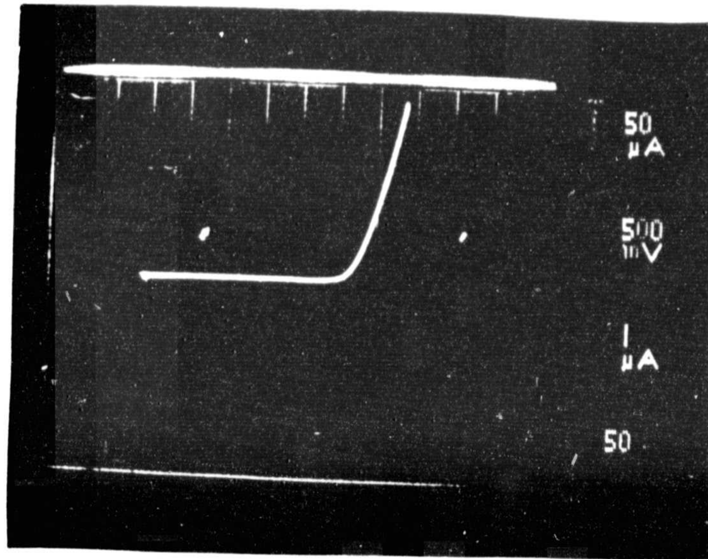
II. Ion Beam Textured Silicon

In the progress report for 1977 (NASA CR-135314) it was shown that textured silicon can be used to increase the effective surface area of

MOS capacitor by a factor of two to three. The one detrimental feature of the devices was their premature voltage breakdown. This was especially true when the top aluminum electrode was biased positively with respect to the silicon substrate. Test results showed that the breakdown voltage could be substantially increased if the aluminum and silicon dioxide were etched off and the wafer reoxidized. These capacitors, however, did not have as large an increase in the effective surface area because the cones and ridges which resulted from the texturing process were partially consumed by the oxide growth.

What has been investigated this past year is the potential fabrication of a majority carrier diode like device using what appears to be field emission of electrons from the silicon peaks. The field emission of electrons is at this time an unproven hypothesis but it is a reasonable assumption when one considers the high electric field which would exist in the vicinity of the silicon peaks. Figure 1 shows the current versus voltage characteristic of an MOS capacitor fabricated on textured silicon. This is the same as Figure 2 in last years progress report (NASA CR-134314). Not all of the devices tested exhibited these diode like characteristics. Some of the capacitors tested showed large reverse currents as well as the diode like current in the forward direction. (By forward direction is meant the aluminum is positive with respect to the silicon.)

To obtain some insight into why such field emission might occur one should look at Figure 2. From this sketch it can be seen that there will be regions along the oxide silicon interface where the electric field can be large. The reason that the current flow is not



I-V CHARACTERISTICS FOR A "CAPACITOR"
ON THE TEXTURED SURFACE OF A-7

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FIGURE 1.

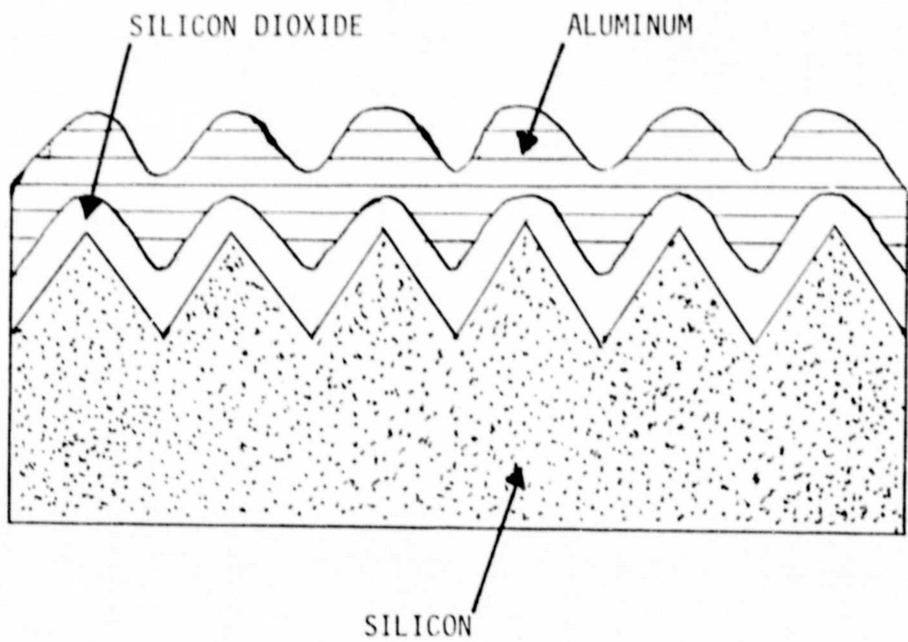

FIGURE 2. Cross Sectional Drawing of Oxidized and Metallized Textured Silicon Surface.

symmetrical with respect to voltage is not quite clear and no theoretical work has been pursued at this time. One possible explanation is that the aluminum oxide interface does not have as sharp points due to the rounding and smoothing effect of the oxidation process.

In order to try and gain more insight into the phenomena one silicon wafer, textured at NASA Lewis, was processed as shown below and then tested.

1. Wafer was degreased and cleaned using our standard semiconductor cleaning procedures.
2. An oxide layer was formed on the textured wafer by applying a solution called "Silicafilm" to the surface of the wafer and spinning at 3000 rpm. It is a mixture of SiO_2 in an alcohol solution and must be baked at an elevated temperature to drive off the solvent. This wafer was baked for 15 minutes at 200° C in air. The "Silicafilm" was purchased from the Emulsitone Company.
3. The wafer was then annealed for 15 minutes at 1000° C in nitrogen to further densify the oxide layer. This spun on film then has the dielectric and optical properties of a pyrolitic oxide. The oxide thickness should have been approximately 2000Å but it is difficult to measure because of the textured surface.
4. 2000 Å of aluminum was evaporated on top of the

entire wafer and patterned using standard photolithographic techniques. This resulted in aluminum electrodes of two sizes and shapes. Half of the devices were made with circular electrodes 32 mils in diameter and the other half with square electrodes five mils on a side.

5. The back side of the wafer was etched in buffered HF to remove any oxide that may have grown and then coated with aluminum for good external electrical contact.
6. The metallized wafer was sintered for 15 minutes at 480^{0} C in forming gas (a mixture of 90% nitrogen and 10% hydrogen) to insure good electrical contact between the silicon and the back side aluminum.

This fabrication sequence should have resulted in structure similar to the sketch shown in Figure 3. Notice that there are no longer valleys where the aluminum can come to a point.

Results from tests on these devices is shown in Figure 4. Figure 4 (a) is a typical current versus voltage characteristic for one of the small square devices. As the photo shows the forward turn on voltage between 300 and 400 mV, is fairly sharp and the reverse leakage current is much less than one micro-amp. The I-V characteristics shown in Figure 4(b) are for the larger circular device. As this photo shows the larger device has a softer forward turn on characteristics and much larger reverse leakage current. Even if the difference in area is taken into consideration it cannot account for the excessive leakage current of

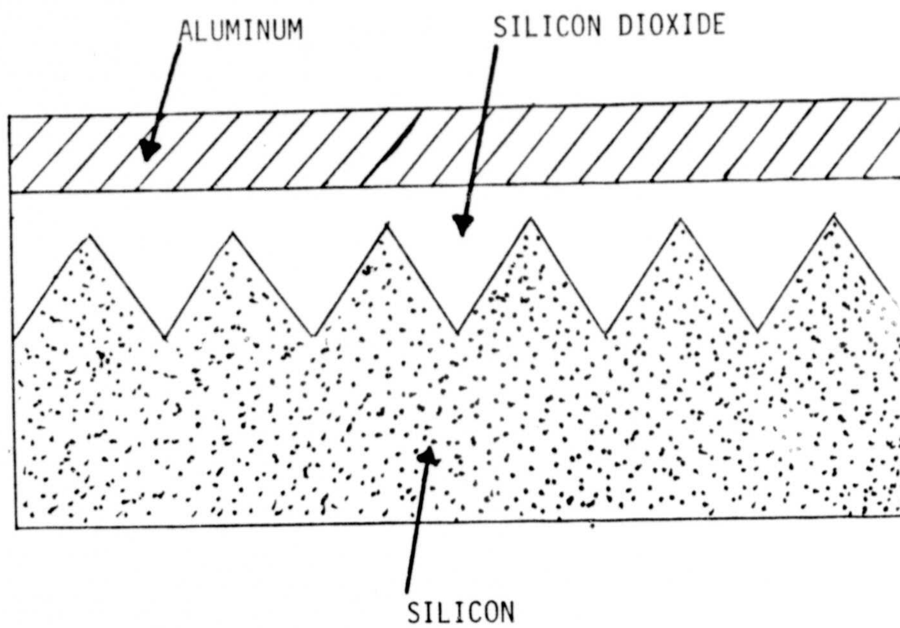

FIGURE 3. Cross Sectional Sketch of Textured Silicon Covered With Spin On Oxide.

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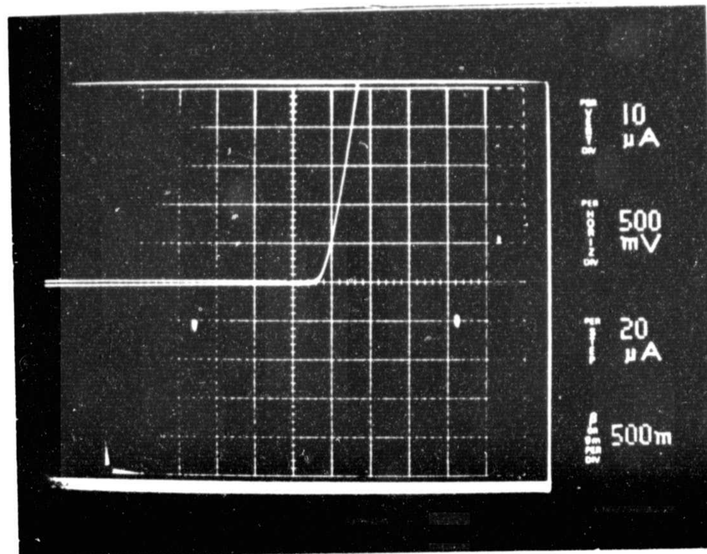
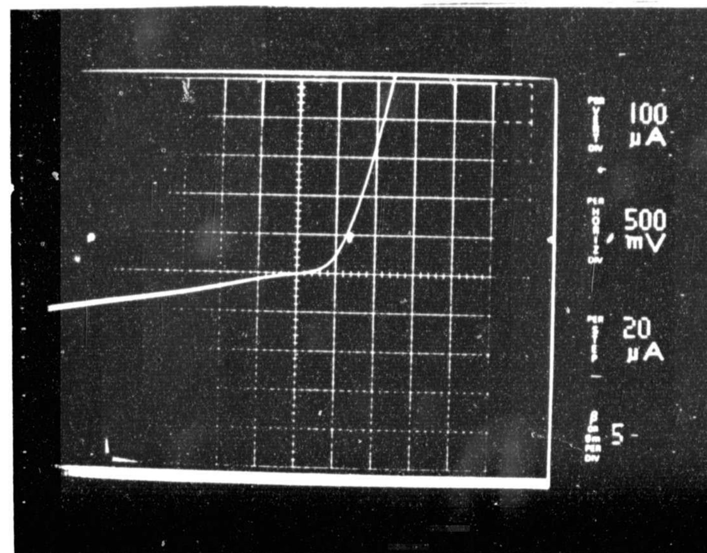


(a)



(b)

Figure 4. Current versus voltage characteristics for (a) small square device and (b) large circular device.

the larger device. If we take the 100μA leakage current at -3 volts and divide it by the area ratio (32) we should see approximately 3μA leakage for the small device. This would easily show up on the photograph taken, but it does not. One possible explanation is that there are some type of low density randomly distributed defects in the oxide layer which contributes to the reverse leakage current. Because of the low density of the defects the small devices are less likely to include such a defect than a larger device. Thus for a random probing of devices, more small devices are likely to exhibit low reverse leakage than large devices.

For the tests discussed above, no thermal oxide was grown because of the desire to maintain the silicon surface in it as textured condition. For the next set of tests it was desired to have a thin thermal oxide over the entire surface that could possibly reduce the excessive reverse leakage current. Therefore, after the first set of tests, the wafer was stripped of all aluminum and the oxide layer etched off. The wafer was then thermally oxidized for one hour at 1050°C in oxygen. This oxidation process typically results in 1000Å of oxide but again because of the textured surface no accurate measurement could be made. After the thermal oxidation two coats of the "Silicafilm" were spun on and densified as discussed above. This process sequence would normally give a uniform layer of silicon dioxide approximately 5000Å thick but because of the rough surface there will most likely be large variations in thickness between the valleys and the peaks which should have enhanced the forward current with respect to the reverse current.

After metallization,photolithography and sintering,tests were performed on both the small and large devices. The oxide layer on these devices, unfortunately, was too thick and no diode like characteristics could be obtained. All devices, large and small exhibited destructive dielectric breakdown at between 20 and 30 volts. No further experimentation has taken place since we have not been able to obtain additional textured wafers.

III. Ion Beam Sputtering of PVC

In the previous progress report, results from a potassium sensitive field effect transistor fabricated using ion beam sputtering were presented.[2] Those devices were processed using standard semiconductor fabrication techniques except that no metal gate was formed over the channel oxide. In place of the metal gate, a potassium sensitive membrane, consisting primarily of polyvinyl-chloride and valinomycin, was ion beam sputtered over the double dielectric consisting of a thermal oxide and a vapor deposited silicon nitride layer. On these devices the membrane was sputtered over the entire device. No attempt was made to leave the membrane over only the active channel area of the device.

If in the future multiple sensors, each sensitive to a different ion, are to be fabricated on the same chip,then a photolithographic patterning process must be developed for each membrane.

The first step which was taken to develop such a process for sputtered PVC was to determine what masking agent would stand up to either tetrahydrofuran or methylene chloride, both solvents for PVC. The photoresist which we use in our processing lab (Shipley

AZ 1350V) was quickly removed by both solvents and thus could not be used as a mask.

The next material to be investigated was vacuum evaporated aluminum. The aluminum is easily patterned, and previous tests showed that there was no observable or measurable degradation of the sputtered PVC layer by the evaporated aluminum. It was also determined that the aluminum could be removed with HF without affecting the PVC. The evaporated aluminum was not attacked by either the tetrahydrofuran or the methylene chloride. However, neither was the sputtered PVC film. When either tetrahydrofuran or methylene chloride was applied to the PVC on the sputtering target it began to dissolve immediately. A silicon wafer covered with the sputtered membrane was soaked for more than three hours in tetrahydrofuran without an observable change in the membrane. Similar tests were performed(xylene, benzene and HCl--all chemicals which attack PVC) but they too had no effect on the sputtered PVC.

To avoid the problem of finding an etchant for the sputtered PVC the "lift off" technique was tried. This method involves coating the substrate with photoresist prior to the deposition of the material to be sputtered. After the photoresist is applied it is exposed and developed as usual but now it remains over the areas of the wafer where one wishes to remove the deposited material and it is absent in those areas where the deposited material is to remain. Figure 5 is a sketch showing a cross sectional view of the relationship between the substrate, photoresist, and the material to be

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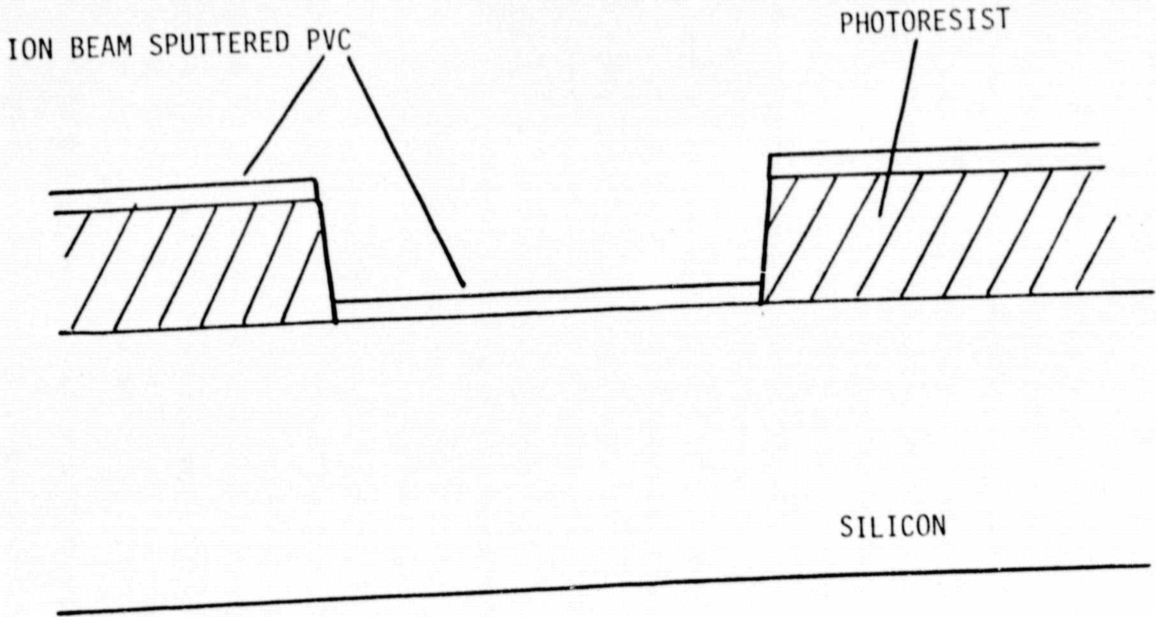

FIGURE 5. CROSS SECTION SHOWING RELATIVE THICKNESSES FOR LIFT-OFF TECHNIQUE.

patterned. The reason that the technique works so well is due to the fact that the photoresist is much thicker than the material which is deposited on top of it. The steps in photoresist are so large that the thin line of sight deposited film cannot come close to adequately covering that step. Thus when the wafer is put into the photoresist solvent, the photoresist under the deposited film is quickly undercut and the film lifts off.

The results reported here were from wafers which underwent the following steps.

1. Bare silicon wafers were degreased and cleaned using our standard procedures.
2. Photoresist was spun on the wafers at 3000 rpm which resulted in a photoresist thickness of approximately 2.5 microns.
3. The photoresist was patterned and developed using the mask shown in Figure 6(a). The photoresist is not hard baked to facilitate its removal.
4. PVC was sputtered over the entire wafer with the following parameters:

   Time 42.5 hr.

   Energy 300 eV

   Beam Current 20mA

   Thickness 1800Å
5. The PVC was lifted off by spraying acetone over the wafer.

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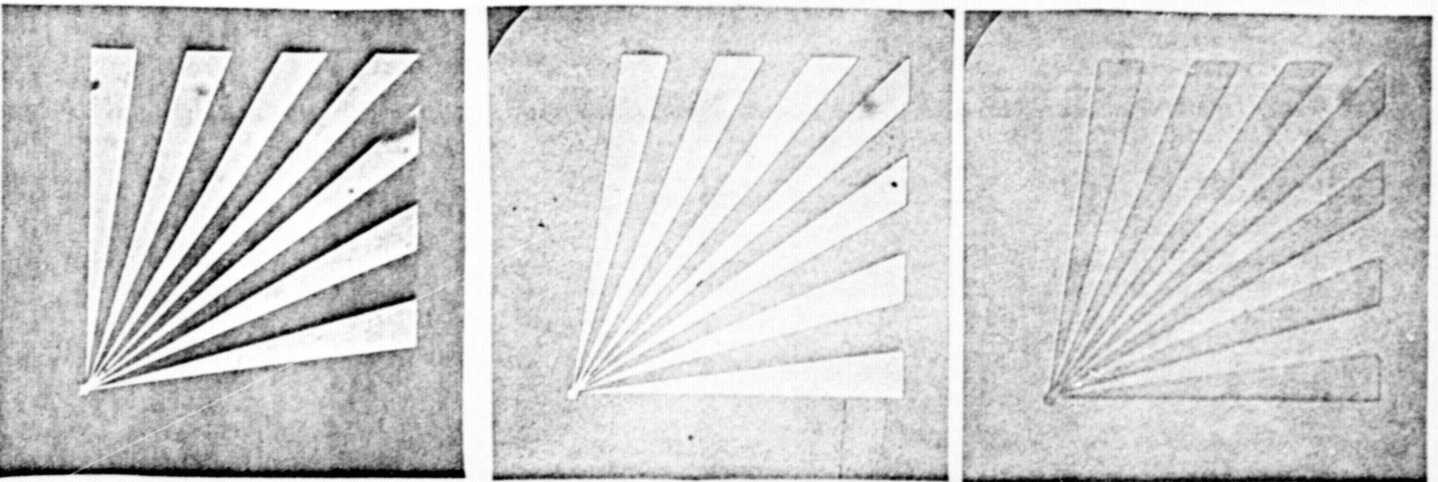


EMULSION MASK

(a)

PHOTORESIST AND PVC

(b)

PVC

(c)

FIGURE 6. PHOTOMICROGRAPHS OF SAMPLES USED FOR LIFT OFF EVALUATION.

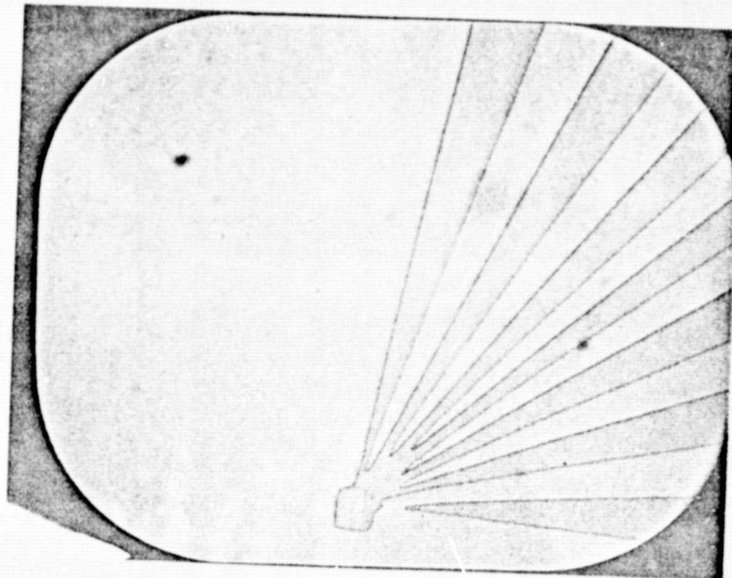
Figure 6(b) is a photomicrograph showing the photoresist after being patterned and coated with the sputtered PVC. Figure 6(c) shows the patterned PVC on the bare silicon. Figure 7 shows a X400 magnification of a portion of the patterned PVC. It is easily seen that dimensions smaller than 1 mil are adequately reproduced.

IV. Ion Beam Sputtered Teflon As A Protective Coating For Miniature Pressure Sensors

A miniature solid state pressure sensor is currently being developed at the Engineering Design Center of CWRU primarily for medical applications. The development of this device has been aimed at overcoming a number of difficulties related to medical transducers. These difficulties include long-term stability, pressure and temperature hysteresis, cost, bio-compatability and packaging. The approach to these problems has been to develop a total system consisting of a packaged sensor, and interface electronics for a wide variety of applications.

The problem which has been the most difficult to solve is that of finding a suitable material with which to coat the device. The material or materials used must not increase the volume of the device significantly, it must have good mechanical strength without being stiff, it must adhere well to the device, it must be an electrical insulator, it must be biologically compatible and finally it should be impervious to moisture.

Our present technique for assembling and packaging our pressure transducer is shown in Figure 8. The pressure sensor itself consists of two identical silicon chips with cavities etched into the back side.



PVC ON SILICON

1 MIL

FIGURE 7. 400 X MAGNIFICATION OF PATTERNED PVC ON SILICON.

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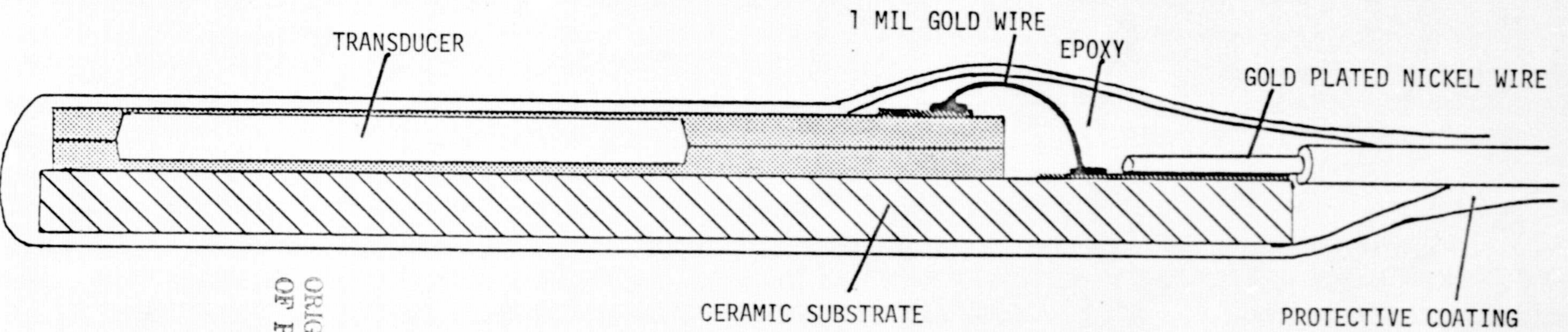

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FIGURE 8. Pressure Sensor Packaging, Cross Sectional View.

An anisotropic etch is used to form the cavities which results in good control over both the shape and the size of the cavity. These two chips are then sealed back to back in a vacuum using a gold -tin perform. The device is sealed in a vacuum to eliminate any temperature effect due to air that would otherwise be trapped within the cavity. The sealed device is then attached to a ceramic substrate by means of a small drop of silicon rubber. One mil gold wires are then thermocompression bonded between metal pads on the chip and gold pads which were screen printed on the ceramic prior to the gold wire bonding. Four teflon coated gold plated nickel wires were welded to the gold pads on the ceramic to provide external connections. The original design had the external leads welded to the silicon but the silicon proved to be too brittle with the result that the leads were easily broken off.

After assembling the device in the above manner; epoxy is placed around the end of the ceramic where the wires are attached as well as overtop the 1 mil gold wires. This epoxy helps to provide mechanical strength. After the epoxy has cured a protective coating is placed around the entire device. Of the materials studied, the most promising have been the polymers; Kraton, Epcar, Polyurethane, Silicone Rubber RTV, silicon filled epoxy.

Non of these materials, however, has been entirely satisfactory for long term protection from fluid leakage while maintaining all other necessary properties. Some were too stiff thus reducing the pressure sensitivity of the device. Others had poor mismatches in thermal expansion coefficients resulting in large temperature coefficients. Still others did not adhere well to all of the surfaces involved.

To date RTV has given the best over all results.

Since one of the surfaces which the protective layer must bond to is the teflon coating on the lead wires, we have begun to investigate the use of ion beam sputtered teflon as a protective coating. Because the sputter coating process is a line of sight operation it would not be sufficient to simply place the pressure transducer in the sputtered beam. In order to obtain a relatively uniform coating over the entire device, it is necessary to "rotate and wobble" the device during the sputtering process. Figure 9(a) is a diagram showing the direction of rotations with respect to the incident sputtered teflon beam and Figure 9(b) is a photograph of the jig which was constructed. Not shown in the photograph is the motor which causes the sample to rotate around the large gear at 60 rpm and rotate around its own axis at approximately 120 rpm. The gears are not exactly in a 2:1 ratio and this removes any synchronization between the two rotations.

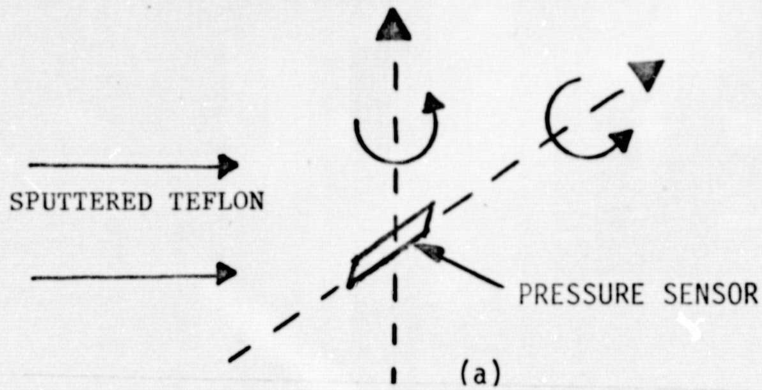
To date three pressure sensors have been coated with the sputtered teflon and then tested in saline solution. All devices were coated under the same conditions except for time. The sputtering parameters are given below.

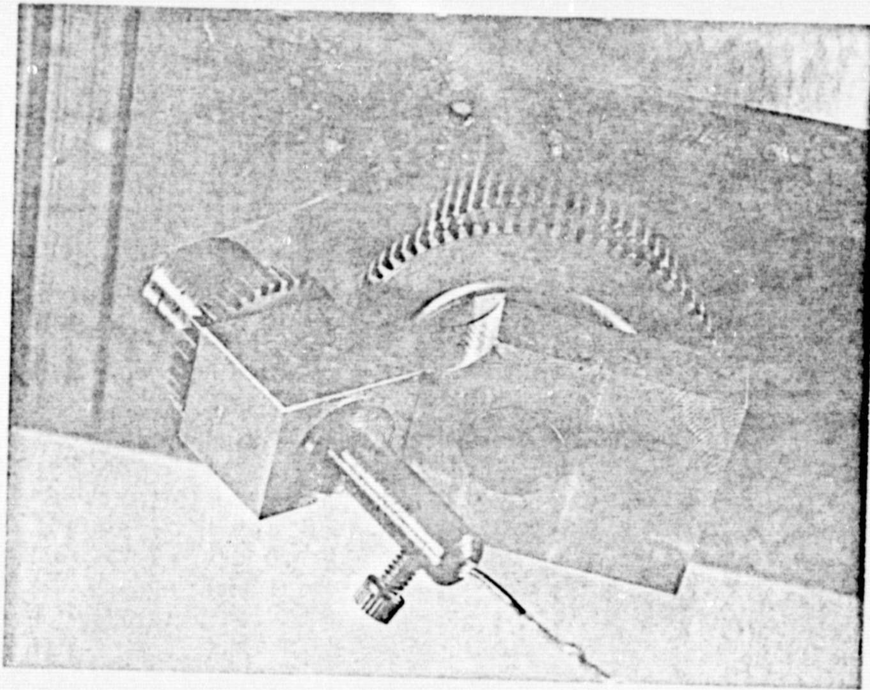
Target material - PTFE

Sputtering Ions - Argon

Beam Current - 110mA

Beam Energy - 1000eV





(b)

FIGURE 9. (a) Diagram and (b) Photograph of Jig Used to Coat Pressure Sensors With Sputtered Teflon.

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Exposure Time

A-95 min

B-95 min

C-4 hr. 45 min.

Sample A consisted of a pressure sensor packaged as described above and shown in Figure 8 except that the RTV coating was left off. After the sputtering process, approximately 5200 Å of teflon was deposited over the device. When the device was immersed in saline solution and the transducer bridge output monitored, it was found that the device failed immediately.

Sample B which had an RTB protective layer was sputtered coated in the same manner as sample A. This device survived approximately 3 hours in saline which is below the average for RTV coated samples, but it is within the statistical distribution which we have measured.

Sample C was a device without the RTV coating but it was sputter coated with approximately 1.5 microns of teflon. This device lasted for more than two hours before failure.

The results so far are not encouraging but it is too early to terminate the investigate. One of the things to look at is sputter cleaning of the device before deposition to improve adhesion. This is important because we know that teflon absorbs moisture but if it can be kept from accumulating at any of the interfaces electrical conduction will not take place.

V. Ion Beam Sputtered Macor

This area of investigation, like that discussed in the previous section, is aimed at improving the packaging method for an implantable

RF powered multiple channel muscle stimulator. The package as it is now being used is shown in Figure 10. As the figure shows, many different materials are used in an effort to keep moisture away from the electrons. The main portion of the package is made from a machinable glass ceramic called "Macor" which is produced by Corning. The "Macor" is impervious to moisture but the problem which we have yet to solve is finding a method of sealing the Macor lid to the base and at the same time providing a moisture barrier. Since the electronics are RF powered a solder seal cannot be used since the metal solder ring would act as a short circuit secondary to the internal coil. Work is proceeding on the use of laser sealing, and solder glasses but those techniques have yet to be perfected.

What we hope to do with the sputtered Macor is coat the rim of the Macor package after the lid is sealed on with epoxy. If the sputtered Macor is as impervious to moisture as the target material then seepage through the epoxy seal will no longer be a problem. Ion beam sputtering has to be used because we wish to keep the electronics inside relatively cool during the deposition process and this is not easily done with conventional RF sputtering.

The work which is currently being done is aimed at determining the sputtering parameters for the Macor. The next step is to determine how impervious is the sputtered Macor to moisture. This will be done by sputter coating a thin layer of easily corroded metal on a Macor substrate. The three layer structure will then be subjected to saline solution. The final step would be to coat the rim of an actual implantable system and test it.

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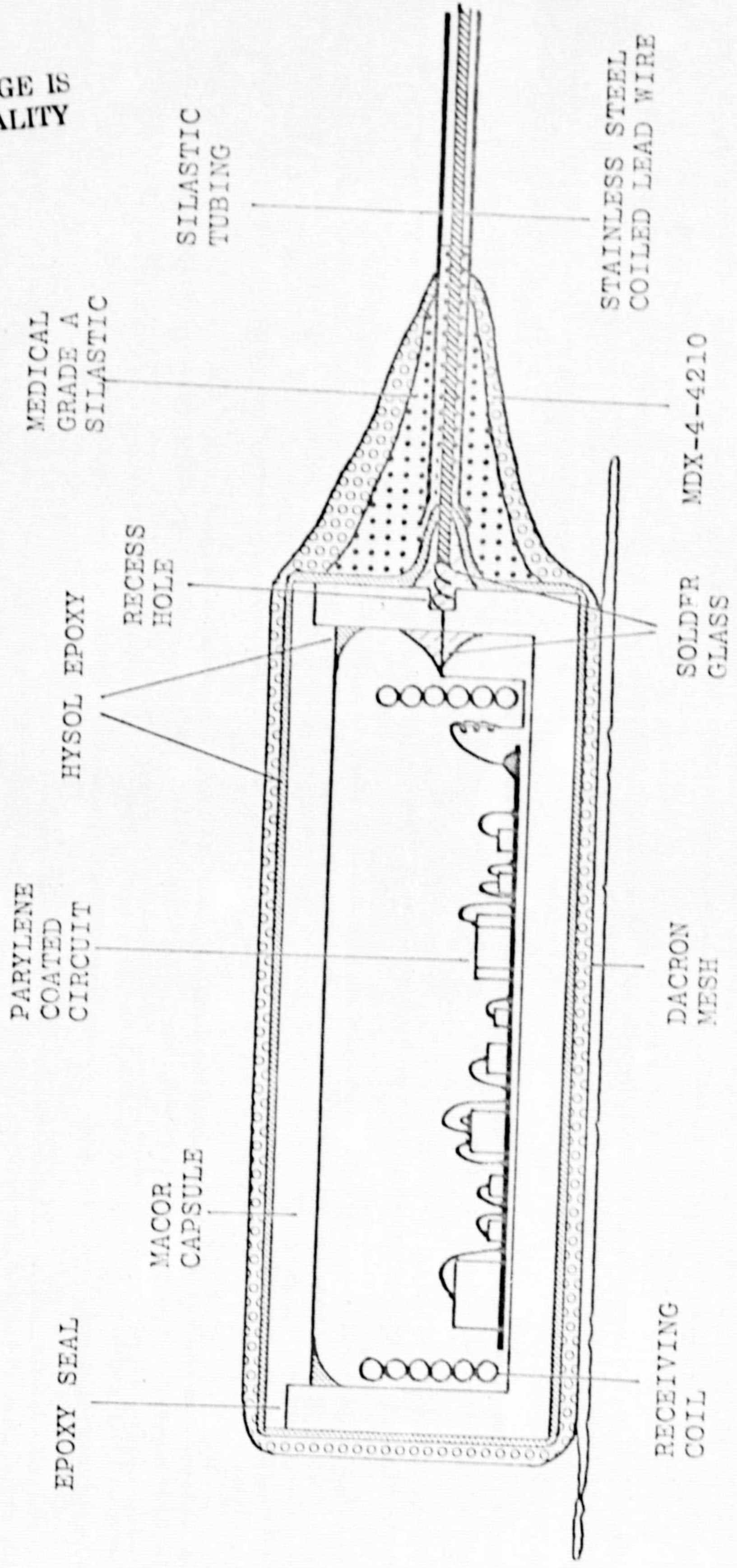

FIGURE 10. ENCAPSULATION OF IMPLANT STIMULATOR (NEW DESIGN)

VI. Sputtering of Teflon To Immobilize Enzymes

The immobilization of enzymes is a rapidly advancing scientific endeavor. The highly selective catalytic characteristics of enzymes are very attractive in many chemical and biological reactions. The reasons for immobilizing enzymes are as follows:

(1) Immobilized enzymes can exhibit selectively altered chemical and/or physical properties which are more desirable.

(2) Immobilized enzymes can be used in vivo for biomedical applications.

(3) Immobilized enzymes offer a considerable operational advantage over freely mobile enzymes.

At present, enzyme immobilization is done either by physical entrapment or chemical covalent bonding [3-6]. Physical entrapment is usually done using a polyacryamide gel. The major disadvantage of gel entrapment is that the gel is at best many mils thick and the gel matrix inhibits the diffusion of the substance of interest. Consequently, the response time of the enzyme reaction becomes very long. Covalent bonding of an enzyme usually requires a bi-functional chemical such as glutaraldehyde. In such a bonding process, the active sites of the enzyme will be used in cross-linking. Thus the enzyme activity becomes limited.

What we are attempting to do is to use ion beam sputtering

to immobilize the enzyme. The rationale behind the work is based on the fact that a porous layer of glass, teflon, or some other material can be sputtered onto a substrate with the enzyme physically trapped between the substrate and the sputtered layer. In this manner, the porosity of the sputtered layer provides a better and quicker pathway for the substance of interest when compared to the gel matrix. The sputtered layer should enhance the response time of the reaction. This method should provide an attractive alternative to existing immobilization techniques.

Trypsin has been chosen initially for this investigation because it has been well studied and characterized. The entrapment layer will be teflon since the workers at NASA Lewis have a great deal of experience with that material.

The trypsin enzyme and the substrates have been brought out to NASA Lewis for sputter coating. When they are returned the enzyme properties will be evaluated as well as the degree of enzyme leaching and denaturalization.

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B. "Fabrication of a Potassium Sensing FET Using Ion Beam Sputtering," Electrochemical Society Meeting, Seattle, Wash., May 1978.

APPLICATIONS OF ION BEAM SPUTTERING TO MICROELECTRONICS

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ABSTRACT

Two novel uses of ion beam sputtering as applied to microelectronics have been investigated. The first was the use of ion beam texturing of silicon to increase the effective surface area of MOS capacitors. Results showed more than a factor of two increase in the capacitance per unit area but the breakdown voltage and interface properties were degraded. The second application was the sputtering of an ion selective membrane for fabricating a potassium sensitive field effect transisotr. The process developed makes batch fabrication of such devices possible.

Introduction

The trend in semiconductor device fabrication has been toward smaller and smaller device geometries. In many laboratories research into submicron fabrication techniques and the development of the associated equipment that is needed is being actively pursued. One area which is receiving a great deal of attention is the use of the ion beam etching as a replacement for wet chemical etching. The reason for this is that ion beam etching results in much less undercutting than wet etching and inaddition the side wall angle can be varied with the proper fixturing.[1,2]

The work reported in this paper utilized ion beam sputtering and etching techniques for two novel applications. One is the use of ion beam textured silicon in the fabrication of semiconductor devices. The second is the ion beam sputtering of an ion sensitive membrane as a part of a potassium sensitive field effect transistor.

Appartus

All of the ion beam sputtering was done using an eight centimeter electron bombardment xenon ion source as shown in Figure 1. The ion source is an outgrowth of technology previously developed for electron bombardment ion thrusters by NASA Lewis. Extraction of the Xe ions is accomplished by means of a dished two grid ion optics system. The ion beam is neutralized by using a heated tantalum wire. The vacuum facility maintains a vacuum of 1×10^{-5} torr during the sputtering process. The ion source is capable of operating at beam energies between 200 and 2000 eV and the beam current is adjustable between 10 milliamps and 200 milliamps.

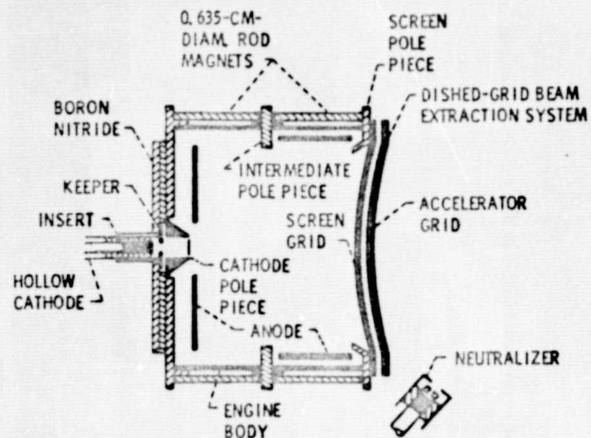

FIGURE 1. Cross sectional view of xenon ion beam source.

For the textured silicon surfaces the beam energy varied between 1000 and 2000 eV with beam currents of approximately 150 milliamps. Figure 2 is a sketch of the appartus arrangement used for ion beam texturing. The seed material, in this case, tantalum, is sputter deposited on the silicon target. The difference in sputter etch rates between the tantalum and silicon results in the textured surface. A detailed description of the texturing mechanism is beyond the scope of this work but it can be found in reference 3 along with some of the physical and optical properties of textured surfaces in references 4 and 5.

In fabricating the ion sensing FET's the ion source was operated at a beam energy of 300 eV and a beam current between 10 and 30 milliamps. Figure 3 is a skematic showing the relationship between the various components of the apparatus. The dip coated target to be discussed in more detail later was placed at a 45° angle with respect to the ion beam and 20 cm from the ion source. The aluminum disk was water cooled so that the temperature of the target would not exceed 100°C during the sputtering process. The FET devices were mounted near the grid plane of the ion source at a 45° angle with respect to the grid plane, so that the FET surface was parallel to the target plane. A water cooled quartz crystal monitor was located adjacent to the FET's and was used to monitor both the de-

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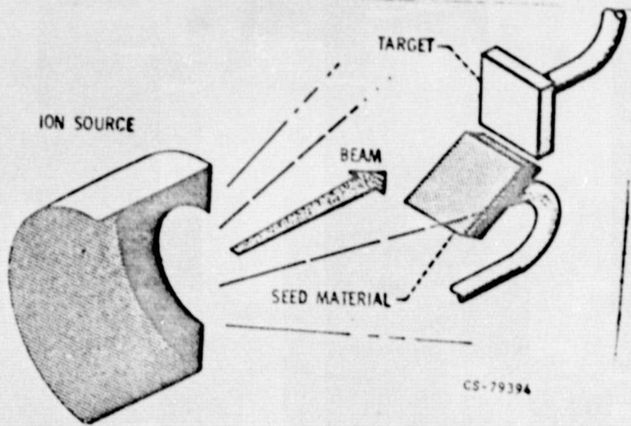


FIGURE 2. Sketch of the apparatus arrangement used for ion beam texturing.

position rate and the total thickness of the sputter deposited layer. The ion source parameters mentioned above resulted in deposition rates between 20 and 40 A per hour.

SKETCH OF XENON ION SOURCE, VALINOMYCIN/ P.V.C./Al TARGET, AND FET SAMPLE LOCATIONS

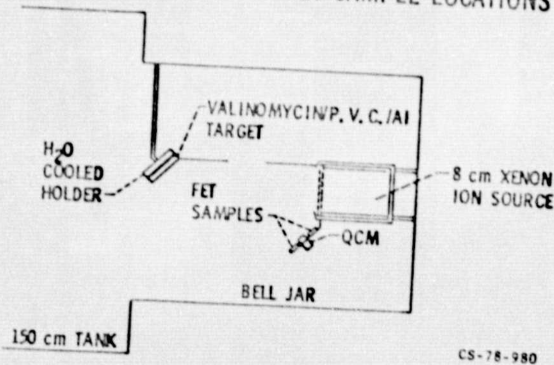
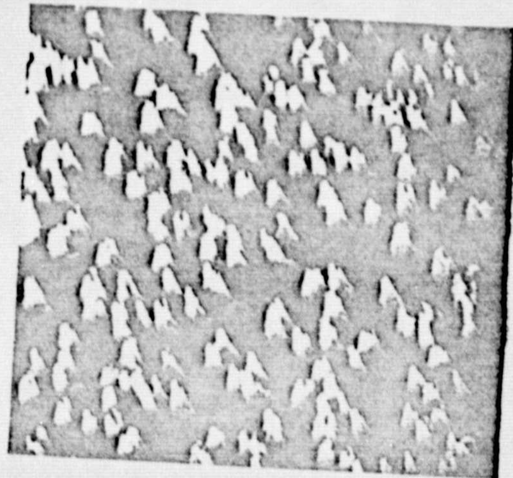


FIGURE 3.

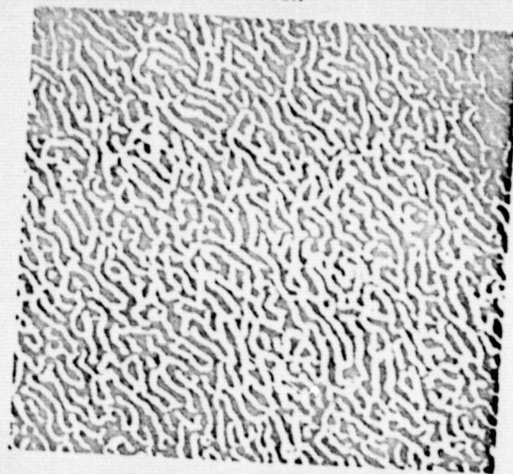
Texturing of Silicon

This phase of the project was aimed at developing and evaluating a fabrication technique which couls be used to minimize the area needed for MOS capacitors on integrated circuits. Most IC designs try to minimize the total capacitance needed by the circuit so as to conserve valuable silicon realestate. Since it is not always possible to reduce or eliminate the capacitance needed in a circuit, such a technique could have considerable value.

The surface morphology for the sample used in this study varied both in shape and dimensions. Figure 4 shows SEM pictures of the two types of surface structures which have been encountered. These two structures are referred to as ridges and cones. The vertical height was on the order of a micron or less.



CONES 3000X



RIDGES 10,000X

FIGURE 4. Examples of textured surfaces with cones and ridges.

After texturing, the silicon wafers were put through standard degreasing and cleaning procedure prior to being oxidized in dry O_2. Aluminum was evaporated over the entire surface and then patterned into dots using photolithographic techniques. During the texturing procedure a portion of the wafer was masked so that comparisons could be made using the same oxide. Table I shows the increase in effective surface area as measured at zero bias. These devices had very low breakdown voltage, a few hundred millivolts. It was suspected that the sharp points of the textured surface caused the premature breakdown due to increased electric field strength in those regions.

ZERO BIAS CAPACITANCE OF MOS CAPACITORS FABRICATED ON TEXTURED SILICON

SAMPLE	TEXTURED	NONTEXTURED
B-8	7100 pf	3100 pf
B-10	6500 pf	2800 pf
B-11	4000 pf	3000 pf

TABLE I.

The wafers were stripped of aluminum and oxide, recleaned and then reoxidized. As Table II shows there was again an increase in the effective surface area but it was not as large as for the initial tests. This decrease is explained by the consumption of the silicon peaks during the oxidation process. Table II also shows that the breakdown voltage has significantly increased.

The data for sample B-11 illustrates the effect of the silicon consumption during oxidation. This wafer had the finest textured structured as observed using an SEM and thus, after oxidation there was very little structure left. This is evident in the small increase in effective surface area and the higher breakdown voltage.

	TEXTURED		NONTEXTURED	
SAMPLE	CAPACITANCE	BREAKDOWN	CAPACITANCE	BREAKDOWN
B-8	630 pf	20 V	440 pf	200 V
B-10	530 pf	15 V	430 pf	200 V
B-11	490 pf	70 V	430 pf	200 V

TABLE II. Electrical parameters of reoxidized MOS capacitors fabricated on textured silicon.

The quality of the oxide-silicon interface was examined using capacitance versus voltage measurements, C-V curves from sampel B-10 is shown in Figure 5. The lower trace is for an MOS capacitor fabricated in a nontextured area. Two facts are apparent from this figure. (1) All the devices exhibit turn on voltages (point A on the figure) which are larger than expected. The value of -5 volts for the nontextured surface is more than three volts more negative than one would expect for a good quality oxide. Test performed on virgin silicon wafers in order to evaluate the oxide growth process and those samples showed the expected turn on voltage. At this point in time the cause of the oxide contamination had not been determined. (2) The textured surfaces exhibit an excessive number of surface states as indicated by the stretching out of the C-V characteristics in the depletion region. Although a higher capacitance per unit area can be obtained using the ion beam texturing technique, the surface quality would not be suitable for active MOS devices. This does not mean that the techniques cannnot be used for the fabrication of high density MOS capacitors for integrated circuits. The lower breakdown voltage and increase fabrication steps make their use, however, less attractive.

Potassium Ion Sensing FET

The need for miniature solid state chemical sensors for biomedical applications has been the driving force behind this work. A potassium ion-selective field effect transistor has been reported in the literature.[6] That device was fabricated using a casting technique for placing the ion-selective membrane over the active gate area of the FET. The assembly procedure was performed device by device and does not lend itself to batch fabrication. The technique described below is compatible with other solid state batch fabrication processes.

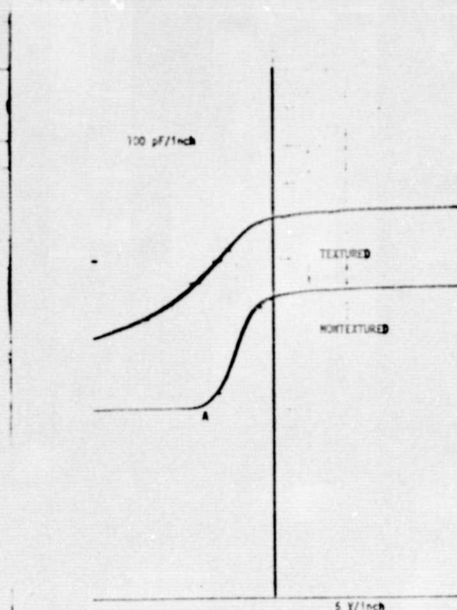


FIGURE 5. C-V CHARACTERISTICS FOR SAMPLE B-10.

The construction of the field effect transistor itself will not be described except to say that it is an n-channel depletion mode MOS FET with oxynitride as the gate dielectric and no gate metallization. The ion sensitive membrane which was sputtered onto the active gate area was deposited from an aluminum target 1/4 inch thick and three inches diameter which was dip coated with a mixture of 500 mg of polyvinylchloride, 1 cc of dioctyladipate, 8 cc of tetrahdrofuran and 10 mg of valinomycin.

Electron spectroscopy (ESCA) studies on membrane coated wafers have shown that there is very little compositional difference between the target material and the sputtered film. The oxygen peak of the sputtered film is shifted approximately 1.4 eV toward higher energies and the half peak width increased by approximately 20%. This would indicate not only a slightly different bonding structure, but also a mixture of bonding structures. No definite information is known however about the resulting chemical structure.

The PVC membrane containing valinomycin was sputtered onto an FET which had previously been fabricated as a pH sensor. After the sputter coating the active gate area of the FET, the device was tested for potassium sensitivity using a test set up as diagramed in Figure 6. A transfer curve for the device was first determined by applying voltages to the reference electrode and monitoring the output voltage measured at the source of the FET. The transfer curve for device designated H103 is shown in Figure 7.

Prior to being sputter coated this device had a measured pH response of 25 mV per pH. Figure 8 shows the output for this same device after sputter coating when subjected to various pH solutions containing molar concentrations of potassium between 0.01 molar and 1.0 molar. As can be seen from the figure there is no systematic variation

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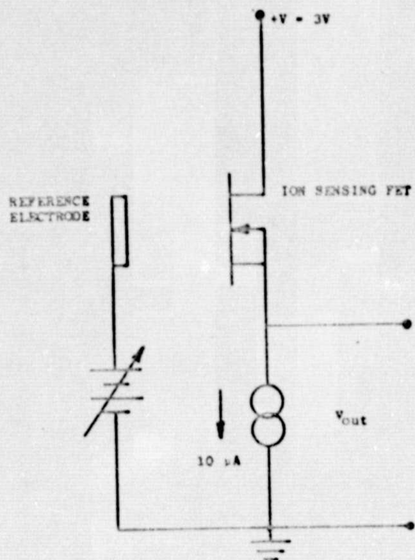


FIGURE 6. Measurement circuit for ion sensing FET's.

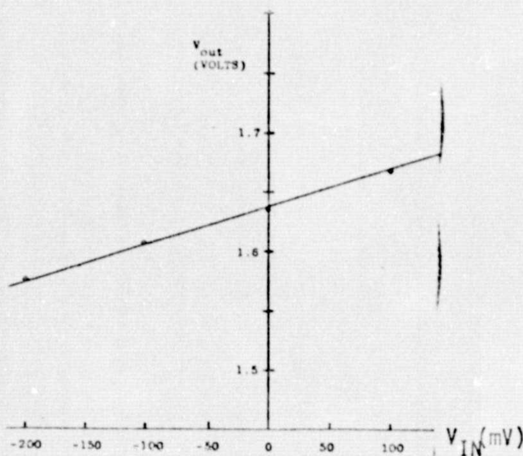
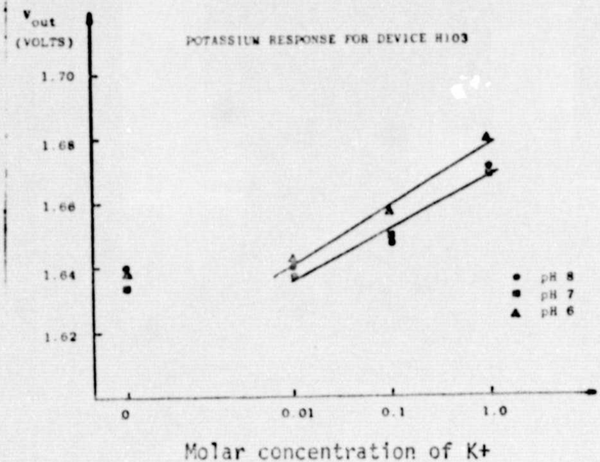


FIGURE 7. Transfer curve for device H103.

in the output which can be correlated with the pH of the solution. When the slope of the lines is combined with the input to output transfer ratio a response of 57 mV per decade of potassium ion concentration is calculated. This is quite close to the theorectical value of 59 mV/decade at room temperature.

While soaking in a 0.01 molar solution for more than 100 hours the device was periodically checked for potassium ion sensitivity. The sensitivity of the device was found to have dropped to approximately 30 mV/decade but the output remained stable with variations in pH and reproducable with changes in potassium concentration. A device which was dip coated in the same mixture the target was dip coated in remained sensitive to potassium for only a few hours. Our tests seem to indicate that the valinomycin does not leach out of the sputtered film as readily as it does from the PVC mixture.

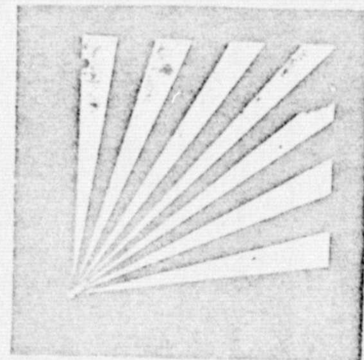


Molar concentration of K+

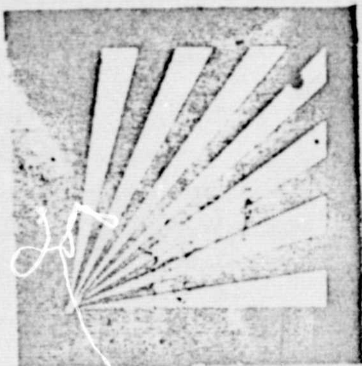
FIGURE 8.

In order to utilize the sputtering technique for the batch fabrication of ion sensitive FET's photolithographic processes for patterning the sputtered membranes had to be developed. Our tests have shown that the sputtered deposited film is not dissolved by the solvents used in the target preparation. When either tetrahydrofuran or methylene chloride was applied to the sputtering target it began to dissolve immediately. A silicon wafer covered with the sputtered membrane was soaked for more than three hours in tetrahydrofuran without any observable change in the membrane.

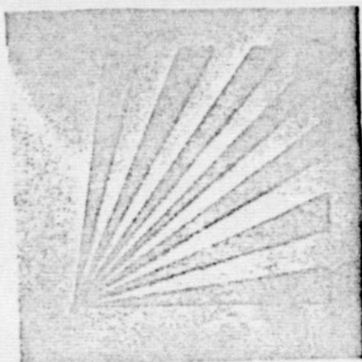
To date only the lift off technique using thick layers of photoresist have proven successful for patterning the sputtered membrane. Figure 9 shows photomicrographs of a test resolution mask used to evaluate the lift off techniques, as well as the photoresist patterned coated with PVC and the PVC after the removal of the photoresist. As the figure shows there is no obvious degradation of the pattern. Figure 10 shows a X400 magnification of a portion of the patterned PVC. It is easily seen that dimensions smaller than 1 mil are adequately reproduced.



Emulsion mask

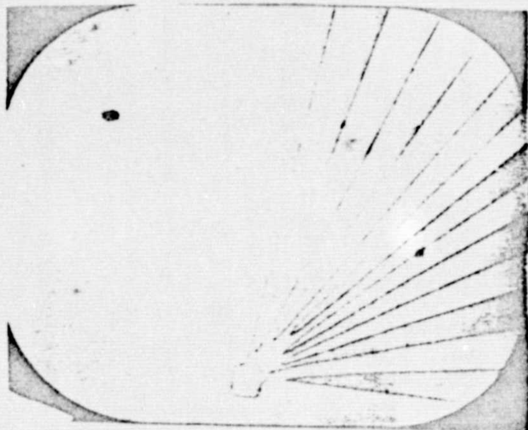


Photoresist and PVC



PVC

FIGURE 9. Photomicrographs of samples used for lift off evaluation.



PVC ON SILICON

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FIGURE 10. 400X magnification of patterned PVC on silicon.

The use of ion beam sputtering for the deposition of ion-selective membranes on FET's makes batch fabrication a possibility as well as the fabrication of multiple sensors each sensitive to a different ion on the same chip.

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James A. Topich was born in Steubenville, Ohio in 1948. He received his B.S.E.E. from Case Institute of Technology in 1970, his M.S.E.E. from Case Western Reserve University in 1972 and his Ph.D. in solid state electronics from C.W.R.U. in 1974. Since 1974 he has worked for the Engineering Design Center of C.W.R.U. in the area of miniature solid state transducers and specialized integrated circuits primarily for biomedical applications.

Michael J. Mirtich received his B.S. degree in Physics from John Carroll University in 1958 and a M.S. in Aeronautics and Space Administration at the Lewis Research Center in 1959. From 1959 to 1971 he was engaged in studying the effects of the micrometeorid and near-earth space environment in the optical properties of surfaces. From 1971 to 1977 he worked in the field of electric propulsion. From 1977 to the present he is a member of the Ion Beam Application Sections, conducting studies on the industrial applications of ion beam technology. He has published over 30 research papers in these various areas.

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Abstract No. 85

FABRICATION OF A POTASSIUM SENSING FET USING ION BEAM SPUTTERING

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The membrane was sputtered using an eight centimeter electron bombardment xenon ion source. Extraction of the Xe ions was accomplished by means of a dished two grid ion optics system. The ion beam is neutralized by using a heated Ta wire. The vacuum facility maintained a vacuum of 1×10^{-5} torr during the sputtering process. The ion source is capable of operating at beam energies between 200 and 2000 eV and the beam current is adjustable between 10 milliamps and 200 milliamps. For the devices reported herein the ion source was operated at a beam energy of 300 eV and a beam current between 10 and 30 mA. The dip coated target was placed at a 45° angle with respect to the ion beam 20 cm from the ion source. The aluminum disk was water cooled so that the temperature of the target would not exceed 100°C during the sputtering process. The FET devices plus a bare silicon wafer, were mounted near the grid plane of the ion source at a 45° angle with respect to the grid plane, so that the FET's surface was parallel to the target plane. A water cooled quartz crystal thickness monitor was located adjacent to the FET's and was used to monitor both the deposition rate and total thickness of the sputter deposited layer. The ion source parameters mentioned above resulted in a deposition rates between 20 and 40 Å per hour.

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References

1. S. D. Moss, J. Janata, and C. C. Johnson, "Potassium Ion Sensitive Field Effect Transistor", Analytical Chemistry, Vol. 47, No. 13, Nov. 1975, p. 2238.

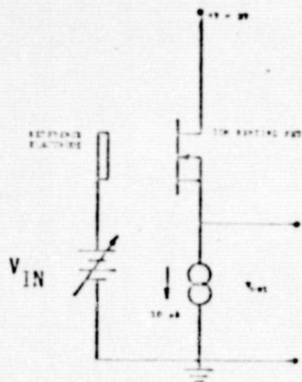

FIG. 1 MEASUREMENT CIRCUIT FOR ION SENSING FET'S.

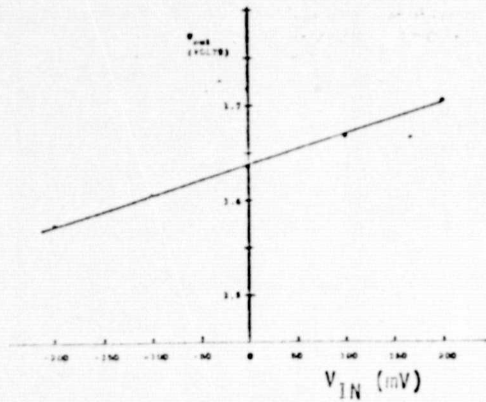

FIG. 2 TRANSFER CURVE FOR DEVICE H103.

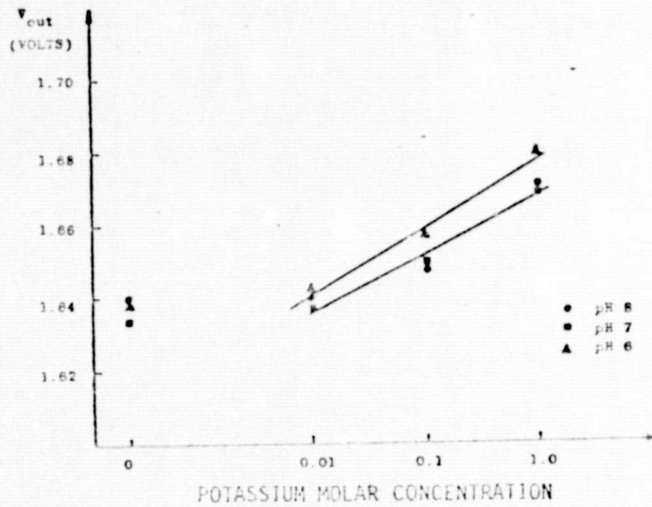

FIG. 3 POTASSIUM RESPONSE FOR DEVICE H103.

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