1. Report No
NASA CR-159407

2. Government Accession No

3. Recipient's Catalog No

4. Title and Subtitle
Development of Single Cell Protectors for Sealed Silver Zinc Cells

5. Report Date
1978

6. Performing Organization Code

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8. Performing Organization Report No

9. Performing Organization Name and Address
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10. Work Unit No

11. Contract or Grant No
NAS3-19432

13. Type of Report and Period Covered

12. Sponsoring Agency Name and Address
National Aeronautics & Space Administration
Lewis Research Center, 2100 Brookpark Road
Cleveland, Ohio 44135

14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

This program resulted in a family of single-cell protector systems that offer overcharge and overdischarge protection at the cell level for the silver zinc (AgZn) batteries. Three design approaches to cell-level protection were developed, fabricated, and tested. These systems are referred to as the single-cell protector (SCP), multiplexed-cell protector (MCP), and the computer-controlled protector (CCP). The SCP uses only analog circuits, and the MCP uses both analog and digital circuits. The MCP multiplexes the cell voltages into a set of voltage comparators thereby reducing the number of electronic parts required. The CCP is based on a microprocessor for logical and mathematical computations, and it requires the least number of parts.

To evaluate the benefits of each cell level protection system, 18-cell battery packs without cell level control were also subjected to cycle life test. A total of five batteries were subjected to simulate synchronous orbit cycling at 40% depth of discharge at 22°C. Batteries without cell-level protection failed between 345 and 255 cycles. Cell failure in the cell-level protected batteries occurred between 412 and 540. All electronics performed successfully throughout duration of the test program.

Based on the results of concurrent life testing of cell-level and battery-level protected systems for a 18-cell battery, it was determined that the cell-level monitoring and protection is necessary to attain the long cycle life of a AgZn battery. The cell-level protection was found to increase the life of the AgZn battery in synchronous orbit operation by a factor of at least 1.5. If spare cells are provided in the case of the CCP system, this factor can be further enhanced.

The best method of providing control and protection of the AgZn cells depends on the specific application and capability of the user. For testing a large number of cells and batteries, the microprocessor approach provides a low-cost low weight system with high flexibility in changing charge control limits. The SCP, on the other hand, is best suited for testing a limited numberr of cells or batteries if volume and weight requirements can be tolerated.

17. Key Words (Suggested by Author(s))
Charge Control, Microprocessor, Sealed Silver Zinc Cell, Cell Level Control Protection

18. Distribution Statement

19. Security Classif. (of this report)
Unclassified

20. Security Classif. (of this page)

21. No. of Pages

22. Price*

* For sale by the National Technical Information Service, Springfield, Virginia 22161

FOREWORD

This report covers the work performed for the National Aeronautics and Space Administration (NASA), Lewis Research Center, during the Phase II and III periods of contract NAS3-19432. Phase II and III periods were from April 1976 to April 1978. The results of Phase I are presented in the report, *Development of Singer-Cell Protectors for Sealed Silver-Zinc Cells,* NASA CR-135054, Martin Marietta Corporation, September 1976. This report describes the results of continuation of life testing started in the Phase I period and the development of the multiplexed-cell charge control and protection system.

All work reported herein was accomplished by the Power Systems Section of the Electronics Department at Martin Marietta, Denver Division.

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SUMMARY

This program resulted in a family of single-cell protector systems that offer overcharge and overdischarge protection at the cell level for the silver zinc (AgZn) batteries. Three design approaches to cell-level protection were developed, fabricated, and tested. These systems are referred to as the single-cell protector (SCP), multiplexed-cell protector (MCP), and the computer-controlled protector (CCP). The SCP uses only analog circuits, and the MCP uses both analog and digital circuits. The MCP multiplexes the cell voltages into a set of voltage comparators, thereby reducing the number of electronic parts required. The CCP is based on a microprocessor for logical and mathematical computations, and it requires the least number of parts.

To evaluate the benefits of each cell level protection system, 18-cell battery packs without cell level control were also subjected to cycle life test. A total of five batteries were subjected to simulate synchronous orbit cycling at 40% depth of discharge at 22°C. One battery without cell-level protection failed at 345 cycles and another at 255 cycles. The initial cell failure in the SCP-controlled battery occurred on cycle 412 with the last cell failure at cycle 540. Initial cell failure of the CCP-controlled cells occurred on cycle 354. Life testing of the MCP-protected battery was still in progress at the end of the contract period (April 18, 1978) with a total of 415 cycles without cell or component failure. All electronics performed successfully throughout the duration of test program.

Based on the results of concurrent life testing of cell-level and battery-level protected systems for a 18-cell battery, it was determined that the cell-level monitoring and protection is necessary to attain the long cycle life of a AgZn battery. The cell-level protection was found to increase the life of the AgZn battery in synchronous orbit operation by a factor of at least 1.5. If spare cells are provided in the case of the CCP system, this factor can be further enhanced.

The best method of providing control and protection of the AgZn cells depends on the specific application and capability of the user. For laboratory use involving a large number of cells and batteries, the microprocessor approach provides a low-cost system with high flexibility in changing charge control limits. It also provides an added advantage in data acquisition and interfacing with the digital equipment. The SCP, on the other hand, is best suited for testing a limited number of cells or batteries if volume and weight requirements can be tolerated. The MCP is useful whenever a compact small assembly, without the complication of the CCP (i.e., the software), is desired. Control and protection of a battery at the individual cell level using a microprocessor provides the greatest flexibility, both in control and data acquisition. The CCP can implement various protection schemes, including spare cell, via software. The MCP and CCP reduces the weight and volume of the electronics and total battery test cost by eliminating cell matching, and are capable of monitoring total system and individual cell parameters.

1.0 INTRODUCTION

In 1975, NASA Lewis Research Center contracted Martin Marietta Corporation to develop, fabricate, and test a single-cell protector system (SCP). The single-cell protector is capable of providing overcharge and overdischarge protection of a single silver zinc (AgZn) cell. Principal elements in the SCP are the two upper and lower voltage limit comparators and a magnetic latching relay. A single SCP is connected to an individual cell and the relay is used to switch the cell in or out of a series wired battery configuration. Subsequently, two alternative designs with similar functional features were designed and tested. The designs are referred to as the Computer-Controlled Protector (CCP) and the Multiplexed-Cell Protector (MCP).

During the Phase I contract a microprocessor-based system, CCP, which was previously developed under company funding, was used by modifying its software and a demonstration was successfully completed on a 10-cell AgZn battery pack. Fifty cells, manually fabricated by Yardney Electric Corporation, were supplied to Martin Marietta as GFE.

Life testing started in Phase I was continued during Phases II and III, and the design, fabrication, and testing of the MCP was conducted. The multiplexer system is identical to the SCP but uses common voltage comparator and multiplexing circuits to monitor and control each cell in a battery pack. Life testing of the SCP, CCP, and MCP configurations were completed in Phase III. Each configuration has a 18-cell battery pack and two 18-cell battery assemblies to control battery level.

An additional 46 cells were supplied to Martin Marietta as GFE during Phase II. The cells were second generation cells manufactured by Yardney Electric Corporation on its production line.

An 18-cell multiplexed cell protection system was designed and fabricated during Phase II. Life testing was initiated with a fresh 18-cell battery pack protected by the MCP. Another 18-cell battery under conventional battery level control was life tested for comparison purposes.

The Initial HS40-7, 40-Ah silver zinc cells were manufactured by Yardney Electric Corporation (YEC). The cells used in Phase I were hand made and assembled in the facility built and maintained for NASA LeRC by YEC. The second generation cells used in the Phase II and III periods were from a production lot and designated LeRC HS40-14.

The main objective of this report is to present the results of work accomplished during Phases II and III. Figure 1 is a photograph of the cell and a drawing giving its dimensions. Table I summarizes the key design and physical features.

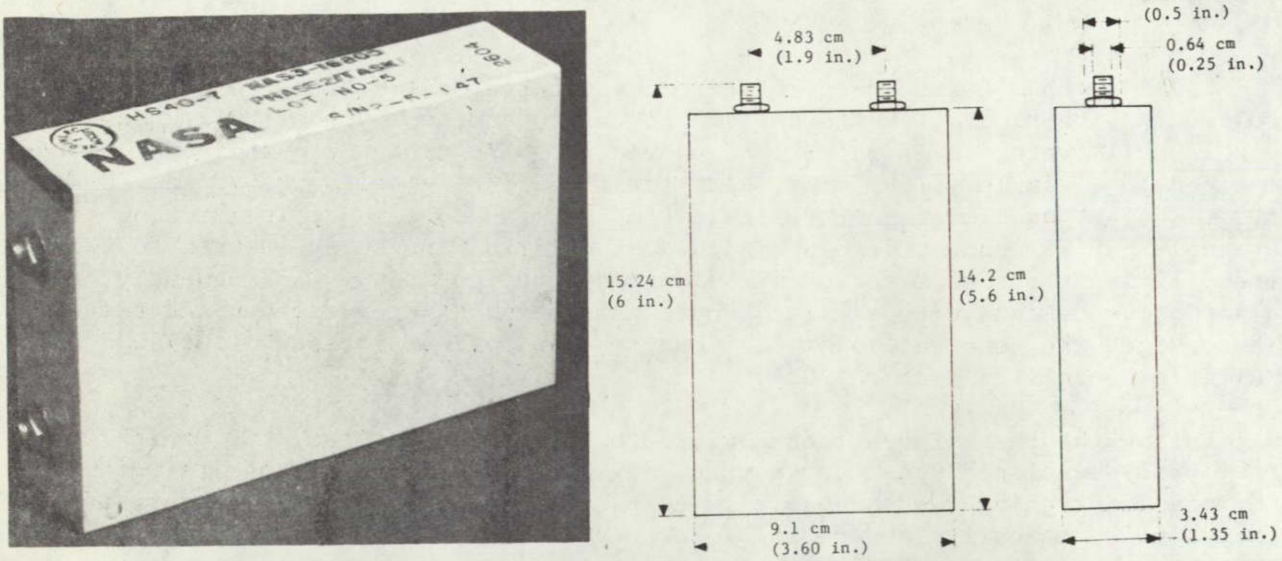


Figure 1. - 40-Ah silver-zinc cell, HS40-7, with organic separator.

Table I. - KEY FEATURES OF THE HS40-7 AND HS40-14 SILVER ZINC CELLS.

Capacity:	40 ampere hours
Number of plates:	6 positive, 5 negative
Separator material:	Inorganic, fuel cell grade asbestos
Header seal:	Ultrasonically welded to provide uniform and complete seal
Electrolyte:	KOH
Case Material:	Polyphynl Ethylene Oxide
Weight:	263 g (0.58 lb)

2.0 PROGRAM OBJECTIVES

2.1 Phase I Objectives. - The objectives of Phase I was to design, develop, fabricate, and test a single-cell protector system that would improve the NASA Lewis Research Center Solid State Voltage Comparator (SSVC) system and to investigate an alternative approach to the SCP system based on the use of a dedicated microprocessor with the SCP providing the cell-level protection (ref. 1). The three basic tasks were as follows:

Task 1 Design, develop, and fabricate an improved cell protector.

Task 2 Life test an 18-cell assembly with SCP control and an 18-cell battery controlled at the battery level.

Task 3 Evaluate a computer control approach.

2.2 Phase II Program Objectives. - The objectives during Phase II were to (1) determine the life capability of the battery under SCP protection, and (2) develop a system with a lower electronic parts count that potentially would result in a higher reliability of the overall system.

2.3 Phase III Objectives. - The Phase III objective was simply to continue the life-cycle testing started during the previous phases to determine the long-term operational performance of SCP-, CCP-, and MCP-controlled batteries, and to further evaluate the benefits of cell-level protection as compared to battery-level protection.

3.0 MULTIPLEXED-CONTROL PROTECTOR DEVELOPMENT

3.1 Objectives. - The primary objective of the MCP development was to provide a system that represented an improvement over the SCP design. The basic approach was to reduce the total number of electronic parts by combining like functions, such as the window comparator, for sensing battery charge and discharge voltage limits.

3.2 Design and Performance Requirements

Function. - The cell protectors are designed to provide individual cell-level protection against overcharge and overdischarge. The protection is accomplished by terminating charge, or discharge, when the cell voltage reaches a preset limit. Although designed specifically for AgZn cells, the SCP and MCP designs are flexible enough to permit adaptation to other rechargeable cells. The CCP design can be used for any secondary cells with only software changes. The cell protectors are capable of providing individual cell protection for batteries consisting of any number of series-wired cells to a maximum of 18.

Operating Modes. - The cell protectors have two operating modes: a "latch" mode and a "pulse" mode. When operating in the latch mode, the cell protectors are capable of automatically switching cells out of circuit only after reception of an external command. When operating in the pulse mode, the cell protectors automatically switch cells both in and out of circuit. Cells are automatically switched into circuit following a time delay that is initiated by the return of the cell voltage to an in-limit condition.

Incorporation of a pulse mode of operation permits automatic charge/discharge cycling of a battery without the need for an external reset during changeover from charge phase to discharge phase or vice versa.

Charge Protection. - To prevent premature charge termination due to the monoxide-to-peroxide transition overvoltage, the cell protectors incorporate a time delay during which switching operation is inhibited (Fig. 2). When the cell voltage is below the enable threshold voltage, the charge limit detection function (but not the discharge limit detection function) is inhibited. When the cell voltage rises to enable threshold voltage, a timer is started that establishes a time delay T1. After the delay T1, the charge limit detector is enabled and a subsequent increase in cell voltage to the charge voltage limit results in the immediate switching of the cell to an open circuit condition.

If the cell voltage remains above the enable threshold voltage after charge completion, and the cell is then returned to the charge mode by remote command, the cell protector will immediately switch the cell to an open circuit condition (without the time delay T1) subsequent to the cell voltage reaching the charge voltage limit. If the cell voltage falls below the enable threshold voltage after charge completion, and the cell is then returned to the charge mode by remote command, the cell protector will switch the cell to an open circuit condition after a time delay T1.

Discharge Protection. - End-of-discharge is indicated by a fall in cell voltage to a discharge voltage limit. Subsequent to cell voltage falling to the discharge voltage limit, the cell protector immediately switches the cell to an open circuit condition without delay.

Other specific features of the cell protectors are listed in Table II. The detailed performance characteristics of the protector designed for a 40-Ah AgZn cell are given in Table III.

3.3 Electrical Design. - A complete cell protector system consists of a battery, a cell protector, a control and display panel serving as a user interface, a single floating power supply for cell protector and C&D panel power, and a battery charger and load bank. The equipment is arranged as shown in Figure 3.

The control and display panel receives and displays individual cell status signals from the cell protector circuitry indicating whether the cells are switched in or out of a series-wired battery configuration. The control and display panel also transmits operational commands to the cell protector obtained from switches on the face of the panel.

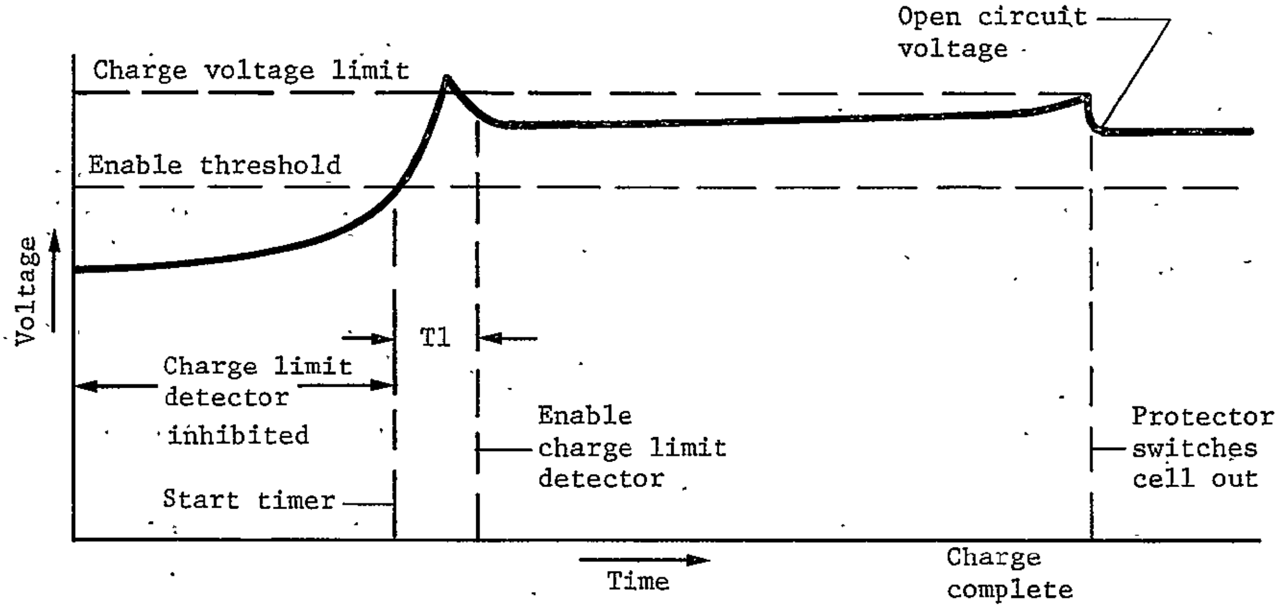


Figure 2. - Cell protector operation during charge for AgZn and AgCd cells.

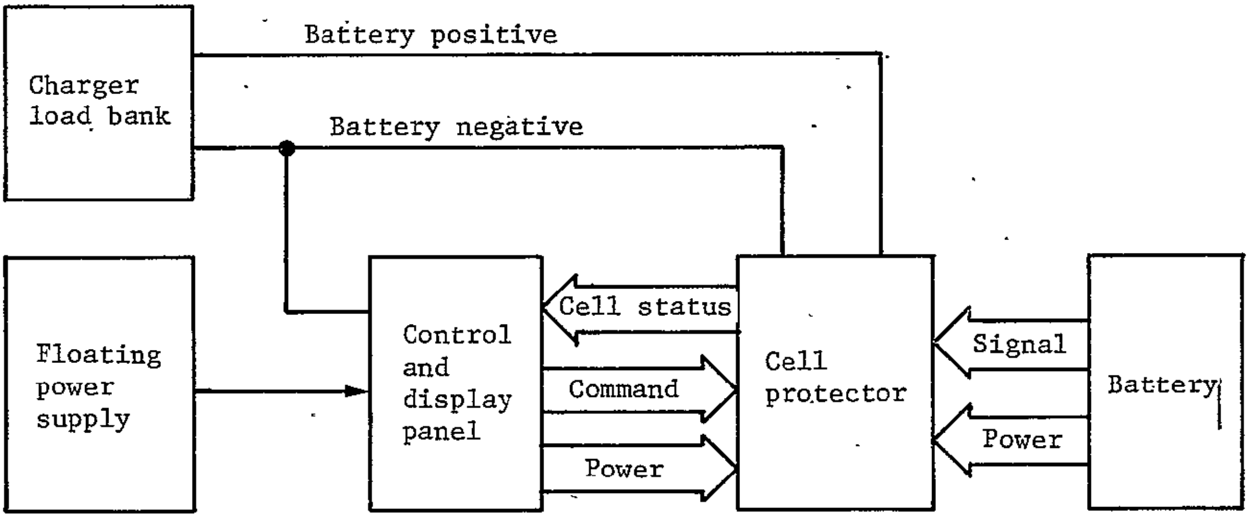


Figure 3. - Basic cell protector system block diagram.

TABLE II. - OTHER FEATURES OF AgZn CELL PROTECTOR.

Out of Limit Override - Ability to override the cell protector protection function and operate the battery as a standard battery without protection.

Power - Capability to operate from a single floating power supply.

Battery Interrupt - During discharge, the cell protector does not interrupt current flow through a series-wired battery group of cells when switching a cell out of circuit. During charge, the cell protector may interrupt battery current when switching a cell out of circuit.

Internal Protection - Protection against circuit damage due to inadvertent short circuits or misconnection at the external interfaces.

Operating Range - Capable of protecting an individual cell in an 18-cell series-wired AgZn battery group.

Operating Temperatures - The cell protectors are capable of operating over a temperature range of 0°C to 50°C.

Power Transients - Improper cell switching prevented when power is removed.

TABLE III. - SINGLE-CELL PROTECTOR CHARACTERISTICS FOR 18-CELL AgZn BATTERY.

Parameter	Limit
Operating Current Range	20 A Maximum
Operating Battery Voltage Range	40 V Maximum
Power Dissipation	7.5 W Maximum
Cell Charge Voltage Limit	0.5 to 2.15 Vdc
Cell Discharge Voltage Limit	0.1 to 1.35 Vdc
Cell Enable Voltage Level	1.75 ± 0.05 Vdc
Voltage Measurement Accuracy	±10 mV
Enable Time Delay	2.5 to 40 min
Pulse Mode Time Delay	5 s to 5 min

The battery cells are interconnected by magnetic latching relays internal to the cell protector (Fig. 4). Each cell is connected across the contact of its associated relay, and the relay wipers are connected to the negative side of the succeeding cell in the battery string. When all relays are in the "IN" position, the battery is at maximum voltage and capacity with all cells connected. As individual relays are switched to the "OUT" position, the associated cells are bypassed and the effective number of cells in the battery is reduced. Potential leads from the cell protector are connected directly to each cell terminal for voltage monitoring. Direct connection of the potential leads to the cell terminals, rather than to the relay terminals, eliminates measurement errors caused by current flow through the interconnecting wiring and relay contact resistance.

Cell bypass diodes are connected across each relay in an "alternative path" arrangement. These diodes are not necessary for fundamental control of cell switching, but are desirable because:

(1) The diodes provide an alternate path for battery discharge current flow during relay contact switching transitions, thus preventing the load bus from being momentarily open-circuited during relay switching.

(2) By virtue of their current-shunting action, the diodes provide supprесion for the relay contacts. If a relay is commanded to switch a cell out of the battery group under conditions of heavy discharge, the voltage through which the current must be switched is clamped to the small forward drop of the diodes, and relay contact stress is minimized.

Magnetic latching relays were selected for use in the cell protectors because of their zero standby power consumption. However, their advantage in power dissipation over nonlatching-relay types is somewhat offset by special operational constraints associated with their use. Foremost among these constraints is the problem of determining relay position (cell in or out of circuit) because, with no coil power supplied, relay position cannot be conclusively ascertained from available signals in the cell protector circuitry. The possibility of confusing the cell protector and damaging the protector and/or the battery cells is thus raised. To eliminate the concern, a spare set of relay contacts is used to provide a positive indication of relay state to the cell protector circuitry. A third and final set of contacts provides status information to the C&D panel.

A block diagram of the MCP illustrating the major functional elements is shown in Figure 5. The battery cells are interconnected in series by a relay network, one relay being required for each cell. Battery connection to the charger and load bank is also made in the relay network. The central governing element in the MCP system is the control logic section. This section received buffered-cell information and external commands from peripheral signal conditioning blocks and issues "CELL IN" or "CELL OUT" commands to the relay network. This causes the cells to be configured in or out of a series-wired battery arrangement.

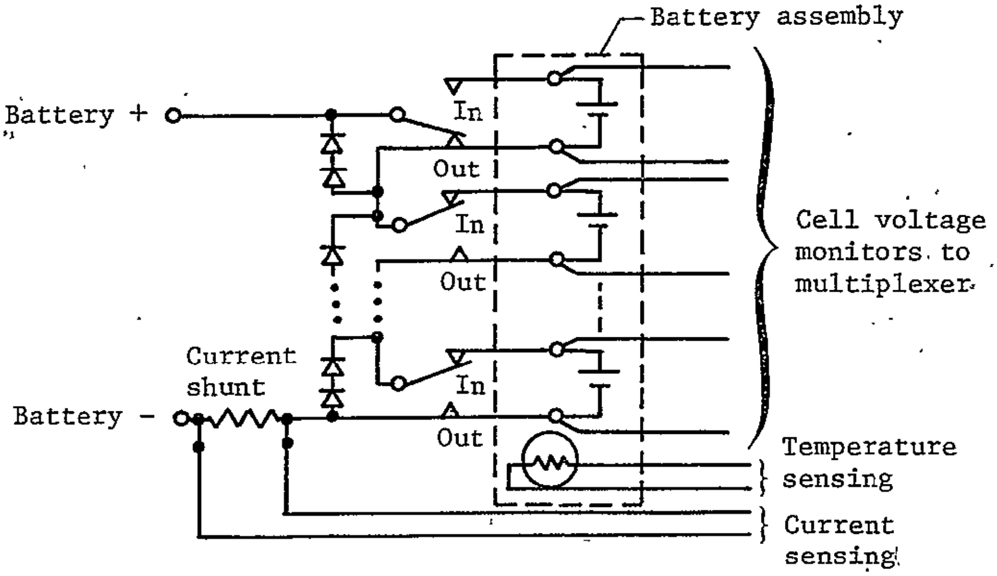


Figure 4. - Cell interconnection network.

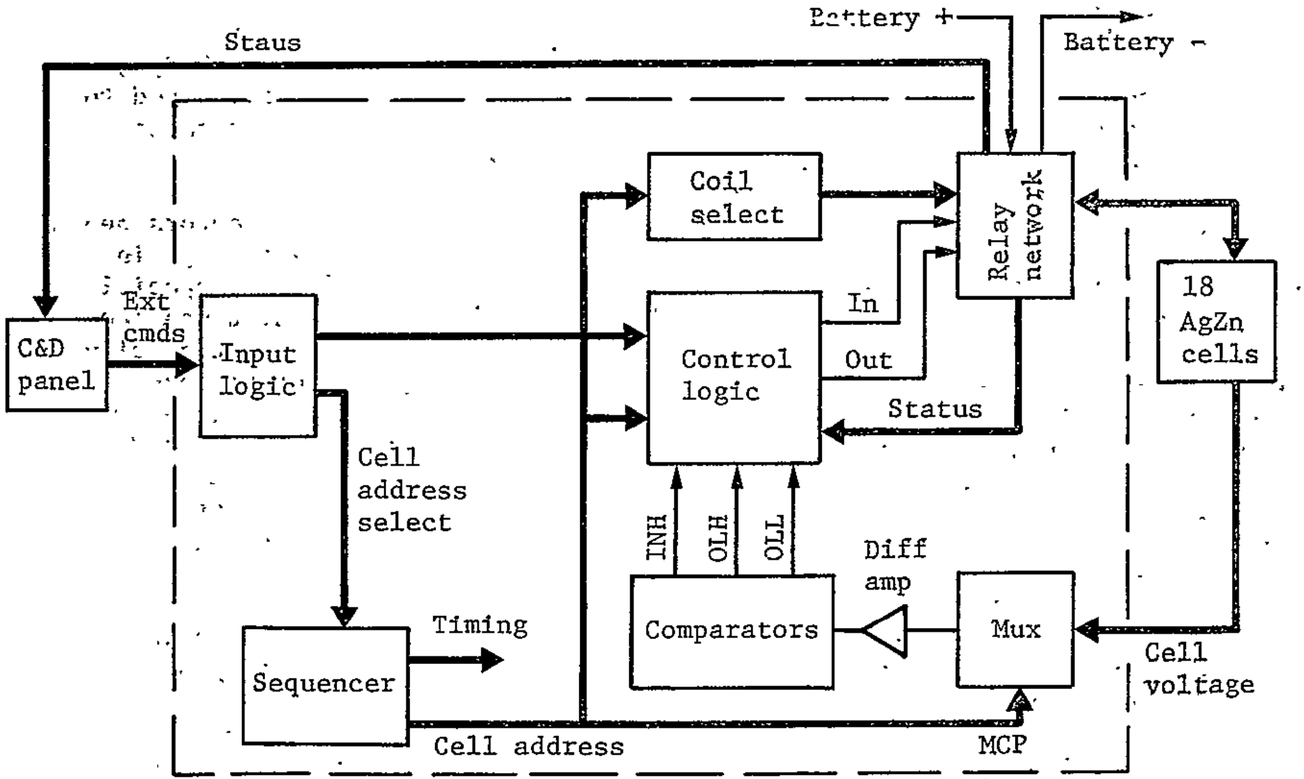


Figure 5. - MCP block diagram.

The MCP normally operates in a sequential manner. Each cell is addressed in turn, the cell voltage is measured, and, if an out of limits condition is detected, the cell is switched out of circuit. The MCP then addresses the next cell and repeats the process. When the last cell has been addressed, the cycle repeats starting with the first cell. The MCP sequencing operation is automatic. The MCP will repetitively cycle through the cells unless interrupted by an external command.

Control of the sequencing operation is provided by the sequencer, which generates the timing and cell address signals for use by the rest of the MCP circuitry. The cell address is routed to the multiplexer, control logic, and coil-select blocks enabling the circuitry in the sections associated with the cell being monitored.

The sequence of operations for monitoring a specific cell begins when the sequencer issues a particular cell address. The multiplexer channel corresponding to the addressed cell is enabled and the cell voltage is coupled to the signal conditioner which amplifies the cell voltage and removes the common mode battery voltage from the signal. At the output of the signal conditioner, the conditioned cell voltage is fed into a common network that issues three commands (INH, OLH, and OLL) to the control logic block depending on cell voltage level. The commands are described in Table IV.

TABLE IV. - MCP COMMAND DESCRIPTION.

OLL (Out of Limit Low) - Indicates that the cell voltage is below the lower, or discharge, limit.

OLH (Out of Limit High) - Indicates the cell voltage is above the higher, or charge, limit.

PER (Peroxide) - Used with AgZn cells to indicate the cell voltage is above the monoxide-to-peroxide transition level. The PER command, when issued, inhibits the control logic from issuing a CELL OUT command for a preset time, thus allowing the cell to pass through the AgZn voltage spike region of operation.

The control logic section operates on the INH, OLH, and OLL signals from the comparators. The conditioned external commands operate from the input logic block, and the cell status signals operate from the relay network and issue CELL IN or CELL OUT commands to the relay network. The cell status signals obtained from the relay network indicate whether the cells are in or out of circuit. They are used to inhibit unnecessary relay coil pulsing. For example, if the control logic determines that a CELL OUT command is in order, the cell is already out of circuit, then the cell status signal will inhibit the CELL OUT command rather than transmit an unnecessary relay coil pulse.

The coil select block addresses coil driver circuitry for the particular relay to be operated on by the CELL IN or CELL OUT commands from the control logic block. The input logic block buffers external commands from the C&D panel, latching and synchronizing them for use by the control logic block.

3.4 Packaging Design and Fabrication

Mechanical Design Considerations. - Basic MCP packaging criteria are as follows:

(1) Construction of the MCP is sufficiently rugged to withstand the normal handling expected in a laboratory environment.

(2) All internally mounted components are readily accessible to facilitate circuit repairs or part replacement.

(3) The circuit performs its function reliably over its expected life with minimum failure rate and downtime.

(4) The MCP is configured to provide minimum voltage drop between the MCP and the battery cell.

(5) Fabrication cost and size of the MCP are kept to a minimum, consistent with the preceding requirements.

Packaging Design Description. - The MCP, shown in Figure 6, is a modular design with 18 cell bypass circuits housed in a single unit. The requirement for the MCP to be placed close to the cell influenced the MCP configuration to reduce the voltage drop from the cell to the MCP. Thus, to minimize wire lengths, the MCP was designed to accommodate two 9-cell packs.

A single connector provides the interface to the power supply and the control and display panel. The electronics parts are mounted on two double-sided PC Boards (Fig. 7). Gold-plated fingers are provided on the PC boards to facilitate board level functional testing.

Board design is in compliance with the part mounting and interconnection requirements of NHB 5300.4 and the PC board design specification, MSFC STD 154A.

The case is welded sheet metal and consists of two end plates, U-Channel sides and bottom, and a top cover for aesthetic purposes. The case exterior was painted the same color as the battery cells.

Fabrication. - Figure 8 shows the assembly sequence for fabricating the MCP, starting with the PC board assembly. The electrical components are mounted on the PC boards and wire wrapped in place to the requirements of the Martin Marietta Assembly Process STP85132.

After completion of board-level tests, the PC boards, relay, switch, and connector are placed in an assembly fixture for prewiring the assembly. Wires to the battery cell terminals are also soldered to the relay at this time. When soldering operations are complete, detailed inspection and continuity tests are performed. The electronics are then installed in the case.

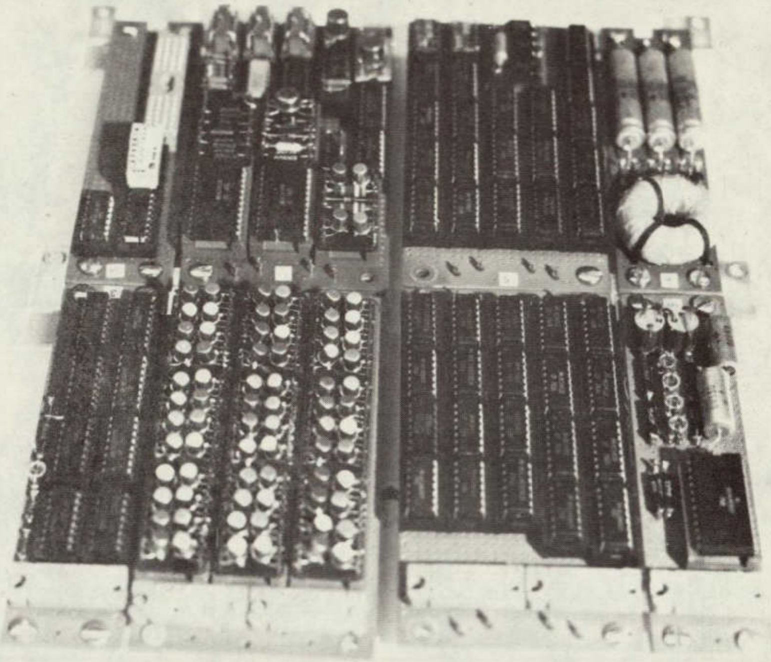


Figure 6. - Multiplexed cell protector connected to 18 AgZn cells.

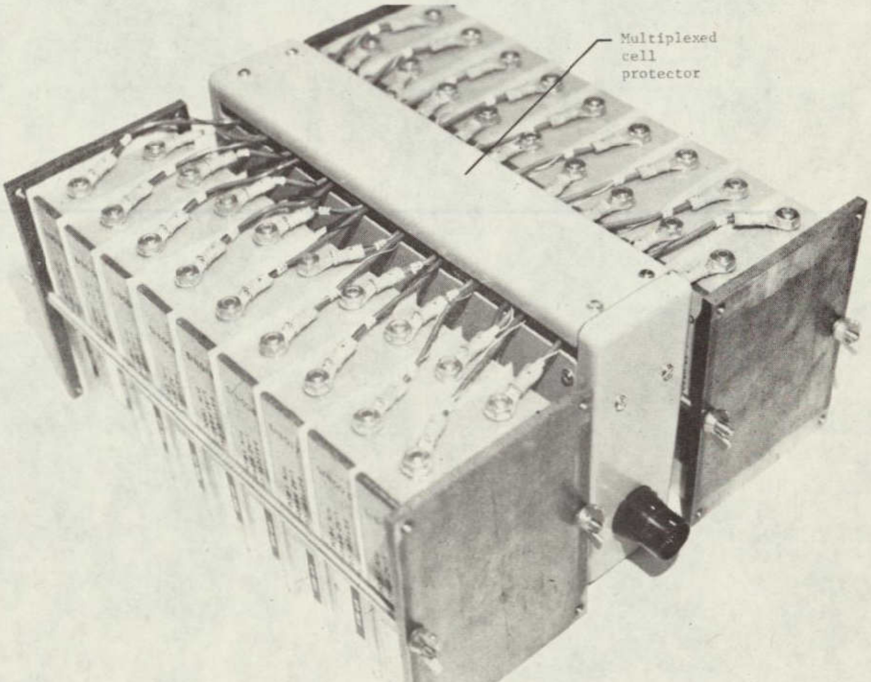
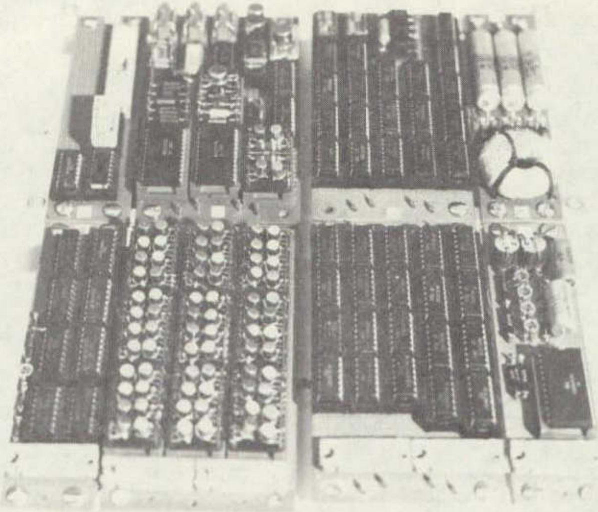
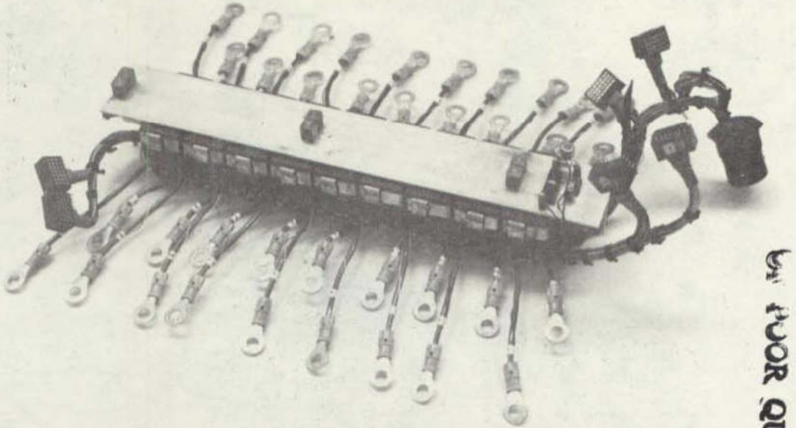


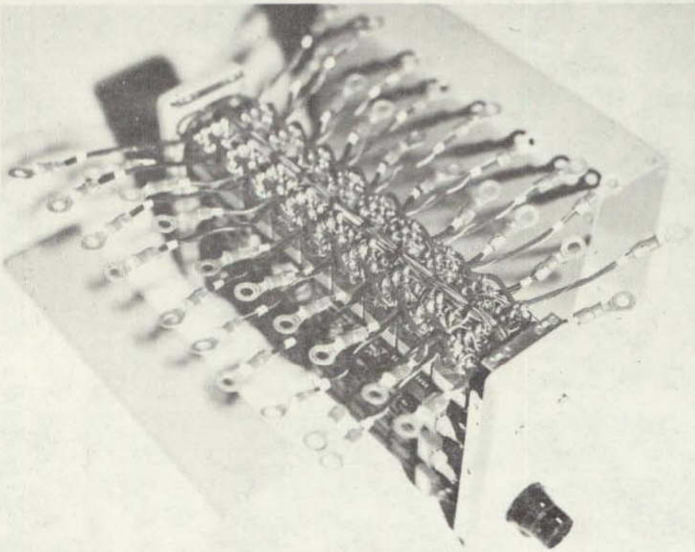
Figure 7. - MCP two-sided circuit boards.



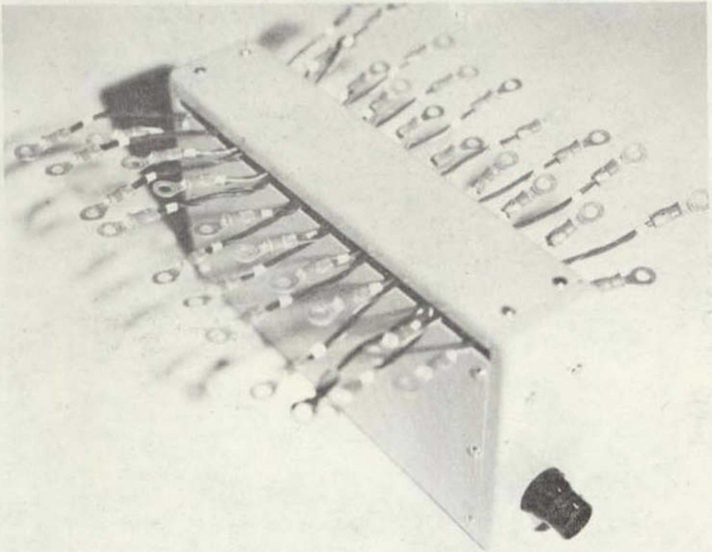
Printed circuit boards



Bypass relay



Fit Check



MCP assembly

Figure 8. - Manufacturing flow of multiplexer cell protector.

With the relay securely mounted to the case, the remainder of the electronics is installed and secured in place. A fit check is then performed to verify that the unit has not been degraded by pinched or damaged wires, wires bearing on sharp points, contamination, etc. Minimum clearance between components on the PC boards and protrusions on adjacent boards has been ensured by control dimensions for PC board assembly. The U-channel is set in place and the cover is mounted to the case.

4.0 BATTERY LIFE TESTING

4.1 Objectives. - Task 2 objectives in Phases I and II were to assemble five battery packs to (1) determine the effects of cell level control in extending the life of the 40-Ah silver zinc batteries, and (2) evaluate the performance of the SCPs, CCP, and MCP by cycle testing battery assemblies.

The scope of the task as defined in the Statement of Work is as follows:

"Life cycle tests shall be made to compare the cell-protected battery against a standard, identical size battery that does not have single cell protection. Cells for the standard battery shall also be furnished by NASA as GFE. The cycle regime for this test shall be equivalent to a synchronous-type orbit. Test shall consist of a 40% DOD, 1 cycle per day. Discharge at 13.3 amps for 1.2 hours followed by charging at 0.75 ampere for 22.8 hours. Cells shall be tested to failure or until end of the contract period of performance. Failure is defined as the inability of the battery to perform the duty cycle outlined above or whenever the average cell voltage of the battery falls below 1.25 volts/cell before the end of the 1.2 hour discharge period."

4.2 Test Configuration

Battery Cell Description. - The 40-Ah HS40-7 silver-zinc cells were manufactured by Yardney Electric Corporation for NASA Lewis Research Center. Ninety-three cells were provided to Martin Marietta as government furnished parts to support Task 2 testing. Figure 1 is a photograph of the cell and a drawing showing its dimensions. Table I summarizes key design and physical features.

Group I Battery/SCP Configuration. - The 18-cell battery pack designated Group I consists of two 9-cell assemblies. Each assembly is restrained between two steel plates. The cells are individually controlled and protected by the SCPs. Figure 9 shows the typical electrical connection of one SCP and one silver-zinc cell.

The control and display panels (C&D) in Figure 10 provides the following functions:

Sets/resets individual cell control relays;

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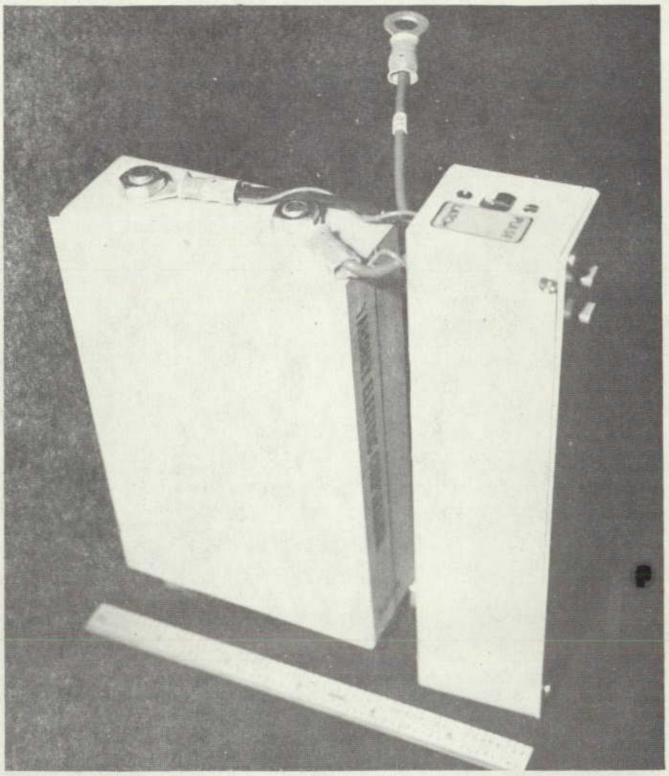


Figure 9. - Single-cell protector (SCP) and one 40-Ah AgZn cell.

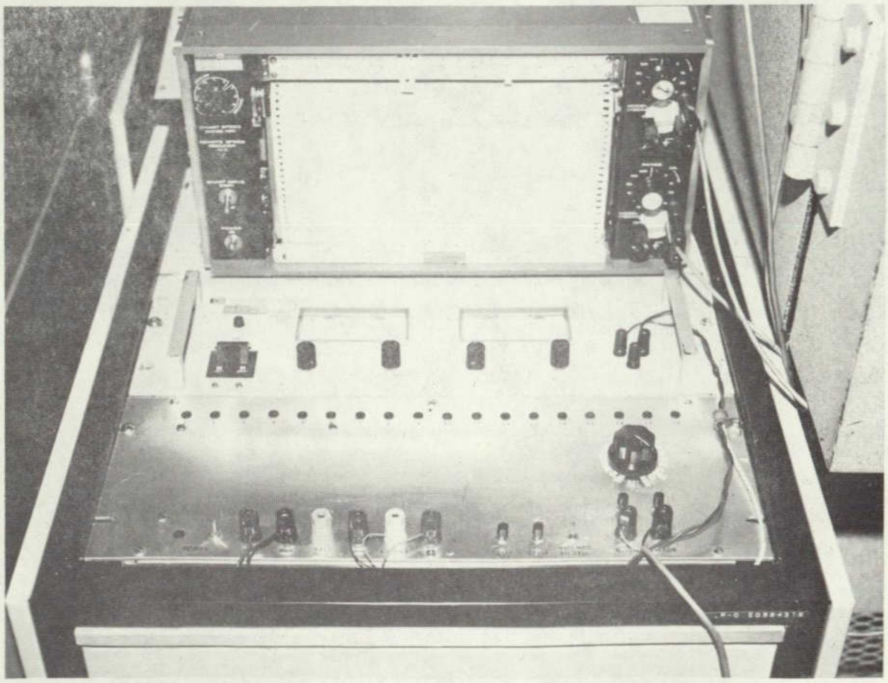


Figure 10. - Control and display panel.

Sets/resets all cell control relays;

Monitors cell voltages and battery voltage;

Provides cell on/off status lamp.

The test setup for Group I assembly is shown in Figure 11. In case of a failure by the SCP, the Automated Control and Data Acquisition System (ACDAS) automatically aborts the test and prints out which SCP failed. ACDAS control limits are the SCP voltage limits and function only in case of an SCP failure. Appendix A gives a detailed description of the ACDAS.

In addition to the SCP reset command capability of the C&D panel, ACDAS supplies a signal upon entering the charge phase, which resets all cell bypass relays, thus ensuring that all cells are connected in series at the start of each cycle.

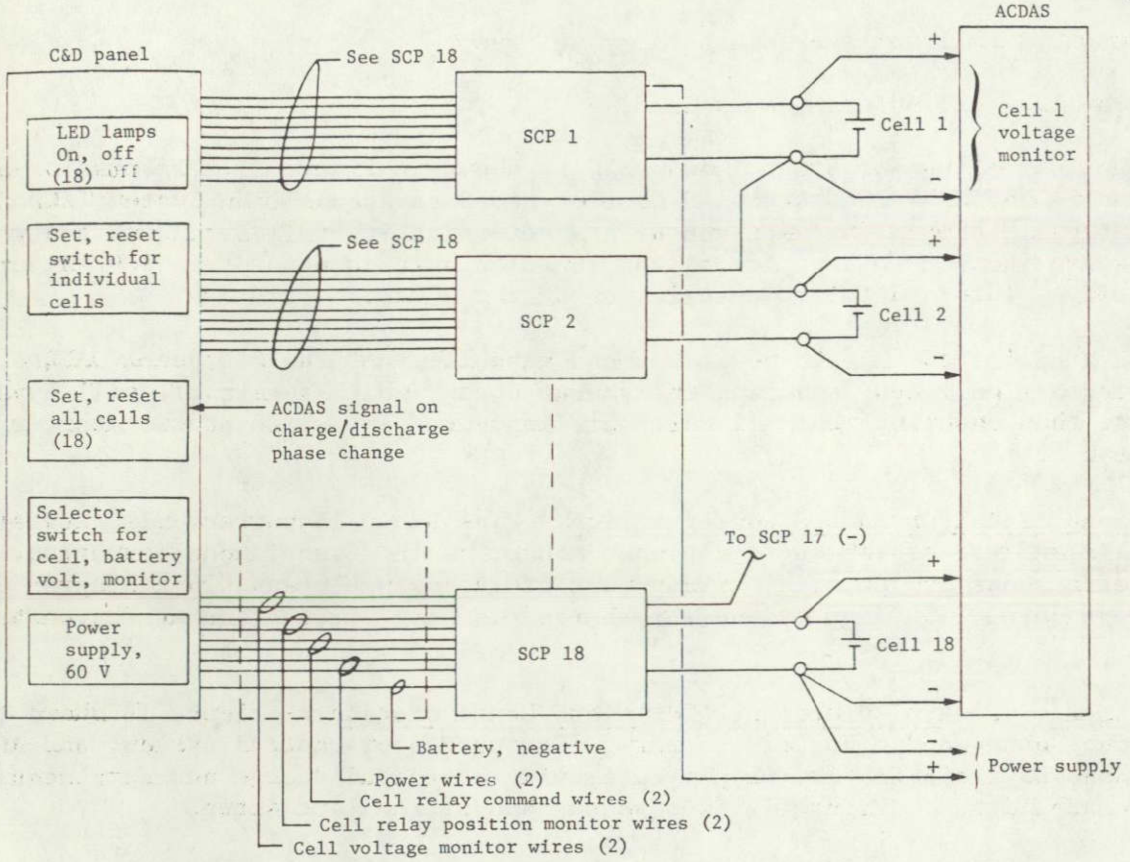
Group II Battery/ACDAS Configuration. - The Group II battery also contained 18 cells and was assembled in the same manner as the Group I configuration. Figure 12 shows the physical arrangement of the assembly and block diagram of the test setup. ACDAS provided the charge/discharge protection at the battery level.

Computer Control Protector (CCP) Test Configuration. - Figure 13 shows the interface between the 10-cell battery, microprocessor control system, and ACDAS. Functions of the ACDAS are mainly to provide charge/discharge and data acquisition capabilities. Figure 14 is a photograph of the test setup.

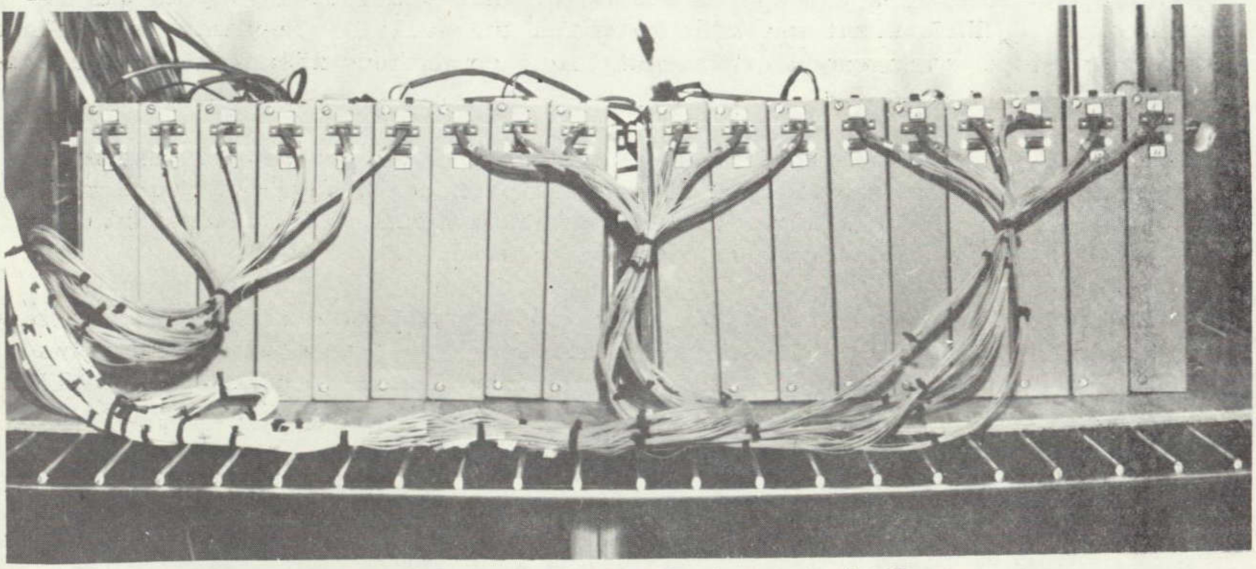
The test procedure for the CCP follows. Ten cells were conditioned by charging them at the rate of 1.5 A for 30 hours, then discharging them at the rate of 6.0 A to a cell voltage of 1.250 V. This conditioning cycle was repeated twice. (No attempt was made to match the cells.) They were then placed in an equivalent synchronous orbit under test conditions identical to those for the Group I battery in Task 2.

The ACDAS controlled the orbital functions such as charge and discharge time limits. It also provided backup system protection capability and monitored and stored charge and discharge current and individual cell voltage data for verification of the microprocessor system accuracy.

Multiplexed Cell Protector (MCP) Test Configuration. - The 18-cell battery pack used in the MCP test also consisted of two 9-cell assemblies restrained between two steel plates. The MCP was sandwiched between the cell assemblies. The cells are individually controlled and protected by the MCPs. Figure 6 shows the electrical connections of the MCP and the cells.



Functional block diagram



Group I battery and SCPs in test chamber.

Figure 11. - Test setup for SCP/Group I battery.

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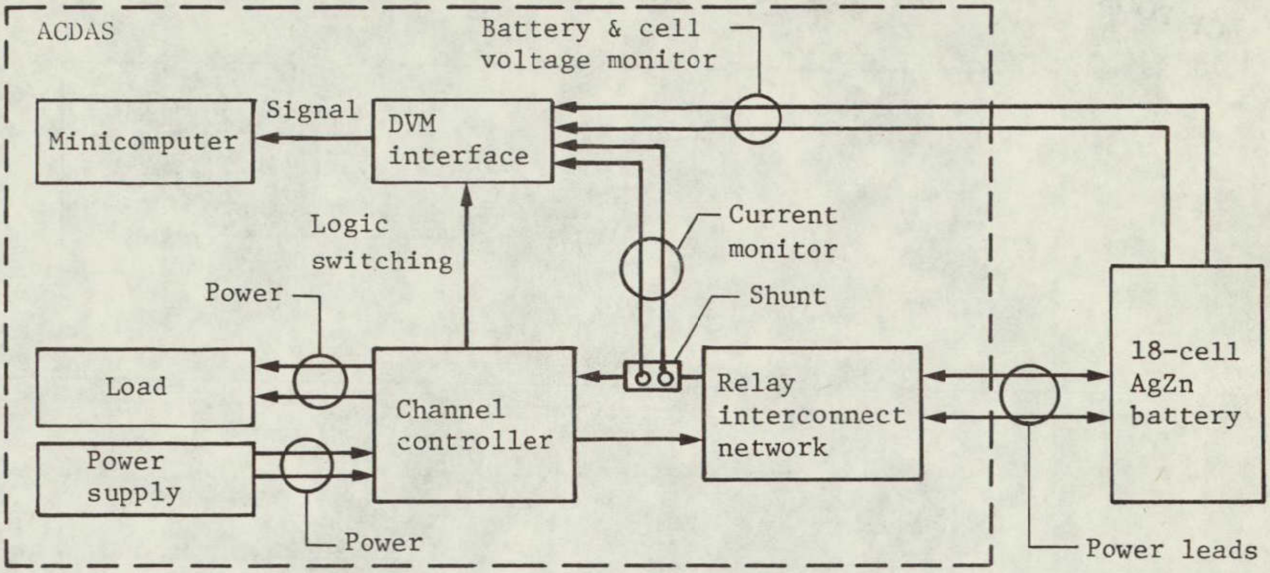
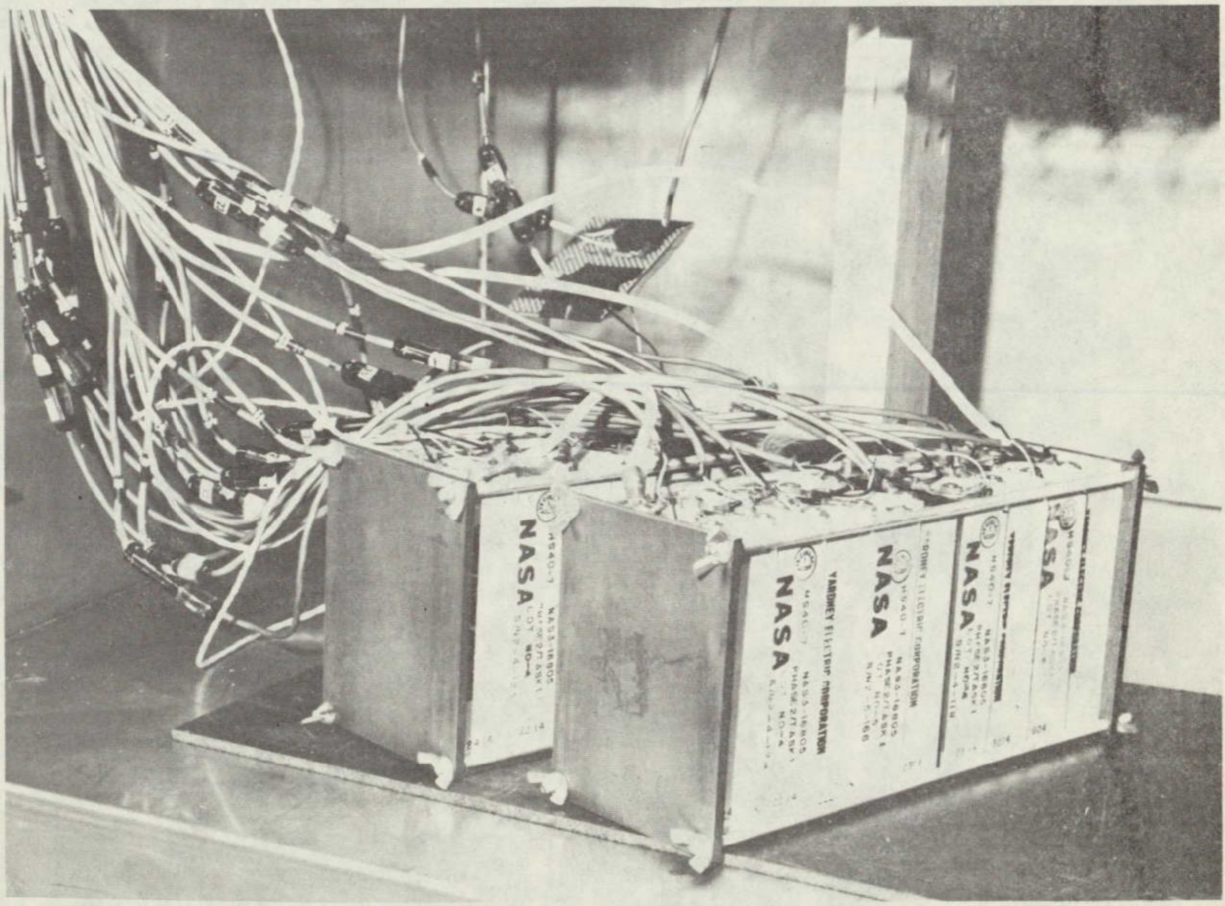


Functional block diagram



Group II battery in temperature chamber.

Figure 12. - Group II battery/ACDAS test setup.

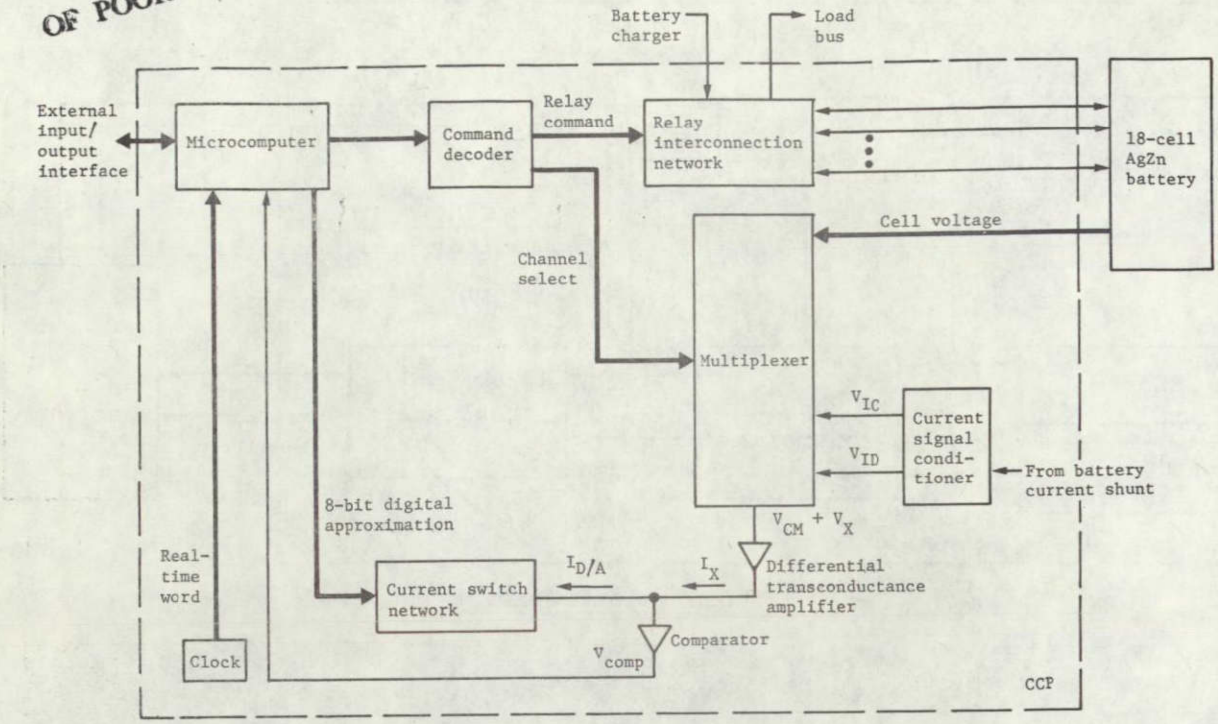


Figure 13. - Block diagram of test setup for 10-cell battery under microprocessor control.

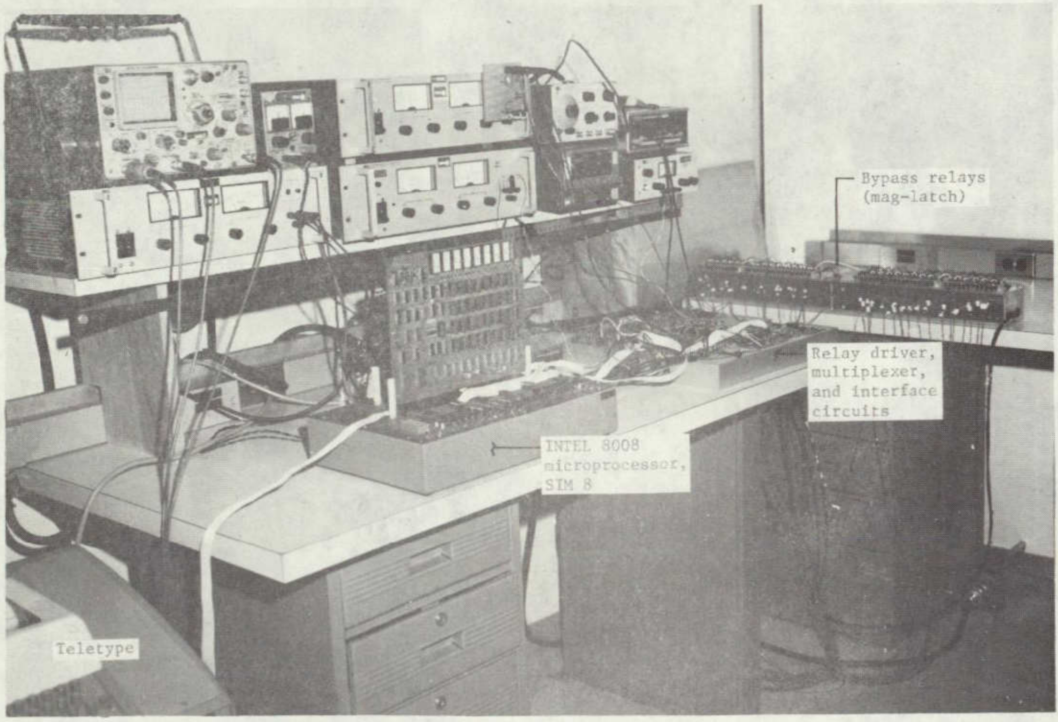


Figure 14. - Breadboard microprocessor-based protector test setup for 10 AgZn cells.

The following data were acquired and stored on the ACDAS magnetic tape:

Battery voltage;

Battery current;

Cell voltage;

Battery temperature;

Number of cycles.

Battery data were automatically recorded every 10 minutes during charge and every 5 minutes during discharge. Also, the end of charge and discharge voltages were recorded.

4.4 Failure and Test Continuation Criteria. - Test failure is the point at which all cells in the batteries will not perform within the limits of the test regime. As failure of a cell occurs, the cell will be removed and the test continued until the end of the contract period. For the SCP-controlled battery the bypass circuit provides the necessary bypass function in case a cell fails. When any anomaly or failure occurs, the LeRC project manager will be contacted within one working day. Any changes to the test condition or configuration will be verbally coordinated and approved by the LeRC project manager or his representative before implementing the changes and continuing the test.

4.5 Results and Discussion

Cell Matching Phase I and Phase II. - Tables VI and VII summarize the capacity obtained for the Phase I and II cells. Figure 16 shows the capacity distribution of the Phase I cells plotted on statistical probability graph paper. Figure 17 shows the same data on Phase II cells. When data are plotted on probability graph paper, statistical parameters such as standard deviation and mean value can be readily obtained.

The average capacity of the Phase II cells (41 cells) was 34.15 Ah with a standard deviation in capacity of 3.15 Ah. The total capacity dispersion was a maximum of 5.4 Ah. The mean capacity degradation of the 41 cells in three months of activated life was 0.5 Ah. Note that in Figure 18 the Phase II cells (second generation) data show a lower capacity and a wider dispersion among the 41 cells.

Two 18-cell battery groups were selected from this 41-cell lot. Selection of the cells was based on the closest grouping in capacity. The MCP battery cell capacity ranged from 34.5 to 37.8 Ah. The battery level cell capacity ranged from 33.47 to 34.47 Ah. These data are plotted in Figures 19 and 20, respectively.

Cell matching test conditions were identical to those of Yardney Electric Corporation (YEC) during their postmanufacturing formation and acceptance test. The secondary objective of the matching test was to determine the extent of possible cell degradation by comparing the capacity data obtained by YEC in August 1976 and Martin Marietta in October 1976.

TABLE VI. PHASE I CAPACITY DATA

Cell S/N	Cycle 1, Ah	Cycle 2, Ah	Avg cap., Ah	Battery Test Group
4-108	39.833	43.267	41.550	Group I
4-113	39.833	43.185	41.509	
4-136	39.833	42.919	41.376	
4-134	39.833	42.769	41.301	
4-131	39.833	42.703	41.268	
4-127	39.833	42.637	41.235	
4-132	39.833	42.504	41.169	
4-137	39.833	42.354	41.094	
5-162	39.833	42.188	41.011	
4-121	39.833	42.121	40.977	
5-146	39.833	41.855	40.844	
4-133	39.833	41.838	40.836	
5-163	39.833	41.672	40.753	
4-111	39.833	41.655	40.744	
4-116	39.833	41.605	40.719	
4-119	39.833	41.555	40.694	
5-165	39.833	41.539	40.686	
4-107	39.833	41.539	40.685	
5-158	39.833	40.572	40.203	
5-164	39.800	40.539	40.170	
4-130	39.833	41.522	40.678	Group II
5-160	39.833	41.522	40.678	
4-117	39.833	41.456	40.645	
4-120	39.833	41.356	40.595	
5-147	39.833	41.356	40.595	
4-109	39.833	41.289	40.561	
4-115	39.833	41.141	40.487	
4-123	39.833	41.122	40.478	
4-125	39.833	41.072	40.453	
4-135	39.833	14.038	40.436	
4-124	39.833	40.989	40.411	
5-167	39.833	40.989	40.411	
5-166	39.833	40.956	40.394	
5-161	39.833	40.922	40.378	
4-118	39.833	40.806	40.320	
5-171	39.833	40.706	40.270	
5-149	39.833	40.656	40.245	
4-126	39.833	40.639	40.236	
5-173	39.833	40.639	40.161	Group IV[a]
4-122	39.833	40.205	40.019	
5-148	39.833	40.039	39.936	
5-159	39.715	40.039	39.877	
5-169	39.443	40.172	39.808	
5-156	39.833	39.705	39.769	
5-172	39.833	39.621	39.727	
5-157	39.359	40.089	30.720	
4-112	39.833	39.421	39.627	
4-129	39.833	39.021	39.427	

[a] Microprocessor-controlled pack, See para 4.2.

TABEL VII.-PHASE II CELL CAPACITY DATA

Phase II Evaluation (LeRC)

MCP Cell Selection

HS 40-14, 40-Ah AgZn Cells, Inorganic Separator

Position	Cell S/N	Average Capacity
1	032	37.443
2	031	37.269
3	041	37.233
4	035	37.174
5	040	37.119
6	037	36.953
7	039	36.645
8	034	36.617
9	038	36.399
10	036	36.188
11	033	36.050
12	006	35.770
13	004	35.746
14	019	35.445
15	008	34.936
16	017	34.898
17	003	34.711
18	007	34.481
19	018	34.477 (Spare)
20	030	34.477 (Spare)

TABLE VII (concluded)

Phase II Evaluation (LeRC)

Battery Assembly Cell Selection

HS 40-14, 40-Ah AgZn Cells, Inorganic Separatpr

Position	Cell S/N	Average Capacity
1	022	34.171
2	025	34.168
3	016	34.148
4	011	34.068
5	026	34.056
6	013	33.987
7	020	33.972
8	009	33.971
9	028	33.953
10	023	33.863
11	014	33.786
12	012	33.719
13	015	33.701
14	024	33.645
15	001	33.590
16	021	33.534
17	002	33.505
18	010	33.475
	Spare Cells	
1	005	33.378
2	029	32.682
3	027	32.062

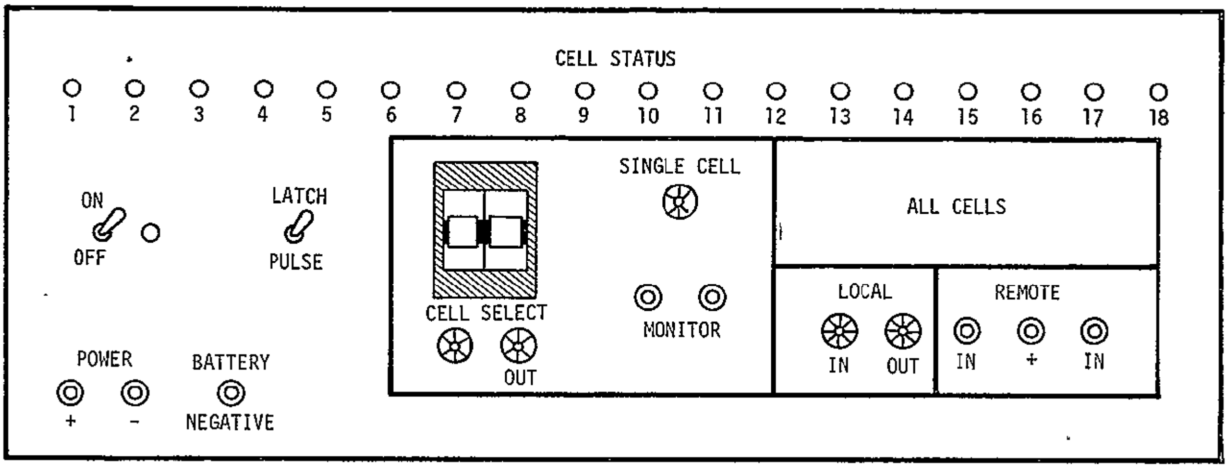


Figure 15. - Control and display panel for MCP.

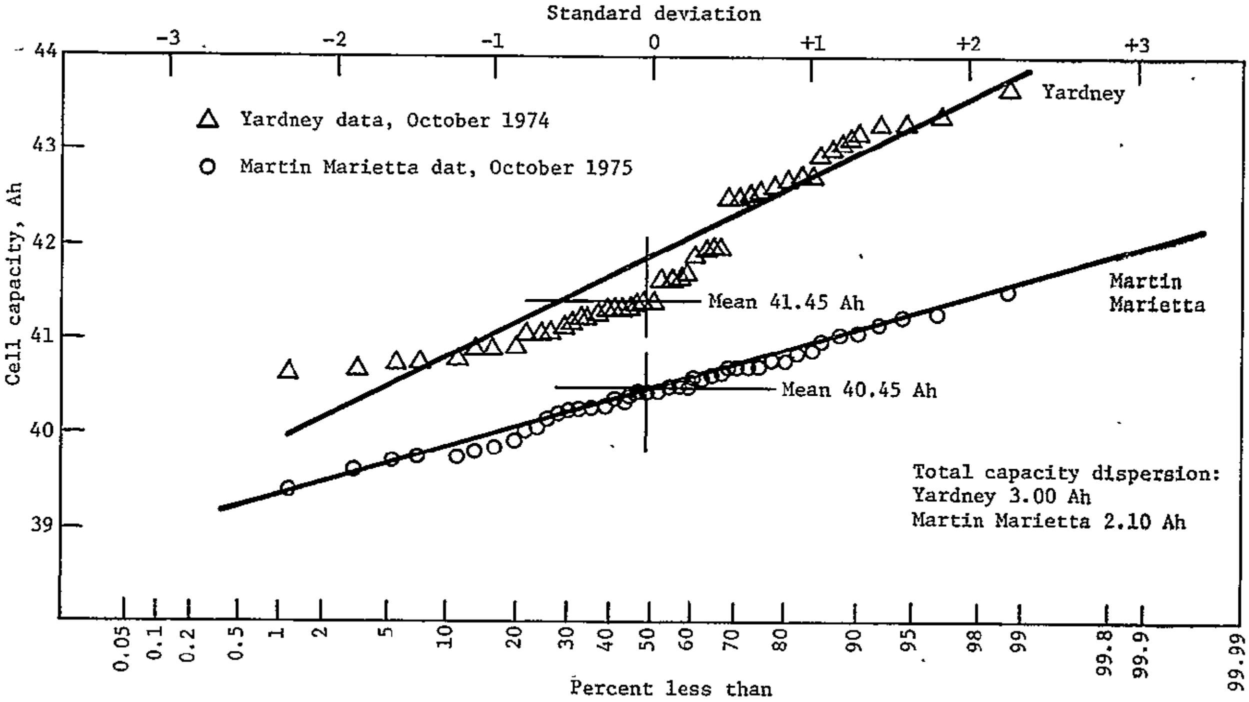


Figure 16. - Comparison of Yardney and Martin Marietta data on 48 cells, Phase I.

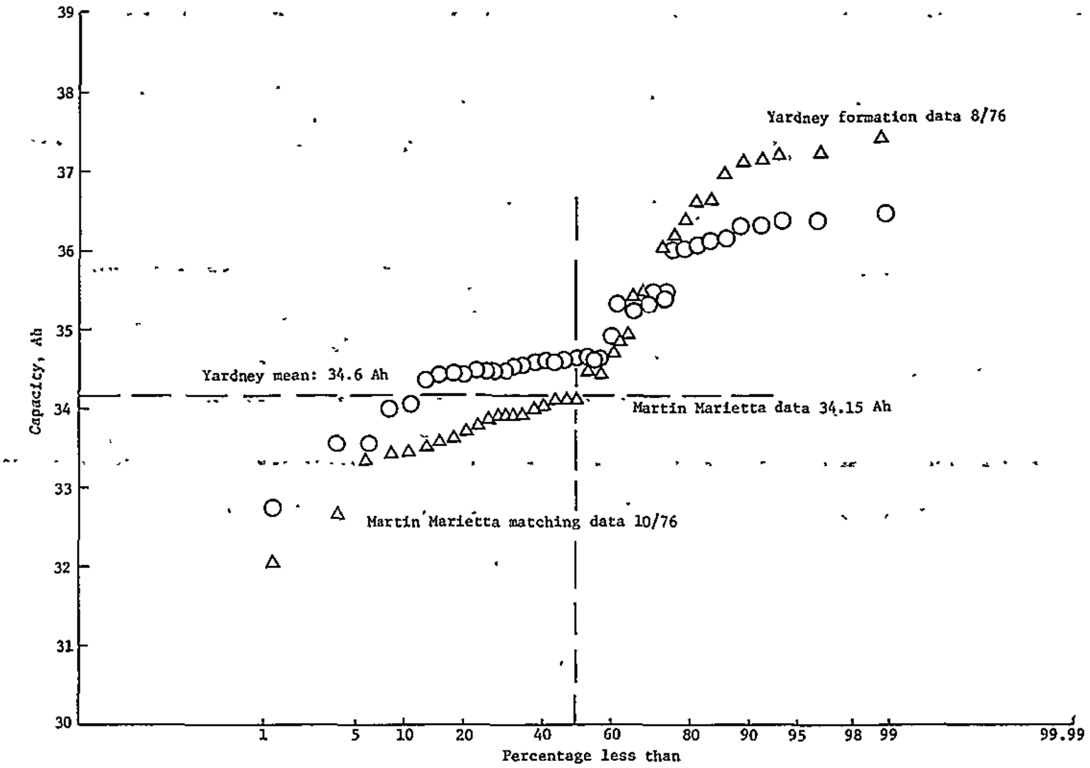


Figure 17. - Comparison of Yardney and Martin Marietta capacity data on 40 cells.

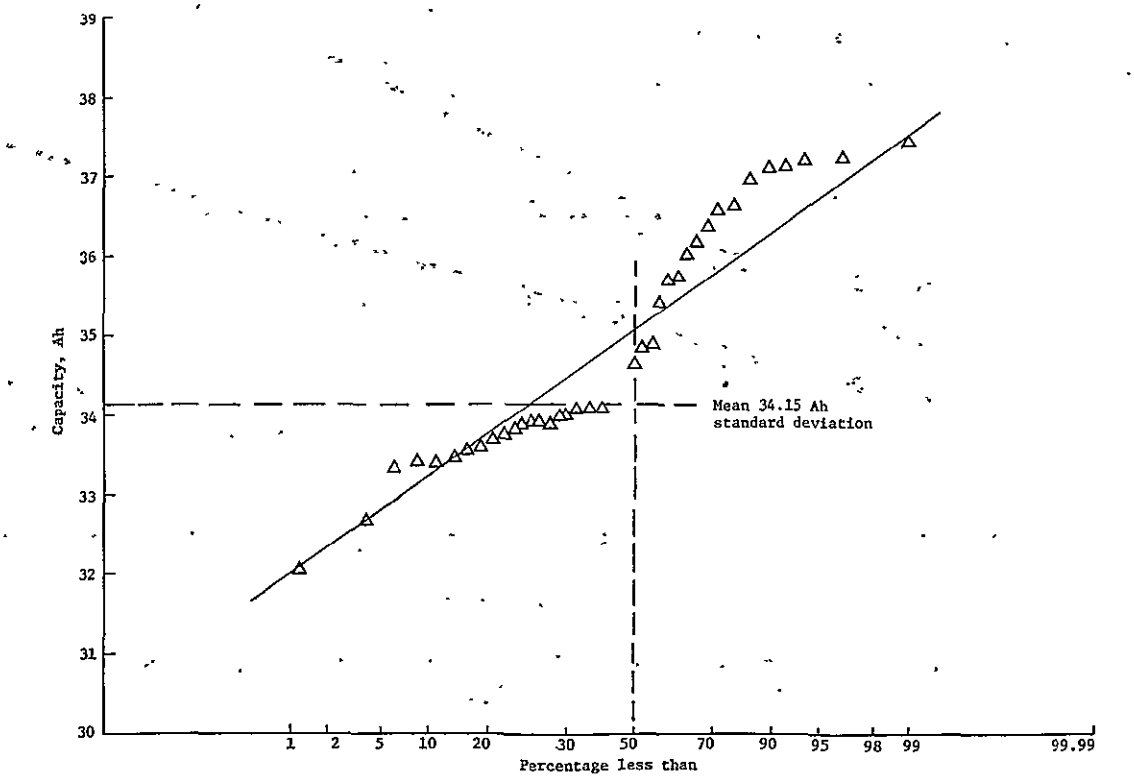


Figure 18. - Capacity distribution of forty-one, HS40-14 cells.

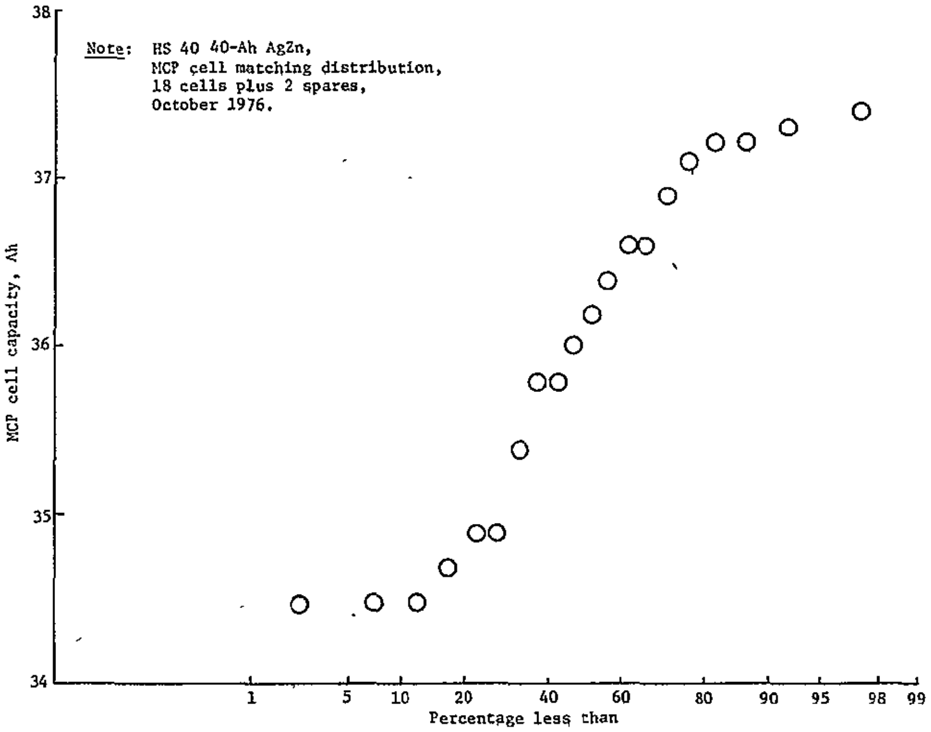


Figure 19. - MCP battery cell capacity distribution.

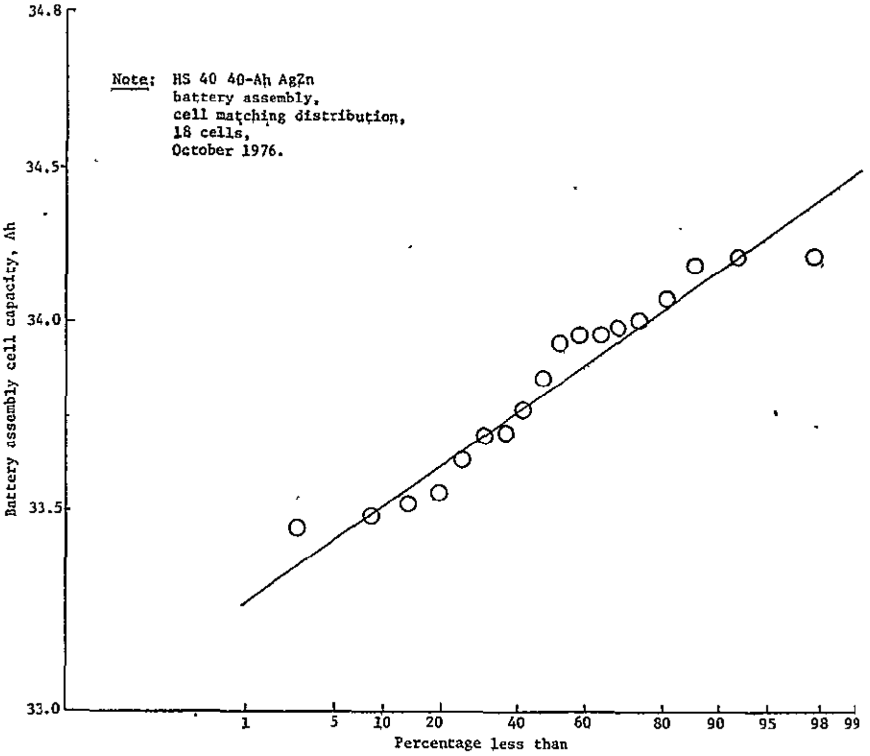


Figure 20. - Capacity distribution of cells for battery pack.

SCP Configuration. - A total of 540 cycles were completed on the SCP-controlled battery assembly. Figure 21 shows the distribution of cell failures as a function of cycle life. Figure 20 is a plot of the average end of charge voltage (EOC). Although the cells were fully charged initially (45 Ah input), it required 12 full cycles before all cells reached the voltage limit. During the first 12 cycles, the cells operated under an average ampere hour recharge fraction (RF) of 1.07. The voltage limit of each SCP was adjusted at this point to a limit of 1.98 V/cell. This change was the result of a pressure test evaluation, which indicated that 1.98 V per cell will prevent pressure buildup in a cell. Operation at 1.98 V per cell limit resulted in an ampere hour RF of 1.02. Again 12 full cycles were required before the cells reached 1.98 voltage limit. Voltage limiting continued throughout the life of the SCP testing. All 18 SCPs operated for the total life test without any failures.

Figure 23 shows the EOC voltage deviation for the SCP battery assembly. The large deviation during the early cycles (1 thru 12) is mainly attributed to the higher voltage limit of 2.0 V per cell and the fact that only a few cells reached voltage limit during the time.

Figure 24 shows the average end of discharge (EOD) voltage for the cells. Figure 25 shows the end of discharge voltage dispersion. It can be seen that the EOD dispersion spread generally increases with cycling. Figure 26 shows the average ampere hour and watt hour recharge fraction for the SCP battery cell assembly.

Figures 27 and 28 show the typical charge/discharge voltage profile as a function of cycle life. As expected, the time required to reach the peroxide level decreased with cycling.

A partial failure of the battery-level control pack occurred at cycle 345 with total battery failure at cycle 536. Figure 29 shows the cell failure as a function of cycle life. The first twelve cycles were conducted at a voltage limit of 36.0 Vdc or an average of 2.0 Vdc per cell. As with the SCP assembly, the charge voltage limit was reduced to 35.64 Vdc (1.98 V per cell) on the 13th cycle and this limit was held until battery failure. On cell failure and removal, the voltage was adjusted equivalent to 1.98 Vdc per number of cells under test.

Figures 30 and 31 show the battery EOC and maximum deviation 10 cell EOC voltage, respectively, as a function of cycle. Figures 32 and 33 show the battery EOD voltage and battery cell EOD voltages as a function of cycling. The recharge fraction data with cycling is shown in Figure 34.

CCP Configuration. - The 10 spare cells of Phase I were breadboard-tested with the CCP. A total of 446 cycles were completed on the cells under CCP control. Figure 35 shows the distribution of the cell failures as a function of cycle life. Unlike the SCP/battery testing, the voltage limit of 1.98 V per cell was set at the onset of the test. A plot of the average EOC voltage is shown in Figure 36.

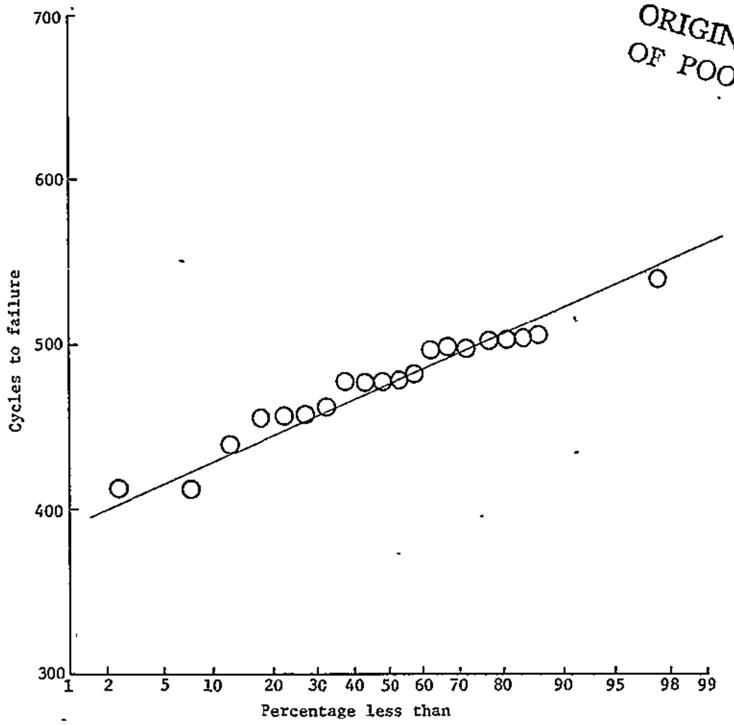


Figure 21. - Cell failure after test start, Group I (SCP control group).

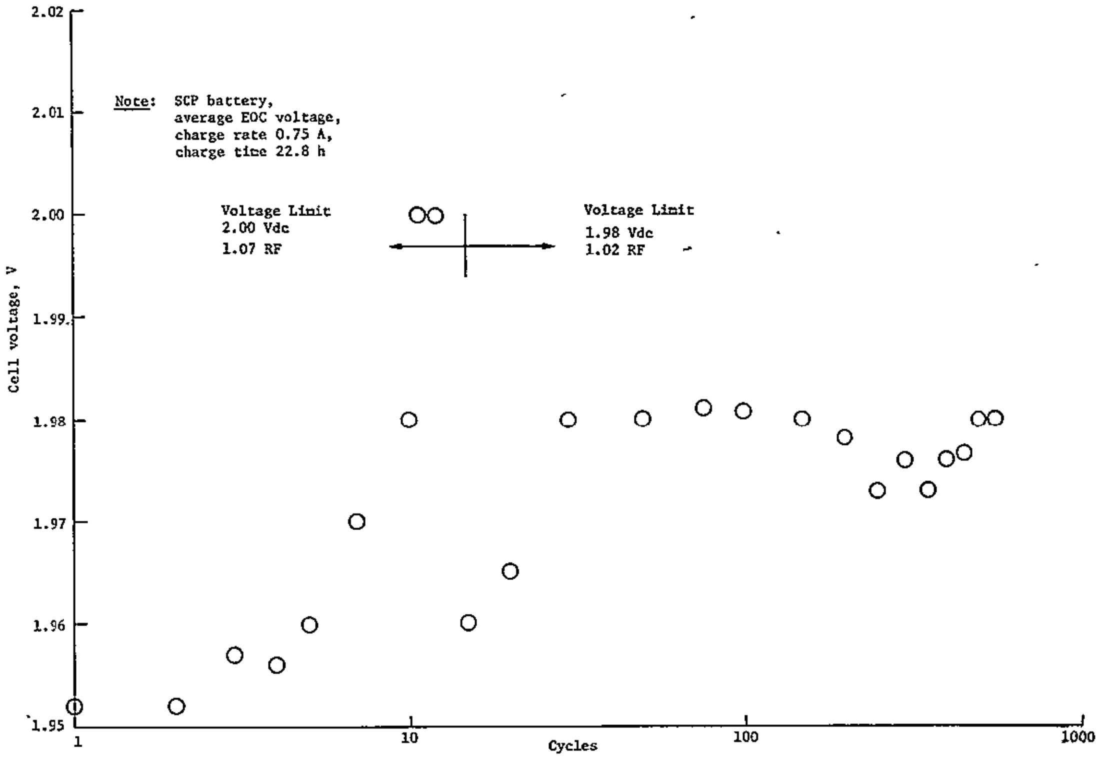


Figure 22. - Average end of charge voltage for SCP-controlled cells.

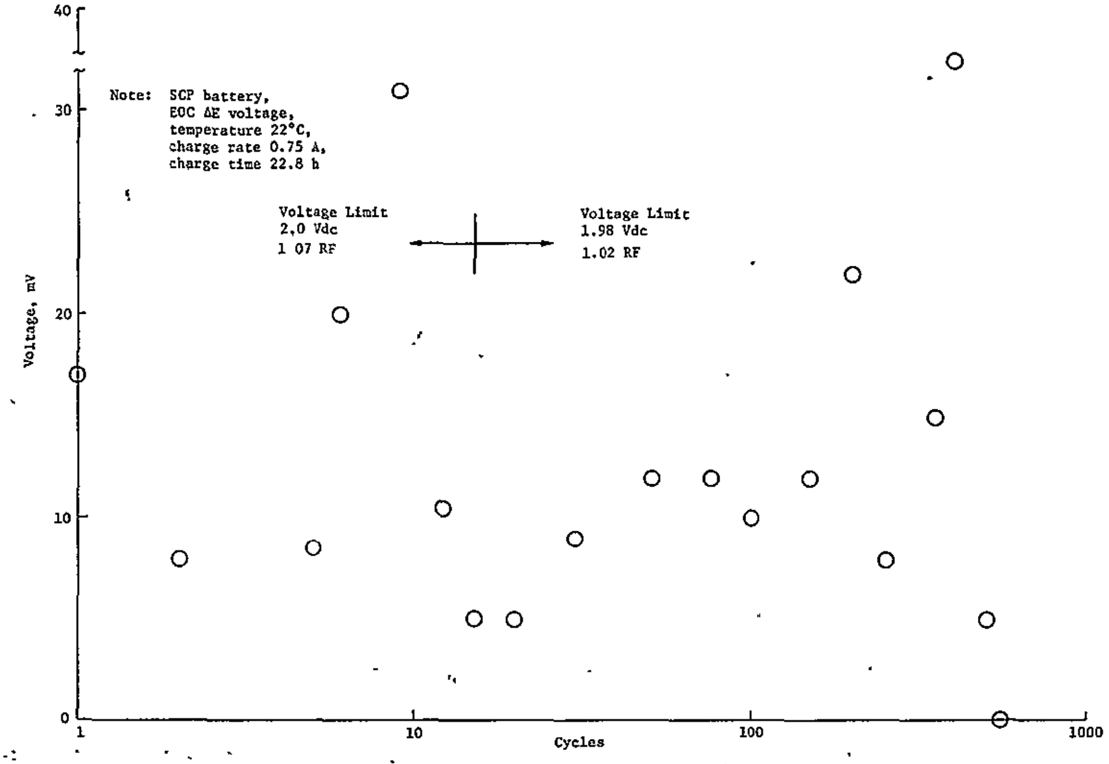


Figure 23. - Maximum cell EOC voltage deviation for cells in SCP battery.

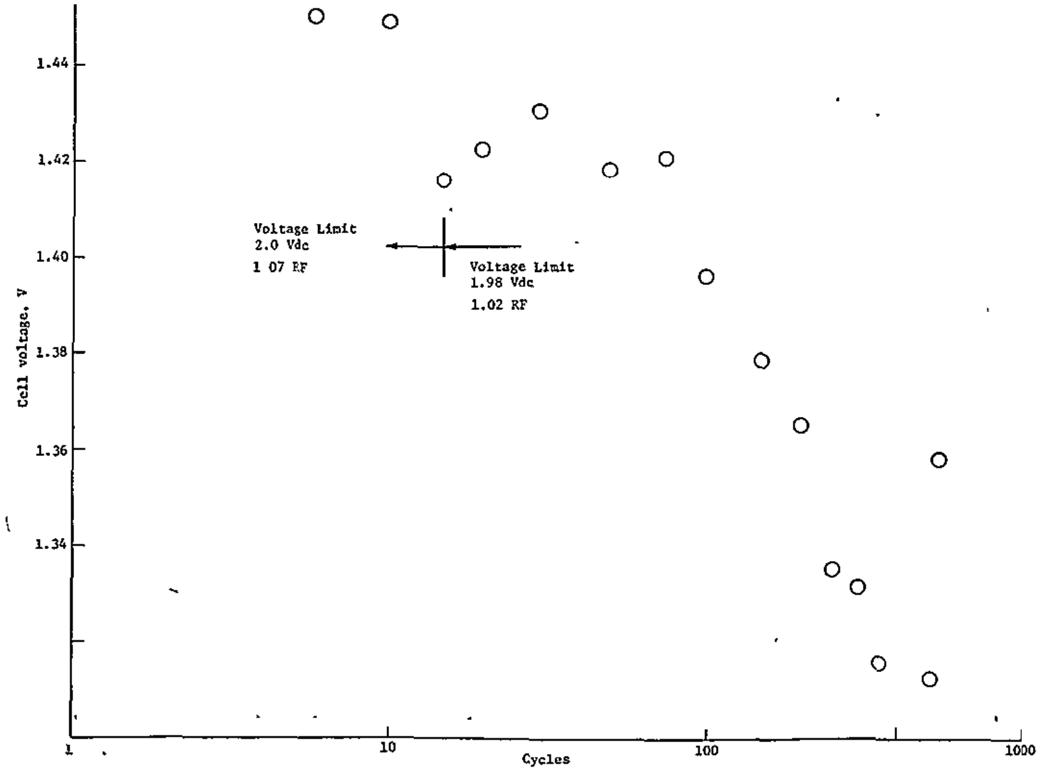


Figure 24. - Average end of discharge cell voltage for SCP battery.

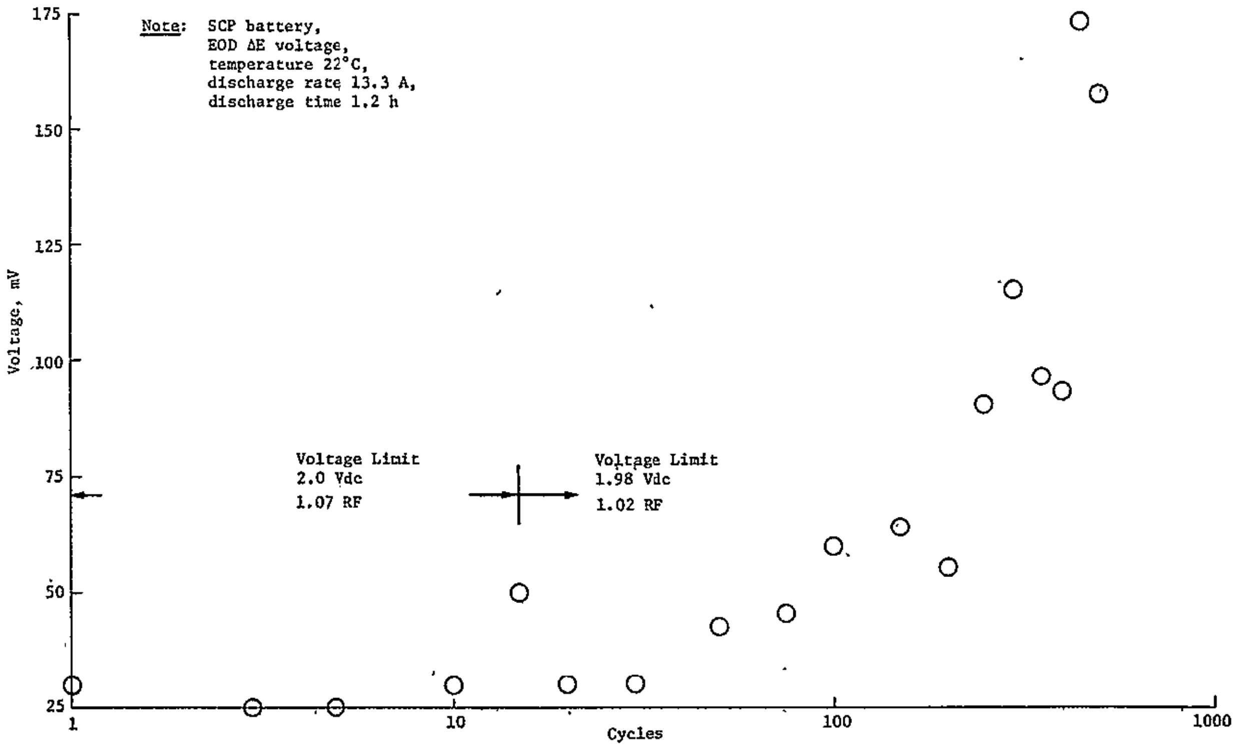


Figure 25. - Maximum cell EOD voltage dispersion for SCP battery.

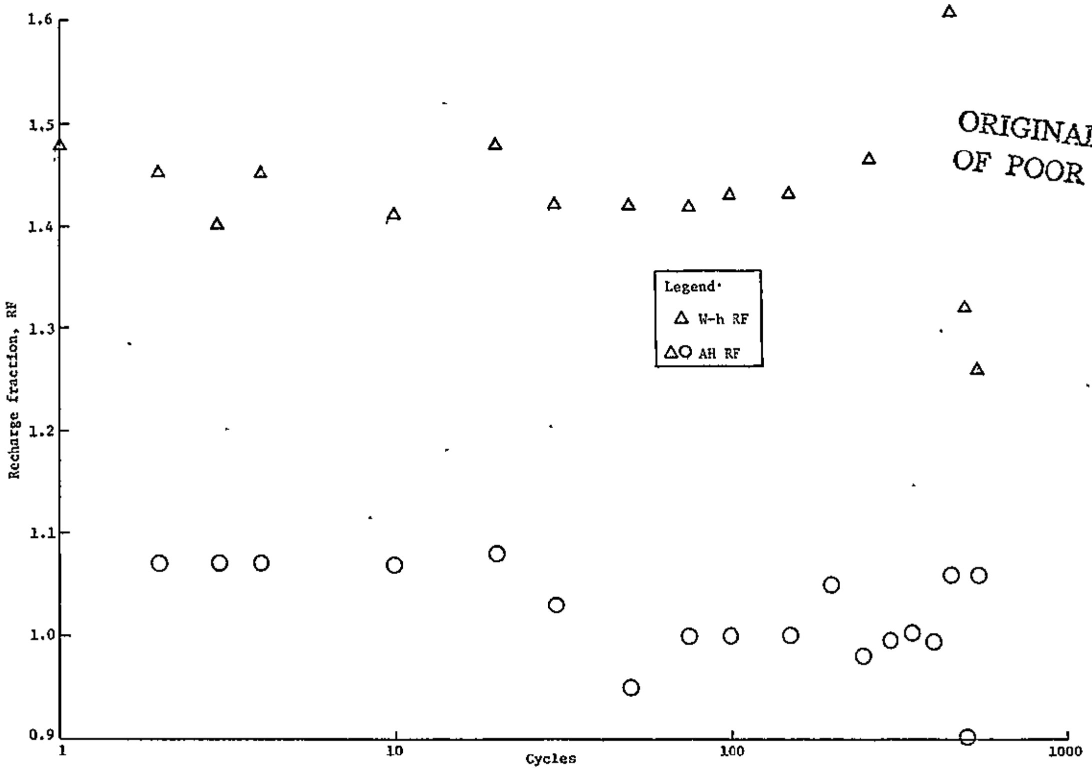


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Figure 26. - Recharge fraction for SCP battery.

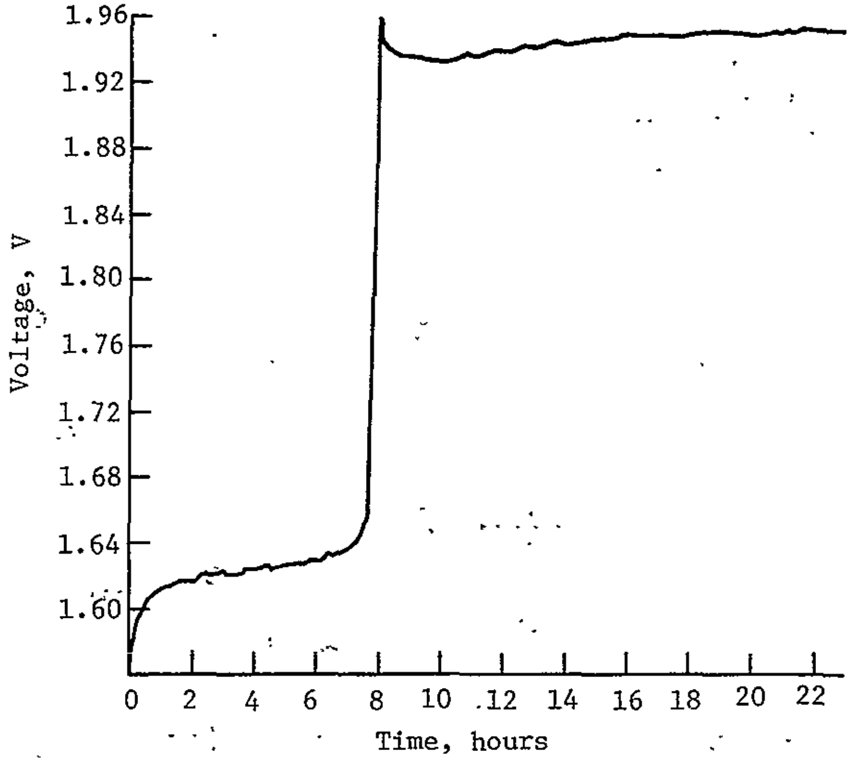


Figure 27. - Charge profiles.

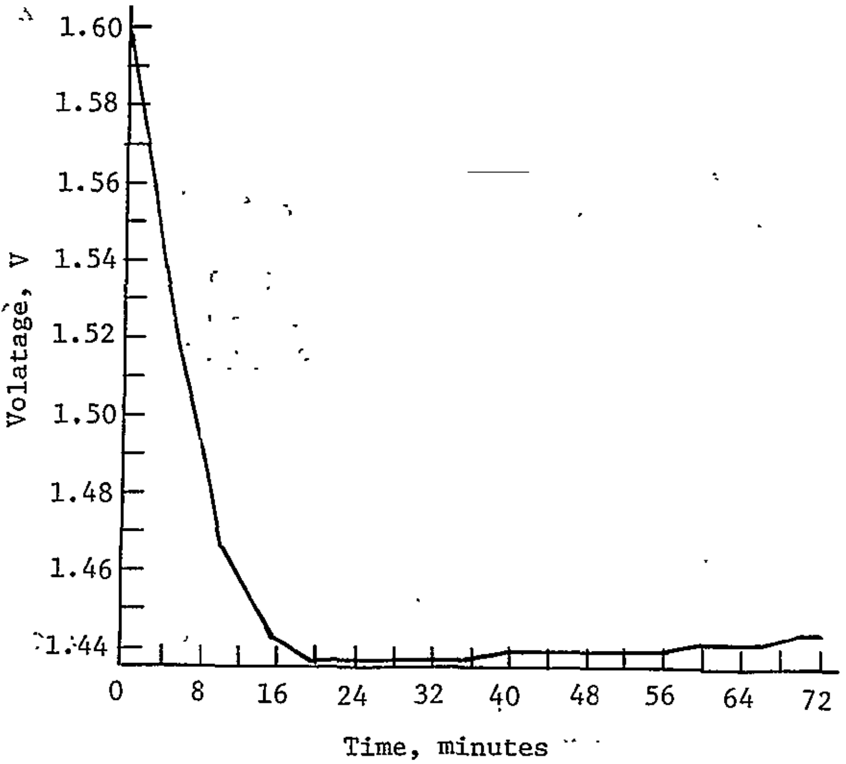


Figure 28. - Dicharge profiles.

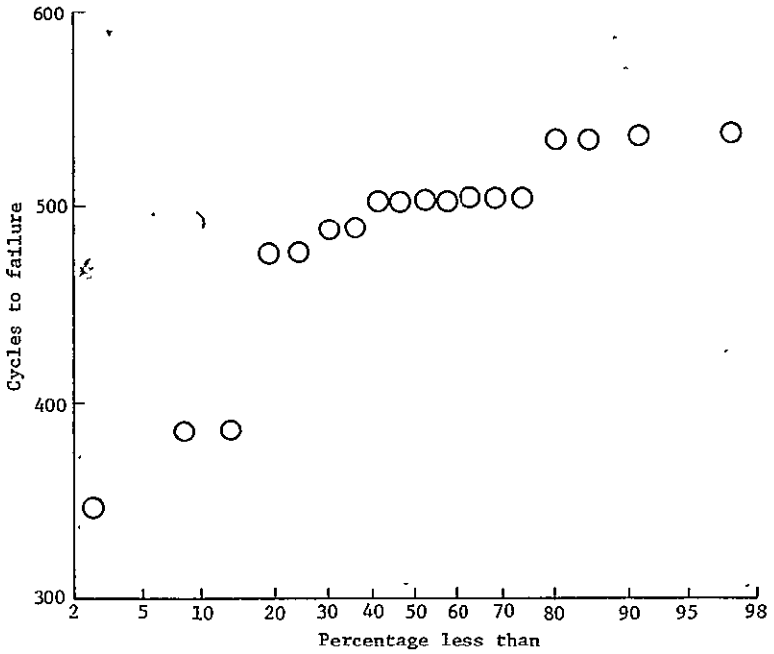


Figure 29. - Cell failure after test start, Group II (battery level).

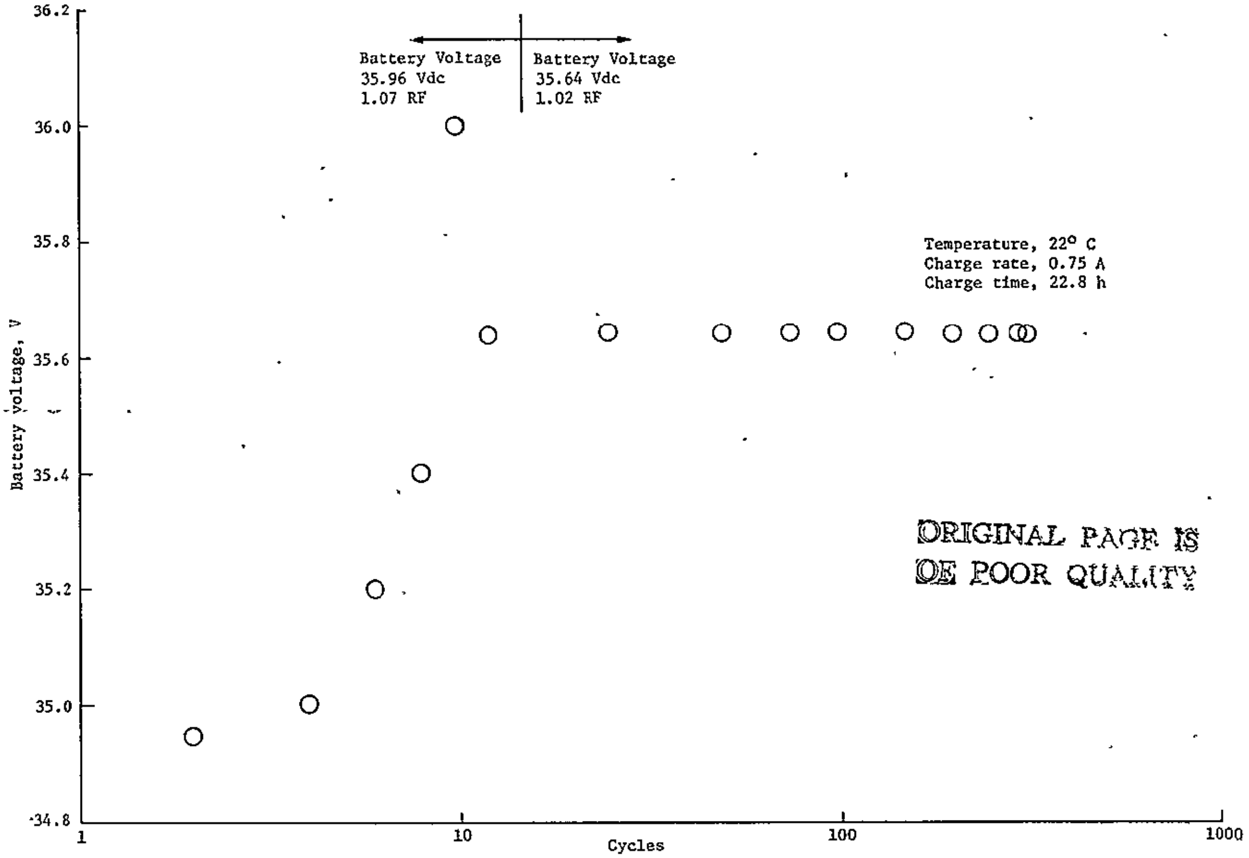


Figure 30. - End of charge battery voltage, battery level control pack (Group II).

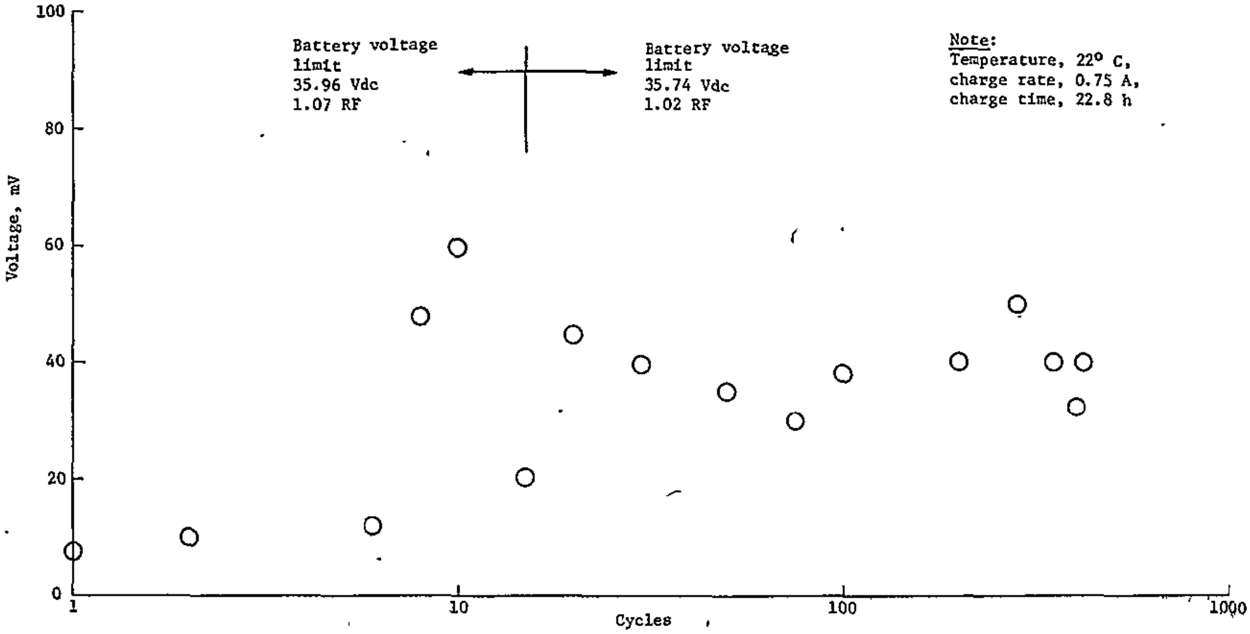


Figure 31. - Maximum EOC cell voltage deviation, battery level.

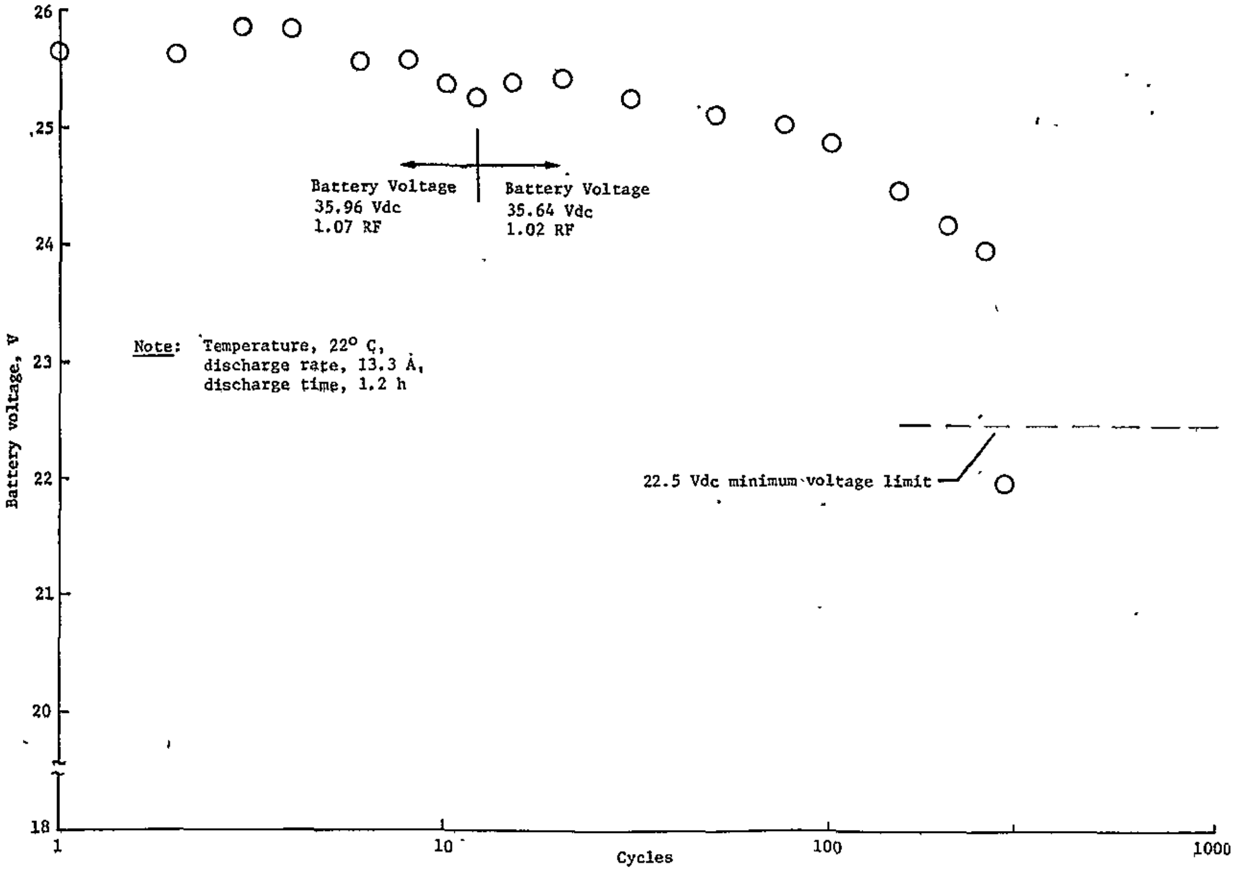
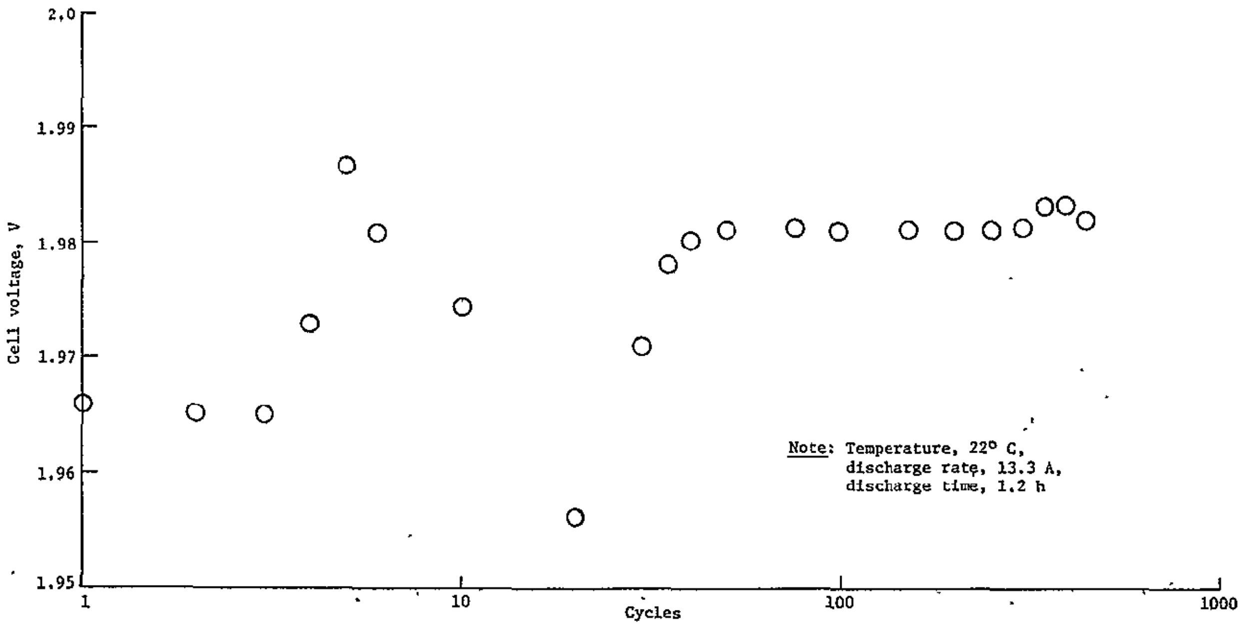


Figure 32. - Battery level control pack (Group II).



Note: Temperature, 22° C,
discharge rate, 13.3 A,
discharge time, 1.2 h

Figure 33. - End of discharge voltage of cells in battery level control pack (Group II).

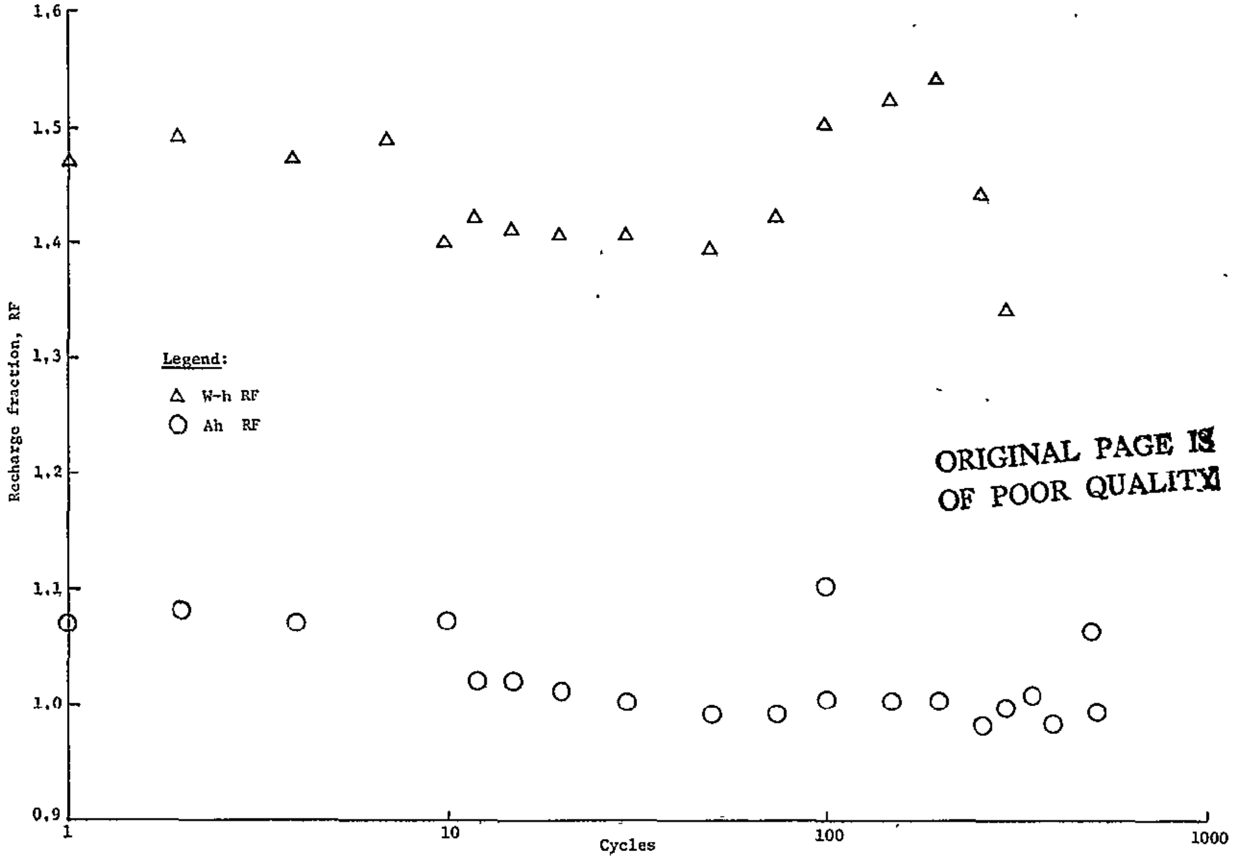


Figure 34. - Recharge fraction for battery level control pack (Group II).

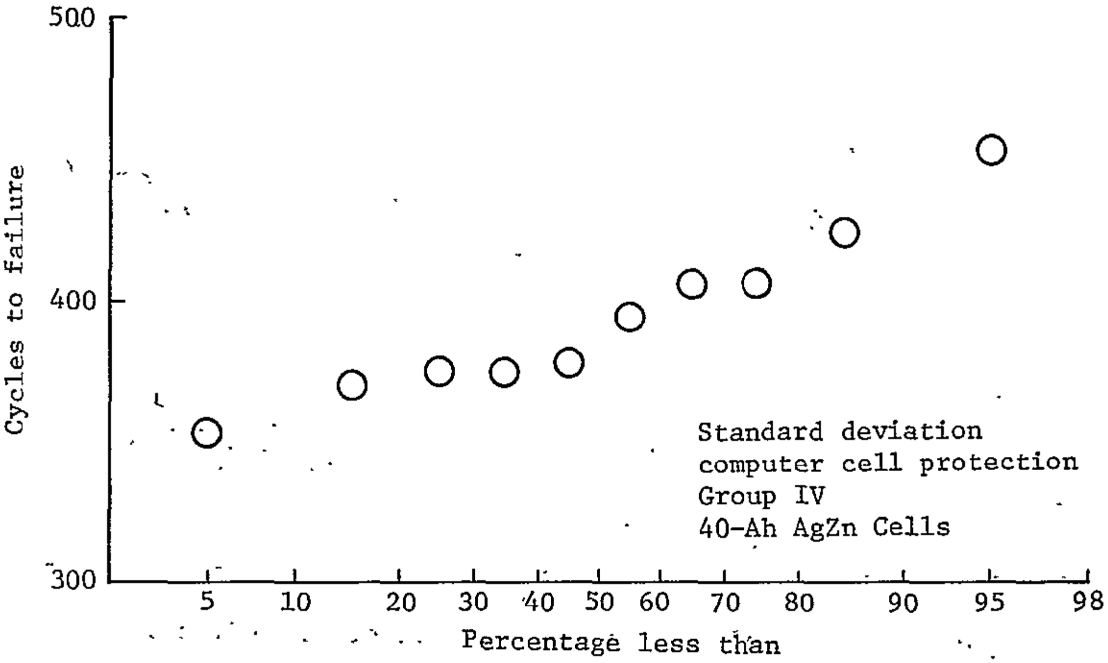


Figure 35. - Cell failure after test start for CCP control pack (Group II).

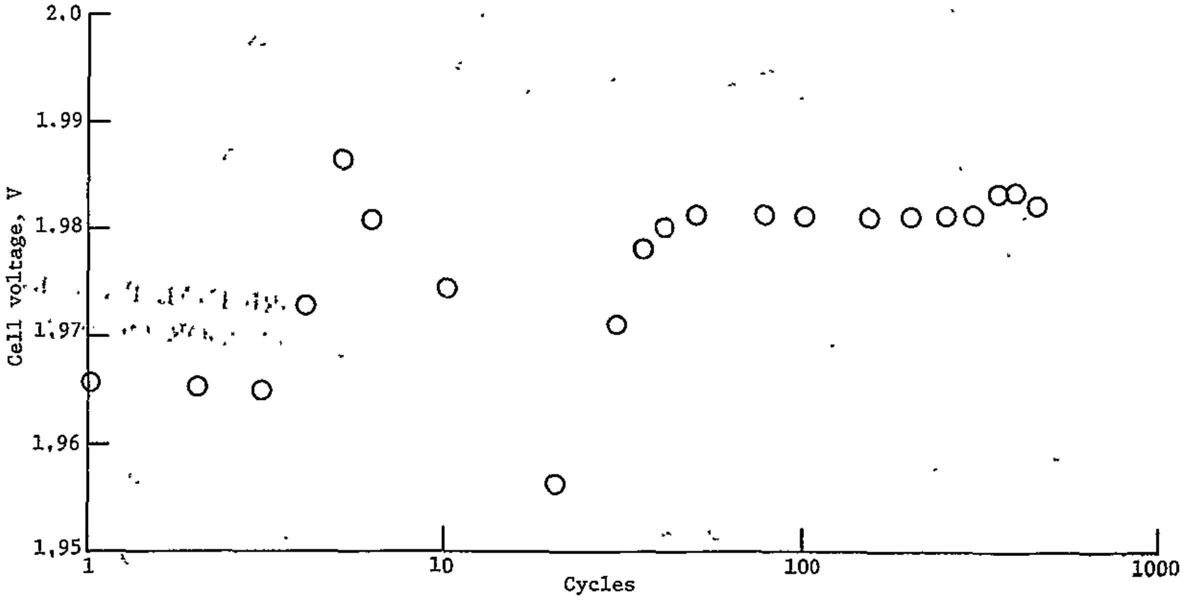


Figure 36. - End of charge voltage, CCP control pack.

Figure 37 shows the average deviation at EOC. Figure 38 shows the average EOD voltage for the 10 cells. End of discharge dispersion is shown in Figure 39. Figure 40 shows the average ampere hour and watt hour recharge fraction (RF) for the CCP cell test.

Degradation failure followed the same slope as those cells under SCP control, but failure occurred 58 cycles earlier. This short life span may be the result of manufacturing processes. It should be noted that the cells under CCP control were the spare cells from the initial lot.

MCP Configuration. - Life testing was still in progress at the completion of the Phase III contract April 18, 1978. A total of 415 cycles had been completed on the 18 cells without a component failure (cells or electronics). Figure 41 shows the plot of the average EOC voltage through 415 cycles of operation. Cell voltage deviation at EOC is shown in Figure 42. Figure 43 shows the average EOD voltage. The slope of the EOD curve is 2.2 x 10^{-4} V per cycle between 100 and 415 cycles. Figure 44 shows the EOD voltage dispersion. It can be seen that dispersion remained relatively constant with cycling. Figure 45 shows the average ampere hour and watt hour recharge fraction (RF).

In the battery-level control pack, the initial cell failure occurred on cycle 175 with a cell voltage dropping to -0.625 volts. The battery has completed 415 cycles at a voltage limit of 35.64 or 1.98 V per cell. Figure 46 shows the average EOC voltage. Figure 47 shows the average EOD voltage for the battery. It can be seen that the battery failure occurred between cycles 250 and 260. Cell EOD voltage profile is depicted in Figure 48.

End of Discharge voltage dispersion is not shown in that upon failure of the first cell (negative voltage) in the battery, the voltage dispersion exceeded 2.0 V from cycle 175. Figure 49 shows the ampere hour and watt hour recharge fraction (RF). It can be seen that after cell failure at cycle 175 the watt hour RF increased with cycling.

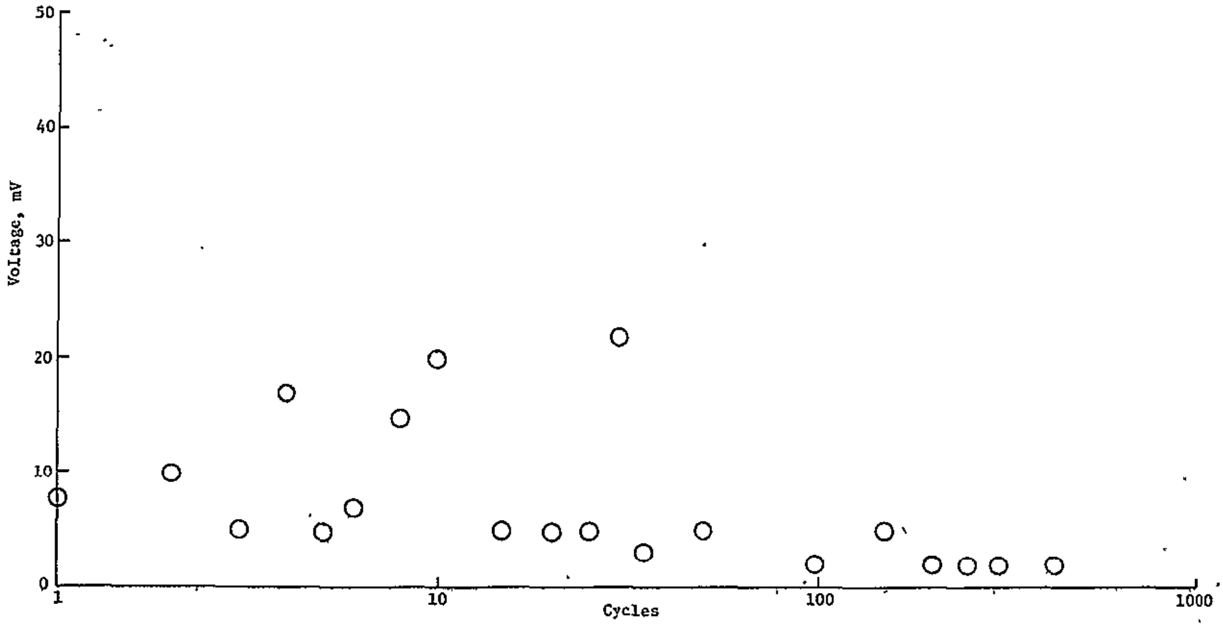


Figure 37. - Maximum deviation in EOC voltage, CCP control pack (Group III).

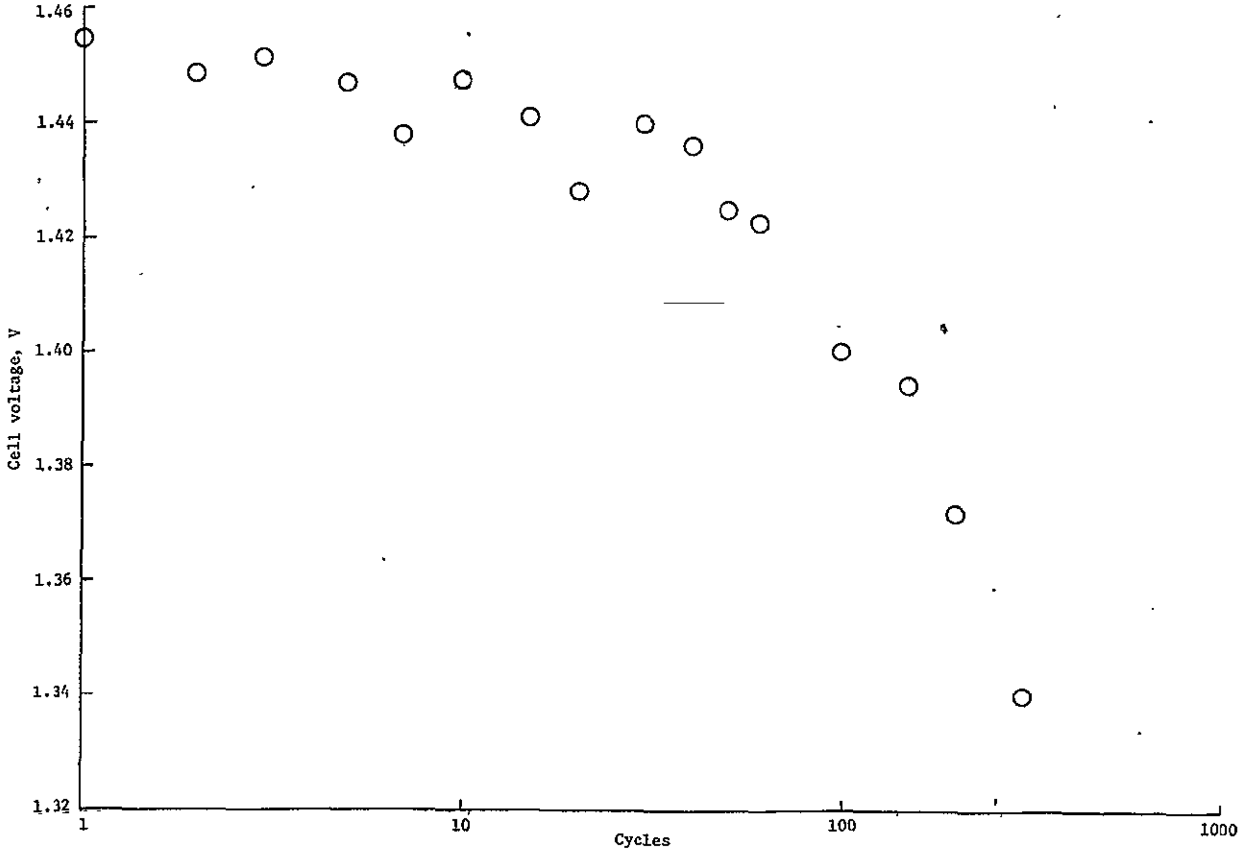


Figure 38. - Average end of discharge voltage for CCP control pack (Group III).

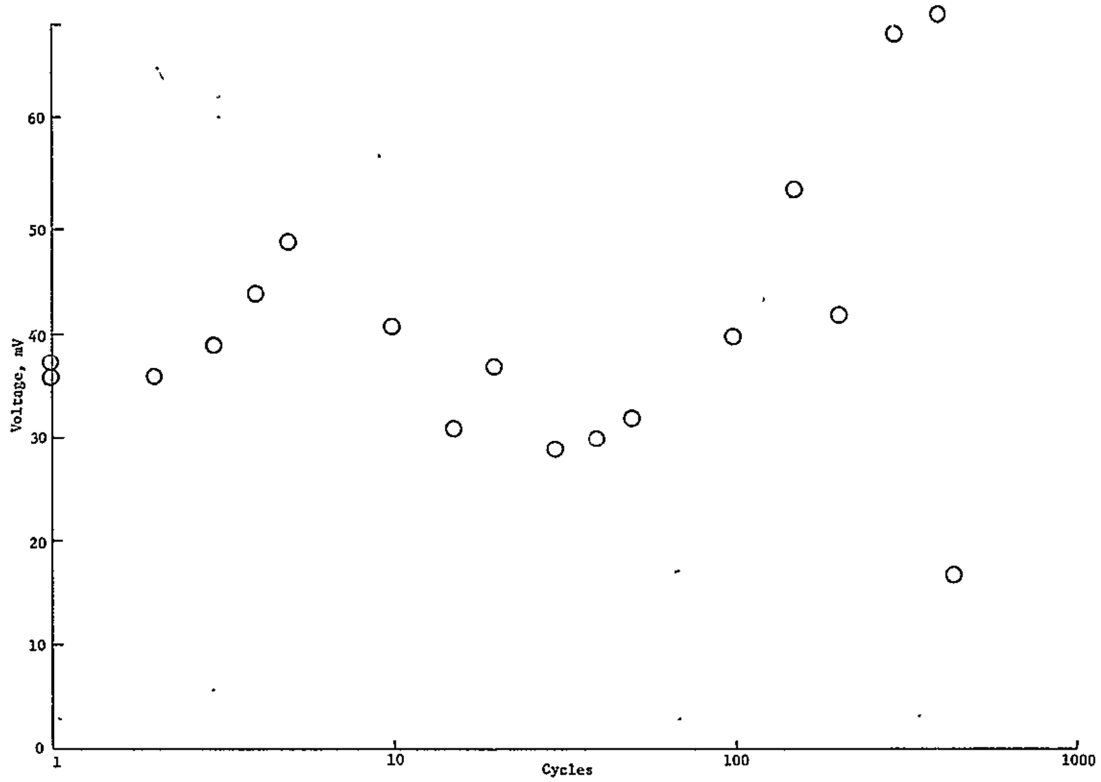


Figure 39. - Maximum deviation in end of discharge voltage of cells in CCP control pack (Group III).

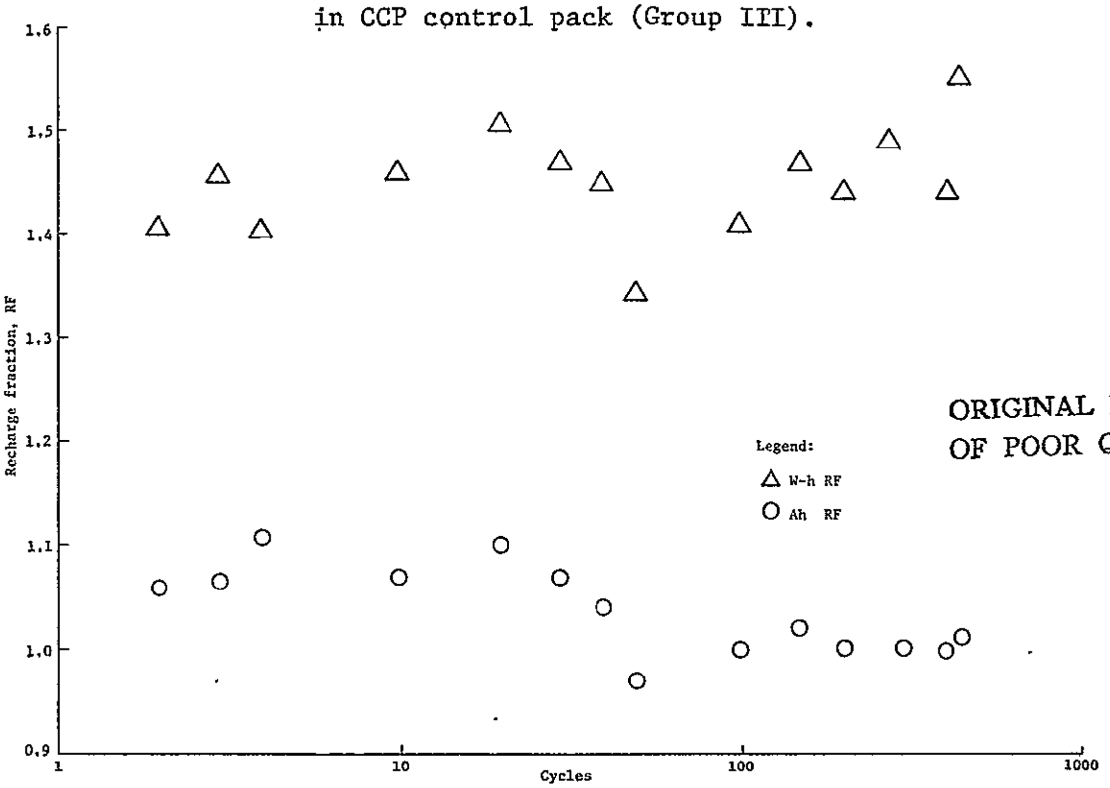


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Figure 40. - Recharge fraction, CCP control pack (Group III).

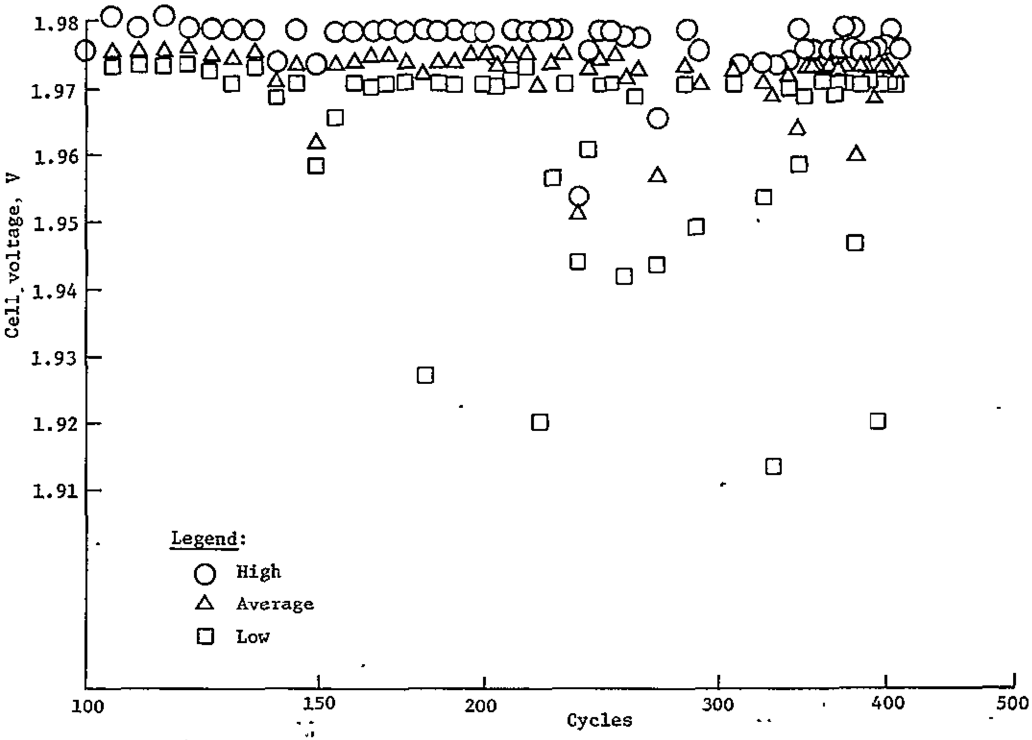


Figure 41. - End of charge voltage of cells, Group V (MCP).

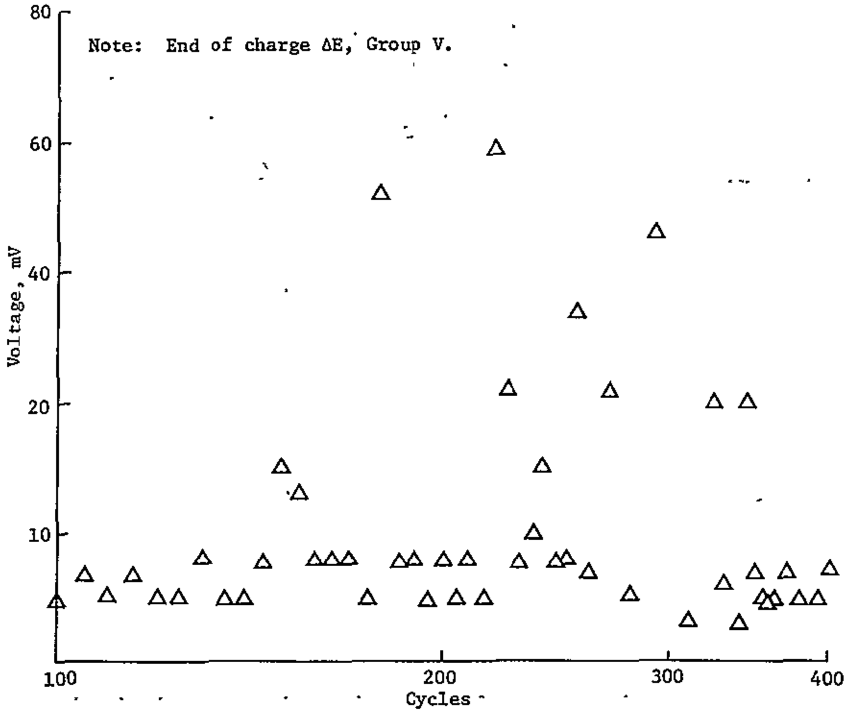


Figure 42. - Maximum deviation in EOC voltage of cells, Group V (MCP).

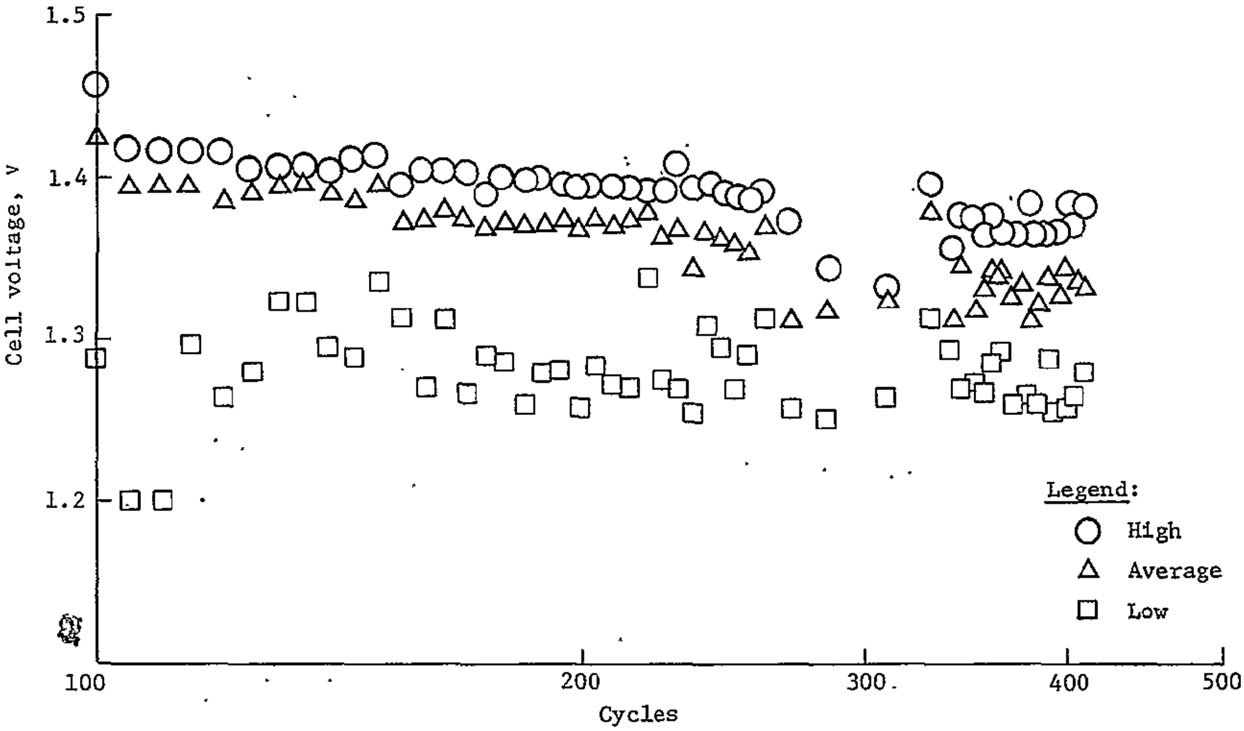


Figure 43. - End of discharge voltage of cells, Group V (MCP).

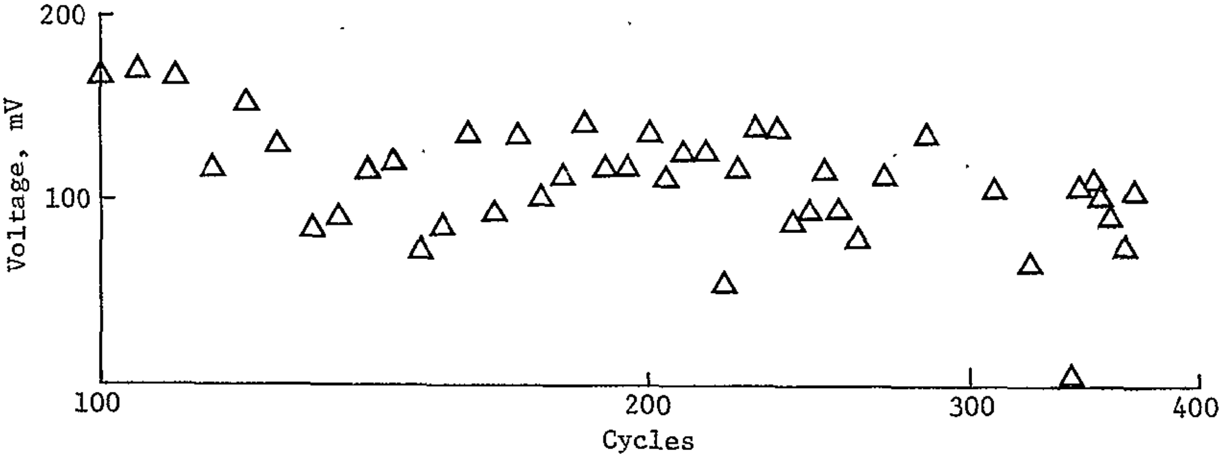


Figure 44. - Maximum deviation in end of discharge voltage of cells for MCP control pack (Group V).

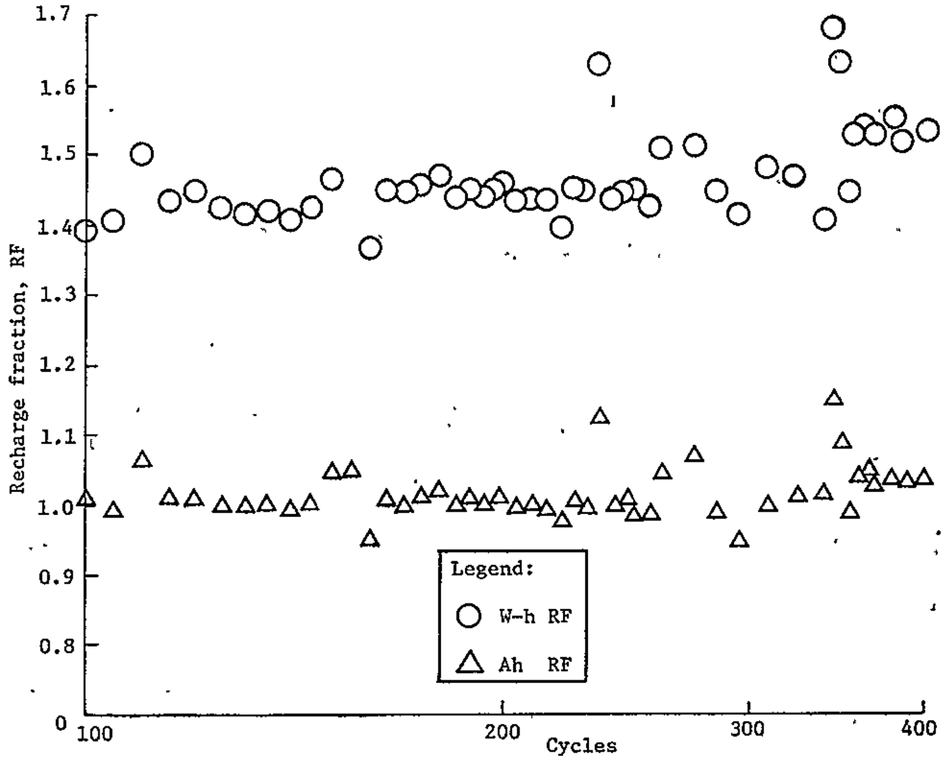


Figure 45. - Recharge fraction, ampere-hours and watt-hours for MCP control pack (Group V).

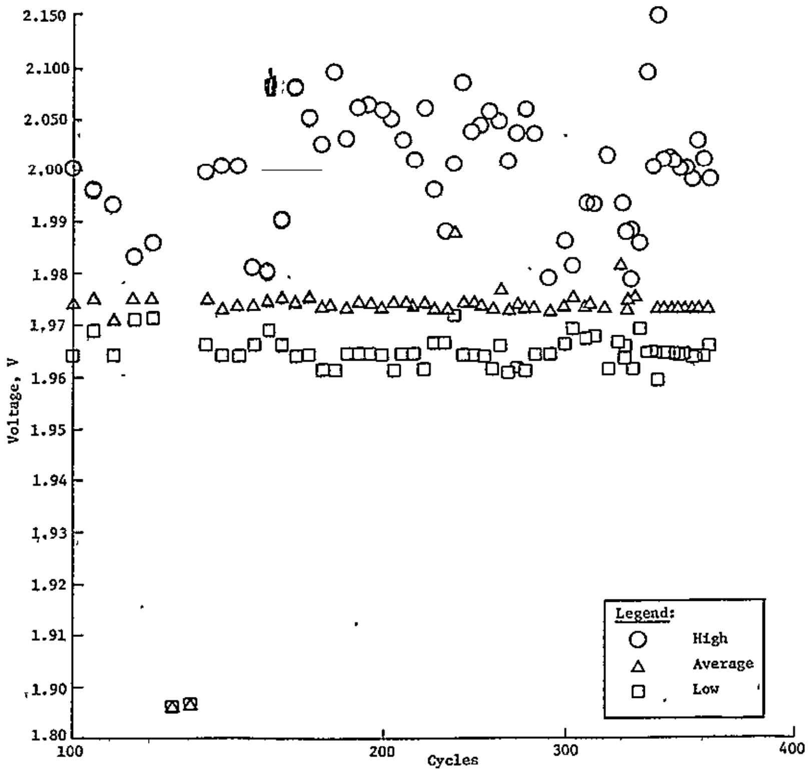


Figure 46. - End of charge voltage of cells, Group VI (battery level).

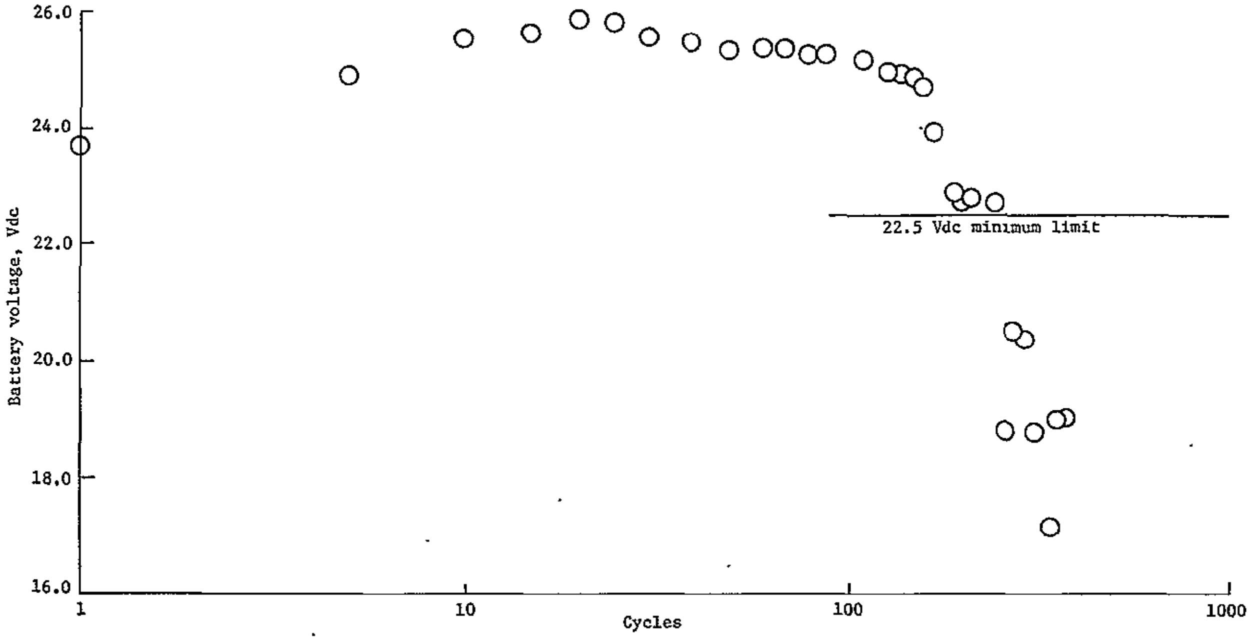
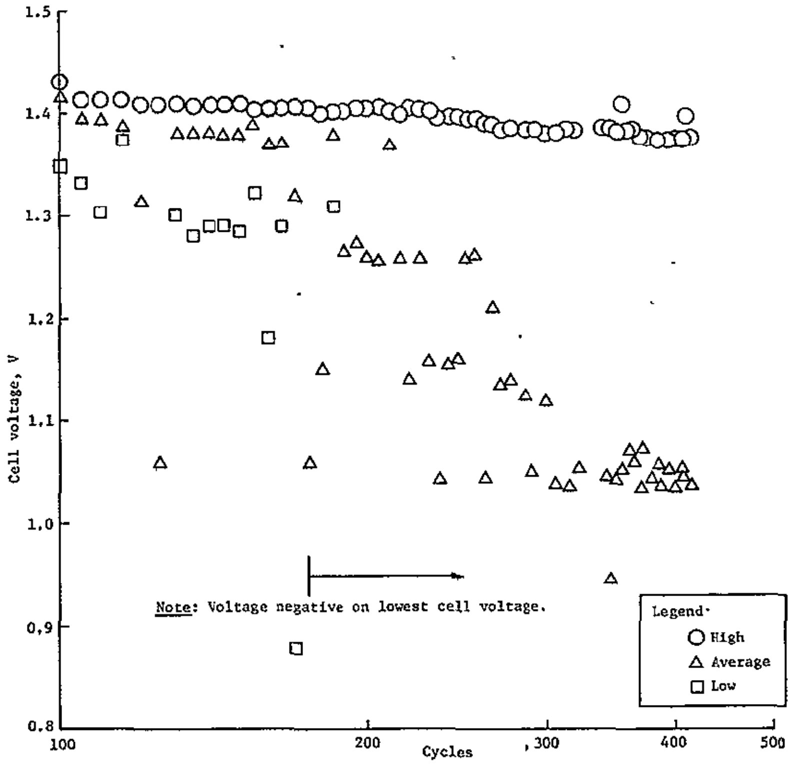


Figure 47. - End of discharge voltage, battery-level control pack (Group VI).



<u>Note</u>: Voltage negative on lowest cell voltage.

Figure 48. - End of discharge voltage cells, Group VI (battery level).

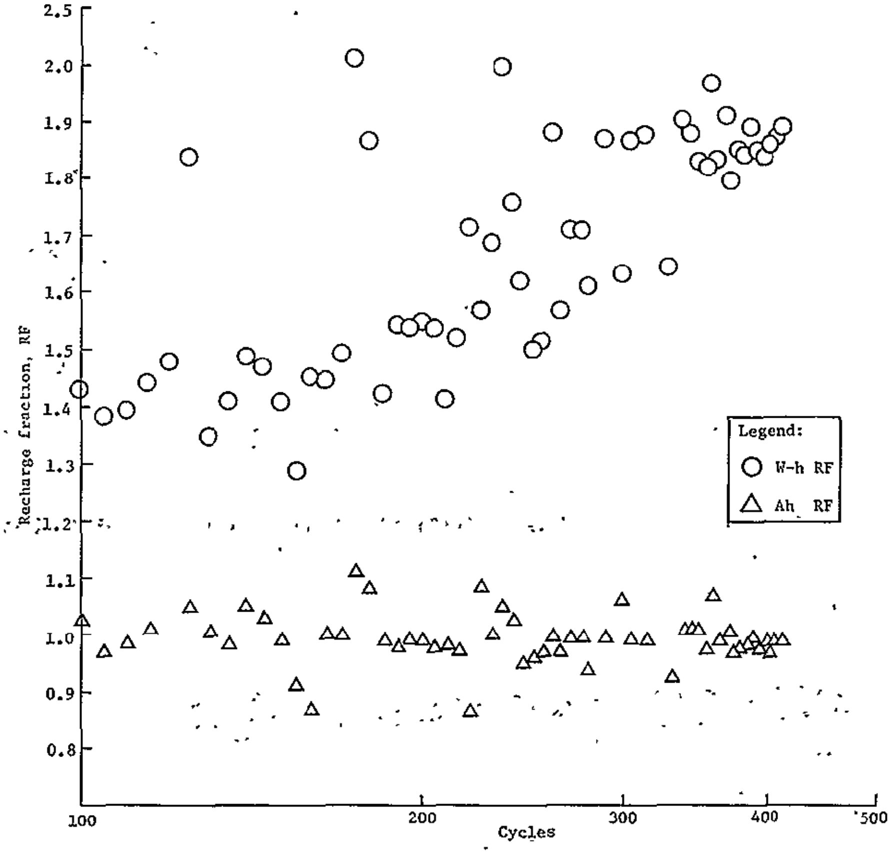


Figure 49. - Recharge fraction, ampere-hours and watt-hours, Group VI (battery level).

5.0 ANALYSIS OF PROTECTION APPROACHES

The objective of the analysis was to evaluate the merits of three design approaches and recommend a preferred method of protecting the scaled rechargeable AgZn battery.

The comparison parameters identified are cost, performance, reliability, weight, size, power consumption, and control flexibility. Table VIII summarizes these factors. The electronic parts list for the three design approaches are listed in Tables IX through XI, respectively.

TABLE VIII. - COMPARISON OF SCP AND CCP DESIGN APPROACHES FOR 18-CELL Ag-Zn BATTERY

Parameter	SCP	CCP	MCP
Material Cost	3,899.00 ($216.61 per SCP)	2,827.12	$2,358.57
Performance			
Charge control flexibility	Limited to simple charge control technique (i.e., voltage cutoff	Various techniques can be implemented via software (e.g., amperehour recharge fraction, multiple voltage limits, & modified constant current). Voltage limit adjustment make via TTY; relatively simple	Hardware changes required
Cell-voltage monitoring	Limited to hardwired connection to cell terminals	Capability to store all measured parameters & dump data on output device such as teletype whenever required.	(Same as SCP)
Application flexibility	Modular design; well suited to single-cell applications	Integrated design; best suited for full battery application	Suited for full battery application
Power consumption	6.5 W (360 mW per SCP)	2.5 W	7.5 W
Reliability			
Success probability for 1 year	0.943	0.974	0.9488
Success probability for 2 years	0.889	0.949	0.900
MTBF	148 000 hours	331 000 hours	166 788 hours
Design			
No electronic piece parts	1378	398	382
Circuit board area	1684 cm^2 (93.55 cm^2/SCP)	477 4 cm^2	445 cm^2
Weight	4.73 kg (263 gm/SCP	2.82 kg	
Interface			
No. of power & signal wires With Data Handling System (DHS)	162 Hardwired connection required, resulting in complex wiring; Requires A-to-D conversion in DHS	58 Minimum required because CCP transmits control and signal data in serial format	58 Similar to CCP but less flexible

The main advantages of the SCP design relative to the CCP approach are as follows:

(1) It is a modular design and better suited for single cell applications;

(2) No software is involved;

(3) The analog circuits are straightforward and relatively simple.

Advantages of the CCP approach range from cost factors to reliability, interface and application flexibility, as indicated in Table VIII. The major disadvantage is that it involves the software and requires a specially trained person to prepare the computer program. In the case of Intel 8008 (SIM 8), the program was written in assembly language and loaded into the RAM.

After a careful evaluation of the advantages and disadvantages, it was concluded that no single approach can satisfy all applications. The CCP approach is better suited for the 18-cell battery where (1) flexibility in changing the charge control limits or conditions are required, (2) both volume and weight must be minimized, and (3) extensive data acquisition is desired. The MCP approach is similar to that of the CCP. The principal difference is that the MCP does not have a computer; it's flexibility is limited because all the control limits such as the charge and discharge voltage limits are stored in hard-wired logic. Its primary advantage over the CCP is that no software is involved, and thus, it does not require an additional skill (i.e., an assembly language programmer) to implement the design. However, the CCP is preferred over the MCP because the CCP requires less effort to fabricate the unit and permits more flexibility in changing protection limits and adaptation to other rechargeable battery systems such as the nickel-hydrogen and nickel-zinc.

6.0 CONCLUSIONS AND RECOMMENDATIONS

Three cell-level protection systems have been designed, fabricated, and tested. Each system has successfully provided individual cell protection during charge and discharge for the respective 18-cell battery packs.

Based on the results of concurrent life testing of cell-level and battery-level protected systems for a 18-cell battery, it was determined that the cell-level monitoring and protection is necessary to attain the long cycle life of a AgZn battery. The cell-level protection was found to increase the life of the AgZn battery in synchronous orbit operation by a factor of at least 1.5. If spare cells are provided, this factor can be further enhanced.

The best method of providing control and protection of the AgZn cells depends on the specific application and capability of the user. For laboratory use involving a large number of cells and batteries, the microprocessor approach provides a low-cost system with high flexibility in changing charge control limits. It also provides an added advantage in data acquisition and interfacing with the digital equipment. The SCP, on the other hand, is best suited for testing a limited number of cells or batteries if volume and weight requirements can be tolerated.

TABLE IX. - SCP PARTS LIST

Description	Quantity	Estimated Part Cost[a], $
Switch monlatching, MSS - 22	1	1.17
1C dual in-line op amp, LM324N	2	2.50
1C dual in-line, MC14020CP	2	3.33
1C dual in-line, MC14001	1	0.42
1C dual in-line, MC14011	1	0.42
Relay 25-A magn latching, KCL - D2A-oo2	1	77.00
Diode, 1N4148	8	0.22
Diode, 1N458	2	0.47
Diode unitrode, JAN 1N5550	1	1.32
Zener diode, 1N5257B	1	0.93
Zener diode, 1N4566	1	11.70
Transistor, field effect, 2N5392	3	5.00
Transistor, 2N2907A	3	0.91
Transistor, 2N2222A	5	0.27
Transistor, 2N3019	1	1.50
Resistor, variable, 3006P-1-103	2	1.19
Resistor, 10 KΩ	3	0.28
Resistor, 1 KΩ	2	0.44
Resistor, 2.15 KΩ	1	0.44
Resistor, select in test	2	0.44
Resistor, 2.87 KΩ	1	0.44
Resistor, 7.5 KΩ	1	0.44
Resistor, 10 MΩ	3	0.28
Resistor, 2.2 MΩ	4	0.28
Resistor, 750 KΩ	2	0.28
Resistor, 110 KΩ	1	0.44
Resistor, 10 KΩ	1	0.44
Resistor, 13.3 KΩ	1	0.44
Resistor, 2.61 KΩ	1	0.44
Resistor, 51 KΩ	3	0.28
Resistor, 5.1 KΩ	2	0.28
Resistor, 100 KΩ	2	0.28
Resistor, 300 KΩ	1	0.28
Resistor, 20 KΩ	1	0.28
Capacitor, 15 μF	1	0.70
Capacitor, 0.1 μF	4	0.57
Connector, receptacle	2	5.50
Connector, plug	4	0.57
Case & cover	1	44.34
Printed circuit boards (recurring cost)	3	65.00[b]
Total per SCP:	77	$213.00
Total 18 SCPs:	1386	$3,899.00

[a] 1976 Cost

[b] Recurring

TABLE X. - CCP PARTS LIST

Description	Quantity	Estimated cost[a], $
Multiplexer		
2N5392 N-channel FET	96	480.00
Resistor, 1 mΩ 5%	48	7.00
8-Channel differential		
D125BK 6-channel FET-switch driver	1	8.50
100 KΩ, 5% resistor	6	0.84
1N4148 diode	1	0.19
Subtotal	152	496.53
Relay Driver		
MC14628 Binary-to-octal decoder	2	4.00
2N2222 NPN transistor	22	22.00
2N2907	6	6.00
5 KΩ 5% 1/2-W resistor	14	2.10
2 KΩ 5% 1/2-W resistor	14	2.10
1.8 KΩ 5% 1-W resistor	6	1.00
Subtotal	64	37.20
Relay Interface		
Relay, latching 25 A	18	1396.00
1N4148 diode	72	13.46
1N5550 diode	18	22.86
Subtotal	108	1432.32
Transconductance Amplifier		
LH0004CH high-voltage operational Amplifier	2	70.20
2N3811 dual PNP transistor	1	1.00
1N4148 diode	7	1.30
10 KΩ resistor 5%	2	0.30
390 KΩ resistor 5%	1	0.15
Select 1% resistor	1	0.15
100, 47, 300, 510 pF capacitor	4	4.00
Subtotal	18	77.10
Current Switch Network & Comparator		
LM324 quad operational amplifier	1	3.75
LM111 voltage comparator	1	4.85
2N2907 PNP transistor	1	1.00
1N4148 diode	3	0.56
1N4566A 6.4-V zener	1	12.00
ICL8018 quad current switch	1	3.30
ICL8018 quad current switch	1	3.30
Resistor, 5%	4	0.60
Resistor, 1%	10	1.00
Resistor, ladder network	2	50.00
4.7 μF capacitor	2	2.00
0.1 μF capacitor	3	3.00
3300 pF capacitor	1	1.00
Subtotal	31	86.36
Signal Conditioner		
LM324 quad operational amplifier	1	3.75
Resistor select, 1%	5	0.50
1 KΩ, 1% resistor	2	0.20
Subtotal	8	4.45
Microcomputer		
Intel 8080 microprocessor	1	175.00
MC14508 dual 4-bit latch	5	32.50
MC14081 AND gate qual 2 input	2	2.00
MC14011 NAND gate qual 2 input	2	2.00
MC14020 14-stage counter	2	6.66
1 Crystal	1	10.00
Intel 5101 256X4 static RAM	2	60.00
Intel 8702 256X8 PROM	1	40.00
Clock generator & driver for 8080	1	65.00
Subtotal	17	393.16
Miscellaneous (connectors, case & cover)		
Connector, case & cover	3	200.00
Printed circuit board	2	100.00
Total:	403	$2827.12

[a] 1976 Cost

TABLE XI. - MCP PARTS LIST

Description	Quantity	Estimated Cost,(a) $
Comparator		
Buffer inverter	1	5.75
Counter	1	6.35
Quad voltage comparator	1	2.00
4 to 16 line decoder	2	9.50
Operational amplifier	2	2.00
Clock discrete	1	1.25
Discrete diff amp	1	1.00
Relay driver discrete	1	11.00
Quad op amp	1	3.75
Capacitor	10	5.00
Resistors 1.2k 5% 1/2 W	2	0.50
Diode Assy	1	2.00
Compensating resistor	1	15.00
Trim pot	1	11.00
Subtotal	26	
Relay Driver Discrete		
2N2222A NPN transistor	2	2.00
2N2907A PNP transistor	2	2.00
Resistors RCRO 5% 1/2 W	6	1.50
Subtotal	10	
Comparator Resistors		
Resistors RN55	2	0.50
RCRO	3	0.75
1N4148 diodes	2	0.40
Subtotal	7	
Differential Amplifier Discrete		
Resistor RN60	8	2.00
2N3811 dual transistors	1	0.50
1N4148 diode	2	0.40
1N4569 zener diode	1	11.70
Subtotal	12	
Diode and Capacitor Assy		
1N4148 diode	3	0.60
Capacitor	4	1.00
Resistor RN55 5% 1/2 W	1	0.25
Subtotal	8	
Clock Discrete		
Capacitor	1	0.50
Resistor RN60	5	1.25
Subtotal	6	
Operational Amplifier		
Integrated circuit, LM0004C	1	32.50
Subtotal	1	
Multiplexer		
MCP01210	9	315.00
FET N channel, 2N3685	24	60.00
FET N channel, 2N5393	48	120.00
Resistors, RCRO	36	9.00
Subtotal		
Relay Control		
2N2222 NPN transistor	1	1.00
MC140498 hex inverter	1	7.35
MC140499 hex inverter	2	14.70
ULN2003A relay coil driver	5	55.00
Resistor RCRO 1/2 W 5%	3	0.75
Capacitor	3	1.50
Subtotal	15	

[a] 1976 Cost

TABLE XI. - (concl)

Description	Quantity	Estimated Cost,(a) $
<u>Data Selector</u>		
MC14025CP Nor gate	2	1.00
MC14023CP Nand gate	3	1.50
MC14008CP 4 bit full adder	1	5.65
MC14519CP 4 bit and/or selector	1	6.00
MC14011CP Quad nand gate	4	2.00
MC14501CP 8 input nand gate	1	8.35
MC14012CP 4 input nand gate	1	4.00
MC14512CP 8 chan data selector	4	33.40
MC14013CP dual flip flop	3	6.00
CK06 capacitor	20	10.00
Subtotal	40	
<u>Counter</u>		
MC14519CP 4 bit and/or selector	2	11.30
MC14025CP Nor gate	1	0.50
MC14012CP Nand gate	2	
MC14040CP Binary counter	1	22.70
MC14049CP Hex inverter buffer	2	14.70
MM74C1N4 Hex Schmitt trigger	1	2.00
MC14011CP Nand gate	3	3.00
MC14013CP Flip flop	6	10.50
CD4556BE Decoder mux	1	15.00
Capacitor	26	13.00
Resistor	16	4.00
Subtotal	61	
<u>Memory & Regulator</u>		
MC14552CP Static RAM	1	60.00
2N5154 Transistor	2	4.34
2N2222 NPN transistor	4	4.00
Resistor RA60	6	1.50
Capacitor	9	4.50
Subtotal		
<u>Interconnection Assy</u>		
Resistor, RN60	4	1.76
Capacitor, CK06	1	0.50
Nand gate, MC14012	1	2.00
Resistor network, 316B103	1	2.00
Switch network, CTS-206-8	1	3.30
Subtotal	8	
<u>Power Converter</u>		
T1 Transformer	1	15.00
600D Capacitor	3	2.25
1N5417 Diode	6	8.10
RNR60 Resistor	3	1.32
Subtotal	13	
<u>Cell Bypass Network</u>		
Relay	18	1,386.0
Diode, 1N	18	
Subtotal	36	
Total	382	$2,358.57

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7.0 NEW TECHNOLOGY

The new technology item developed under this contract is the multiplexed-cell protector (MCP) described in Section 3.0. A new technology disclosure has been written and submitted to NASA Lewis Research Center in accordance with the requirements of the contract.

REFERENCES

The following documents are referenced in this report.

1. M. S. Imamura et al.: *Development of Single Cell Protectors for Sealed Silver-Zinc Cells Phase I.* Final Report, NASA CR-135054. Martin Marietta Corporation, September 1976.

2. *Handbook of Piece Part Failure Rates.* T-70-48891-007. Martin Marietta Corporation, Denver Division.

APPENDIX A

AUTOMATIC CONTROL AND DATA ACQUISITION SYSTEM (ACDAS)

The ACDAS is a fully automated fail-safe system that remotely monitors and controls individual calls or batteries and acquires test data for near-real time or subsequent analysis. An overall view of the system is shown in Figure A-1. A block diagram of the ACDAS is given in Figure A-2. The ACDAS is comprised of the following subsystem:

(1) Computer (central processor/memory unit)

(2) Data Acquisition

(3) Control and Display

(4) Input/Output Devices

Computer Subsystem. - The computer system consists of a central processor, 8K of magnetic core memory, 96K of dic memory, and a magnetic tape for data storage. The central processor takes the data acquired, performs the required arithmetic and logical manipulations, and issues appropriate commands for cell or battery control, data storage, and input/output functions. The major element in the subsystem is the PDP-8E computer. This computer is a fully parallel, 12-bit random access, 8192-word core memory system. It performs general purpose computations and process control operations. The PDP8-E is a single address, fixed work length system that uses twos complement arithmetic. The computer includes transfer facilities.

The disc file and control units, DEC DF32E and DS32E, are used for random access memory storage. They use a magnetic process for recording information on an aluminum disc. The units consist of two assemblies, the disc assembly and the logic module assembly. The storage capacity for the DF32E and the DS32E is 32 768 thirteen-bit words each. The data transfer rate is 32 µs/word for the DF32E and 39 µs/word for the DS32E. The discs have 16 data tracks and 2048 words per track.

All acquired data is stored on magnetic tape in a form that can be reduced and analyzed by programs written for the CDC 6500 computer. Data that can be obtained from the magnetic tapes are as follows:

(1) Single channel evaluation of statistical parameters;

(2) Performance trends and parameter prediction;

(3) Cell matching and selection;

(4) X-Y plots.

Figure A-1. - Pictorial view of Automatic Control and Data Acquisition System.

The data stored on magnetic tape can also be printed on teletype 1 in real time. These data include:

(1) Cell and battery voltages;

(2) Current;

(3) Any parameter that can be instrumented such as third electrode, pressure, and temperature;

(4) Ampere hour integration.

Data storage is on an 800 bits per inch, 7- or 9-track magnetic tape. The system has a synchronous write and synchronous read capability with either odd or even parity.

The computer software is written in a language developed by the Digital Equipment Corporation and is called INDAC.

Data Acquisition. - The data acquisition subsystem consists of signal conditioning, multiplexing, and A/D conversion. The subsystem is capable of accepting 600 data inputs. These data inputs are routed to a scanner (or multiplexer). The central processor controls the scanner and selects data for analog-to-digital conversion. The data are printed on teletype and stored on magnetic tape in accordance with computer program instructions.

The scanner, which is a key element in the data acquisition system, is a "flying spot" (or "flying capacitor") scanner capable of handling low level signals. It achieves high isolation as well as excellent common mode rejection by commutating a charged capacitor from the signal source to the input of the system amplifiers.

Both gain and channel selection are controlled by the computer. The system accepts signal source from -200 mVdc to +5.0 Vdc.

The accuracy of the system is ± 10 mV worst case, and is 15 mV probable error or 0.05% ± 1/2 the least significant bit. The gain accuracy of the system is 1% worst case, and the common mode is 120 dB from dc to 60 Hz. The input impedance at dc is 100 megohm or greater. The data sampling rate is 200 per second.

Control and Display. - The control and display subsystem consists of channel controllers that establish charge/discharge parameters; a cell bypass network; charge mode power supplies; discharge mode load banks; and a bypass control matrix that includes bypass relay position indicators. The channel controllers control the magnitude or voltage on a single cell or a string of cells and current through each channel. Each controller can provide different voltage/current levels for up to four time phases in a given charge/discharge cycle. The bypass control matrix provides visual indications by a light matrix of cell or battery state (i.e. in or out of the charge/discharge circuit). The cell

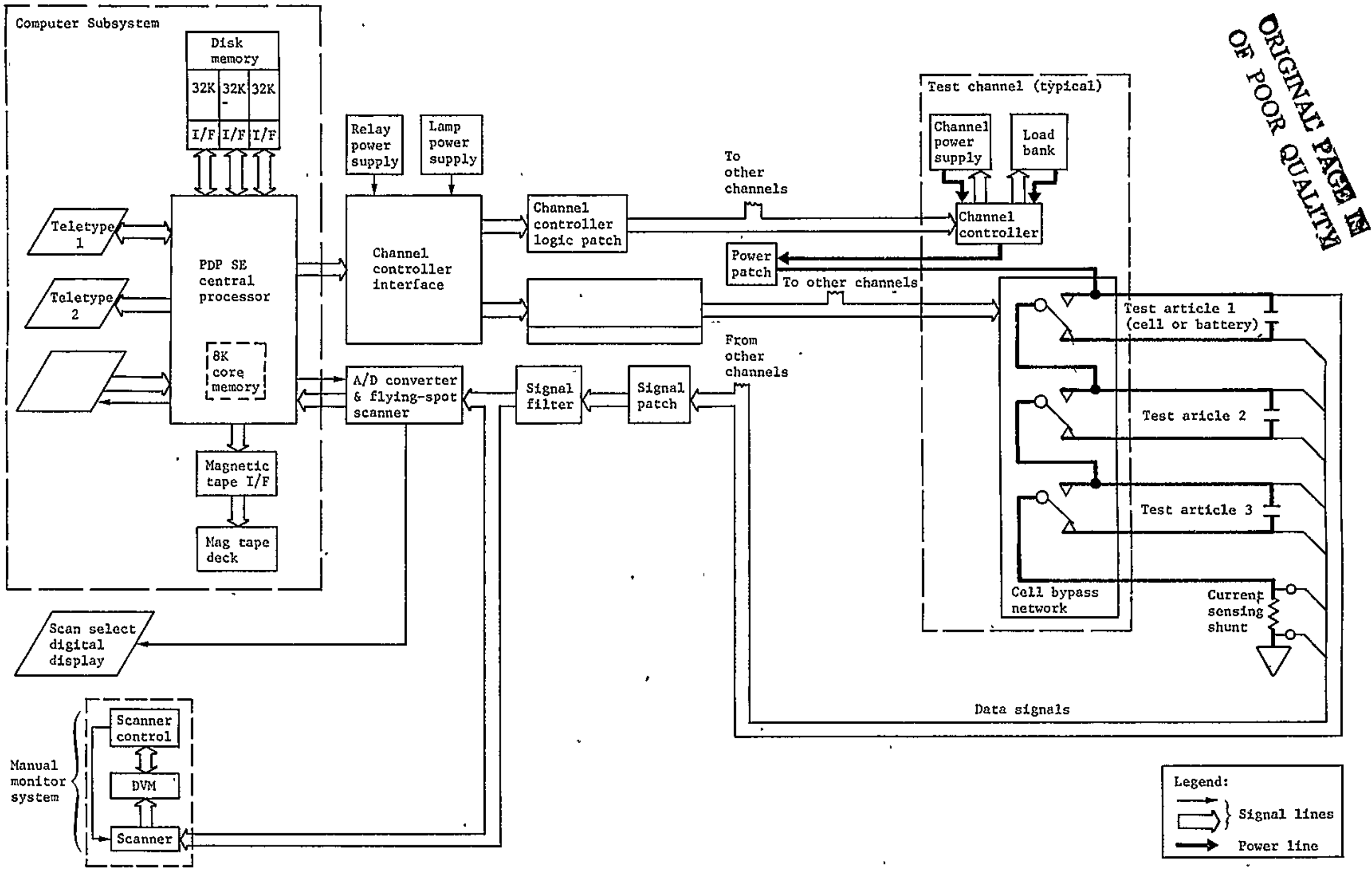

Figure A-2. - Functional block diagram of Automated Control and Data Acquisition System.

bypass network contains relays that serve as cell/battery bypass elements. The bypass relays are mounted close to the cells to minimize IR voltage drops in the charge/discharge lines. They are connected to the central processor through the Bypass Control Matrix unit. The central processor directly controls the Channel Controllers and the Cell Bypass Circuit.

The Cell Bypass Network places the cells or batteries in or out of series connection using magnetic latching relays. The Channel Controllers place the channel cell strings or batteries in charge, discharge, or open circuit condition. The Channel Controllers can establish different test conditions in each of a given charge/discharge cycle. The computer automatically sequences a given string through the four phases.

The Channel Controller Interface Unit provides logic to relay and lamp interface with the PDP-8E computer to control the magnetic latching relays in the Channel (phase) Controllers.

Digital display capability is provided to display any of the measured test parameters. The display is controlled by the teletype keyboard.

A light matrix on the Bypass Control Matrix unit indicates which cell (or battery) is in or out of the circuit.

An electronic load bank is used with the Channel Controller to provide constant current discharge for the string under test.

Input/Output Subsystem. - The input/output functions are accomplished via teletype or tape reader control of the central processor. Near-real time test data are printed on hard copy as well as all test parameters and operator instructions and request.

The tape reader/punch allows test parameters to be stored on paper tape and read into the computer memory.

Teletype 2 is a dot matrix impact printer and keyboard for use as a hard copy data output terminal. The unit is capable of printing a set of 64 ASCII characters at a speed of up to 30 characters/inch on sprocket-fed 9 7/8-inch wide fanfold paper. Data entry is made from a keyboard capable of generating 96 to 128 characters. Line length has a 80-character capability.

Two teletypes are used: one for interactive program control and modification between computer and operator, and one dedicated to data recording only. With this two-teletype system, programming can be performed on a given channel with teletype 1 without interfering with data from other channels being printed simultaneously on teletype 2.

RELIABILITY ANALYSIS - APPENDIX B

A reliability analysis was conducted to estimate the reliability of the Multiplexer Cell Protector (MCP). Procedures and data of MIL-HDBK-217B, Reliability Prediction of Electronic Equipment, were used to estimate the probabilities that the denoted charge and battery protection system will maintain each cell of an 18-cell battery within specified voltage limits for a specific period of time (success).

Conclusions and Recommendations. - Estimated probabilities of success for 1 and 2 years of continous spatial operation are shown in Table B-1. The electronic parts count of each configuration is included for comparison.

TABLE B-1. - PROBABILITY OF SUCCESS FOR OPERATING ONE BATTERY

	Parts Count	Success Probability	
		1 Year	2 Years
Multiplexer Cell Protector	382	0.9488	0.900

The electonmechanical relays greatly contribute to total failure probabilities. Table B-2 presents failure probabilities for generic categories for the MCP configuration. Solid-state switched, which have higher reliability than relaysk cannot be used in this application because of their high voltage-drop characteristics.

Approach. - Reliability was-estimated using the parts count by generic category and generic failure rates modified by environmental and quality level factors. MIL-HDBK-217B provided the general approach and data. Basic assumptions concerning the parts were as follows:

(1) A benign satellite environment;

(2) An average temperature of 25°C;

(3) All parts must function for success;

(4) JAN TX parts quality;

(5) Class A parts screening;

(6) Part deratings in general agreement with NASA practice:

Resistors - 60% of rating

Transistors - 70% of rating

Diodes - 70% rating

Relays - 60% of rating

Switches - 70% rating

Capacitors - 60% rating

(7) Average IC chip area = 4900/sq. mils;

(8) Thick film networks used in hybrid;

(9) Conductor density = $66/\text{in}^2$;

(10) Gold wires and qutectic bonding employed;

(11) Three mat etch cycles used;

(12) Equipment operates continuously.

Operating in-service failure rates for each generic part category were calculated using the general relationship for nonhybrids:

$$\lambda_p = \lambda_b \ (\Pi_E \times \Pi_A \ \Pi_S \ 2 \times \Pi_C \times \Pi_Q)$$

where: λ_p = part failure rate, ppm/hr

λ_b = base part failure rate, ppm/hr

E = environmental factors other than temperature

A = application factor

S^2 = voltage stress factor

C = construction class factor

Q = quality level factor

For example, the failure rate of an RCR05, 10-kΩ resistor (MIL-R-39008) is calculated as (per MIL-HDBK-217B, Tables 2.5.1-1 through 2.5.1-4) follows:

λ_b = 0.0004 ppm/h (derated 40%, @ 25°C)

Π_E = 1.0 satellite, S_F

Π_R = 1.0 (up to 100 k)

Π_Q = 0.3 (level P)

$$\lambda_p = \lambda b \quad \lambda E \quad \lambda R \quad \lambda Q$$

$$\lambda_p = (0.0004)\ (1.0)\ (1.0)\ (0.3) = 0.00012 \text{ ppm/h each.}$$

This type of calculation is performed for all resistors and the failure rates added to obtain the total failure rate for all resistors. As listed in Table B-2, the total resistor failure rate for the MCP is 0.01 ppm/hr. The procedure for the resistors is repeated for all generic categories of parts. Their sum (no redundancies) equals the total failure rate of a particular configuration--5.996 ppm/hr for the MCP (Table B-2).

The success probability for one year of continous operation is calculated by the equation

$$P(S) = \exp\ (-\lambda_p t)$$

where:

$P(S)$ = success probability for one year

λ_p = sum of part failure rates for configuration

t = operating hours = 8760

Hence, the 1-year success probability for the MCP configuration is

$$P(S) = e^{-(7.185)\ (8760)\ (10^{-6})} = e^{0.05252}$$

$$\doteq 0.9488$$

The Martin Marietta-derived average failure rate of 0.030 x 10^{-6}/h was used for all ICs rather than perform laborious calculations for each type of IC. The value is for achieved-operating, hi-reliability ICs. Industrial and government surveys by Martin Marietta plus our comparative studies proved this to be a good average value (ref 2).

TABLE B-2. - FAILURE PROBABILITIES BY GENERIC PART CATEGORY AND MTBF

Piece Part	Quantity	Failure Probability (ppm/h)
Relay	18	2.16
FETs	72	1.10
Resistor	198	0.009
Transistor (non-FET)	12	0.07
Diode	32	0.109
IC	70	2.10
Capacitors	77	0.198
Switche	1	0.22
PC Board	2	0.03
Total	382	5.996
MTBF		166 778

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