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NASA TECHNICAL MEMORANDUM

NASA TM-78211

DESCRIPTION OF THE THREE AXIS LOW-g ACCELEROMETER PACKAGE

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November 1978

NASA

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MSFC - Form 3190 (Rev June 1971)

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DESCRIPTION OF THE THREE AXIS LOW-g ACCELEROMETER PACKAGE

INTRODUCTION

The function of the three axis low-g accelerometer package (Figs. 1 and 2) is to measure accelerations along the orthogonal triad axes and generate output signals proportional to these accelerations. The full range output of each accelerometer is ±0.031 g. The signal conditioning section converts the accelerometer digital output into a 24-bit serial binary coded word. This word consists of 4 bits for timing and 20 bits of data (Fig. 3). The output of each accelerometer is integrated for 1 s and is converted to this 24-bit word each second. The theoretical resolution of the output is 1.1×10^{-7} g/bit change/s. The package parameters are given in Tables 1 and 2. Documents applicable to the accelerometer package are given in Table 3.

ACCELEROMETERS

The low-g measurement module uses three Kearfott 2412 accelerometers (Fig. 4) mounted in an orthogonal triad on a temperature stabilized mounting cube. The cube is thermally isolated from the package to minimize power required to maintain operating temperature. Temperature control of the cube is provided by a proportional controller which maintains the temperature precisely at 50° ± 2°C. The thermal isolation of the cube is obtained by using polytrifluorachloroethylene, unplasticised Kel-F, AMS-3650 materials.

This accelerometer is a hinged pendulum, fluid damped, electrically restrained type. The pendulosity is 6540 dyne-cm/rad, the largest Kearfott provides in the 2400 series accelerometers. It uses an air core differential pickoff excited by 4.5 Vrms, 19.2 kHz. The torquer used to restrain the pendulum is a dc permanent magnetic type. Detailed specifications and characteristics of this sensor are available from the Kearfott literature.

TABLE 1. THREE AXIS LOW-g ACCELEROMETER PARAMETERS

Mass Moment of Inertia: 200 dyne-cm-s^2/rad
Damping Coefficient: 9×10^6 dyne-cm-s/rad
Elastic Restraining Torque: 6540 dyne-cm/rad
Pickoff Sensitivity: 36 rms V/rad
Acceleration Scale Factor: 30 mA/g
Pickoff Frequency: 19.2 kHz
Pickoff Excitation: 4.5 Vrms
Pickoff Impedances:
Output: 205 + J241.5 (± 20 percent) Ω
Input: 168 + J406 (± 20 percent) Ω
Resistance of Restoring Coil: 23 ± 7 Ω
Pickoff Null Voltage: 1.0 rms mV maximum

TABLE 2. THREE AXIS LOW-g PACKAGE PARAMETERS

Range: ±0.031 g
Threshold: 2×10^{-7} g
Data Word: 24 bits
Interrogation: 1 word/s
Limit Cycle Frequency: 2.4 kHz
Size (L × W × H): 29.2 cm × 17.8 cm × 15.2 cm
Weight: 12.5 kg
Power: 28 ± 4 Vdc
Cold Start Current: 2 A, dc maximum
Operating Temperature Current: 0.75 A, dc nominal
Accelerometer Block Temperature Range: 23° to 80°C
Accelerometer Operating Temperature: 50° ± 2°C

TABLE 3. DOCUMENTS APPLICABLE TO THE ACCELEROMETER PACKAGE

Applicable Documents	Drawing Number
Low-g Measurement Module (Designating Input Vectors Applicable to the Low-g Measurement Module)	95M18700
Low-g Assembly Drawing	95M18702
Abbreviated Measurement Module Schematic	95M18750
Accelerometer Block Drawing	95M18721
Low-g Triad Assembly Drawing	95M18720
Accelerometer	95M18724
Low-g Measurement Module Wiring List	95M18755
Torquer Current Generator Schematic	95M18781
Error Signal Processor Schematic	95M18776
Digital Control Electronic Schematic	95M18771
Signal Conditioning Schematic	95M18786
Timing and Signal Conditioning Schematic	95M18791
Heater Control Schematic	95M18766
Power Supply Schematic	50M27785

PRINTED CIRCUIT CARDS

The servoelectronics, the signal conditioning, heater control, and power supply consist of printed circuit cards with associated components mounted securely to the cards. The printed circuit cards are constructed and inspected in accordance with MSFC STD-152. The card consists of a plastic sheet,

laminated and copper-clad in accordance with MSFC SPEC-377, Type FL-GB-C2-2/0.062. The hot tin-lead coat conductors and solder terminations are per MSFC STD-154. Tin-lead plating is not acceptable unless it is followed by a hot tin-lead solder coating operation. Components with leads or connections subject to breaking off or becoming loose during a hard vibration period are stycast in place. Finally, a conformal coating encompasses the printed circuit assembly per MSFC PRO-508 using Type I, Class II epoxy urethane compound except it is post-cured for 8 h at 10^{-3}-mm Hg at 80°C.

The printed circuit cards have a WTB24PR9SY connector. The card slides in a guide during assembly to keep it properly aligned to mate with its associated connector. The printed circuit cards (electronics) shown in Figure 2 are, from right to left, as follows:

PC-6	Error Signal Processor	Z-Axis
PC-7	Torquer Current Generator	
PC-8	Error Signal Processor	Y-Axis
PC-9	Torquer Current Generator	
PC-10	Error Signal Processor	X-Axis
PC-11	Torquer Current Generator	
PC-12	Digital Control Electronics Assembly	
PC-16	Signal Conditioning Assembly	
PC-15	Timing and Signal Assembly	
PC-14	Heater and Control Assembly	
PC-13	Power Supply Assembly	

Each accelerometer has its individual error signal processor and torquer current generator printed circuit card. The three accelerometers share the following printed circuit cards: Digital Control Electronics Assembly, Signal Conditioning Assembly, Timing and Signal Assembly, Heater and Control Assembly, and Power Supply Assembly.

BASIC ORGANIZATION OF THE PULSE WIDTH-MODULATED FORCED LIMIT CYCLE REBALANCE LOOP

The basic organization of the pulse width-modulated rebalance loop consists of four basic parts as shown in Figure 5. They are the accelerometer, error signal processor, pulse width-modulator, and the digital control logic. Each of these four basic parts may be further broken down into the following functions or circuits (see Fig. 5).

The accelerometer has a mass that tends to change position from a quiescent or null position while undergoing an acceleration. A differential pickoff transducer excited by an ac signal generator produces an error signal proportional to the motion of the mass. This amplitude modulated error signal is passed on to the error signal processor.

The error signal processor (Figs. 6 and 7) receives the error signal from the pickoff and processes the signal by sending it through the following steps: ac preamplifier, bandpass filter, ac amplifier, synchronous demodulator, and the dc amplifier loop compensator. From the dc amplifier loop compensator the signal is forwarded to the automatic overload recovery if the signal warrants it and is passed through to the pulse width modulator.

The overload recovery circuit is useful when the accelerometer is saturated and a rapid recovery is desired when the acceleration is removed (Fig. 8). The overload recovery circuit senses when the loop is outside its dynamic range and then switches to a large torque current to reduce the loop recovery time. When the amplified error signal in the error signal processor drops back within the dynamic range, the overload recovery circuit reverts back to the original scaled precision low torque current value.

The digital control electronics provides a digital function generator, ramp generator, duty cycle generator, and data and torque generator (Fig. 9). The digital control electronics generates the timing and control signals for the proper operation of the loop. The time reference is a highly stable crystal oscillator. The digital control electronics transmits synchronizing blanking signals to the duty cycle generator to set the rate at which the processed error signal is sampled and to set the minimum positive and negative torque currents. The torquing status information is contained in the duty cycle pulse which the digital control electronics uses to generate digital data pulses.

TORQUE CURRENT GENERATOR

The torque current generator (Fig. 9) has the most severe requirement of high accuracy and low drift of any element within the electronic rebalance loop for the accelerometer. The rebalancing torque for the accelerometer is produced by current pulses which must be of precise shape and amplitude.

The torque current generator consists of a dc feedback loop containing a current regulator comprised of a precision voltage reference, a comparator operational amplifier, level shifting amplifier, and a power transistor current driver. An H-switch bridge is used to switch the direction of the current through

the torquer. The amount of power dissipated in the torquer is always constant, and the net torque produced is the difference in the positive and negative current pulses. This feedback signal (torque current) to the restoring coil produces a force to balance precisely the acceleration associated force acting upon the pendulous mass (Fig. 10).

DIGITAL CONTROL ELECTRONICS

The logic is controlled by a precision hybrid IC CMOS Crystal Oscillator (IC-1 with reference to Fig. 10) manufactured by Q-Tech Corporation. The output is a square wave signal of 1.2288 mHz with a stability within 0.33 ppm/°C and 10 ppm/year. This frequency is counted down by a 4404, an eight-stage binary counter (IC-2) to obtain the four binary control frequencies of 19.2, 9.6, 4.8, and 2.4 kHz.

The data clock frequency is 614.4 kHz and is obtained by the binary division of the 1.2288 mHz frequency. The data pulses are from IC-12. In the basic limit cycle frequency interval, 1/2.4 kHz (416.7 μsec), there are 256 data pulse intervals. The "0" to "15" pulses from IC-3 occupy the first 16 and the 241-256 occupy the last 16 data pulse intervals of each limit cycle period (Fig. 11).

RAMP GENERATOR – DUTY CYCLE GENERATOR

The analog to digital conversion process for the width-modulated binary rebalance electronic loop is accomplished by comparing the amplified error signal output from the error signal processor to a linear ramp voltage from IC-8 and determining the time crossing by a comparator amplifier IC-4.

Whenever the 0-15 blanking pulse is present, the output of the comparator IC-4 will be low (0 V) regardless of the amplitude of either the error signal or the ramp within an interval of ±15 V. When the 241-256 blanking pulse is present the output of IC-10 will be high (+15 V) regardless of other signals. This process provides setup time for the ramp generator and data transfer for each interrogation interval.

DATA TORQUE GENERATOR

The output pulse from the IC-4 mixer comparator gated with the 0-15 and 241-256 blanking pulses, drives a 74C175-D flip-flop (IC-5) that is clocked by the 614.4-kHz data clock. With reference to Figures 11 and 12, the output of IC-5 is a pulse whose width is directly proportional to the crossing of the error signal and the ramp, and at the limit cycle frequency of 2.4 kHz. For zero rebalance condition the duty cycle of this torque pulse is 50 percent, indicating an equal positive and negative torque current to the accelerometer. A net positive or net negative torque is then a duty cycle of either greater than, or less than, 50 percent. The output of IC-5 with the 614.4-kHz clock is applied to a NAND gate IC-10. The output of IC-10 is a series of pulses whose total count is directly proportional to the amount of positive or negative torque applied to the torquer coil of the accelerometer (Fig. 7). An output count of 614 400/2 or 307 200 pps would represent a 50-percent duty cycle for the torque signal out, or zero net torque to the accelerometer. The largest positive (or negative) torque would occur for a count (256-16) × 2400 or 576 000 pps. The largest negative (or positive) torque could occur for a count of 16 × 2400 or 38 400 pps.

SINUSOIDAL SIGNAL GENERATOR

The sine wave drive signal to the pickoff input for the accelerometer is obtained by feeding the 19.2-kHz output square wave form from IC-2 through an RC bandpass filter (Figs. 10 and 13).

SIGNAL CONDITIONING

The data pulses from each accelerometer are counted for 1 s in an accumulator and then parallel loaded into a 24-bit shift register. The accumulator is cleared and counting is continued. The 2.4 kHz from the digital control electronics is counted down in a decimal counter to provide a 24-Hz signal which is used to clock the accumulated 1-s data out serially to telemetry. The four high-order bits of the shift register are loaded as ones. They are shifted out first as timing markers, followed by the 1-s data accumulation most significant bit (2^{19}) first (Fig. 3). Twenty-four bits of information shifted to a 24-Hz clock rate require 1 s for transmission.

A schematic of the signal conditioner is shown in Figure 14.

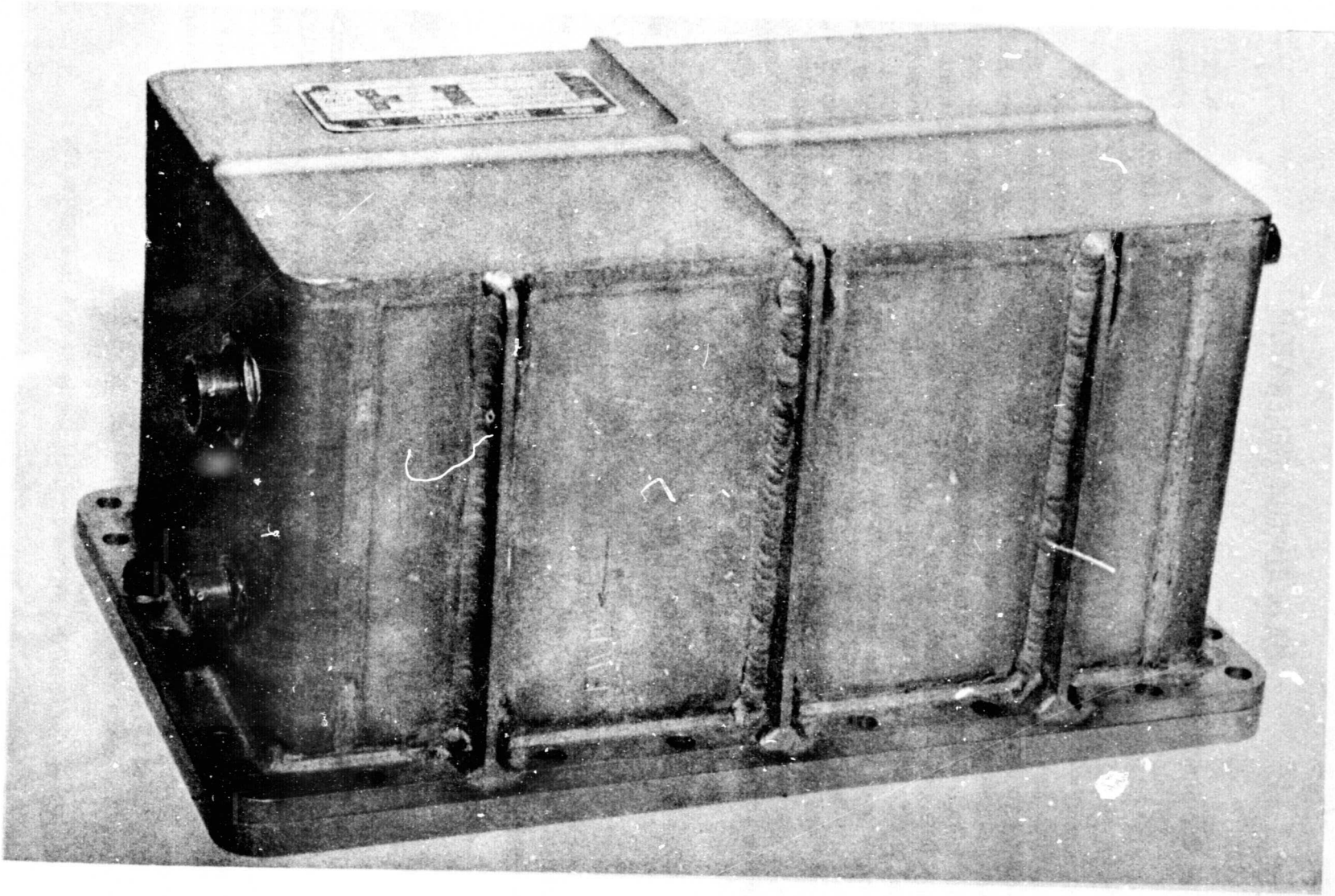


Figure 1. Low-g measurement module.

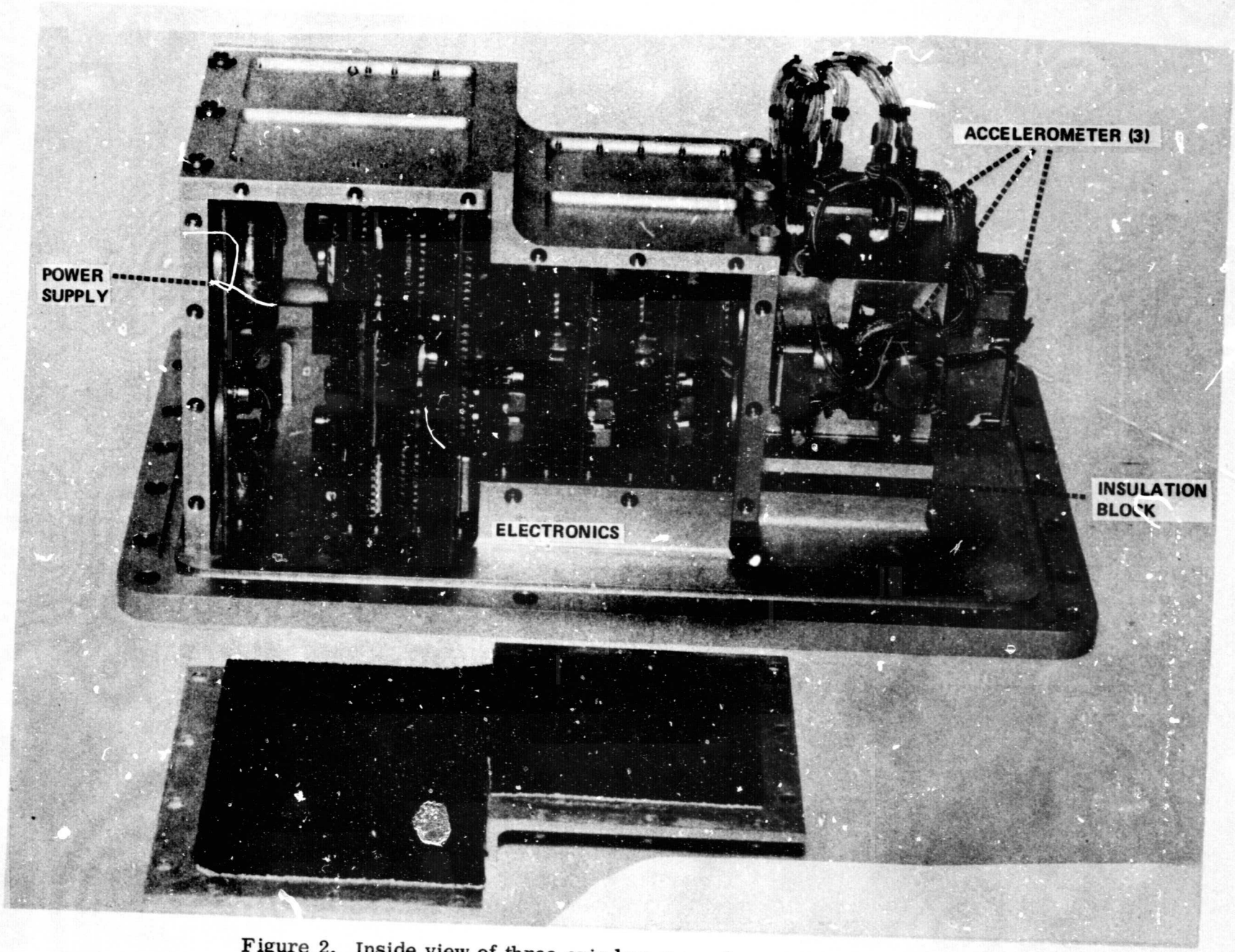


Figure 2. Inside view of three axis low-g accelerometer package.

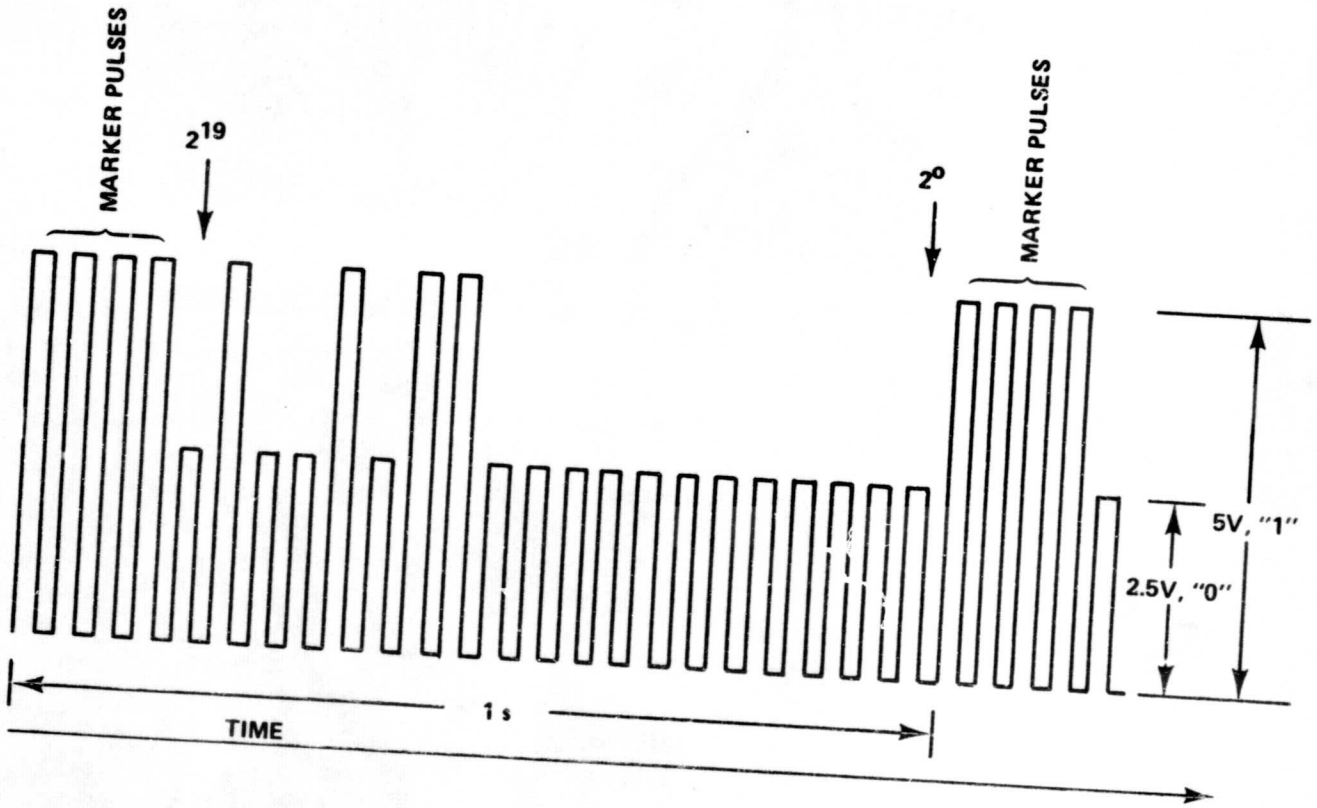


Figure 3. Telemetry word format.

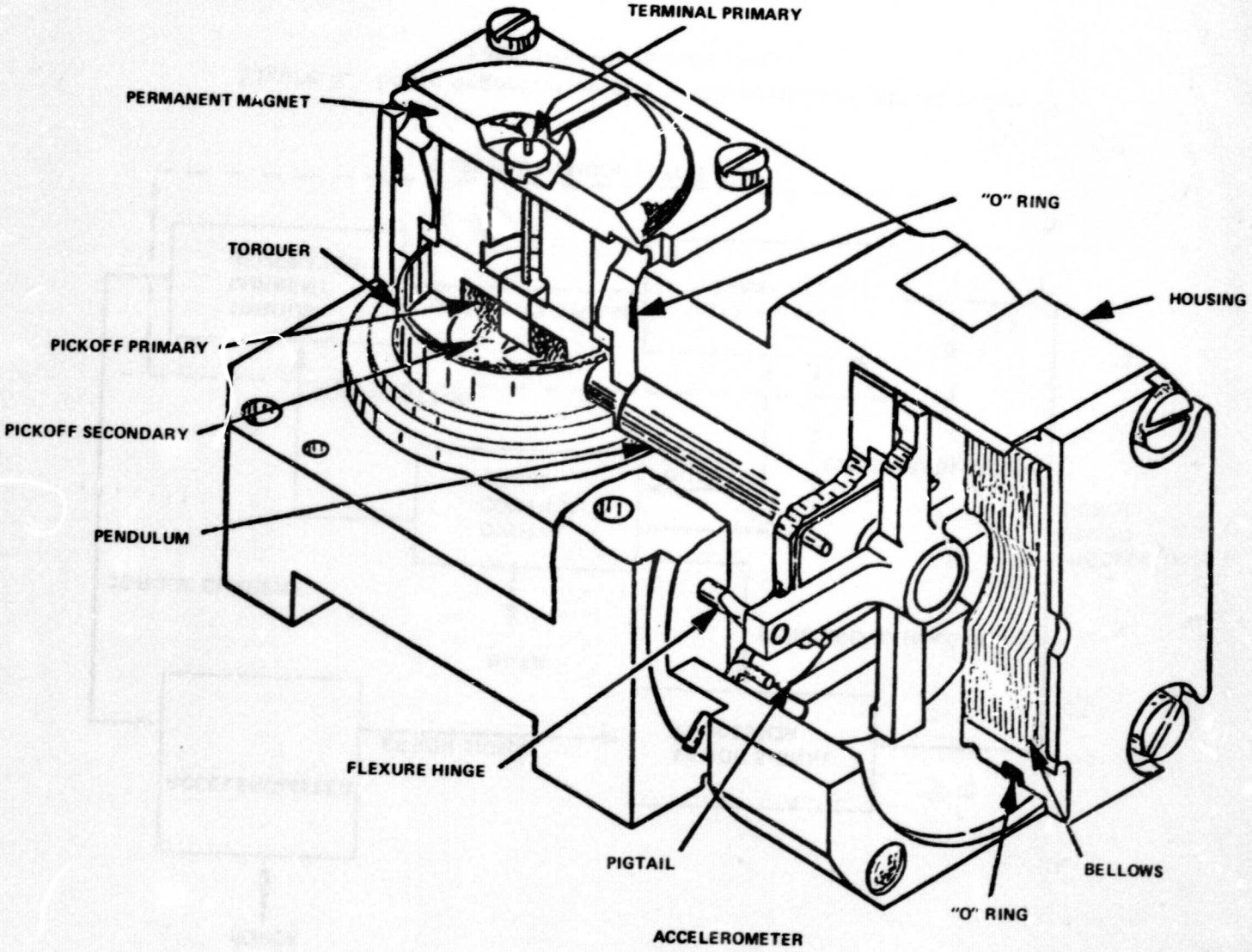


Figure 4. Kearfott permanent magnet force balance accelerometer.

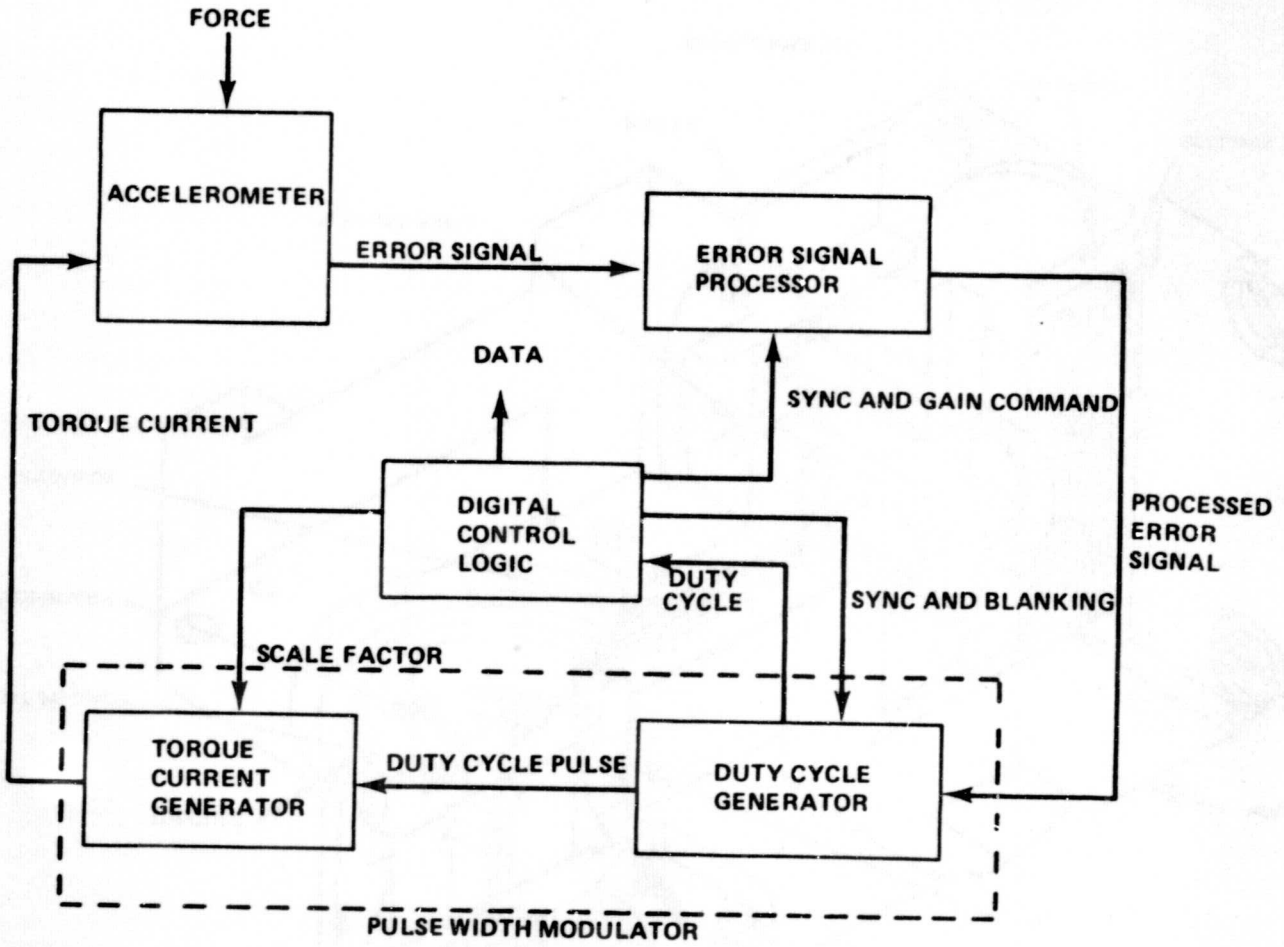


Figure 5. Basic organization of a width-modulated binary pulse rebalance electronic loop.

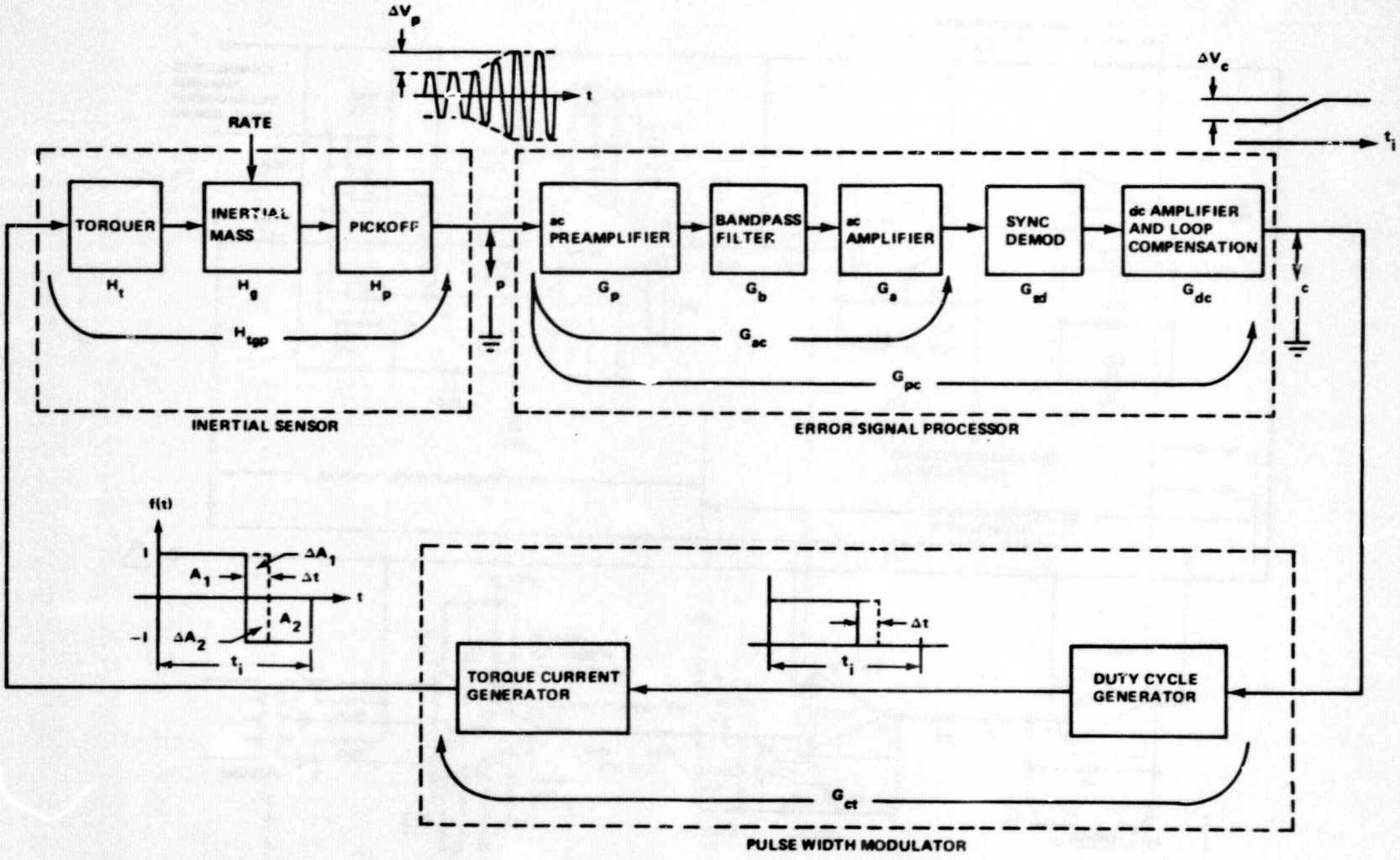


Figure 6. Basic elements of a width-modulated binary rebalance loop.

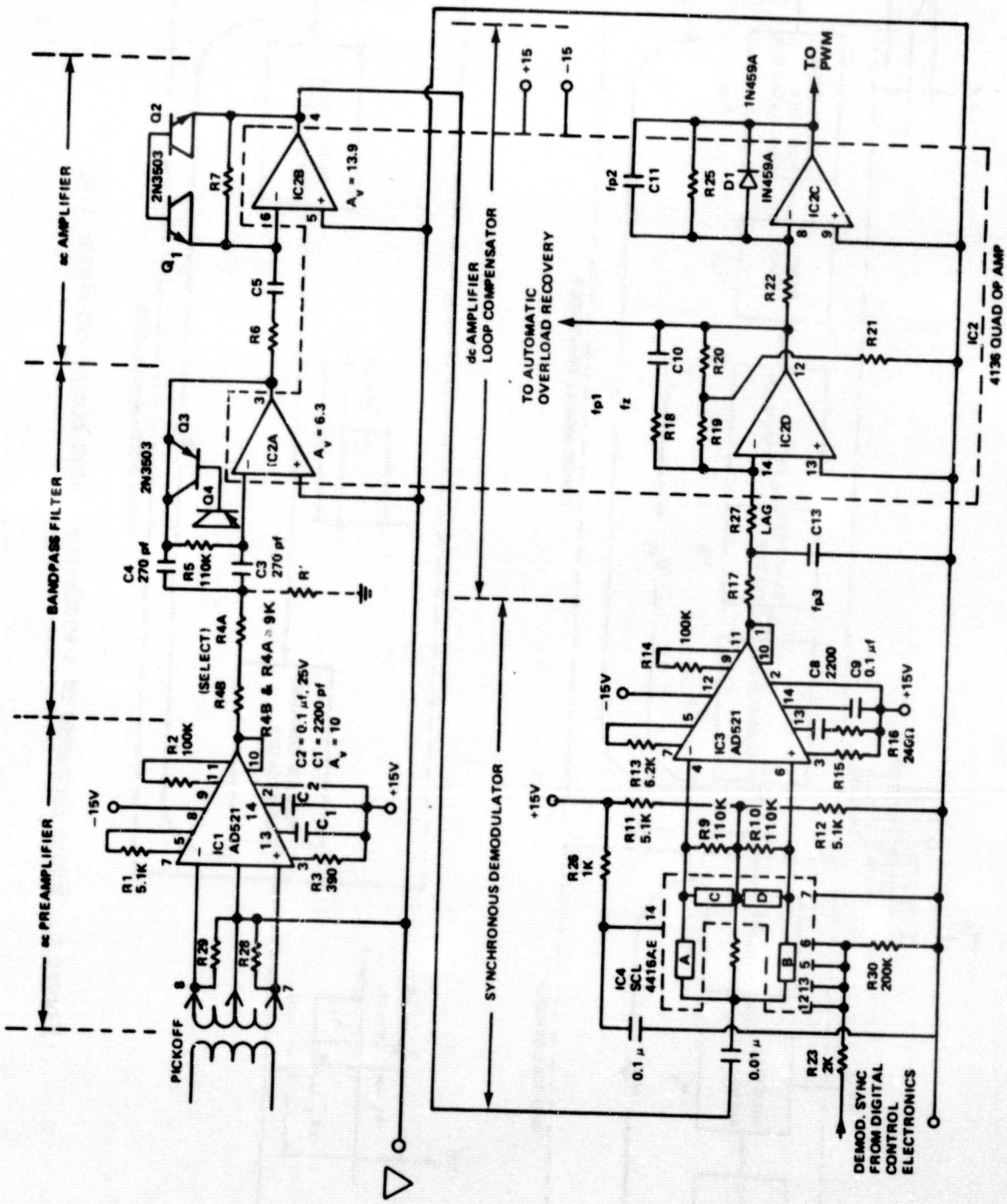


Figure 7. Electrical schematic for the error signal processor.

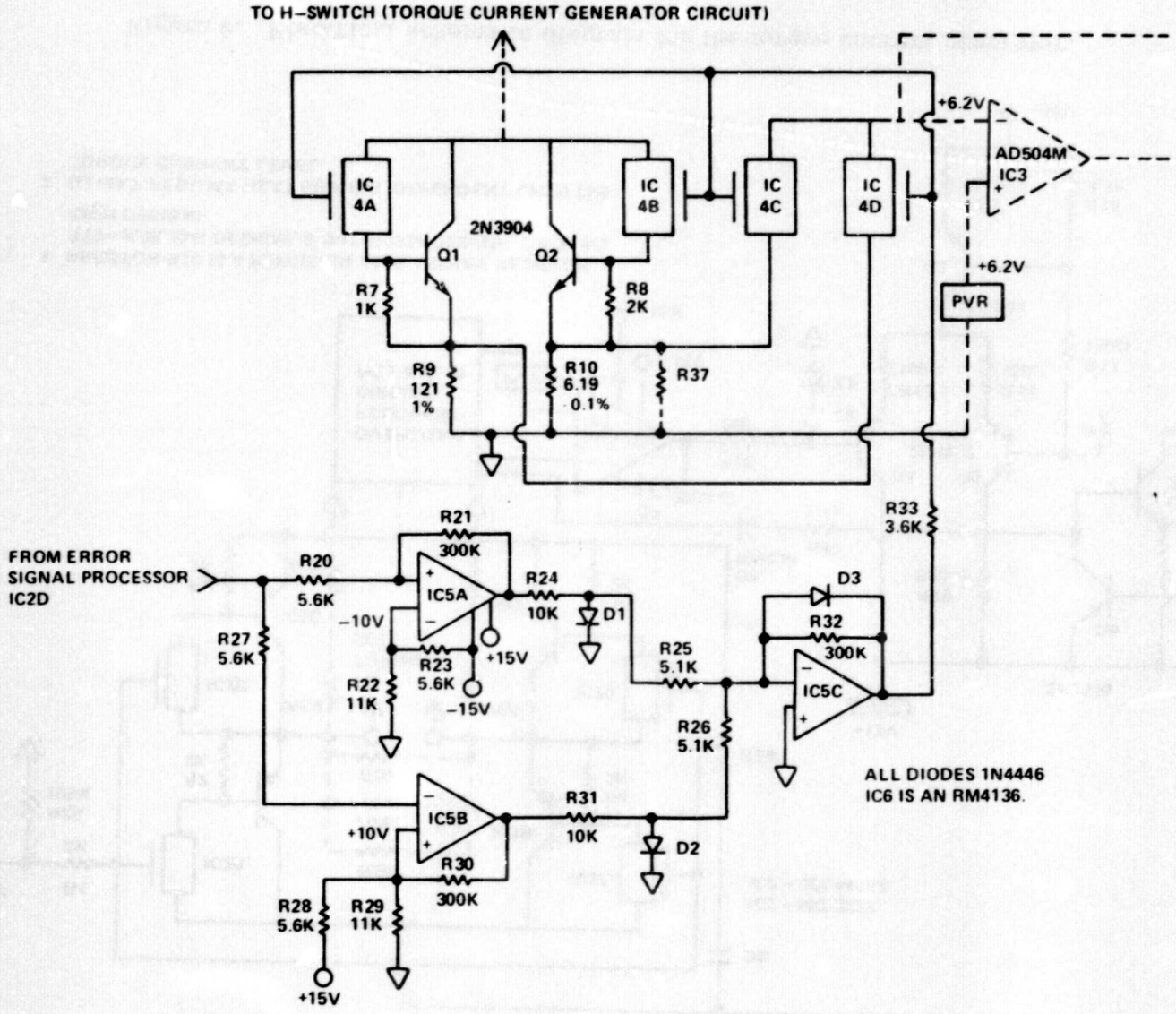
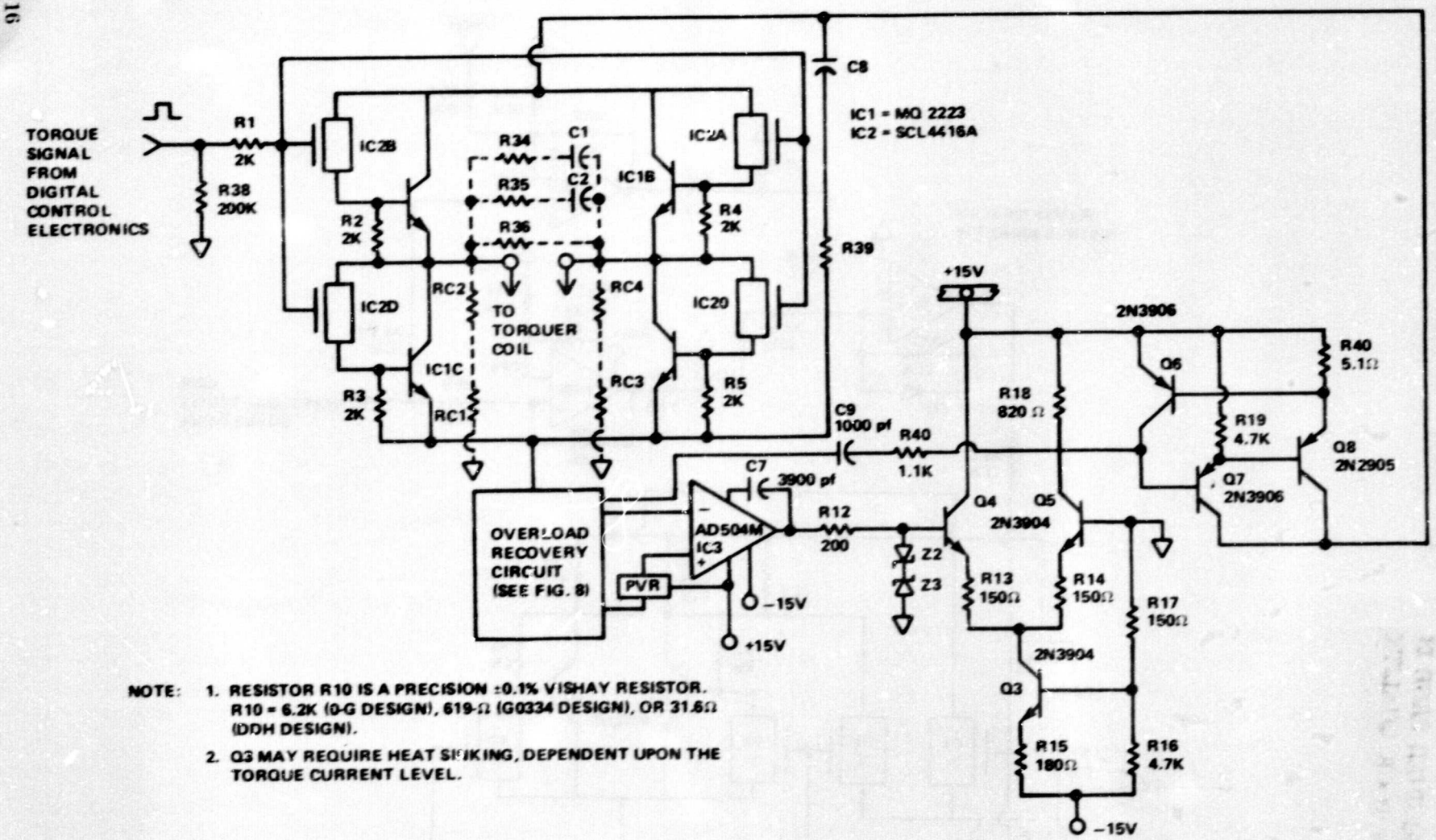


Figure 8. Overload recovery circuit.



NOTE:
1. RESISTOR R10 IS A PRECISION ±0.1% VISHAY RESISTOR. R10 = 6.2K (0-G DESIGN), 619-Ω (G0334 DESIGN), OR 31.6Ω (DDH DESIGN).
2. Q3 MAY REQUIRE HEAT SINKING, DEPENDENT UPON THE TORQUE CURRENT LEVEL.

Figure 9. Electrical schematic diagram for the torque current generator.

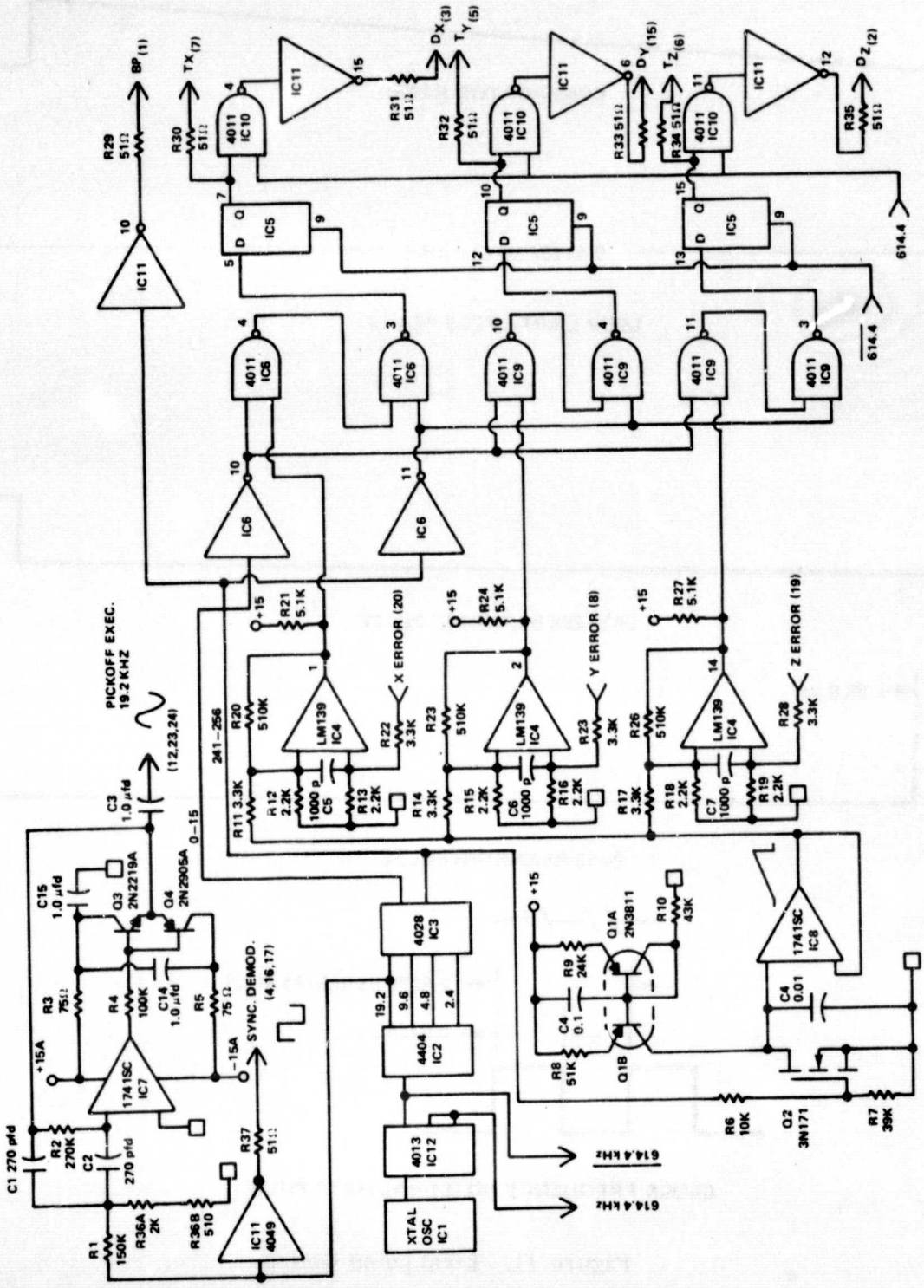


Figure 10. Digital control electronics.

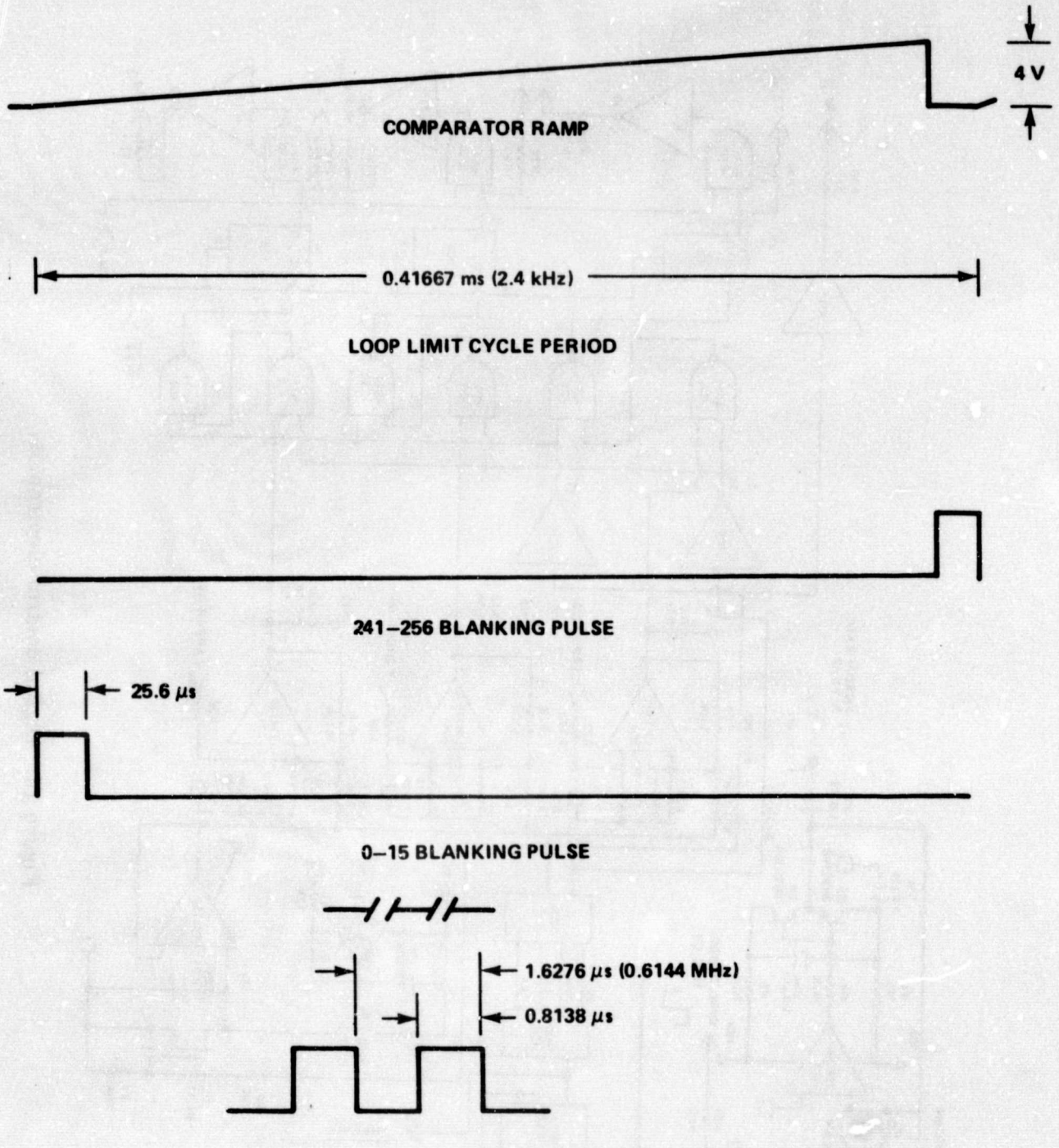


Figure 11. Loop pulse timing.

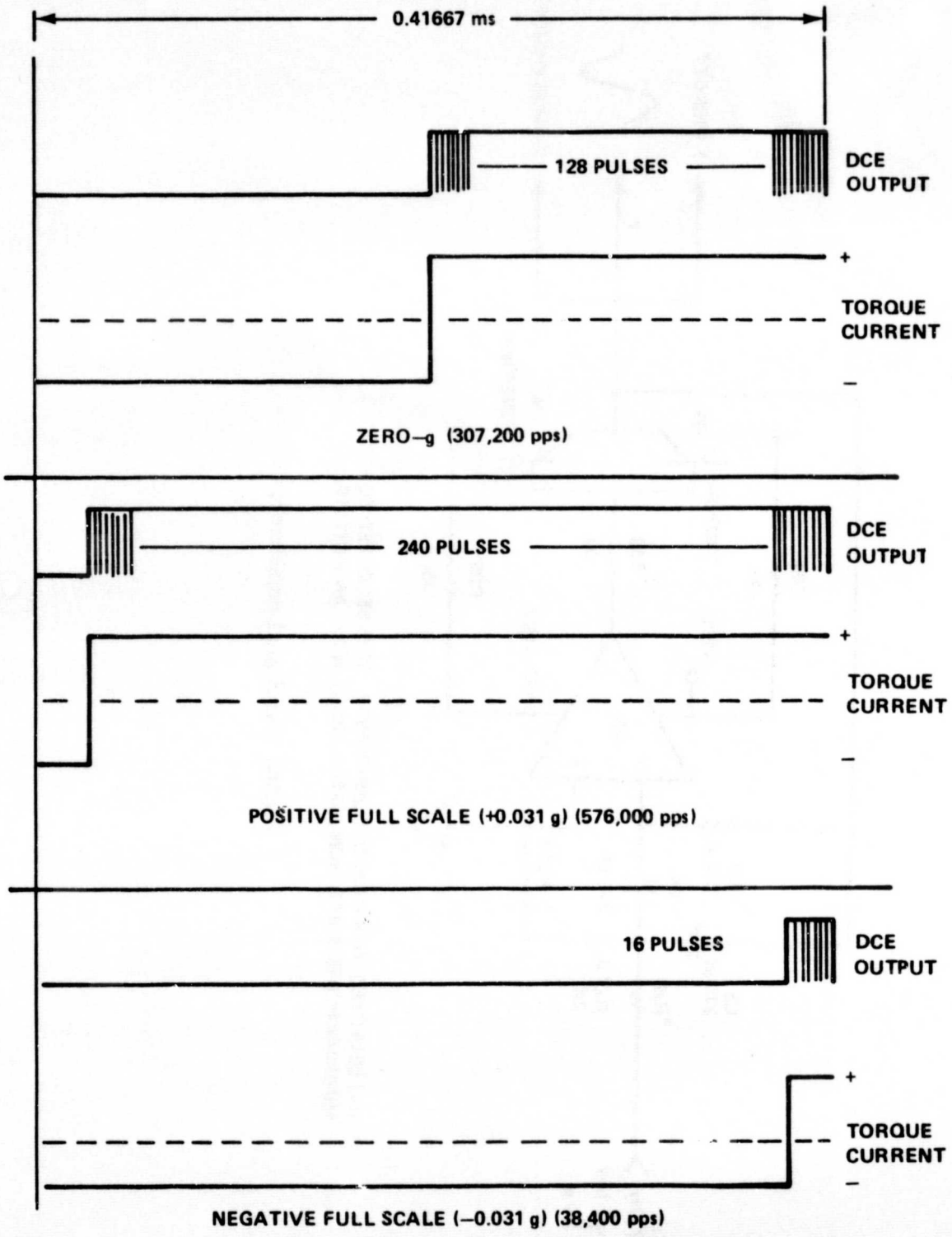
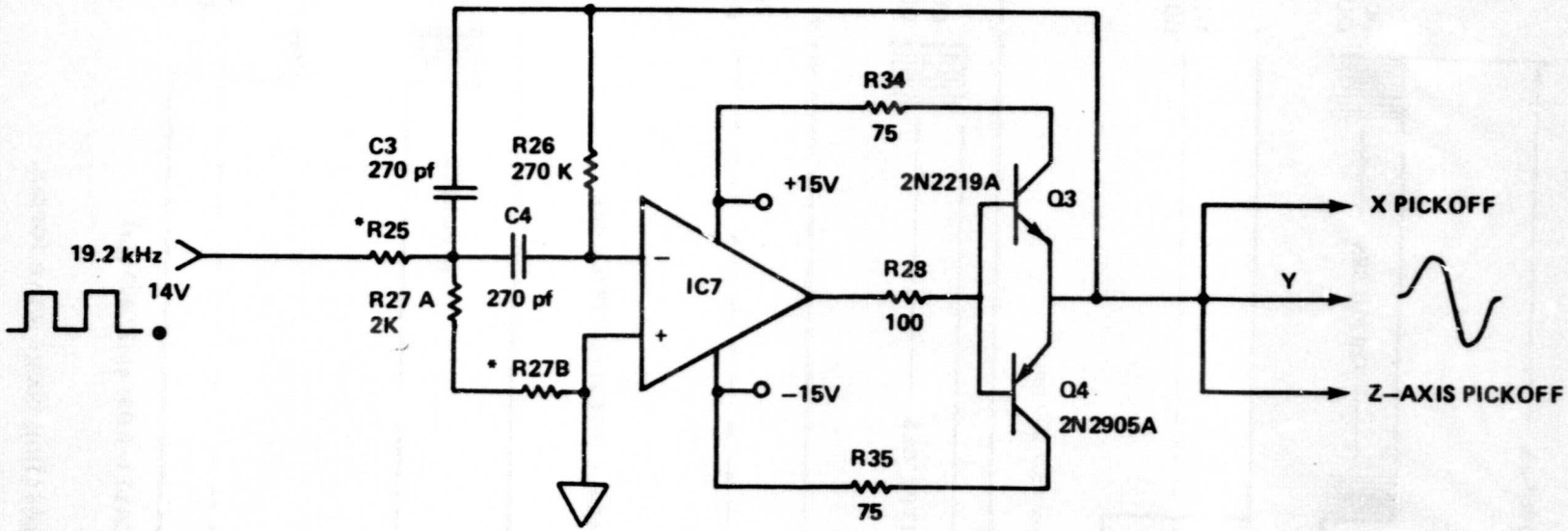


Figure 12. Operating range wave forms.



* R25 SELECTED FOR GAIN REQUIREMENTS. R27B SELECTED FOR MINIMUM PHASE SHIFT (NOM. R27B = 820 Ω). IC7 IS AN MC1741S.

Figure 13. Signal generator.

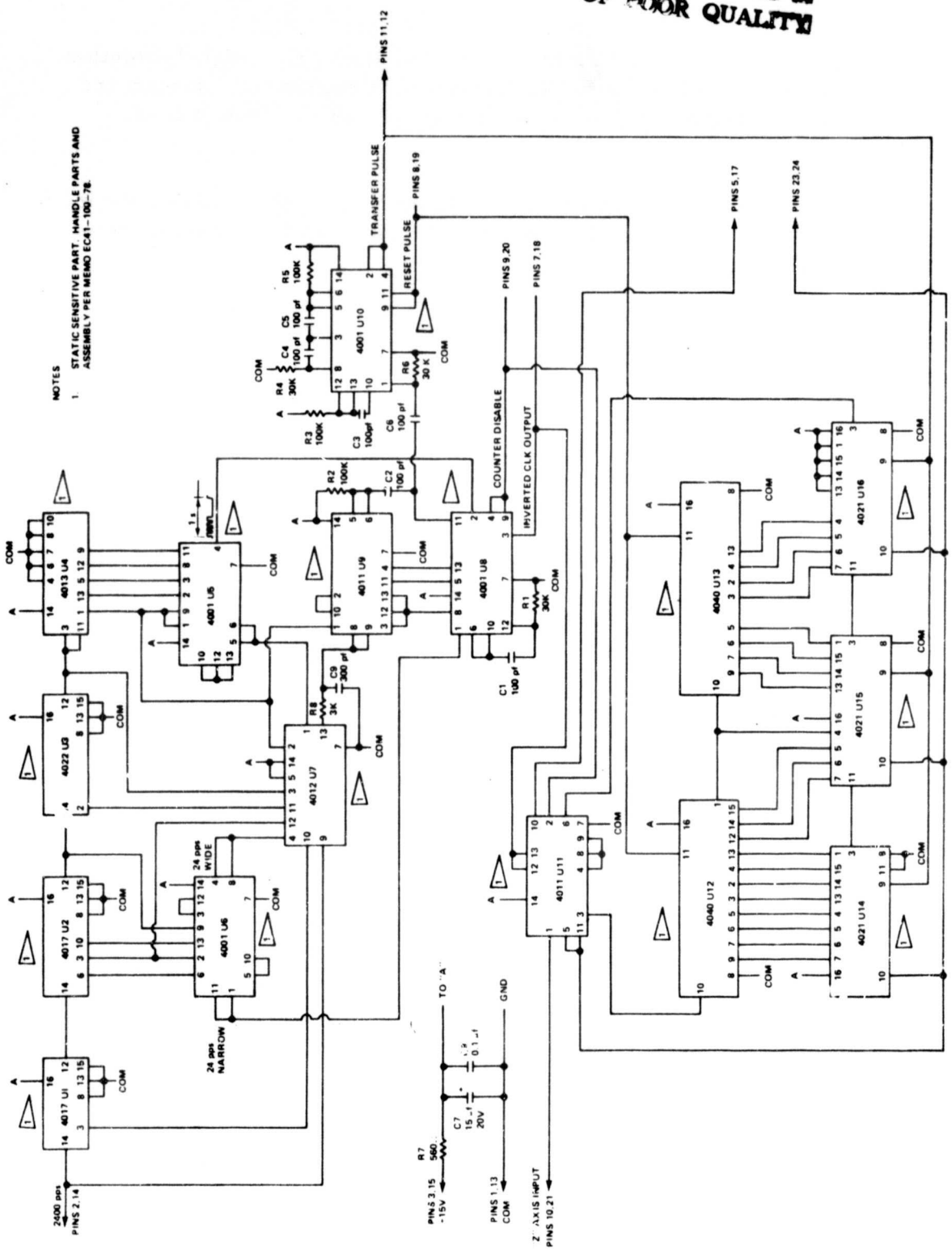


Figure 14. Signal conditioner schematic.