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PHASE 2

ARRAY AUTOMATED ASSEMBLY TASK

LOW COST SILICON SOLAR ARRAY PROJECT

QUARTERLY TECHNICAL REPORT No.4

July - September, 1978

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JPL CONTRACT NO. 954865

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"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE"

PREFACE

The information presented in this report, represents the work performed from July 1st, 1978 through September 30th, 1978 by Sensor Technology, Inc., in Chatsworth, California. The program is directed by Sang S. Rhee. Principal contributors include Gregory T. Jones, Kimberly L. Allison, Sanjeev Chitre, Charles Snyder, Louis R. Rosinski, Nelson E. David and A. PeBenito.

ABSTRACT

Work on Phase 2 of the Array Automated Assembly Task, a low-cost solar array project, was conducted this quarter. This project covers the period from July 1st, 1978 through September 30th, 1978.

Data was gathered and analysis continued on seventeen process groups. Ten of these process groups were completed; six process groups were completed this quarter. They include: laser scanning inspection, low pressure vapor metal deposition, wafer plating, solder coating and flux removal, cell handling for module construction, and laser trimming and holing automation. Work on the remaining tasks lies in the intermediate stage.

Very promising results to date were achieved. Several modifications instituted in the wafer surface preparation process have served to significantly reduce the process cost to 1.55 cents per peak watt in 1975 cents. Performance verification tests of a laser scanning system showed a limited capability to detect hidden cracks or defects, but with potential equipment modifications this cost effective system could be rendered suitable for our present applications.

Installation of a new electroless nickel plating system was completed along with an optimization of the wafer plating process. The solder coating and flux removal process verification test was completed. An optimum temperature range of 500-550°C was found to produce uniform solder coating with the restriction that a modified dipping procedure is utilized.

The construction of the spray-on dopant equipment was completed this quarter. A preliminary process verification test of the front surface spray-on dopant process produced 90 mm hexagonal solar cells with 11.2 to 12% efficiencies. Other performance verification tests led to the optimization of key parameters related to the dopant spray-on performance and throughput rate. A significant reduction in the dopant consumption rate led to a corresponding reduction in the overall process cost. A preliminary process cost estimate for the application of both front and back surface spray-on dopants is 1.52 cents per peak watt in 1975 cents.

A cumulative summary of SAMICS results to date indicate that the 1986 LSA goals for CELLCO can be achieved. The preliminary results show a process cost of 21.37 cents per peak watt in 1975 cents for CELLCO. A further cost reduction by about 4 cents to achieve

total process cost well below the LSA goal of 18.7 cents per peak watt could be made by eliminating the laser holing operation. Additional work, however, is recommended on the overall module cost to evaluate this potential area for cost reduction.

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INTRODUCTION

An automated processing sequence is being investigated in seventeen process groups which each encompass a number of processing steps. An indepth analysis of the process steps incorporated within the individual process groups is currently being performed, and each group is discussed in the technical section of this report. A final SAMICS report will be submitted at the conclusion of the overall process analysis.

TECHNICAL DISCUSSION

1. Cell Test Data Acquisition

All work has been completed for this task. A solar cell test data acquisition system has been fabricated and its feasibility in terms of production line applications has been evaluated and found to comply with previous expectations. This equipment has demonstrated than an automated system for collecting data on solar cell performance is extremely conducive for module assembly.

2. Plasma Etching of Resist

The process of plasma etching of resist has been reviewed and its applicability towards the removal of thick film resist has undergone extensive investigation. The available evidence points conclusively to the fact that the process time for a 5 mil thick resist used throughout the photovoltaic industry will be approximately 40 hours. SAMICS shows that the cost per watt for this process is $1.02. In view of this result the application of plasma etching to thick film resist removal does not look promising in the near future.

3. Laser Trimming and Holing Operation

A wafer trepanning experiment and also a wafer cracking experiment was performed by Quantronix Corporation in order to ascertain the feasibility of these two processes. In their final report to Sensor Technology, they presented documentation of both studies, and concluded that these processes yielded favorable results. Following the wafer trepanning experiment, all wafer samples were inspected for edge quality and found to be acceptable. Of the ten wafers which were processed in the wafer cracking experiment, one wafer was broken across the wafer face, which constituted a failure. However, the ease with which cracking occurred demonstrated the feasibility of the method.

Following the delivery and installation of the wafer trepanning and scribing equipment at Sensor Technology, a preliminary trepanning experiment was conducted in order to verify the results obtained by Quantronix Corporation. This test yielded negative results, which could be attributed to the shallow depth of the optical focal point. Consequently, optical adjustment of this equipment is currently underway in order to attain the optimum optical focal point depth for laserscribing a central hole in a hexagonal solar cell.

4. Wafer Surface Preparation

An indepth study and cost analysis of this process was completed during previous months. The results of this study indicated that the process cost was 6.39 cents per peak watt in 1975 cents, which is in excess of approximately three times the pricing goal set by IPEG. The predominant cost factor incurred during the surface preparation process was material costs which accounted for almost 60% of the total processing cost. In particular, the exhorbitant cost of the chemicals utilized in the two cleaning steps had made it imperative that the wafer surface preparation process study be extended this quarter for the purpose of seeking a means of reducing the excessive chemical costs.

The first approach utilized in the attempt to rectify this situation was the extension of the use of the precleaning solution which consists of trichloroethylene and methanol. The previous cycle for this solution utilized 1000 wafers per 9.4 liter tank which led to a material consumption rate of 4.33 cc per wafer and yielded clean surfaces. It was found experimentally, that the extended use of the solution to 5000 wafers did not lead to any degredation in the subsequent performance of surface texturization which implies that a sufficient amount of organic contaminants had been removed from the wafer surfaces. Repeated

use of 5000 wafers per solution cycle proved to be consistently successful, and thus, the material consumption rate can be reduced to 0.9 cc per wafer without adversely affecting the texturizing process.

The final cleaning step was also modified this quarter in an attempt to effect a reduction in the overall texturizing process cost. In the final cleaning steps chemical cleaning agents were replaced with a rigorous D.I. water rinse. The results demonstrated that the rigorous D.I. water rinse did not lead to any degradation in cell performance. This implies that the NaOH residue on the wafer surface can be successfully removed by D.I. water with ultrasonic agitation. In retrospect, the two process modifications described above will serve to significantly reduce the overall texturizing process cost as evidenced from the results of an indepth cost analysis. The revised process cost which is 1.55¢ per peak watt, is a considerable improvement over the previously reported value of 6.39 cents per peak watt., and conforms to the 1986 LSA price guidelines.

5. Laser Scanning

A representative from Sensor Technology, Inc., recently visited Advanced Semiconductor Materials Laboratory in Phoenix, Arizona for the purpose of establishing the range of applicability of the ASM Automatic Surface Inspection System (ASIS). In this

capacity, samples of silicon cells with nickel metallization and solder, and also nickel metallization without solder on texturized and untexturized cells were provided for the performance verification tests of the ASIS equipment. The primary objectives of the performance verification tests were as follows:

(1) Detection of micro-cracks
(2) Detection of floating metal
(3) Detection of breaks in metallization which develop during the plating process.
(4) Detection of saw damage
(5) Detection of soldering defects

The current equipment has been designed specifically for the inspection of 3" diameter wafers, but with the incorporation of minor equipment modifications, its range of applicability can be extended to 90 mm diameter wafers.

The ASM Automatic Surface Inspection System (ASIS) is an MPU-controlled system that quantitatively measures the defect level present on a highly reflective surface. Primarily designed for application in the semiconductor industry, the ASIS system will auto-

matically monitor the wafer surface quality before and after critical processing steps.

The ASIS system incorporates a highly sensitive solid state detector to collect laser energy that has been scattered by defects such as surface haze, particles, scratches, fingerprints, moisture, hillocks, spikes and surface fractures. The laser beam traverses the wafer surface forming an Archimedes spiral, which ensures 100% coverage of wafer surfaces in 4 seconds. The system compares product wafers against standard or "clean" wafer data stored in memory. This unique capability makes it possible to measure patterned wafers at any process steps, up to metallization. This system is equipped with automated cassette loaders and sorting stations and with control electronics and software to provide sorting of measured wafers into pre-selected surface quality groups.

During the course of the experimental studies, the laserbeam size which is currently 15 mils wide, has been determined to be a major limiting factor with regard to the ultimate diversity in application of the ASIS equipment. This conclusion is a consequence of the inherent resolution limitations of the laser beam.

It was experimentally shown for polished surfaces, that major cracks greater than 15 mils, saw damage, and fingerprints could all be easily detected. Due to the inherent resolution limitations of the laser beam, micro-cracks, floating metal, and poor solder contacts were all undetectable. This same line of reasoning will apply equally well to texturized surfaces with the one exception of fingerprint detection which is precluded as a result of the discontinuity of the fingerprint pattern over the pyramidal surface structure of the texturized cell.

A preliminary cost estimate has been performed for the ASM automatic surface inspection system for the purpose of establishing its cost effectiveness. The resulting process step cost corresponding to the ASM system was found to be 0.672¢/watt in terms of 1975 dollars which is low enough to ensure its feasibility for usage in an automated assembly line. In addition, potential equipment modifications designed to enhance the throughput of this system will serve to lower the process costs even further.

The only problem area foreseen at the present moment is the detection of hidden cracks or defects such as poor solder contacts and floating

metal. A tentative solution to this dilemma would be to alter the orientation of the laser beam from normal incidence to non-normal incidence and also to decrease the laser beam width. It is therefore recommended that an investigation of the technological feasibility of the proposed modifications be implemented in the future, since the present ASIS equipment is unsuitable for most of our applications.

6. Wafer Printing

The general review of thick film printing machines conducted during the previous quarter provided the indication that state-of-the-art technology can adequately transform the throughput capability of the current machines to the elevated rate of 7200 wafers/hr. The manufacturers possessing this capability include Presco Division of Affiliated Manufacturing Inc., Universal Instrument Co., and Fursland Division of Hutchington Industrial Co. For the purpose of obtaining a process cost estimation, the commercially available Fursland Model 33 was chosen since it is an automated version of the equipment currently in use at Sensor Technology, Inc.

A detailed SAMICS cost analysis for the wafer printing process was performed during the previous quarter. The SAMICS calculation indicates that the printing process cost accounts for 0.77¢/peak watt and the drying process cost accounts for 0.44¢/peak watt. The total printing process cost thus becomes 1.21 cents/peak watt in terms of 1975 dollars, which is consistent with the 1986 LSA pricing goals.

7. Low Pressure Vapor Metal Deposition

The original plan devised for this task was formulated exclusively to investigate the deposition of p^+ copper onto silicon wafers. The low pressure vapor metal deposition of p^+ copper onto silicon wafers would serve primarily as a back surface field.

Despite the fact that numerous companies were contacted which reportedly possessed vapor metal depositions, no one could be found during the scheduled time phase of this program task to have successfully performed p^+ copper depositions. Consequently, any conclusive results pertaining to the viability of

this process is not reported.

8. Silicon Nitride A.R. Coating

The System 8000, manufactured by LFE Corporation in Waltham, Massachusetts can be cost-effective as a mechanism for depositing silicon-nitride antireflective coating on solar cells only if its throughput rate is significantly enhanced. With this objective in mind, LFE Corporation has indicated that it is technologically feasible to incorporate a number of changes in the existing system in order to achieve an enhanced throughput.

The wafer throughput of the System 8000 is strongly dependent upon the following five parameters:

1. Wafer velocity on the process track
2. Time for a single wafer to move both through the vacuum locks
3. Travel time for a wafer on the Sender and Receiver tracks
4. Index time for the cassettes on the Sender and Receiver
5. Deposition Rate

The problem of enhancing the wafer throughput therefore consists primarily of optimizing these five parameters by means of equipment modifications.

The technical staff at LFE has accumulated extensive experience with the System 8000 and can foresee no immediate problems associated with the adoption of the state-of-the-art equipment modifications described above.

A batch of one-hundred wafer samples have been delivered to LFE Corporation for a performance verification test of the silicon nitride A.R.coating process. These wafers were sent out prior to the pattern printing and metallization process steps in order to establish the viability of inserting the A.R.coating process step within the overall cell processing sequence in contrast to the more conventional method of performing the A.R.coating process step after the solar cell has been fabricated. No conclusive results are available at the present time.

A batch of 50 fully processed solar cells have been delivered to the LFE facility to be sample coated with silicon nitride A.R.coating. The application of silicon nitride onto the batch of 50 silicon solar cells has been completed and they were received by Sensor Technology.

A preliminary electrical performance test has been conducted on five, fully processed solar cells which have each undergone the silicon nitride A.R. coating process step. This test was implemented by comparing the I-V curves of solar cells which had undergone the A.R.coating process, with the I-V curves of cells which had undergone an identical processing sequence with the exclusion of the A.R.coating step. Upon analysis of the representative I-V curves which are shown in Figure 1, it was found that the silicon nitride, A.R.coated cells displayed a definite improvement in electrical performance over the uncoated cells. In order to illustrate this point, I_{SC} for the A.R. coated cells was found to be 1.42 amps with a corresponding efficiency of 11.3% whereas for the uncoated cells, I_{SC} was 1.25 amps with a correponding efficiency of 9.9%.

9. Wafer Plating

All work has been completed for this task. The installation of the revised wafer plating system reported in the previous quarterly report has been completed along with the optimization study of the wafer plating process. The major problem which had to be overcome in the optimization study was the

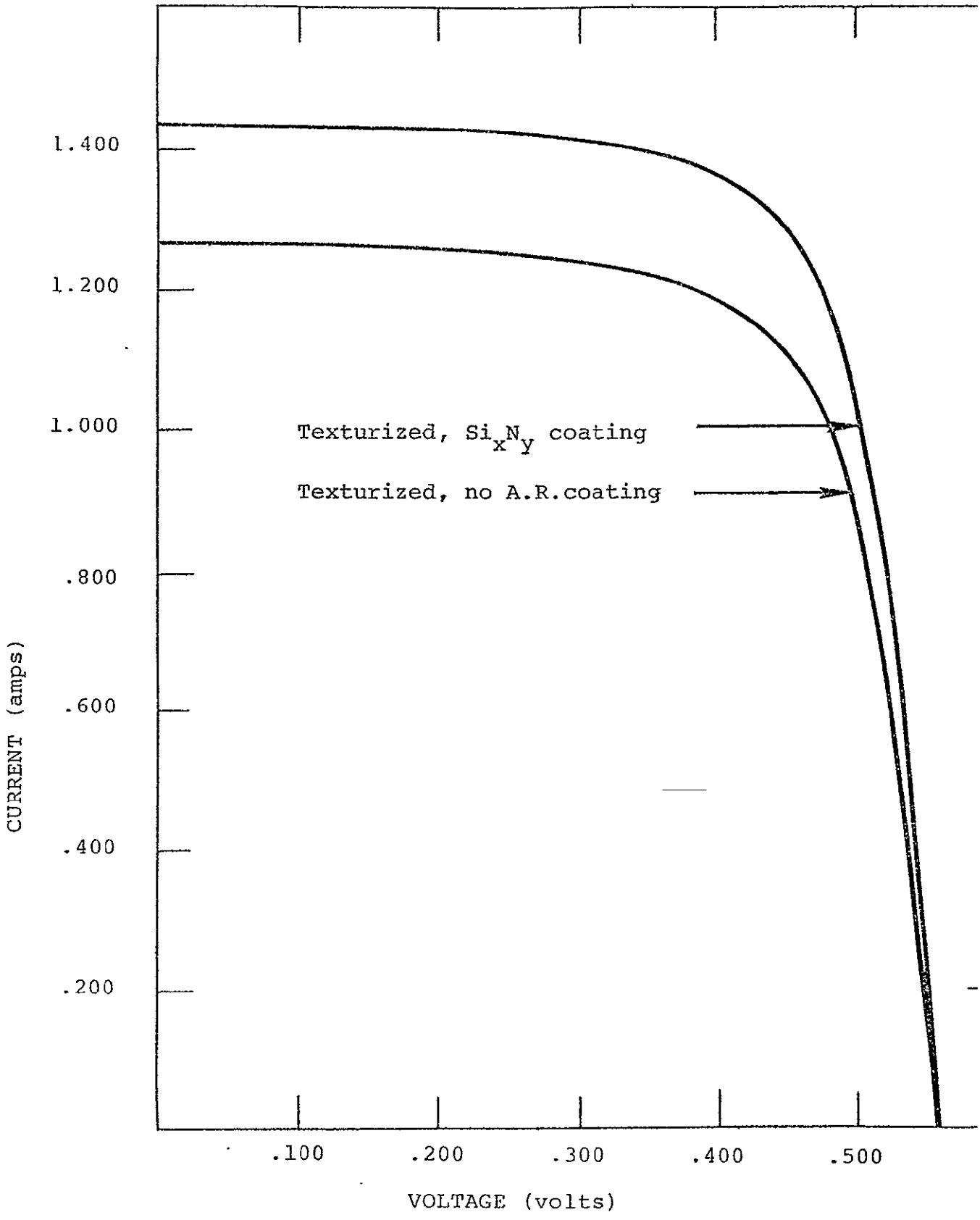

Figure 1. Electrical performance curves of texturized solar cells with and without a silicon nitride (Si_xN_y) anti-reflective coating. The solar cells are hexagonal with 50.8 cm^2 active area. They are tested at 28°C, 100 mw/cm^2 under tungsten light.

reduction of the material consumption rate without causing a corresponding degredation in the plating performance capability. A total of three hundred 90 mm wafers underwent the revised processing procedure in order to establish the production rate and plating performance capability. A large portion of the 300 cells which had been utilized in the revised plating process were obtained directly from the regular production line.

The important findings resulting from the revised wafer plating process sequence are as follows:

(1) The consumption rate of the gold solution was reduced by a factor of one-half.

(2) The nickel solution usage time was extended by a factor of four.

(3) The overall processing time was reduced by 20%.

(4) The plating uniformity due to the new system had reduced the variations in cell power output from 14.7% to 4.6%.

(5) The process yield was significantly increased. All 300 wafers were defect free.

The major contributing factor responsible for the improvements described above lies entirely with the use of the new, large sized bath with uniform solution and precise temperature control. A comparison between various characteristics of the new larger-sized bath and the formerly used bath will further illustrate this point. The former bath for the gold solution had only a 3 liter capacity, whereas the new gold bath has an 8 liter capacity. The new nickel bath functions by means of indirect heating of the walls, while the former nickel bath used a directly submerged heating element. Consequently, the solution temperature variation in the new bath was $\pm$ 2°C, whereas the former nickel bath had a $\pm$ 5°C temperature variation. The former nickel bath also had localized heat variations in the vicinity of the heater element. The localized heat variations of the former nickel bath was observed to cause breakdowns in the resist, since the resist could not withstand temperatures in excess of 85°C. In spite of the fact that the former nickel bath was maintained at 80°C, the average temperature at the wafer surface may have been higher due to poor convection of the solution. All of these facts make it apparent

that the old nickel bath solution becomes quickly contaminated, which in turn causes the usage time of the solution to be significantly reduced. The new nickel bath maintains precise temperature control and hence good solution uniformity. In addition, a newly installed agitation system underneath the nickel bath has proven very effective in maintaining the solution uniformity. An increase in bath temperature to 83°C did not lead to resist failure and the reduction in processing time from 5 to 4 minutes has not been found to sacrifice plating performance. The feasibility of the new plating method has thus been amply demonstrated by experimental means.

10. Solder Coating and Flux Removal

All work has been completed for this task. A solder coating and flux removal process verification test was devised and implemented in previous months. A specially designed fixture which served in the capacity of a wafer carrier had been utilized along with a 6" x 6" x 6" solder bath with 40/60 solder, during the testing procedure. The manually performed solder dipping test was able to provide information pertaining to the optimum operating temperature of the system. At a temperature of 450°F the solder proceeded

to coagulate on both the front and back surfaces of the cell which indicated that this temperature was too cold. The temperature of 500°F was found to yield good solder coating uniformity only after adopting a modification in the dipping procedure which consisted of removing excess solder by striking the fixture containing vertically positioned cells against the solder pot and then cooling the cells in a horizontal position. When the dipping procedure was carried out at this temperature without utilizing the above modification, the solder coagulated in isolated segments of the back surface of the cell, which of course resulted in nonuniformity of the solder coating.

For temperatures in excess of 600°F, the cells had incurred excessive breakage due to thermal stresses.

The conclusion of the solder coating and flux removal process verification test was that the optimum temperature range providing solder coating uniformity was 500-550°F with the restriction that the modified dipping procedure advanced above is utilized.

To supplement these test, it is recommended that the following potential process improvements should undergo investigation:

(1) use of a preheater

(2) flux dipping

(3) air blow to enhance uniformity of solder thickness.

11. Cell Handling for Module Construction

Cell handling for module construction will require precise positioning techniques in addition to an approximate rate of 2 cells per second if the module construction line is to produce 7200 wafers per hour or 60 modules per hour in accordance with the projected 1986 industrial production goals.

Several varieties of cell handling units are available from semiconductor industries and most of them are designed to fit a particular machine. It has been determined that the robot arm technique is extremely suitable for our present requirements since this technology is readily available and can easily be adapted to solar cell applications. Consequently, all work has been completed for this task and a SAMICS analysis is scheduled to be performed.

12. Laser Trimming and Holing Automation

All work for this task has been completed including a detailed cost analysis. Two potentially automated systems capable of laserscribing silicon wafers to produce hexagonally shaped wafers with central holes have been studied in order to establish the output capability, maintainability, reliability, and economic characteristics of each system. Upon comparing the two systems, it was found that the serial flow laserscribing system was more cost effective than the parallel flow system. The cost analysis indicates that the critical cost factor is the utility cost which accounts for almost 90% of the total process cost. This conclusion is not entirely unexpected since the laser efficiency is only 0.5% for the most technologically advanced laser system currently available in todays market. Consequently, the most effective method of reducing the laser scribing process cost will be to improve the laser efficiency.

13. Cell and Module Test and Data Storage

Literature pertaining to the microprocessing equipment currently available in today's market had been reviewed in previous months and a system was selected which appeared to be compatible with out present requirements. The Motorola M6800 micro-

processor development system with a line printer was selected for usage in this task, and both items have been received by Sensor Technology. The line printer will be utilized in conjunction with the microprocessor to print out the results of the work scheduled to be performed for this task.

The major work performed during this quarter was the design, fabrication and debugging of all essential logic and computer interface electronics which permit collection of relevant solar cell electrical performance characteristics via computer-controlled automated test equipment. To date, the test logic and computer interface electronics have been designed and all parts ordered.

Programming of the Motorola M6800 microprocessor system is currently in progress. The final program completion will be achieved at the time of the system integration. The electronic test circuit board has been built, however, the test was delayed due to the late delivery of several critical parts. Final testing and interface with the Motorola M6800 system is scheduled for next quarter.

14. Module Construction Study

A flameless inert gas soldering method was investigated in order to determine its applicability for use in conjunction with a specified base material for the flexible pc sheet. The flameless heating unit studied offers extremely precise temperature control for production soldering, brazing, bonding, curing or melting at temperatures up to 1600^{o}F. The heater consists of a tungsten filament inside a quartz tube over which air or inert gasses such as argon or nitrogen are passed. The coil design provides extremely efficient energy transfer which permits precision non-contact heating of parts in open of confined areas. Controls permit regulation of gas flow, pressure, and electrical input into the heater thus allowing pin-point repeatable heat control.

The following experiments have been performed with this equipment:

(1) Front surface contact soldering

(2) Back surface contact soldering

(3) Soldering cell to a 2oz. copper Kapton sheet

All experimental results proved to be extremely satisfactory. The applicability of this process to production line applications will be considered next quarter.

15. Spray-On Dopants

The construction of the spray-on dopant equipment was completed, and an initial performance verification test was conducted by Advanced Concepts Co. Upon completion of this performance verification test, the spray-on dopant equipment was transferred to Sensor Technology, and in-house, preliminary experimentation was performed in order to optimize key parameters related exclusively to the dopant spray-on performance and throughput rate.

A batch of ten, 3.5" modified hexagonal solar cells with parallel track grid patterns were selected for usage in the spray-on dopant equipment process verification test in Advanced Concepts. Each cell underwent the following sequential processing steps:

(a) Texturizing

(b) Application of spray-on-dopant

(c) Aluminum back surface metallization

(d) A.R.coating

The wafer samples were coated with Emulsitone N 250 phosphosilica film by means of a 20 mm diameter nozzle. No spray-on dopants had been applied to the back surfaces of the cells, however, a standard aluminum evaporation procedure was used to provide the back surface metallization.

Upon completion of the above mentioned processing steps, the electrical performance of each solar cell had been experimentally measured and a quantitative analysis for the determination of key electrical parameters such as fill factor and cell efficiency was made from the experimental results. The resulting conclusions were used to elicit a comparison with a batch of cells which had undergone an identical processing sequence with the one exception of the utilization of a standard $POCl_3$ diffusion in place of the spray-on dopant process. It is evident from Figures 2 and 3 that the efficiency range of the two batches lies between 11.2% and 12% and the fill factors are within a range of 0.62 - 0.66. The conclusion which may be drawn from these results is that both processes yield cells which maintain the same degree of electrical performance. In addition, it was found that the electrical performance of cells which had been processed with spray-on dopants remains insensitive to thickness variations of the dopant film.

The following additional conclusions were formulated on the basis of the preliminary process verification test:

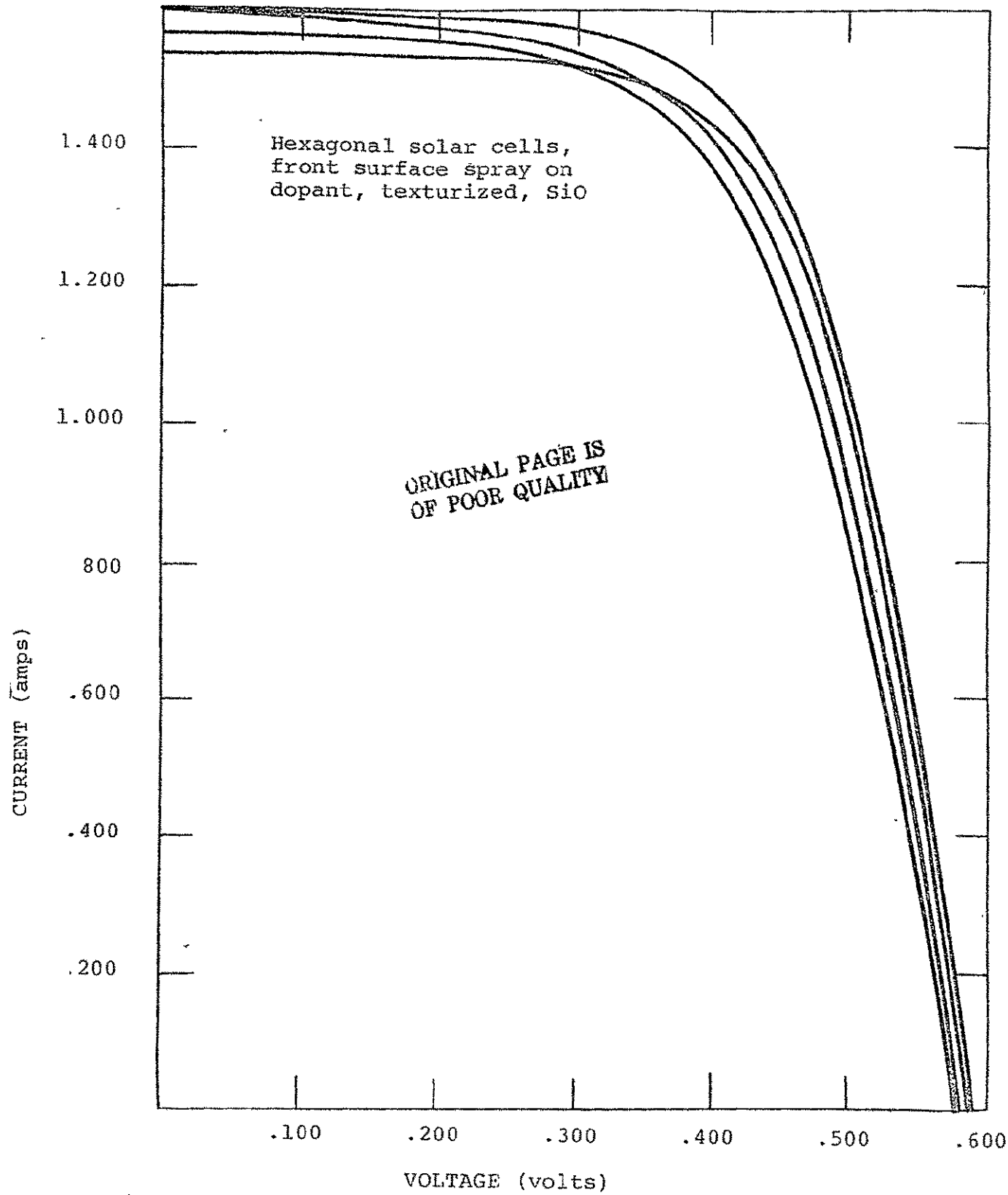

Figure 2. Electrical performance curves of hexagonal solar cells made by spray on dopant method (front surface). The solar cells are texturized, A.R.coated with SiO and have a 50.8 cm^2 active area with a parallel track pattern. They are tested at 28^{o}C, 100 mW/cm^2 under tungsten light.

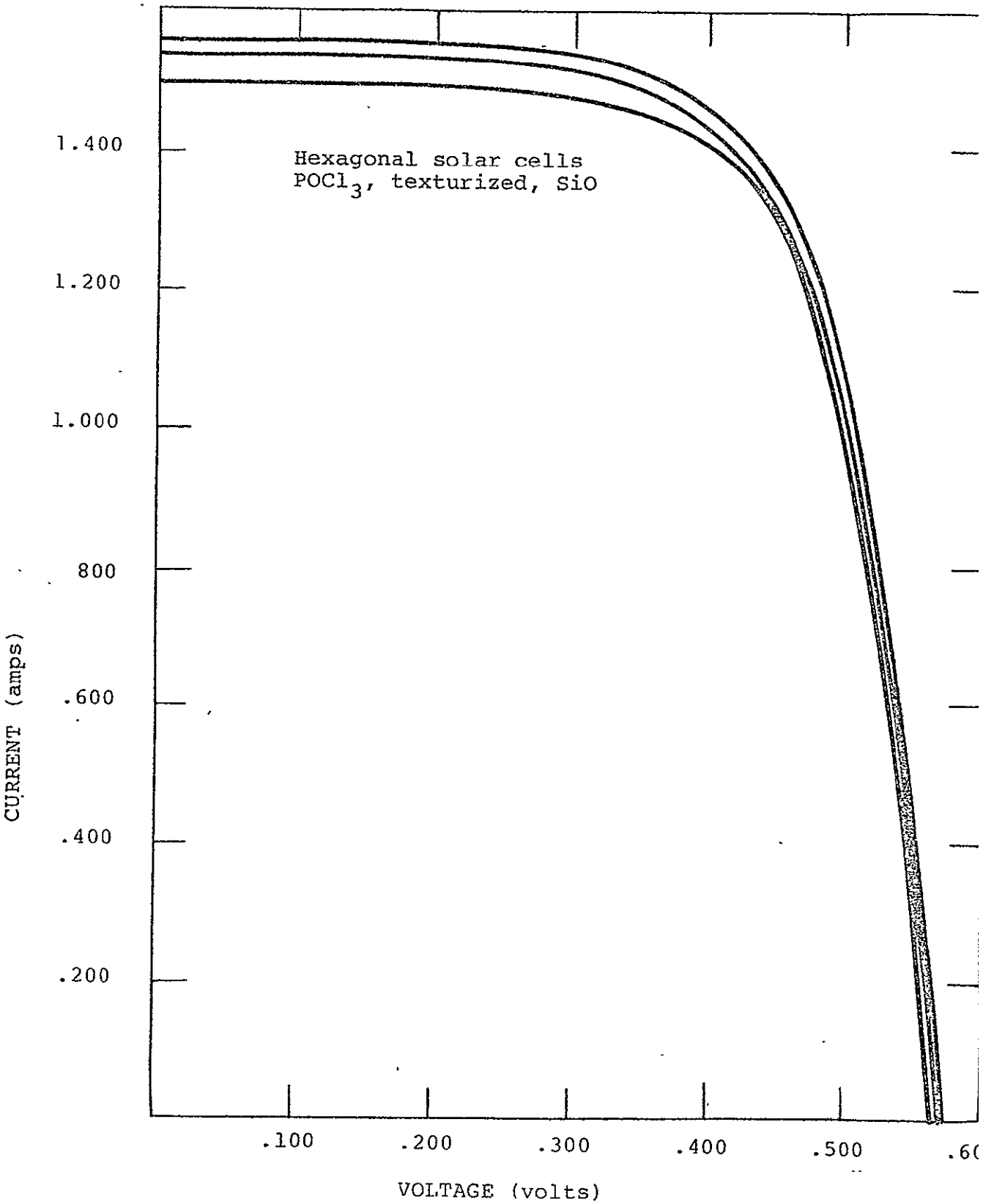

Figure 3. Electrical performance curves of hexagonal solar cells made by $POCl_3$ diffusion method. The solar cells are texturized, A.R.coated with SiO and have a 50.8 cm^2 active area with a parallel track pattern. They are tested at 28°C, 100 mW/cm^2 under tungsten light.

(a) Dopants do not cross over to the back wafer surface to any significant degree.

(b) A thickness uniformity of 5 to 7 μ was obtained.

(c) The dopant consumption rate was 5.55cc/min. which implies 0.3 cc of dopant per wafer at a conveyor speed of 2ft/min.

(d) The equivalent throughput rate of the conveyor was 1080 wafers/hour.

The most significant achievement obtained from the process verification test was the reduction of the dopant consumption rate, which leads to a corresponding reduction in the overall process cost. A preliminary SAMICS calculation shows that the process cost for the application of both front and back surface spray-on dopants is now 1.53 cents per peak watt in 1975 cents.

16. Conveyorized Dopant Diffusion

Pacific Western Systems Inc., has temporarily displaced their laboratory facility and therfore indicated to us that they would be unable to perform our designated tests within the timeframe of this contract. Advanced Silicon Material Co., ASM, has subsequently been selected to perform the dopant tests and to design a fixture to simulate the conveyor. Upon carrying out the experimental

test tuns in the LTO system, the special fixturing for the 3¼ inch wafers was found to actually improve the uniformity across the wafers to an extent which exceeded the expectations of ASM, made on the basis of their system's guaranteed performance capacity. A total of 25 cells had undergone processing in the LTO system, with a deposition time of 9 minutes at 425^{o}C and .196 torr. The processed cells have recently arrived at Sensor Technology, and electrical performance tests are scheduled to be performed next quarter in order to determine the process feasibility.

17. Module Model Fabrication and Materials

The majority of the parts required for the construction of the module model have been received and the cells have been fabricated. The flexible printed circuit sheet has been delivered to Sensor Technology, and the module model is scheduled to be constructed during the following quarter.

B. SAMICS - Process Cost Analysis

1. Wafer Surface Preparation (Ref. Task 4)

This process cost computation has already been performed and is discussed in the 2nd quarterly report. However, several process improvements which were instituted during the present quarter have necessitated a revision of the previous cost analysis. A major improvement dealt with the wafer cleaning process. The detailed technical discussion concerning this improvement is presented in Section A. The modified SAMICS format A is presented in the standard JPL format. The resulting modified process costs are presented in Table 1.

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] WFSURPR

A2 [Descriptive Name] Wafer Surface Preparation

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] SURPRWF

A4 Descriptive Name [Product Name] Texturized and Surface Clean Wafer

A5 Unit Of Measure [Product Units] Wafer

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 100 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 96 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] 0.875 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	PROTNK	DRTUN	WFHDMC
A9a	Component [Descriptive Name] (Optional)	Process Tanks	Drier Tunnel	Wafer Handling Machine
A10	Base Year For Equipment Prices [Price Year]	1978	1978	1978
A11	Purchase Price ($ Per Component) [Purchase Cost]	$120,000	$31,000	$20,000
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	7
A13	[Salvage Value], ($ Per Component)	$10,000	$3,000	$1,000
A14	[Removal and Installation Cost] ($/Component)	$4,000	$2,000	$500

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

mat A: Process Description (Continued)

A1 Process Referent (From Page 1 Line A1) WFSURPR

RT 4 — DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	448	Sq.Ft.	Factory Space (Type A)
B 3672 D	1	Prsn.a year	Chemical Operator II
B 3736 D	0.1	" " "	Inspector (Q.C.)
B 3736 D	0.05	" " "	Maintenance Mech. II
B 3688 D	0.05	" " "	Electronics Maint.
B 3256 B	0.014	" " "	Production Planner

PART 5 — DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
G 1001 D	0.09	Liter	Trichloroethylene
G 1002 D	0.09	Liter	Methanol
E 1600 D	0.0882	Lbs.	Sodium Hydroxide
E 1416 D	0.0783	Cu.Ft.	Nitrogen Gas
C 1144	0.03531	Cu.Ft.	D.I. Water
C 2032 D	10	Cu.Ft.	Clean Compressed Air
C 1064 B	0.01	Cu.Ft.	Natural Gas
C 1032 B	0.289	Kw.Hr.	Electric Power
D 1048 B	1.676	Gal.	Polluted Water
D 1064 D	0.05	Wafer	Rejected Wafer

PART 6 — INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
P WAFER	0.9995	Wafer / Wafer	Wafer from Wafer CO.

Prepared by Sang. S. Rhee Date 9/30/78

Table 1. Process costs of wafer surface preparation process.

	1986 cents	1975 cents
Equipment	0.32	0.167
Floor Space	0.1	0.052
Labor	0.5	0.260
Material	0.81	0.422
Utility	.523	0.273
TOTAL	2.253	1.1736

The process cost per unit peak watt turns out to be:

2.98¢/watt in 1986 dollars

1.55¢/watt in 1975 dollars

2. Spray-on Dopant Process (Ref. Task 15)

A revision in the preliminary SAMICS calculation of the spray-on dopant process cost presented in the third quarterly report had been necessitated due to an increase in the value of the overall throughput rate from 900 wafers/hr., to 1080 wafers/hr., and a decrease in the dopant consumption rate from a value of 2cc/wafer to .30 cc/wafer. The values of all other process parameters remain unchanged, and equation (3) in the samics section of the third quarterly report was again utilized for the computation of the process cost breakdowns and overall process cost. The results of the calculations are as follows:

EQUIPMENT	0.296
FLOOR SPACE	0.065
LABOR	0.296
MATERIAL	0.781
UTILITY	0.0887
TOTAL	1.5267 cents/peak watt

This result is considerably lower than the previously calculated overall process cost of 3.502 cents/peak watt. The process cost reduction will therefore render the spray-on dopant process extremely conducive towards the attainment of the projected 1986 pricing goals.

3. Nickel Plating Process (Ref. Task 9)

The process cost estimation for the newly installed nickel plating system was performed in accordance with the standard SAMICS industry as defined in the 2nd quarterly report. All data were obtained directly from experimental studies. The input data for SAMICS Format A is discussed below.

Process Characteristics

Six wafer carriers which contain 25 wafers each, constitute a single batch. The first three tanks which consist of the HF tank, gold tank, and overflow rinse tank compose a single station. The three nickel baths are also to be considered as a single station, as well as each of the two cascade tanks. These characteristics will therefore result in four processing stations. A batch of 150 wafers will remain at a station for 4 minutes and then be transferred over to the next station in one minute which leads to a production rate of 150 wafers for each five minute interval, or 30 wafers per minute. One hour per shift will be required for the clean-up period and the start-up period. Thus, the machine "up" time fraction becomes 0.875.

Equipment Cost

The machine was designed and fabricated at Sensor Technology. The actual cost of this plating system was $8,232.32.

Floor Space

The floor space includes operator working space and was measured to be 72 sq. ft.

Labor

One operator can handle this system at full capacity without any problem. In order to apply the SAMICS method as defined in the 2nd quarterly report, four shifts are assumed to be necessary in order to operate the plant for a 24 hour period. Two maintenance men who maintain the entire process line are assumed to be required during each shift. In addition, one production planner per shift will be used.

Utilitities and Commodities

Direct measurements from experimental test runs yielded the following material consumption rates:

(a) 49% Hydro-Fluoric Acid:

0.5cc/wafer = 15 cc/min. = 0.039 lbs/min.

(sp.gr. of sol. = 1.18)

(b) Gold plating solution (premixed commercial item)

0.5 cc/wafer = 15 cc/min.

(c) Nickel plating solution (premixed commercial item)

5cc/wafer = 150 cc/min.

(d) Nitrogen Gas

10 l/min. for each rinse tank

Total 20 l/min. = 0.706 cu. ft./min.

(e) D.I. water

1.5 gal./min for each rinse tank.

Total 3 gal/min = 0.401 cu. ft./min.

(f) Electric power:

3.12 KW heater unit per tank

Total power usage over three hours for these units is $3.120 \times {}^{1}/_{6} \times 3 = 1.560$ Kwatt-hr.

Power consumption per minute is 8.66 watt-hr./min.

Process Cost Computation

The temporary cell process catalog items which were utilized in the standard SAMICS Format A can be found in Table 2.

The process cost computation was achieved by means of the SAMICS work sheet in conjunction with SAMICS Format A. The wafer cost was set to zero in order to obtain the process cost along. In addition, the production yield was not taken into consideration

FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] ELNIPL

A2 [Descriptive Name] Electroless Nickel Plating.

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] NIPLC

A4 Descriptive Name [Product Name] Nickel Plated Cell

A5 Unit Of Measure [Product Units] Cell

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 30 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 20 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] 0.875 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	NIPLTK		
A9a	Component [Descriptive Name] (Optional)	Nickel Plating System		
A10	Base Year For Equipment Prices [Price Year]	1978		
A11	Purchase Price ($ Per Component) [Purchase Cost]	8232		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	800		
A14	[Removal and Installation Cost] ($/Component)	900		

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) ELNZPL

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A2064 D	72	sq.ft.	Factory Space
B3672 D	1	prsn.a yr.	Chemical Operator II
B3720 D	0.1	" " "	Inspector (Q.C.)
B3736 D	0.05	" " "	Maintenance Mech. II
B3688 D	0.05	" " "	Electronic Maint.
B3256B	0.014	" " "	Production Planner

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
E 1328 D	0.039	lbs.	Hydrofloric Acid
G 1010 D	0.015	liter	Gold solution
G 1011 D	0.150	liter	Nickel solution
E 1416 D	0.706	cu.ft.	Nitrogen gas
C 1144 D	0.401	cu.ft.	D.I. water
C 1032 B	0.0087	Kw.Hr.	Electricity

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
FSPPW	Front Sur.Print Cell	Cell / Cell	0.9995

Prepared by Sang. S. Rhee Date Sept. 20, 1978

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Table 2. List of temporary cell process catalog items

Catalog No.	Item Description	Units	Price	I_C	YR.	Account Class
G1001D	Hydrogen Gas	Cu.Ft.	0.258	C	75	E
G1002D	Tungsten Coil	Coil	1.75	D	77	E
G1003D	Strip Solution A	Liter	1.178	C	77	E
G1004D	Strip Solution B	Liter	1.580	C	77	E
G1010D	Gold Solution	Liter	13.40	C	78	E
G1011D	Nickel Plat.Sol.	Liter	1.210	C	78	E
G1007D	Resist Ink	Gal.	32.00	C	77	E
G1008D	Thinner	Gal.	40.00	C	77	E
G1009D	Silicon Oxide	Gr.	0.90	C	77	E
G1010D	60/40 Solder	lbs.	6.04	D	77	E
G1011D	Solder Flux 30%	Gal.	16.50	C	77	E
G1012D	Hydrogen Peroxide	Liter	9.50	C	77	E
G1013D	Trichlorethylene	Liter	2.03	C	77	E
G1014D	Methanol	Liter	1.13	C	77	E
D2032D	Compressed Air	Cu.Ft.	0.00063	E	77	C

Table 3. Process costs of Nickel Plating Process

	1986	1975
Equipment	0.054	0.028
Floor space	0.054	0.028
Labor	0.429	0.224
Materials	3.730	1.945
Utility	0.196	0.102
TOTAL	4.462	2.327

The Process Cost per unit peak watt:

5.90 cents/watt in 1986 dollars

3.08 cents/watt in 1975 dollars

for this calculation. The results of the calculations are tabulated in Table 3. The predominant cost factor is the material cost which accounts for 84% of the total processing cost.

The total process cost of 3 cents/watt in 1975 cents is a resonable value which meets the LSA pricing goals of 1986. If the nickel plating equipment is fully automated, the resulting price reduction is expected to be extremely small since the labor costs for this process were not the predominant cost factor.

C. Cumulative Summary of SAMICS Results

A cumulative summary of the process costs which have been obtained up to and including this report is presented in this section. The selected process steps which are used in the CELLCO company are defined as follows:

1. Wafer Surface Preparation (WFSURPR)

Sensor Technology's system was modified to a conceptual automated production line which includes:

(a) Wafer surface cleaning

(b) Surface texturizing

(c) Final cleaning and drying

2. Junction Formation (JUNCF)

This process procedure consists of the application of spray-on-dopants onto the front and back wafer surfaces and the subsequent dopant drive-in. The junction formation process consists of the following steps:

(a) Spray-on N^+ and bake-in.

(b) Spray-on P^+ on back surface and bake-in.

(c) Drive-in procedure with conveyorized oven.

3. Front Surface Pattern Printing (FSPP)

This process will print a negative pattern on the wafer surface, followed by a bake-in.

4. Electroless Nickel Plating (ELNIPL)

Sensor Technology's newly devised plating system will be utilized in this process.

5. Resist Removal (RESMOV)

The wet chemical resist removal method was chosen because it is more economical in relation to the plasma etching method. Sensor Technology's wet chemical method will be modified for the conceptual automation line.

6. Hexagon Laserscribing (HEXLS)

The conceptual automated line (series model) is treated in this process cost study.

7. Solder Flow on Grid Lines (SOFLW)

The conventional dipping method will be used in this process study. The process steps include:

(a) Preheating

(b) Dipping

(c) Flux cleaning

8. A.R.Coating (ARCT)

LFE's automatic plasma deposition method has been chosen for this process.

9. Cell Testing (CELTEST)

A newly-developed testing system will be utilized in this process, which includes:

(a) Testing

(b) Data acquisition and storage

(c) Data analyzer

(d) Grouping mechanism

10. Packing the Cell (PKCELL)

The grouped solar cells are packed and then

loaded into a shipping cassette.

The cumulative process cost summary is presented in Table 4. Four process steps have not been completed, however if these process steps are each assumed to be 1 cent/watt, the total process cost at CELLCO will be 21.37 cents/watt. According to the 1986 price guidelines set by the LSA project, the process cost in CELLCO must be 18.7 cents/watt in 1975 dollars which means that the anticipated overall process cost of 21.31 cents/watt is slightly in excess of the 1986 pricing goals. This price discrepancy could easily be resolved if the hexagonal scribing process did not include the central hole operation. The cost of hexagonal scribing will be reduced by a factor of three if the central hole operation is omitted which implies that this process cost will be in the vicinity of 4 cents/watt.

The final cost analysis for the selected process sequence is expected to be completed during the following month.

TABLE 4. SAMICS CELLCO Process Cost Summary in 1975 cents per Peak Watt

Process No.	Process Referent	Process Cost	Reference
1	WFSURPR	1.55	4th quarterly
2	JUNF	1.53	4th quarterly
3	FSPP	1.07	3rd quarterly
4	ELNIPL	3.08	4th quarterly
5	RESMOV	--	not completed
6	HEXLS	5.36	3rd quarterly
7	SOFLW	--	not completed
8	ARCT	4.78	3rd quarterly
9	CELTEST	--	not completed
10	PKCELL	--	not completed

CONCLUSIONS AND RECOMMENDATIONS

The work performed on Phase 2 of the Array Automated Assembly Program during this quarter had led to a number of conclusions and recommendations:

Costs can be reduced from 6.39 cents per peak watt to 1.55 cents per peak watt (1975 cents) in the wafer surface preparation task by reducing the amount of chemicals utilized to clean the silicon wafers.

Low-cost laser scanning equipment was investigated and found to be suitable for large scale production. The only problem area foreseen at the present moment is the detection of hidden cracks such as poor solder contacts or floating material. A tentative solution to this dilemma would be to alter the orientation of the laser beam from normal incidence to non-normal incidence and also to decrease the laser beam width. It is recommended that an investigation be performed regarding the technological feasibility of the proposed recommendations.

An optimization study of the wafer plating process established the feasibility of reducing the material consumption rate without sacrificing the plating performance. As a direct consequence of the

reduction in the material consumption rate, the total process cost has been reduced to 3.08 cents per peak watt (1975 cents) which conforms to the price guidelines of the LSA project.

It was concluded in the solder coating and flux removal task that the optimum temperature range for solder coating uniformity for wafers in a teflon cassette was 500 to 550°F. It is recommended that three areas regarding this task be investigated. They are (1) use of a wafer pre-heater, (2) flux dipping to enhance solder uniformity and thickness, and (3) use of air blowing to enhance solder uniformity and thickness upon cassette removal.

The laser trimming and holing automation task was found to be by far the most expensive cell processing step at 5.36 cents per peak watt in 1975 cents. Since approximately 90% of the total process cost resides in utility costs alone, a reduction in the overall process cost can occur only with an improvement in laser beam efficiency. It was found, however, that the cost of the laser-scribing process could be reduced by a factor of

three if the central hole operation was omitted. It is recommended that an indepth cost/benefit analysis be performed in the future with respect to cell efficiency, cell inter-connection, and module assembly to establish due cause for keeping or eliminating the wafer holing operation.

A cumulative summary of SAMICS results to date indicates that the 1986 LSA goals for CELLCO can be achieved. The preliminary results show a cost of 21.37 cents per peak watt in 1975 cents as compared with 18.7 cents per peak watt LSA goal for CELLCO. A further cost reduction by about 4 cents to achieve a total cost well below the 18.7 cents per peak watt could be made by eliminating the laser holing operation as discussed above. It is recommended that additional work be performed to investigate this potential area for cost reduction.