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Axiomatix

Marina del Rey • California

SHUTTLE ORBITER S-BAND COMMUNICATIONS EQUIPMENT DESIGN EVALUATION

FINAL REPORT

Contract No. NAS 9-15514A

Prepared for

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1.0 EXECUTIVE SUMMARY

1.1 Purpose of Effort and Degree of Performance

The overall objective of the effort has been to critique the design and assess the performance of the Orbiter S-band communication equipment. The work has three principal aspects/goals:

(1) Review and analysis of the ability of the various subsystem avionic equipment designs to interface with, and operate on, signals from/to adjoining equipment.

(2) Assessment of the performance peculiarities of the hardware against the overall specified system requirements.

(3) Evaluation of EMC/EMI test results of the various equipment with respect to the possibility of mutual interference.

All objectives were attained to various degrees. Due to the long-term nature of the hardware development activity (several years), the first two goals were given the greatest attention during CY78.

The contract statement of work calls out the following tasks:

Task #1 - S-band Network Equipment Design Evaluation
Task #2 - S-band Payload Equipment Design Evaluation
Task #3 - S-band System Electromagnetic Compatibility.

During the contract period, the greatest effort was devoted to Task #2, as the payload equipment was in its conceptual design and early development phases. The degree of results produced with respect to Tasks #1 and #3 are directly proportional to design and test data made available by the network hardware contractor, TRW. Additional testing by TRW, Rockwell, and NASA is needed before full evaluations are possible.

1.2 General Approach to the Activity

The general approach has been to work with cognizant NASA personnel and individuals at the principal prime contractor (Rockwell International) and equipment subcontractor (TRW) to ascertain directions taken. A vital part of this activity has involved Axiomatix attendance and participation in the regular monthly program reviews, as well as all special meetings, at TRW. These latter gatherings usually involved detailed

discussions on design and specification issues that surfaced at the regular monthly reviews.

Each month, Axiomatix prepared a Monthly Technical Report which contained a brief summary of all relevant technical activity, including design reviews, technical conferences, design and analysis efforts and results, critical problem areas, and a forecast of effort for the next monthly reporting period.

Apart from attendance at meetings, monthly reporting, and analysis activities, Axiomatix also acted in a technical consulting role to both NASA and the contractors. Most of the in-depth discussions were conducted at TRW or with various engineers over the phone.

1.3 Contents of the Final Report

This report provides information on all activities with which Axiomatix was involved during CY78.

Section 2.0 is an expanded introduction which addresses the in-depth nature of the tasks and indicates the continuity of the reported effort and results with previous work and related contracts.

Section 3.0 contains functional descriptions of the various S-band equipment. This material is included in this report as a primer for those readers not routinely familiar with the equipment. As such the texts are simply summaries of the principal operating functions/capabilities of each subsystem. Functional block diagrams are provided.

Section 4.0 summarizes the year's history and highlights of the monthly reviews and meetings. Charts and tables are used to depict the important issues, problem solutions are stated, and open or continuing actions are outlined.

In Section 5.0, specific supporting Axiomatix studies and analysis are presented. Some of this work is finished while other parts are ongoing.

Section 6.0 contains design and performance assessments of the principal S-band hardware subsystems. None of the results and conclusions are final; those for the Network Transponder are based upon prototype and flight hardware performance testing while, for the payload supporting equipment, they are taken from the preliminary designs and limited breadboard tests.

Finally, Section 7.0 addresses the expected future activity and

provides some recommendations with respect to second-generation hardware designs.

1.4 Principal Activities, Studies, Results, and Assessments

By virtue of the monthly review meetings and other dicussions held at TRW, Axiomatix had considerable involvement with a number of major issues and problems. Table 1 summarizes the major issues and problems by addressing their nature and the effort expended by all concerned (TRW, Rockwell, NASA and Axiomatix) toward their resolution.

Axiomatix also performed seven detailed studies in support of the design of the payload-related avionic equipment and the performance evaluation of the S-band network hardware. The study titles are:

PI Receiver Triplexer Evaluations
PI Receiver Interference Levels
PI Receiver False Lock Avoidance
PI Receiver Wideband Output Highpass Characteristics
Costas Loop Acquisition Characteristics
Network Transponder Interference Susceptibility
Costas Loop False Lock Margin

With respect to the payload S-band hardware, CY78 saw PI and PSP conceptual designs, trade-off studies, specification detailing and issue resolution, some breadboard testing, and preliminary production engineering. Because work on these subsystems was constrained due to FY78 funds limitation and a need to divert manpower to the network hardware production and testing problems, the designs will not reach the full preliminary development stage until about mid-CY79. A number of significant design and performance problems await solution. A growing concern of Axiomatix is the degree to which most of the PI circuits have been carried to the production design stage while, at the same time, significant conceptual and basic design problems still exist. There is little flexibility in the production configuration to accommodate any necessary extensive redesign and, especially, there is virtually no room within the overall PI hardware package to accept additional circuits that may prove necessary. If this trend continues well into CY79 (the PDR is not scheduled until September) and if extensive changes prove necessary, the schedule could

be affected and costs increased. It is therefore recommended that an interim review of the open design problems and issues be held early in 1979 so that a total understanding of the problems will be obtained and a firm approach for their solution can be implemented.

Summing up the S-band network hardware efforts during CY78, the bulk of the activity was concerned with flight hardware production, testing, and performance troubleshooting. It was generally concluded by Axiomatix that the network hardware performs well and, in most cases, within specification. Some hardware design deficiencies exist within a few of the Network Transponder and FM Transmitter circuits; however, they appear to be correctable through minor redesign and detailed test procedures. Also, a review of TRW's EMI and EMC test data has led Axiomatix to conclude that no serious problems exist which might lead to significant system performance degradation.

1.5 Continuing Effort

Axiomatix will continue to support the overall S-band system developments and, in particular, all activities associated with the development of the S-band avionic hardware. During CY79, this effort will include:

(1) Evaluation of the S-band network hardware verification testing plans and results.

(2) Continuing review and resolution of payload hardware specification issues.

(3) Providing support to the payload hardware development at TRW.

(4) Working with all concerned agencies (principally, NASA, RI, and TRW) to solve design and operational problems in a timely, efficient, low-cost manner.

Table 1. Major Issue Summary

Issue	Issue Nature	Effort Toward Resolution	Resolution
PI Receiver Wideband Output Regulation	1. Incompatibility between PI and KuSP specifications 2. Proposed PI RMS AGC regulator does not optimize FM bent-pipe link performance	1. Assess bent-pipe performance using various types of regulation characteristics (Axiomatix) 2. Propose a signal peak regulation circuit (Axiomatix)	Change PI output to KuSP to be unregulated (no AGC). Place regulation circuit in KuSP (NASA and Rockwell)
PI Modulation Index Limits	1. Undetermined PI receiver performance for payload subcarrier modulation index larger than 1 radian 2. Undetermined PI receiver performance for two or more payload subcarriers	Complete parametric analysis of the PI carrier and subcarrier levels as a function of modulation index and waveform types (Axiomatix)	Results of analysis made known to TRW (Axiomatix)
PI Triplexer Design	1. Required filter characteristics 2. Maximum insertion loss allowable 3. Switch contact degradation	1. Design specification prepared (TRW) 2. Resolution of design details (TRW and Rockwell) 3. Assessment of proposed design (Axiomatix)	Subcontractor design proposal and engineering data (Transco)
PI Interference Susceptibility	Rockwell specification that the PI receiver should work with an in-band interference signal level as large as -25 dBm	Analysis showed that, with the expected receiver first LO noise characteristics, only a -65 dBm interference signal level can be tolerated (TRW and Axiomatix)	Specification amended to the -65 dBm signal level (Rockwell)
PI False Lock Susceptibility	1. PI receiver false lock discrimination with respect to standard and nonstandard payload modulations 2. Degree to which basic PI design should be augmented to include anti-false lock circuits	1. Analysis of PI susceptibility to standard modulations (TRW) 2. Survey of anti-false lock methods (TRW and Axiomatix) 3. Analysis of strong signal phase demodulation discriminator (TRW and Axiomatix)	In-process. Only protection against standard modulations will be considered. Methods still under review

Table 1 (continued)

Issue	Issue Nature	Effort Toward Resolution	Resolution
PI Input Sensitivities Ranges	Exact requirement of Rockwell specification on three receiver sensitivity levels needed further definition	1. Meet the requirement by the use RF signal level limiting (TRW) 2. Use manual signal level attenuators (TRW and NASA)	Manual attenuator approach selected. Preamplifier overload will not cause damage
PI Transmitter Phase Noise	1. Incomplete specification on transmitter phase noise with respect to DSN payloads 2. Possible excessive phase noise due to TRW frequency synthesizer	1. Analysis of synthesizer phase noise (TRW) 2. Phase noise measurements of synthesizer breadboard (TRW)	In process. Preliminary measurements show phase noise to be within spec
PI Wideband Output HPF	The PI wideband output to all interfaces is AC coupled. For nonstandard modulations (e.g., NRZ and no subcarrier) excessive waveform distortion may result	1. Establishment of nonstandard NRZ lower data rate limits (Axiomatix) 2. Analysis of HPF effects (Axiomatix)	Current TRW design acceptable but close to marginal. Recommended changes suggested (Axiomatix)
PI Receiver Preacquisition AGC	Receiver has no AGC prior to tracking state. This results in IF amplifier clipping (saturation). Receiver acquisition performance could be unpredictable or degraded	Recommend the use of noncoherent AGC (Axiomatix)	Open issue. Solution tied in with false lock problem
PSP Tracking Loop Design	Acquisition performance of a Costas loop of the polarity type (in-phase arm limiter) is unknown	Analysis and results for acquisition behavior (Axiomatix)	Analysis and results supplied to TRW

Table 1 (continued)

Issue	Issue Natu	Effort Toward Resolution	Resolution
PSP Data Transition Characteristics	1. Lack of consideration in PSP design for data formats 2. Unspecified transition requirements for minimum performance	1. Evolving TRW design has incorporated provisions for formats 2. Transition characteristics require definition by NASA/ Rockwell	Use NASA Data Standards
PSP Performance Losses	Overall PSP degradation is specified at 1.5 dB. No partitioning between subcarrier loop and bit synchronizer is given	1. Analysis indicates subcarrier loop will contribute majority of loss (TRW) 2. Bit synchronizer performance will depend on data transition density (Axiomatix)	In process
Network Transponder EMI Testing	Concern that electromagnetic radiation apart from nominal transponder output could affect either the PI or payload receivers	Review of TRW Engineering Model EMC tests (Axiomatix)	No apparent problem exists. Radiated emissions are within specification
Network Transponder False Lock	Network transponder receiver indicates lock for conditions which should not produce an in-lock state	1. Parametric set of tests (TRW) 2. Effect and cause analysis (TRW)	Apparently no true false lock occurs. The lock detector has some fundamental design limitations. The problem was solved through some design modifications
Network Transponder Critical 2nd IF Module	Second IF module very difficult to align to maximum performance specifications	1. Tight manufacturing parts screening (TRW) 2. Some specification relief (TRW/Rockwell) 3. Consideration of redesign (TRW)	Open issue. Redesign appears unnecessary

Table 1 (continued)

Issue	Issue Nature	Effort Toward Resolution	Resolution
Network Transponder BER Degradation	Network transponder acts to excessively degrade throughput signal, as measured by BER, when operating in duplex mode	1. Experimental observations (TRW and NASA) 2. Possible degradation models proposed (TRW)	Open issue
FM Transmitter Frequency Drift	All production units have a significant upward frequency drift over a protracted period of time	1. Experimental investigations (TRW and Teledyne Electronics) 2. Analysis of temperature compensating circuits (TRW) 3. Review manufacturing operations (TRW)	Open issue. Possible solution in 48-hour vacuum bake followed by 100-hour burn-in

2.0 INTRODUCTION

2.1 Statement of Work

2.1.1 Objectives

The overall objective of the effort has been to critique the design and assess the performance of the Orbiter S-band communication equipment. The work has three principal aspects/goals:

(1) Review and analysis of the ability of tne various subsystem avionic equipment designs to interface with, and operate on, signals from/to adjoining equipments.

(2) Assessment of the performance peculiarities of the hardware against the overall specified system requirements.

(3) Evaluation of EMC/EMI test results of the various equipments with respect to the possibility of mutual interference.

All objectives were attained to various degrees. Due to the long-term nature of the hardware development activity (several years), the first two goals were given the greatest attention during CY78.

2.1.2 Stipulated Tasks

The contract statement of work calls out the following tasks:

"Task #1 - S-band Network Equipment Design Evaluation - The contractor shall evaluate the design baselined by the S-band system vendor for the S-band network communications equipment, assess the ability of this design to meet NASA's requirements, and report on the results of this assessment. This assessment shall include, but is not limited to, the effects of environment, aging, and manufacturing tolerance on the following performance areas:

1. Uplink bit error rate
2. Uplink carrier acquisition times
3. Uplink carrier tracking performance
4. Uplink spread spectrum acquisition time
5. Uplink spread spectrum tracking performance
6. Downlink transmitted power

The contractor shall identify areas expected to require adjustment or maintenance during the expected 10-year life of the S-band network equpment."

"Task #2 - S-band Payload Equipment Design Evaluation - The contractor shall review the conceptual design and breadboard design of the S-band payload communications equipment as they develop,

assess the ability of these designs to meet NASA's requirements, and report on the results of this assessment. This review shall include, but is not limited to, the following areas:

1. Transmitter phase noise
2. Receiver carrier tracking loop performance
3. Compatibility with existing payload transponder designs

The contractor shall recommend possible design changes for parameter optimization in critical areas."

"Task #3 - S-band System Electromagnetic Compatibility - The contractor shall evaluate areas of possible electromagnetic interference involving the S-band equipment. Performance degradation or operational constraints expected to result from electromagnetic interference shall be defined. The contractor shall recommend and evaluate possible design changes to reduce problems with electromagnetic interference."

During the contract period, the greatest effort was devoted to Task #2, as the payload equipment was in its conceptual design and early development phases. The degree of results produce with respect to Tasks #1 and #3 are directly proportional to design and test data made available by the network hardware contractor, TRW. Additional testing by TRW, Rockwell, and NASA is needed before full evaluations are possible.

2.1.3 General Approach

The general approach has been to work with cognizant NASA personnel and individuals at the principal prime contractor (Rockwell International) and equipment subcontractor (TRW) to ascertain directions taken. A vital part of this activity has involved Axiomatix attendance and participation in the regular monthly program reviews, as well as all special meetings, at TRW. These latter gatherings usually involved detailed discussions on design and specification issues that surfaced at the regular monthly reviews.

Each month, Axiomatix prepared a Monthly Technical Report which contained a brief summary of all relevant technical activity, including design reviews, technical conferences, design and analysis efforts and results, critical problem areas, and a forecast of effort for the next monthly reporting period. Many of the Axiomatix in-process analysis activities and results were appended to these Reports.

Apart from attendance at meetings, monthly reporting, and analysis activities, Axiomatix also acted in a technical consulting role to both

NASA and the contractors. Most of the in-depth discussions were conducted at TRW or with various engineers over the phone.

2.1.4 Continuity with Previous Work

The subject contract effort was new for CY78. However, previous activity, especially that associated with the network equipment, was carried out under contracts NAS 9-14614C, "Study to Investigate and Evaluate Means of Optimizing the Communications Functions," and NAS 9-13467, "Integrated Source and Channel Encoded Digital Communication System Design Study."

2.1.5 Relationship to Parallel Work

The work performed under the subject contract was strongly interrelated to parallel efforts. Contract NAS 9-15240D, "Shuttle Payload S-Band Communications Study," forms the system framework which ties the various payload-related equipments together. Under contract NAS 9-15604B, a handbook, entitled "Users' Handbook for Payload-Shuttle Data Communication," was produced; it includes much of the S-band system hardware details that were produced as a part of the subject contract. Finally, the report "Guidelines for Choosing and Evaluating Payload RF Frequencies," produced under contract NAS 9-15604, was also related to this effort.

2.2 Scope of the Final Report

There are four sections following which address various aspects and details of the work.

Section 3.0 contains functional descriptions of the various S-band equipments. This section is primarily intended for orientation of the reader.

Section 4.0 summarizes the year history and highlights of the monthly reviews and meetings. Charts and tables are used to depict the important issues, problem solutions are stated, and open or continuing actions are outlined.

In Section 5.0, specific supporting Axiomatix studies and analysis are presented. Some of this work is finished, while other parts are ongoing.

Finally, in Section 6.0, design and performance assessments of the principal S-band hardware subsystems are given. None of the results

and conclusions are final; those for the Network Transponder are based upon prototype and flight hardware performance testing while, for the payload supporting equipment, they are taken from the preliminary designs and limited breadboard tests.

3.0 BRIEF DESCRIPTIONS OF THE PRINCIPAL AVIONIC EQUIPMENT

The following subsections are functional descriptions of the Orbiter avionic subsystems with which this contract has dealt (at least in some sense) over the past year.

This material is included in this report as a primer for those readers not routinely familiar with the equipments. As such, the texts are simply summaries of the principal operating functions/capabilities of each subsystem. Functional block diagrams are provided.

3.1 S-Band Network Transponder

A functional network transponder block diagram is shown in Figure 1. The received signal, processed through the preamplifier in the TDRS mode or through the transponder triplexer receive filter (high or low) in the SGLS or STDN direct link modes, is amplified by a low-noise S-band input amplifier prior to down-conversion to approximately 240 MHz. A second coherent down-conversion brings the signal to 31 MHz where, in the TDRS mode, depsreading is accomplished by the spread spectrum processor which uses a noncoherent code search loop. The TDRS despread signal is routed to the carrier Costas loop used to derive phase tracking information. In the SGLS and STDN modes, the Costas loop configuration is also used to track the residual carrier. Demodulation of command and ranging signals is accomplished using an off-line wideband phase detector so that the Costas loop detector predetection bandwidth is optimized for tracking performance. Both tone ranging and data outputs from the receiver are noncoherently AGC'd to maintain a constant rms signal-plus-noise level to the associated subsystems.

All frequencies are derived from two switchable VCXO subassemblies and one reference crystal oscillator. The reference oscillator operates at 31 MHz and thus places the second IF at 31 MHz. This is sufficiently high in frequency to provide good first IF image rejection and still allow the use of narrowband second IF filters. Channel selection is provided by changing the VCXO frequency. Each VCXO subassembly contains four VCXOs for two-channel operation in either the SGLS or STDN/TDRS modes. A simple unique multiplier configuration is used, employing phase-locked oscillators to accomplish the X25 (second LO), X14 or X15 (first LO), and X15 or X16 (transmitter drive) multiplication. By simply changing the

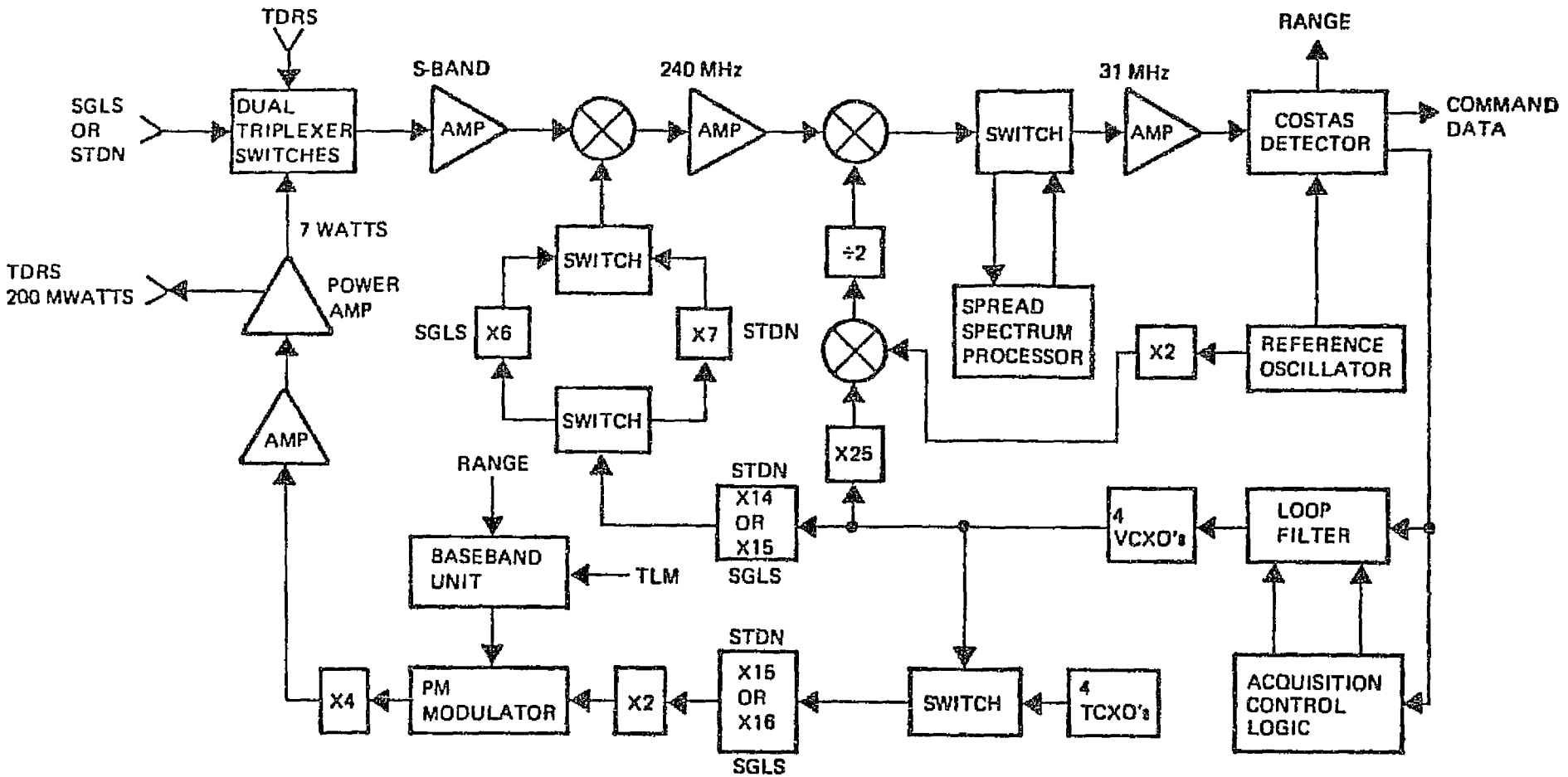


Figure 1. S-Band Network Transponder Block Diagram

divider feedback ratios, the multiplication factor can be changed. This technique provides the wide percentage bandwidth multiplication required for multimode operation while yielding very low spurious products. The final first local oscillator multiplication ratio (X6 or X7) is selected as a function of mode.

The third mixer in the second LO chain offsets the second LO frequency using a 62 MHz reference signal so that the second IF is fixed and does not vary as a function of received frequency. Therefore, the spread spectrum processor and the Costas loop preselection filters operate at the same frequency regardless of input channel selection. The drive frequencies to the third mixer are at twice the first IF and twice the reference oscillator frequency. This eliminates the potential problem of generating a high-level signal at the third mixer exactly equal to the first IF frequency, which could result in a self-lock condition.

Downlink STDN or SGLS linear modulation is accomplished at about 560 MHz, then multiplied by 4 to S-band. An S-band solid-state power amplifier provides a low-level (TDRS) or high-level (STDN/TDRS) output depending on mode selection.

3.2 Network Signal Processor

The block diagram of the Network Signal Processor (NSP) is shown in Figure 2.

The NSP consists of individual forward link, return link, and record mode processing circuits. The three processes operate concurrently, thus providing full duplex operation of the forward and return links in addition to the record mode processing.

Mode controls define the particular data rates, the nature of the data, the need for convolutional encoding and decoding, and the need for voice delta modulating or demodulating. Interface controls define the input data source and the PCM telemetry source.

All input data is introduced through the bit synchronizer, with four input controls identifying the data source, one input control identifying the data rate, and another input control identifying the hard or soft decision. When bit synchronization is achieved, a status bit is provided to the MDM.

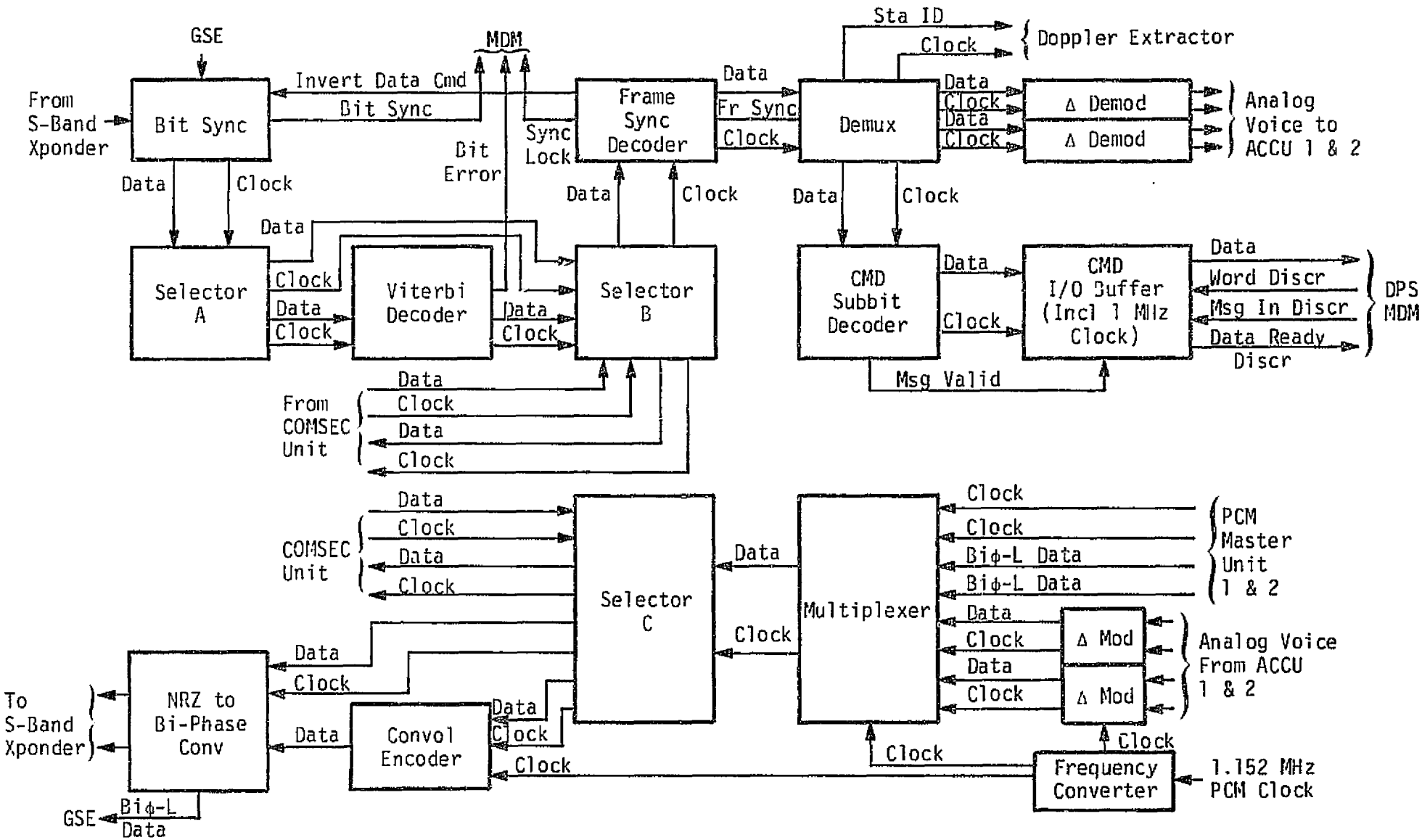


Figure 2. Network Signal Processor Functional Diagram

The bit synchronization data output and the derived clock are delivered to the convolutional decoder through selector A which has data invert control logic. Selector A is where the mode control determines if the convolutional decoder is to be employed. In the coded mode, the convolutional decoder provides its own data inversion capability. At selector B, if the data is identified as DOD data by mode control, it is output to the COMSEC unit and clocked back into the NSP after decryption.

Following detection (and decoding), the data is presented to the frame synchronization logic for frame pattern recognition. Once frame synchronization lock has been achieved, a lock signal informs the MDM of the frame synchronization status. Finally, the forward link function of demultiplexing and rate buffering is performed.

Command data is checked for errors in the BCH decoder, modified appropriately, and stored in a buffer. A message-valid pulse is sent to the MDM for every command word that passes the BCH and vehicle address checks. After ten commands have been received, a signal is sent to the MDM indicating a data-present status. Upon request, 32 16-bit words are sent to an associated subsystem. The first word contains the status of the NSP, words 2 through 31 contain commands, and word 32 contains a bit for each command transmitted, representing the validity of that command.

The return link consists of multiplexing telemetry and voice data. The multiplexing function is keyed to the frame synchronization pattern included with the telemetry data. For DOD data, once the multiplexing function has been performed, the data is routed to the COMSEC equipment for encryption. All data (NASA or DOD) may also be convolutionally encoded as desired. Finally, the coded or uncoded data is NRZ-to-Manchester converted prior to transmission. Return link data is provided simultaneously to the S-band and Ku-band network.

The record mode multiplexes the voice data only with the selected 138 kbps PCM data. In NASA submode 1, the 128 kbps telemetry is multiplexed with the two dedicated voice channels. In NASA submode 2, the 128 kbps telemetry is simply routed to the drivers for transmission to the recorders. In the DOD mode, the recorder data is taken from the return link COMSEC encrypter (effectively bypassing the entire record mode processing logic).

3.3 Payload Interrogator

The function of the Payload Interrogator (PI) is to provide the RF communication link between the Orbiter and detached payloads. For communication with the NASA payloads, the PI operates in conjunction with the Payload Signal Processor (PSP). During DOD missions, the PI is interfaced with the Communication Interface Unit (CIU). Nonstandard (bent-pipe) data received by the PI from either NASA or DOD payloads is delivered to the Ku-Band Processor, where it is processed for transmission to the ground via the Shuttle/TDRSS link.

Simultaneous RF transmission and reception is the primary mode of PI operation with both NASA and DOD payloads. The Orbiter-to-payload link carries the commands, while the payload-to-Orbiter link communicates the telemetry data. In addition to this duplex operation, the PI provides for "transmit only" and "receive only" modes of communication with some payloads.

Figure 3 shows the functional block diagram for the Payload Interrogator. The antenna connects to an input/output RF port which is common to the receiver and the transmitter of the PI unit. Because of a requirement to operate the PI simultaneously with the Shuttle-ground S-band network transponder which radiates and receives on the same frequency bands, a dual triplexer is employed. The S-band network transponder emits a signal at either 2217.5 MHz or 2287.5 MHz; both frequencies thus fall directly into the PI receive band of 2200 MHz to 2300 MHz. Conversely, the payload transmitter, operating either in the 2025-2120 MHz (NASA) or in the 1764-1840 MHz (DOD) bands, can interfere with uplink signal reception by the S-band network transponder receiver. Therefore, by use of the triplexer and by simultaneously operating the PI and network transponder in the mutually exclusive subbands, the interference problem is effectively eliminated.

When detached payloads are in the immediate vicinity of the Orbiter, excessive RF power levels may impinge on the interrogator antenna. Thus, the RF preamplifier of the receiver is protected by a set of manually operated sensitivity control attenuators. The output of the preamplifier is applied to the first mixer, where it is converted to the first IF for amplification and level control. The first local oscillator frequency, f_{LO1}, is tunable, and its frequency corresponds

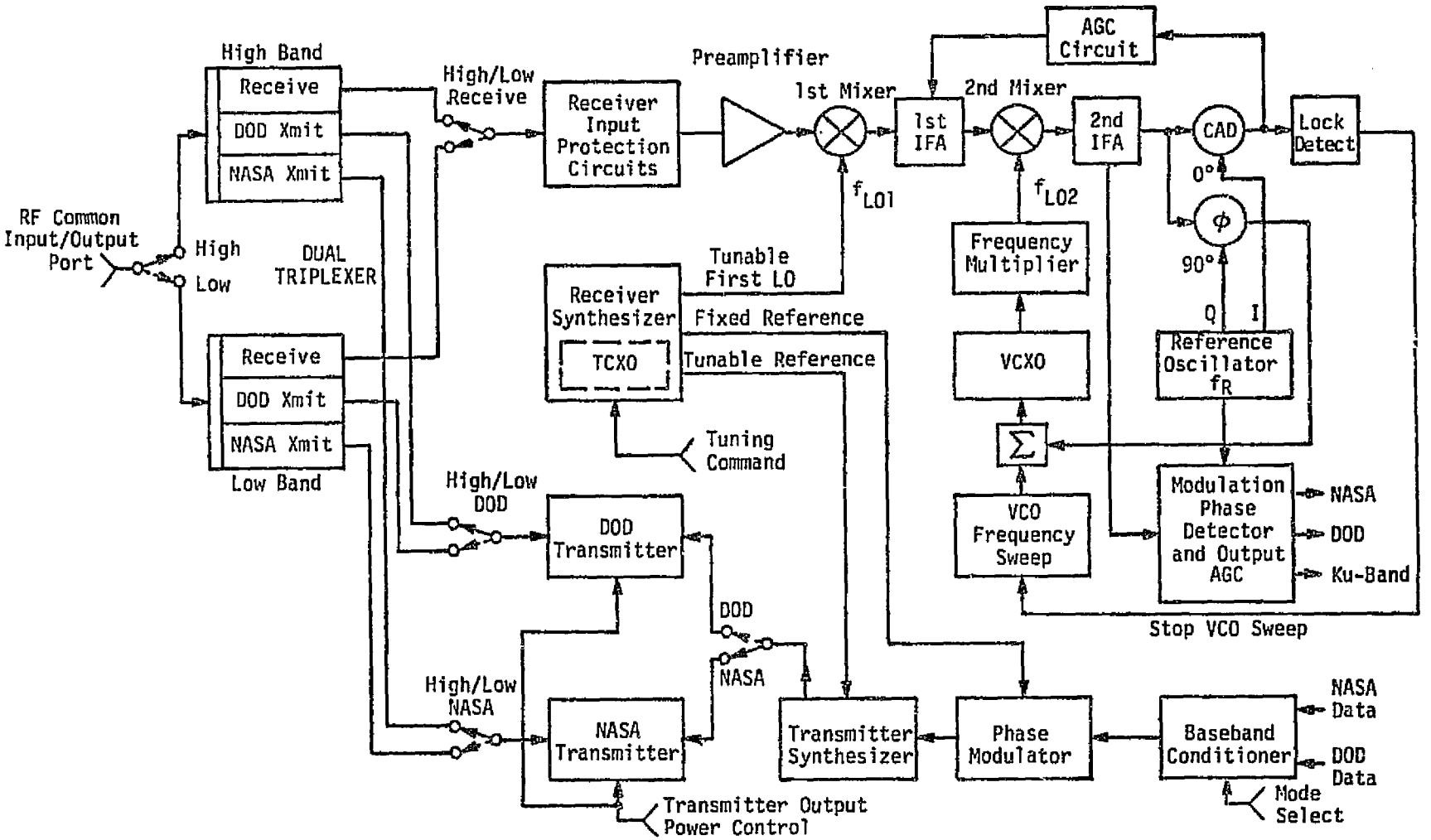


Figure 3. Payload Interrogator Functional Block Diagram

with the desired PI receive channel frequency. Except for channel selection, however, f_{LO1} is fixed. Consequently, any unspecified frequency difference between the received payload signal and f_{LO1} will appear within the first IF amplifier and at the input to the second mixer.

The receiver frequency and phase tracking loop begins at the second mixer. As shown in Figure 3, the output of the first IF amplifier is down-converted to the second IF as a result of mixing with a variable second LO frequency, f_{LO2}. The portion of the second IF which involves only the carrier tracking function is narrowband, passing the received signal residual carrier component and excluding the bulk of the sideband frequencies. Demodulation to baseband of the second IF signal is accomplished by mixing with a reference frequency, f_R. The output of the tracking phase detector, after proper filtering, is applied to the control terminals of a VCO which provides the second local oscillator signal, thereby closing the tracking loop. Thus, when phase track is established, f_{LO2} follows frequency changes of the received payload signal.

For the purpose of frequency acquisition, the f_{LO2} may be swept over a ±75 kHz uncertainty region. Sweep is terminated when the output of the coherent amplitude detector (CAD) exceeds a preset threshold, indicating that the carrier tracking loop has attained lock. The output of the CAD also provides the AGC to the first IF amplifier. To accommodate payload-to-Orbiter received signal level changes due to range variation from about a few feet to 10 nautical miles, 110 dB of AGC is provided in the first IFA.

A wideband phase detector is used to demodulate the telemetry signals from the carrier. The output of this detector is filtered, envelope level controlled, and buffered for delivery to the PSP, CIU and Ku-Band Processor units.

The PI receiver frequency synthesizer provides the tunable first LO frequency and the corresponding exciter frequency to the transmitter synthesizer. It also delivers a reference signal to the transmitter phase modulator. Baseband NASA or DOD command signals modulate the phase of this reference signal which, in turn, is supplied to the transmitter where it is upconverted to either the NASA or DOD transmit frequency and applied to the power amplifiers.

For transmitter efficiency optimization, separate NASA and DOD RF

power amplifier units are used. Depending on the operating band selected, transmitter output is applied to either the high- or low-band triplexer. To compensate for varying distances to payloads, each transmitter has three selectable output power levels.

3.4 Payload Signal Processor

The Payload Signal Processor (PSP) performs the following functions: (1) it modulates NASA payload commands onto a 16 kHz sinusoidal subcarrier and delivers the resultant signal to the PI and the attached payload umbilical, (2) it demodulates the payload telemetry data from the 1.024 MHz subcarrier signal provided by the PI, and (3) it performs bit and frame synchronization of demodulated telemetry data and delivers this data and its clock to the Payload Data Interleaver (PDI).

The PSP also transmits status messages to the Orbiter's general purpose computer (GPC); the status messages allow the GPC to control and configure the PSP and validate command messages prior to transmission.

The functional block diagram for the PSP is shown in Figure 4. The PSP configuration and payload command data are input to the PSP via a bidirectional serial interface. Transfer of data in either direction is initiated by discrete control signals. Data words 20 bits in length (16 information, 1 parity, 3 synchronization) are transferred across the bidirectional interface at a burst rate of 1 Mbps, and the serial words received by the PSP are applied to word validation logic which examines their structure. Failure of the incoming message to pass a validation test results in a request for a repeat of the message from the GPC.

Command data is further processed and validated as to content and the number of command words. The function of the command buffers is to perform data rate conversion from the 1 Mbps bursts to one of the selected standard command rates. Command rate and format are specified through the configuration message control subunit.

From the message buffers, the command bits are fed via the idle pattern selector and generator to the 16 kHz subcarrier biphase modulator. The idle pattern (which, in many cases, consists of alternating "ones" and "zeros") precedes the actual command word and is usually also transmitted in lieu of command messages. Subcarrier modulation is biphase NRZ only.

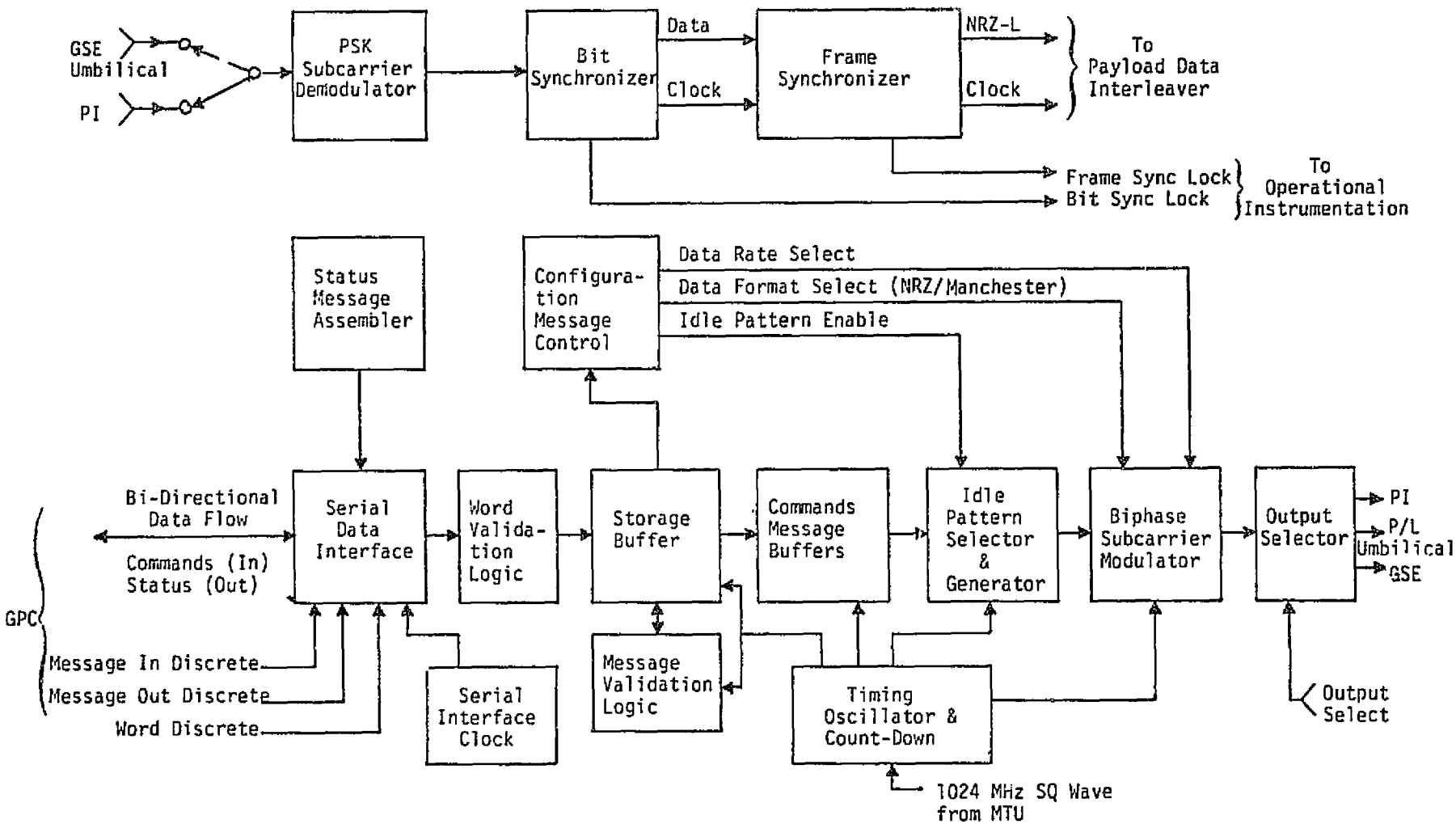


Figure 4. NASA Payload Signal Processor Functional Block Diagram

The 1.024 MHz telemetry subcarrier from the PI is applied to the PSK subcarrier demodulator. Since the subcarrier is biphase modulated, a Costas-type loop is used to lock onto and track the subcarrier. The resulting demodulated bit stream is input to the bit synchronizer subunit, where a DTTL bit synchronization loop provides timing to an integrate-and-dump matched filter which optimally detects and reclocks the telemetry data.

Detected telemetry bits, together with clock, are input to the frame synchronizer where frame synchronization is obtained for any one of the four NASA standard synchronization words. The frame synchronizer also detects and corrects the data polarity ambiguity caused by the PSK demodulator Costas loop.

From the frame synchronizer, the telemetry data with corrected frame synchronization words and clock are fed to the PDI. The telemetry detection units also supply appropriate lock signals to the Orbiter's operational instructional equipment, thus acting to indicate the presence of valid telemetry.

3.5 Ku-Band Signal Processor

The Ku-Band Signal Processor (KuSP) shown in Figure 5 performs the functions of data and signal processing for the Ku-band forward and return links. For the forward link, two modes are available:

(1) A special mode for amplification and impedance matching of data from the Ku-band receiver and communication processor assemblies for delivery to the NSP.

(2) A nominal mode which performs the operations of bit synchronization, clock generation, ambiguity resolution (data and clock), bit detection, frame synchronization, and data decommutation of Ku-band received data.

Return link signals are handled in the KuSP by modulating the data in one of two modes before upconversion to Ku-band frequencies. The two selectable modes multiplex three channels carrying a wide variety of data. In mode 1, the PM mode, the high rate data channel is convolutionally encoded before modulation onto the carrier. The lower rate data channels 1 and 2 are QPSK modulated onto a square-wave subcarrier which is, in turn, PSK modulated in quadrature with channel 3 onto the carrier.

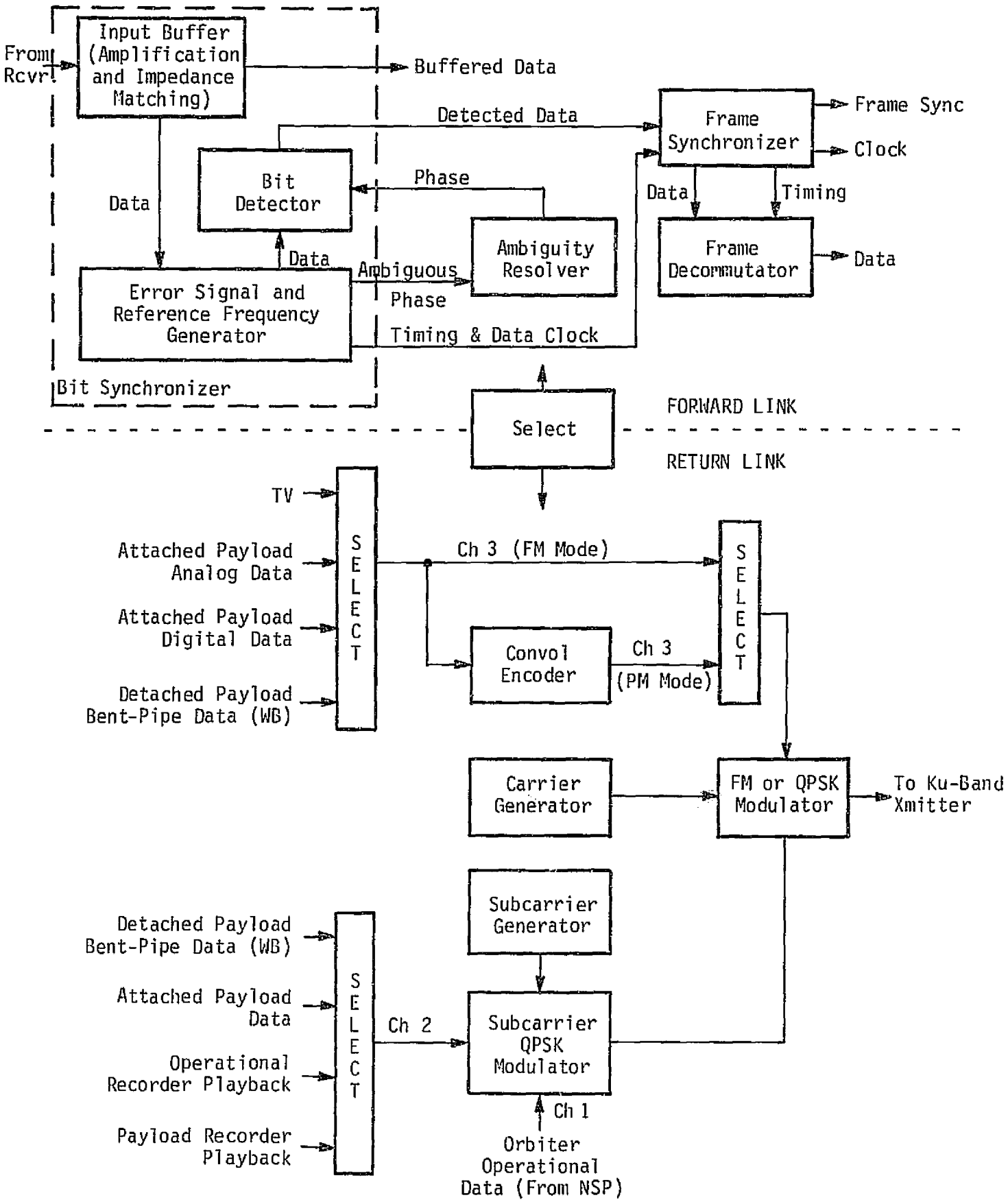


Figure 5. Ku-Band Signal Processor Block Diagram

In mode 2, the FM mode, the two lower rate channels are QPSK modulated onto a square-wave subcarrier as in mode 1. The resulting signal is then summed with the third wideband channel, and the composite signal is then frequency modulated (FM) onto the carrier.

3.6 Typical Payload Transponders

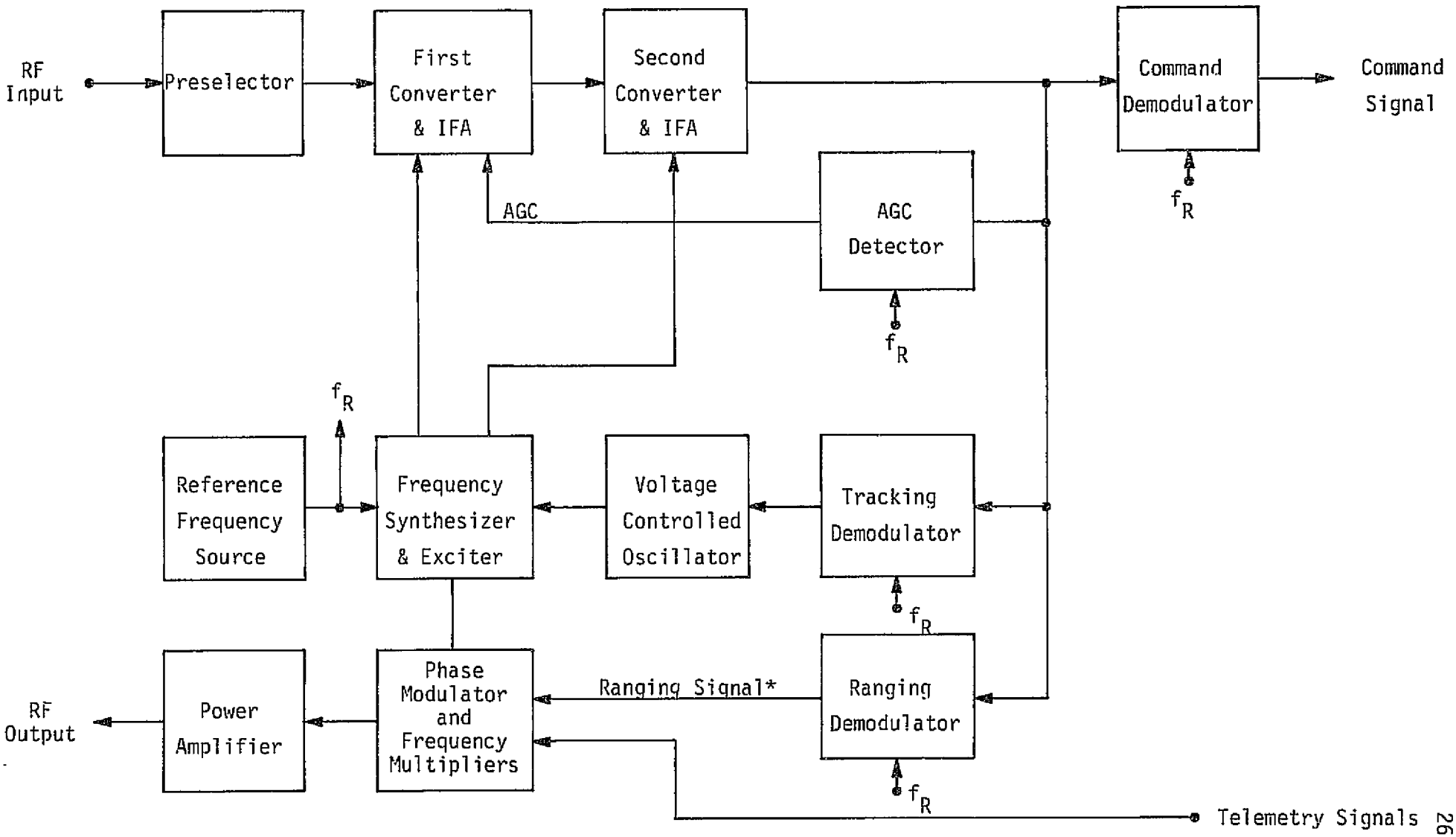
NASA and DOD payload transponders are generically quite similar in terms of their functions and architectures. NASA transponders are standardized, with three mission-oriented types available--deep space transponders [for use with the Deep Space Network (DSN)], near-Earth transponders [for use with the Space Tracking and Data Network Ground stations (GSTDN)], and TDRSS transponders (for use with the TDRSS or GSTDN). DOD transponders interface with the USAF Satellite Control Facility (SCF).

Conspicuous differences between NASA and DOD transponders are the forward link frequency bands and transponding ratios. The NASA receive frequency range is S-band (2025 MHz to 2120 MHz), while the DOD receive frequency range is L-band (1760 MHz to 1840 MHz). The transmitter frequency is related to the receiver frequency by a ratio of integers, called the coherency (or turn-around) ratio. Both the NASA and DOD transmitter frequency ranges are S-band (2200 MHz to 2300 MHz). The corresponding coherency ratios are, for NASA, 240/221 and, for DOD, 256/205.

Figure 6 is a block diagram of the typical payload transponder. The forward link RF input is preselected, filtered for the frequency band utilized [S-band for NASA and L-band for Inertial Upper Stage (IUS) and DOD], and the input is then mixed down to the first IF. Further mixing translates the first IF signal to the second IF, where the output from the second IF amplifier is distributed to four phase detector/demodulator functions.

The carrier tracking loop functions to acquire and track the residual carrier component of the input signal. A second-order tracking loop is employed. Frequency and phase coherence are supplied from the VCO to the synthesizer/exciter where the coherent reference frequencies are derived for the demodulation functions.

AGC is obtained through in-phase demodulation of the residual carrier. The AGC voltage is filtered and applied to the first IF amplifier



*Not used for payload communications with the Shuttle.

Figure 6. Typical Payload Transponder Diagram

to control the gain of the receiver. The AGC voltage is also filtered and compared with a threshold to determine whether the carrier tracking loop is in or out of lock.

The command demodulator coherently recovers the command phase modulation from the carrier. Spectral conditioning (in most cases, limited to lowpass filtering) is usually provided in the output to the command detector.

Most transponders also have a turn-around ranging capability; there is, however, no plan to make use of such ranging capability with the payload/Shuttle link.

The synthesizer/exciter provides all reference frequencies to the transponder. A reference oscillator supplies standard frequencies to the receiver synthesizer, and coherence is provided by the receiver VCO. Synthesized frequencies are distributed to the receiver mixers and phase detectors and to the transmitter phase modulator through a frequency multiplier.

The phase modulator provides the means of modulating the return link carrier with telemetry and ranging signals. Its output drives the transmitter frequency multiplier, producing the required modulated carrier signal in the S-band frequency range.

Finally, the power amplifier raises the modulated S-band transmitter signal to the level required by the return link. For near-Earth spacecraft, the power levels may range from a few hundred milliwatts to several watts, while deep-space vehicles employ power levels on the order of 100 W.

Typical transponder operating and performance parameters are indicated in Table 2.

Table 2. Typical Payload Transponder Characteristics

Item	Parameter and Range
Receive Frequency Range	
L-Band Frequency (DOD)	1760-1840 MHz
S-Band Frequency (NASA)	2025-2120 MHz
Transmitter Frequency Range	2200-2300 MHz
Tracking Loop Bandwidth	18, 60, 200 or 2000 Hz
Tracking Loop Order	Second
AGC Dynamic Range	100 dB
Command Channel Frequency Response	1 kHz to 130 kHz
Ranging Channel Frequency Response	1 kHz to 1.2 MHz
Noise Figure	5 dB to 8 dB
Transmitter Phase Deviation	Up to 2.5 radians
Transmitter Output Power	200 mW to 5W*

*Up to 200 watts with external power amplifiers.

4.0 RESULTS FROM EQUIPMENT CONTRACTOR MONTHLY REVIEWS AND OTHER MEETINGS

The S-band hardware contractor is TRW, Redondo Beach, California, and the principal subsystems they are responsible for designing, fabricating and testing are:

Payload Interrogator (PI)
Payload Signal Processor (PSP)
Network Transponder
Network Signal Processor (NSP)
FM Transmitter
FM Signal Processor.

Each month (with the exception of November), a scheduled program review was held at TRW. Axiomatix was represented at every review. The formal presentations of the hardware development status, schedules and problems usually required one complete day. Often, a second day following was used for splinter meetings wherein technical and specification issues were addressed. The results of the monthly reviews as seen from Axiomatix's perspective and involvement have been summarzied in regular Monthly Technical Reports prepared by Axiomatix.

A number of informal engineering discussions were held between Axiomatix and TRW personnel during the year. The subjects most frequently addressed dealt with various aspects of the evolving PI and PSP designs. The information gained generally formed the basis for, or aided in, the analysis of specific problem areas by both TRW and Axiomatix.

4.1 Summary of Important Issues/Problems and Their Resolution/Status

The following recounts the major issues with which Axiomatix had some degree of involvement and which appeared in the Monthly Technical Reports. Figure 7 portrays the topics in terms of when the issue was first identified, the time periods over wich Axiomatix contributed to the issue resolution or problem solution, and the point in time at which the issue was resolved insofar as Axiomatix's involvement was concerned.

Several general observations are first made with respect to Figure 7. First, the PI and PSP design activities were begun by TRW in January 1978, and this accounts for a large number of issues being raised at that time. Secondly, the PI conceptual design review was held in April and the

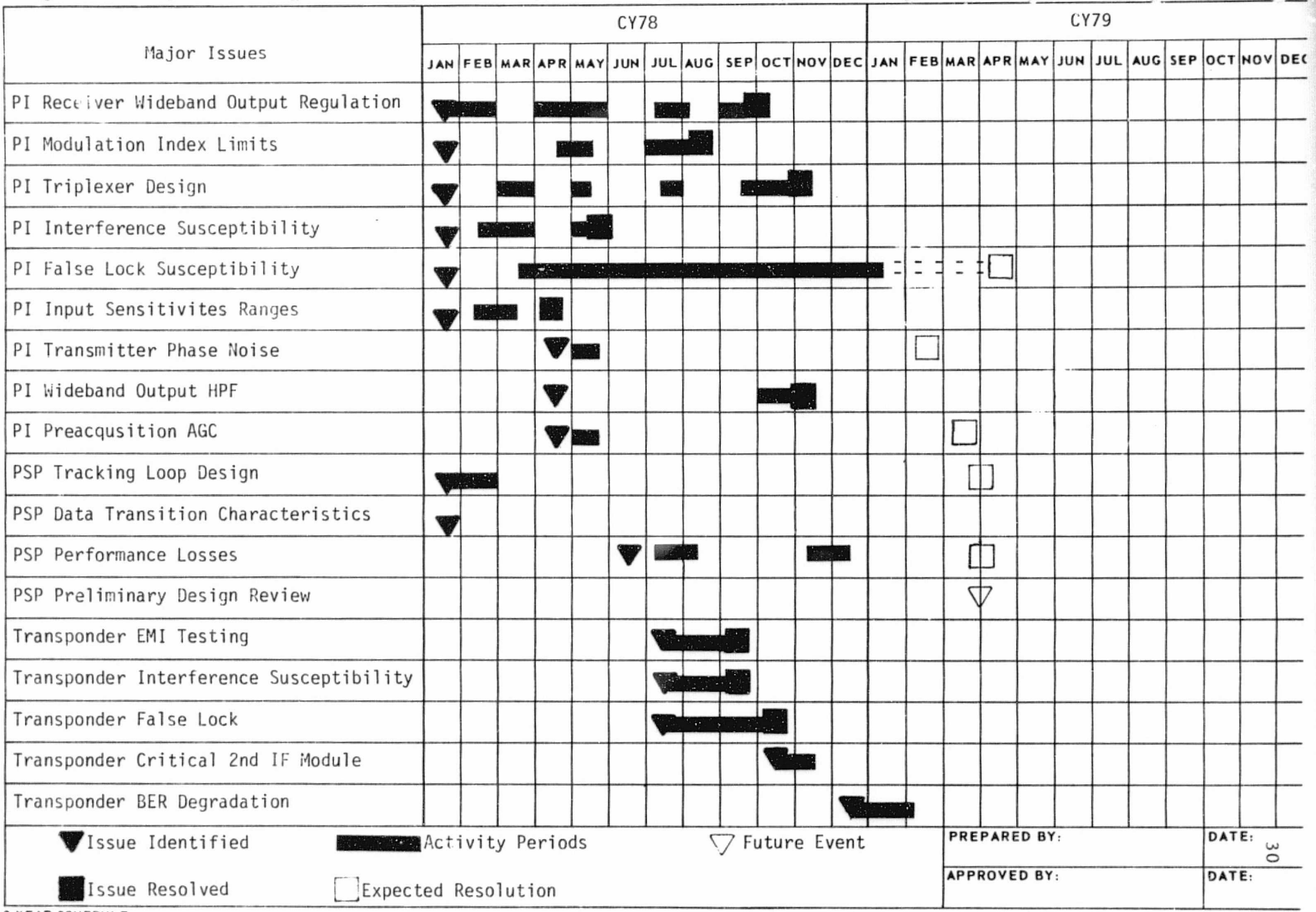


Figure 7. Activity with Respect to Hardware Major Issues/Problems

remaining PI issues were identified at that time. A third point with respect to the payload supporting hardware development is that the total activity was significantly throttled in the late spring months and throughout the summer period due to a combination of FY78 funding limitations and the need by TRW to divert some of the PI and PSP design personnel to problems associated with the production and testing of the network hardware. As an example of the resulting delays, the PSP Preliminary Design Review originally scheduled for June 1978 was postponed several times and is currently set for March 1979. Thus the initial flurry of activity on the PI and PSP at TRW (and, as a result, at Axiomatix on those items which depended upon TRW output) became subdued from June through October and is just now (January 1979) regaining momentum.

A fourth observation made concerning the schedule of issues shown in Figure 7 is that the first half of CY78 was devoted to network hardware production, and the first test results became available in July. Further, the test data was very thin, and continuing production and test equipment problems at TRW's Colorado facility precluded much in-depth testing. As a result, some of the observed test anomalies have yet to be fully evaluated, and resolution will probably not be made until sometime during the first quarter of CY79.

Table 3 summarizes the major issues listed in Figure 7 by addressing the nature of the issue and the effort expended by all concerned (TRW, Rockwell, NASA and Axiomatix) toward its resolution. Details on selected issues appear in subsections 4.2 and 4.3, and the Axiomatix supporting studies and analyses are found in Section 5.0.

4.2 S-Band Payload Equipment Design and Performance

4.2.1 Payload Interrogator

4.2.1.1 PI Receiver Wideband Output Regulation

As indicated by Figure 7, this issue was some nine months under consideration. Its history is as follows:

TRW proposed to employ a "noncoherent rms type" AGC loop to regulate the PI wideband output to 2.0 volts rms. The following problems concerning their initial design were apparent.

(1) The "detector" was not square-law, but tended toward a νth law rectifier with ν on the order of unity.

Table 3. Major Issue Summary

Issue	Issue Nature	Effort Toward Resolution	Resolution
PI Receiver Wideband Output Regulation	1. Incompatibility between PI and KuSP specifications 2. Proposed PI RMS AGC regulator does not optimize FM bent-pipe link performance	1. Assess bent-pipe performance using various types of regulation characteristics (Axiomatix) 2. Propose a signal peak regulation circuit (Axiomatix)	Change PI output to KuSP to be unregulated (no AGC). Place regulation circuit in KuSP (NASA and Rockwell)
PI Modulation Index Limits	1. Undetermined PI receiver performance for payload subcarrier modulation index larger than 1 radian 2. Undetermined PI receiver performance for two or more payload subcarriers	Complete parametric analysis of the PI carrier and subcarrier levels as a function of modulation index and waveform types (Axiomatix)	Results of analysis made known to TRW (Axiomatix)
PI Triplexer Design	1. Required filter characteristics 2. Maximum insertion loss allowable 3. Switch contact degradation	1. Design specification prepared (TRW) 2. Resolution of design details (TRW and Rockwell) 3. Assessment of proposed design (Axiomatix)	Subcontractor design proposal and engineering data (Transco)
PI Interference Susceptibility	Rockwell specification that the PI receiver should work with an in-band interference signal level as large as -25 dBm	Analysis showed that, with the expected receiver first LO noise characteristics, only a -65 dBm interference signal level can be tolerated (TRW and Axiomatix)	Specification amended to the -65 dBm signal level (Rockwell)
PI False Lock Susceptibility	1. PI receiver false lock discrimination with respect to standard and nonstandard payload modulations 2. Degree to which basic PI design should be augmented to include anti-false lock circuits	1. Analysis of PI susceptibility to standard modulations (TRW) 2. Survey of anti-false lock methods (TRW and Axiomatix) 3. Analysis of strong signal phase demodulation discriminator (TRW and Axiomatix)	In-process. Only protection against standard modulations will be considered. Methods still under review

Table 3 (continued)

Issue	Issue Nature	Effort Toward Resolution	Resolution
PI Input Sensitivities Ranges	Exact requirement of Rockwell specification on three receiver sensitivity levels needed further definition	1. Meet the requirement by the use RF signal level limiting (TRW) 2. Use manual signal level attenuators (TRW and NASA)	Manual attenuator approach selected. Preamplifier overload will not cause damage
PI Transmitter Phase Noise	1. Incomplete specification on transmitter phase noise with respect to DSN payloads 2. Possible excessive phase noise due to TRW frequency synthesizer	1. Analysis of synthesizer phase noise (TRW) 2. Phase noise measurements of synthesizer breadboard (TRW)	In process. Preliminary measurements show phase noise to be within spec
PI Wideband Output HPF	The PI wideband output to all interfaces is AC coupled. For nonstandard modulations (e.g., NRZ and no subcarrier) excessive waveform distortion may result	1. Establishment of nonstandard NRZ lower data rate limits (Axiomatix) 2. Analysis of HPF effects (Axiomatix)	Current TRW design acceptable but close to marginal. Recommended changes suggested (Axiomatix)
PI Receiver Preacquisition AGC	Receiver has no AGC prior to tracking state. This results in IF amplifier clipping (saturation). Receiver acquisition performance could be unpredictable or degraded	Recommend the use of noncoherent AGC (Axiomatix)	Open issue. Solution tied in with false lock problem
PSP Tracking Loop Design	Acquisition performance of a Costas loop of the polarity type (in-phase arm limiter) is unknown	Analysis and results for acquisition behavior (Axiomatix)	Analysis and results supplied to TRW

Table 3 (continued)

Issue	Issue Nature	Effort Toward Resolution	Resolution
PSP Data Transition Characteristics	1. Lack of consideration in PSP design for data formats 2. Unspecified transition requirements for minimum performance	1. Evolving TRW design has incorporated provisions for formats 2. Transition characteristics require definition by NASA/Rockwell	Use NASA Data Standards
PSP Performance Losses	Overall PSP degradation is specified at 1.5 dB. No partitioning between subcarrier loop and bit synchronizer is given	1. Analysis indicates subcarrier loop will contribute majority of loss (TRW) 2. Bit synchronizer performance will depend on data transition density (Axiomatix)	In process
Network Transponder EMI Testing	Concern that electromagnetic radiation apart from nominal transponder output could affect either the PI or payload receivers	Review of TRW Engineering Model EMC tests (Axiomatix)	No apparent problem exists. Radiated emissions are within specification
Network Transponder False Lock	Network transponder receiver indicates lock for conditions which should not produce an in-lock state	1. Parametric set of tests (TRW) 2. Effect and cause analysis (TRW)	Apparently no true false lock occurs. The lock detector has some fundamental design limitations. The problem was solved through some design modifications
Network Transponder Critical 2nd IF Module	Second IF module very difficult to align to maximum performance specifications	1. Tight manufacturing parts screening (TRW) 2. Some specification relief (TRW/Rockwell) 3. Consideration of redesign (TRW)	Open issue. Redesign appears unnecessary

Table 3 (continued)

Issue	Issue Nature	Effort Toward Resolution	Resolution
Network Transponder BER Degradation	Network transponder acts to excessively degrade throughput signal, as measured by BER, when operating in duplex mode	1. Experimental observations (TRW and NASA) 2. Possible degradation models proposed (TRW)	Open issue
FM Transmitter Frequency Drift	All production units have a significant upward frequency drift over a protracted period of time	1. Experimental investigations (TRW and Teledyne Electronics) 2. Analysis of temperature compensating circuits (TRW) 3. Review manufacturing operations (TRW)	Open issue. Possible solution in 48-hour vacuum bake followed by 100-hour burn-in

(2) The regulation signal-plus-noise bandwidth was approximately 7 MHz (set by IF filter characteristics), and the postregulation bandwidth was approximately 4.5 MHz.

(3) The AGC loop bandwidth was on the order of 1.5 Hz, which is significantly narrower than the PI coherent AGC loop (≈5 Hz).

Changing from a peak-to-peak type of regulator (as inferred by the Rockwell specification) to an rms-type regulator meant that the peak-to-peak value of the signal input to the Ku-band signal processor's (KuSP) frequency modulator will vary with the PI signal level range (SNR), and with baseband signal type, over a range of at least 3:1. This, it was concluded (by Axiomatix), could prove very detrimental to the Ku-band wideband bent-pipe performance.

Based on these observations, Axiomatix proceeded to analyze the implications of using either a $\nu = 1$ or $\nu = 2$ regulating loop in place of a peak regulating loop. It was initially determined that a penalty as great as 11.5 dB could be paid when $\nu = 1$ and the signal is a lowpass data stream (two-level waveform). Additional analysis which fully accounted for both noise sources in the Ku-band bent-pipe link model showed that a peak-type regulator outperformed the rms-type regulator under all conditions and, for the expected signal forms, would provide a minimum improvement of 1.5 dB. All these results were presented to those concerned (NASA, Rockwell and TRW).

Following several round-table technical discussions, NASA concluded that any necessary signal waveform conditioning required to optimize the Ku-band FM bent-pipe link is properly a function of the KuSP. This conclusion was based upon the fact that attached, as well as detached, payload signals must be regulated and properly scaled within the KuSP. Thus, in order to avoid potential problems with tandem regulator circuits (one in the PI and the other in the KuSP), TRW was requested to revise the PI receiver wideband output design so that the signal interface to the KuSP circumvents the rms AGC circuits. The rms regulator will therefore be used only for the PSP and CIU interfaces. As to whether the regulator within the KuSP should be a peak type, this resolution awaits some experimental evaluations to be conducted by Axiomatix as part of Contract No. NAS 9-15240D.

4.2.1.2 PI Modulation Index Limits

From the beginning of the PI development activity, TRW consistently commented on the fact that the PI carrier tracking loop operation would be TBS for phase deviation β on the range of $1.0 < \beta \leq 2.5$ radians. They further recommended that PI receiver performance be specified only for the range $0.3 \leq \beta \leq 1.0$ radians.

The major problem appeared to be one of interpretation of intent on the part of the PI specification. Rockwell had established the minimum PI residual carrier levels which, in effect, bound the modulation index insofar as carrier suppression is concerned (given maximum range and worst-case performance conditions). The modulation indices for standard 1.024 MHz and 1.7 MHz subcarriers are set at 0.3 or 1.0 radians peak. No specific characteristics were established, however, for nonstandard bent-pipe modulations. All that was specified is:

> "Information (modulations) with indices of up to 2.5 radians will be detected, provided a minimum of -122.5 dBm for acquisition and -124 dBm for tracking residual carrier is present."

This is the proper general way to specify the relationship of modulation index to receiver acquisition and demodulation performance.

The β range ($0.3 < \beta < 2.5$ radians) is, in reality, on the payload transmitter capability, and not on the PI receiver. The receiver need only work with received signals whose characteristics are such that a residual carrier is present with sufficient power. It should also be noted that there may be payload signal formats where three or more subcarriers could simultaneously modulate the transmitter, each with a $\beta < 1.0$ radian but with a combined peak deviation on the order of 2.5 radians (thus the need for the β range specification).

As a result of all these considerations, Axiomatix proceeded to perform an analysis intended to:

(1) Determine PI output component levels for the mixed subcarrier cases.

(2) Show when various combinations of individual bent-pipe signal modulation index violate the residual carrier requirements or otherwise degrade PI performance.

Since this work is S-band system rather than hardware related (the results do not impact the PI design), the effort has been carried out and reported under Contract NAS 9-15240D. (See the Final Report for CY78.)

4.2.1.3 PI Triplexer Design

The payload interrogator will use a dual triplexer between the antenna and the receiver input and transmitter output; its purpose is to prevent interference with other Orbiter communication equipment and to reject image frequency signals plus the usual T/R isolation. This triplexer divides both the transmit and the receive bands of the PI into "low" and "high" regions.

To satisfy all triplexer requirements specified by Rockwell International, the triplexer design must involve a compromise between a low insertion loss and high selectivity. For the transmitter filter section of the triplexer, low loss is important to maximizing the efficiency of the radiated RF power while, for the receiver filter sections, low loss is necessary to minimizing noise figure. High filter selectivity necessary to sharply define the high and low band limits dictates a large number of sections (i.e., transfer function zeros and poles)--a requirement which could lead to relatively large insertion loss.

Both TRW and Axiomatix recognized early the problems of implementing the triplexer. Preliminary analysis by Axiomatix of the specified triplexer selectivity indicated that the requirements for the receive band high and low sections would be the most difficult to meet. For example, a Chebyshev filter characteristic having 0.1 dB of passband ripple could require up to nine sections in each of the high and low band filters. Implementation of this filter with quarter-wavelength cavity resonators results in the lowest insertion loss, estimated at about 0.7 dB. In addition, about 0.5 dB of physical junction losses can be expected, resulting in a total center band insertion loss of about 1.2 dB.

Axiomatix estimated the physical dimensions of such cavity-implemented filters to be about 2 inches by 2 inches by 10-1/2 inches. This was judged an excessive size considering that at least two of these filters are required, and that the other four filters making up the dual triplexer could have dimensions of the same order of magnitude. As a result of this initial assessment, Axiomatix considered the impact of relaxing triplexer specifications on PI receiver performance. Filter simplification and size reduction were also studied. Detailed analysis involved such factors as passband ripple, passband attenuation shape, passband symmetry, and skirt selectivity.

Axiomatix made available a summary of its initial assessment of the triplexer implementation during March. At the April 25-26 design review, TRW presented the results of their triplexer study, which indicated requirements similar to those ascertained by Axiomatix. TRW then prepared a detailed design specification which became the basis for a procurement activity which ultimately selected Transco to design and build the triplexer. During the precontract negotiation period, a number of problems were raised and the specifications were revised.

One concern which arose over the triplexer design was that of switch (relay) contact degradation with time due to "hot switching." Transco test data showed that, at a 4-watt power level, after approximately 50,000 hot switches, contact deterioration might manifest itself as increased insertion loss. While this may not be a problem at the 4-watt level, it would be at the low power milliwatt level. (The implication is that the insertion loss becomes greater at low power levels.) This problem was resolved by a number of actions:

(1) Requirements were added to allow hot switching up to 16 watts power levels on transmit ports only.

(2) TRW designed in a transmit inhibit capability (via the command processor) to inhibit the transmitter output to the triplexer during switching.

(3) The transmitter coaxial switches will be hot-switched only during SRU testing but will not be hot-switched for LRU testing and mission operations. The 4 watts incident on the antenna port should be no problem as the Transco switch was tested at 15 watts for 20,000 cycles and 20 watts for 10,000 cycles with only minor degradation (<0.1 dB).

Axiomatix also raised some questions concerning transmitter power level switching:

(1) Will the power level be switched after the payload's receiver has been acquired and is tracking?

(2) If so, will the combination of

(a) the resulting amplitude transient

(b) the carrier phase step (due to differential circuit path delay/phase-shift), and

(c) the switch-over dead zone time (approximately 50 ms)

be such as to cause the payload receiver to lose lock?

(3) Does the possibility of payload receiver lock-loss and the

the need to institute the reacquisition procedure introduce operational problems in terms of payload deployment? As of the writing of this Final Report, no answers are available. Test data is needed which will likely come only from ESTL system tests. Once available, this information may be used in conjunction with the payload receiver's operating parameters and maximum loop stress conditions to determine the probability of loss-of-lock.

TRW distributed its "final" (before go-ahead on Transco contract) triplexer design specification in September. Since there were a number of variances with respect to the original Rockwell specification, Axiomatix was requested by Rockwell to perform a comparative assessment. This work, which appears in subsection 5.1, concluded:

"An examination and comparison of the TRW and Rockwell specifications for PI triplexer SRU has shown that the TRW specification does not compromise on any critical parameters, and that it is consistent with providing flexibility for the practical design optimization of the triplexer filters."

Axiomatix recommended that Rockwell accept the TRW specification and update the Rockwell design requirements accordingly.

Rockwell subsequently questioned whether 90 dB of attenuation in the transmitter filters over the PI receive frequency range is sufficient. The principal concern is whether transmitter signal sidebands due to high-frequency, large-index modulations (e.g., 200 kHz at 2.0 radians) will be attenuated to a level of less than -50 dBm at the receiver input port. TRW was requested to review the triplexer specification from this point of view and, if it is found to be inadequate, change the triplexer design or add more filtering to the transmitter modulation and drive circuit.

4.2.1.4 PI Interference Susceptibility

An early concern of TRW was that of meeting the Rockwell PI specification concerning receiver in-band interference. The essence of the Rockwell specification was that an interfering signal (of any form) with a power level as high as -25 dBm, and being 10 MHz or more distant from the desired received signal at the minimum signal level, shall cause no more than 1 dB of receiver performance degradation. TRW held that,

because of the need to "tune" the PI receiver over a 100 MHz frequency range, which is accomplished by changing the frequency of the first L.O. over the 100 MHz range, L.O. sideband noise 10 MHz from the L.O. nominal frequency, when mixed with the interfering signal, will produce an equivalent noise level at the receiver frequency which is more than 1 dB greater than the receiver ambient noise level. The problem is that, because of the 100 MHz tuning range, narrow filters cannot be installed within the L.O. circuits to sufficiently attenuate L.O. sideband power at $\pm$10 MHz.

A number of aspects of the receiver design and performance required study to determine whether the Rockwell specification could be met. The specification impacts the triplexer, receiver predetection bandwidths, IF filter characteristics, and the problems of acquisition and interference signal "capture" of the receiver tracking loop. Most specifically, Axiomatix considered the effects of the in-band interference from three perspectives: (1) receiver overload; (2) spurious responses of the first mixer; and (3) increase of ambient noise level due to local oscillator sidebands.

Receiver overload occurs when the desired signal level is at its minimum value, and the receiver's AGC loop has therefore regulated the receiver's gain to its maximum value. Under such a condition, the wideband sections of the receiver may become overloaded with the -25 dBm interference present. To what extent this is a real problem would be dependent upon the characteristics of the TRW receiver design. The second consideration is concerned with intermodulation products generated within the first mixer between the interfering signal and the mixer reference signal, and whether, for example, false lock conditions might ensue. The third problem was the one that most concerned TRW and the one for which they requested a specification change. As a result, Axiomatix and TRW independently analyzed the contribution of the L.O. sidebands to the overall receiver noise level when CW interference was present at a frequency 10 MHz offset from the desired signal. The conclusion of TRW's effort was that the maximum tolerable interference signal level is -65 dBm.* TRW requested that the specification be amended to reduce the interference power level from -25 dBm to -65 dBm, and Rockwell changed the specification to read:

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*This result is inconsistent with a receiver performance degradation of 1 dB. See Subsection 5.2 for Axiomatix's analysis and resolution of the inconsistencies.

> "The presence of a -25 dBm signal level, modulated or unmodulated at any frequency within 200 MHz and 16 GHz, but outside (a) 2276.6 ±50 MHz when in the "high" mode, and (b) 2226 ±50 MHz when in the "low" mode, shall not degrade the receiver performance by more than 1 dB. Within the above cited bands (a) and (b), a -65 dBm signal level, modulated or unmodulated, shall not degrade the receiver performance by more than 1 dB."

Axiomatix also concluded that, at a -65 dBm interference signal level, the problems of receiver overload and first mixer spurious responses would be insignificant and therefore did not pursue the matter further.

4.2.1.5 PI False Lock Susceptibility

This particular subject is probably the one most extensively discussed from month to month. It still awaits final resolution; however, considerable progress has been made.

Rockwell's specification most generally states: "The receiver shall not lock-on to sidebands." TRW's initial asssessment was that they would comply with the false lock specification by "precluding sideband false lock as a design goal." TRW held that there probably would be no problem in meeting the intent of this specification for normal modulations by the 1.024 MHz and 1.7 MHz subcarriers. Their concern was with "bent-pipe" modulations. Since the nature of such "bent-pipe" signals was totally undefined, TRW elected to take no further action until Rockwell/NASA adequately defined the signals.

Subsequent discussions at the monthly review meetings soon established several points of concern:

(1) It was unclear whether "standard" payload modulations might not produce false lock conditions. Analysis was needed.

(2) Definitions of "nonstandard" payload modulation characteristics would be required if the receiver design was to be such as to preclude false lock to "bent-pipe" signals.

(3) Methods for antisideband false lock would require study if such circuits were to be incorporated into the PI receiver.

TRW investigated the potential of PI false lock on the carrier sidebands for "standard" signals (i.e., biphase modulated 1.024 MHz and 1.7 MHz subcarriers). The approach taken was to first calculate the maximum sideband level appearing in a ±100 kHz window* about the carrier

*Receiver frequency sweep acquisition range.

frequency. A determination was then made as to whether the sideband spectral characteristics and power level would be sufficient to cause the tracking loop lock detector to indicate a state of in-lock. Thus, the ability of the PI receiver to preclude false lock would be based upon the operation of the PLL lock detector and its function to inhibit receiver sweep frequency acquisition for relatively small discrete sideband levels compared to that of the true carrier component. (See subsection 5.3.2.) The TRW results showed that the STDN/16 kbps/1.024 MHz mode presented no false lock problems, while the SGLS/128 kbps/1.024 MHz and SGLS/256 kbps/1.7 MHz modes do present a false lock threat. TRW offered some potential solutions:

(1) Employ filtering in the payload transmitter to reduce the sideband level with $\pm$100 kHz about the carrier.

(2) Use noncoherent AGC in the PI to reduce the effective sideband power level as seen at the input to the tracking loop (especially to preclude IF circuit amplitude limiting).

(3) Use a discriminator-based antisideband lock circuit within the carrier tracking loop.

It was quickly concluded that the first solution is impractical as there is no universal mechanism for implementing it. The second solution, however, has considerable merit since the false lock potential created with respect to the standard modulations is a direct function of a lack of receiver preacquisition AGC. The manifestation is IF amplifier amplitude limiting (clipping). Axiomatix has shown (see subsection 6.1.1) that the use of a noncoherent AGC would probably eliminate the false lock threat for the standard modulation case. As of the writing of this report, TRW is further considering this fix.

The concept of employing a discriminator-based antisideband lock circuit as a cure for the standard modulation false lock potential, as well as for undefined bent-pipe signals, resulted in a number of studies by both TRW and Axiomatix. The principal ideas investigated were:

(1) Employ an AFC loop and discriminator-based lock detector in conjunction with the APC loop and coherent lock detector in the PI receiver.

(2) Eliminate receiver swept acquisition in favor of frequency-discriminator centering of the VCO's frequency (basic IUS transponder approach).

(3) Use a noncoherent (discriminator-type) receiver for strong signals, relegating the PI to weak signal conditions only, thus avoiding the strong signal false lock problems.

(4) Determine via ground-based observations whether bent-pipe signals are proper, i.e., whether the PI receiver may be tracking a sideband rather than the carrier, and command the PI into a reacquisition mode if needed.

(5) Employ several receiver swept acquisition frequency sweep rates as a function of received signal level. Faster rates at strong signal levels precludes false lock to sidebands.

Of the above, only (1) and (3) were given in-depth consideration.

Axiomatix surveyed four discriminator antilock circuits that have been used in other receiver designs; see subsection 5.3.3 for details. Additional analyses have been performed* to show how a closed-loop frequency discriminator may be used to decrease PLL false lock sensitivity. From the results, one may make the necessary trade-off between improving acquisition performance (as measured by false lock sensitivity for a given sweep rate) and deteriorating tracking performance (as measured by mean-squared phase jitter due to additive noise). No AFC loop techniques are, however, currently being given serious consideration for implementation within the PI.

Both TRW and Axiomatix have analyzed the use of a discriminator for strong signal phase demodulation. (Subsection 5.3.4. contains the motivation and analysis details.) The results are nearly identical, and the slight differences have the following explanations. Axiomatix calculated the PI receiver false lock region to begin at signal levels greater than -107 dBm, while TRW claims the region begins at -110 dBm. This small difference stems from the analytical models of the receiver used. Axiomatix shows that the discriminator may be successfully employed down to signal levels as low as -93 dBm, while TRW presented -87 dBm as the lower limit. In this case, the Axiomatix figure was obtained using a more exact definition of threshold based upon BER as contrasted to TRW's simpler +10 dB discriminator input SNR criteria. In any event, it is quite clear from both analyses that there is a significant range of received signal levels over which the discriminator will not work, yet the false

*This work appears in the final report for Contract NAS 9-15240D.

lock problem exists. Thus, the discriminator is not a cure-all for the strong signal false lock problem. TRW amended its results with the recommendation that, if a discriminator-based phase demodulation is used for strong signals, the manual sensitivity attenuators that precede the PI input must also be used for moderate signal levels to preclude the likelihood of false lock. Given that the receiver is false lock resistant for standard signals at received levels less than -100 dBm (TRW number), the recommendation may be summarized as:

Signal Level Range	Configuration
Threshold to -100 dBm	Set "sensitivity = high" and use PLL receiver
-100 dBm to -80 dBm	Set "sensitivity = medium" and use PLL receiver
-80 dBm	Use discriminator

It is to be noted, however, that there is no provision which allows the "operator" to know what the received signal level is and, therefore, which operating range to select. Disposition of these results is under study by Rockwell and NASA.

Finally, efforts to define a set of nonstandard modulation characteristics have been nil. Both Rockwell and Axiomatix have made some contributions to the issue (see the final report for Contract NAS 9-15240D), but NASA has the responsibility for producing an official set of requirements. Such requirements must be established from four perspectives:

(1) Modulation waveform types

(2) Modulation spectra

(3) Modulation index

(4) PI acquisition, tracking and demodulation performance.

In summary, the problem of PI receiver false lock is still an open issue. Since the current TRW receiver design has a false lock potential under stated conditions of payload standard modulations, Rockwell has formally requested that TRW investigate what changes/additions are required to preclude false locking. Only automatic (no men in the loop) solutions will be acceptable. As to the false lock threat from nonstandard modulations, Rockwell will formally request that this be studied by TRW only after NASA has completely defined the nonstandard modulation signal set.

4.2.1.6 PI Input Sensitivity Ranges

The Rockwell specification calls for three receiver sensitivity levels or ranges, and the initial TRW approach to meeting the requirement was to use RF limiting circuits (breakdown diodes) at the input to the receiver. Further studies showed, however, that the use of such circuits would significantly increase the receiver noise figure.

The adopted solution was to place manual attenuators prior to the receiver input and to design the preamplifier so that it would tolerate up to +20 dBm of signal level without damage. A flight crew member will set the attenuators according to some operational criteria yet to be defined.

4.2.1.7 PI Transmitter Phase Noise

The PI transmitter S-band output phase noise was initially specified at 4° rms in a 300 Hz test bandwidth. Axiomatix raised the point that this does not necessarily guarantee that a 10° rms error in a 10 Hz test bandwidth will be obtained. This latter requirement stems from the need to properly communicate with DSN-type payload transponders.

TRW has proposed a transmitter frequency synthesizer which employs one TCXO, two VCXOs and two VCOs, all of which interact in generating reference and output frequencies. Two problems were subsequently noted by Axiomatix:

(1) Incomplete performance parameters preclude analysis to predict internal PLL acquisition and tracking characteristics or whether frequency-divider induced noise will be prevalent.

(2) There is no indication whether the S-band phase noise will be sufficiently small to achieve a 10° rms error in a 10 Hz test bandwidth.

TRW, in turn, offered a two-year-old analysis from a previous program for a similar synthesizer which showed that the phase noise should be between 6° rms and 10° rms in a 10 Hz bandwidth. It was concluded, however, that the final assessment would have to await breadboard tests. Such testing, originally scheduled for the summer months of 1978, was delayed due to fiscal year funding problems and manpower diversion. No definitive test results have been produced, as of the writing of this report, which convince Axiomatix that the requirement will be met by the TRW design.

4.2.1.8 PI Wideband Output HPF

TRW proposed that the 3 dB frequency of the wideband output highpass filter (AC coupling) should be 1 kHz. It was Axiomatix's view that, since the highpass 3 dB frequency of the receiver PLL is on the order of 200 Hz, this value would appear to be too high. Axiomatix reviewed this problem, therefore, at Rockwell's request, and made recommended changes. Axiomatix's analysis is found in Subsection 5.4. The conclusion is that the HPF 3 dB frequency should be less than 678 Hz and that a 200 Hz 3 dB frequency would be a safe design.

4.2.2 Payload Signal Processor

4.2.2.1 PSP Tracking Loop Design

TRW's basic approach to the design of the PSP is to utilize a Costas type subcarrier demodulator and a sampled-data, microprocessor-implemented, DTTL bit synchronizer. At the initial conceptual design presentation early in 1978, Axiomatix was concerned that the TRW engineers were not particularly familiar with many of the developments and working implementations of this general configuration and, as a result, might spend significant efforts on performing trade-offs and solving problems that have been previously researched by other organizations. In addition, the following technical problems were noted at that time.

(1) The relationship between the Costas loop arm LPF bandwidth and the ADC sampling rate did not appear proper for all data rates to be processed.

(2) The AGC loop was undefined.

(3) Lock detection (subcarrier and bit synchronizer) was undefined.

(4) The bit synchronizer tracking algorithm appeared to change characteristics as a function of bit rate.

(5) No provision was made for handling biphase formats.

(6) The use of a "baseline direct voltage offset correction" circuit did not appear to be adequately justified.

Axiomatix worked closely with the TRW engineers during the initial period of design detailing. As a result, most of the above problems were quickly dispelled. Certain answers, however, must await breadboard testing which was delayed to the latter part of CY78. Results are just being received as of the writing of this report (see Subsection 6.2).

One problem that Axiomatix analyzed as a result of TRW's expressed concern with the acquisition behavior of "decision-directed"* Costas loop was the true lock acquisition performance of the Costas loop with the in-phase arm hard-limited. (See Subsection 5.5 for analysis details.) The results show that, in the absence of noise, a second-order decision-directed Costas loop, when compared with a second-order conventional Costas loop of equal loop bandwidth, has twice the frequency acquisition range. In the presence of noise, one can account for the suppression effect of the noise on the decision-directed loop's S-curve (noise has no effect on the S-curve of the conventional loop). Neglecting then the statistical effect of the noise in both cases (that is, only accounting for the suppression of the decision-directed loop S-curve due to noise), it is possible to compare the frequency acquisition range of the decision-directed and conventional-type Costas loops as a function of the signal-to-noise ratio. Numerical evaluation of this comparison for various data formats (e.g., NRZ and Manchester) and single-pole arm filters was accomplished. Similar comparisons were made for the frequency acquisition time performance of the two loops. Again, the results indicate that, for the same loop bandwidth, the decision-directed loop is superior.

4.2.2.2 PSP Data Transition Characteristics

The question of minimum data transition density with respect to the PSP bit synchronizer tracking performance was raised from time to time. NASA stated that the existing data standards should be invoked. This, however, leaves the performance undefined with respect to nonstandard (bent-pipe) data streams.

This problem must be considered relative to other portions of the system that also affect low data transition bit patterns. See Subsection 5.4.

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*The phrase "decision-directed" is a TRW designation. It should not be confused with the application of the same phrase to Data-Aided Loops, wherein optimum decisions are made on each data bit interval using a matched filter. The "decision-directed" Costas loop simply employs a hard limiter between the output of the in-phase arm filter and the cross-multiplier (which may, therefore, be mechanized as a chopper). Axiomatix prefers to designate this loop as a "polarity" type Costas loop.

4.3 S-Band Network Equipment Design and Performance

4.3.1 Network Transponder

4.3.1.1 Transponder EMI Testing

In April 1978, TRW made available the results of their EMI tests on the network transponder in a report entitled "Electromagnetic Compatibility (EMC) Evaluation Test Report for the SCTE S-Band Transponder" (TRW Report No. 78-8722.1-14). This report deals with the results of the EMI tests performed on the engineering model of the S-band transponder to determine the degree of compliance with the EMI specification, NASA Document Number SL-E-0002A. The tests were run during February and March 1978.

Axiomatix carefully reviewed the report. Of specific interest to Axiomatix were the results of the radiated emission measurements relative to Specification RE-02. An examination of the test data indicates that, over the region of 1 to 10 GHz, no significant narrowband or broadband interference was detected. This implies that payload receiver communication interference from the network transponder should not be a problem.

4.3.1.2 Transponder Interference Susceptibility

During the latter part of June and the early part of July, TRW conducted a series of tests to determine the susceptibility of the network transponder receiver to an interferer on the out-of-band portions of the 1 GHz to 10 GHz frequency range. The salient parameters of the test conditions were:

Uplink signal level = -100 dBm

Interference signal level = -15 dBm

Interference frequency step increments = 1 kHz

As a result of these tests, two types of responses were observed: (1) degrading spurs with power level on the order of the transponder's thermal noise level and (2) complete loss of lock of the uplink signal.

To assist JSC with an interpretation of the significance of these results, Axiomatix was requested to examine this test data and provide an appropriate evaluation.

The first partial samples of the test data were received from RI/SD about July 10 and were examined, with no serious anomalous behavior being detected. Additional information was obtained during the July 20 monthly

meeting held at TRW. Specifically, TRW presented their interpretation of spur phenomenon and provided an explanation of the adaptive threshold mechanism used for detecting spurs. During the month of August, it was reported that an intermittent transmitter spur ±800 Hz from the carrier had been detected on the engineering model network transponder. Testing disclosed, however, that the spur, perhaps a function of transponder vibration level, does not appear to compromise S-band system performance.

Axiomatix's overall assessment of the network transponder interference susceptibility tests appears in Subsection 5.6.

4.3.1.3 Transponder False Lock

At the May monthly review, TRW presented their findings concerning unexpected false lock states of the network transponder in the nonspread spectrum modes as observed from various tests. TRW's initial assessment was:

> "The existence of a false lock frequency close to the normal Shuttle transponder input carrier in the SGLS frequency high, data low mode was uncovered in the course of routine EMC evaluation. Further investigation revealed that it was not simply a discrete frequency, but rather a band of frequencies on either side of the assigned carrier frequency. In addition, it was found that each band extends approximately 300 kHz to 800 kHz from the carrier in all SGLS and STDN data low configurations for relatively high level inputs.
>
> Preliminary evaluation of the test results indicates that this phenomenon is inherent in the design of receivers employing the Costas loop. The problem stems from the physical impossibility of being able to perfectly match the gain and phase characteristics of the low pass filters in the two Costas arms over a wide frequency range, especially in the region beyond the 3-dB response points. Thus, an offset high-level input carrier causing a response in that region results in activation of the coherent AGC and unbalanced inputs to the loop phase detector. The resultant large phase error drives the loop VCXO to one of its frequency limits. As the offset frequency is increased, however, eventually a point is reached where the filter gain response is down far enough to deactivate the coherent AGC and reactivate the normal sweep. Inasmuch as the cause of this anomalous behavior appears to be intrinsic to Costas loop receivers, it is recommended that action be taken to ensure that spurious inputs from other equipment are below the false lock threshold in these bands."

Axiomatix reviewed the facts and came to the same general conclusions. The "false locks" were not actual Costas loop phase tracking

states but, rather, false states of in-lock produced by the lock detector due to anomalous performance. The essence of the problem is marginal design of the Costas lock detector circuits. Axiomatix, therefore, could not accept the TRW statement that "anomalous behavior appears intrinsic to Costas loop receivers." Redesign was necessary.

At the Aguust monthly review, TRW announced that the problem had been solved by certain "modifications to the tracking loop filter" (details not supplied). Although this appeared to be true for the engineering model, new problems arose during September and October with the flight hardware. The trouble was with the second IF module, concerning which it was stated, "only the designer can align--it takes him 4 to 6 weeks for each module--there is no production margin." The solution has consisted of a combination of performance prescreening of critical components (to minimize the number of compensations required) and early building and testing to uncover and correct problems with the module prior to incorporation into the overall transponder assembly. It is unclear as of the writing of this report that there will not be additional problems. (See subsection 6.3.2. for some further comments.)

Another genuine false lock situation was observed to occur in the TDRS or spread spectrum modes. These false locks are expected; see subsection 5.7 for analysis results. To avoid such false lock situations, Rockwell recommended that ground station procedures should require the removal of data modulation during acquisition of the spread spectrum signal.

4.3.2 FM Subsystem

Two of the FM transmitters experienced an unexplained upward frequency drift over a protracted period of time. A similar drift was not observed in the engineering model. The transmitters were returned to Teledyne Electronics for evaluation and problem resolution.

At the writing of this report, the reason for the FM transmitter frequency drift is still under investigation. It appears that the problem may stem from a combination of manufacturing operations, component contamination and aging, and the need for a 48-hour vacuum bake followed by a 100-hour burn-in.

5.0 AXIOMATIX SUPPORTING STUDIES AND ANALYSIS

This section contains seven detailed pieces of work that were done in support of the design of the payload-related avionic equipment and the performance evaluation of the S-band network hardware. Each of the topics/subsections are reasonably self-contained in that they introduce the nature of the problem, describe the study/analysis, and present the results with conclusions.

Reference to the relationship of these efforts to the hardware subsystems developments over the reporting year was made in Section 4.0. The following list, therefore, indexes each work back to the appropriate Section 4.0 topical subsection.

	Subject Title	Relevant Subsection
5.1	PI Receiver Triplexer Evaluations	4.2.1.3
5.2	PI Receiver Interference Levels	4.2.1.4
5.3	PI Receiver False Lock Avoidance	4.2.1.5
5.4	PI Receiver Wideband Output Highpass Characteristics	4.2.1.8
5.5	Costas Loop Acquisition Characteristics	4.2.2.1
5.6	Network Transponder Interference Susceptibility	4.3.1.2
5.7	Costas Loop False Lock Margin	4.3.1.3

5.1 PI Receiver Triplexer Evaluations

5.1.1 General Background

A triplexer is required between the payload antenna and the Payload Interrogator (PI) transmitter/receiver output/input terminals. This triplexer functions to divide the PI transmit and receive bands into "low" and "high" regions for both the NASA and the DOD modes of operation. The purpose of the low/high band selectivity is to prevent mutual interference between the PI and the S-band network transponder during times of simultaneous operation.

To satisfy all of the various requirements imposed upon the triplexer, a designer must make trade-offs between low in-band insertion loss and high selectivity needed to reject adjacent-band signals. Therefore, the specifications imposed upon the overall capability must provide latitude to perform a reasonable trade-off.

The following is a summary commentary on the similarities and differences between th payload interrogator triplexer functional

specification originally prepared by Rockwell International and a practical design specification prepared by TRW in conjunction with the triplexer subcontractor, Transco.

5.1.2 Triplexer Functional Configuration

A block diagram of the triplexer unit is shown in Figure 8. Note that the configuration includes the attenuators used to prevent saturation of the PI receiver during very strong signal conditions (see 4.2.1.6) as well as the filter selector switches. For the discussion which follows, the attenuator function is disregarded and the state of "0 dB" is assumed.

5.1.3 Receive Selectivity Characteristics

Figures 9 and 10 show, respectively, attenuation-frequency plots of the receive selectivity specification for the low and high bands of the triplexer. TRW's characteristics are indicated by solid lines, and the Rockwell specifications are superimposed as dashed lines.

A comparison of the two specifications shows that both provide 55 dB of attenuation at the critical network transmitter frequencies of 2217.5 MHz (low) and 2287.5 MHz (high). The exact rolloff characteristic, however, is not specified by TRW, thereby providing latitude for the filter configuration design. By indicating only the locations of the breakpoint frequencies, many characteristics (Butterworth, Chebyshev and elliptic function, for example) may be used to minimize in-band insertion loss and provide maximum in-band flatness

At frequencies below the two receive subbands, the TRW specification provides for significantly more attenuation than the Rockwell requirement (i.e., 90 dB versus 55 dB). With such capability, the PI transmitters will be well isolated from the PI receiver input port. Above 2340 MHz, TRW proposes only 40 dB of attenuation versus the 55 dB specified by Rockwell. This, however, should not present any practical or operational problems since there are no transmitters above 2340 MHz (except the Ku-band system) which operate in close proximity to the PI receiving antenna.

5.1.4 Transmit Selectivity for the DOD and NASA Low Mode

Figures 11 and 12 show, respectively, the triplexer selectivity characteristics for the low transmit modes of the NASA and the DOD filters.

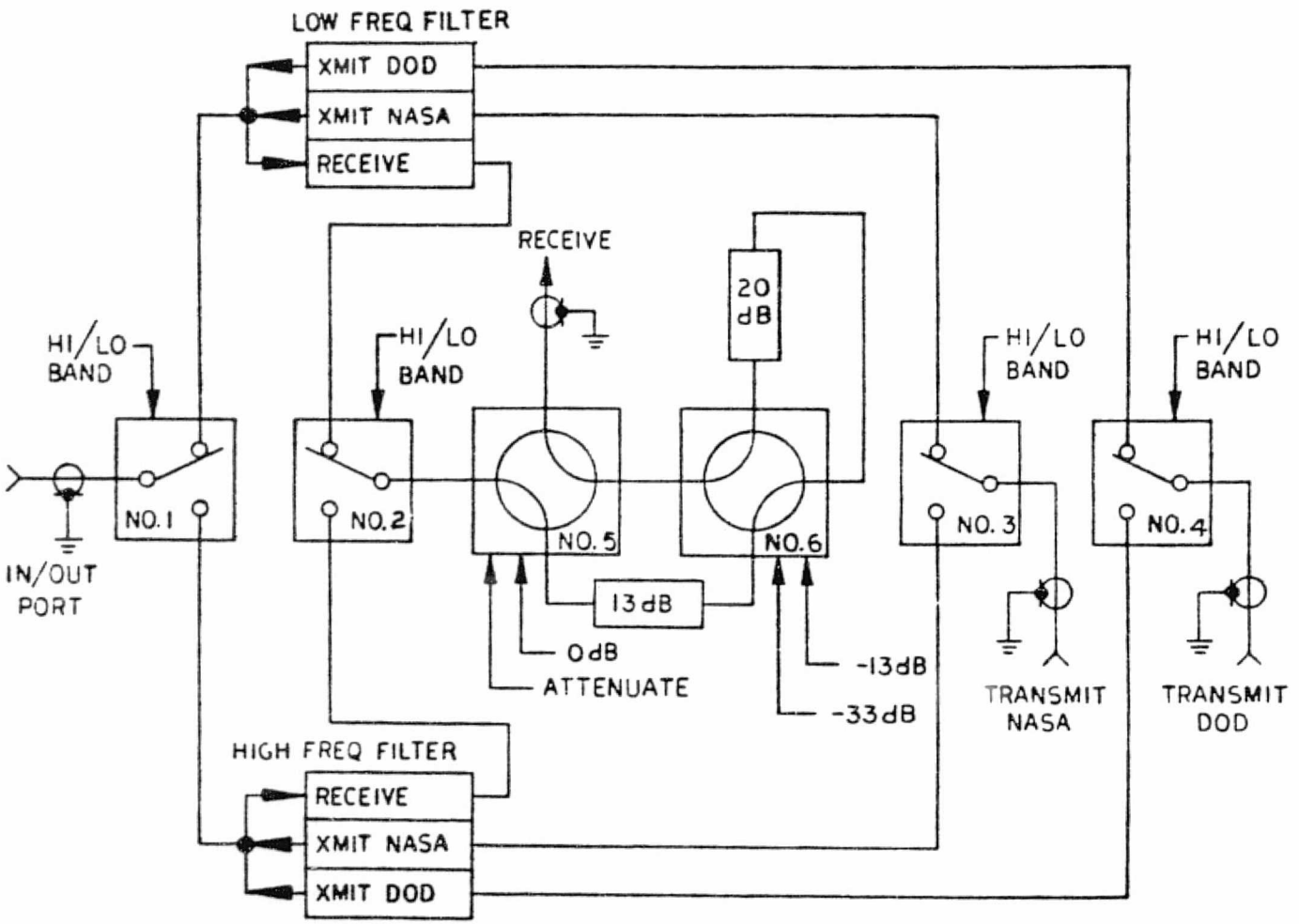


Figure 8. Block Diagram of Triplexer/Switch SRU

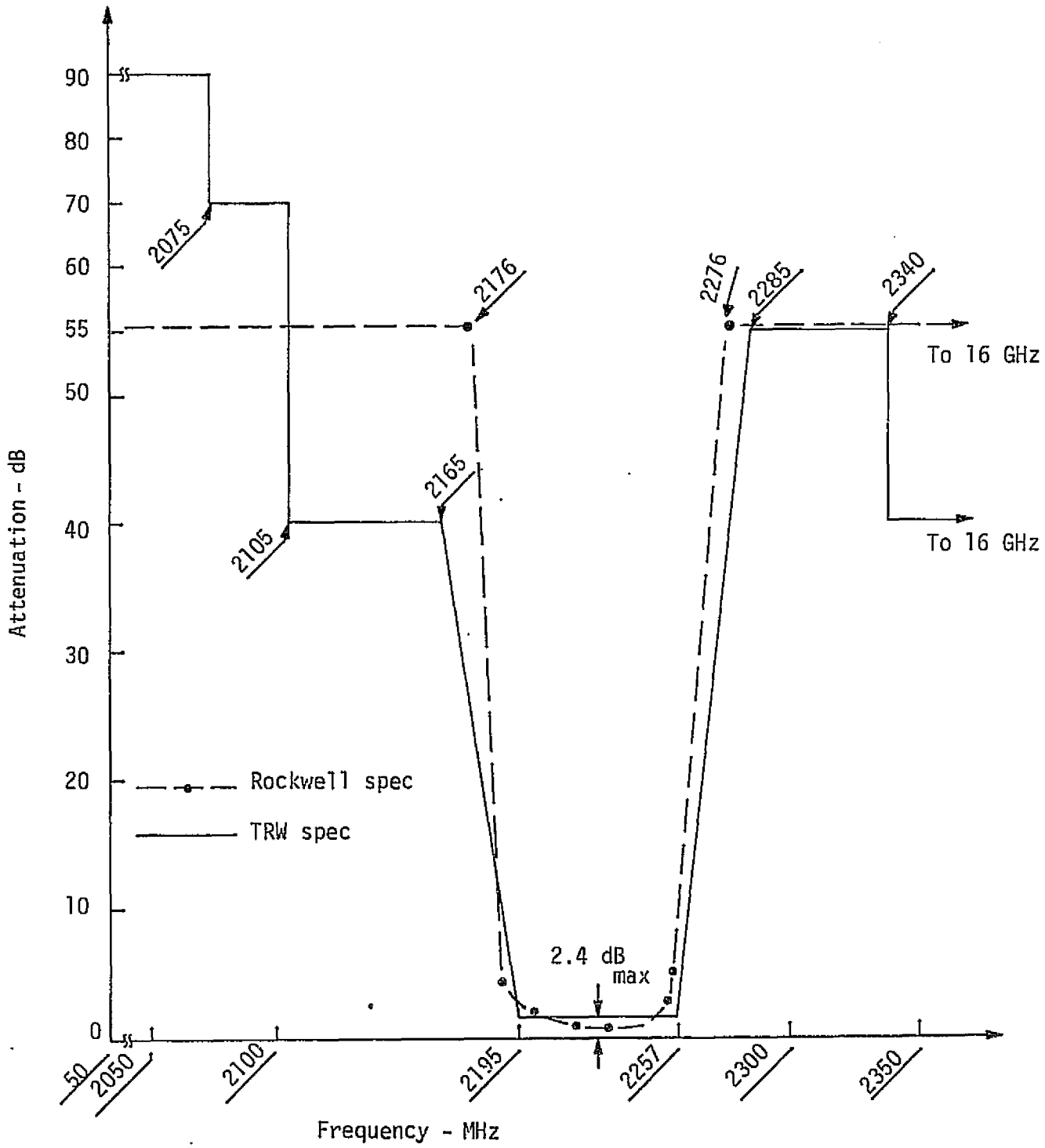


Figure 9. NASA/DOD Low Mode Triplexer Receive Filter

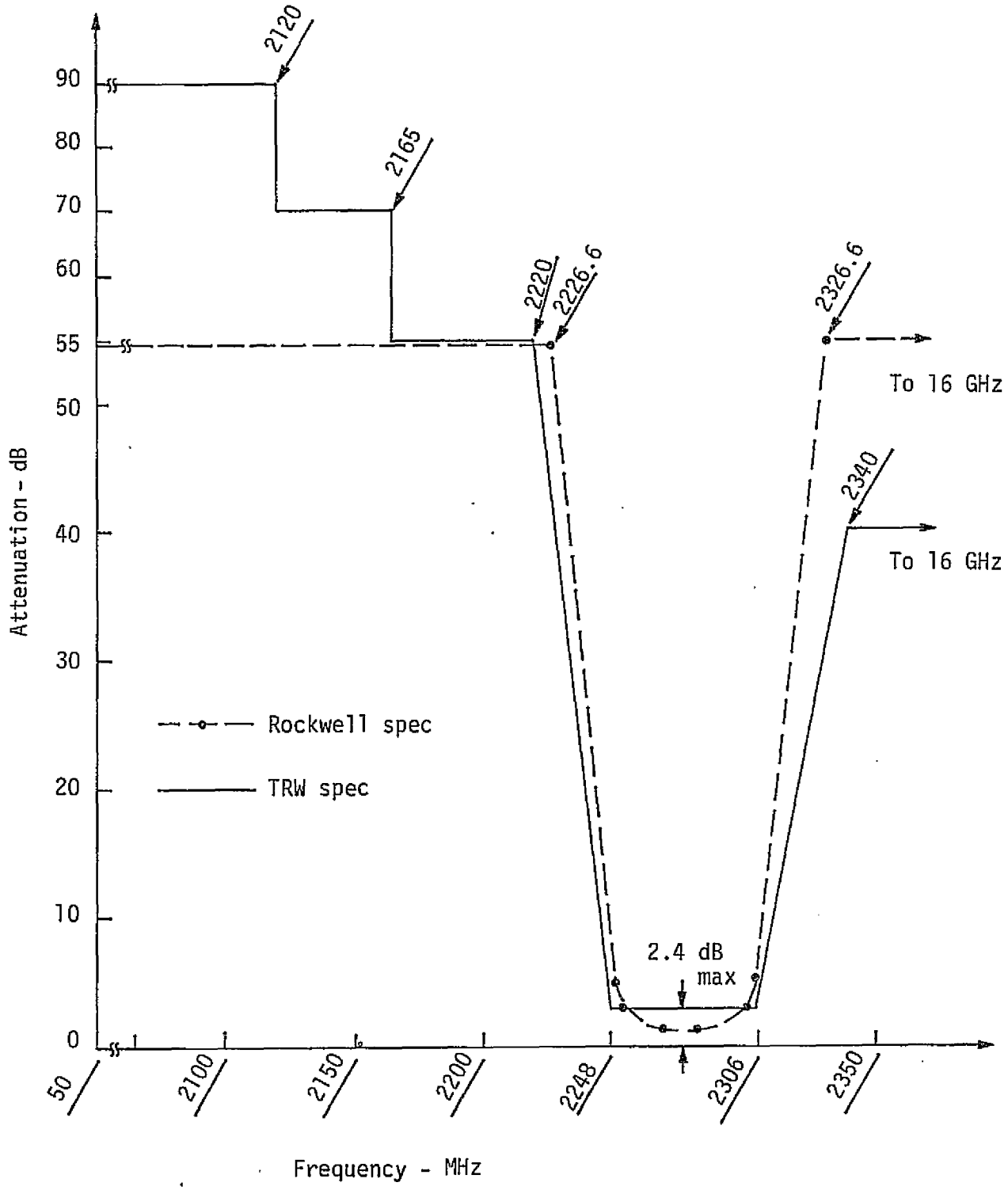


Figure 10. NASA/DOD High Mode Triplexer Receive Filter

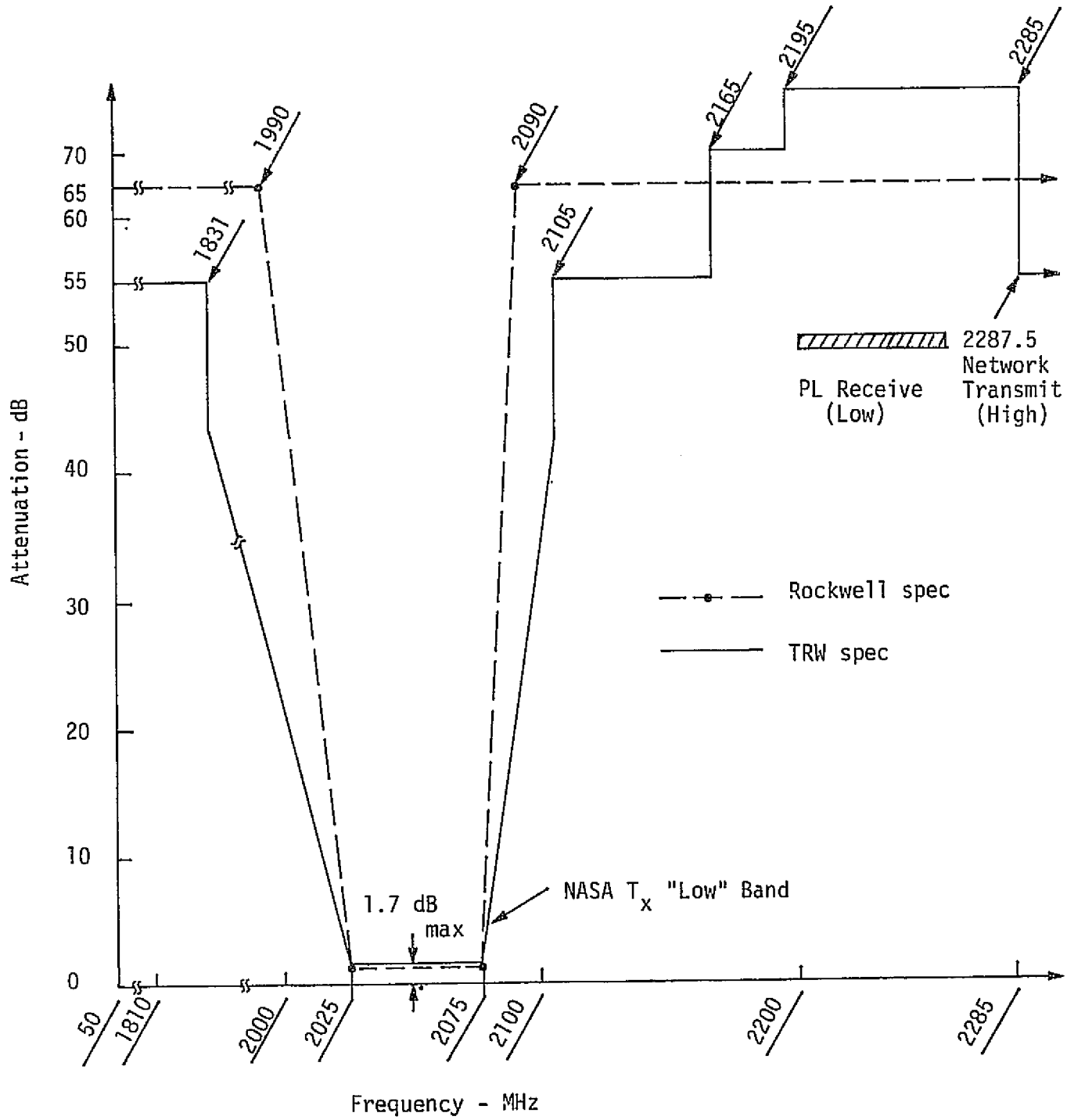


Figure 11. NASA Low Mode Transmit Filter

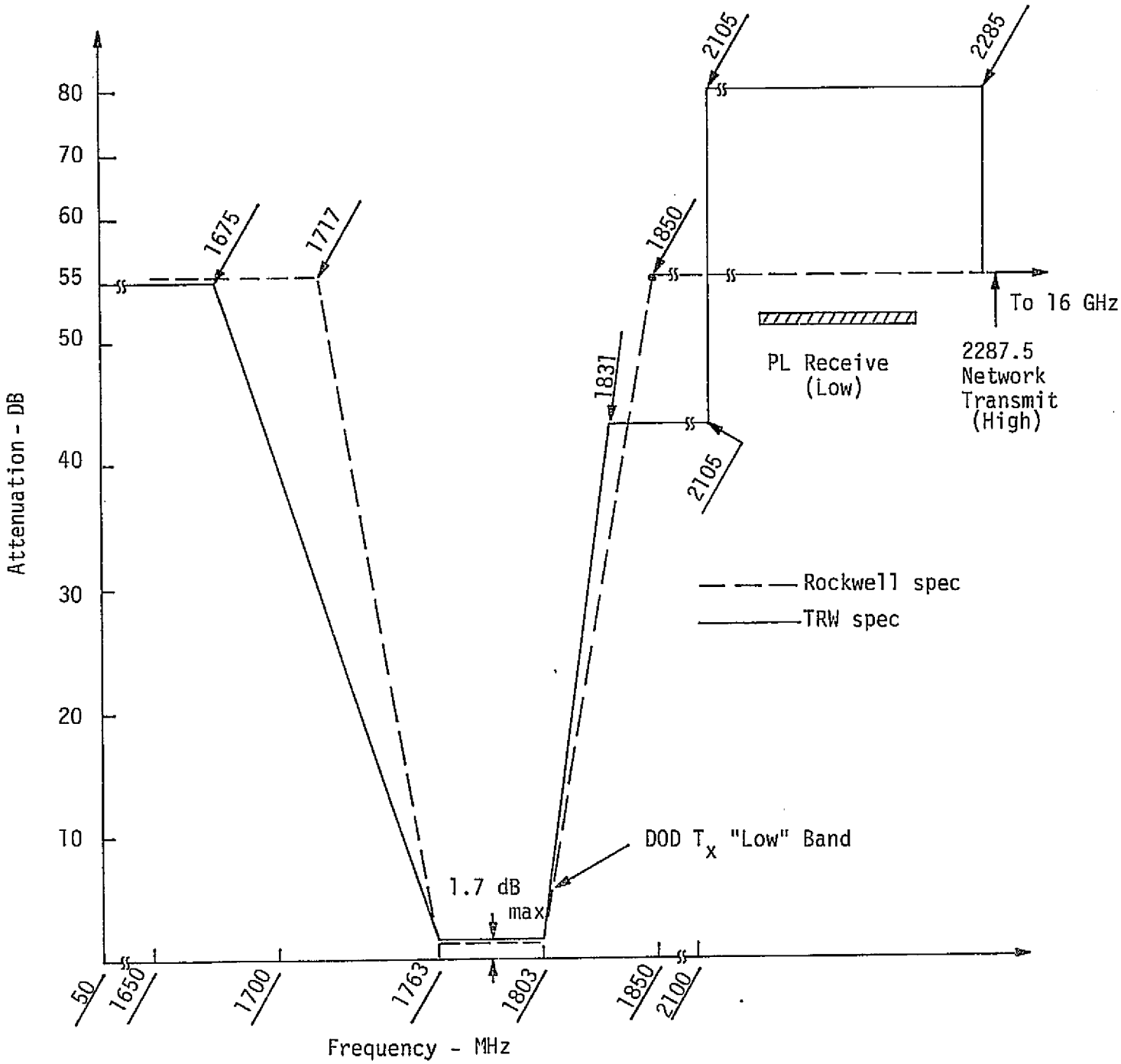


Figure 12. DOD Low Mode Transmit Filter

From these plots, it can be seen that, at the expense of reduced rolloff in the noncritical frequency regions, the TRW specification provides superior attenuation over the PI receive bands. This is a good design philosophy.

5.1.5 Transmit Selectivity for the DOD and NASA High Mode

Figures 13 and 14 show, respectively the comparative specifications for the NASA and DOD filter characteristics in the transmit mode. Similar comments to those made for the transmit mode are appropriate.

5.1.6 Conclusions

An examination and comparison of the TRW and Rockwell specifications for the PI triplexer show that the TRW specification does not compromise on any critical parameters while, at the same time, it is consistent with providing flexibility for the practical design optimization of the triplexer filters.

5.2 PI Receiver Interference Levels

5.2.1 Problem Statement

Given a certain receiver topology, it is desired to calculate the degrading effects of an interference signal with offset frequency appearing at the input to the receiver along with the desired signal. In particular, the interference signal level which increases the receiver effective noise spectral density by 1 dB, when the frequency of the interference is offset from the receiver nominal tuned frequency by 10 MHz, is to be determined.

The following general assumptions are made with respect to the analytical model:

(1) The interference signal is not significantly attenuated by the input filter circuits (diplexer and preselector).

(2) The interference signal does not cause overload or saturation of the receiver RF and IF amplifiers (i.e., the receiver is linear).

(3) First mixer spurs are neglected.

(4) The sole source of the increased noise level is the result of the interfering signal mixing with the first local oscillator (L.O.).

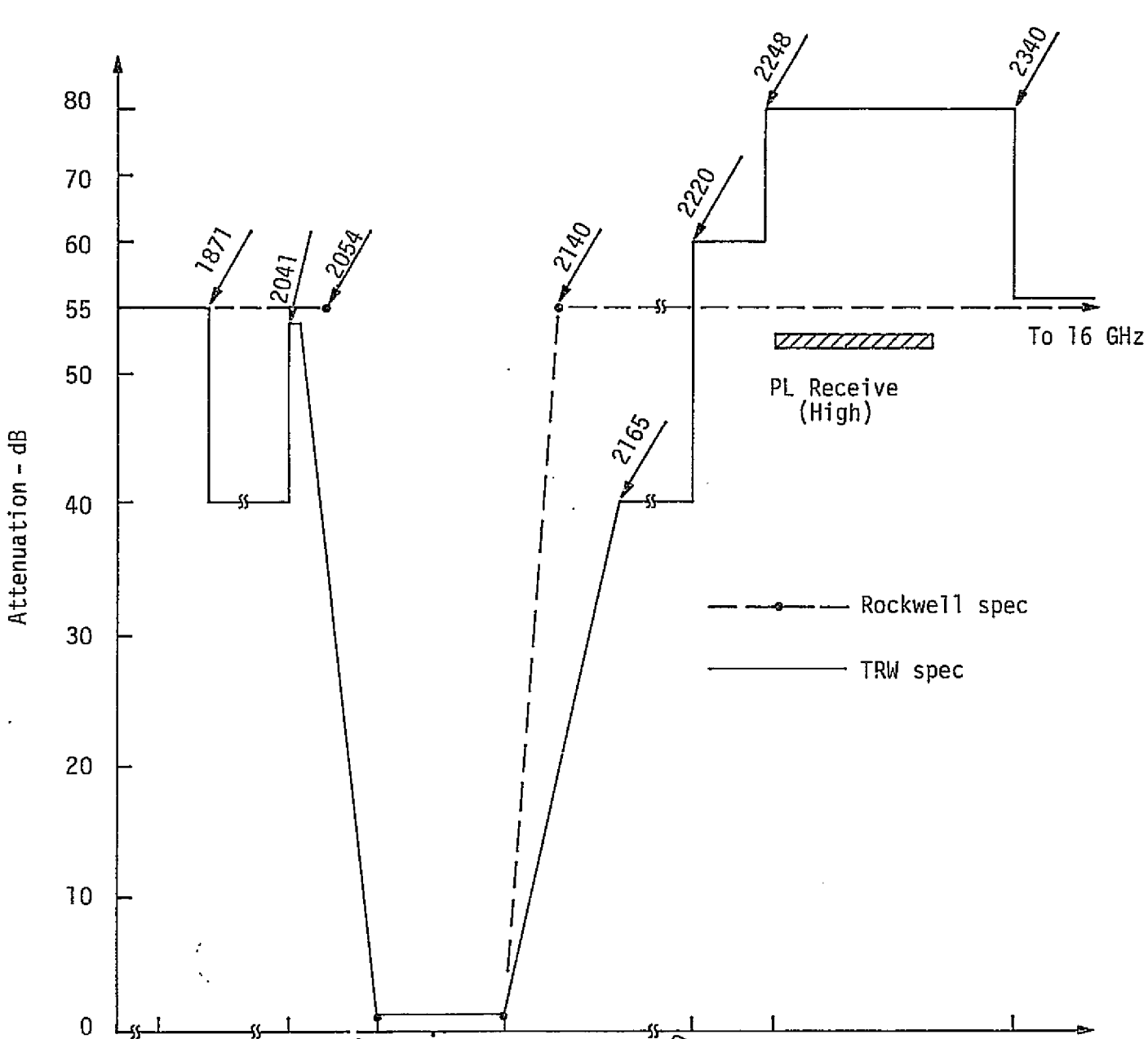


Figure 13. NASA High Mode Transmit Filter

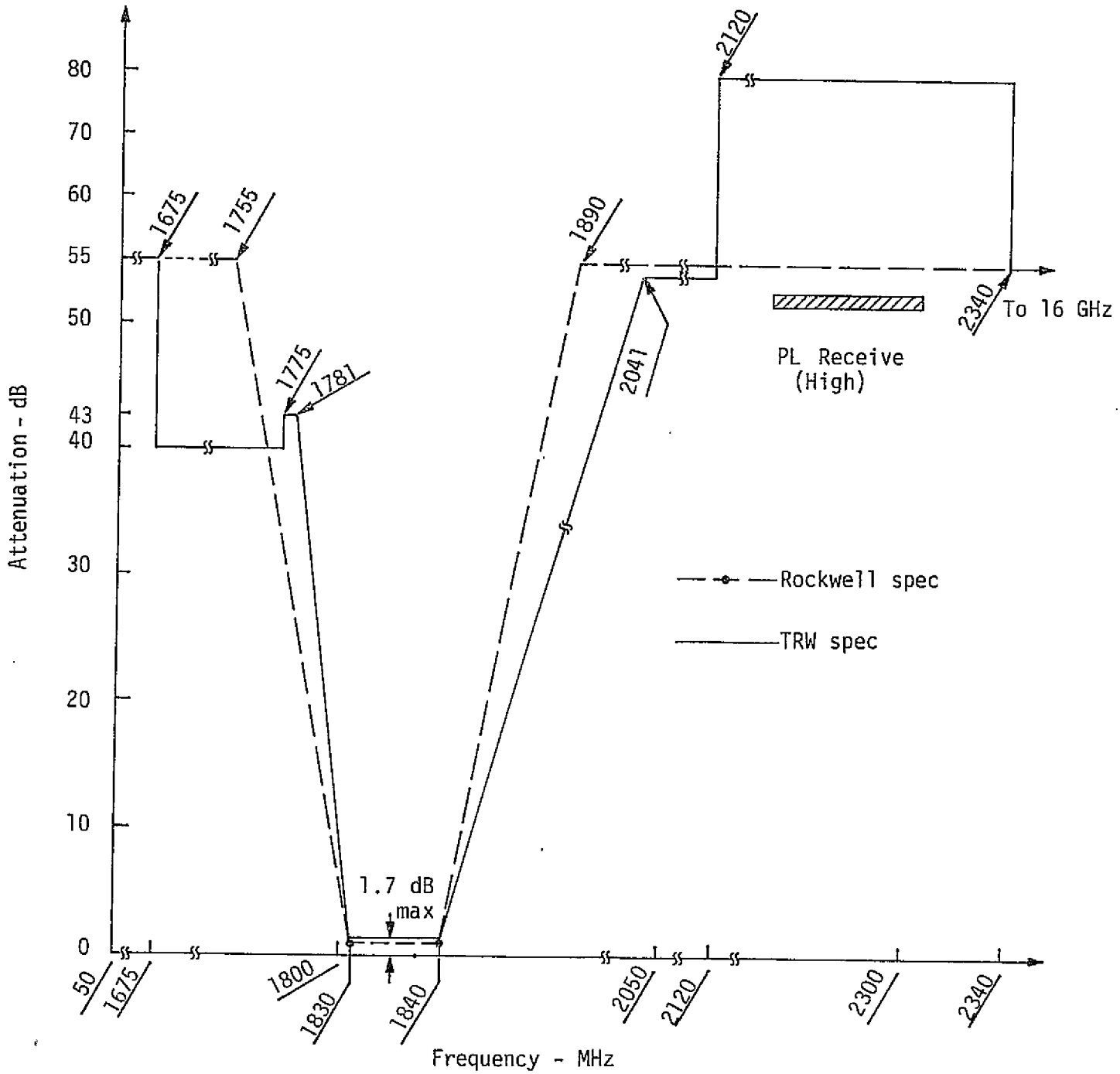


Figure 14. DOD High Mode Transmit Filter

(5) The large discrete component of the interference mixed with the L.O. is greatly attenuated by the postmixer IF filters.

5.2.2 Analytical Model

Figure 15 shows a functional block diagram of the relevant portions of the receiver model. The symbols are defined along with their assumed numerical values* as follows:

Input filter insertion loss = L_F = -2 dB

Preamp noise figure = NF = 5 dB

Preamp gain = G_1 = 20 dB

Mixer conversion loss = L_M = -7 dB

Since the IF circuits following the mixer affect all effective signal components equally in terms of gain, they may therefore be taken analytically to have unit gain.

Now S(t) is the desired input signal and $S_i(t)$ is the interference signal defined by the function

$$S_i(t) = \sqrt{2\,P_i}\,\cos\left[2\pi(f_{IF} + f_{LO} \pm 10) \times 10^6 t\right] \qquad (1)$$

where P_i is interference signal power, f_{IF} is the IF frequency (MHz), f_{LO} is the L.O. frequency (MHz) and the ±10 is the frequency offset of the interference signal.

The reference or L.O. signal is defined by

$$S_{LO}(t) = \sqrt{2\,P_R}\,\cos\left[2\pi f_{LO} \times 10^6 t + \psi(t)\right] \qquad (2)$$

where $\psi(t)$ is the L.O. phase noise modulation due to the thermal noise within the circuits that generate the L.O. signal. The power, P_R, is sufficient to produce the mixer conversion loss given above.

5.2.3 Analysis

The effective noise spectral density, N_0', is comprised of two components: (1) N_0, the thermal noise generated within the preamp input circuits, and (2) N_{0i}, the effective noise produced by the interference signal mixing with the L.O.

*Supplied by TRW.

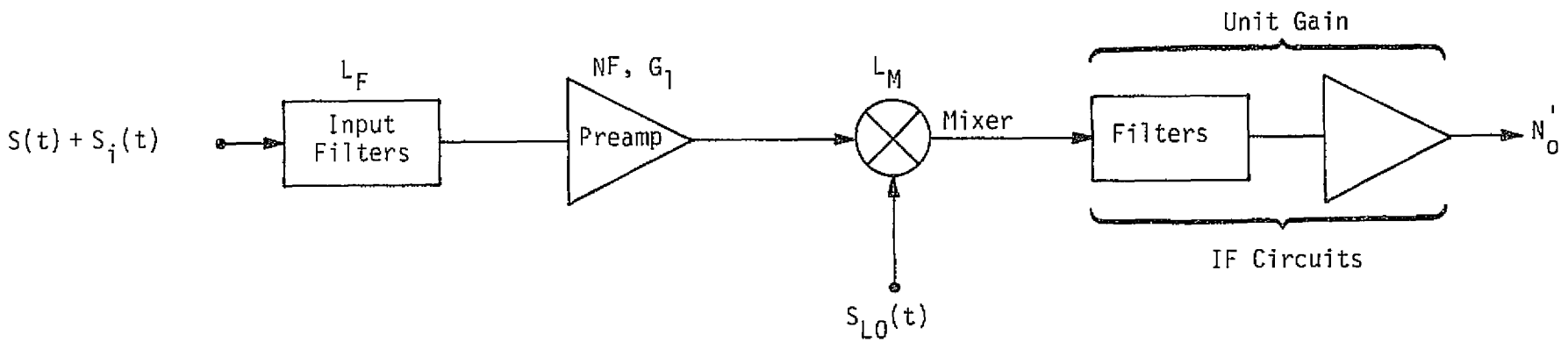


Figure 15. Interference Level Analytical Model

Calculation of the thermal noise, N_0, is straightforward using the equation

$$N_0 = -174 \text{ dBm/Hz} + NF \text{ (dB)} + G_1 \text{ (dB)} + L_M \text{ (dB)}. \quad (3)$$

Substitution of the numerical values given under 5.2.2 results in

$$N_0 = -156 \text{ dBm/Hz} = 2.512 \times 10^{-16} \text{ mW/Hz}.$$

Since it was stated that the contribution of N_{0i} should increase the effective noise spectral density by only 1 dB, then

$$N_0' = -155 \text{ dBm/Hz} = 3.163 \times 10^{-16} \text{ mW/Hz} = N_0 + N_{0i}. \quad (4)$$

Solving for N_{0i},

$$N_{0i} = 0.651 \times 10^{-16} \text{ mW/Hz} = -161.9 \text{ dBm/Hz}.$$

The interference signal translated to the output of the mixer has the form:

$$\sqrt{2 P_i L_F G_1 L_M} \quad \cos \left[2\pi (f_{IF} \pm 10) \times 10^6 t - \psi(t) \right].$$

What must now be determined is the effective noise spectral density of this signal at the IF frequency, f_{IF}. Consider, therefore, the typical spectrum plot shown in Figure 16. Figure 16a is the overall spectrum of the mixer output, with the sidebands relative to the central frequency, $f_{IF} + 10$, arising due to the phase modulation term $\psi(t)$. In Figure 16b, a postulated sideband level relative to the total power $P_i L_F G_1 L_M$ is shown. The relative level at 10 MHz is taken to be -122 dBc/Hz*. The power of the interference is then calculated from:

$$P_i = -161.9 + 122 - L_F - G_1 - L_M , \quad (5)$$

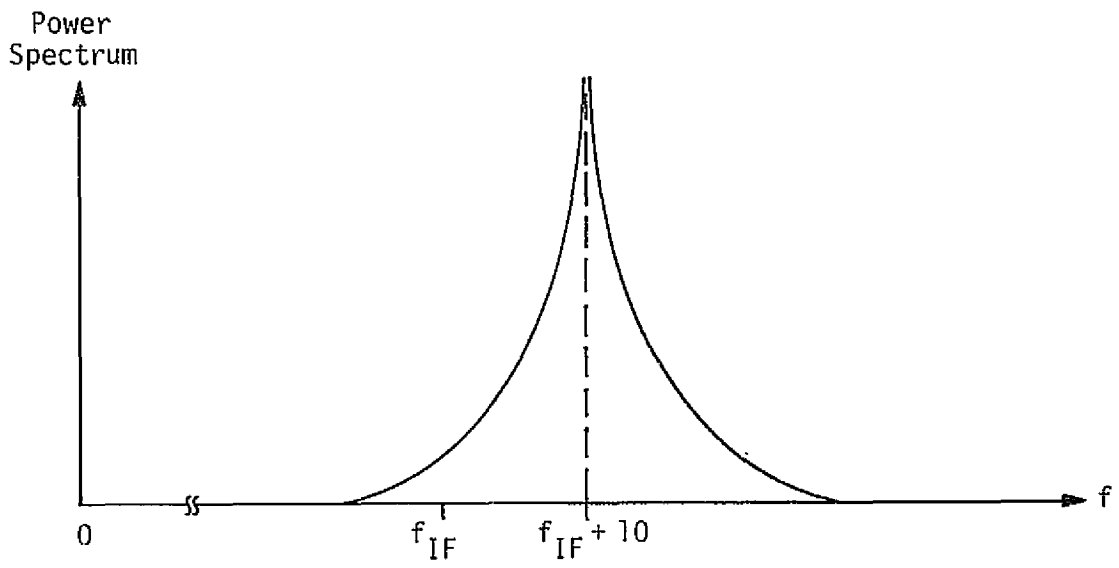
which yields

$$P_i = -50.9 \text{ dBm}.$$

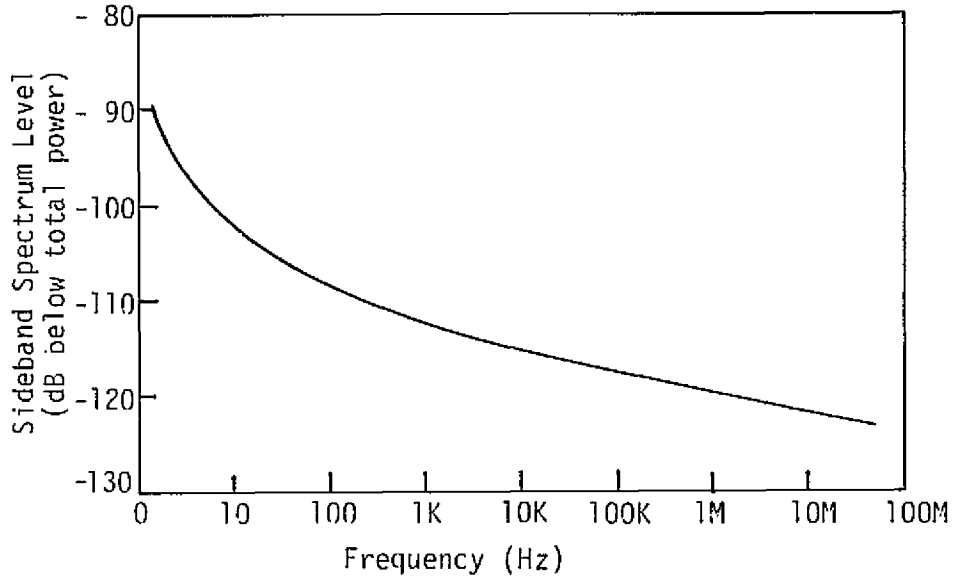
5.2.4 Reconciliation with TRW's Result

TRW obtained a value of $P_i = -65$ dBm based upon a similar analysis. The difference between this result and the one obtained via the above analysis is that (a) TRW used a criterion of 0.1 dB noise spectral density increase due to the interference (this accounts for 10.4 dB), and (b) TRW

*TRW-conjectured value for the PI frequency synthesizer.



(a) Overall Spectrum of Mixer Output



(b) Postulated Sideband Spectrum Level

Figure 16. Mixer Output Spectrum

erroneously included the input filter insertion loss in the calculation of the thermal noise level, N_0.

The P_i = -65 dBm number is therefore very conservative in that it was incorporated into a Rockwell-revised specification (see subsection 4.2.1.4) in terms of a 1.0 dB rather than a 0.1 dB receiver performance degradation factor.

5.3 PI Receiver False Lock Avoidance

5.3.1 Definition of Problem

The problem of avoiding receiver false lock onto modulation generated sidebands of the carrier has no easy solution. For this reason, the potential of a number of methods has been investigated, but no approach has yet been selected in lieu of, or as an addition to, the basic PI receiver lock detector "threshold" technique.

Before proceeding with the specific studies performed under this contract, it is important to define several aspects of the problem so that the various efforts are properly categorized. First, there are two distinct false lock problems to be considered. The first, and most fundamental, is the false lock susceptibility of an "ideal" swept acquisition phase-lock type receiver to sidebands of the carrier whether they are caused by "standard" or "nonstandard" modulation forms. This may be defined as Fundamental False Lock Susceptibility (FFLS). The second problem is concerned with the false lock state (however manifested) of a practical receiver implementation to standard or nonstandard modulation situations that would not give rise to false lock conditions in the ideal receiver. This problem will be referred to as Implementation False Lock Susceptibility (IFLS).

Now, regarding antifalse lock techniques, there are also two distinctions. First, there is False Lock Avoidance (FLA), wherein the basic premise is that some direct means are provided to preclude the actual state of false phase lock by the tracking loop or to use alternate demodulation means when the likelihood of false lock conditions exist. FLA is an absolute technique; i.e., false lock is precluded within some set of requirements and restrictions whether the susceptibility is fundamental or a function of implementation. Some methods which have been investigated for FLA are:

(1) use of optimized frequency sweep rates

(2) closed-loop AFC aiding

(3) phase feedback (antimodulation)

(4) strong signal noncoherent carrier phase demodulation.

Method (2) will be discussed in this report only from the aspect of general functional configurations (see subsection 5.3.3). The use of methods (1) and (2) from an overall system point of view is covered in the final report on Contract NAS 9-15240D. An analysis of method (4) appears in subsection 5.3.4.

The second antifalse lock technique is defined as False Lock Detection (FLD). Here the premise is that of providing subsidiary means for detecting a possible state of false lock or, alternately, mechanizing the receiver's lock detector in such a way that it will not indicate lock for a specific set of potential false lock conditions even though the tracking loop may have indeed achieved a state of valid lock to a carrier sideband component. Thus, FLD is a relative technique in that it allows false lock to occur, but acts (in some way) to negate such lock and continue the acquisition process until valid carrier lock is obtained. Some methods that have been investigated for FLD include:

(1) high-biased lock detectors

(2) frequency error detection

(3) spectrum analyzer.

Only method (1) is addressed in this report in subsection 5.3.2.

One final note is made. The TRW receiver design makes use of FLD method (1). In addition, because the receiver has no AGC prior to acquisition, it has an IFLS to standard modulations (see subsection 4.2.1.5).

5.3.2 Lock Detector Threshold Method

Figure 17 is a functional block diagram of the PI receiver's sweep acquisition and lock detector circuits. (See subsection 3.3 for the overall PI functional description.) The in-phase phase detector, known as the Coherent Amplitude Detector (CAD), produces the signal that is used to derive both the receiver's AGC and lock detector voltages. The quadrature phase detector generates the loop error signal which is processed by the loop filter and input to the VCO. An acquisition sweep voltage is also generated through the loop filter and applied to the VCO in order that the receiver frequency may be swept over a $\pm$85 kHz input signal

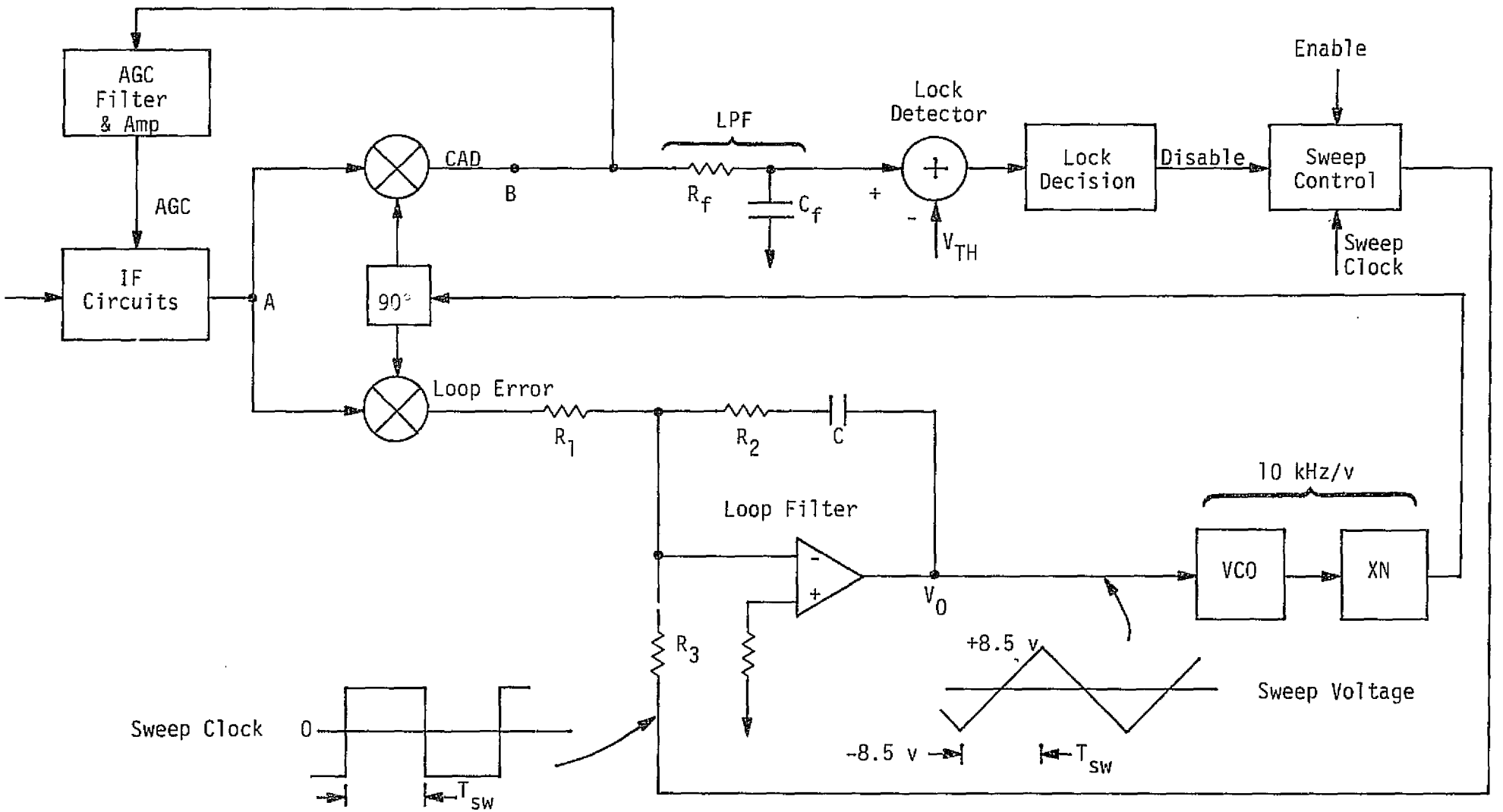


Figure 17. Functional Block Diagram of the PI Sweep Acquisition and Lock Detector Circuits

frequency range uncertainty. Enabling of the sweep function is provided by a manual initiation (or perhaps by external command), while the disable signal is generated when the lock detector attains its in-lock state. When the sweep is disabled, it remains so until an operator again brings it to an enabled condition.

The portion of the receiver to be examined in the following paragraphs is the lock detector itself which consists of a lowpass filter (LPF) followed by a comparison relative to a fixed threshold voltage. For the purpose of analysis, the signal appearing at the input to the phase detectors (point A in Figure 17) will be taken as a sinusoid of frequency f_c, phase modulated by a second sinusoid of frequency, f_m, viz.,

$$S(t) = \sqrt{2P}\cos\left[\omega_c t + \beta\cos(\omega_m t)\right] \tag{6}$$

where β is the phase modulation index. When β is small, as it must be in order to have sidebands with relatively low power content (less than -20 dBc), (6) may be approximated by:

$$\begin{aligned} S(t) \cong\ & \sqrt{2P_0}\cos\omega_c t \\ & - \sqrt{2P_1}\sin(\omega_c - \omega_m)t \\ & - \sqrt{2P_1}\sin(\omega_c + \omega_m)t \end{aligned} \tag{7}$$

with $P_0 = J_0^2(\beta)P$ and $P_1 = J_1^2(\beta)P$. Thus, the input signal may simply be considered as a carrier with power P_0, and a pair of sidebands, f_m Hz away from the carrier, each with power P_1.

Now, when the loop is attempting acquisition, a frequency sweep linearly changes the frequency of the reference signals to the phase detectors. Assume for this scenario that the sweep is from above f_c+f_m and downward in frequency. Then, when the reference frequency becomes on the order of (nearly identical to) f_c+f_m, there is a possibility that the loop may false lock to the f_c+f_m sideband provided the conditions are right. Given that a state of false lock occurs, it is then desired to determine the lock detector requirements such that the lock detector will not declare an in-lock state. The pertinent situation is depicted in Figure 18. The multiplication of the f_c+f_m reference with the f_c+f_m input component produces a direct voltage* designated V_1. By contrast,

*All RF second harmonic terms are ignored.

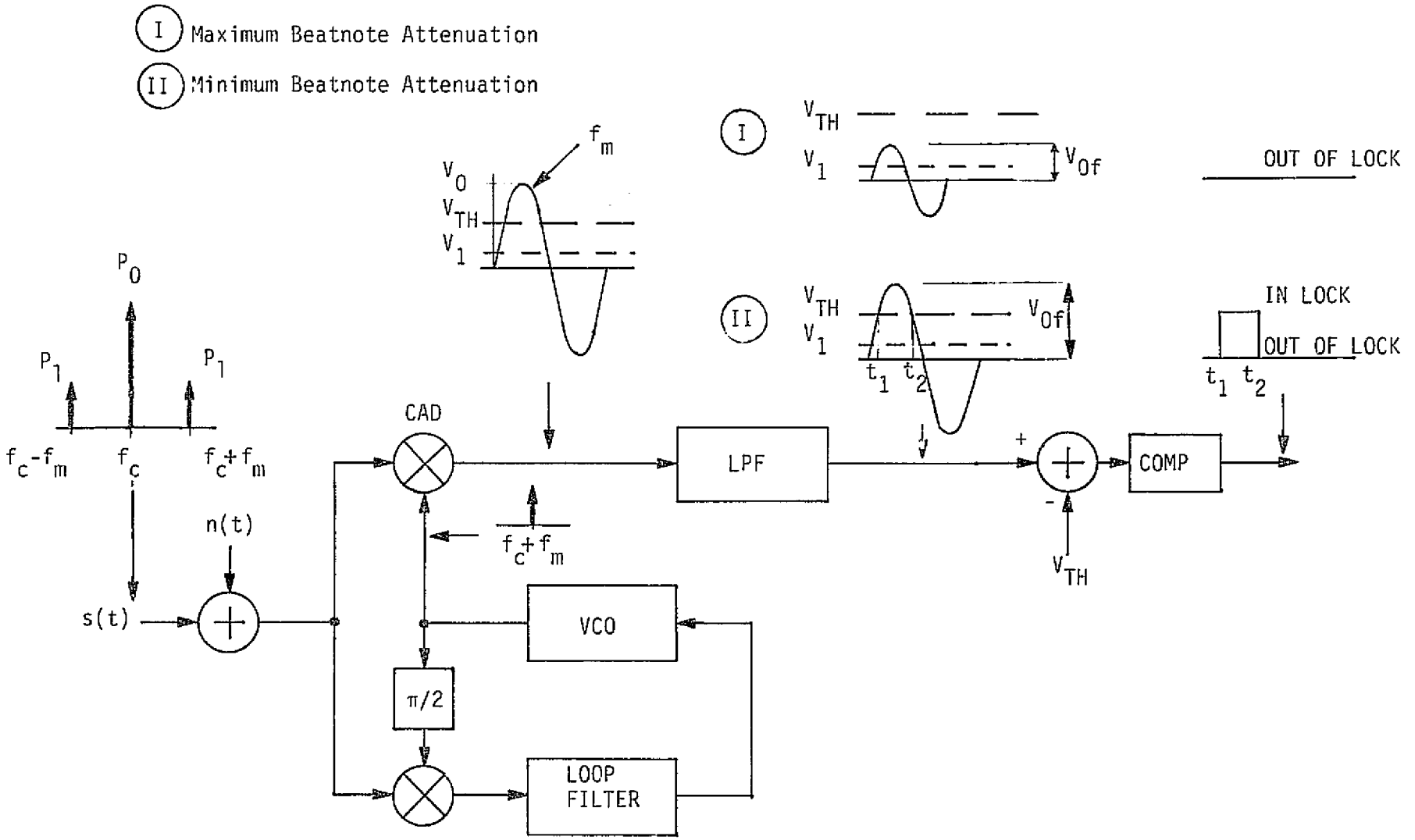


Figure 18. PI Receiver Simplified Block Diagram With Waveforms at Different Points of CAD Channel

the input f_c carrier component results in a beat note of frequency f_m at the CAD output. The peak value, V_0, of the beat note is very large; i.e., $V_0 >> V_1$ (see Figure 18). A second beat note at frequency $2f_m$ is also produced by the phase detection process, but this can be neglected as will become apparent when the desired effects of the LPF following the CAD are considered.

Referring to Figure 18, it can be seen from the graphical inset above the CAD that the maximum positive voltage swing of the combined direct voltage and beat note voltage will be V_1+V_0, and that this can be much greater than the comparator threshold voltage, V_{TH}. However, the LPF between the CAD and comparator should have a significant attenuating effect on the beat note depending upon (a) the relationship between the beat note frequency, f_m, and the filter 3 dB frequency, f_0, and (b) the order of the LPF. Two possible results may thus be obtained as depicted on Figure 18 following the LPF: Case I, where the beat note is sufficiently attenuated so that the threshold voltage is not exceeded and the detector indicates out-of-lock all of the time; and Case II, where the beat note is insufficiently attenuated so that the lock detector has an in-lock state for some fraction of the beat note cycle.

Clearly, only Case I is acceptable for all situations conducive to false lock*. Therefore, the designer of the lock detector must specify f_0 and the order of the LPF to meet the requirement. As an aid in making the necessary trade-offs, Axiomatix plotted the comparative LPF responses of 1st, 2nd and 3rd order Butterworth filters. The overall characteristics are shown in Figure 19, and magnified characteristics for the 1st and 3rd order filters appear in Figure 20. A number of vertical scales for the ratio of V_{0f}/V_1 are supplied as a function of the sideband to carrier power ratio, P_1/P_0, V_{0f} being the attenuated value of V_0.

Typically, the threshold voltage, V_{TH}, will be four to five times greater than V_1 and about one-half of the direct voltage value, V_0, for the true lock situation. (This result stems from noise and the false alarm probabilities as discussed below.) Therefore, the V_{0f} should be

*It should be noted that, if f_m is small and on the order of the PLL bandwidth, false lock is not likely to occur as the presence of the beat note within the loop should cause the loop to lock to the true carrier, the desired condition.

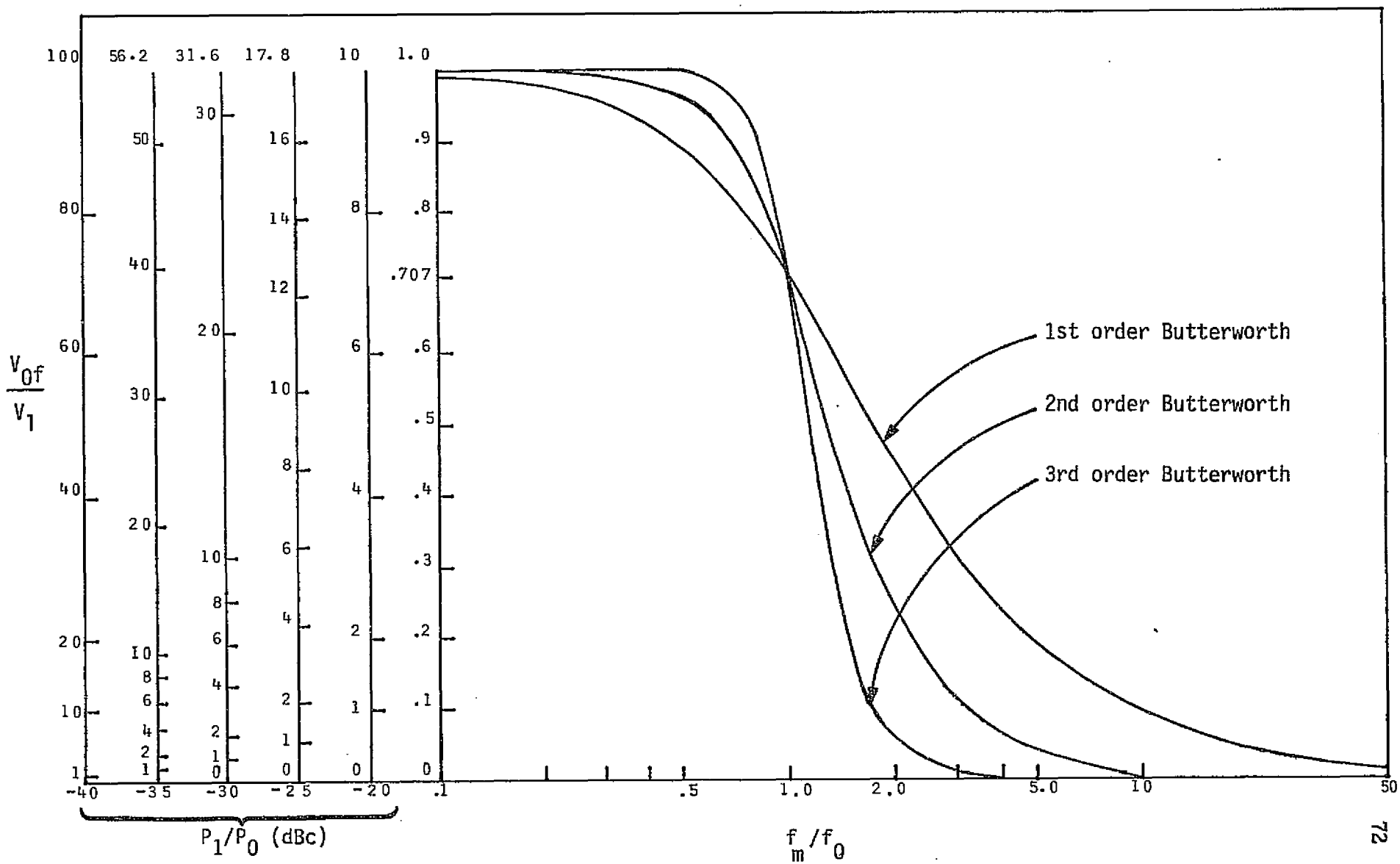


Figure 19. Beatnote Attenuation Characteristics

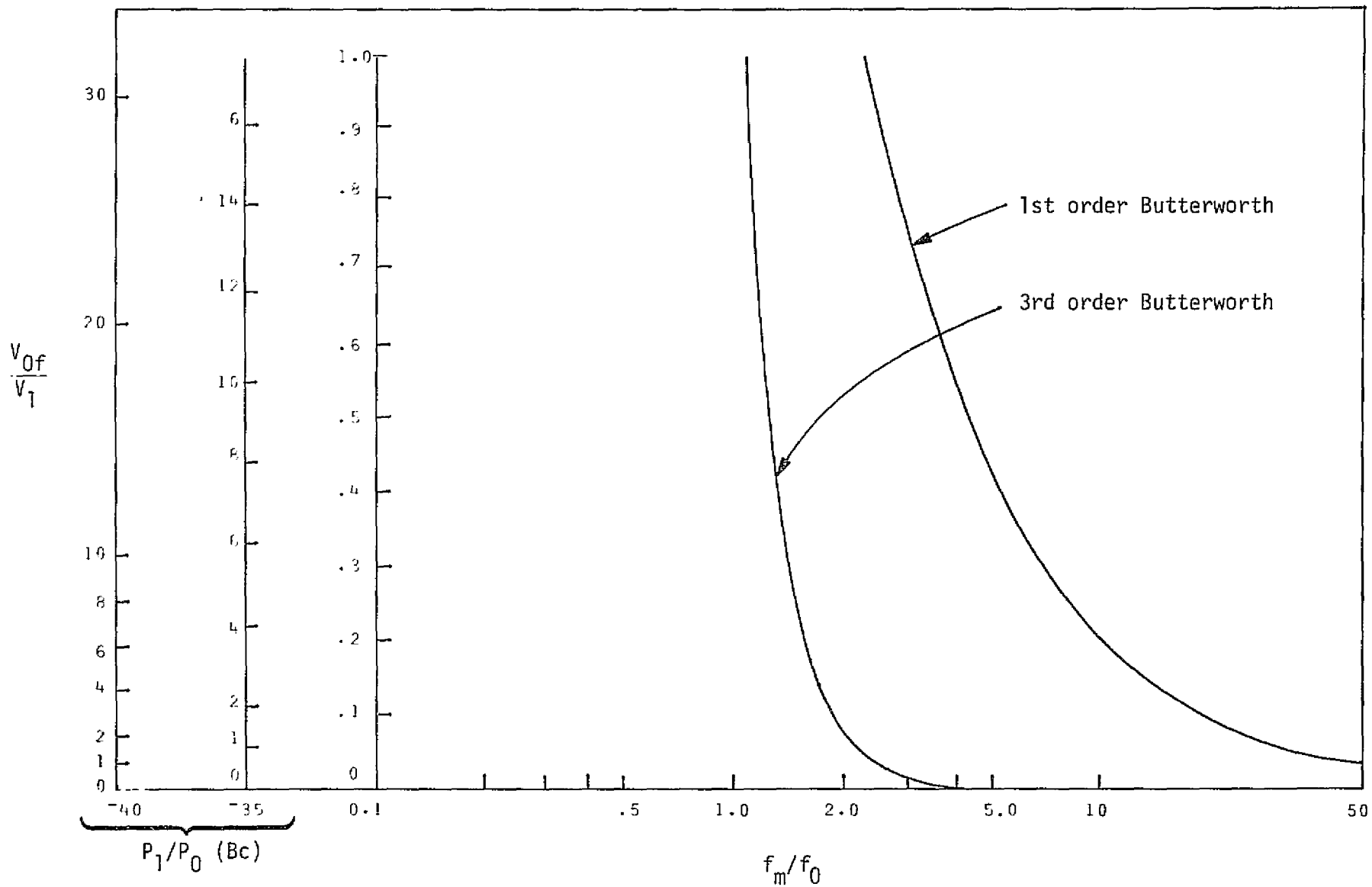


Figure 20. Magnified Beatnote Attenuation Characteristics

no more than about two times V_1 (this allows some margin for noise peaks). Clearly, the first order filter is not very effective in attenuating V_0 for values of f_m/f_0 greater than 2. Furthermore, f_0 certainly should be no larger than the one-sided tracking loop noise bandwidth, B_L, and probably a good deal less. Axiomatix therefore recommends that a third-order filter be used so that the beat note component produces a minimum contribution to the conditions which may cause the lock detector to issue a valid lock indication for a state of false lock.

Once the order and 3 dB frequency of the LPF are selected, the only remaining lock detector parameter that is available for optimization of the overall lock detector performance is the threshold voltage, V_{TH}. Two operational performance probabilities provide the basis for setting V_{TH}: (a) the probability of erroneously indicating a state of in-lock for all conditions apart from true carrier lock, and (b) the probability of indicating a state of out-of-lock when the PLL is in fact locked onto the true carrier. (Neither of these values has been specified as of the writing of this report.) An additional factor which complicates the situation is that, when the receiver is out-of-lock, there is no AGC. For the TRW design, this manifests itself as wideband limiting within the IF circuits, causing maximum drive to the loop phase detectors. At strong received signal levels, the result is "magnification" of the false lock components V_0 and V_1 discussed above. For weak received signals, however, the limiting is on receiver noise, and the desired true carrier signal component in the lock detector is suppressed.

If, equivalently, the receiver is said to have a normalized gain of unity for strong signals, then the receiver has relative gain α, with $\alpha < 1$, when weak signals prevail.

Consider, now, that noise as well as signal appears at the input to the lock detector model shown in Figure 18. The noise is assumed to have the usual Gaussian and wideband characteristics. Taking all variables as they appear at the output of the lock detector LPF, the probability of erroneously indicating a state of in-lock (also known as the false alarm probability) when the loop becomes locked to the f_c+f_m sideband at relatively strong signal levels is:

$$P_{FL} = \text{Prob}\left[V_1 + V_{0f} \sin(2\pi f_m t) - V_{TH} + n_{fs}(t)\right] > 0 \qquad (8)$$

where $n_{fs}(t)$ is the strong-signal noise appearing at the LPF output and V_{0f} is the peak value of the beat note term attenuated by the LPF. The subscript "FL" stands for "false lock." A more useful form of (8) is obtained when all variables are normalized to V_1, viz.,

$$P_{FL} = \text{Prob}\left[1 + \frac{V_{0f}}{V_1}\sin(2\pi f_m t) - \frac{V_{TH}}{V_1} + \frac{1}{V_1}n_f(t)\right] > 0, \qquad (9)$$

wherein the ratio V_{0f}/V_1 may be related to Figures 19 and 20, and $n_f(t)/V_1$ is proportional to the sideband noise-to-signal ratio which may be calculated from the total received signal-to-noise ratio and the specified relative sideband level, P_1/P_0. Note that (9) contains two time variables, the beat note and the noise. In order to calculate P_{FL}, the convolution of sinusoidal and Gaussian probability densities is required.

For the situation of true carrier lock, the probabilities of indicating out-of-lock given the in-lock state for a weak carrier signal is:

$$P_{OL/IL} = \text{Prob}\left[\alpha V_0 - V_{TH} + n_{fw}(t)\right] < 0, \qquad (10)$$

where α is the weak-signal gain factor (suppression) and n_{fw} is the weak-signal lowpass noise.

Having observed all of the preceding considerations, the analysis is essentially complete at this time save for actual calculations. The latter, however, was not carried to completion during the contract period since the TRW receiver design as of December 1978 was insufficiently detailed to yield valid parameter values. Thus, the results of the analysis remain to be quantified, probably during the spring months of 1979. By that time, several important design issues should be resolved relating to receiver out-of-lock/in-lock AGC, lowpass filter order and 3 dB frequency, and the performance probabilities.

5.3.3 AFC Aiding Techniques

5.3.3.1 Introduction

The sidebands generated due to carrier phase modulation are symmetrical in frequency about the carrier. As a result, the use of some form of frequency discriminator, which produces an error signal proportional to frequency offset from the carrier, may be able to aid in preventing receiver lock to sideband components. Known as antisideband lock (ASL)

circuits, a general model of an ASL circuit, together with some specific implementation examples, is presented.

5.3.3.2 Summary of the General False Lock Problem and ASL Functional Capabilities

While searching to acquire a discrete carrier frequency, a PLL is generally susceptible to lock onto any sideband component of sufficient power that falls within the frequency acquisition range of the receiver. This phenomenon is called false lock.

False lock can be detected by an ASL circuit that will function to preclude lock on a sideband and allow the loop to continue search for the desired carrier. Figure 21 shows the general configuration of an ASL system associated with a PLL; the components of this system are a frequency discriminator and a logic circuit.

Consider the simple example of an input signal s(t) (carrier at f_c) phase modulated by a sinusoidal waveform (of frequency f_m); s(t) can be written in terms of its sideband components as

$$s(t) = AJ_0(\beta) \cos \omega_c t - AJ_1(\beta) \sin (\omega_c \pm \omega_m)t + AJ_2(\beta) \sin (\omega_c \pm 2\omega_m)t - \ldots \quad (11)$$

The spectrum of s(t) is shown in Figure 22. When scanning the spectrum in search of the carrier frequency, f_c, the receiver will also encounter the discrete sidebands and the PLL by itself could false lock. The discriminator, however, will generate a voltage due to frequency offset that can be used by the logic circuit to produce an additional error which may be employed in one of several ways to preclude the likelihood of false lock occurring.

Three mechanizations of such ASL circuits that are currently being used within various receiving systems are therefore reviewed as to their functional operation.

5.3.3.3 ASL of the STDN Multifunction Receiver (MFR) [1]

A functional diagram of this circuit is shown in Figure 23. The incoming IF signal s(t) drives three discriminators, D1, D2 and D3, that function over different frequency regions. D3 is a narrowband crystal discriminator, while D1 and D2 use two L-C type tuned circuits above and below the intermediate frequency to generate error signals that cancel

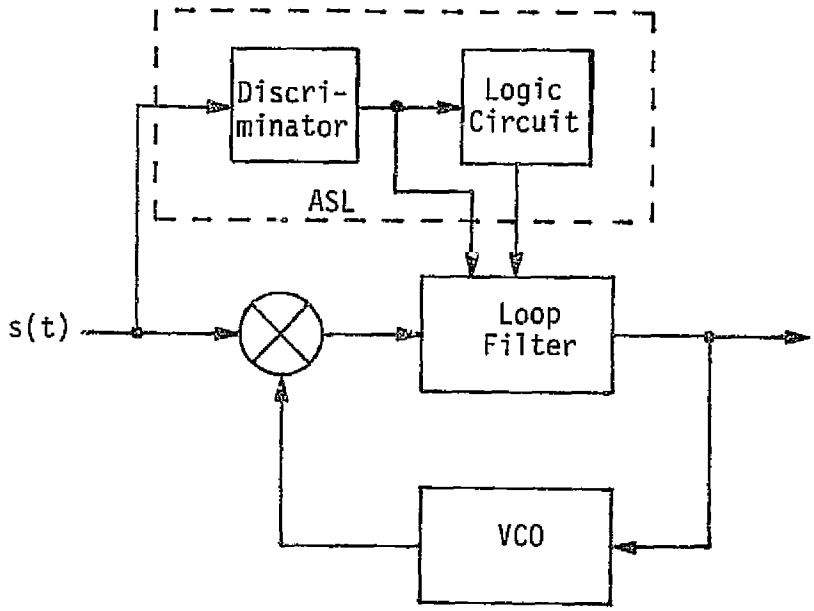


Figure 21. General Configuration of ASL Circuit

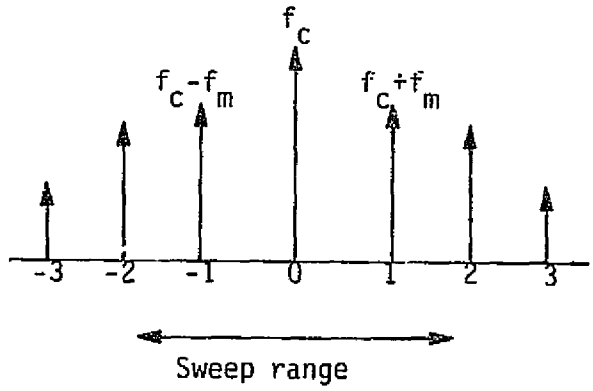


Figure 22. Spectrum of s(t)

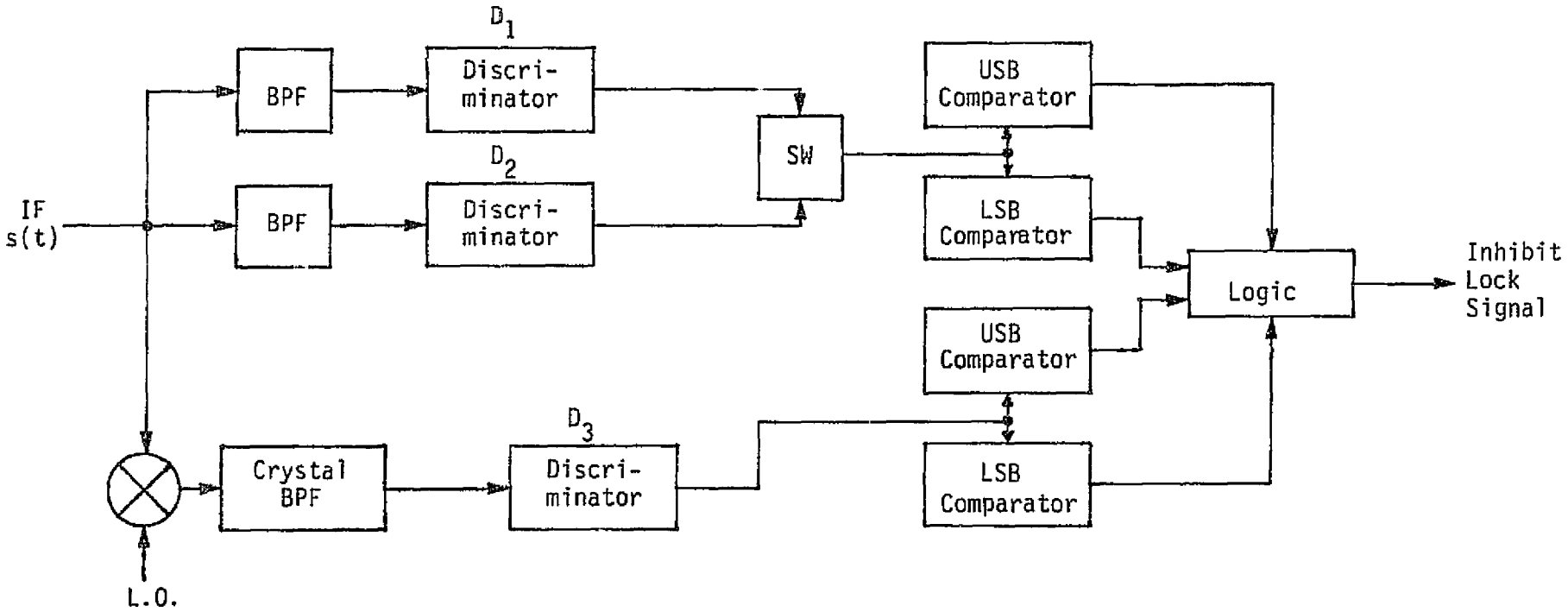


Figure 23. ASL Circuit of the MFR

when the driving signal falls at the carrier frequency. By means of downconversion and the crystal BPF, frequency error to within 100 Hz of the carrier may be detected by D3.

The signals developed by the discriminators are tested for the possibility of sideband lock in USB comparators (for upper sideband lock) and LSB comparators (for lower sideband lock). When the receiver is tuned above or below its nominal frequency, error signals will result causing the outputs of one or two of the comparators to go positive. This, in turn, causes a disable signal to be sent to the PLL loop filter to inhibit lock and continue the acquisition process.

This ASL configuration is effective for any type of modulation that that does not reduce the carrier to zero* provided that the SNR at the input to the widest band discriminator is on the order of 10 dB or greater.

5.3.3.4 Antisideband Circuit (Vitro Electronics) [2]

A functional circuit appears in Figure 24. The approach is similar to the previous one as a frequency discriminating circuit allows the effects of sidebands to cancel when the receiver is properly tuned.

The discriminator consists of two narrowband tuned circuits followed by envelope detectors which are differenced to form the error signal. When the receiver is locked on the carrier, the input to the discriminator consists of the intermediate frequency (f_R) carrier with its symmetrical information sidebands. Under this condition, the output of the discriminator is zero. When the receiver is locked on a sideband, however, the sideband is translated to the reference frequency f_R, and the carrier is displaced by a multiple of the modulation frequency f_m. (For a sideband of order N, the translated carrier frequency is f_R+Nf_m.) The symmetrical spectrum of the input to the discriminator now generates an error signal which, in turn, is used by a logic circuit to send a continue search command to the PLL loop filter. Further, the discriminator generated voltage is added to the linear VCO sweep voltage, accelerating the sweep rate, and thus reducing acquisition time for very large frequency offsets. Since this increased sweep rate is effective only outside of a zone greater than $\pm$600 Hz away from the carrier, true carrier lock is not compromised.

*Suppressed carrier conditions and Costas loops are not considered here.

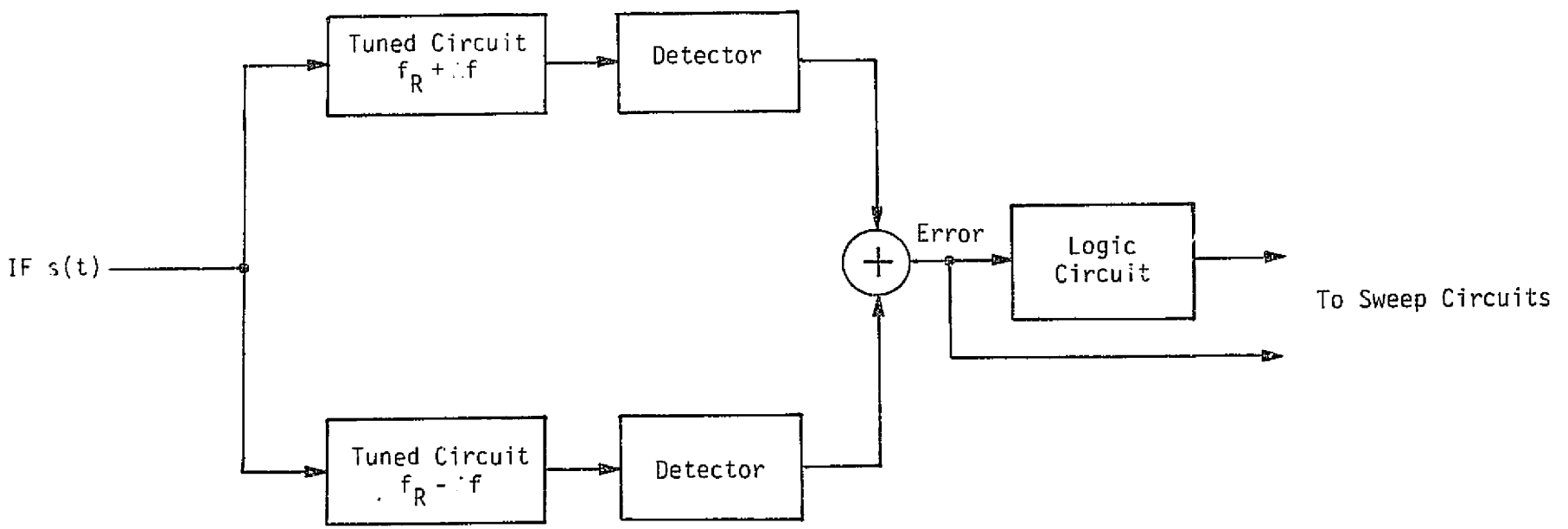


Figure 24. Sideband Discriminator of Vitro Electronics

5.3.3.5 SGLS Transponder AFC Acquisition Circuits [3]

The diagram of this system is shown in Figure 25. Two loops, one AFC and one APC, are used in this configuration to generate the control signal to a common loop filter. When the APC loop is out of lock and the frequency error is larger than $\pm\Delta f$ Hz (as determined by the Δf detector), the switch places the configuration in the AFC loop mode. The frequency discriminator generates a correcting voltage which is applied to the VCO through the loop filter, thus causing the error to decrease.

When the error becomes less than $\pm\Delta f$, the Δf detector functions to switch the loop to the APC mode, where phase lock to the discrete carrier component of the input signal is virtually certain because the received signal frequency falls within the self-capture range of the APC loop.

It should be noted that, for this configuration, a linear sweep voltage need not be applied to the receiver's VCO. The discriminator generated error voltage is sufficient to bring the receiver frequency to within the critical Δf value, and the "memory" within the loop filter serves to keep the received and VCO signal frequencies within $\pm\Delta f$ so that the APC loop will be able to acquire.

5.3.3.6 Technical Evaluation

As seen from the preceding descriptions, two underlying techniques for ASL are used, both based upon frequency error voltages derived from frequency discriminators. They are:

(1) Command the receiver sweep associated circuits in such a way as to continue the acquisition process in spite of a false lock state in the PLL.

(2) Use the discriminator output directly as a control to the APC loop VCO.

Of the three implementations, none has been analyzed rigorously and, furthermore, there appears to be no published experimental information which shows how well they perform with various modulations and for noisy conditions. Thus, to recommend their immediate application to the solution of the PI false lock problems would be to do so without reasonable proof that they will work. At the very least, a program of simulation and experimentation should be conducted before any ASL method is

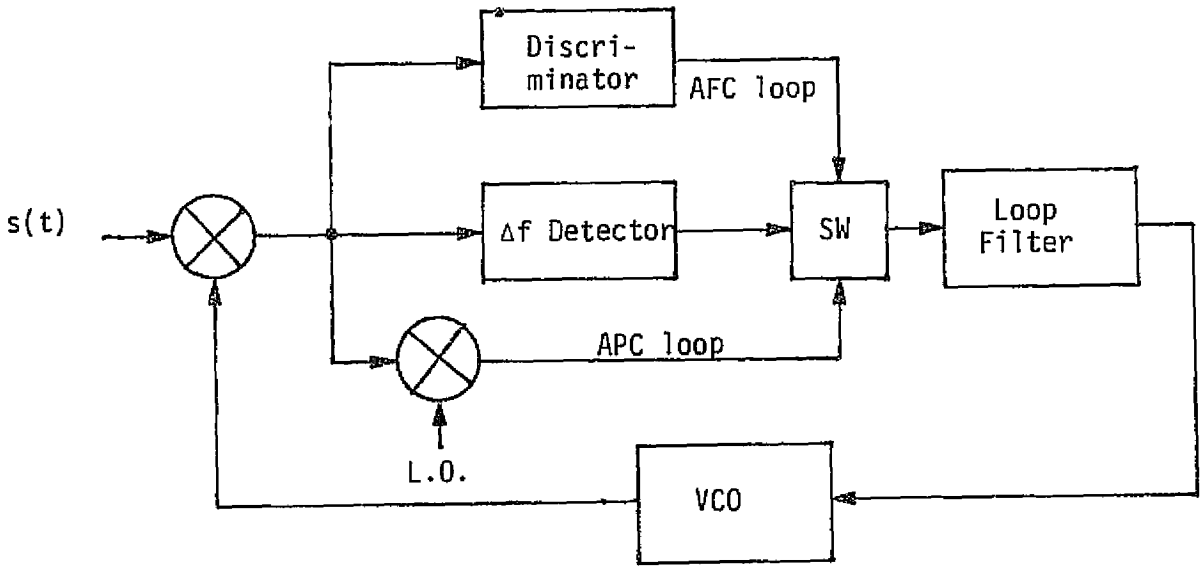


Figure 25. SGLS Transponder AFC Acquisition Circuit

adopted for inclusion in the PI receiver design.

5.3.4 An Analysis of the Use of a Discriminator-Based Phase Demodulator for PI Receiver Strong Signal Levels

5.3.4.1 Motivation

Prior to the PI receiver attaining carrier phase lock, there is no receiver AGC. As a result, the receiver IF circuits operate at their maximum gain values and amplitude clipping or limiting takes place. For strong signal conditions, the resulting signal level drive into the PLL circuits is sufficient to promote the likelihood of receiver false lock onto carrier sideband components for certain conditions (e.g., 256 kbps data on the 1.7 MHz subcarrier). For the sake of this discussion, receiver false lock can be said to have occurred (whether it actually has or hasn't) whenever the PLL lock detector declares an in-lock state as a result of any signal waveforms falling within its bandwidth that cause the reference threshold to be exceeded.

As the signal level input to the receiver is diminished, the receiver begins to limit on its own internal noise rather than the signal itself. This action results in an amplitude suppression of the signal components which gave rise to the strong signal false lock condition. When the suppression is sufficiently large, the propensity of the lock detector to indicate an in-lock state ceases. Figure 26 shows the reduction of false lock threat due to suppression for the current TRW design. Based upon some false lock threat data supplied by TRW, the threat for 256 kbps data on a 1.7 MHz subcarrier with the carrier modulation index, β, of 1.0 radian may be eliminated if the suppression is 12 dB or greater. From Figure 26, it may be seen that the 12 dB suppression corresponds to a net* received signal level of -107 dBm.

The question now raised is: If the receiver may not be effectively used for signal levels above -107 dBm because of false lock threat, is there an alternate and acceptable means of performing carrier-phase demodulation for signal levels greater than -107 dBm? A suggested solution is to make use of a noncoherent phase demodulation discriminator. The following section, therefore, investigates the performance of this approach.

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*This is the signal level at the input to the preamp, beyond any outboard attenuation.

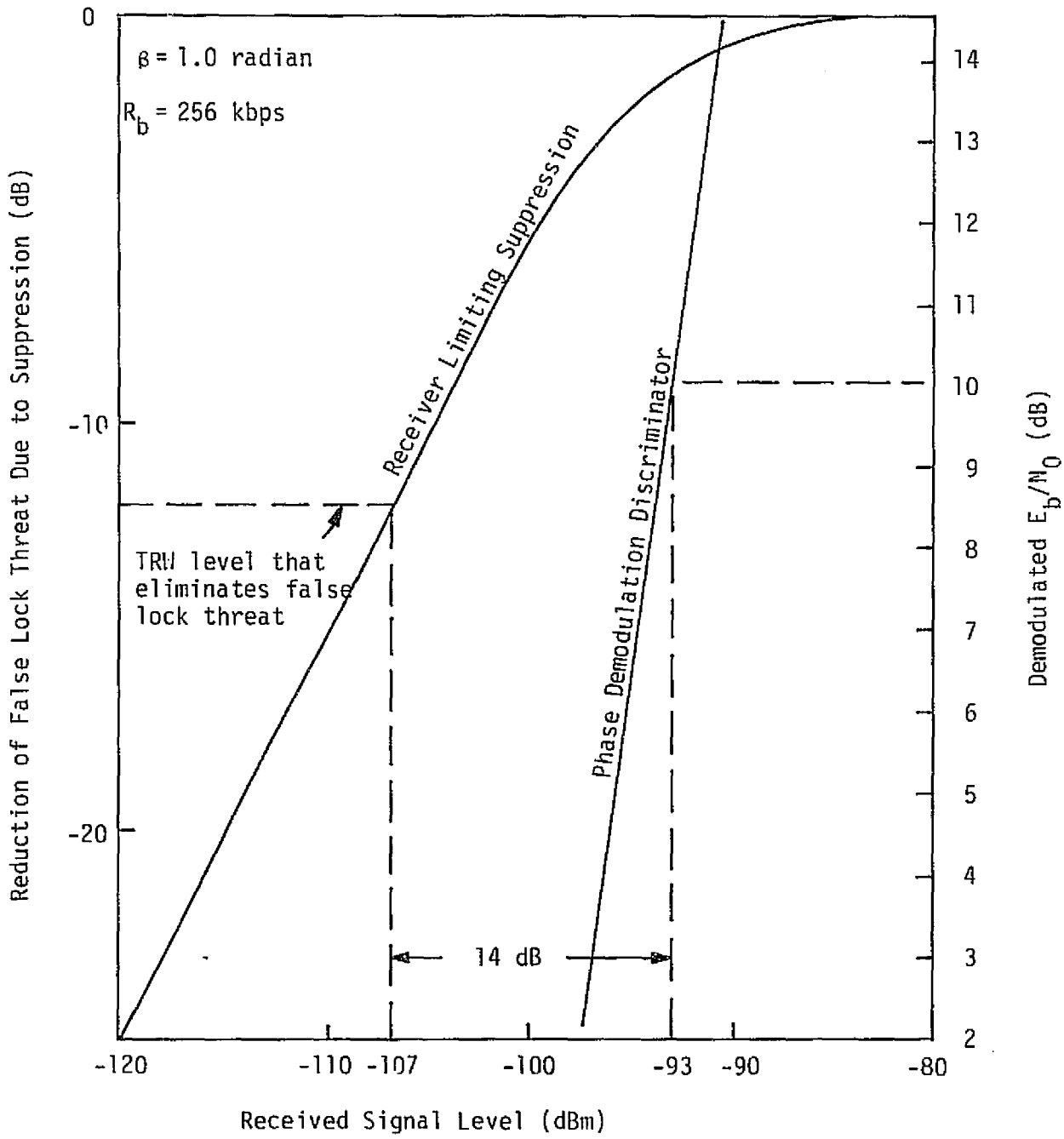

Figure 26. Analysis Results

5.3.4.2 Phase Demodulation Discriminator Performance

For the sake of the ensuing discussion, it has been assumed that the input bandwidth to the discriminator is the same as that which precedes the PI receiver's wideband phase detector. This bandwidth is essentially the second IF bandwidth which is about 12 MHz. It may be logically argued that this bandwidth is too wide for the example case of 256 kbps on a 1.7 MHz subcarrier, and that it should be narrowed to, say, 5 MHz. As will be seen once the results are clear, this difference is not sufficient to alter the conclusions. Further optimizing the phase demodulation discriminator performance for the example case somewhat ignores the fact that the full 12 MHz bandwidth is needed for other modulation conditions, especially for bent-pipe circumstances. Therefore, if the phase demodulation discriminator solution does not act as a coherent PLL demodulator replacement for all nominal existing requirements including bandwidth, it probably should not be accepted as a fix to the problem.

A model of the phase demodulation discriminator is shown in Figure 27. The input BPF establishes the signal-to-noise ratio, $(SNR)_i$, input to the frequency discriminator. The frequency discriminator itself acts functionally as a differentiator/envelope-demodulator over the frequency range of interest. An output filter (LPF/HPF) removes high-frequency noise and any direct voltage component caused by the discrete carrier term. Finally, an integrator restores the demodulated signal to its proper form from its differentiated equivalent produced by the discriminator.

The general performance for discriminators operating with FM and PM signals is the same. Fortunately, published curves of FM performance may be used (with reasonable accuracy) to obtain the PM performance. Only the equivalent FM β' need be established. Now, for a phase modulation discriminator operating in the full improvement input SNR region, the output SNR, when the modulation is in a sinusoidal subcarrier, is given by:

$$(SNR)_o = \frac{\beta^2 B_i}{2B_o} (SNR)_i ,$$

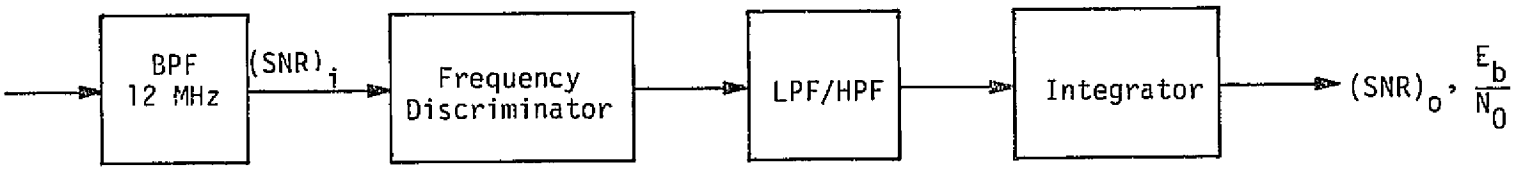

Figure 27. Phase Demodulation Discriminator Model

where B_i is the input noise bandwidth and B_o is the output noise band bandwidth. In order to determine β', take $(SNR)_i = 20$ dB, $\beta = 1$ radian, $B_i = 12$ MHz and $B_o = 5$ MHz. (These bandwidth values are representative of the current TRW PI receiver wideband phase demodulation channel design.) The equation then yields $(SNR)_o = 20.8$ dB. Referring to Figure 28, it can be seen that the curve labeled $\beta' = 1.25$ yields almost exactly this input/output performance; thus, it will be used to obtain the phase demodulation discriminator performance for all $(SNR)_i$.

The phase demodulation discriminator output E_b/N_0 is selected as the performance figure of merit. To establish the E_b/N_0 to received signal level relationship, the following parameter values have been assumed (in addition to those already stated): $R_b = 256$ kbps and $L_D = 2.0$ dB. The loss, L_D, is included to account for all miscellaneous RF and waveform losses plus those associated with the nonideal mechanization of the discriminator and integrator. Using these numbers in conjunction with the $\beta' = 1.25$ discriminator curve of Figure 28, the phase demodulation discriminator performance is obtained and plotted on Figure 26.

Consider an example value of $E_b/N_0 = 10$ dB. Figure 26 shows that this is obtained when the received signal level is -93 dBm. Based upon the premise set forth at the end of subsection 5.3.4.1, however, this is 14 dB higher than that desired, namely, the -107 dBm received signal level for which the coherent receiver false lock threat disappears.

An interesting point of note is that, for the phase demodulator performance shown in Figure 26, the discriminator is operating in the nonimprovement region, i.e., below the knee of the curve. This may be seen from the fact that $E_b/N_0 = 10$ dB corresponds to $(SNR)_o = -2.9$ dB (see Figure 26). It is clear that this will always be the situation if B_i and B_o are on the order of the numbers cited for the current PI wideband channel.

5.3.4.3 Conclusions

From the results shown in Figure 26, it has been established that use of a noncoherent phase demodulation discriminator in place of the coherent PLL demodulator over the complete range of received signal levels for which the PLL/lock-detector circuits portend false lock will not work. This conclusion is based upon the fact that the phase demodulation

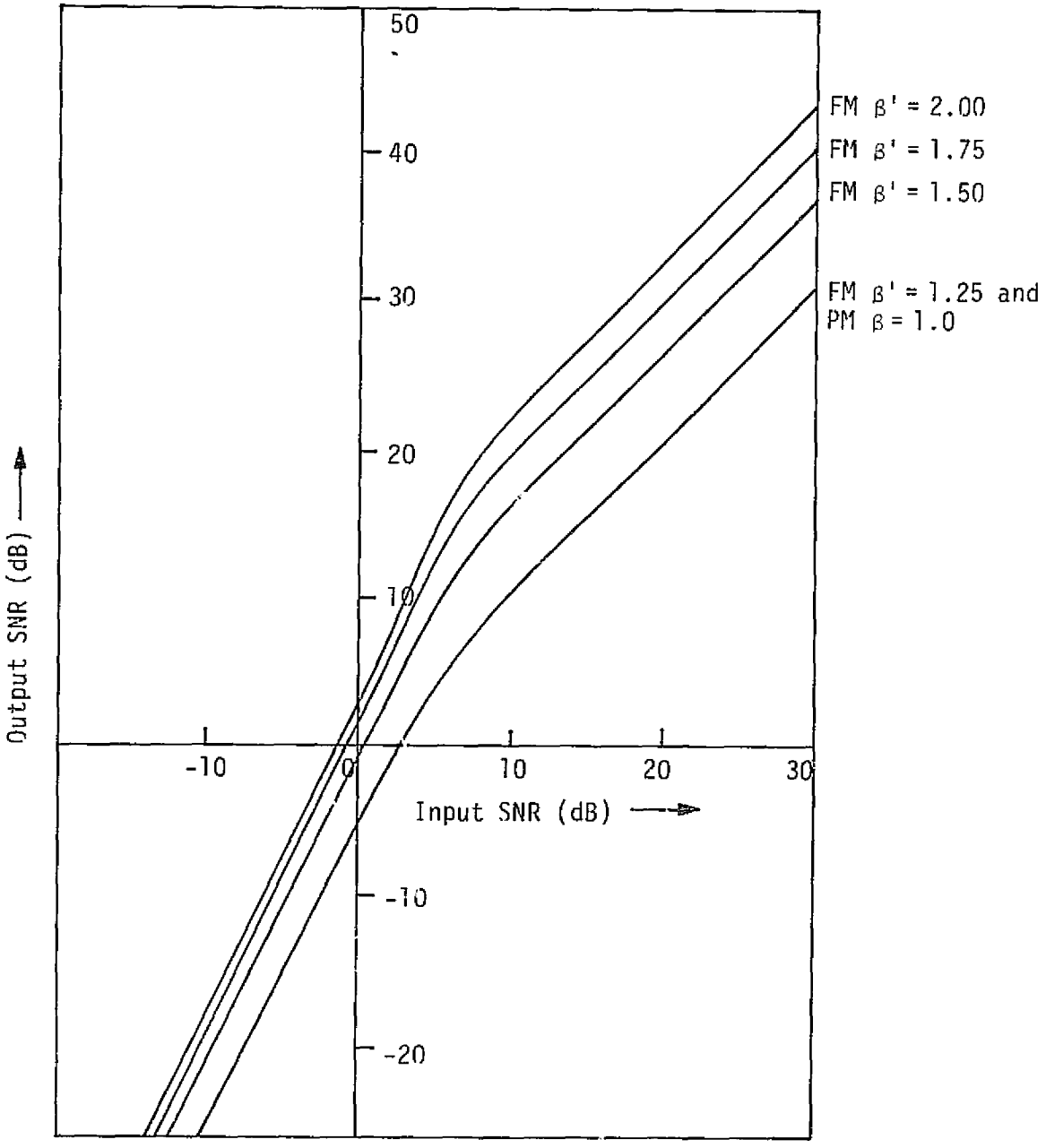

Figure 28. Discriminator Performance

discriminator performance, as measured by E_b/N_0 available at the output, "thresholds" at a received signal level of some 14 dB above that for which the false lock problem vanishes.

It may be questioned as to whether the 14 dB gap may be abridged to the point where the false lock and phase demodulation discriminator received signal level limits will cross. The primary approach to attain such would be to lower the phase demodulation discriminator "threshold." It may be possible to (1) accept a lesser E_b/N_0 (say, 6 dB) and (2) decrease B_i and B_0 (e.g., 5 MHz and 2.5 MHz, respectively). This, however, lowers the threshold in received signal level by only 4.5 dB, far short of making a significant reduction of the 14 dB gap. The prospects for additional improvement are virtually nil.

5.4 PI Receiver Wideband Output Highpass Characteristics

5.4.1 Introduction

It is desirable that the video amplifier which provides the PI receiver wideband output signal to the KuSP have a dc blocking capacitor between its output and the KuSP input. Motivation for such a configuration stems from the fact that all of the circuits within the KuSP, including those of the FM transmitter, are direct coupled. Thus, any direct voltage offsets arising within the PI receiver output circuits could, without the use of ac coupling, "detune" the FM transmitter.

The net effect is to place a highpass filter between the PI receiver's wideband phase demodulator and the input to the KuSP. Given that an output coupling capacitor is to be used, it is also desirable to utilize additional capacitive coupling within the PI circuits themselves. A general block diagram which shows the ac coupling appears in Figure 29. HPF_1 is the internal ac coupling, while HPF_2 forms the blocking filter at the input to the KuSP.

Given such a configuration, the design question simply becomes: What should be the maximum allowable highpass filter 3 dB frequency (comprised jointly of HPF_1 and HPF_2) such that the throughput signal (digital data stream) is not measurably degraded?

5.4.2 Data Rate and Transition Restrictions

Although the highpass filter sections within the output circuits of the PI receiver are the subject under study, the phase-locked tracking

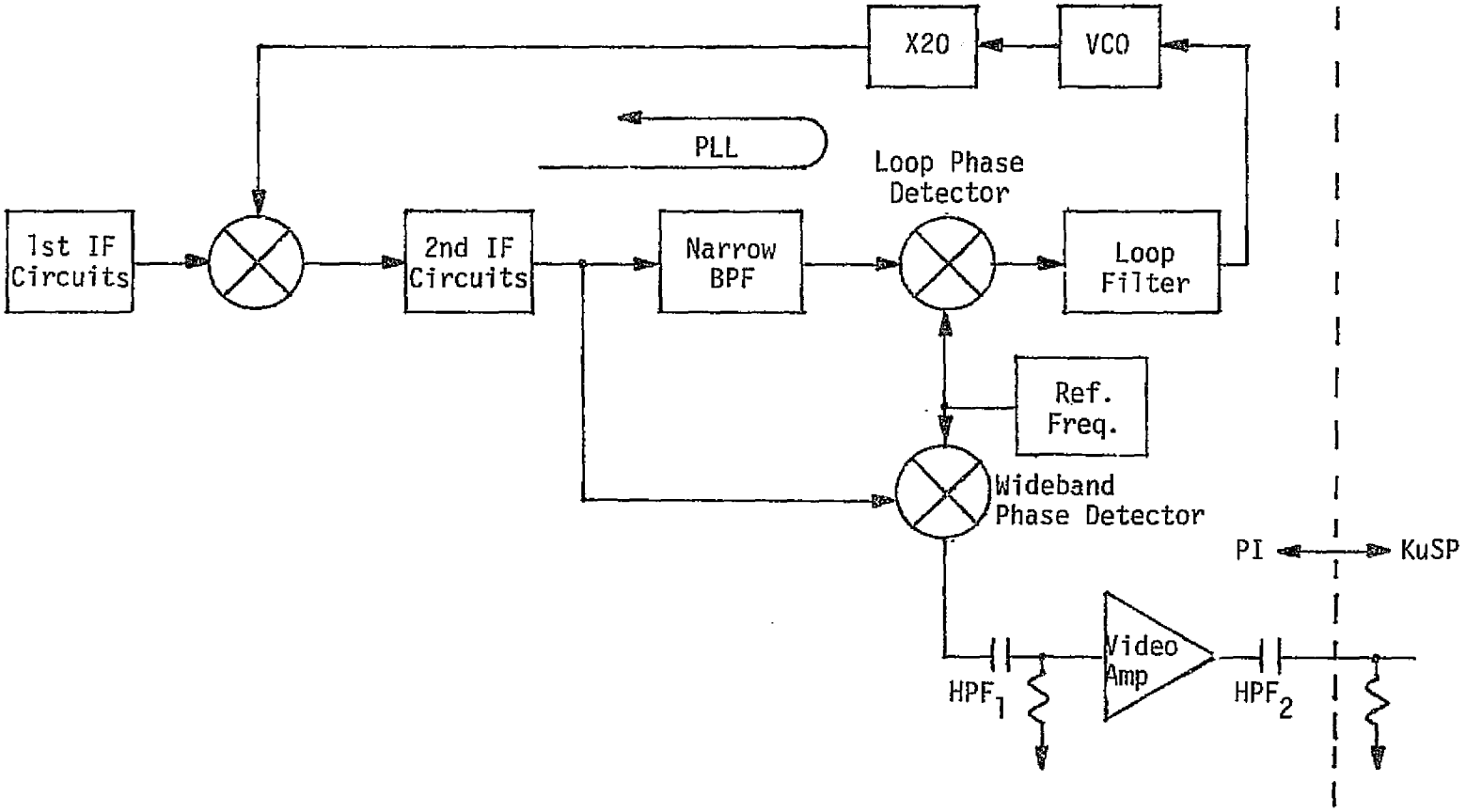

Figure 29. PI Receiver Tracking, Demodulation, and Wideband Output Circuits

loop and demodulator which precedes these filters is itself a highpass filter. In fact, it is the highpass characteristics of the PLL demodulator which dictate restrictions on the carrier modulating digital data signal. In Figure 29, the complete receiver configuration which contributes to the overall PLL/HPF model is shown. This may be reduced to the simple analytical model of Figure 30 where the PLL has the highpass transfer function 1-H(s) and the combination of HPF_1 and HPF_2 has the transfer function X(s). H(S) is the usual phase transfer function for a second order PLL.

The type of signal that will most strongly interact with the PLL/HPF model is an NRZ data stream that has been directly phase-modulated onto the carrier. Such a condition could prevail for nonstandard bent-pipe modulations that do not employ a subcarrier. The NRZ modulating signal, therefore, must have its data rate and transition density constrained by the maximum allowable effects of the data stream on the PLL tracking performance; i.e., the modulation-produced sidebands of the carrier falling within the PLL tracking bandwidth must be constrained. Since the PLL 1-H(s) transfer function is established by other acquisition and tracking requirements, it is the given condition upon which the data stream restrictions must be based.

The first consideration is that NRZ data directly modulated onto the carrier will give rise to a PLL phase jitter component due to modulation sideband tracking. Let the form of the signal input to the PLL be given by:

$$\begin{aligned} S(t) &= \sqrt{2P_T}\cos\left[\omega_c t + \theta + \beta d(t)\right] \\ &= \sqrt{2P_T}\cos\beta\cos\left[\omega_c t + \theta\right] - \sqrt{2P_T}\sin\beta\sin\left[\omega_c t + \theta\right] \\ &= \sqrt{2P_c}\cos\left[\omega_c t + \theta\right] - \sqrt{2P_d}\sin\left[\omega_c t + \theta\right], \end{aligned} \tag{12}$$

where θ is an arbitrary (random) phase angle. The left-hand term in (12) is the discrete carrier component which the PLL locks onto and tracks, while the right-hand term is the information-bearing component which gives rise to sidebands of the carrier that fall within the PLL tracking bandwidth, causing phase jitter. d(t) is the NRZ data stream with bit rate R_b and having the one-sided power density spectrum:

$$G_d(f) = \frac{2}{R_b}\,Sa^2\left[\frac{\pi}{R_b}f\right] \tag{13}$$

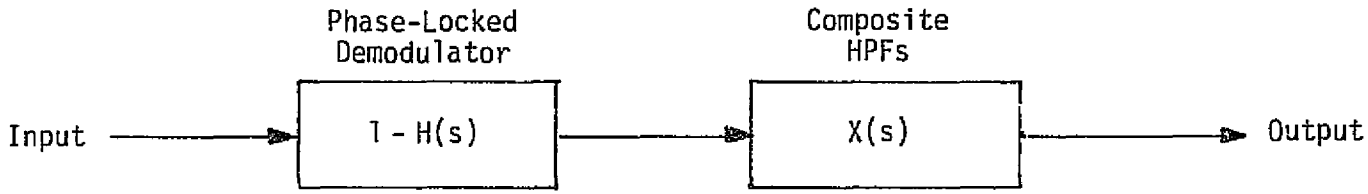

Figure 30. PI Receiver Highpass Analytical Model

Now, the amount of data power tracked by the PLL with transfer function H(f) is:

$$\text{Power Tracked} = P_d \int_0^\infty G_d(f)\, H(f)\, H(-f)\, df \tag{14}$$

For a second-order loop with passive filter and large loop gain,

$$H(f) = \frac{-j2\zeta f_n f - f_n^2}{f^2 - j2\zeta f_n f - f_n^2} \tag{15}$$

where ζ is the loop damping factor, and f_n is the loop natural frequency. Taking $\zeta = \sqrt{2}/2$ (the usual practice), f_n may be related to the two-sided loop noise bandwidth, $2B_L \triangleq W_L$, by

$$f_n = \frac{\sqrt{2}}{3\pi} W_L \tag{16}$$

This is convenient as the two-sided loop noise bandwidth is the parameter usually specified for the loop design.

Substituting (15) and (13) into (14) yields:

$$\text{Power Tracked} = \frac{2R_b P_d}{\pi 2} \int_0^\infty \frac{\left[2f_n^2 f^2 + f_n^4\right] \sin^2\left(\frac{\pi}{R_b} f\right)}{f^2\left(f^4 + f_n^4\right)} df \tag{17}$$

Evaluation of the integral using tables is straightforward, giving the result:

$$\begin{aligned}\text{Power Tracked} = {} & \frac{3}{2}\frac{R_b}{W_L} P_D \left\{1 - \exp\left(-\frac{2}{3}\frac{W_L}{R_b}\right)\left[\cos\left(\frac{2}{3}\frac{W_L}{R_b}\right) + \sin\left(\frac{2}{3}\frac{W_L}{R_b}\right)\right]\right\} \\ & + P_D \\ & - \frac{3}{4}\frac{R_b}{W_L} P_D \left\{1 - \exp\left(-\frac{2}{3}\frac{W_L}{R_b}\right)\left[\cos\left(\frac{2}{3}\frac{W_L}{R_b}\right) - \sin\left(\frac{2}{3}\frac{W_L}{R_b}\right)\right]\right\}\end{aligned} \tag{18}$$

Equation (18) is rather cumbersome; fortunately, it simplifies when $R_b >> W_L$ (the practical case of interest) to the form:

$$\text{Power Tracked} \cong P_d W_L / R_b \tag{19}$$

The loop phase noise due to modulation tracking is simply given by the expression

$$\sigma_\phi^2 = \frac{1}{P_c} \times (\text{Power Tracked}) \qquad (20)$$

when $\sigma_\phi < 20°$ (rms). Using the relationships established by (12), (20) may be rewritten as

$$\sigma_\phi^2 = \left[\frac{W_L}{R_b}\right] \tan^2 (\beta) \qquad (21)$$

The data rate restriction may now be established. Total loop phase jitter is usually comprised of three components arising from (1) additive noise, (2) oscillator instability, and (3) modulation sideband tracking. The rms value of that caused by the noise is less than 15° for a properly designed tracking/demodulation loop, and that contributed by oscillator instability is between 1° and 5°. If the total jitter is to be less than 20°, which represents the upper limit of good engineering practice, the modulation-induced component will have to be 10° or less. Taking, then, $\sigma_\phi = 10°$, together with $W_L = 1460$ Hz (TRW design value) and $\beta = 1.1$ radian (NASA specification), the data rate restriction is established using (21) as:

$$R_b \geq 185 \text{ kbps.}$$

There is a second consideration that gives rise to another restriction on the data stream d(t), that of data transition density. With reference to (12), when d(t) is balanced and has a high transition density, the PLL tracks the carrier phase θ. If, however, the transitions of d(t) cease for a period of time, say $d(t) \equiv 1$, then the PLL slews to the phase $\theta + \beta$. This causes the demodulated data waveform to decay to zero, a very undesirable condition. The result is loss of effective data power. As this quantity is currently not specified for the overall receiver or system performance, Axiomatix believes a reasonable specification is that the maximum data power lost due to demodulation reference slewing be no greater than 0.5 dB for worst-case conditions. This corresponds to a maximum phase slewing of 18° and, for $R_b = 185$ kbps, the maximum number of transitionless bits allowed to maintain slewing less than 18° is 30 bits.

5.4.3 Calculation of Output HPF 3 dB Frequency

Given the data stream characteristics established above, the output HPF 3 dB frequency may now be determined. The basis for calculation of the 3 dB frequency is that of average power lost by the NRZ data stream due to the highpass filtering effects (i.e., attenuation of the very low frequency components). Again, the amount of performance loss to be allowed is somewhat subjective but, abiding by past engineering practice, the degradation should probably not exceed 0.1 dB.

Assume the HPF transfer function is given by:

$$X(f) = \left(\frac{f}{f_0}\right)^2 \left[1 + j\left(\frac{f}{f_0}\right)\right]^{-2} \qquad (22)$$

where f_0 is the 3 dB frequency for each of the cascade HPFs (HPF_1 and HPF_2). (The individual filter time constants have been taken as identical.) The fraction of data power passed by the HPF is then obtained by evaluating the integral:

$$2\int_0^\infty |X(f)|^2 \, G_d(f) \, df \, .$$

Substituting (13) and (22) into the integrand, and evaluating the integral yields:

$$\text{Fraction of Power Passed} = \exp\left(-\frac{2\pi f_0}{R_b}\right) \qquad (23)$$

Taking, then, the 0.1 dB loss criterion which results in the fraction of power passed of 0.977, together with $R_b = 185$ kbps, the 3 dB frequency of each filter section is calculated to be 678 Hz.

5.4.4 Summary

Direct carrier modulation of the carrier by NRZ data should not introduce more than 10° rms phase jitter in the PI receiver PLL, and the maximum phase reference slewing due to periods of transitionless data should not exceed 18°. For the TRW maximum PLL noise bandwidth design value of 1460 Hz, the data stream restrictions are:

(1) $R_b > 185$ kbps, and

(2) Maximum string of no-transition bits = 30 for the bit rate of 185 kbps.

Additionally, the HPF following the PLL should not introduce any more than -0.1 dB of data power loss; therefore, the 3 dB frequency of each of the two cascade HPFs should be less than 678 Hz.

5.5 Unaided Frequency Acquisition Performance of Polarity-Type Costas Loops with Imperfect Integrating Loop Filters

5.5.1 Introduction

Considerable attention [4-8] has recently been directed toward obtaining a complete understanding of the performance of the Costas loop with hard-limited in-phase channel (polarity-type Costas loop) (Figure 31a) relative to that of the more conventional Costas loop (Figure 31b). The principal reason for all this activity stems from the fact that the polarity-type loop offers considerable implementation advantage over the conventional loop with regard to the reduction of dc voltages which appear at the error control point apart from those attributable to the loop phase error itself. In particular, by hard-limiting the output of the in-phase channel arm filter, the analog multiplier used in the conventional Costas loop to form the error signal can be replaced by a chopper or switching-type multiplier which typically exhibits considerably improved dc offset properties.

Until now, attention has been primarily focused on the tracking and false lock behavior of such polarity-type loops with specific results being obtained for single-pole (RC) arm filters and both NRZ and Manchester data formats [4-8]. In particular, it has been shown that, for large signal-to-noise ratio applications, e.g., uncoded data links, the polarity-type loop offers slightly improved tracking performance (as measured, for example, by the loop's rms phase error) over the conventional loop with, however, a small penalty in margin against false lock. The only major question which remains, in order to complete the performance characterization, is: How well does the loop acquire from the standpoint of both frequency acquisition range and acquisition time?

This report presents a theoretical analysis of such acquisition performance behavior for polarity-type Costas loops without acquisition aids of any type. Specific numerical results are presented as before for the case of single-pole arm filters and both NRZ and Manchester data formats. The acquisition time performance of polarity-type Costas loops operating in the frequency search mode is the subject of a future report.

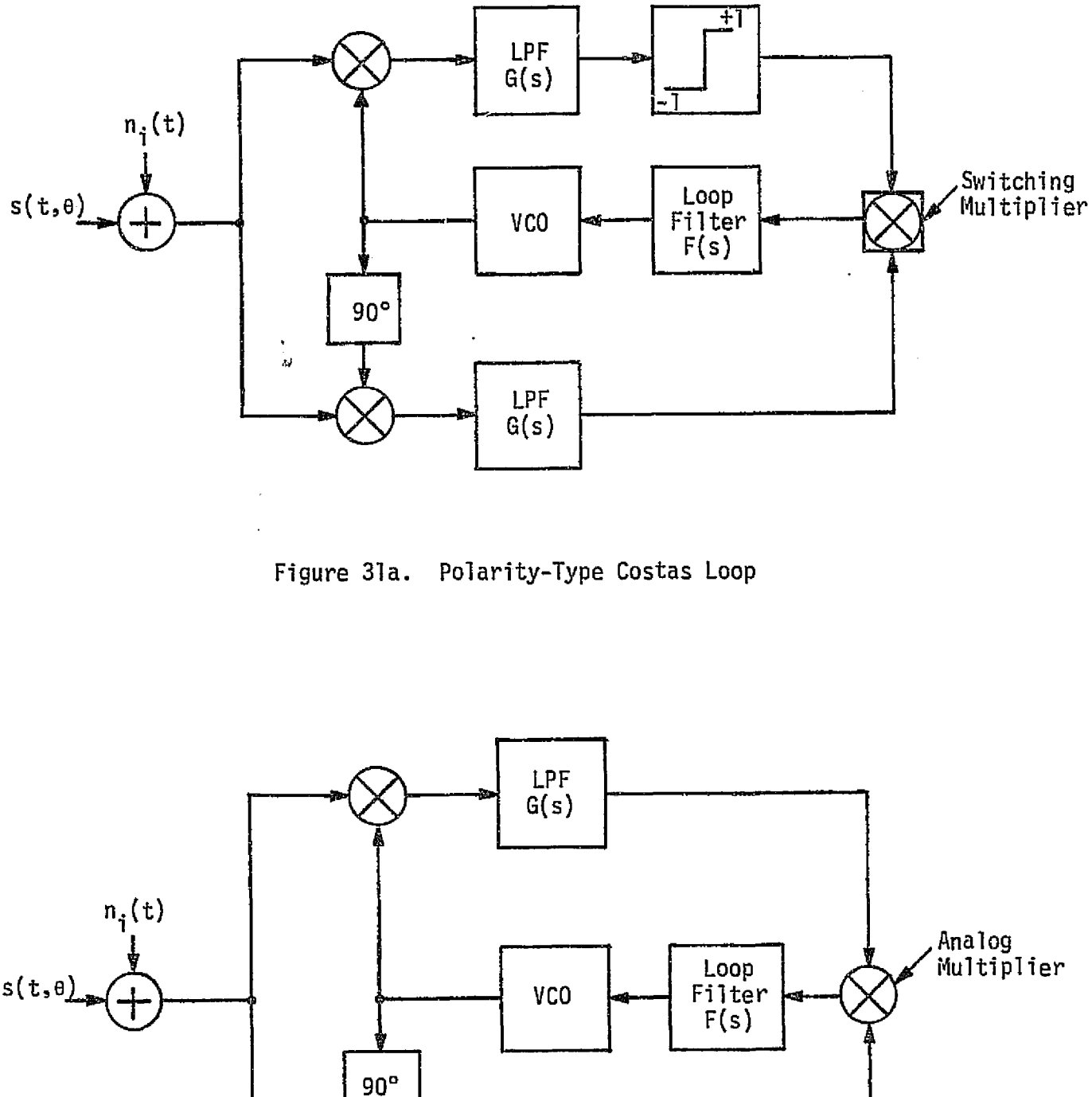

Figure 31a. Polarity-Type Costas Loop

Figure 31b. Conventional Costas Loop

5.5.2 Frequency Acquisition Range of Second-Order Polarity-Type Costas Loops with Imperfect Integrating Loop Filters

The literature abounds with discussions and results pertaining to the frequency acquisition performance of unaided second-order phase-locked loops operating in the absence of noise [9-15]. In some cases, these results have been generalized so as to correspond to tracking systems with an arbitrary periodic phase detector characteristic [9,16-19]. It is these generalized results which are useful in assessing the acquisition performance of both conventional and polarity-type Costas loops with those given in [18], perhaps the most convenient to use from the standpoint of performing numerical computations. In particular, it is shown in [18] that, for a second-order tracking loop with arbitrary periodic phase detector characteristic g(x) and imperfect integrating loop filter, the normalized pull-in range γ_m, in the absence of noise, is given by

$$\gamma_m \triangleq \frac{\Omega_m}{AKF_0} = 2\left[\frac{\langle g^2(x)\rangle}{F_0} + \frac{\langle x\, g(x)\rangle}{r} + \left(\frac{\pi F_0}{r}\right)^2\right]^{1/2} - \frac{2\pi F_0}{r}, \tag{24}$$

where Ω_m is the unnormalized radian pull-in frequency in rad/sec, A^2 is the power of the synchronizing signal, K is the open loop gain, $F_0 \triangleq \tau_2/\tau_1$ is the ratio of time constants of the imperfect integrating loop filter

$$F(s) = \frac{1+\tau_2 s}{1+\tau_1 s}, \tag{25}$$

and $r \triangleq AKF_0\tau_2$ is a parameter proportional to the loop damping. Also in (1), the symbol $\langle\cdot\rangle$ denotes the average of the enclosed quantity on the interval $-\pi \le x \le \pi$. Thus, for example,

$$\langle g^2(x)\rangle = \frac{1}{2\pi}\int_{-\pi}^{\pi} g^2(x)\, dx$$

$$\langle x\, g(x)\rangle = \frac{1}{2\pi}\int_{-\pi}^{\pi} x\, g(x)\, dx. \tag{26}$$

When $F_0 << 1$ (as is the usual high gain second-order loop case), then (24) reduces to the simple well-known result [9, p. 463]:

$$\frac{\Omega_m}{AKF_0} \cong 2\sqrt{\frac{\langle g^2(x)\rangle}{F_0}} \ . \tag{27}$$

It is convenient when comparing loops with different phase detector characteristics to normalize the expressions for pull-in range of (24) and (27) to the loop noise bandwidth rather than AKF_0 Since for a second-order loop, the single-sided loop bandwidth B_L is given by

$$B_L = \frac{r+1}{4\tau_2\left[1+\frac{F_0}{r}\right]} \cong \frac{r+1}{4\tau_2} \ , \tag{28}$$

the latter approximation being valid when $F_0 << r$, then from (28) and the definition of r, we have that

$$AKF_0 = \frac{r}{\tau_2} = 4B_L\left(\frac{r}{r+1}\right)\left(1+\frac{F_0}{r}\right) \cong 4B_L\left(\frac{r}{r+1}\right). \tag{29}$$

Substituting (29) into (24) and (27) and letting $\Omega_m = 2\pi f_m$, we get the desired normalized results.

$$\frac{f_m}{B_L} = \frac{4}{\pi}\left(\frac{r}{r+1}\right)\left(1+\frac{F_0}{r}\right)\left\{\left[\frac{\langle g^2(x)\rangle}{F_0}+\frac{\langle x\,g(x)\rangle}{r}+\left(\frac{\pi F_0}{r}\right)^2\right]^{1/2}-\frac{\pi F_0}{r}\right\}$$

$$\frac{f_m}{B_L} = \frac{4}{\pi}\left(\frac{r}{r+1}\right)\sqrt{\frac{\langle g^2(x)\rangle}{F_0}} \ ; \quad F_0 << 1 \ . \tag{30}$$

For a conventional Costas loop, $x = 2\varphi$, $g(x) = \sin 2\varphi$, and $f_m = 2f_{acq}$, where f_{acq} is the actual pull-in or frequency acquisition range of the loop. Thus,

$$\langle g^2(x)\rangle = \frac{1}{2\pi}\int_{-\pi}^{\pi} \sin^2 x\, dx = \frac{1}{2}$$

$$\langle x\, g(x)\rangle = \frac{1}{2\pi}\int_{-\pi}^{\pi} x \sin x\, dx = 1. \tag{31}$$

and,

$$\frac{f_{acq}}{B_L} = \frac{2}{\pi}\left(\frac{r}{r+1}\right)\left(1+\frac{F_0}{r}\right)\left\{\left[\frac{1}{2F_0}+\frac{1}{r}+\left(\frac{\pi F_0}{r}\right)^2\right]^{1/2} - \frac{\pi F_0}{r}\right\}$$

$$\frac{f_{acq}}{B_L} \cong \frac{1}{\pi}\left(\frac{r}{r+1}\right)\sqrt{\frac{2}{F_0}}\ ; \qquad F_0 << 1\ . \tag{32}$$

For the polarity-type Costas loop in the absence of noise, we have $x = 2\varphi$, $g(x) = 2\sin\varphi\ \mathrm{sgn}\ (\cos\varphi)$, and $f_m = 2\, f_{acq}$. Thus,

$$\langle g^2(x)\rangle = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left[2\sin\frac{x}{2}\ \mathrm{sgn}\ \left(\cos\frac{x}{2}\right)\right]^2 dx$$

$$= \frac{2}{\pi}\int_{-\pi}^{\pi}\sin^2\frac{x}{2}\, dx = 2$$

$$\langle x\, g(x)\rangle = \frac{1}{2\pi}\int_{-\pi}^{\pi} x\left[2\sin\frac{x}{2}\ \mathrm{sgn}\ \left(\cos\frac{x}{2}\right)\right] dx$$

$$= \frac{1}{\pi}\int_{-\pi}^{\pi} x\sin\frac{x}{2}\, dx = \frac{8}{\pi} \tag{33}$$

and

$$\frac{f_{acq}}{B_L} = \frac{2}{\pi}\left(\frac{r}{r+1}\right)\left(1+\frac{F_0}{r}\right)\left\{\left[\frac{2}{F_0}+\frac{8}{\pi r}+\left(\frac{\pi F_0}{r}\right)^2\right]^{1/2} - \frac{\pi F_0}{r}\right\}$$

$$\frac{f_{acq}}{B_L} \cong \frac{2}{\pi}\left(\frac{r}{r+1}\right)\sqrt{\frac{2}{F_0}}\ ; \qquad F_0 << 1\ . \tag{34}$$

Comparing (32) and (34), we observe that, in the absence of noise and $F_0 << 1$, polarity-type Costas loops have twice the acquisition range (for the same loop bandwidth) as the conventional Costas loop.

When noise is present, the phase detector characteristic of the polarity-type loop is affected because of the signal amplitude suppression caused by the low-pass limiter in the in-phase arm. By contrast, the phase detector characteristic of the conventional Costas loop is unaffected by the presence of additive noise at the loop input. Thus, to a first approximation, we can account for the effect of noise on the frequency acquisition performance of the polarity-type Costas loop by treating the loop as though it were free of additive noise but possessing a phase detector characteristic which is signal-to-noise ratio dependent. A comparison of the resulting performance with that of the noise-free conventional Costas loop would then render an indication as to how the 3 dB improvement in acquisition range achieved by the polarity-type loop in no noise degrades as a function of signal-to-noise ratio. (This is not to say that the additive effect of noise on acquisition performance is the same for both loops; in fact, it is undoubtedly quite different. Unfortunately, however, the formulas for frequency acquisition range in (30) do not account for the additive effects of noise and thus cannot show up this difference.)

When noise is present, the equivalent phase detector characteristic of the polarity-type loop is, in addition to being signal-to-noise ratio dependent as mentioned above, also a function of the type of arm filter employed in the loop and the data format of the input signal.

5.5.2.1 NRZ Data, Single-Pole Arm Filters

For single-pole arm filters in the loop and NRZ data, the phase detector characteristic (normalized to unit slope at $\varphi = 0$) is given by

$$g(x) = \frac{f(2\varphi)}{\tilde{\alpha}} \triangleq f_1(2\varphi), \tag{35}$$

where $\tilde{\alpha}$ is the signal amplitude suppression factor which results due to the combined distortion effects on the input modulation of the hard-limiter and finite arm filter bandwidth [7, Eq. (14)], and $f(2\varphi)$ is the unnormalized loop nonlinearity defined just above Eq. (14) of [7]. In particular [6,7]:*

$$\tilde{\alpha} \triangleq \left.\frac{df(2\varphi)}{d(2\varphi)}\right|_{\varphi=0} = \frac{1}{2}\left\{\frac{2}{\omega_c T}\int_0^{\tanh \omega_c T/2}\left(\frac{y}{1-y^2}\right)\operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\,y\right]dy + \operatorname{erf}\sqrt{\frac{\rho_i}{2}}\right\}$$

$$= \frac{1}{2}\operatorname{erf}\sqrt{\frac{\rho_i}{2}} + \frac{1}{2}\left[1 - \frac{2}{\omega_c T}\ln\left(\frac{2}{1+e^{-\omega_c T}}\right)\right]\operatorname{erf}\left(\sqrt{\frac{\rho_i}{2}}\tanh\frac{\omega_c T}{2}\right)$$

$$+ \frac{1}{2\omega_c T}\sqrt{\frac{2\rho_i}{\pi}}\int_0^{\tanh \omega_c T/2}\ln(1-x^2)\exp\left(-\frac{\rho_i x^2}{2}\right)dx\,, \tag{36}$$

where $\omega_c = 2\pi f_c$ is the radian 3 dB cutoff frequency of the single-pole arm filter, $R_s = 1/T$ is the data symbol rate, and $\rho_i \triangleq 2S/N_0B_i$ is the signal-to-noise ratio in the two-sided arm filter noise bandwidth B_i. Since, for a single-pole filter, we have that $B_i = \pi f_c$, then in terms of the signal-to-noise ratio in the data bandwidth, namely, $R_d \triangleq ST/N_0$, the parameter ρ_i can be expressed as

$$\rho_i = \frac{2}{\pi}R_d\frac{1}{f_c T}\,. \tag{37}$$

Also, from [8],

$$f(2\varphi) = \sin\varphi\left\{\frac{2}{\omega_c T}\int_0^{\tanh \omega_c T/2}\left(\frac{y}{1-y^2}\right)\operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\,y\cos\varphi\right]dy + \operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\cos\varphi\right]\right\} \tag{38a}$$

or

*The validity of the results which follow requires that $f_c T \geq 1$.

$$f(2\varphi) = \sin\varphi \left\{ \left[1 - \frac{2}{\omega_c T} \ln\left(\frac{2}{1+e^{-\omega_c T}} \right) \right] \operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}} \left(\tanh \frac{\omega_c T}{2} \right) \cos\varphi \right] \right.$$

$$+ \frac{1}{\omega_c T} \sqrt{\frac{2\rho_i}{\pi}} \cos\varphi \int_0^{\tanh \omega_c T/2} \ln(1-y^2)$$

$$\left. \times \exp\left(-\frac{\rho_i}{2} y^2 \cos\varphi \right) dy + \operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}} \cos\varphi \right] \right\}. \qquad (38b)$$

Substituting (36) and (38) in (35) gives g(x) as a function of R_d and $f_c T$ (or B_i/R_s) from which the frequency acquisition range can be computed by calculating the averages required in (30).

Figure 32 illustrates f_{acq}/B_L versus B_i/R_s ($\pi f_c T$) with R_d in dB as a parameter for $r = 2$ and $F_0 = 0.002$. The no-noise ($R_d = \infty$) value of $f_{acq}/B_L = 13.42$ for the polarity-type loop is obtained from (34). The corresponding value for the conventional loop is $f_{acq}/B_L = 6.71$ as given by (32). Note from Figure 32 that, for a fixed loop bandwidth, the polarity-type loop always has a greater frequency acquisition range than the conventional Costas loop. To prove this statement analytically, note that

$$\lim_{\substack{f_c T \text{ large} \\ R_d \text{ fixed}}} \tilde{\alpha} = \operatorname{erf} \sqrt{\frac{\rho_i}{2}}$$

$$\lim_{\substack{f_c T \text{ large} \\ R_d \text{ fixed}}} \langle f^2(2\varphi) \rangle = \frac{1}{2\pi} \int_{-\pi}^{\pi} \sin^2 \frac{x}{2} \operatorname{erf}^2 \left[\sqrt{\frac{\rho_i}{2}} \cos \frac{x}{2} \right] dx$$

$$= \frac{8}{\pi} \int_0^{\pi/2} \sin^2 z \operatorname{erf}^2 \left[\sqrt{\frac{\rho_i}{2}} \cos z \right] dz . \qquad (39)$$

Thus, from (35),

$$\lim_{\substack{f_c T \text{ large} \\ R_d \text{ fixed}}} \langle g^2(x) \rangle = \frac{\frac{8}{\pi} \int_0^{\pi/2} \sin^2 z \operatorname{erf}^2 \left[\sqrt{\frac{\rho_i}{2}} \cos z \right] dz}{\operatorname{erf}^2 \sqrt{\frac{\rho_i}{2}}} . \qquad (40)$$

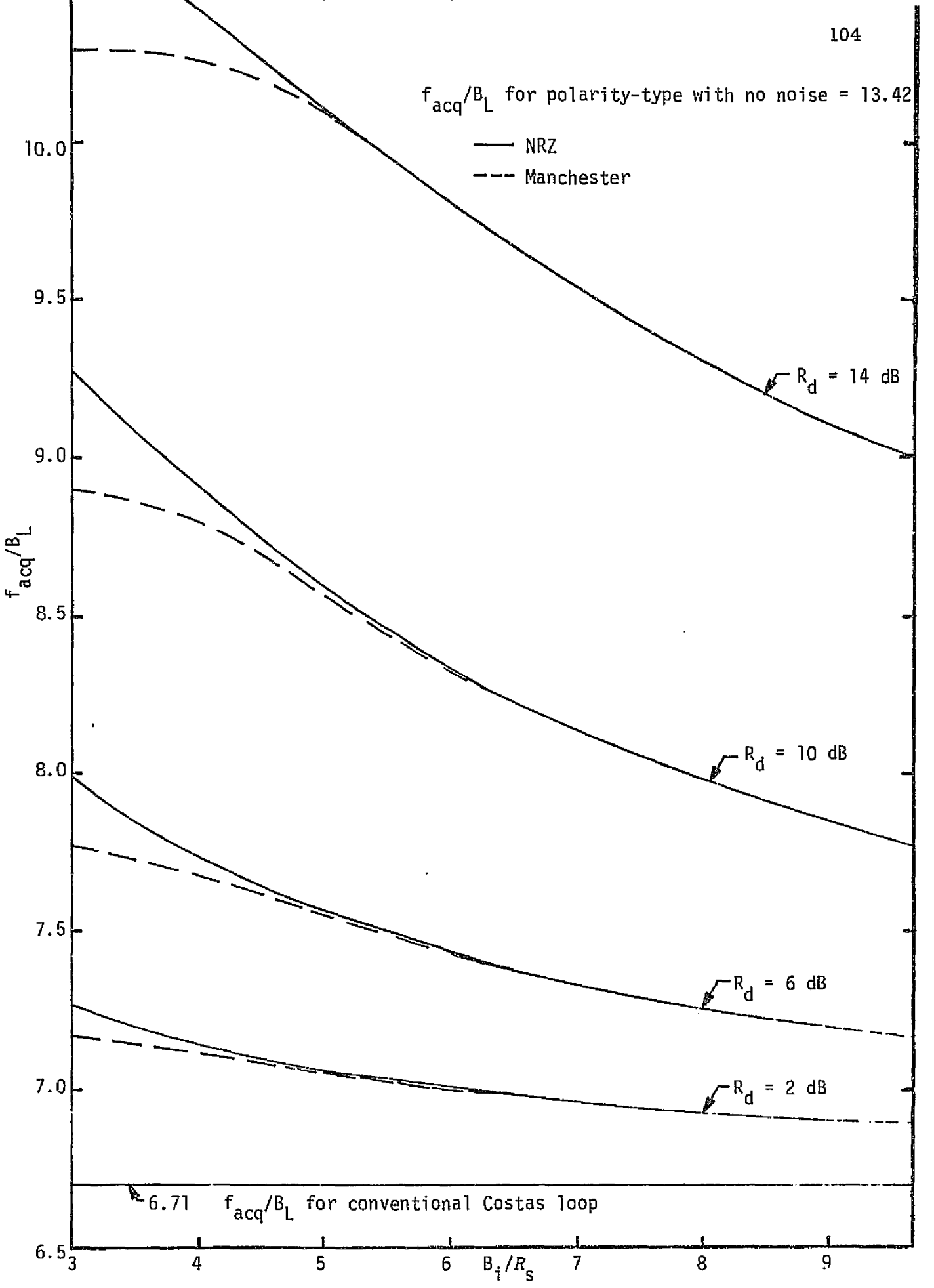

Figure 32. Normalized Frequency Acquisition Range vs. Ratio of Two-Sided Arm Filter Bandwidth to Data Rate; $F_0 = 0.002$, $r = 2$

For small values of its argument,

$$\text{erf } x \cong \frac{2}{\sqrt{\pi}} x \,. \tag{41}$$

Substituting (41) into (40) gives

$$\lim_{\substack{f_c T \text{ large} \\ R_d \text{ fixed}}} \langle g^2(x) \rangle = \frac{\frac{8}{\pi} \int_0^{\pi/2} \sin^2 z \left(\frac{4}{\pi} \left(\frac{\rho_i}{2} \right) \cos^2 z \right) dz}{\frac{4}{\pi} \left(\frac{\rho_i}{2} \right)}$$

$$= \frac{8}{\pi} \int_0^{\pi/2} \frac{\sin^2 2z}{4} dz = \frac{1}{2} \,, \tag{42}$$

which is the value of $\langle g^2(x) \rangle$ previously obtained for the conventional Costas loop. Thus, considering only the effect of noise on the equivalent phase detector characteristic of the polarity-type Costas loop, we observe from (42) that all the curves in Figure 32 approach $f_{acq}/B_L = 6.71$ as B_i/R_s becomes large, which is the ratio of frequency acquisition range to loop bandwidth for the conventional Costas loop.

5.5.2.2 Manchester Data, Single-Pole Arm Filters

For Manchester data and single-pole arm filters, g(x) is still given by (35) with, however [4,5]:

$$\tilde{\alpha} = \frac{1}{2} \left\{ \frac{2}{\omega_c T} \int_0^{\tanh \omega_c T/2} \left(\frac{y}{1 - y^2} \right) \text{erf} \left[\sqrt{\frac{\rho_i}{2}} \, y \right] dy \right.$$

$$\left. + \frac{4}{\omega_c T} \int_0^{\tanh \omega_c T/4} \left(\frac{y}{1 - y^2} \right) \text{erf} \left[\sqrt{\frac{\rho_i}{2}} \, y \right] dy \right\} \tag{43a}$$

or

$$\tilde{\alpha} = \frac{1}{2}\left[1 - \frac{2}{\omega_c T}\ln\left(\frac{2}{1+e^{-\omega_c T}}\right)\right]\operatorname{erf}\left(\sqrt{\frac{\rho_i}{2}}\tanh\frac{\omega_c T}{2}\right)$$

$$+ \frac{1}{2\omega_c T}\sqrt{\frac{2\rho_i}{\pi}}\int_0^{\tanh \omega_c T/2}\ln(1-x^2)\exp\left(-\frac{\rho_i x^2}{2}\right)dx$$

$$+ \frac{1}{2}\left[1 - \frac{4}{\omega_c T}\ln\left(\frac{2}{1+e^{-\omega_c T/2}}\right)\right]\operatorname{erf}\left(\sqrt{\frac{\rho_i}{2}}\tanh\frac{\omega_c T}{4}\right)$$

$$+ \frac{1}{\omega_c T}\sqrt{\frac{2\rho_i}{\pi}}\int_0^{\tanh \omega_c T/4}\ln(1-x^2)\exp\left(-\frac{\rho_i x^2}{2}\right)dx\,, \qquad (43b)$$

and

$$f(2\varphi) = \sin\varphi\left\{\frac{2}{\omega_c T}\int_0^{\tanh \omega_c T/2}\left(\frac{y}{1-y^2}\right)\operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\,y\cos\varphi\right]dy\right.$$

$$\left. + \frac{4}{\omega_c T}\int_0^{\tanh \omega_c T/4}\left(\frac{y}{1-y^2}\right)\operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\,y\cos\varphi\right]dy\right\}$$

$$= \sin\varphi\left\{\left[1 - \frac{2}{\omega_c T}\ln\left(\frac{2}{1+e^{-\omega_c T}}\right)\right]\operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\left(\tanh\frac{\omega_c T}{2}\right)\cos\varphi\right]\right.$$

$$+ \frac{1}{\omega_c T}\sqrt{\frac{2\rho_i}{\pi}}\cos\varphi\int_0^{\tanh \omega_c T/2}\ln(1-y^2)$$

$$\times \exp\left(-\frac{\rho_i}{2}y^2\cos^2\varphi\right)dy$$

$$+ \left[1 - \frac{4}{\omega_c T}\ln\left(\frac{2}{1+e^{-\omega_c T}}\right)\right]\operatorname{erf}\left[\sqrt{\frac{\rho_i}{2}}\left(\tanh\frac{\omega_c T}{4}\right)\cos\varphi\right]$$

$$+ \frac{2}{\omega_c T}\sqrt{\frac{2\rho_i}{\pi}}\cos\varphi\int_0^{\tanh \omega_c T/4}\ln(1-y^2)$$

$$\left.\times \exp\left(-\frac{\rho_i}{2}y^2\cos^2\varphi\right)dy\right\}. \qquad (44)$$

Superimposed in dashed lines on Figure 32 are the frequency acquisition range results for Manchester coded data as computed from (7) together with (35), (43), and (44). We observe that, in all cases, the frequency acquisition range for Manchester coded data is worse than that for NRZ data, with the two results approaching each other as B_i/R_s becomes large.

5.5.3 Frequency Acquisition Time Performance of Second-Order Polarity-Type Costas Loops with Imperfect Integrating Loop Filter

Many of the same references cited in the beginning of the previous section also treat frequency acquisition time performance. Here again, the results given in [15] are most useful for our purposes here. In particular, it is shown in [15] that, for a second-order tracking loop with arbitrary period phase detector characteristic g(x) and imperfect integrating loop filter, the normalized frequency acquisition time τ_f is given by

$$\tau_f \triangleq AKF_0T_f = \frac{r}{F_0}\left\{\ln\left(\frac{\gamma}{\lambda}\right) + \left[\frac{2\pi F_0}{r} + \gamma\left(1+\frac{P}{Q}\right)\right] \times \frac{\left[\tan^{-1}\left(\frac{\gamma}{R}\right) - \tan^{-1}\left(\frac{2\lambda-\gamma}{R}\right)\right]}{R} + \frac{1}{2}\left(1-\frac{P}{Q}\right)\ln\left[\frac{\lambda^2 Q}{\gamma^2(\lambda^2-\gamma\lambda+Q)}\right]\right\}. \quad (45)$$

where T_f is the unnormalized frequency acquisition time in seconds and

$$\lambda \triangleq 1.3 \max_x g(x); \qquad \gamma \triangleq \frac{\Omega}{AKF_0};$$

$$P \triangleq \langle g^2(x)\rangle + \frac{1}{r}(2F_0-1)\langle x\,g(x)\rangle - \frac{\pi\gamma F_0}{r} + \frac{1}{2}\left(\frac{2\pi F_0}{r}\right)^2;$$

$$Q \triangleq \frac{\langle g^2(x)\rangle}{F_0} + \frac{\langle x\,g(x)\rangle}{r} - \frac{\pi\gamma F_0}{r}; \quad R \triangleq \sqrt{4Q-\gamma^2}, \quad (46)$$

with $\Omega \leq \Omega_m$ denoting the radian frequency offset. Once again, it is convenient to normalize T_f with respect to the loop bandwidth B_L. Thus, using the relations,

$$T_f B_L = \tau_f \left(\frac{r+1}{r}\right) \left[\frac{1}{4\left(1+\frac{F_0}{r}\right)}\right]$$

$$\gamma = \frac{\Omega}{4 B_L} \left(\frac{r+1}{r}\right) \left[\frac{1}{1+\frac{F_0}{r}}\right] , \tag{47}$$

(45) can be rewritten as

$$T_f B_L = \frac{C_1}{2} \left\{ \ln \left(\frac{C_1 C_2 \frac{\Omega}{4\pi B_L}}{\lambda} \right) + C_2 \left[1 + C_1 \left(1+\frac{P}{Q}\right) \frac{\Omega}{4\pi B_L} \right] \right.$$

$$\times \frac{\left[\tan^{-1} \left(\frac{C_1 C_2 \frac{\Omega}{4\pi B_L}}{R} \right) - \tan^{-1} \left(\frac{2\lambda - C_1 C_2 \frac{\Omega}{4\pi B_L}}{R} \right) \right]}{R}$$

$$\left. + \frac{1}{2}\left(1-\frac{P}{Q}\right) \ln \left[\frac{\lambda^2 Q}{C_1^2 C_2^2 \left(\frac{\Omega}{4\pi B_L}\right)^2 \left(\lambda^2 - C_1 C_2 \lambda \left(\frac{\Omega}{4\pi B_L}\right) + Q\right)} \right] \right\} \tag{48}$$

where we have introduced the constants

$$C_1 \triangleq \frac{r+1}{2 F_0 \left(1+\frac{F_0}{r}\right)} ; \qquad C_2 \triangleq \frac{2\pi F_0}{r} , \tag{49}$$

and thus P, Q, and R can be rewritten as

$$P = \langle g^2(x) \rangle + \left(\frac{C_2}{\pi} - \frac{1}{r}\right) \langle x\, g(x) \rangle - \frac{1}{2} C_1 C_2^2 \left(\frac{\Omega}{4\pi B_L}\right) + \frac{1}{3} C_2^2 \tag{50a}$$

$$Q = \frac{\langle g^2(x) \rangle}{F_0} + \frac{\langle x\, g(x) \rangle}{r} - \frac{1}{2} C_1 C_2^2 \left(\frac{\Omega}{4\pi B_L}\right) \tag{50b}$$

$$R = \sqrt{4Q - C_1^2 C_2^2 \left(\frac{\Omega}{4\pi B_L}\right)^2} \quad . \tag{50c}$$

For a conventional Costas loop, we can use the results of (31) for the averages required in (50). Furthermore, since the maximum value of $g(2\varphi) = \sin 2\varphi$ is 1, then from (46), $\lambda = 1.3$.

For the polarity-type Costas loop, in no noise, the maximum value of $g(2\varphi) = 2 \sin \varphi \operatorname{sgn}(\cos \varphi)$ is 2; thus, $\lambda = 2.6$. When noise is present, the maximum value of $g(2\varphi) = f(2\varphi)/\tilde{\alpha}$ [see (35)] depends on the signal-to-noise ratio, type of arm filter, and data format, and must be determined numerically rather than analytically.

Figure 33 illustrates $T_f B_L$ as computed from (48) versus $\Delta f/B_L = \Omega/4\pi B_L$ for no noise, a damping coefficient $r = 2$, and two values of the ratio of loop filter time constants, namely, $F_0 = 0.001$, 0.01. The values of $\Delta f/B_L$ are, of course, chosen to be less than f_{acq}/B_L since, for $\Delta f = f_{acq}$, $T_f \to \infty$. As was true for frequency acquisition range, the polarity-type Costas loop offers superior acquisition time performance (smaller acquisition time for a fixed frequency offset) relative to the conventional Costas loop. For small frequency offsets (an order of magnitude smaller than the frequency acquisition range), the performance of either loop is essentially insensitive to the value of F_0 (as long as it is small). Figures 34 and 35 illustrate the frequency time acquisition performance in the presence of noise (once again assuming the effect of noise only on the equivalent phase detector characteristic of the polarity-type loop) for NRZ data and RC arm filters.

In Figure 34, $T_f B_L$ is plotted versus $\Delta f/B_L$ for $F_0 = 0.002$, $r = 2$, $R_d = 10$ dB, and B_i/R_s as a parameter. The no-noise curves corresponding to the conventional and polarity-type Costas loops are superimposed on this figure in dashed lines. We observe that, as B_i/R_s becomes large, the frequency acquisition time performance of the polarity-type loop approaches that of the conventional loop. Figure 35, on the other hand, is a plot of $T_f B_L$ versus $\Delta f/B_L$ for $F_0 = 0.002$, $r = 2$, B_i/R_s fixed at a value of 5, and R_d as a parameter. Again, the two noise curves are superimposed in dashed lines for comparison. Again neglecting the additive effects of the noise in

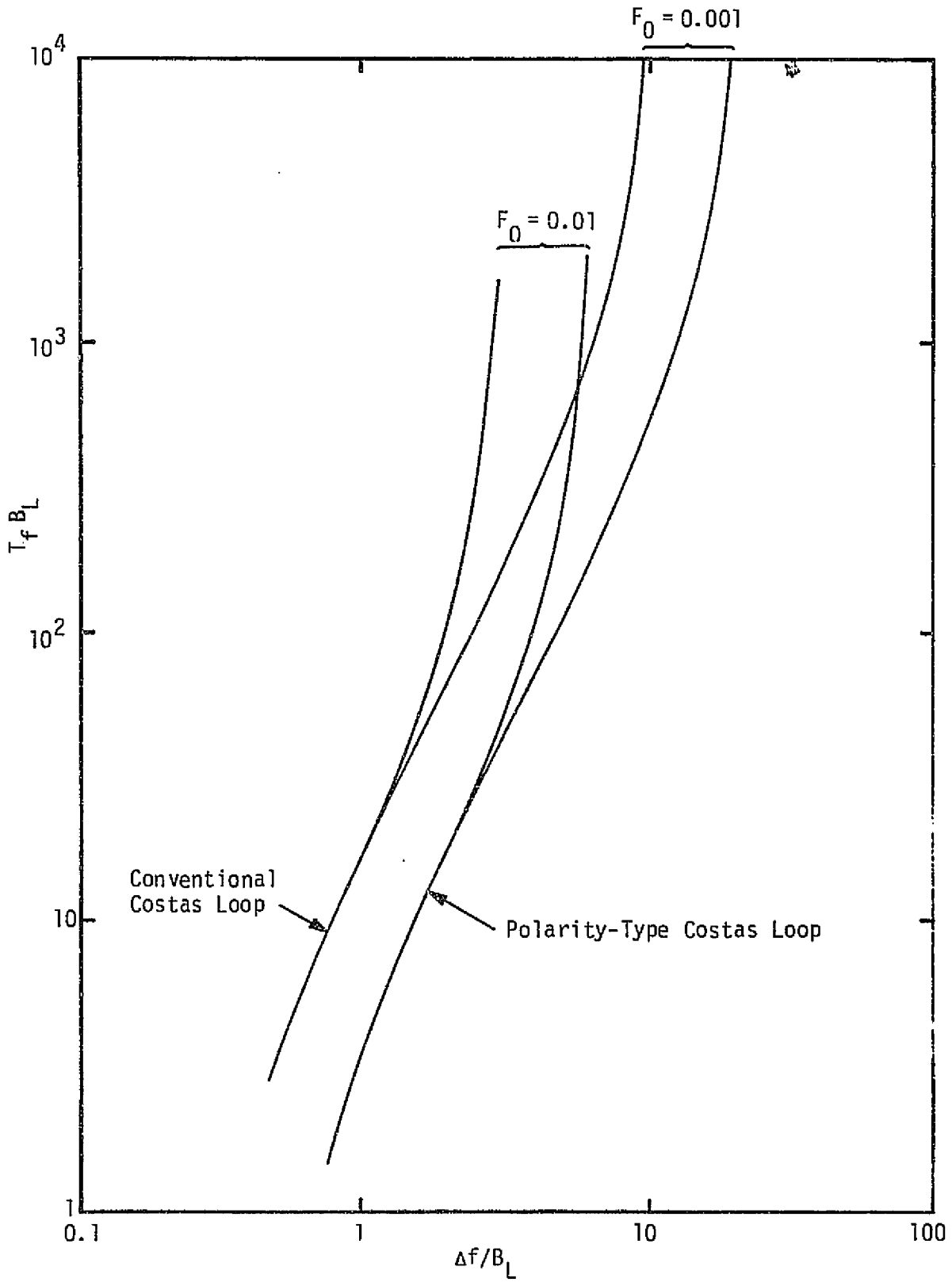

Figure 33. Frequency Acquisition Time Performance of Conventional and Polarity-Type Costas Loops in the Absence of Noise; $r = 2$

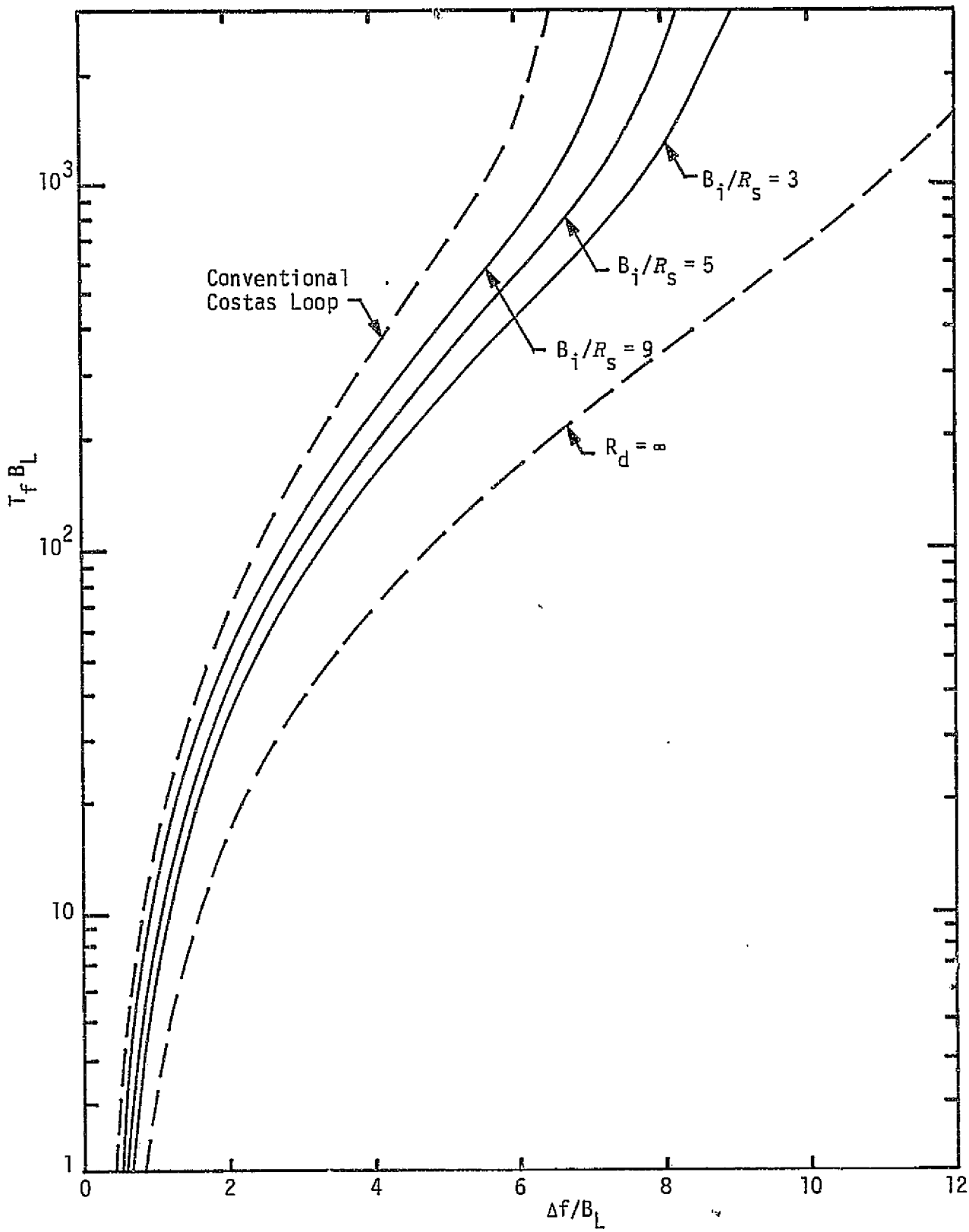

Figure 34. Frequency Acquisition Time Performance of the Polarity-Type Costas Loop in the Presence of Noise; NRZ Data, RC Arm Filters, $F_0 = 0.002$, $r = 2$, $R_d = 10$ dB

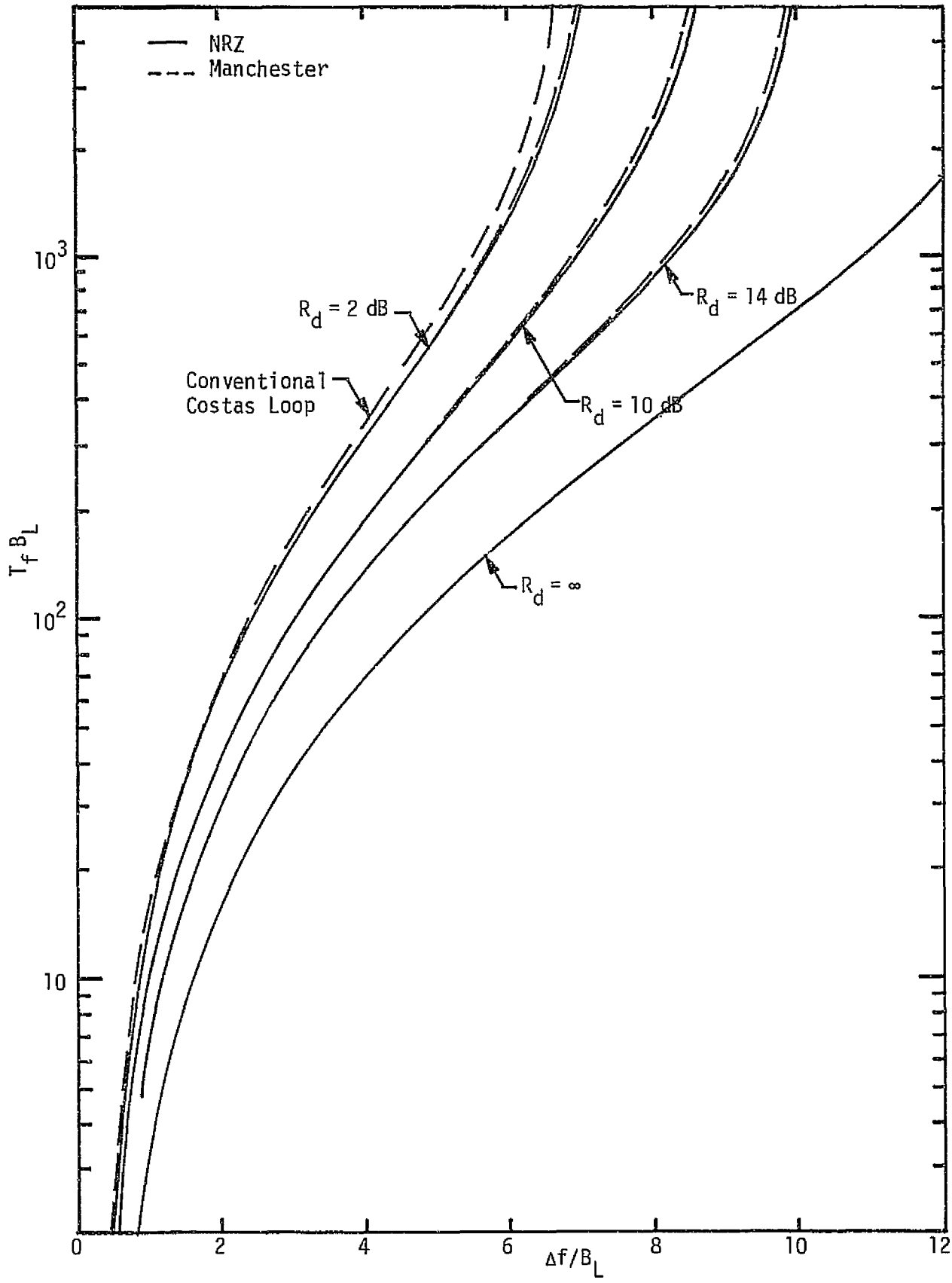

Figure 35. Frequency Acquisition Time Performance of the Polarity-Type Costas Loop in the Presence of Noise; NRZ Data, RC Arm Filters, $F_0 = 0.002$, $r = 2$, $B_i/R_s = 5$

the two loops, we observe that, for small signal-to-noise ratios, the polarity-type loop approaches at worst the frequency acquisition time performance of the conventional loop.

5.5.4 Conclusions

From the results given in this report, we can conclude that, for the high signal-to-noise ratios wherein the dominant effect of the channel noise is its effect on the phase detector characteristics of the polarity-type Costas loop, this loop offers superior frequency acquisition range and frequency acquisition time performance. While the results further indicate that, even at low signal-to-noise ratios, the polarity-type loop outperforms the conventional loop, one must exercise care in drawing definite conclusions for this case, since here the additive effect of the noise is significant and it is not clear that it affects both loops in the same way, i.e., degrades them by the same amount. Since analytical models to determine the frequency acquisition performance of these loops taking into account the additive effects of the noise are not readily available, the answers to such questions must be determined either experimentally or by simulation methods, given an appropriate definition of acquisition in noise.

5.6 Network Transponder Interference Susceptibility

5.6.1 Background

During the summer months of 1978, TRW performed a number of specialized tests to determine the susceptibility of the network transponder to an out-of-band interferer. The results, in the form of computer printouts, were supplied to Axiomatix by both Rockwell and TRW.

The general approach to the test involved stepping the frequency of the interfering signal across a preselected band while the baseband output of the network transponder was monitored and recorded at those frequencies for which either an excessive output (of any nature) or an unlock condition was observed.

In the paragraphs which follow, the specifics of the test setup are described and the significance of the resultant data is discussed.

5.6.2 Functional Description of the Test Setup

Figure 36 shows a functional block diagram of the test setup used for determining the effect of an undesired signal (the interferer) on the performance of the network transponder. As shown, two signal generators were used. Signal generator #1 provided the desired or true signal while signal generator #2 simulated the interferer. For any particular test run, the frequency of generator #1 was selected and remained fixed while the frequency of signal generator #2 was incrementally varied by the computer over the proper frequency range. A notch filter at the output of generator #2 prevented the possible occurrence of an in-band interference component.

The effect of the interfering signal on the performance of the transponder was determined by observing both the baseband output of the transponder wideband phase detector and the receiver AGC voltage. As shown in Figure 36, the transponder wideband output was applied to a spectrum analyzer, the results being recorded by a printer to obtain a permanent record of any spurious outputs.

The frequency of the simulated interferer was stepped in increments of 1 kHz. Whenever the level of the transponder output, as measured by the spectrum analyzer (V_n), exceeded an adaptive threshold, a printout was provided which indicated the interference frequency, the ratio of the

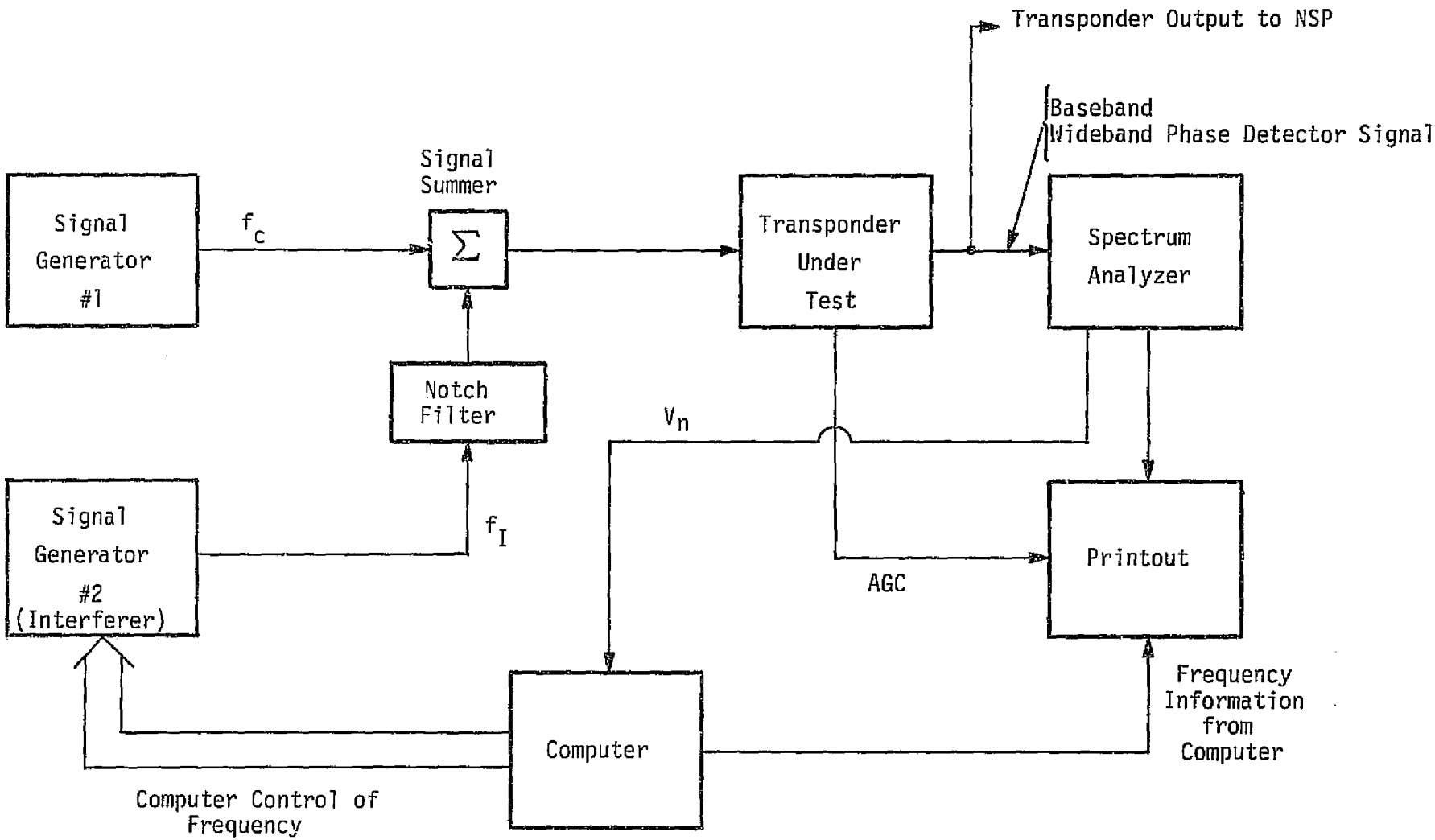

Figure 36. Functional Block Diagram for Interference Test Setup

output level to the threshold level, and the value of V_n. On the other hand, if the receiver lost lock, as measured by a rapid decrease of the AGC voltage, this event was recorded together with the frequency at which it occurred. The printer also made a record of the AGC voltage at 1 MHz increments.

Quantitative parameters for the test were:

(1) Uplink signal = -100 dBm

(2) Interferer = - 15 dBm

(3) Interferer stepped in 1 kHz steps from 1700 MHz to 2400 MHz

(4) Spurious output recorded when $V_n > 1.5\ V_{th}$, where V_{th} is a continuously updated average of the receiver output noise level.

Figure 37 shows a section of a typical printout. As indicated in the figure, there are four columns: the first column indicates the nature of the anomalous behavior while the second column records the frequency at which the anomaly occurs; the third column is the ratio of the output level to the threshold level, and the fourth column shows the value of the parameter V_n.

An equation relating the value of V_n to the output level is:

$$\text{Output Level} = -100\ (0.8 + V_n)\ .\ (\text{dB})$$

As an example, the output level at 1753.281 MHz (first entry on Figure 37) can be computed as:

$$\text{Output Level} = -100\ (0.8 - 0.02)$$
$$= -78\ \text{dB}.$$

5.6.3 Test Result Trends and Interpretations

Figure 38 shows a typical frequency relationship between the unlock responses and the desired signal. For the case of Test A shown on Figure 38, the desired signal is input to the transponder at 2041.9 MHz (STDN-Low frequency). When the transponder is in the STDN-Low frequency mode, the triplexer configuration also allows signals within the SGLS-Low frequency band to reach the receiver. Thus, this explains the unlock region in the vicinity of the 1775.7 MHz SGLS-Low frequency region. On the other hand, the interference in the vicinity of the derived signal is due to direct in-band interference which occurred despite the presence of the notch filter at the output of signal generator #2.

Type of Anomaly	Frequency (MHz)	Output Level to Threshold Level Ratio	V_n
AGC VOLTAGE @ 1753 MHZ =		.0050	
SPUR	@ 1753.281 0 MHZ	1.7750	-.0200
SPUR	@ 1753.282 0 MHZ	2.0333	-.0270
SPUR	@ 1753.283 0 MHZ	2.2293	-.0360
SPUR	@ 1753.284 0 MHZ	2.3162	-.0460
SPUR	@ 1753.285 0 MHZ	2.4529	-.0610
SPUR	@ 1753.286 0 MHZ	2.4920	-.0780
SPUR	@ 1753.287 0 MHZ	2.4886	-.0980
SPUR	@ 1753.288 0 MHZ	2.4075	-.1180
SPUR	@ 1753.289 0 MHZ	2.2569	-.1350
SPUR	@ 1753.290 0 MHZ	2.1301	-.1530
UNLOCKED	@ 1753.291 0 MHZ		
UNLOCKED	@ 1753.292 0 MHZ		
UNLOCKED	@ 1753.306 0 MHZ		
NOISE FLOOR SUPPRESSED IN BAND: 1753-1754 MHZ			
AGC VOLTAGE @ 1754 MHZ =		.0050	
UNLOCKED	@ 1754.414 0 MHZ		
UNLOCKED	@ 1754.433 0 MHZ		
UNLOCKED	@ 1754.452 0 MHZ		
UNLOCKED	@ 1754.512 0 MHZ		
UNLOCKED	@ 1754.529 0 MHZ		
UNLOCKED	@ 1754.617 0 MHZ		
UNLOCKED	@ 1754.636 0 MHZ		
NOISE FLOOR SUPPRESSED IN BAND: 1754-1755 MHZ			

NOTE: This printout was obtained for the following conditions:

Mode: STDN
Frequency: Low
Power: Low

Figure 37. Typical Section of a Printout Chart Showing Spur and Unlock Conditions

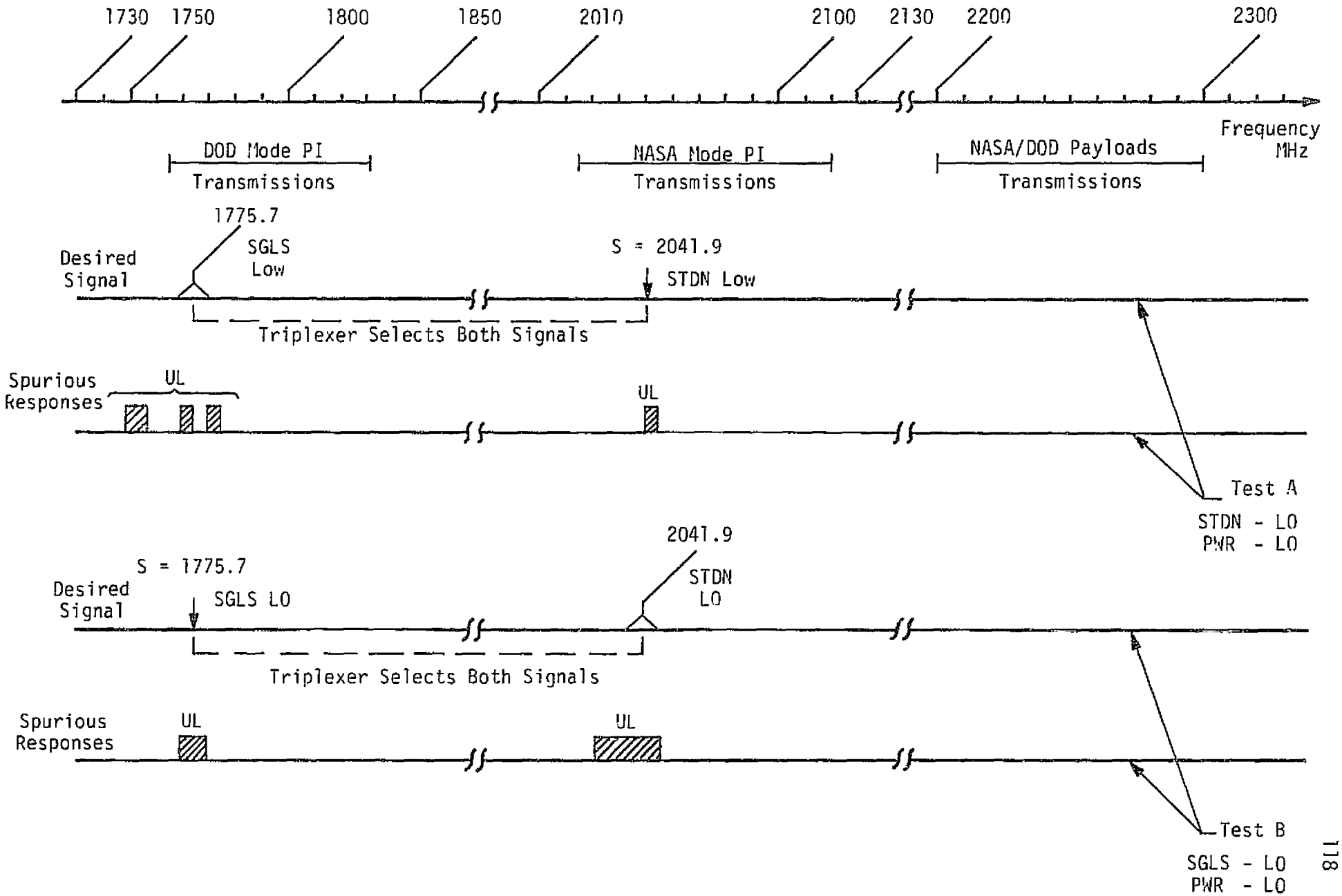

Figure 38. Typical Relationship Between the Unlock Spurious Response and the Desired Signal

The same pattern of interference response is seen in the data provided by Test B. Here the derived signal is applied at the SGLS-Low frequency of 1775.7 MHz, while the companion section of the triplexer is tuned to 2041.9 MHz, the STDN-Low midband frequency. The entire set of tests, which included the various combinations of operating modes, resulted in similar behavior to that just described. Such results, however, are to be expected considering the design philosophy of the transponder's triplexer. Prevention of such "paired" responses would have required a very complex triplexer design.

An analysis of the probable cause of the spurious output responses gave rise to a hypothesis (stated by TRW) that the high-order harmonics of both the desired and interference signals within the receiver's first mixer interact to generate IF in-band terms. This hypothetical mechanism appears feasible, particularly as it explains the rather unique frequencies observed at the receiver output.

The spurious outputs of the receiver occur, however, only for a set of test conditions that should not be encountered within the Shuttle's operating RF environment. Therefore, it is unlikely that such anomalous outputs will be present with sufficient strength to cause system degradation.

5.7 Improved Calculation of False Lock Margin in Costas Loop Receivers

5.7.1 Introduction

The problem of false lock in Costas loop receivers has recently received much attention [5,6,20-22], partially in an effort to correct previous erroneous results [23]. In all cases (except for brief mention in Section VI of [22], the false lock phenomenon has been accounted for only insofar as its effect on the S × S component of the Costas loop error signal. Thus, computation of false lock margin, namely, the relative strength of true lock to false lock, has until now been computed by taking the square of the ratio of the true lock S-curve slope to the false lock S-curve slope for the particular false lock mode of interest.

While it is true that the N × N term in the Costas loop error signal is identical under true and false lock conditions, the same is not true for the S × N component. In fact, analogous to the S × S signal component, the S × N term in the equivalent noise of the loop error signal is, in general, smaller for false lock than it is for true lock. Thus, a more accurate computation of false lock margin should be based on the relative tracking thresholds which are determined from the squaring losses [24] under true and false lock conditions. Neglecting the effect of self-noise terms of the filtered modulation,* the squaring loss for true lock is given by [24]:

$$S_L = \frac{\left[\int_{-\infty}^{\infty} S_m(f)\,|G(j2\pi f)|^2\,df\right]^2}{\int_{-\infty}^{\infty} S_m(f)\,|G(j2\pi f)|^4\,df + \frac{N_0}{2S}\int_{-\infty}^{\infty}|G(j2\pi f)|^4\,df} \tag{52}$$

whereas, for false lock, the corresponding result is [22]:

*In general, the self-noise of the modulation is different under true and false lock conditions; however, in both cases, it is small enough to be neglected.

$$S_L = \frac{\left[\frac{1}{T}\int_{-\infty}^{\infty} |G(j2\pi f)|^2 P\left[j2\pi\left(f-\frac{k}{2T}\right)\right] P\left[-j2\pi\left(f+\frac{k}{2T}\right)\right] df\right]^2}{\frac{1}{T}\int_{-\infty}^{\infty} |G(j2\pi f)|^4 \left|P\left[j2\pi\left(f+\frac{k}{2T}\right)\right]\right|^2 df + \frac{N_0}{2S}\int_{-\infty}^{\infty} |G(j2\pi f)|^4 df};$$

$$k = \pm 1, \pm 2, \ldots \qquad (53)$$

In (52 and (53), $|G(j2\pi f)|^2$ is the squared magnitude of the Costas loop arm filter transfer function, $P(j\omega)$ is the Fourier transform of the data modulation pulse $p(t)$ with $S_m(f) \triangleq |P(j2\pi f)|^2/T$ the corresponding power spectrum, where T denotes the signaling interval. Also, in (52) and (53), S denotes the signal power, N_0 the single-sided noise spectral density, and k is the multiple of half the data rate corresponding to the frequencies at which the Costas loop can false lock.

The first part of this report is devoted to an evaluation of the first term in the denominator of (53) for RC arm filters and both NRZ and Manchester random data. Then, using the closed-form expressions obtained from this evaluation and the results given previously in [20], [22], and [24], the true lock and false lock squaring losses can be computed from (52) and (53), and the false lock margin determined from their ratio. Finally, the false lock margin computed as above will be compared with the same computation based only upon the S × S error signal component.

5.7.2 Evaluation of the S X N Component of the Costas Loop Error Signal in the False Lock Mode

For an RC arm filter, we have that

$$|G(j2\pi f)|^4 = \frac{1}{\left[1 + (f/f_c)^2\right]^2}, \qquad (54)$$

where f_c is the 3 dB cutoff frequency. For NRZ data, i.e.,

$$p(t) = \begin{cases} 1; & |t| \le \frac{T}{2} \\ 0; & \text{otherwise}, \end{cases} \qquad (55)$$

the Fourier transform of the pulse shape in (55) is

$$P(j2\pi f) = T\left(\frac{\sin \pi fT}{\pi fT}\right). \tag{56}$$

Letting $\omega = 2\pi f$ and $\omega_c = 2\pi f_c$, then the first $(S \times N)$ term in the denominator of (53) becomes

$$W_k \triangleq \frac{1}{T}\int_{-\infty}^{\infty} |G(j\omega)|^4 \left|P\left[j\left(\omega + \frac{\pi k}{T}\right)\right]\right|^2 \frac{d\omega}{2\pi}$$

$$= \int_{-\infty}^{\infty} \frac{1}{\left[1 + (\omega/\omega_c)^2\right]^2} \left[\frac{\sin^2\left(\frac{\omega T + \pi k}{2}\right)}{\left(\frac{\omega T + \pi k}{2}\right)^2}\right] \frac{d(\omega T)}{2\pi} . \tag{57}$$

Further letting $x = \omega T$ and noting that

$$\sin^2\left(\frac{x + \pi k}{2}\right) = \frac{1 - (-1)^k \cos x}{2} , \tag{58}$$

then (57) simplifies to

$$W_k = \frac{(\omega_c T)^4}{\pi} \int_{-\infty}^{\infty} \frac{1}{\left[x^2 + (\omega_c T)^2\right]^2} \left[\frac{1 - (-1)^k \cos x}{(x + \pi k)^2}\right] dx . \tag{59}$$

The denominator of (59) is of the form

$$\frac{1}{\left[x^2 + a^2\right]^2 (x+b)^2} = \frac{Ax + B}{(x^2 + a^2)^2} + \frac{Cx + D}{x^2 + a^2} + \frac{E}{(x+b)^2} + \frac{F}{(x+b)} , \tag{60}$$

where

$$a \triangleq \omega_c T$$
$$b \triangleq \pi k . \tag{61}$$

The coefficients of the partial fraction expansion of (60) can, after some straightforward algebra, be evaluated as

$$A = -\frac{2b}{(a^2+b^2)^2}\,; \qquad B = -\frac{a^2-b^2}{(a^2+b^2)^2}\,;$$

$$C = -\frac{4b}{(a^2+b^2)^3}\,; \qquad D = -\frac{a^2-3b^2}{(a^2+b^2)^3}\,;$$

$$E = \frac{1}{(a^2+b^2)^2}\,; \qquad F = \frac{4b}{(a^2+b^2)^3}\,. \tag{62}$$

Substituting (60) together with (61) in (59) and evaluating the resulting integrals term by term gives, after considerable simplification,

$$W_k = \frac{1}{\left[1+\left(\frac{\pi k}{\omega_c T}\right)^2\right]^2}\left\{1+\left[\left(\frac{\pi k}{\omega_c T}\right)^2-1\right]\left[\frac{1-(-1)^k(1+\omega_c T)\,e^{-\omega_c T}}{2\omega_c T}\right]\right\}$$

$$+\frac{1}{\left[1+\left(\frac{\pi k}{\omega_c T}\right)^2\right]^3}\left[3\left(\frac{\pi k}{\omega_c T}\right)^2-1\right]\left[\frac{1-(-1)^k\,e^{-\omega_c T}}{\omega_c T}\right]\,. \tag{63}$$

Note that, for $k=0$, W_k of (63) simplifies to

$$W_0 = 1-\frac{3-(3+\omega_c T)\,e^{-\omega_c T}}{2\omega_c T}\,, \tag{64}$$

which agrees with the true lock parameter $K_D D_m$, as given by (8-5) of [25].

For Manchester coded data, the analogous expression to (57) becomes

$$W_k = \int_{-\infty}^{\infty}\frac{1}{\left[1+(\omega/\omega_c)^2\right]^2}\left[\frac{\sin^4\left(\frac{\omega T+\pi k}{4}\right)}{\left(\frac{\omega T+\pi k}{4}\right)^2}\right]\frac{d(\omega T)}{2\pi}\,. \tag{65}$$

Using the trigonometric identity,

$$\sin^4 y = \sin^2 y - \frac{1}{4}\sin^2 2y , \tag{66}$$

then analogous to the relation obtained (see (39) of [26]), for true lock we have that

$$W_k\Big|^{MANCH} = 2W_k\Big|^{NRZ}_{\substack{k\to k/2\\ \omega_c T\to \omega_c T/2}} - W_k\Big|^{NRZ} , \tag{67}$$

where the notation "a→b" means "a replaced by b." Substituting (63) in (67) and simplifying results in

$$W_k = \frac{1}{\left[1+\left(\frac{\pi k}{\omega_c T}\right)^2\right]^2}\left\{1+\left[\left(\frac{\pi k}{\omega_c T}\right)^2-1\right]\left[\frac{3-4(-1)^{k/2}\left(1+\frac{\omega_c T}{2}\right)e^{-(\omega_c T)/2}+(1+\omega_c T)\,e^{-\omega_c T}}{2\omega_c T}\right]\right\}$$

$$+\frac{1}{\left[1+\left(\frac{\pi k}{\omega_c T}\right)^2\right]^3}\left[3\left(\frac{\pi k}{\omega_c T}\right)^2-1\right]\left[\frac{3-4(-1)^{k/2}\,e^{-(\omega_c T)/2}+e^{-\omega_c T}}{\omega_c T}\right];$$

$$k = 0, \pm 2, \pm 4, \ldots \tag{68}$$

Again, for $k=0$, (68) reduces to

$$W_0 = 1 - \frac{9-4\left(3+\frac{\omega_c T}{2}\right)e^{-(\omega_c T)/2}+(3+\omega_c T)\,e^{-\omega_c T}}{2\omega_c T} , \tag{69}$$

which agrees with the true lock result (see (40) of [26]).

The remaining terms of S_L for true and false lock have been previously evaluated and are repeated below for completeness.

5.7.2.1 NRZ Data, RC Filter

True Lock:

$$V_0 \triangleq \int_{-\infty}^{\infty} S_m(f)\,|G(j2\pi f)|^2\,df = \frac{1-e^{-\omega_c T}}{\omega_c T} \tag{70}$$

False Lock:

$$V_k \triangleq \frac{1}{T}\int_{-\infty}^{\infty} |G(j2\pi f)|^2 P\left[j2\pi\left(f-\frac{k}{2T}\right)\right] P\left[-j2\pi\left(f+\frac{k}{2T}\right)\right] df$$

$$= \begin{cases} \left(\dfrac{1}{1+\left(\dfrac{\pi k}{\omega_c T}\right)^2}\right)\left[\dfrac{1+e^{-\omega_c T}}{\omega_c T}\right] ; & k = 1,3,5,\ldots \\ \left(\dfrac{1}{1+\left(\dfrac{\pi k}{\omega_c T}\right)^2}\right)\left[\dfrac{1-e^{-\omega_c T}}{\omega_c T}\right] ; & k = 2,4,6,\ldots \end{cases} \qquad (71)$$

5.7.2.2 Manchester Data, RC Filter

True Lock:

$$V_0 \triangleq \int_{-\infty}^{\infty} S_m(f)\,|G(j2\pi f)|^2\,df = 1 - \frac{3 - 4e^{-(\omega_c T)/2} + e^{-\omega_c T}}{\omega_c T} \qquad (72)$$

False Lock:

$$V_k \triangleq \int_{-\infty}^{\infty} |G(j2\pi f)|^2 P\left[j2\pi\left(f-\frac{k}{2T}\right)\right] P\left[-j2\pi\left(f+\frac{k}{2T}\right)\right] df$$

$$= \begin{cases} \left(\dfrac{1}{1+\left(\dfrac{\pi k}{\omega_c T}\right)^2}\right)\left[\dfrac{1+e^{-\omega_c T}}{\omega_c T}\right] ; & k = 1,3,5,\ldots \\ \left(\dfrac{1}{1+\left(\dfrac{\pi k}{\omega_c T}\right)^2}\right)\left[\dfrac{3-4(-1)^{k/2}e^{-(\omega_c T)/2}+e^{-\omega_c T}}{\omega_c T}\right] ; & k = 2,4,6,\ldots \end{cases} \qquad (73)$$

Also,

$$\frac{N_0}{2S}\int_{-\infty}^{\infty} |G(j2\pi f)|^4\,df = \frac{1}{2\rho_i} = \frac{\omega_c T}{8R_d}, \qquad (74)$$

where

$$\rho_i \triangleq \frac{2S}{N_0 B_i} = \text{signal-to-noise ratio in arm filter bandwidth}$$

$$B_i \triangleq \int_{-\infty}^{\infty} |G(j2\pi f)|^2 \, df = \text{two-sided arm filter noise bandwidth} = \omega_c/2$$

$$R_d \triangleq \frac{ST}{N_0} = \text{detection signal-to-noise ratio.} \tag{75}$$

Figures 39 and 40 illustrate true lock and false lock S_L in dB versus $f_c T$ with R_d as a parameter for NRZ and Manchester data, respectively. In each case, the strongest false lock mode has been chosen which, for NRZ, corresponds to $k = 1$ ($f_f = \frac{1}{2T}$) and, for Manchester, $k = 2$ ($f_f = \frac{1}{T}$), where f_f denotes the false lock frequency of the VCO relative to the true lock carrier frequency.

5.7.3 Calculation of False Lock Margin

False lock margin is appropriately defined as the amount (in dB) by which the input S/N_0 must increase to produce a false lock signal-to-noise ratio in the Costas loop error signal (or, equivalently, the lock detector output signal) equal to that obtained under true lock conditions. Letting S'/N_0 denote the input S/N_0 during false lock, then for equal loop signal-to-noise ratios, we require that

$$\frac{S'}{N_0 B_L} S_L' = \frac{S}{N_0 B_L} S_L, \tag{76}$$

where B_L is the single-sided loop bandwidth, S_L' is the false lock squaring loss defined in (53) and S_L is the true lock squaring loss defined in (52). Alternately, substituting (52) and (53) in (76) gives

$$\frac{S'}{N_0}\left[\frac{V_k^2}{W_k + \frac{\omega_c T}{8(S'T/N_0)}}\right] = \frac{S}{N_0}\left[\frac{V_0^2}{W_0 + \frac{\omega_c T}{8(ST/N_0)}}\right], \tag{77}$$

where V_0, V_k, W_0, and W_k are defined in (70), (71), (64), (63) or (72), (73), (69), (68) depending, respectively, on whether the data

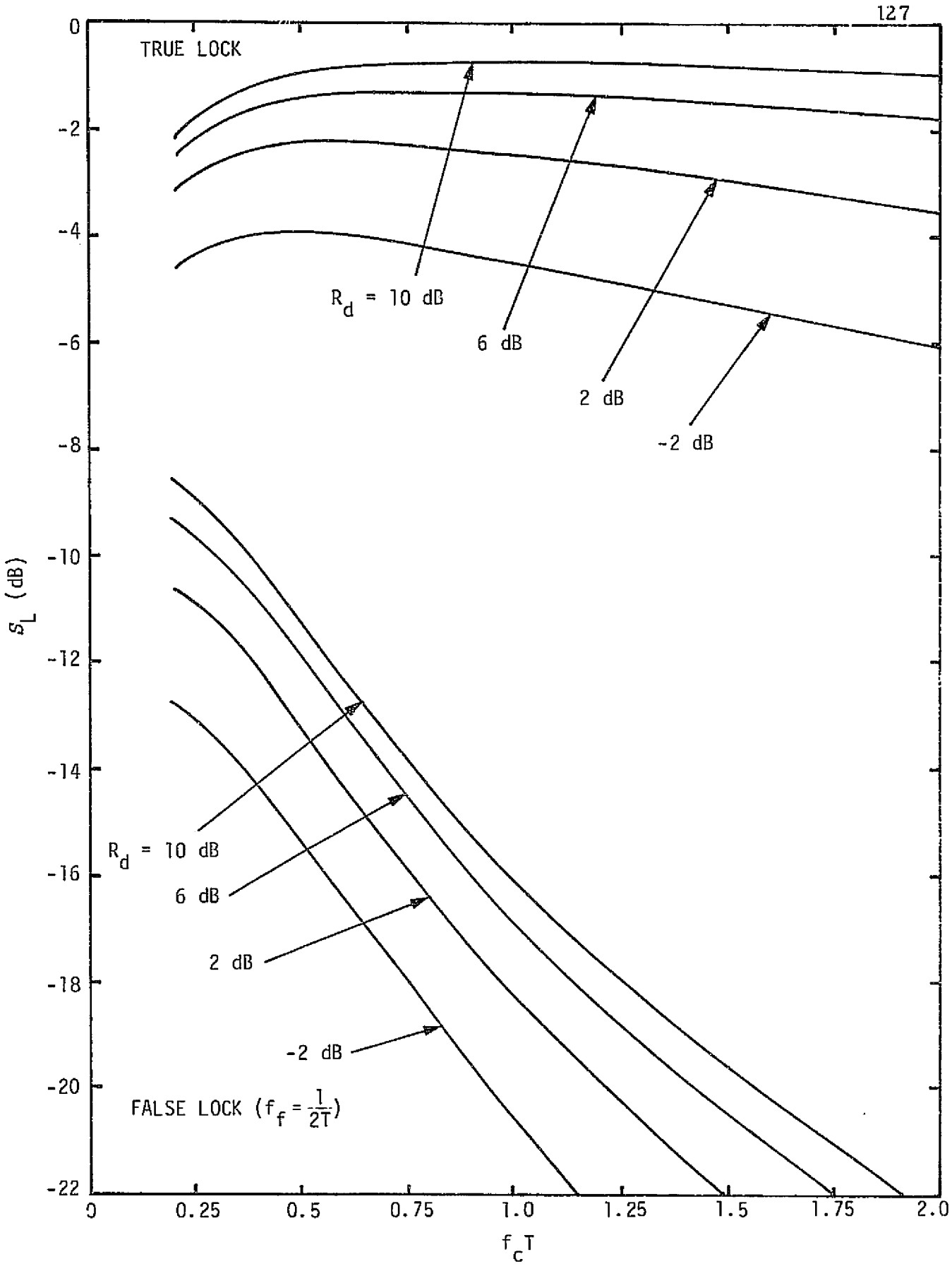

Figure 39. True Lock and False Lock Squaring Losses Versus f_cT With $R_d = ST/N_0$ as a Parameter; NRZ Data

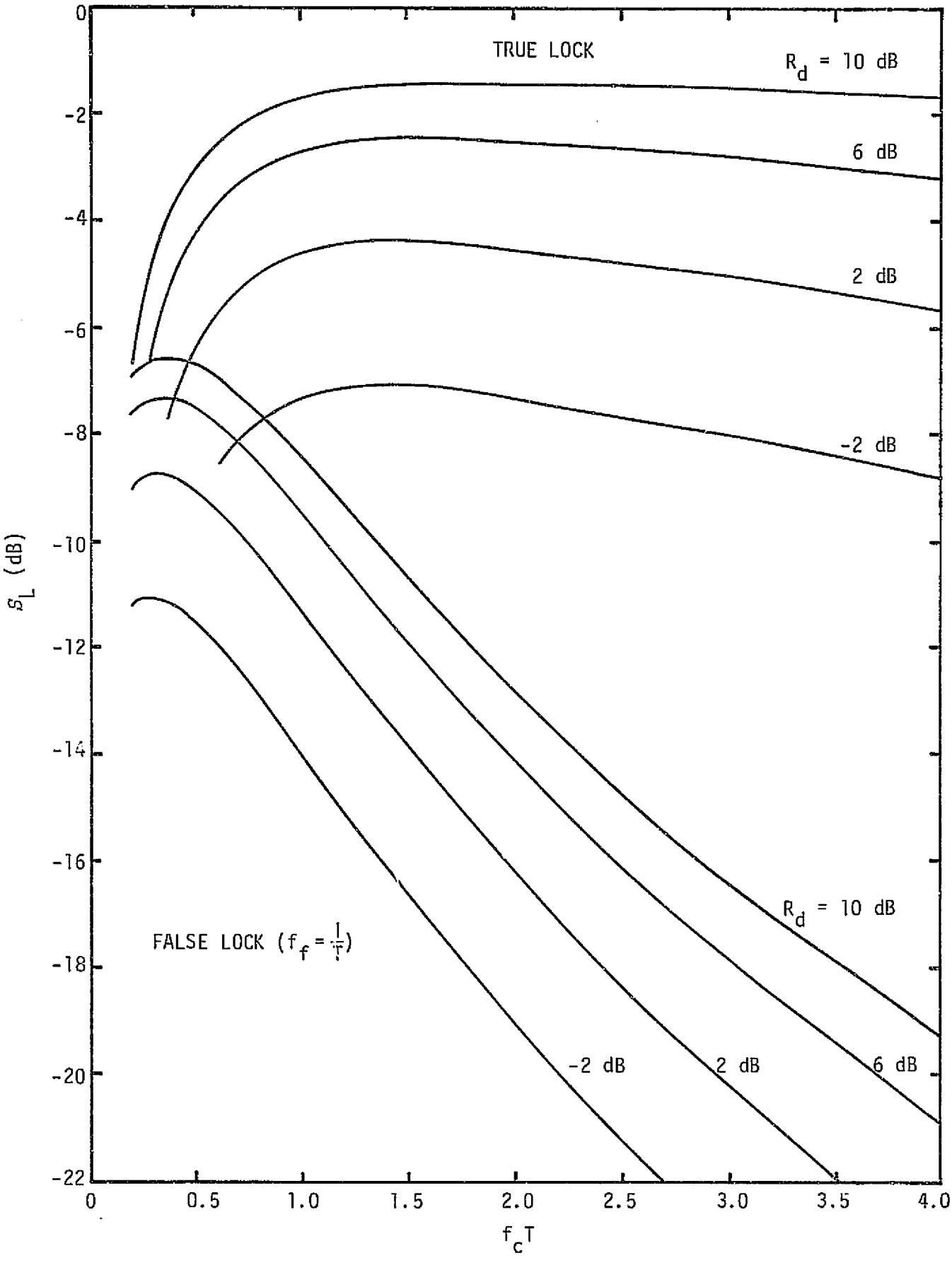

Figure 40. True Lock and False Lock Squaring Losses Versus f_cT with $R_d = ST/N_0$ as a Parameter; Manchester Data

is NRZ or Manchester. Letting $R_d' \triangleq S'T/N_0$ and recalling the definition of R_d from (75), we can rewrite (77) as

$$R_d'^2 \left[\frac{V_k^2}{R_d' W_k + \frac{\omega_c T}{8}}\right] = R_d^2 \left[\frac{V_0^2}{R_d W_0 + \frac{\omega_c T}{8}}\right] . \tag{78}$$

Solving for R_d' in terms of R_d gives

$$R_d' = \frac{W_k}{2V_k^2}\left[R_d^2\left(\frac{V_0^2}{R_d W_0 + \frac{\omega_c T}{8}}\right)\right]\left[1 + \sqrt{1 + \frac{4V_k^2\left(\frac{\omega_c T}{8}\right)}{W_k^2 R_d^2\left(\frac{V_0^2}{R_d W_0 + \frac{\omega_c T}{8}}\right)}}\right] \tag{79}$$

from which the false lock margin M becomes

$$M \triangleq 10 \log_{10}\left(\frac{S'/N_0}{S/N_0}\right) = 10 \log_{10}\left(\frac{R_d'}{R_d}\right)$$

$$= \frac{W_k R_d}{2V_k^2}\left(\frac{V_0^2}{R_d W_0 + \frac{\omega_c T}{8}}\right)\left[1 + \sqrt{1 + \frac{4V_k^2\left(\frac{\omega_c T}{8}\right)}{W_k^2 R_d^2\left(\frac{V_0^2}{R_d W_0 + \frac{\omega_c T}{8}}\right)}}\right] . \tag{80}$$

Figures 41 and 42 illustrate M versus $f_c T$ with R_d as a parameter for NRZ ($k = 1$) and Manchester ($k = 2$) data, respectively. Superimposed in dashed lines are the corresponding results, previously obtained by defining M as $10 \log_{10} V_0^2/V_k^2$, which are independent of R_d. Clearly, as the detection signal-to-noise ratio R_d increases, the effect of the $N \times N$ component of the error signal [second term in the denominator of the squaring loss expressions in (52) and (53)] diminishes. Thus, in the limit of large R_d, the false lock margin approaches

$$M = 10 \log_{10}\left[(V_0^2/V_k^2)(W_k/W_0)\right] , \tag{81}$$

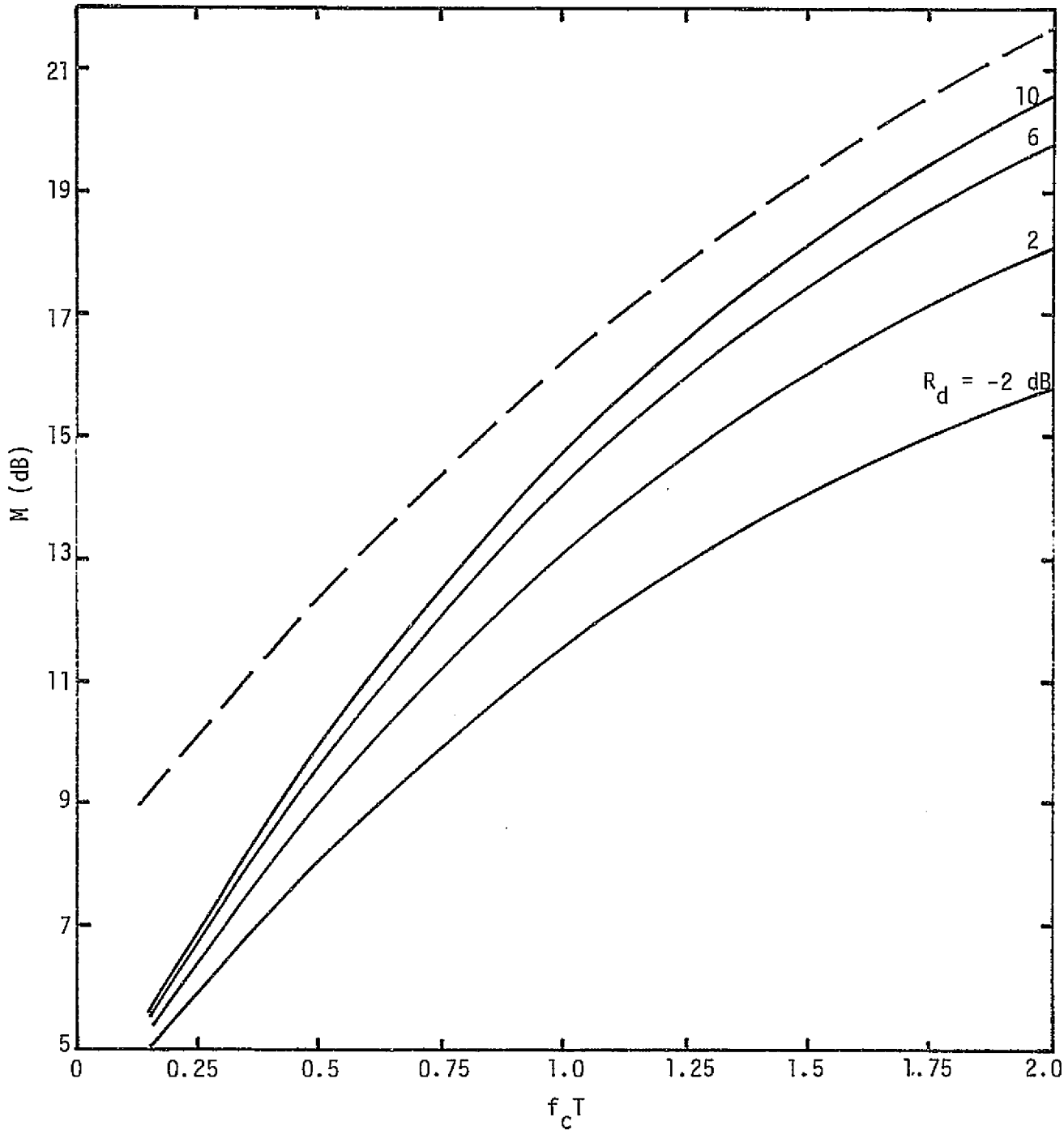

Figure 41. False Lock Margin Versus f_cT With $R_d = ST/N_0$ as a Parameter; NRZ Data

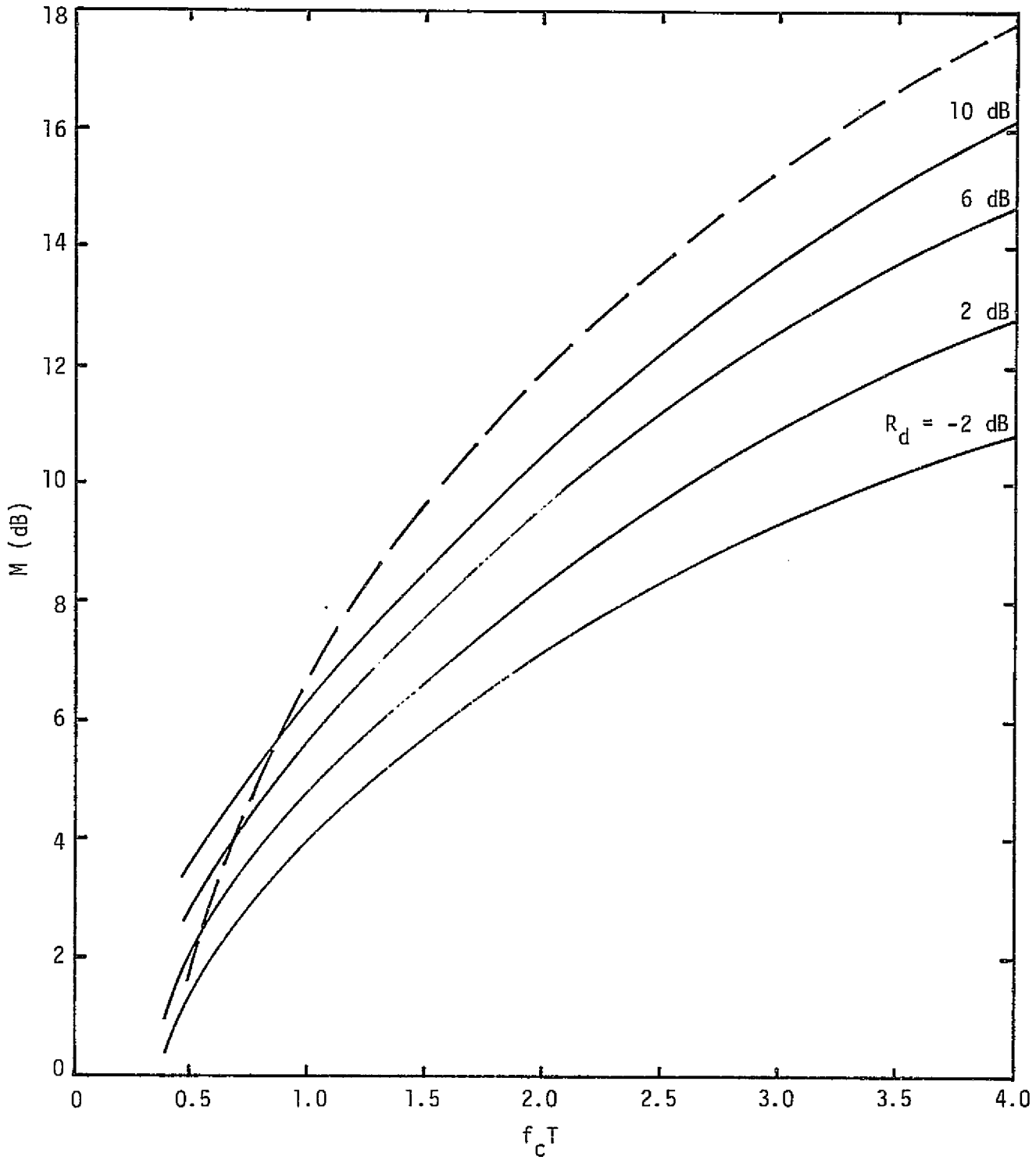

Figure 42. False Lock Margin Versus f_cT With $R_d = ST/N_0$ as a Parameter; Manchester Data

which differs from the dashed curves in Figures 41 and 42 by the factor W_k/W_0. This factor represents the difference in the S × N error signal component for false lock versus true lock.

5.7.4 Conclusions

Proper evaluation of false lock margin in Costas loop receivers requires examination of the effect of false lock on both the S × S and S × N components of the loop error signal. The results obtained in this report indicate that false lock margin computed solely on the basis of the S × S error signal component can, depending on the value of detection signal-to-noise ratio, be overly optimistic. The theory developed is clearly applicable to other arm filter types.

6.0 EQUIPMENT DESIGN AND PERFORMANCE ASSESSMENTS

6.1 Payload Interrogator (PI)

The design of the PI is still in the preliminary stages. A conceptual design review was held by TRW during the month of April 1978, and the preliminary design review is not scheduled until September 1979! Therefore, many design details have yet to surface and a large number of the performance goals remain to be verified through breadboard test.

A history of many of the PI design issues and problems has been given in subsection 4.2.1 Thus, the following paragraphs deal with those specific areas that have been given special consideration by Axiomatix apart from the supporting studies and analyses of Section 5.0.

6.1.1 PI Receiver AGC

The PI receiver AGC loop is a carrier coherent type which is effective only after the receiver PLL has achieved lock. Thus, no gain control is possible during acquisition. The usual practice for receivers of this type is to make use of a narrowband amplitude limiter within the last IF circuits just prior to the PLL phase detectors. By this method, when the receiver is out of lock and there is no coherent AGC, gain control of the carrier component into the PLL is obtained through the nature of the constant power output of the limiter irrespective of the receiver signal level. As a result, the operation is fully predictable, and minimum performance is a function of the well-known limiter suppression factor.

For reasons not fully apparent, TRW chose not to design the PI receiver in this manner but, rather, to allow several successive stages of wideband IF circuits to saturate or limit when the receiver is out of lock. This, it turns out, creates a number of problems. First, it is apparent that performance as a function of received signal level is quite difficult to predict. This is because, when the received signal level is low (< -90 dBm), the only circuits which actually become saturated by the signal-plus-noise within the receiver are those associated with the second IF (31 MHz). However, as the received signal level increases above -90 dBm, successively earlier stages also begin to limit until, for maximum signal level, all of the IF amplifiers in both the first (215 MHz) and second IFs are output saturated. Further, when such behavior is

coupled with the overall gain tolerance that can be expected due to manufacturing variabilities, aging, and temperature, no two receivers can be expected to perform alike. Therefore, Axiomatix believes that this general approach is unsound and will not give wholly predictable operation.

A second problem created by the TRW approach is a potential for the receiver to false lock or, rather, falsely indicate a state of lock, for strong signal conditions (see Subsections 4.2.1.5 and 5.3). This is primarily a function of the large suppression factor obtained because the limiting takes place in wideband (12 MHz) rather than narrowband (200 kHz) circuits. Table 4 indicates the suppression factor ranges that would be expected for ideal limiter models. With wideband limiting, the suppression changes some 25 dB from the carrier acquisition threshold signal level to strong signals while, for narrowband limiting, the suppression ranges over only 9.3 dB for the same input signal level variation. TRW has predicted for their design, which allows progressively successive stages of limiting as a function of signal level (explained above), that the expected suppression variation will be about 16 dB. Since the minimum acquisition operating point (threshold) of the receiver is based upon the suppression factor obtained at the carrier acquisition signal level, the larger the suppression factor, the more problems with false states of in-lock produced by the receiver lock detector (see Subsection 5.3.2).

As explained in Subsections 4.2.1.5 and 5.3, much effort has gone into finding a "fix" for the problem of false in-lock. However, little consideration has been given to redesign which eliminates the underlying source of the problem, namely, the wideband limiting and its manifestations. Axiomatix suggests that a sound solution lies in the use of a noncoherent AGC to the IF circuits when the receiver is out-of-lock. This approach may be straightforwardly implemented through the use of a square-law circuit within the present AGC loop. When carrier lock is obtained and a coherent AGC voltage is available, a switch operated by the lock detector would change the AGC loop from noncoherent to coherent operation. Figure 43 shows the functional configuration. Since this AGC loop will function from signals derived after the 200 kHz narrowband IF, its range of drive level variation to the CAD, over the input signal level range, will be nearly identical to that of the narrowband limiter.

Table 4. Ideal Wideband and Narrowband Limiting Performance

	Wideband Limiting			Narrowband Limiting		
Receiver Signal Level, P (dBm)	P/N_0* (dB)	SNR in 12 MHz (dB)	12 MHz# Limiter Suppression	P_c/N_0† (dB)	SNR in 200 kHz (dB)	200 kHz# Limiter Suppression
-125	42	-29	0.031	39.7	-13.3	0.19
→ -120	47	-24	0.056	44.7	- 8.3	0.33
-115	52	-19	0.10	49.7	- 3.3	0.55
-105	57	-14	0.18	54.7	+ 1.7	0.79
-100	62	- 9	0.30	59.7	+ 6.7	0.94
- 95	67	- 4	0.51	64.7	+11.7	0.98
- 90	72	+ 1	0.76	69.7	+16.7	0.99
- 85	77	+ 6	0.93	74.7	+21.7	0.99

Carrier Acquisition Threshold

*NF = 7.0 dB

#Voltage suppression factor

†β = 1.0 radian

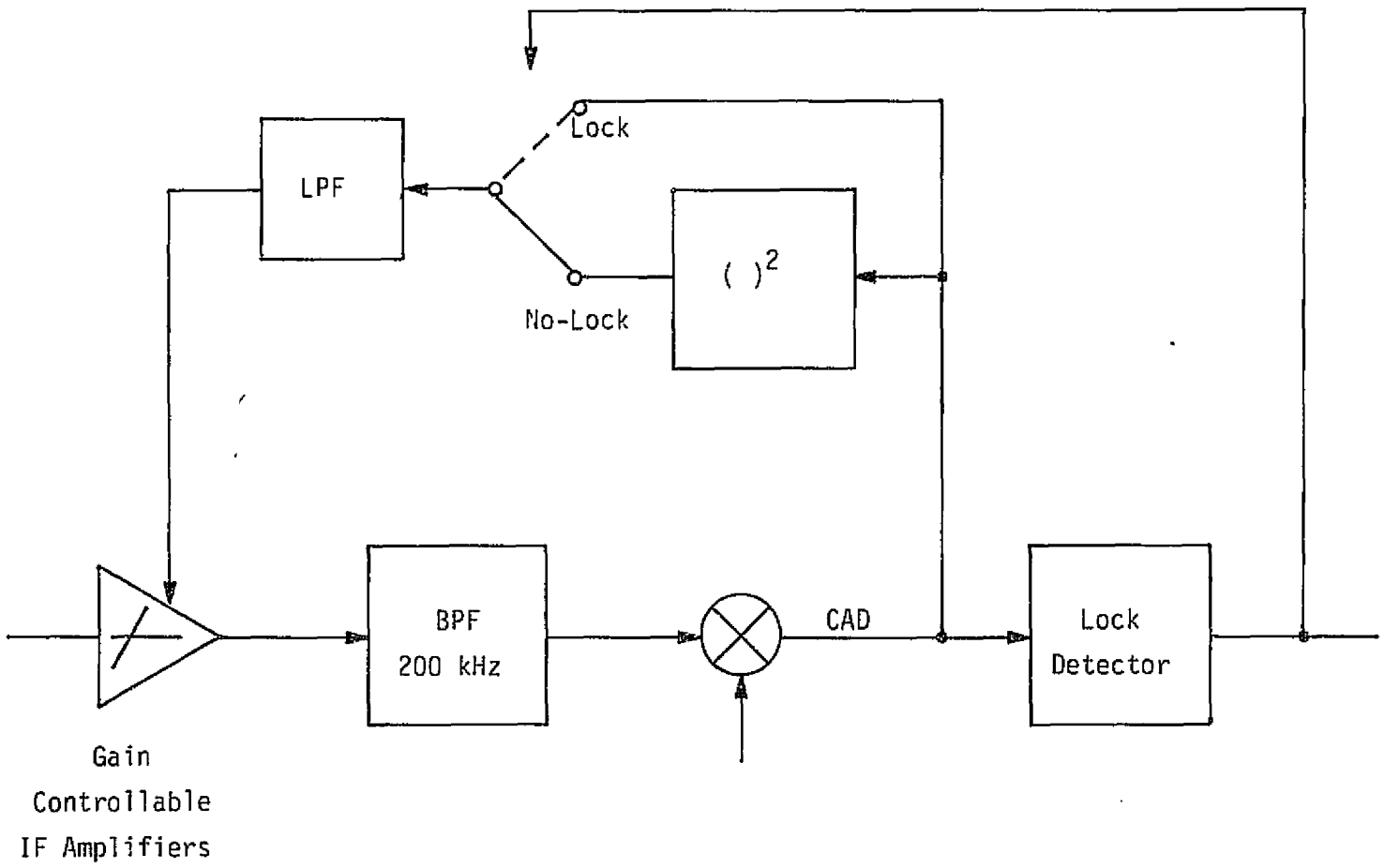

Figure 43. Dual Coherent/Noncoherent AGC Loop

About 8.9 dB total change can be expected, which is significantly superior to the present design approach.

6.1.2 PI Receiver False Lock Susceptibility

As outlined in the previous subsection, the receiver, because of design philosophy, may, for certain standard modulation conditions, falsely indicate states of lock. It is not clear, however, whether actual phase locked tracking of the sideband(s) will occur. What does happen is that, when the lock detector produces an in-lock indication, the sweep voltage into the PLL VCO is switched off, leaving the loop in a static state which is certainly conducive to the conditions for lock. Even when the relative sideband signal level is below the critical value (-35 dBc is the TRW goal), false lock indications may still occur due to the presence of a large sinusoidal signal within the receiver's lock detector bandwidth which is proportional to the true carrier level (see Subsection 5.3.2). This problem also arises, in part, because of the design approach taken with respect to the lock detector (see Subsection 6.1.3). The problem for standard modulations is solvable through redesign.

6.1.3 PI Receiver Tracking Loop and Lock Detector

The overall approach taken by TRW to the design of the tracking loop and lock detector (see Subsection 5.3.2) is conventional, but has two notable weaknesses.

First, so that the receiver can be frequency swept to promote acquisition, a sweep voltage is added to the PLL to control the frequency of the VCO. Therefore, in order for the loop to achieve and maintain carrier lock with the sweep voltage still applied, a counteracting error voltage must be generated within the loop. When the receiver lock detector indicates that lock has been attained, the source of the sweep voltage is abruptly switched out of the loop, causing a transient within the PLL that must be tracked without losing lock. The final steady-state condition is one that may therefore result in a large steady-state loop phase error, depending upon the actual frequency offset of the received signal.

Axiomatix believes that insufficient thought was given to possible alternatives to this approach. In particular, since a somewhat elaborate

frequency synthesizer design is needed so that the receiver will "tune" to a set of some 855 channels, incorporation of the frequency sweep capability into the frequency synthesizer should have been given serious consideration. By such an approach, the degree of large dynamic voltage swing capability needed for the PLL circuits would be minimized. Further, the frequency synthesizer could have the capability to "hold" at the frequency for which lock was achieved, thereby eliminating the potential of large tracking loop stress.

A second weakness with respect to TRW's design is the lock detector. Again, it would appear that a comprehensive study was not made prior to the proposed conceptual design. The use of a simple RC lowpass filter having a time constant of about 2 ms seems to be motivated solely by the need to rapidly switch out the sweep acquisition signal to the PLL when lock is detected. The problem associated with beat note signals (see Subsection 5.3.2) was apparently not considered.

Axiomatix has recommended that a 3-pole LPF should be used in place of the current single-pole design. Axiomatix also believes that the potential and performance of a periodically reset integrating filter should be investigated. This latter approach could provide both a rapid response for stopping the sweep process and the means for greatly minimizing the contribution of beat note components into the threshold detector.

Also, the overall philosophy concerning the enabling and disabling of the sweep requires review. Presently, once the sweep is stopped by the lock detector, it cannot be automatically reinitiated until after a 1/2 second period of continuous out-of-lock indication by the lock detector. Axiomatix believes that, with the present design, there are conditions when beat note components are present that preclude sweep from being enabled once a false state of in-lock has been declared.

6.1.4 PI Receiver Throughput Signal Characteristics

Axiomatix has already reviewed the PI design changes necessary with respect to the wideband output to the KuSP (see Subsection 4.2.1.1) and the output circuits' highpass filter (ac coupling) characteristics (see Subsection 5.4).

The only remaining concern is that the exact nature of the 4.5 MHz

lowpass requirement has not been established in detail, nor is it clear that the linear output circuits to the KuSP have sufficient dynamic capability to cope with the receiver total signal level operating range and conditions.

One additional area not fully defined by TRW is the relationship between the response time of the rms regulating circuit used to gain control of the receiver output to the PSP and CIU, and the response time of the receiver's coherent AGC loop. It appears that the rms regulator has a faster response than the receiver AGC loop, rather than the reverse.

6.1.5 PI Frequency Synthesizer

When the proposed design of the frequency synthesizer was presented at the April 1978 Conceptual Design Review, Axiomatix expressed concern that the use of a larger number of indirect frequency synthesizing phase-locked circuits could contribute to excessive phase noise, especially at the L-band and S-band output frequencies. To date, TRW has provided no convincing evidence that such is not a problem. Promises of breadboard tests have yet to be fulfilled and the ability of the PI to meet phase noise requirements cannot, therefore, be assessed.

6.1.6 PI Overall Engineering Development

What is of particular concern to Axiomatix is the degree to which most of the PI circuits have been carried to the production design stage while, at the same time, significant conceptual and basic design problems still exist, as stated in the above subsections and in Section 4.0. There is still little flexibility in the production configuration to accommodate any necessary extensive redesign and, especially, there is virtually no room within the overall PI hardware packge to accept additional circuits that may prove necessary. If this trend continues well into CY79 (the PDR is not scheduled until September) and if extensive changes prove necessary, the schedule could be affected and costs increased. It is therefore recommended that an interim review of the open design problems and issues be held early in 1979 so that a total understanding of the problems will be obtained and a firm approach for their solution can be implemented.

6. Payload Signal Processor (PSP)

Like the PI, the design of the PSP has also been drawn out and delayed to the extent that little substantive information has been supplied by TRW.

Apart from some initial design concept issues (see Subsection 4.2.2), Axiomatix is not currently aware of any critical design problems. The subcarrier demodulator and bit synchronizer circuits and software are in the process of breadboard evaluation. The PSP PDR is scheduled for March 1979.

Relative to performance evaluation, TRW has completed a series of tests on the PSP demodulator breadboard to experimentally determine the acquisition and tracking thresholds which appear as TBDs in the Rockwell specification. Based upon a criterion of a fixed minimum input signal level threshold for the PI receiver irrespective of modulation bit rate, the poorest performance for the PSP demodulator can be expected to occur for the highest bit rate of 16 kbps. Therefore, TRW has made the following threshold recommendations for the 16 kbps bit rate:

Tracking Threshold:	44 dB-Hz subcarrier-to-noise density at PSP LRU input. Mean time to lose lock of 10 seconds.
Acquisition Threshold:	45 dB-Hz subcarrier-to-noise density at PSP LRU input. The probability of achieving phase lock in 2 seconds or less shall be at least 0.9.

These numbers are some 2.6 dB higher than the corresponding PI receiver acquisition threshold. Improved performance could be obtained if the PSP demodulator's subcarrier loop tracking bandwidth is made smaller (current design is 100 Hz) or is switchable to a lower value after acquisition. The 100 Hz bandwidth was selected based upon "accommodating a 0.01% subcarrier instability." It appears that this specification has been somewhat misinterpreted and that the criteria for selecting the loop bandwidth should be reevaluated. TRW's suggestion of a 50 Hz bandwidth would lower the threshold by about 2 dB. As to switching the bandwidth after acquisition, the current PSP design does not include a subcarrier loop lock detector which would be absolutely necessary to the method.

The PSP overall maximum allowable data SNR degradation remains at 1.5 dB for E_b/N_0 between 2 dB and 12 dB. The expected partition of this total is about 0.6 dB to the subcarrier demodulator and 0.9 dB to the bit synchronizer.

6.3 Network Transponder

The network transponder performance from the standpoints of false lock susceptibility, EMC, and interference susceptibility has been summarized in Subsections 4.3.1 and 5.6. However, one additional observation on the Costas loop 2nd IF module design problems is offered.

The problem with the network transponder, previously noted in Subsection 4.3.1.3, is that the 2nd IF module which contains the Costas loop is very difficult to align to maximum performance specifications. Voltage offsets and drifts, as well as reference frequency shifts (all with temperature), are the primary sources of difficulty. TRW has attempted to solve these problems through careful parts screening and selection, plus attempting to seek some performance specifications relief, and it is hoped that redesign will be unnecessary.

The difficulties are quite typical of the particular analog circuit mechanization adopted by TRW. The use of a true analog cross-multiplier circuit has proven tenuous even for ground receivers and laboratory equipment. If redesign ever becomes necessary, the analog multiplier should be replaced by a chopper type, with a hard amplitude limiter being used in the in-phase arm of the Costas configuration. This approach virtually eliminates the direct voltage bias and drift problems of the present circuit.

Another problem with the current loop design has been maintenance of a true 90° phase relationship between the I and Q phase detector references. Hybrid mismatches and circuit nonsymmetries create the inaccuracy. An improvement of the situation may be obtained by replacement of the hybrid with a quadrature logic (flip-flops) circuit. This solution is not without some problems when using analog phase detectors but should be effective towards lowering the error to less than 5°.

The ultimate solution, which probably could not be realized until the next generation of the network transponder, would make use of a totally digital sampled data design which replaces the I-Q phase detectors with an

ADC controlled by logic-derived quadrature effective clock signals. Once the I and Q signal components are in digital form, all of the Costas loop functions of cross-multiplication, lock detection and AGC are formed through arithmetic processing of the samples in drift-free logic circuits.

7.0 CONCLUSIONS

7.1 Continuation of Effort and Additional Work

The reader of this report will easily sense that the overall effort is a continuing one. For this reason, many of the results reported herein are incomplete while, in other cases, study and analysis activity is just beginning.

Summing up the S-band network hardware activity it is seen that, during CY78, the bulk of the activity was concerned with flight hardware production, testing, and performance troubleshooting. During CY79, the effort will concentrate on qualification and system testing.

As to the payload S-band hardware, CY78 saw PI and PSP conceptual designs, trade-off studies, specification detailing and issue resolution, some breadboard testing, and preliminary production engineering. Because work on these subsystems was constrained due to FY78 funds limitation and a need to divert manpower to the network hardware production and testing problems, the designs will not reach the full preliminary development stage until about mid-CY79. A number of significant design and performance problems await solution.

Axiomatix will continue to support the overall S-band system development, and in particular, all activities associated with the development of the S-band avionic hardware. During CY79, this effort will include:

(1) Evaluation of the S-band network hardware verification testing plans and results.

(2) Continuing review and resolution of payload hardware specification issues.

(3) Providing support to the payload hardware development at TRW.

(4) Working with all concerned agencies (principally NASA, RI, and TRW) to solve design and operational problems in a timely, efficient, low-cost manner.

7.2 Second-Generation Hardware Design Changes and Improvements

Axiomatix has been intimately involved with the S-band program from its inception and is fully aware of the current design details, intricacies, and problems. From its perspective, Axiomatix is therefore

in a unique position to recommend approaches that should be taken with regard to the next generation of S-band hardware. Thus, the following improvements are suggested at this point as a guideline to help NASA with planning for future programs.

7.2.1 Improved Performance S-Band Network Transponder

The current S-band network transponder has several imperfections with regard to its design and operation. Principal among the deficiencies are: (1) excessively long spread spectrum signal (PN code) acquisition times at low signal levels; (2) propensity of the suppressed carrier Costas loop to false lock for various conditions; and (3) marginal circuit performance with respect to temperature and aging, which necessitates painstaking component part prescreening, ultra-precise alignment/adjustment and very time-consuming testing.

Substantial improvements of the receiver with respect to these problems are attainable. The spread spectrum signal acquisition time may be significantly reduced by means of sequential detectors (nonfixed-period integrators) and several parallel search processing channels. False lock may be minimized through a combination of Costas loop redesign and the incorporation of one or more well-known anti-false-lock circuits/algorithms. Several approaches and levels of improvement are feasible with regard to the marginal circuit designs, depending upon the degree of "digitization" deemed desirable. In fact, all of the cited problems find ready solutions through the use of sampled-data and digital algorithm technology. For example, if the spread spectrum signal is represented in a sequence of time samples, the entire correlation/detection process may be realized by a computational algorithm implemented, in part, by a microprocessor. The Costas loop may also be mechanized through digital processing, with samples being taken at the IF, thus effecting demodulation without the use of analog circuit phase detectors. With such digital approaches, the problems of alignment, drift, direct voltage offsets and aging, which plague the current design, will be virtually eliminated.

7.2.2 Expanded Payload Interrogator Capability

To allow simultaneous RF communications to take place at increased ranges between the Orbiter and two or more payloads, each operating on its

own frequency assignment, will likely require some substantive changes to the current PI and PSP designs. A near-term solution to the problem of accommodating two payloads simultaneously would be to somewhat reconfigure the existing redundant PI and PSP pairs so that they could operate independently (one PI/PSP unit for each payload). Operating into the same (or perhaps separate) antenna subsystem, both payloads could be communicated with concurrently, subject to data processing restrictions imposed by other avionic subsystems such as the PDI and MDM/GPC which must handle the data streams. In the event of failure of a specific PI or PSP unit, the working subsystems may still be interconnected to provide a fully operational configuration for one of the two payloads.

A longer term and technically more excellent solution would be to redesign the PI so that it might transmit and receive on two or more frequency assignments at the same time. Clearly, from the standpoint of minimizing cost, as much of the present PI design and circuits as possible should be retained. The key problem is that of frequency conversion and channelization of the separate payload signals within the PI transmitter and receiver. The optimum solution is currently not obvious. For the receiver, several potential solutions should be studied, including: (a) independently tunable tracking and demodulation subsystems following common downconversion to some IF; (b) pulsed/sample data multiplexing (i.e., a dithered-type mechanization); and (c) modulation multiplexing (i.e., the creation of conversion reference frequencies by means of modulating the existing PI frequency synthesizer). The transmitter chain should also be studied from the standpoint of parallel versus common upconversion and signal amplification, plus means for increasing transmitter effective power output. In addition, some improvements and expansion of PI capability should be considered; among these are: (1) incorporation of antisideband false lock circuits; (2) the ability to track and demodulate suppressed carrier signals; and (3) AFC acquisition aids.

7.2.3 Integration and Improvement of Signal Processors

The various avionic system signal processors (NSP, PSP, PDI, KuSP, FMSP) collectively perform the following basic functions: (a) data detection (extraction of bit streams from additive noise); (b) subcarrier modulation and demodulation; (c) data multiplexing and demultiplexing;

and (d) data encoding and decoding. Allied with the above SPs is the MDM/GPS which operates to both input/output data and perform executive control.

All of the SPs are "fixed entities" insofar as their logical functions are concerned. Further, they are mechanized via hardware or firmware and are therefore not "programmable" to perform variations of their set routines. Yet, many duplicative functions are performed by the various SPs, functions which could be accomplished by a single central processor having programmable flexibility. A study should, therefore, seek to specify the design of an advanced SP which is able to integrate the now disjoint SP functions into a single unit.

Digital signal processing akin to (c) and (d) above is most amenable to integration within a common processing unit. Conditioning of telemetry, commands and digital audio and video may be accommodated by a central system operating in conjunction with data bases. Special processing such as information coding, predictive coding, redundancy removal, and privacy encoding may be handled by secondary programmable or dedicated microprocessors. Where most efficient and cost effective, the use of fixed logic hardware should continue.

Subcarrier demodulators, such as those employed by the PSP and DOD CIU, should be capable of universally handling any subcarrier frequency in the range of 100 kHz to 4 MHz by simple program control of frequency synthesizers which are an integral part of all-digital tracking and demodulation loops. Six such demodulators may be envisioned to serve the entire set of multiple payload processing requirements. Similarly, the bit-synchronizers/detectors found in the PSP, CIU and NSP can have fully digital implementations, with each unit capable of covering any bit rate in a range of 10 bps to 10 Mbps. Eight bit-synchronizers/detectors could be provided, with capability to switch any synchronizer/detector to operate with any subcarrier demodulator or other noisy bit stream source. Thus, individual unit failures may be effectively circumvented.

Other miscellaneous analog signal switching, filtering, and modulation may be performed by a single unit which employs programmable or switchable capability. Filtering, for example, might best be mechanized using A/D and D/A conversion in conjunction with digital filtering, or perhaps programmable CCD sampled data filters will suffice.

REFERENCES

1. STDN MFR Technical Manual, ME-5795, Vol I, March 1974.

2. W. H. Casson and C.C. Hall. "New Phase Tracking Demodulator Will Not Lock On Sidebands," Electronics, February 8, 1963, pp. 52-55.

3. SGLS Transponder S-Band Preliminary Design Review Data Package. TRW SDRL No. 32521-40, 30 June 1978.

4. M. K. Simon. "False Lock Behavior of the Space Shuttle Orbiter Receiver for the Ku-Band Uplink," Axiomatix Report No. R7707-1 (under Contract NAS 9-14614), July 7, 1977.

5. M. K. Simon. "On the False Lock Behavior of Polarity-Type Costas Lopps with Manchester Coded Input," NTC'77 Conference Record, pp. 30:1-1 - 30:1-5.

6. M. K. Simon. "False Lock Performance of Costas Loops With Hard-Limited In-Phase Channel," IEEE Transactions on Communications, Vol. COM-26, No. 1, January 1978, pp. 23-24.

7. M. K. Simon. "Tracking Performance of Costas Loops With Hard-Limited In-Phase Channel," IEEE Transactions on Communications, Vol. COM-26, No. 4, April 1978, pp. 420-432.

8. C. R. Cahn. "Improving Frequency Acquisition of a Costas Loop," IEEE Transactions on Communications, Vol. COM-25, No. 12, December 1977, pp. 1453-1459.

9. W. C. Lindsey. Synchronization Systems in Communication and Control. Englewood Cliffs, N.J.: Prentice-Hall, 1973, Chapter 10.

10. D. Richman. "Color-Carrier Reference Phase Synchronization Accuracy in NTSC Color Television," Proceedings of the IRE, Vol. 42, January 1954, pp. 106-133.

11. A. J. Viterbi. "Acquisition and Tracking Behavior of Phase-Locked Loops," Proceedings of the Symposium on Active Network and Feedback Systems. New York: Polytechnic Press, 1960.

12. T. J. Rey. "Automatic Phase-Control: Theory and Design," Proceedings of the IRE, Vol. 48, October 1960, pp. 1760-1771.

13. J. A. Develet, Jr. "The Influence of Time Delay on Second-Order Phase-Locked Acquisition Range," Proceedings of the International Telemetering Conference, Vol. 1, September 23-27, 1963, pp. 432-437.

14. J. R. Woodbury. "Phase Locked Loop Pull-In Range," IEEE Transactions on Communication Technology, Vol. COM-16, February 1968, pp. 184-186.

15. L. J. Greenstein. "Phase-Locked Loop Pull-In Frequency," IEEE Transactions on Communications, Vol. COM-22, August 1974, pp. 1005-1013.

16. P. D. Shaft and R. C. Dorf. "Minimization of Communication-Signal Acquisition Time in Tracking Loops," IEEE Transactions on Communication Technology, Vol. COM-16, June 1968, pp. 495-499.

17. S. I. Yevtyanov and V. K. Snedkova. "Pull-In Range in Phase-Lock Automatic Frequency Control and Phase-Detector Characteristic," Telecommunications Radio Engineering, May 1970, pp. 113-116.

18. U. Mengali. "Acquisition Behavior of Generalized Tracking Systems in the Absence of Noise," IEEE Transactions on Communications, Vol. COM-21, July 1973, pp. 820-826.

19. M. Mancianti, F. Russo, and L. Verranzzani. "An Extension of Richman Analysis to he Second Order SCS," Proceedings of the IEEE, March 1974, pp. 414-415.

20. M. K. Simon. "False Lock Performance of Costas Receivers," Appendix J of "Integrated Source and Channel Encoded Digital Communication System Design Study, " Final Report, Axiomatix Report No. R7607-3, July 31, 1976.

21. G. Hedin, J. K. Holmes, W. C. Lindsey, and K. T. Woo. "Theory of False Lock in Costas Loops, " IEEE Transactions of Communications, Vol. COM-26, No. 1, January 1978, pp. 1-12.

22. G. Hedin, J. K. Holmes, W. C. Lindsey and K. T. Woo. "False Lock Phenomenon in Costas and Squaring Loops," Proceedings of the 1977 National Telecommunications Conference, Los Angeles, California, pp. 34:4-1 - 34:4-6.

23. M. L. Olsen, "False Lock Detection in Costas Demodulators," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-11, No. 2, March 1975, pp. 180-182.

24. M. K. Simon and W. C. Lindsey. "Optimum Performance of Suppressed Carrier Receivers with Costas Loop Tracking," IEEE Transactions on Communications, Vol. COM-25, No. 2, February 1977, pp. 215-227.

25. W. C.Lindsey and M. K. Simon, "Optimum Design and Performance of Costas Receivers Containing Soft Bandpass Limiters," IEEE Transactions on Communications (Special Issue on Spread Spectrum Communications), Vol. COM-25, No. 8, August 1977, pp. 822-831.

26. M. K. Simon and W. K. Alem. "Tracking Performance of Unbalanced QPSK Demodulators: Part I - Biphase Costas Loop with Passive Arm Filters," IEEE Transactions on Communications, Vol. COM-26, No. 8, August 1978, pp. 1147-1156.