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FINAL REPORT

NATIONAL AERONAUTICS & SPACE ADMINISTRATION

on

Studies in Optical Parallel Processing

(NASA-CR-158237) STUDIES IN OPTICAL
PARALLEL PROCESSING Final Report
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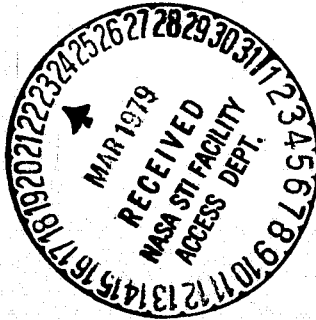
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I. Introduction

This report summarizes the results of a research program on the subject of Optical Parallel Processing, which was carried out in the Applied Physics and Information Science Department of the University of California, San Diego and supported by NASA from March 15, 1974 to October 31, 1978. The overall goal of the project was to develop information processing systems which rely on parallel processing of data to achieve large processing and high goal of the project was to develop information processing capacity and high processing speed. Because optical approaches provide simple solutions to the problems of parallel signal transmission and interconnection between computer components (by using lenses or optical fiber bundles), the all-optical and the opto-electronic approaches to parallel processing were investigated.

To develop parallel processing systems based on the all-optical or the opto-electronic approaches, we investigated threshold and A/D devices for converting a gray scale image into a binary one. To process optical binary signals, the approaches using integrated optical logic circuits (IOC) or optical parallel logic devices (OPAL) were studied.

In the IOC logic scheme, a single row of an optical image is coupled into the IOC substrate at a time through an array of optical fibers. Parallel processing is carried out, on each image element of these rows, in the IOC substrate and the resulting output exits via a second array of optical fibers, Fig. 1. Switching and logic operations are performed on light signals guided in optical channel waveguides in the IOC substrate (electro-optic LiNbO_3). Logic elements are composed of electrooptic light modulators and photodetectors which are electrically interconnected and biased. The advantages of the IOC logic approach to the parallel optical signal processing are its high processing speed, and the ability to perform complex logic operations within a single IOC substrate.

In the scheme where optical parallel logic devices are utilized, binary images are input to the OPAL devices giving rise to new binary images which are logic functions of the input binary images. Thus, an optical parallel logic device consists of an array of cells, each cell performing a Boolean algebraic operation on the input picture elements it receives. (All the picture elements in a binary image are processed completely in parallel). The structure of the OPAL devices which we have been investigating uses an electro-optic light modulating material and a photoconductor appropriately arranged to bring about an interaction between the binary images addressing the device. Several such devices can be interconnected with lenses, mirrors and beamsplitters to construct a circuit for performing more complex processing operations on binary images. The advantage of an optical computer based on OPAL devices is that the degree of processing parallelism which can be achieved is higher than that possible with IOC.

For generating a binary equivalent of an analog image, an analog-to-digital image converter is needed. Binary images can be produced by projecting the analog image through a number of threshold devices with different thresholding levels.¹ Alternately, image thresholding and analog-to-digital conversion can be achieved using a Fabry-Perot phase object processing system. Aside from image thresholding and A/D conversion, Fabry-Perot interferometers have been found to be capable of performing other non-linear optical image processing, such as contrast control and intensity level selection.

The results of our investigation in the three major areas of the project are summarized below. More detailed descriptions are to be found in our publications.

II. Integrated Optical Circuit Logic

The structure of an Integrated Optical Circuit (IOC) information processor with the associated inputs and outputs was shown in Fig. 1. The major tasks which were addressed by our investigation of the IOC approach for parallel processing were i) development of basic IOC logic elements, ii) combining of several of these elements to achieve a more complex logic circuit, iii) fabrication of several sets of logic circuits in parallel on a single substrate and iv) development of a method for coupling optical signals from a linear array of optical fibers into an array of channel waveguides in the IOC substrate. The results of our investigation of IOC logic, as described below, show that solutions to these tasks have been found.

A. The structure of an integrated optical circuit for performing the NOT $A = \bar{A}$ or the (NOT A) AND $B = \bar{A} \cdot B$ operations, is shown in Fig. 2. The logic element consists of two single mode channel waveguides A & B in an electrooptic substrate, and two sets of bordering metal electrodes. Photoconducting film was deposited across electrodes of waveguide A, and constituted a light detector. Optical energy can be coupled from the waveguide to the photoconducting film by direct penetration or by evanescent field. Representing the resistances of the photoconductive film in its light and dark states as R_p^L and R_p^D respectively, the bias resistance R_B is chosen so that $R_p^D \gg R_B \gg R_p^L$. From Fig. 2 it can be seen that whenever light of sufficient intensity propagates in waveguide A, $R_p = R_p^L$ and voltage V_B will be transferred to the waveguide B electrodes. Waveguide B and the electrodes which border it constitute a mode cutoff electrooptic modulator. When an electric field E_y is established between the modulator electrodes, a decrease Δn_e in the refractive index of the waveguide results.

Since the refractive index difference between the waveguide and the surrounding media is decreased, the waveguide operating point can be placed below cutoff for the lowest order guided mode by an application of E_y of sufficient magnitude. With the waveguide below cutoff, light originally in the guided mode radiates into the substrate. Hence, light intensity in the waveguide section which follows the electrodes could be modulated by varying the magnitude of the applied electric field E_y . The modulator is placed in an OFF state whenever the full bias voltage V_B appears across its electrodes. Under this condition, no light emerges from the output end of waveguide B (device output). Since a device output of 1 can result only if both $A = 0$ and $B = 1$, the logic gate output is $\bar{A} \cdot B$.

To achieve a NEGATION operation (\bar{A}) on the input signal A, a CW signal ($B = 1$) is injected into waveguide B. Device output of 1 results if $A = 0$, while an output of 0 results if $A = 1$.

With a different electrical biasing scheme (Fig. 3), the same waveguide-electrode structure can be used to perform the AND logic operation. The two sets of electrodes A and B are now connected electrically in parallel instead of being in series. With this arrangement, the bias voltage V_B appears across electrodes B when no light propagates in waveguide A, and the photoconductor resistance is high $R_p = R_p^D$. Since an output of 1 occurs only when inputs in both waveguides are present ($A = 1, B = 1$), the logic gate output is $A \cdot B$. If a strong CW light beam is present in waveguide B and a weaker time varying signal in A, the device output will be signal A with the peak intensity of the CW light beam in B. Hence pseudoamplification of light in A is achieved.

B. Several of the elementary logic gates just described were combined to produce an integrated optical Half Adder circuit. The structure of the

Half Adder, and the logic functions of its components are shown in Fig. 4.

The Half Adder consists of four channel waveguides W_1, W_2, W_3, W_4 , four mode cutoff electrooptic modulators M_1, M_2, M_3, M_4 , four CdS photodetectors P_1, P_2, P_3, P_4 . Waveguide W_1 and W_3 have signal A as their input, input to W_2 is the signal B, and the input to W_4 is a CW signal K. For the purposes of standardization or pseudoamplification signal K intensity can be larger than that of the outputs from W_2 or W_3 .

Waveguides W_2 and W_3 with associated modulators M_2 and M_3 , and photodetectors P_2, P_3 constitute the portion of the Half-Adder circuit generating the sum signal (S). With the electrical biasing scheme shown in Fig. 4, when light is present in waveguide W_2 ($B = 1$), the voltage V_B is transferred across the modulator M_3 , placing it in an OFF state. Hence, a non-zero output from waveguide W_3 occurs only if both $B = 0$ and $A = 1$, (i.e., the output is $A \cdot \bar{B}$). Similarly, a non zero output from waveguide W_2 can occur only if both $B = 1$ and $A = 0$, (i.e., the output is $\bar{A} \cdot B$). The Half Adder sum signal S can be obtained by adding the outputs of W_2 and W_3 : $S = A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$. This addition can be performed by merging of waveguides W_2 and W_3 , as indicated by dashed lines in Fig. 4. To shorten the overall device length, however, a modified OR gate can be used to perform this addition instead of the merging waveguide section.

The OR gate, consists of two photodetectors P_1 and P_4 across waveguides W_2 and W_3 , and a modulator M_4 across waveguide W_4 . The modulator M_4 will be in an ON state if the output of either one of the modulators M_2 or M_3 is 1. If a CW input $K = 1$ is present in W_4 , the output of modulator M_4 is the sum signal S. Sum signal amplification can be obtained if normalized intensity of K is larger than 1.

The Half Adder carry signal $C = A \cdot B$ emerges at the output of waveguide W_1 . The AND operation is performed by the modulator M_1 across the waveguide W_1 . The modulator is in the ON state only if light is present in waveguide W_2 ($B = 1$), hence waveguide W_1 output is 1 only when both $A = 1$ and $B = 1$.

The IOC Half Adder structure shown in Fig. 4 was fabricated. Half Adder circuit length and width were approximately 4 mm and 1 mm, with waveguide spacing of 260 μm . LiNbO_3 substrate dimensions of 5 x 5 x .5 mm allowed simultaneous fabrication of ten complete logic circuits on each sample. Fig. 5 shows the measured outputs of waveguides W_2 ($\bar{A} \cdot B$) as a function of input light intensity in W_3 ($B = 1$, A varied). Fig. 6 shows the measured output of W_3 ($A \cdot \bar{B}$) a function of light input in W_2 ($A = 1$, B varied). Summing of the output from both of these waveguides would result in a Half Adder sum output. The Half Adder carry signal output $C = A \cdot B$ (Fig. 7) was measured at the output of waveguide W_1 as a function of input light signal in W_2 ($A = 1$, B varied).

C. End fire method was used to couple light ($\lambda = 6328\text{\AA}$) from an array of four single mode optical fibers to an equal number of channel waveguides in the LiNbO_3 substrate (Fig. 8). Fibers were epoxied into a regularly spaced set of V-shaped grooves preferentially etched in silicon² (Fig. 9). To maintain input beam polarization, fiber length was kept to less than 15 cm. Coupling efficiencies obtained were .1 to .2, while typical light power propagating in the channel waveguides was 20-200 μw . This method of light coupling can be directly applied to a larger number of fibers.

The results of our investigation of IOC logic show that several of the major tasks associated with application of IOC to parallel information processing have been solved. Our present research effort aims at increasing

the operating speed of IOC logic elements by replacing the CdS photodetectors with a Si photodiode structure.

III. Optical Parallel Logic (OPAL)

Optical Parallel Logic scheme for information processing is based on processing of picture elements of a binary image. The output of an OPAL device is an image which is the result of a logic operation performed on two input images. The high degree of parallelism utilized in OPAL devices allows constructions of a large capacity computing system.

The major tasks addressed by our research program in this area were: i) development of basic OPAL logic elements, ii) combining of several of these elements to achieve a more complex processing system. Solution to these tasks are described below.

A. The detailed structure of an Optical Parallel Logic (OPAL) device which operates on two binary images is shown in Fig. 10. The device consists of an array of cells, each cell performing the same logic function on the two inputs it receives. Each cell is divided into two parts: one containing photoconductor (opaque) and the other containing transparent dielectric (transmitting). These two parts are interconnected by a patterned transparent electrode. The electrooptic light modulating material is sandwiched between this patterned transparent electrode and a continuous transparent electrode. The i_j^{th} cell receives inputs from the i_j^{th} element of the binary image A, A_{ij} , and from the i_j^{th} element of the binary image B, B_{ij} . Signal A_{ij} is absorbed in the photoconductor, whereas signal B_{ij} is transmitted through the transparent dielectric, the electrooptic light modulating material and an analyzer (not shown) to provide the output C_{ij} . The materials used in the OPAL device at present are: a) photoconductor-CdS, b) transparent dielectric-SiO₂, c) transparent electrode-(In₂O₃)_{.8}(Sn₂O)₁₂, d) electrooptic light

modulating material-twisted nematic liquid crystal.³

The electrooptic response of a twisted nematic liquid crystal was measured and is shown in Fig. 11. The complementary nature of the curves for two orthogonal orientations of the analyzer arises from the polarization properties of light. The presence of a threshold voltage, a sharp transition, and saturation characteristics make this material attractive for use in an OPAL device.

The operation of one resolution cell of an OPAL device can be explained with the help of Fig. 12. In going through the liquid crystal the polarization of signal B_{ij} is rotated by $\pi/2$ when the voltage across the liquid crystal is below the threshold voltage. When a voltage significantly larger than the threshold voltage is applied across the liquid crystal cell, the twist of the liquid crystal molecules, which is induced by alignment agents, is undone. Signal B_{ij} now passes through the liquid crystal with its polarization unaffected. The voltage across the liquid crystal is controlled by the signal A_{ij} on the photoconductor. When the intensity of A_{ij} is zero the photoconductor is in its dark state (high impedance state). Most of the bias voltage now drops across the photoconductor and little across the liquid crystal. But when the signal A_{ij} is maximum, it switches the photoconductor into a conducting state (low impedance state). In this case the bias voltage is largely transferred to the liquid crystal, which in turn affects the polarization of signal B_{ij} . Thus, the interaction between the two input signals is achieved within the OPAL device cell-by-cell. When the output analyzer is oriented parallel to the polarization of the signal B_{ij} , the output C_{ij} is in logic state 1 (bright) only when both A_{ij} and B_{ij} are in the logic state 1 (bright). This corresponds to a logic operation of $A \wedge B$. On

the other hand if the analyzer is oriented perpendicular to the polarization of signal B_{ij} , C_{ij} will be in logic state 1 (bright) if and only if A_{ij} is in logic state 0 (dark) and B_{ij} is in logic state 1 (bright). This corresponds to a logic operation $\bar{A} \wedge B$. It is seen that the same device performs two distinct logic operations on the inputs for two orthogonal analyzer orientations. Simple modifications of this basic scheme will enable the OPAL device to perform other logic operations like OR, NEGATION and pseudo amplification on the input signals.

An 8 x 8 resolution OPAL device was constructed by using standard thin film fabrication techniques. The experimental results obtained with this device are shown in Figs. 13 and 14. Fig. 13(A) shows the calculated and measured input-output characteristics of one resolution cell of the device with the analyzer parallel to input polarization. I_{in} is the light intensity falling on the CdS part of the cell and I_{out} is the light intensity transmitted through the transparent part of the cell. The equivalent circuit of this cell can be modelled as a voltage divider circuit shown in Fig. 13(B). The input-output characteristics were calculated using this equivalent circuit and the experimentally measured CdS and liquid crystal characteristics. It is seen that when the input intensities are below the threshold value I_{in} , the output remains very low and that when the input intensities are above the saturation intensity I_{sat} , the output intensity remains high. These characteristics are valuable when the device is used to perform logic operations on binary signals. The experimental measurements were carried out using the 5145Å output from the Ar-ion laser. The experimental curve was found to be in qualitative agreement with the calculated curve. Fig.14 shows the experimentally obtained photographs of the inputs and the outputs of the OPAL device. In the output photographs, except for the distraction of two non-functioning

cells, two different logic operations are shown for two orthogonal analyzer orientations. The contrast of this device was approximately 20:1. It should be noted that although an Ar-ion laser was used to provide the inputs to the OPAL device, it can also operate with a narrow-band incoherent light source. This feature gives the device greater flexibility and avoids some noise problems encountered with coherent light.

B. Since the Boolean algebraic functions that can be performed with OPAL devices form a complete set, it is possible to carry out more complex processing operations using combinations of OPAL devices. We decided to construct first a half-adder circuit with OPAL devices, because half-adder is a basic component in an arithmetic unit of a digital computer.

A half-adder circuit in the arithmetic unit of a digital computer accepts two input bits of the same significance and generates a SUM and CARRY output bit of different significance. The truth tables as well as the implementation of the half-adder circuit with AND, OR and NEGATION gates are shown in Fig. 15. It can be seen from the truth table that the CARRY output is obtained by performing an AND operation on the two inputs, whereas the SUM output requires a logic operation of Exclusive OR (EXOR). This EXOR operation can be implemented with AND, OR and NEGATION gates using the following decomposition:

$$A \oplus B \equiv (\bar{A} \wedge B) \vee (A \wedge \bar{B})$$

Thus, six gates are normally required to build a half-adder circuit.

To build a half-adder circuit with OPAL devices, one should take notice from Fig. 12 that one device can provide both $A \wedge B$ and $\bar{A} \wedge B$ outputs with two orthogonal analyzer orientations. Furthermore, the two operations encountered in the EXOR decomposition ($\bar{A} \wedge B$) and $A \wedge \bar{B}$) are mutually exclusive.

Therefore, the OR operation between them can be optically performed by a simple superposition without affecting the signal level of logic state 1. Utilizing these special properties, a half-adder circuit can be constructed with two OPAL devices, instead of six. The schematic diagram of the half-adder circuit for processing binary images is shown in Fig. 16. OPAL device 1 (OPAL 1) in conjunction with a polarizing beam splitter provides the CARRY output ($A \wedge B$) as well as $A \wedge B$ (one part of the EXOR decomposition). OPAL device 2 (OPAL 2) in conjunction with a crossed analyzer provides $(\bar{A} \wedge B)$ by transmitting the input signal A as the output and absorbing the input signal B in the CdS part of the cell. Combining the appropriate outputs from OPAL 1 and OPAL 2 gives the SUM output ($A \oplus B$). Fig. 1 details the actual optical configuration of a half-adder circuit, which uses lenses, mirrors and beam splitters (polarizing and ordinary).

The photographs of the experimental results obtained are displayed in Figs. 18 and 19. Fig. 18 contains the two inputs and the CARRY output of the half-adder circuit. Fig. 19 shows the photographs of the two parts of the EXOR decomposition as well as the SUM output which is a simple superposition of these two parts.

In summary we have described the fabrication and operation of an Optical Parallel Logic (OPAL) device for processing binary images. Several logic operations on two input binary images were demonstrated by constructing an 8 x 8 device using a CdS photoconductor and a twisted nematic liquid crystal. It was concluded that a complete set of logic operations could be obtained with such a device.

Our present research efforts are divided into two broad categories: device improvements and system applications.

a) Device related research: Work on higher resolution and higher speed

devices will be continued. Use of new photoconductors (e.g. Silicon) and new electrooptic materials (e.g. PLZT) will be investigated. Also, various schemes for constructing memory devices for binary images will be studied.

b) System related research - Efforts will be made to develop a (electronic) microprocessor controlled Digital Optical Processing System, with the microprocessor controlling the flow of optical data, the optical memory and other logic devices. The use of this hybrid system in performing useful processing operations such as contouring, area counting, etc. will be demonstrated.

IV. Optical Threshold Devices and A/D Conversion

Image thresholding, and analog-to-digital conversion can be achieved using Fabry-Perot interferometer. The Fabry-Perot optical processing system is shown in Fig. 20. It consists of two plane, parallel, dielectric mirrors, one of which is mounted on a piezoelectric translator.

A. When the input to be processed is placed inside the Fabry-Perot processing system as a phase object the spatially varying transmittance function of the system is given by

$$T_{PO}(x,y) = \frac{T^2}{(1-R)^2 + 4R \sin^2(kd + \delta(x,y))} \quad (1)$$

where R,T are the intensity reflectance and transmittance of the mirrors, d is the mirror separation, $k = 2\pi/\lambda$ and $\delta(x,y)$ is the phase shift associated with the input image. T_{PO} is plotted as a function of kd for several different values of δ in Fig. 21, which illustrates the basic operation of intensity level selection. If the mirror reflectance is high ($R > 90\%$) and $\delta(x,y)$ increases monotonically with intensity from 0 to π , the interferometer will only transmit light through those portions of the image which correspond to a single intensity level. The result for a bleached photographic image input are shown in Fig. 22. The level selected by the interferometer is determined

by the equation

$$kd + \delta(x,y) = \ell\pi$$

where ℓ is an integer. To select a different level, the value of kd is changed by moving one of the mirrors on a piezoelectric translator.

B. Using photoresist as the phase recording medium we obtained the experimental results shown in Fig. 23. The photoresist was spun on one of the mirror surfaces, exposed to the gray tone image in the center of Fig. 23, and then developed to achieve a linear phase profile. The eight spots around the outside of the image were exposed for different lengths of time to produce a linear exposure scale which could be compared with the image. The exposure of the spot at 12 o'clock was equal to the exposure of the brightest portion of the image and the spot at 10:30 was unexposed. The phase shift between these two spots was about 0.9π . In Fig. 23, eight different levels are presented. Beginning in the upper left-hand corner and moving left to right, top to bottom across the figure page, the piezoelectric translator was moved in eight equal steps and eight different level slices are presented. The increasing phase shift can be monitored by observing the counterclockwise progression of the spots around the outside of the image.

C. To perform more complicated nonlinear operations, such as image thresholding and analog-to-digital conversion, the laser is modulated as the different levels are selected. For example, image thresholding is performed by scanning the Fabry-Perot through one free spectral range (changing kd by π radians) but only turning on the laser when those levels are being selected which are above the threshold value. In the output, an image is constructed which is bright in those areas where the intensity level in the input is above the threshold, and dark everywhere else. Analog-to-digital conversion is performed in a similar manner. A gray tone image with eight levels (numbered 0-7)

can be represented by three bit planes. The most significant bit plane is generated by thresholding the image at level 4. The next most significant bit plane is produced by turning on the laser when levels 2, 3, 6 and 7 are selected. The least significant bit plane is constructed by turning on the laser levels 1, 3, 5 and 7 are selected.

The phase object, used for the intensity level selection experiment, was used also to demonstrate analog-to-digital conversion. The three bit planes which represent an image divided into 8 gray levels were generated using the technique described above and are shown in Fig. 24. From the figure the gray level of any point in the original can be determined by examining the corresponding point in the three binary images, e.g. the horizontal stripe behind the funnel is a level 5 (101). A resolution of better than 20 λ /mm was established for a mirror spacing of about 0.1 mm.

In conclusion, the Fabry-Perot optical processing system was demonstrated to have several useful processing capabilities. The most important of these in an optical parallel processing digital computer are the image thresholding and analog-to-digital conversion.

V. Publications

The list of publications which resulted from research carried out under NASA sponsorship is as follows:

1. L. Goldberg and S. H. Lee, "Optically Activated Switch/Modulator Using a Photoconductor and Two Channel Waveguides", Radio Science 12, 537 (1977)
2. L. Goldberg and S. H. Lee, "Integrated Optical Half Adder Circuit", accepted for publication in Applied Optics (1979)
3. R. Athale and S. H. Lee, "Development of an Optical Parallel Logic Device and a Half Adder Circuit for Digital Optical Processing", accepted for publication in Optical Engineering (1979), presented at SPIE Symposium on Real Time Signal Processing, San Diego, CA., Aug. 1978
5. S. H. Lee, B. Bartholomew and J. Cederquist, "Two Improved Coherent Optical Feedback Systems for Optical Information Processing", Proceedings of S.P.I.E. on Optical Information Processing, Vol. 83, pp. 78-84 (1976)
6. B. Bartholomew and S. A. Lee, "Non Linear Image Processing Using Fabry-Perot Interferometers", J. Opt. Soc. Amer. 68(10) 1377 (1978). A lengthier manuscript is under preparation.
7. B. Bartholomew, "Nonlinear Optical Processing with Fabry-Perot Interferometers", Doctoral Dissertation, University of California at San Diego, 1979.

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2. L. P. Boivin, Appl. Opt. 13, 391 (1974)
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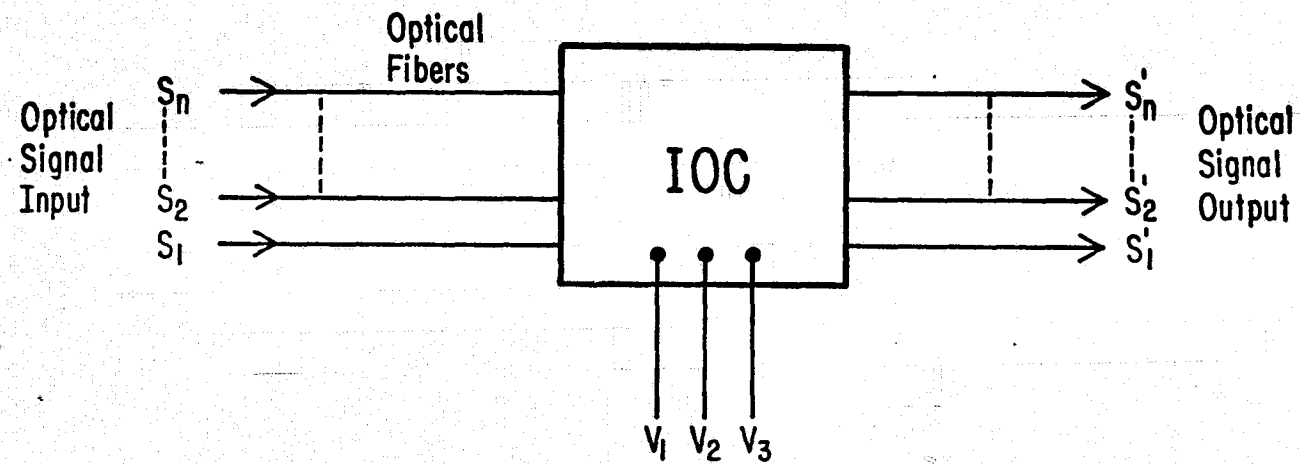


Figure 1. Optical signal IOC signal processing system.

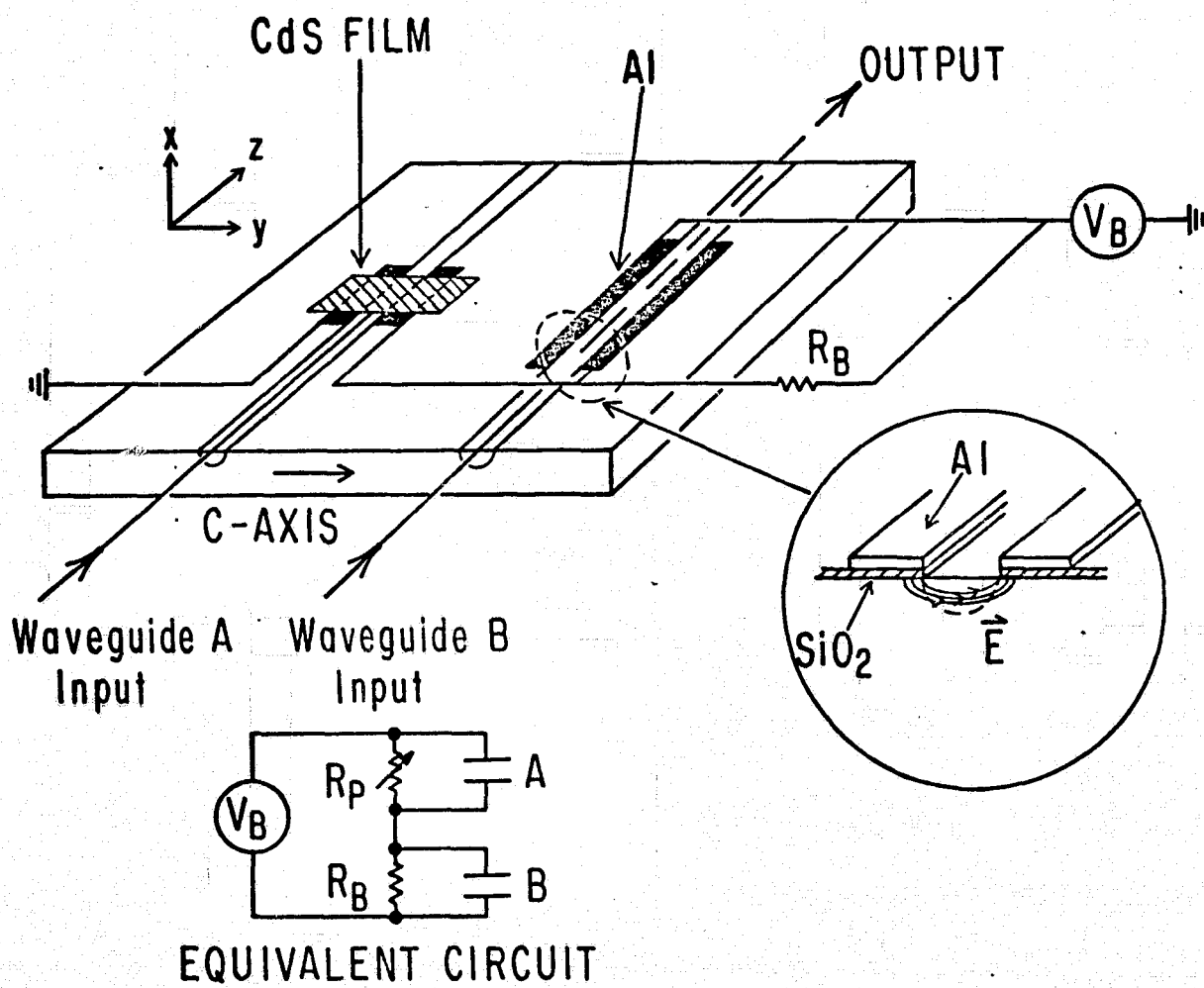


Figure 2. Integrated optical NEGATION logic gate.

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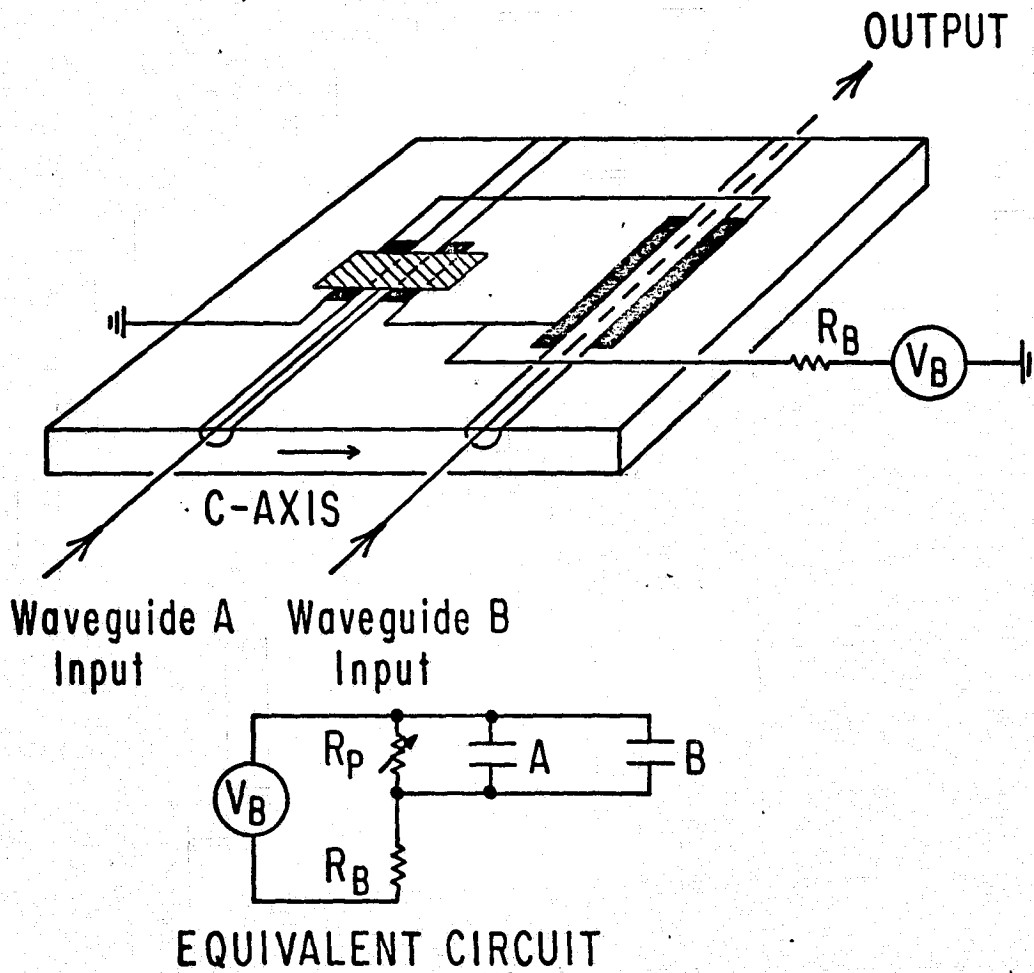
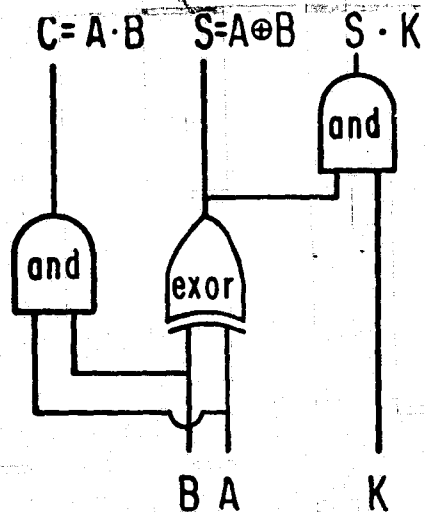


Figure 3. Integrated optical AND logic gate.

(a)



A	B	$\bar{A} \cdot B$	$A \cdot \bar{B}$	S	C
0	0	0	0	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

(b)

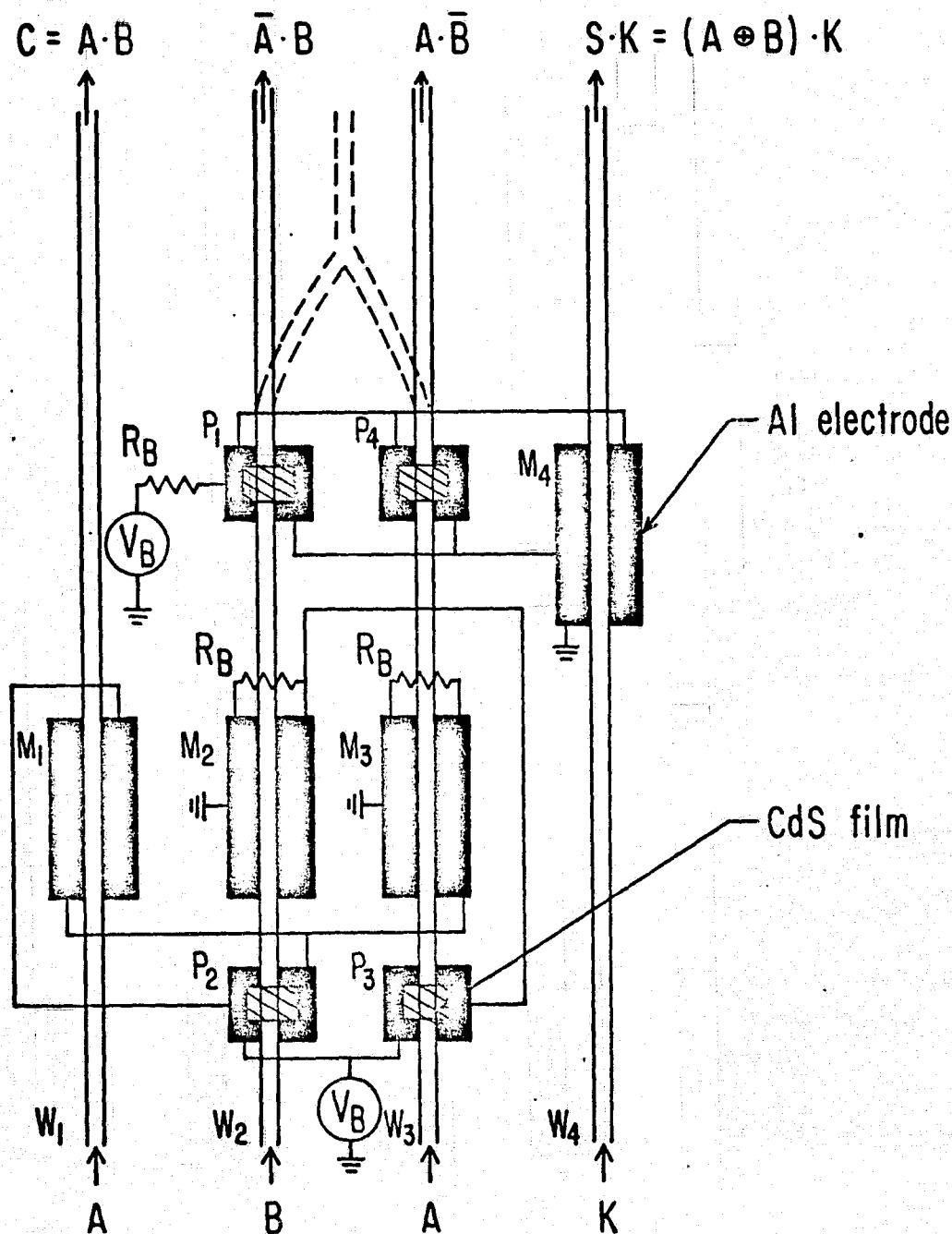


Figure 4. (a) The Logic functions performed, and the truth table for the Half Adder outputs. (b) Structure of an IOC Half Adder.

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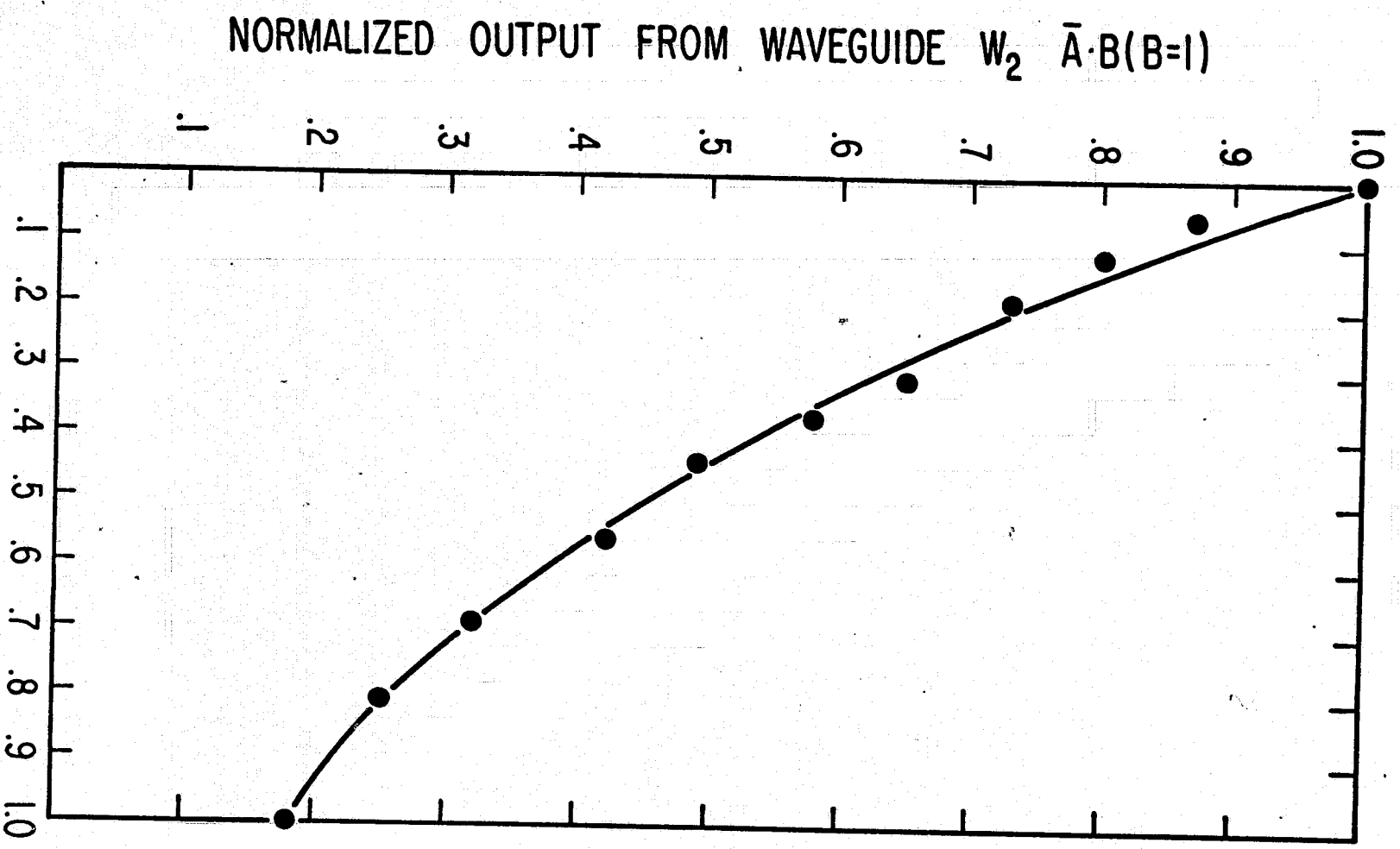


Figure 3 The $\bar{A} \cdot B$ output of the Half Adder as a function of intensity of A (with $B = 1$).

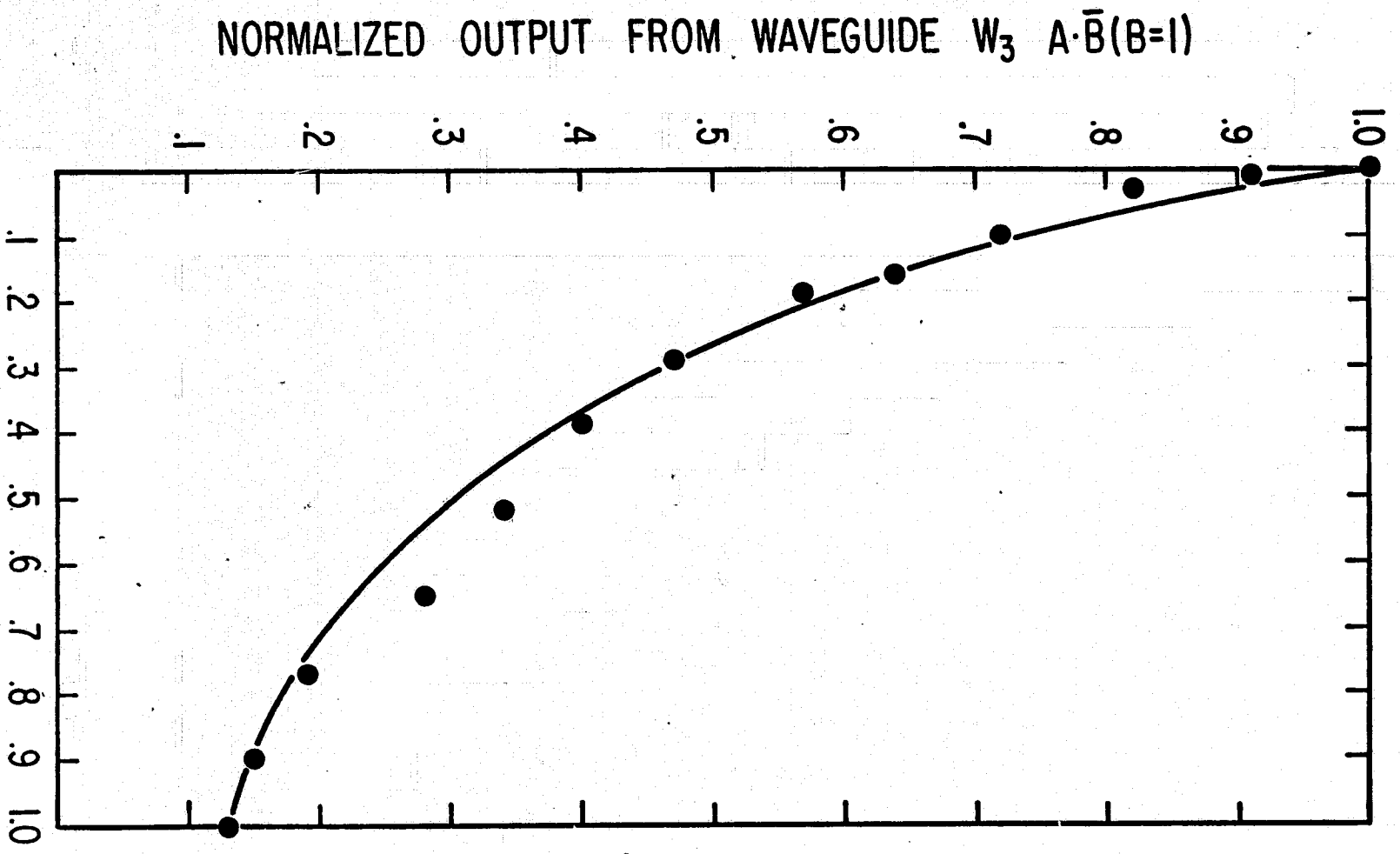


Figure 6

The $A \cdot \bar{B}$ output of the Half Adder as a function of intensity of B (with $A = 1$).

NORMALIZED INPUT IN WAVEGUIDE W_2 (A)

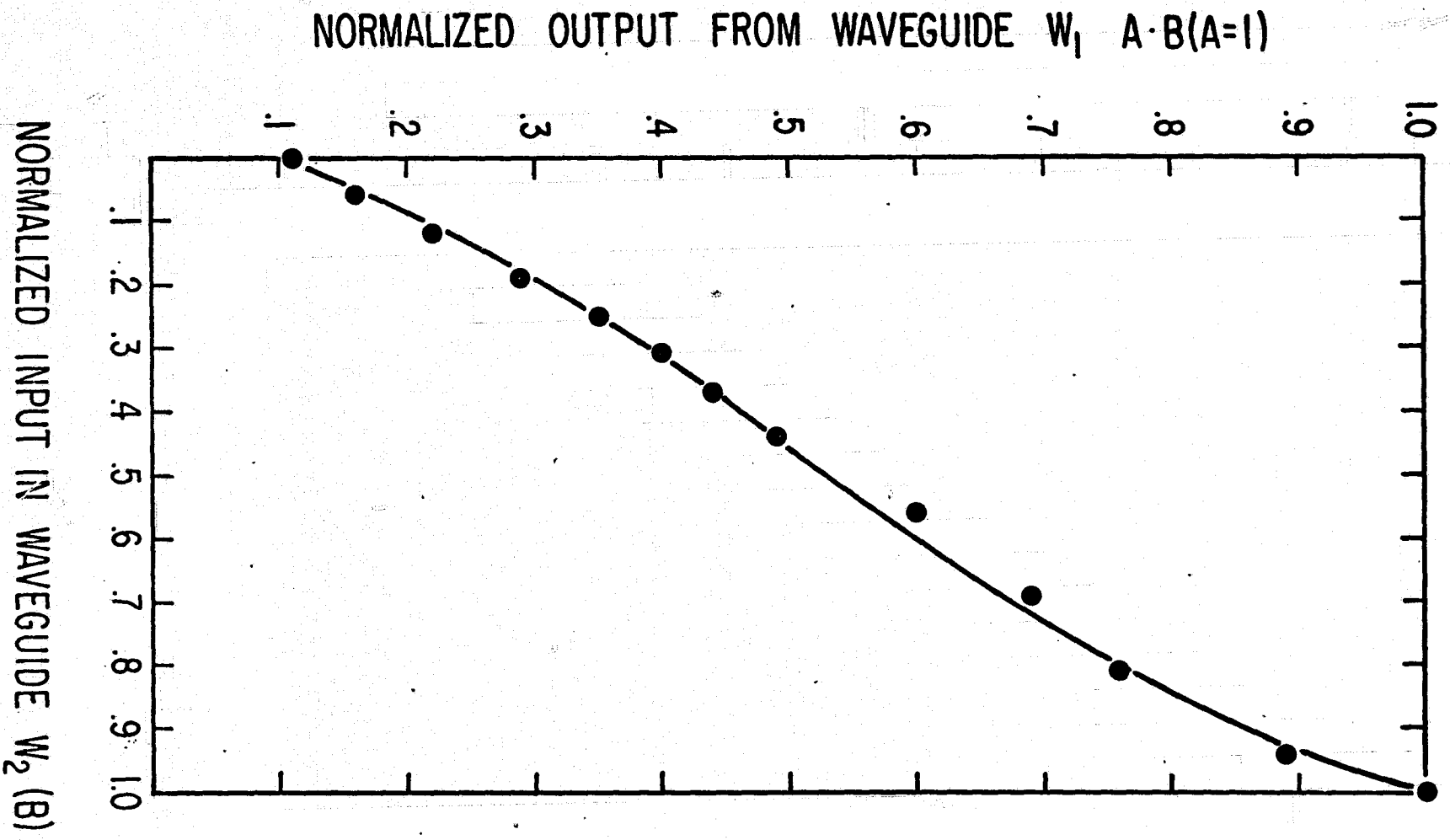


Figure 7 The Half Adder carry signal $C = A \cdot B$ output as a function of intensity of B (with $A = 1$).

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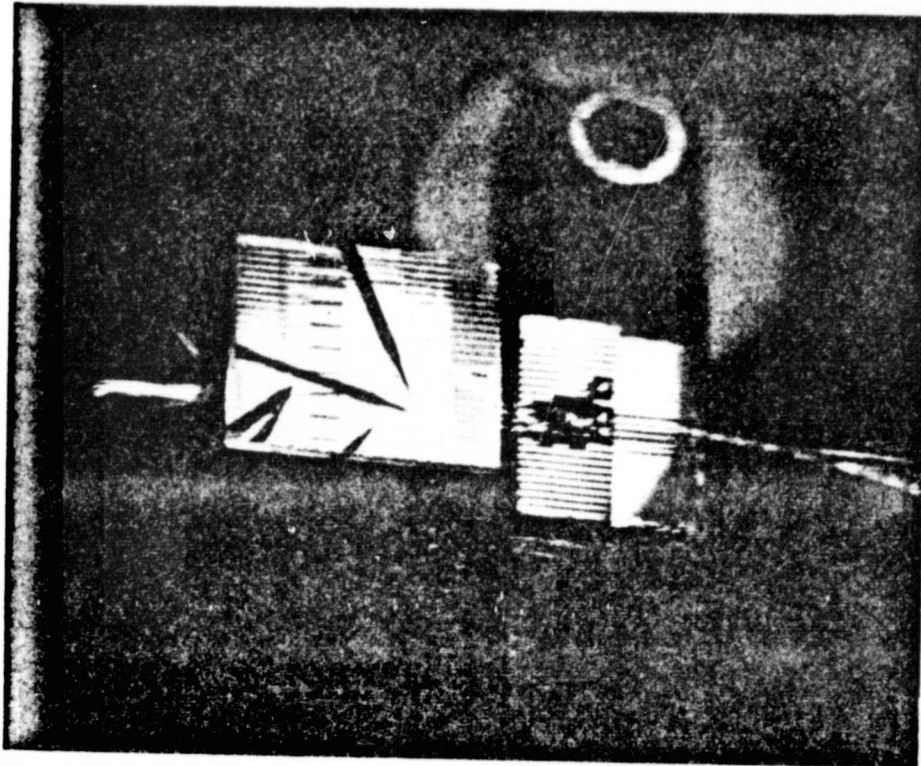


Figure 8 An array of four single mode fibers butted up against the LiNbO_3 substrate. Substrate length is 5 mm.

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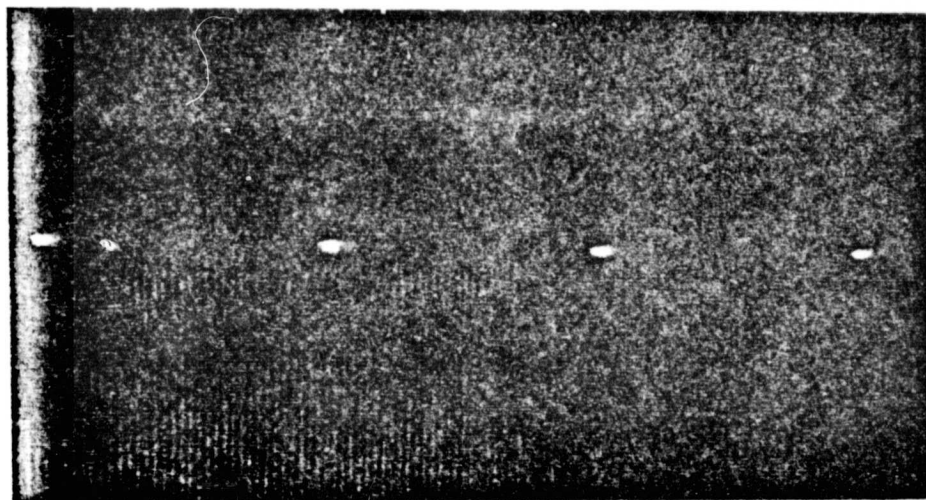
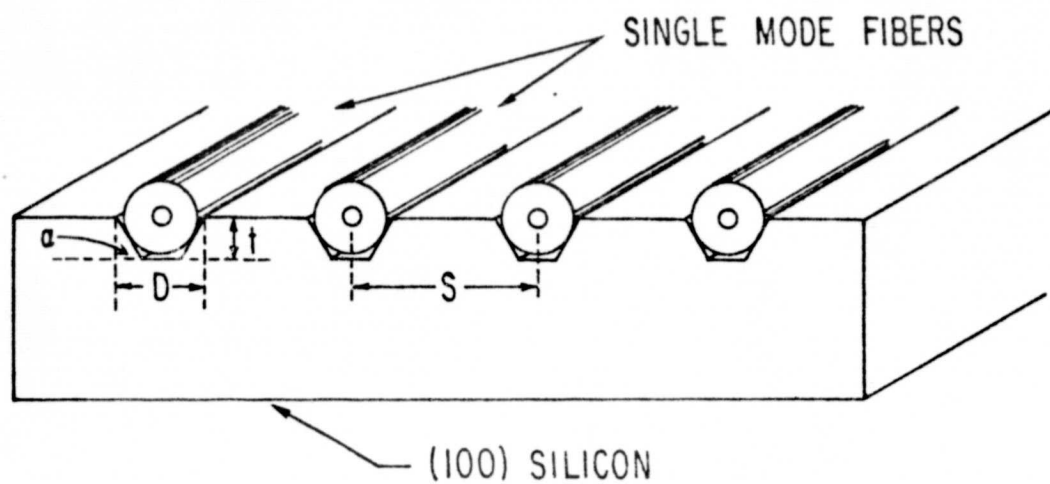
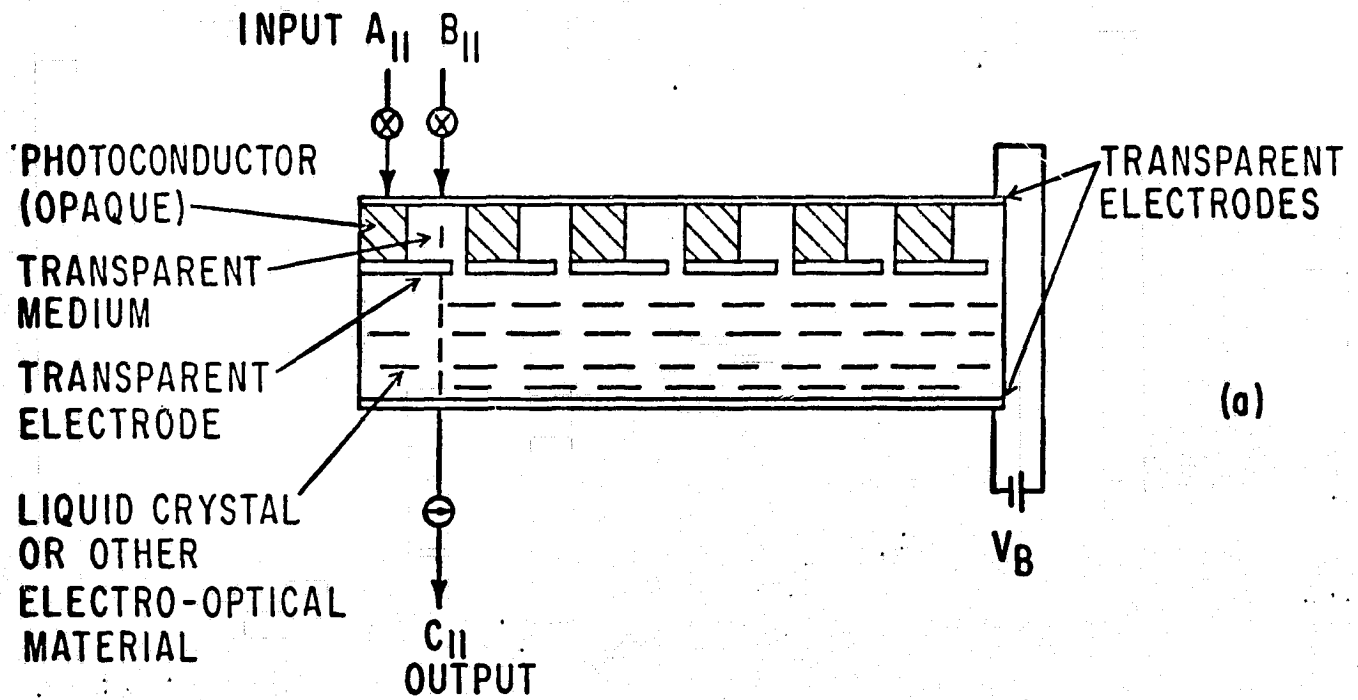
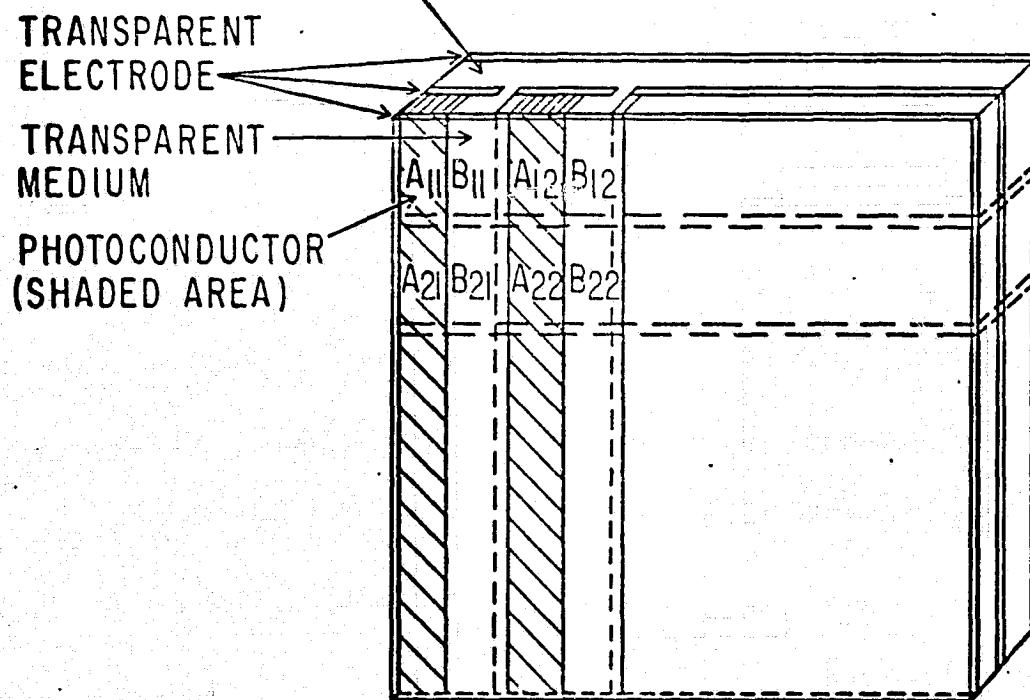


Figure 9. Preferentially etched grooves in Si, and a photograph of the outputs of four simultaneously excited waveguides. $\alpha = 54.7^\circ$, $D = 131 \mu\text{m}$, $t = 68 \mu\text{m}$, $S = 260 \mu\text{m}$.



(a)



(b)

FIGURE 10 OPAL DEVICE STRUCTURE

(A) SIDE VIEW

(B) PERSPECTIVE VIEW

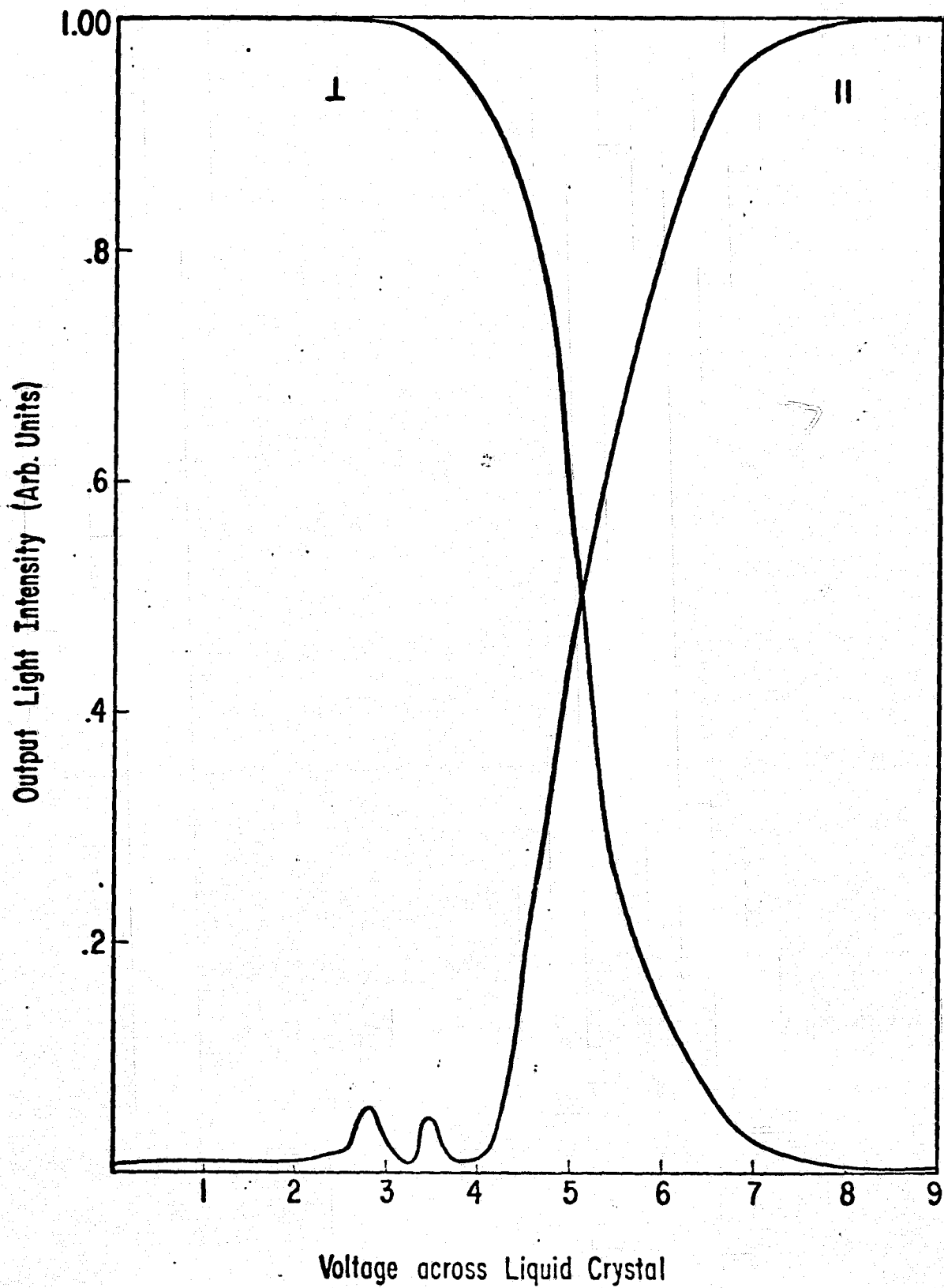
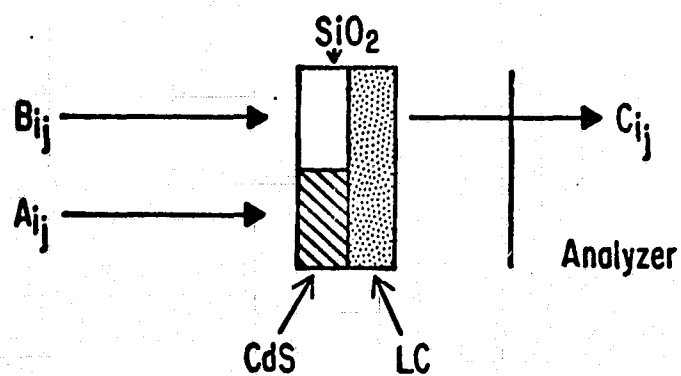


FIGURE 11 ELECTROOPTIC RESPONSE OF A TWISTED NEMATIC LIQUID CRYSTAL CELL FOR ANALYZER ORIENTED PARALLEL (|| CURVE) AND PERPENDICULAR (⊥ CURVE) TO THE INPUT POLARIZER. THE ELECTRIC FIELD APPLIED IS AT 20 KHz.



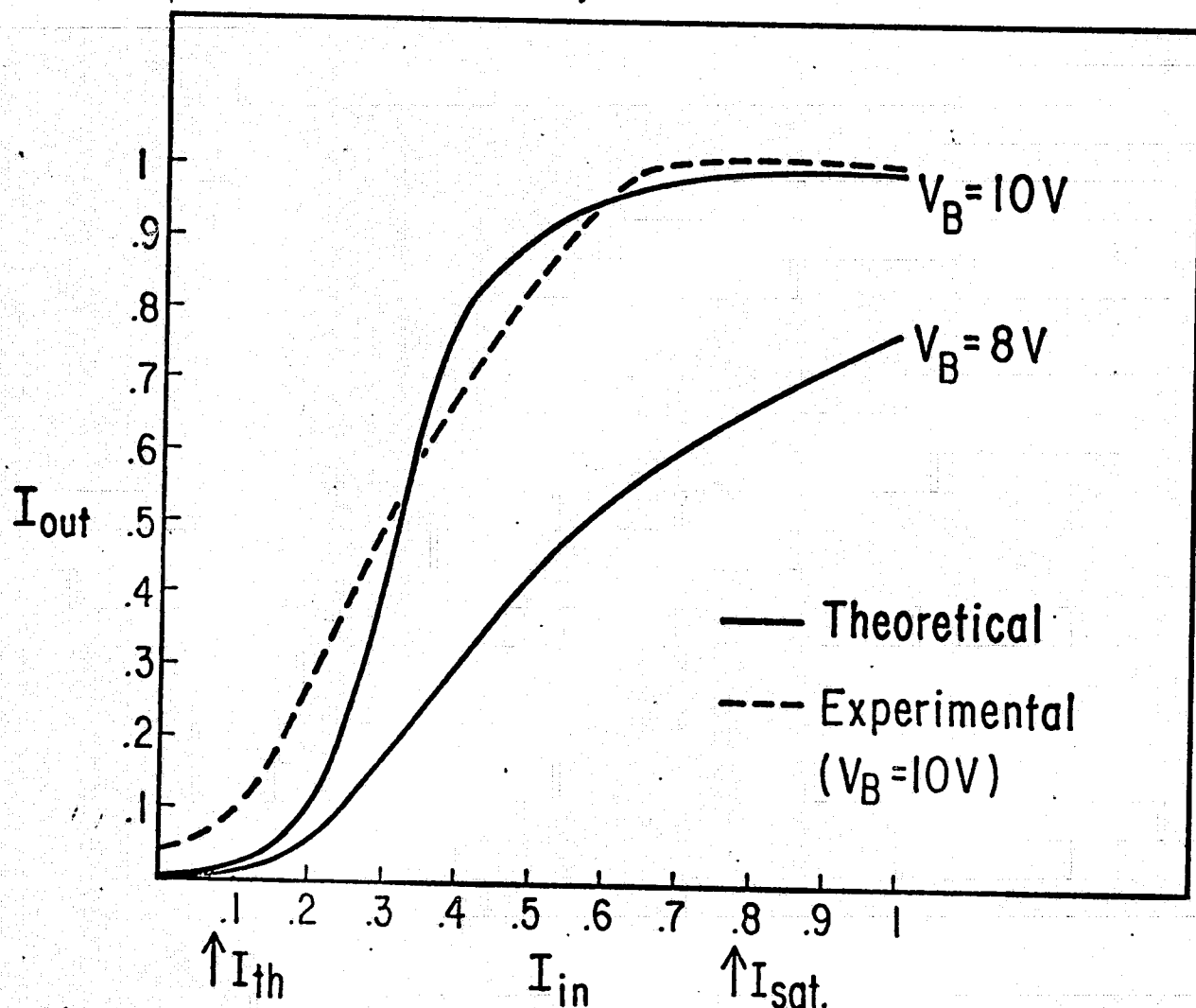
FOR ANALYZER || TO POLARIZER :

$$C_{ij} = \bar{A}_{ij} \wedge B_{ij}$$

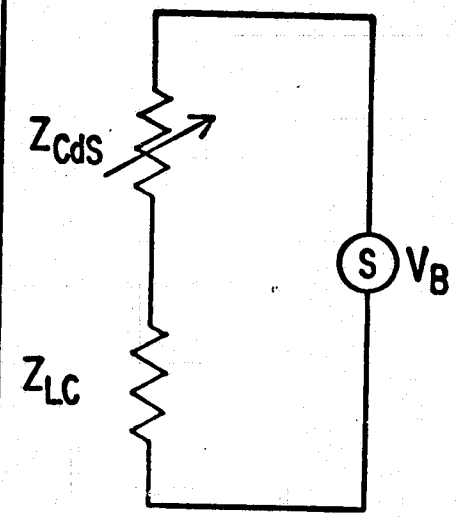
FOR ANALYZER ⊥ TO POLARIZER :

$$C_{ij} = \bar{A}_{ij} \wedge B_{ij}$$

FIGURE 12. OPERATION OF ONE RESOLUTION ELEMENT OF AN OPAL DEVICE



(A)

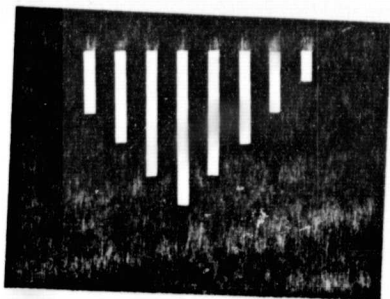


(B)

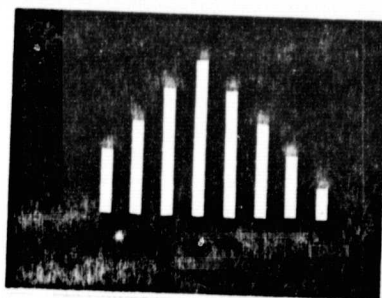
FIGURE 13 (A) THEORETICAL AND EXPERIMENTAL $I_{IN} - I_{OUT}$ CURVES FOR A SINGLE CELL OF AN OPAL AND GATE. I_{IN} IS THE NORMALIZED LIGHT INTENSITY ON THE CdS PART OF THE CELL AND I_{OUT} IS THE NORMALIZED LIGHT INTENSITY TRANSMITTED THROUGH THE CELL AND THE ANALYZER.
 (B) THE EQUIVALENT CIRCUIT DIAGRAM FOR THE SINGLE CELL OF AN OPAL DEVICE

OF HIGH QUALITY
 MADE IN

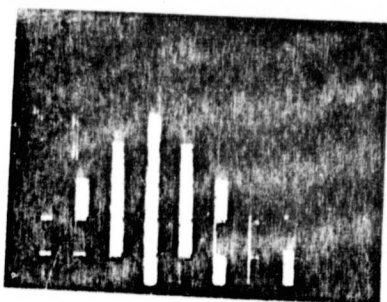
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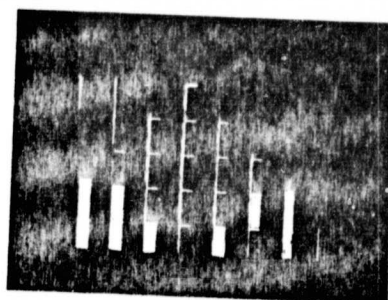
INPUT IMAGE A



INPUT IMAGE B



$A \wedge B$ (ANALYZER II)



$\bar{A} \wedge B$ (ANALYZER I)

Figure 14 Photographs of the inputs and the outputs of an OPAL device

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{SUM} = A \oplus B$$

$$\text{CARRY} = A \wedge B$$

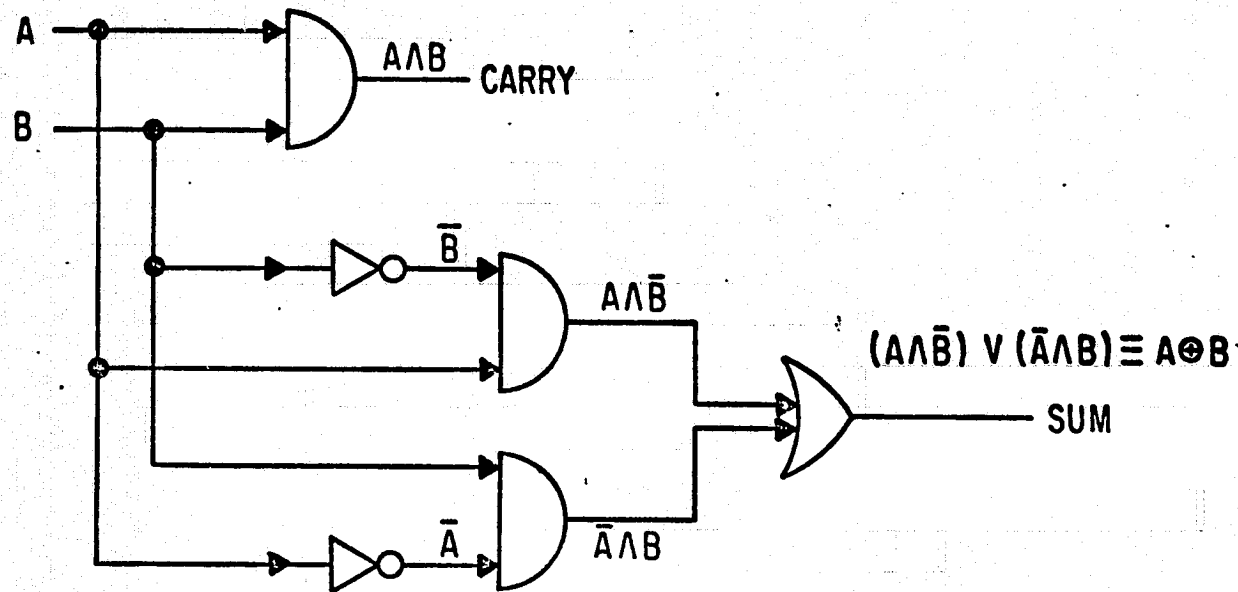


FIGURE 15. TRUTH TABLE FOR A HALF-ADDER CIRCUIT AND IT'S IMPLEMENTATION USING AND, OR, AND NEGATION GATES.

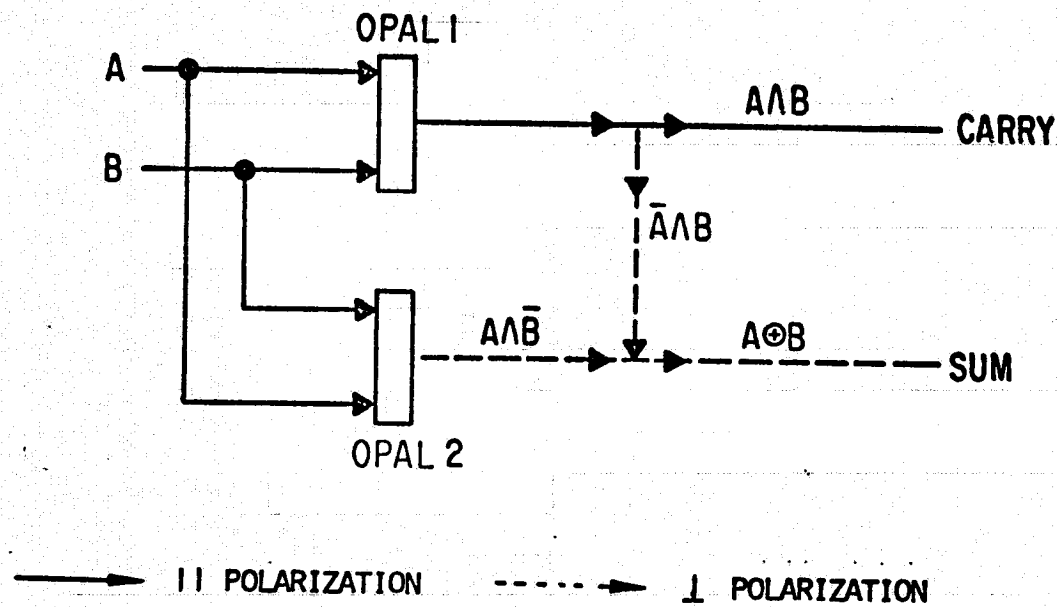
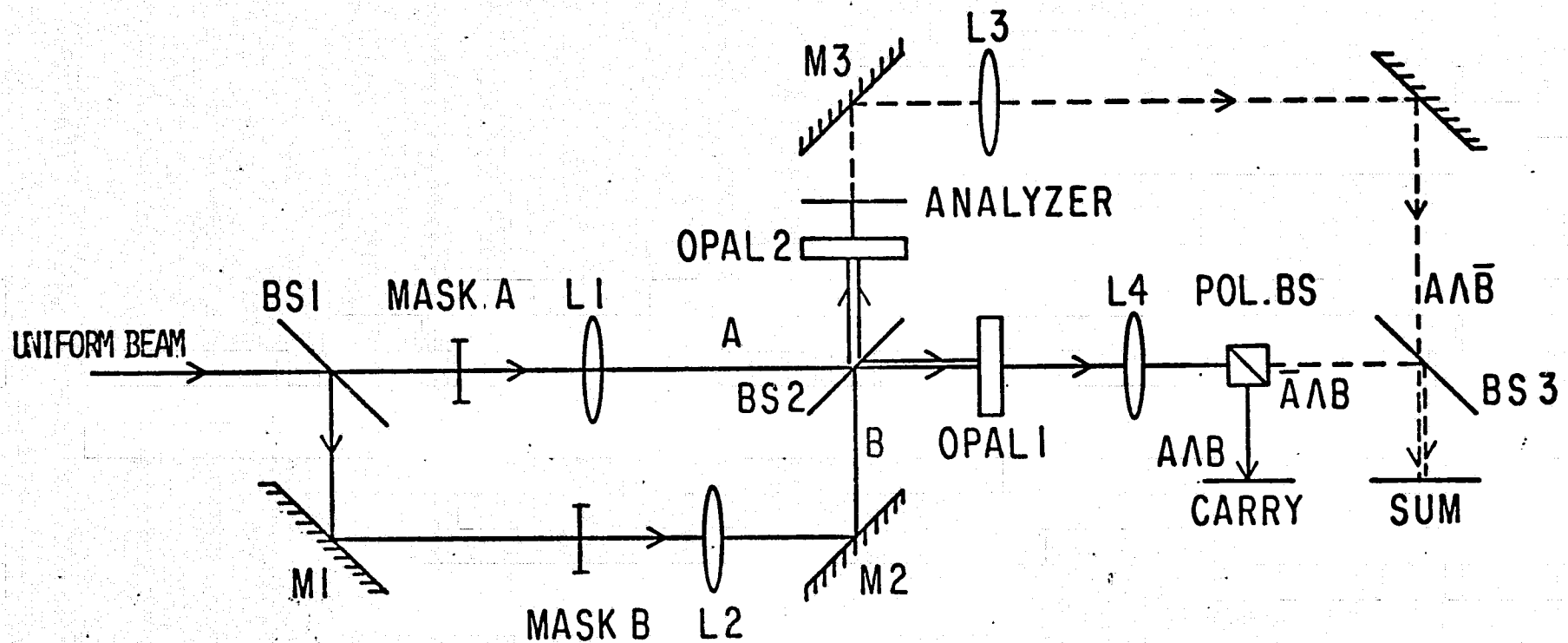
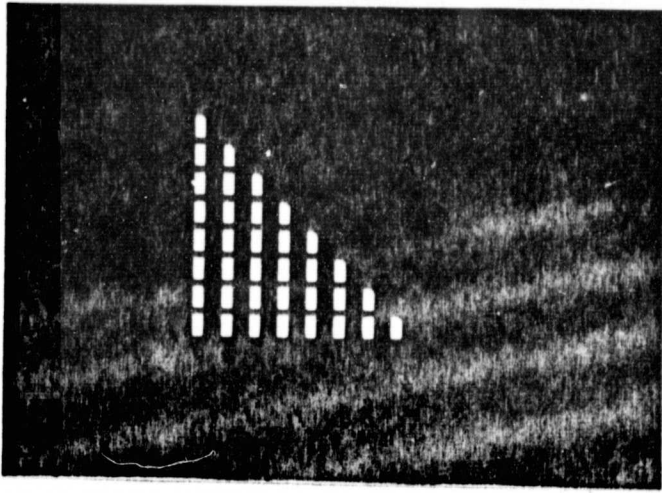


FIGURE 16 SCHEMATIC DIAGRAM OF A HALF-ADDER CIRCUIT IMPLEMENTED WITH TWO OPAL DEVICES.

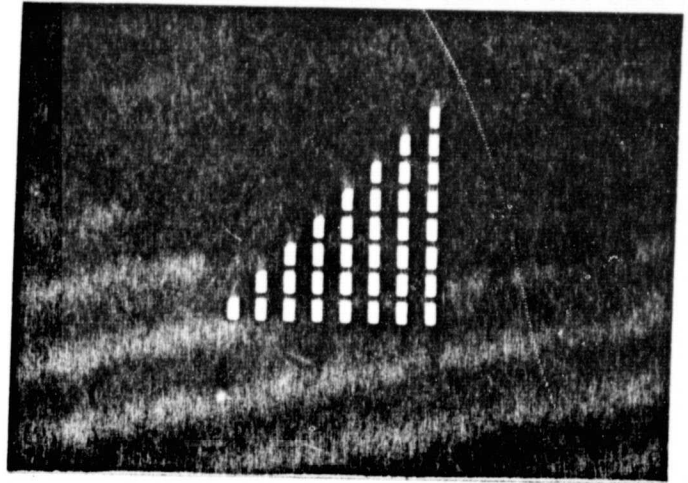


BS - BEAMSPLITTER , POL. BS - POLARIZING BEAMSPLITTER , M - MIRROR
 L - LENS , — || POLARIZATION , ---- ⊥ POLARIZATION

Figure 17 Optical Arrangement of a Half-adder Circuit

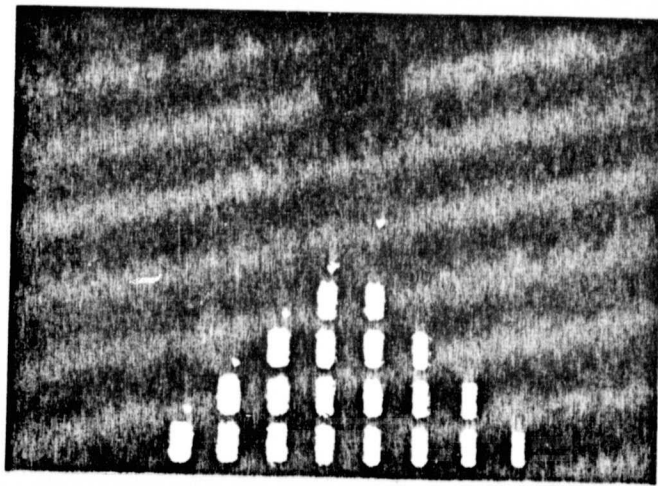


MASK B



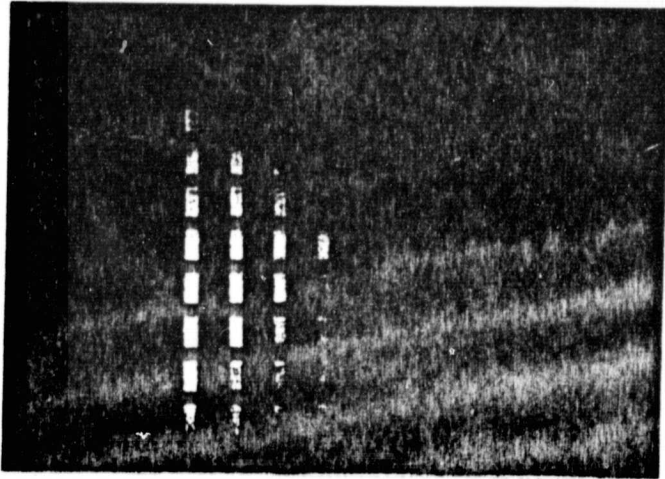
MASK A

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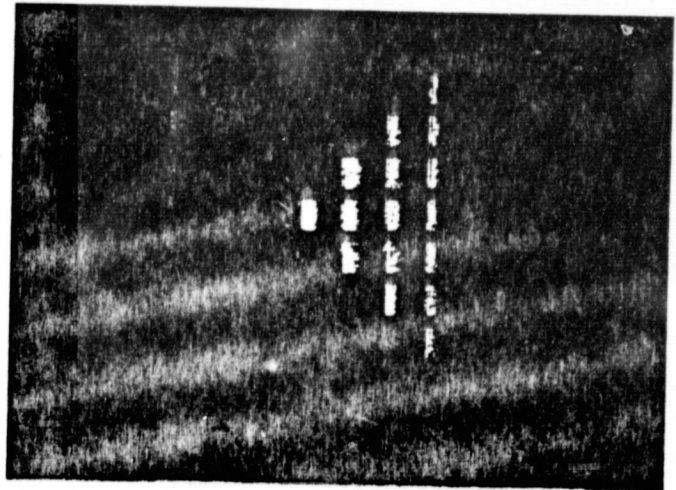


CARRY OUTPUT ($A \wedge B$)

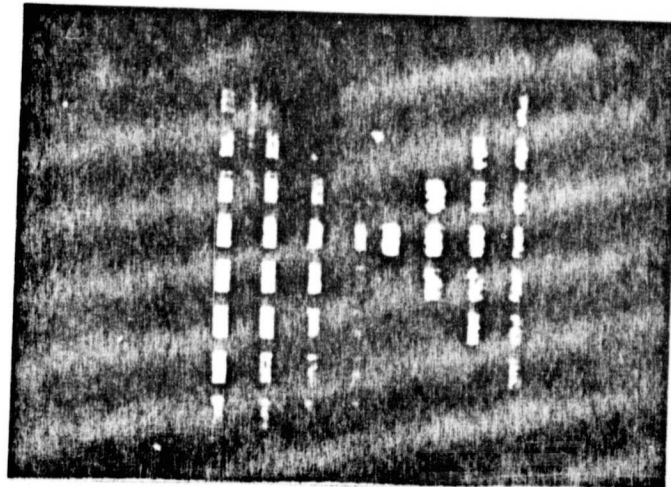
Figure 18 Photographs of the input masks and the CARRY output of the half-adder circuit implemented with OPAL devices.



$\overline{A \wedge B}$



$\overline{A \wedge B}$ ORIGINAL PAGE IS
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SUM OUTPUT ($A \oplus B$)

Figure 19 . The photographs of the two parts of the EXOR operation and their superposition. This superposition corresponds to the SUM output of the half-adder circuit.

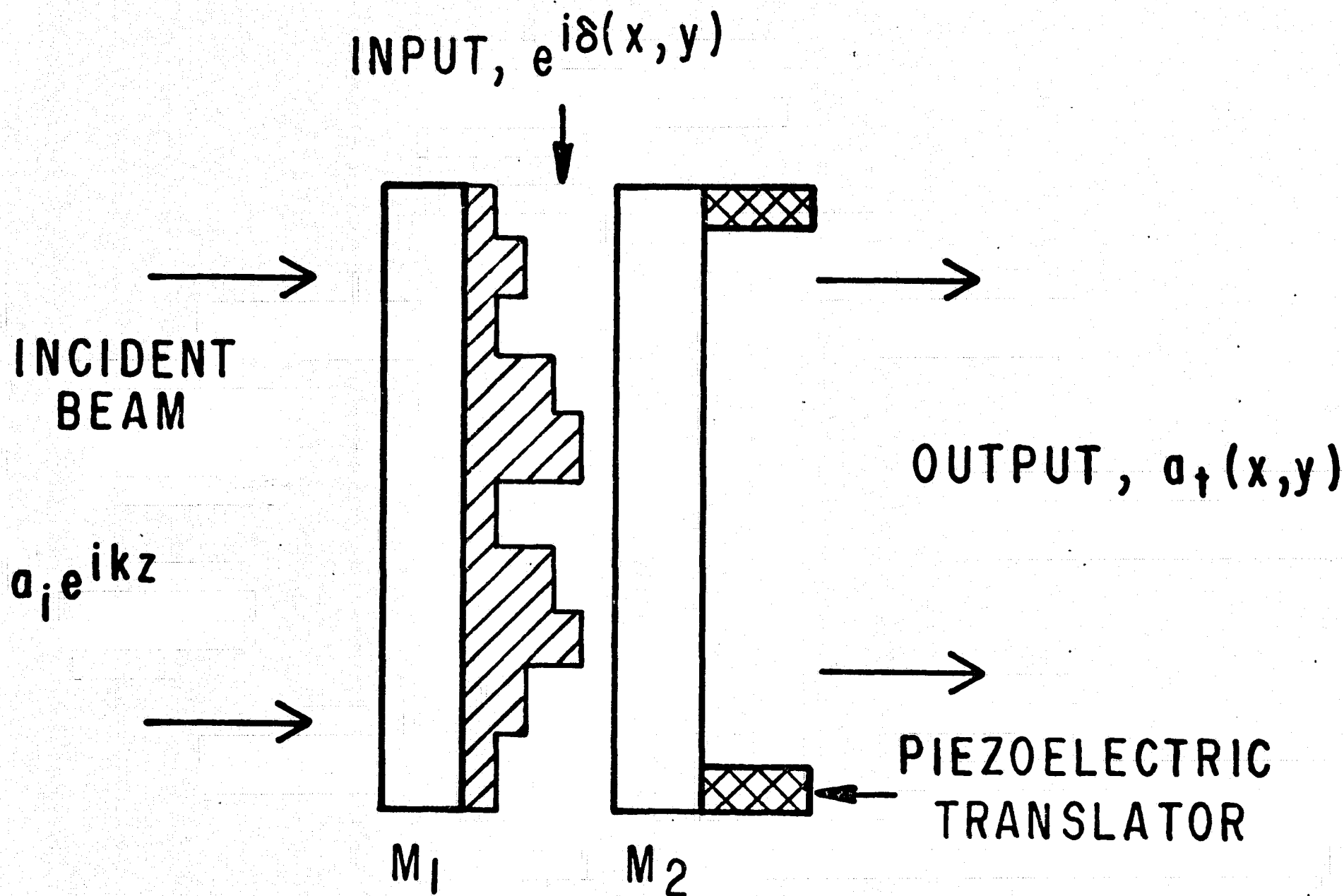


Figure 20 Plane parallel Fabry-Perot phase object processing system. The input image is recorded as a phase object $e^{i\delta(x,y)}$ which is mounted between two mirrors. The system is illuminated with a beam from a single mode laser and the interference properties of the Fabry-Perot cause the light to be transmitted only in those areas where $kd + \delta(x,y) = \delta\pi$.

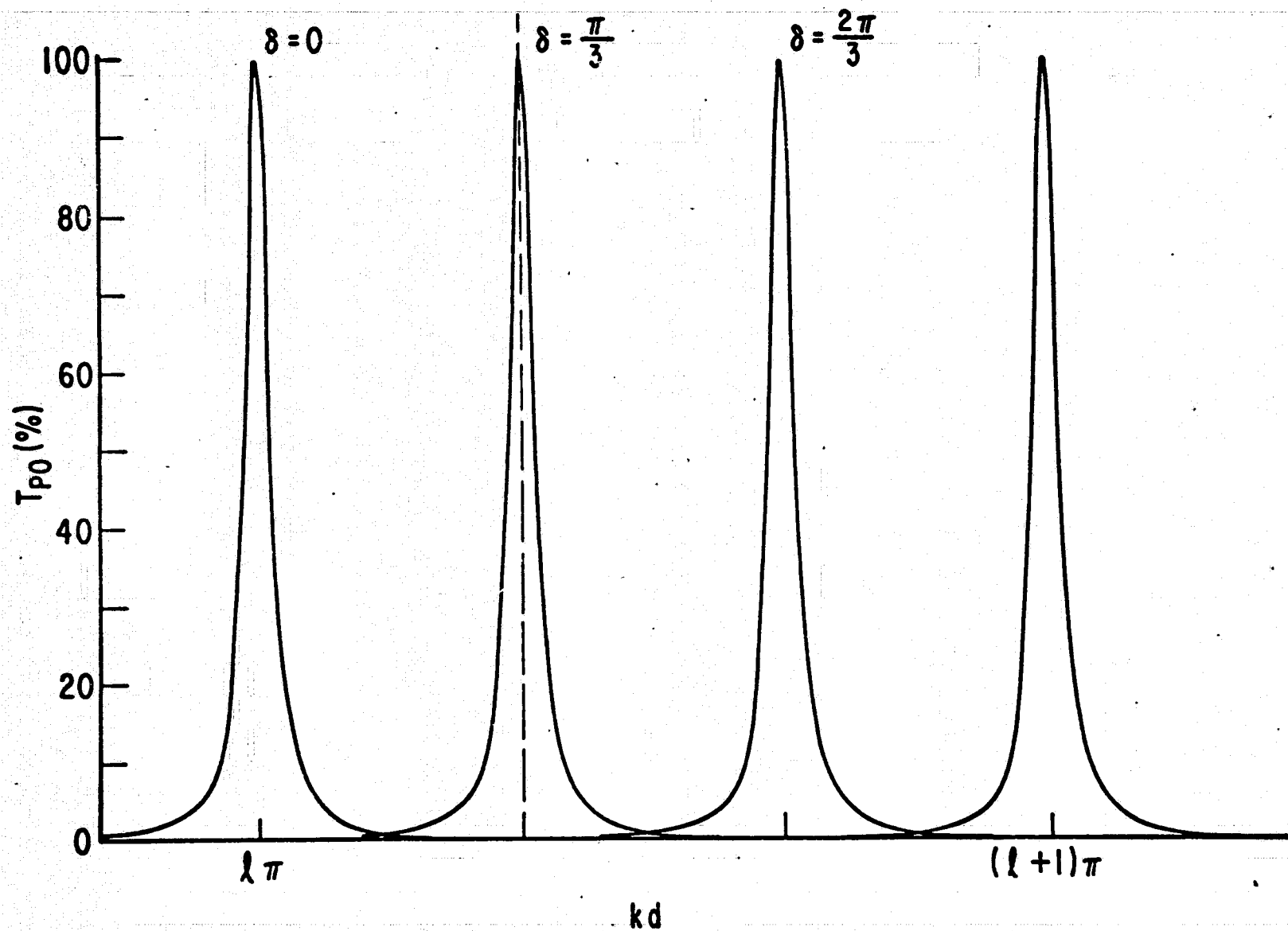


Figure 21 Transmittance function of the Fabry-Perot with phase object. T_{P0} is plotted as a function of kd for different δ 's. The vertical line illustrates intensity level selection. For what value of kd , those areas in the image where the intensity produced a phase shift $\delta = \pi/3$ will transmit light and the other areas are dark. Changing kd selects a new intensity level.

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(a)



(b)



(c)

Figure 22 (a) Original image. (b) Output of device with mirrors tilted slightly. (c) Output illustrating intensity level selection. Extraneous fringes caused by interference effects between mirrors and glass plate.

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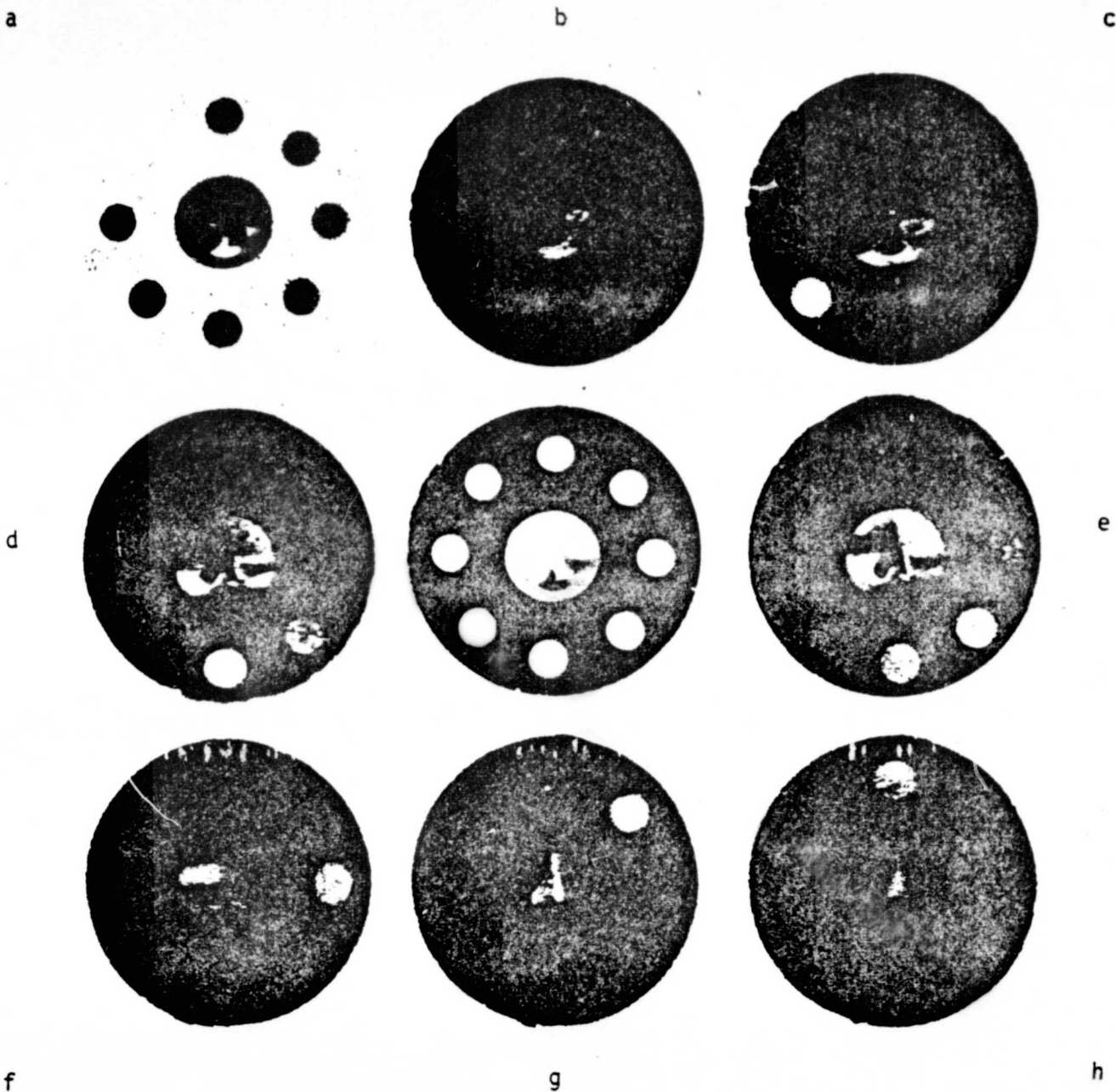


Figure 23 Intensity level selection with the plane parallel system. The central image is gray tone input. Eight dots around the outside were given different exposures to make a gray scale. The dot at 12 o'clock had the highest exposure equal to the exposure of the funnel. The dot at 10:30 had zero exposure. Eight intensity levels are selected with intensity increasing left to right, top to bottom.



Figure 24 Analog-to-digital conversion. A/D conversion of the gray tone image in Fig. 3. The most significant bit plane is on the left. The least significant bit plane is on the right. The intensity level for any point in the original can be found from these three binary images (see text).