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NASA TECHNICAL MEMORANDUM

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A PROGRAMMABLE POWER PROCESSOR FOR A 25-kW POWER MODULE

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LIST OF ABBREVIATIONS

BAT	Battery
CHG	Charger
C/I	Controller/Interface
CMD	Command
DAC	Digital to Analog Converter
DAS	Data Acquisition System
DC	Direct Current
EMI	Electromagnetic Interference
EPS	Electrical Power System
PIA	Peripheral Interface Adapter
PPG	Power Processing Group
PPS	Pulses per Second
PROG	Program
PWR	Power
P^2	Power Processor
P^3	Programmable Power Processor
RAM	Random Access Memory
REG	Regulator

LIST OF ABBREVIATIONS (Concluded)

ROM	Read Only Memory
SA	Solar Array
S. O. C.	State of Charge
TM	Telemetry
USART	Universal Synchronous/ Asynchronous Receiver Transmitter
VDC	Volts Direct Current
V_{in}	Input Voltage
V_{out}, V_o	Output Voltage
μP	Microprocessor

TECHNICAL MEMORANDUM

A PROGRAMMABLE POWER PROCESSOR FOR A 25-kW POWER MODULE

INTRODUCTION

Anticipation of the advent of the Space Shuttle with its associated low cost space travel has sparked the imagination of the scientific and industrial communities. Their enthusiasm is only slightly dampened by the realization that the time duration and energy available for experimentation are somewhat limited in the Shuttle. These limitations are primarily the result of the use of fuel cells as the Shuttle Orbiter's primary power source. Limited volume for stowage of fuel cell consumables dictates these limitations. These considerations have led NASA to investigate the possibility of using a 25-kW Power Module (Fig. 1) with solar arrays as a primary energy source to provide electrical power and energy, thus allowing much longer duration missions and higher power experiments.

A study was made to define the approach for an Electrical Power System (EPS) with requirements to supply 25 kW to the Shuttle Orbiter and housekeeping requirements of 2 kW for 5 years with little or no maintenance. These requirements are for more than three times the power and seven times the life of the Skylab EPS, which was the largest EPS of this type orbited to date. A comparison of systems using Skylab hardware with new systems using high voltage solar arrays and batteries and new technology components revealed EPS savings on the order of $13M for cost, 2800 kg for weight, and 1 kW for EPS power losses with the new high voltage system. The Orbiter dictates that the system output remain a nominal 28 Vdc.

A programmable power processor (P^3) which can meet the requirements for the 25-kW Power Module as well as a wide range of other potential applications was envisioned, and development effort has begun [1]. A single power processor (P^2), capable of having its output characteristics programmed by an internal microcomputer using a microprocessor central processing unit, is proposed. With an input voltage up to 400 V and an output voltage ranging from 28 to 170 V, at up to 100 A, the P^3 offers a unique challenge. However, the promised savings indicate that the challenge is worth accepting.

The concept of programming a switching regulator was demonstrated in 1976 on a basic 30-V regulator under microprocessor control. The output voltage, voltage droop (output impedance), and output current were all controlled by merely reprogramming the microprocessor. This definitely proved the feasibility of such a device. The next step was to select power and voltage ranges to provide the broadest range of applicability without exceeding available component technology. A look to the future, which will have even larger power requirements, led to the conclusion that a nominal 10-kW, 100-V output power processor would be reasonable. The 25-kW Power Module which emerged in this time frame, being an ideal application for the P^3, helped in making this decision. A breadboard was assembled with the battery charger and regulator capability. Test results from this breadboard P^3 are discussed in the following paragraphs.

A PROGRAMMABLE POWER PROCESSOR BASED POWER SYSTEM

The power system configuration is modularized from the power source to the output busses (Fig. 2). A specific portion of the solar array is dedicated to one charger/battery/regulator system or Power Processing Group (PPG). The charger in each PPG will process all of the power from its solar array section, using all power not required by the bus regulator to charge the battery. When the bus power requirement exceeds available solar array power, the charger will deliver the maximum available solar array power and the battery will make up the balance. The power voltage levels and regulator design were chosen in anticipation of future large space power systems using higher voltage distribution networks. Evaluation of requirements led to the decision to specify operation over an input voltage range of 30 to 400 Vdc and an output voltage of 24 to 180 Vdc programmable. The output current is specified as 100 A maximum programmable. The power stage of the P^3 uses three 100-A, 500-V transistors in parallel stages to meet these requirements.

The switching power processors are of the standard "buck" configuration. When used as chargers they will operate with a nominal input of 180 to 360 Vdc and an output of 120 to 170 Vdc. When used as a bus regulator they will use the 120 to 170 Vdc as an input to generate the required bus voltage. Data discussed below show the efficiency of the P^3 for these conditions and for operation into a medium voltage bus (100 to 130 V).

If the bus voltage is a nominal 115 Vdc, it is apparent that the buck configuration is a good choice for the regulator and charger. However, as noted, the required bus output is 30 Vdc and the buck configuration is not the most efficient way to accomplish such a large voltage reduction. In spite of this it is considered cost effective for the 25 kW Power Module to use the approach that identical regulators can be used effectively for the charger and regulator with only the nominal output voltages being different, thus saving development costs. The reduced efficiency from utilizing the same power component configuration in the charger and regulator is minimal and is considered preferable to developing a different bus regulator whose technology might not be applicable to future high voltage distribution systems.

A disadvantage to using the buck configuration for the bus regulator is the problem of protecting the loads from over-voltage in the event of regulator failure. In the 25-kW Power Module this will be accounted for with a shunt regulator on the load bus to clamp the voltage until protection devices can clear a failed regulator off the line. This method was successfully used on one of the primary power systems on Skylab and has the added benefit of clamping the bus during any unforeseen transient condition.

Microprocessor Control

The task of two identical regulators performing different functions is satisfied by microprocessor control. Experience with large space power systems, such as Skylab, indicates a need for greater flexibility in EPS management. Microprocessor-controlled regulators and chargers provide this capability. In the future, the P^3 could be a key element in a self-managing space power system. However, such onboard computer management of the entire EPS has not been proposed for the 25-kW Power Module. The development time and cost prohibit its implementation within the desired time frame. However, development of a P^3 is considered an essential first step towards this goal. The expertise gained in utilizing its flexibility through ground control will provide a data base for developing self-management concepts.

Microprocessor control of a regulator has been demonstrated using an Intel 8080 and a Motorola 6800 based system. The microprocessor system acts as a controller/interface (C/I) which exercises its primary control through a digital to analog interface with the regulator or P^2. This programmable voltage

will be used as a reference adjust voltage in the analog feedback loops of the P^2. The C/I will accept up to 16 analog inputs for data needed for determining its program voltage output and also for generating its outputs to the spacecraft telemetry data bus. All other C/I interfaces are digital: a command and data bus interface with the spacecraft and miscellaneous discrete interfaces with its P^2 and other power elements in the PPG. A block diagram of the C/I will be used in the first PPG breadboard is shown in Figure 3. Determination of the digital hardware for a final development unit is being delayed until a final configuration is defined. Preliminary software has been developed for both P^3's in the PPG.

The battery charger's primary function is to make all of the solar array power available to the battery and regulator. With the charger output and the bus regulator input connected to the battery, the charger must determine the maximum solar array power available and deliver it to the battery terminals. The bus regulator will draw what it needs and the excess will recharge the battery. The charger draws the maximum solar array power by "hunting" for the peak power point on the solar array voltage/current output characteristics. The charger P^2 will use the programmed voltage reference to control its input current while the C/I will periodically vary the program voltage to determine if more input power is available at a higher or lower input current. This peak power tracking will continue as long as the battery parameters indicate that it can accept any excess power. The C/I will be monitoring the battery parameters and will determine when to terminate peak power tracking and control the charger P^2 input current to cause a constant output voltage. This will taper charge the battery until it is completely recharged. The constant output voltage programmed will be dependent upon the battery temperature. Full recharge is when all ampere hours removed on discharge are replaced, including a predetermined extra amount to account for charge/discharge inefficiencies. The C/I will perform a time integration of the battery current to determine the battery's state of charge. A simplified flow diagram of the software for the development P^3 charger is shown in Figure 4. Software for this program has been written and implemented on a breadboard P^3 [2].

The bus regulator will use the programmed reference to control its output voltage. Its software will be comparatively simple: the C/I will monitor the output current and vary the output voltage to present a programmed source impedance to the load bus. This will help the PPG's share the load. Another function that will be monitored for real-time control is an output from a battery protection circuit. This will indicate if several battery cells can no longer

carry the load, and the C/I will then reduce the programmed output voltage to reduce the load on the battery. This software has also been written and tested successfully [2].

The delays in software execution prevent the C/I from being effective in controlling power component stresses under fault conditions. Thus, the P^2 will be current limited by an analog feedback within the power stages. This still allows programming an average output current control through programmed voltage control.

Power Processor

The P^2 (Fig. 5) is a challenge in several areas: power transistor stresses, optimum capacitor bank configurations, thermal control, and compatibility at the digital system with the switching electromagnetic interference (EMI).

The peak voltage stresses are the first concern because component current levels can be reduced by adding parallel power elements. To minimize peak voltages, a decision was made to design the buck power stage for operation to 100 percent duty cycle. This requires a base drive that is always sufficient for maximum loads rather than a simpler more efficient current feedback base drive technique which requires a minimum OFF time to reset the magnetics.

Three parallel power stages, operated phase-sequenced with each power transistor having its own commutating diode and filter inductor, are used to provide the 100-A output. This presumes the availability of transistors that can switch 50 A at 400 Vdc with established reliability and adequate speed. At this time only two candidate transistors have been investigated. A Westinghouse device, the D60T type, developed under a NASA LeRC contract shows the most promise. The transistors were tested in a breadboard of one power stage with the results extrapolated for a full P^3 as shown in Figures 6 through 10. In those cases where the efficiency is not plotted to 100 A, the reason was because of a lab power limitation. Facility modifications are currently being made to permit testing of a full scale P^3 recently completed to its rated output power. The data presented show that the P^3 used as an output regulator for the Power Module will operate between 88 and 90 percent most of the time (Fig. 6). Figures 7 and 8 are typical of operation into a medium voltage bus (100 to 130 V) that might be used on a 100- to 500-kW space power system. There the efficiency would be

nominally between 96 and 98 percent. Figures 9 and 10 are typical of a minimum and maximum charger output voltage for either system (only the output current would differ). Again, the nominal output efficiencies are 96 to 98 percent.

The power stages run at a fixed frequency of 10 kHz with the ON time variable up to 100 percent. Balancing the load and maintenance of proper phasing between power stages is easier to implement under constant frequency control. The ON time for each power stage is determined by a comparison of two signals: one a function of the particular transistor current, the other dependent on the output voltage error and current in the output filter capacitors. The latter signal will be common to all power stages, thus insuring balanced loading. Utilizing the switching transistor current in the control scheme allows minimum delay time in limiting the peak stresses in the transistors. Optimization of the feedback is simplified by not having to account for rapid changes in the source characteristics of either regulator. Response to step changes of the output load is the major consideration.

The input filter bank in the breadboard P^3 is currently planned to be a series-parallel combination of tantalum cased tantalum wet-slug capacitors. This arrangement is far from ideal, but it offers high density energy storage capability and meets NASA/MSFC specified reliability and design criteria. The development of improved film capacitors is being watched in anticipation of their eventual use in this area. For the input filters a limited reduction in capacitance will be acceptable if there is a significant improvement in the dissipation factor; the filter currents are highest on the input side of a buck regulator.

The output filter requirements put a premium on large capacitance values; there are minimal high frequency components in the output filter current but, with step load changes, the capacitors need to limit the excursions of the output voltage. In this application the series-parallel tantalum capacitors may still be the optimum solution.

The basic mechanical design of the P^3 will be driven by the need to limit the junction temperatures of the main power transistors. The dissipation in each junction will be approximately 200 W at maximum load, which requires low thermal resistance from case to heat sink as well as from junction case. A separate packaging study is being performed to evaluate this.

Packaging of the power processor will also concentrate on minimzing the length of the loops that carry currents with high di/dt components. The major source of this type of EMI is the path including the input capacitors, switching transistor, and the commutating diode. The source of the highest dv/dt EMI is the base drive circuitry which is referenced to the emitter of the switching transistor. Care in the layout of those two areas should minimize the need for filtering in the interfaces between the P^2 and the C/I. These problems are also the subjects of the study dedicated to packaging the P^3.

CONCLUSION

The need for higher voltage levels and programmable power processing in the space power systems envisioned for the future is self-evident. The scale of the 25-kW Power Module presents an opportunity for development of technology that will relieve the growing energy demands on the Shuttle and aid in designing the larger electrical power systems that will be needed later. For example, by increasing the load bus voltage to 120 V and providing larger energy sources and storage, the P^3 regulators (discussed herein), reprogrammed for 120 V output, provide 144-kW peak power to the load busses. The outline of the power processing elements being developed for the 25-kW Power Module indicates the major design problems and how the proposed configuration addresses those problems. In general, the design does not require drastic advances in state-of-the-art components but rather a maturing of current technology to the established reliability realm.

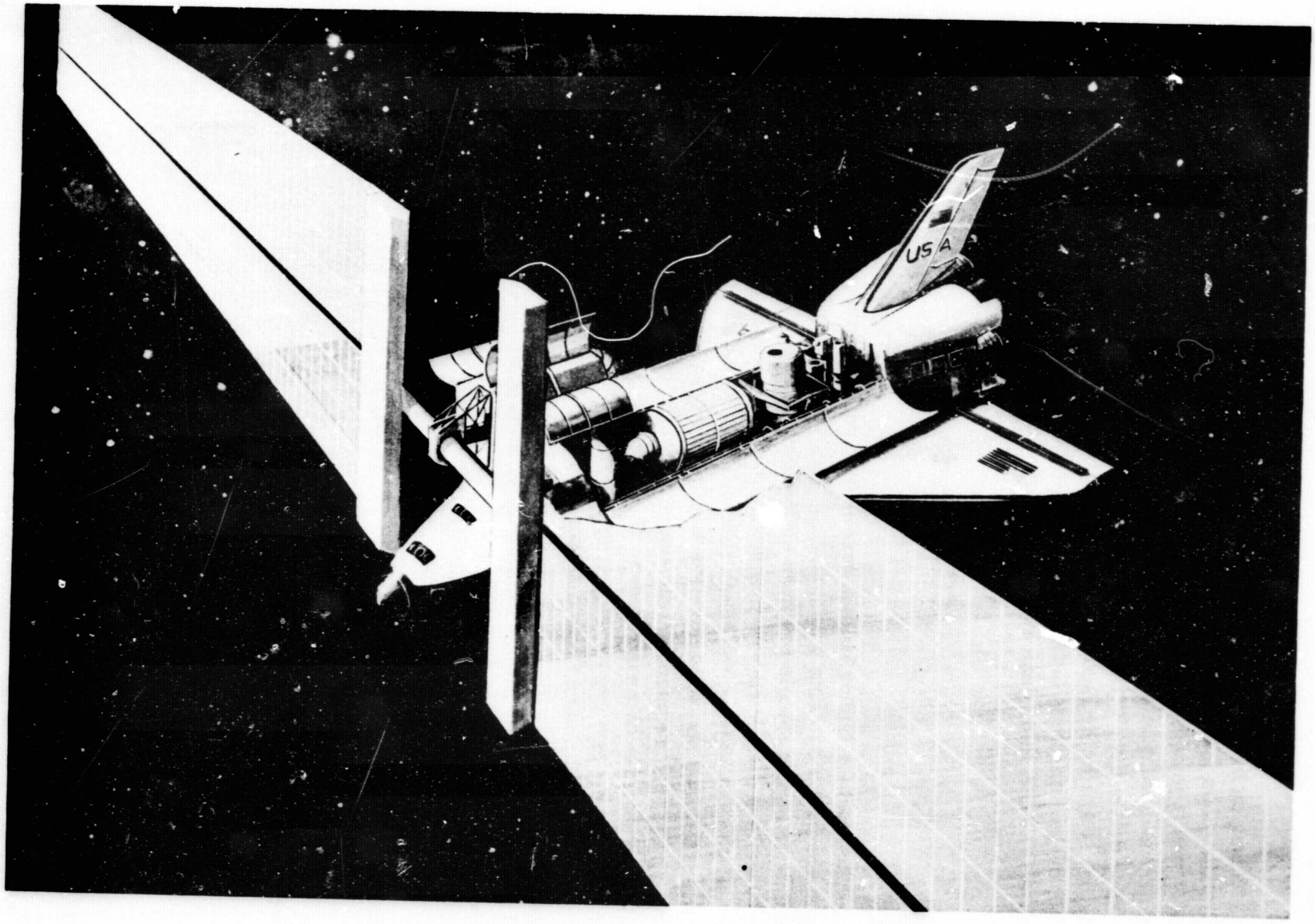

Figure 1. Power Module.

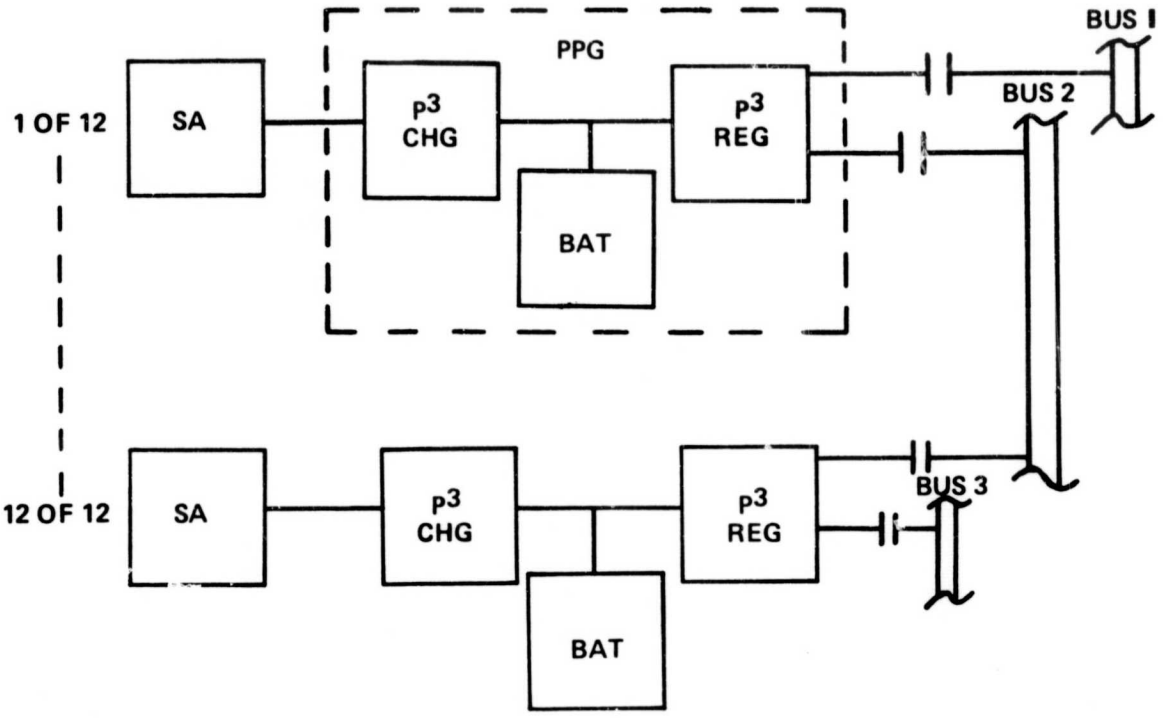

Figure 2. EPS configuration.

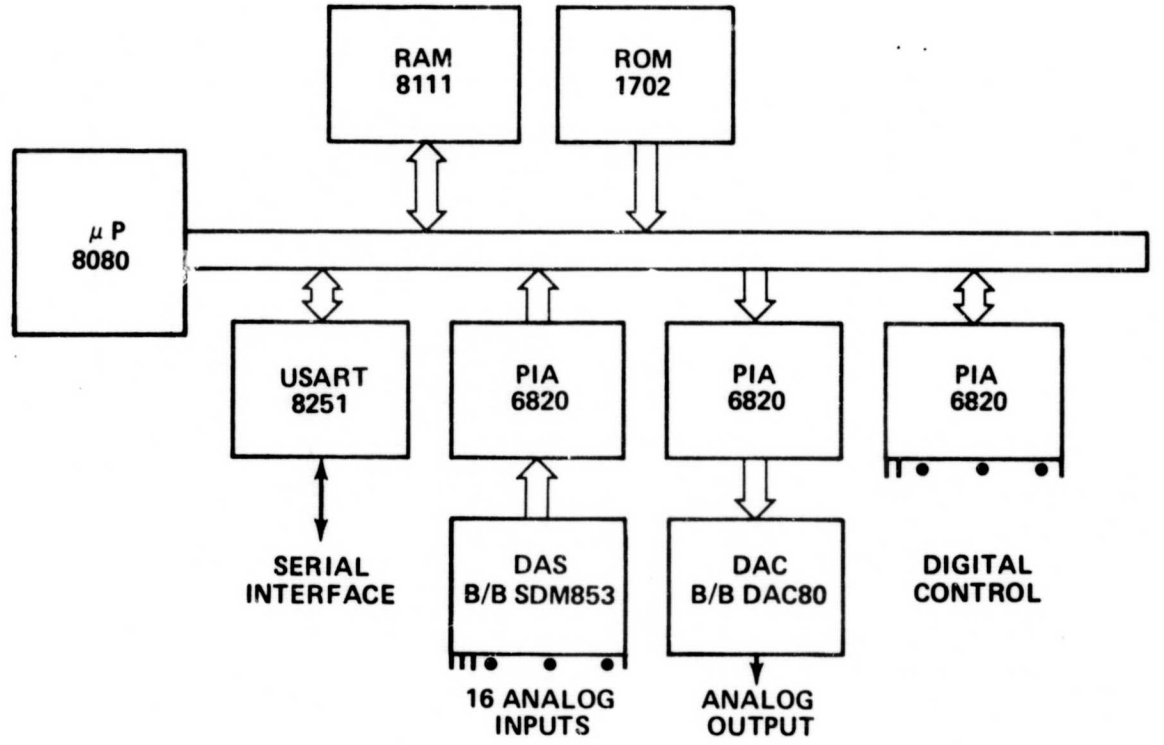

Figure 3. C/I block diagram.

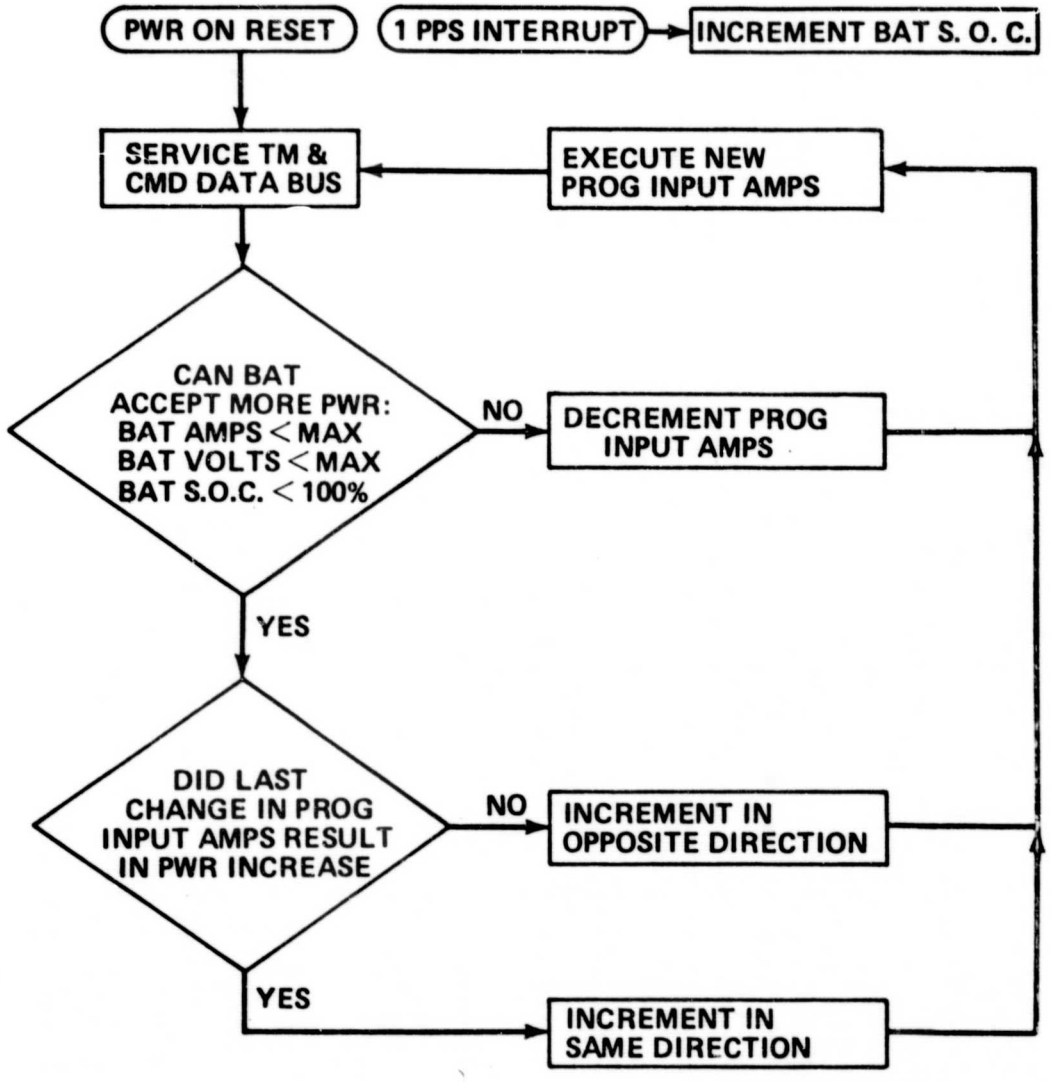

Figure 4. Simplified charger software flow diagram.

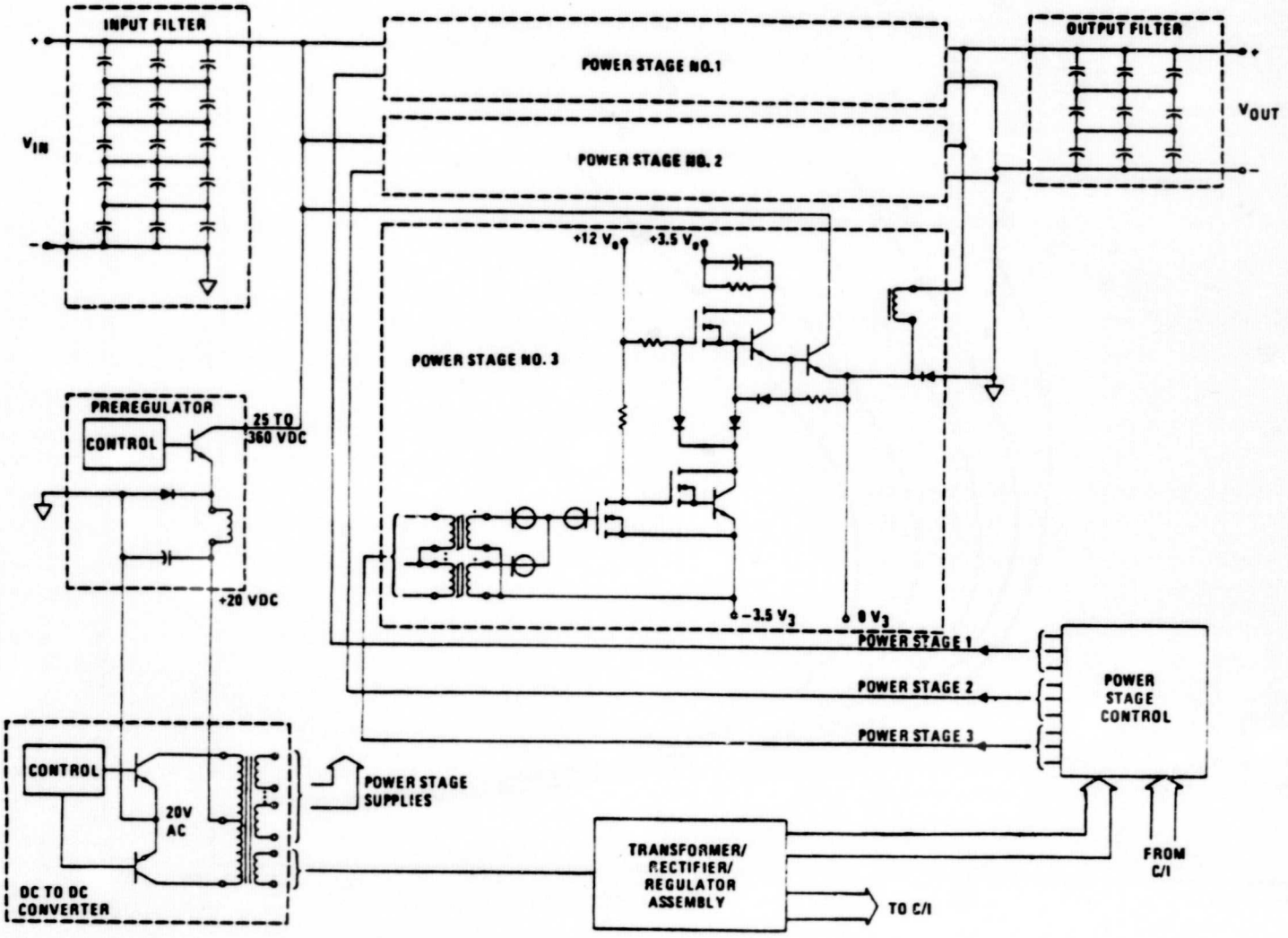

Figure 5. P^2 block diagram.

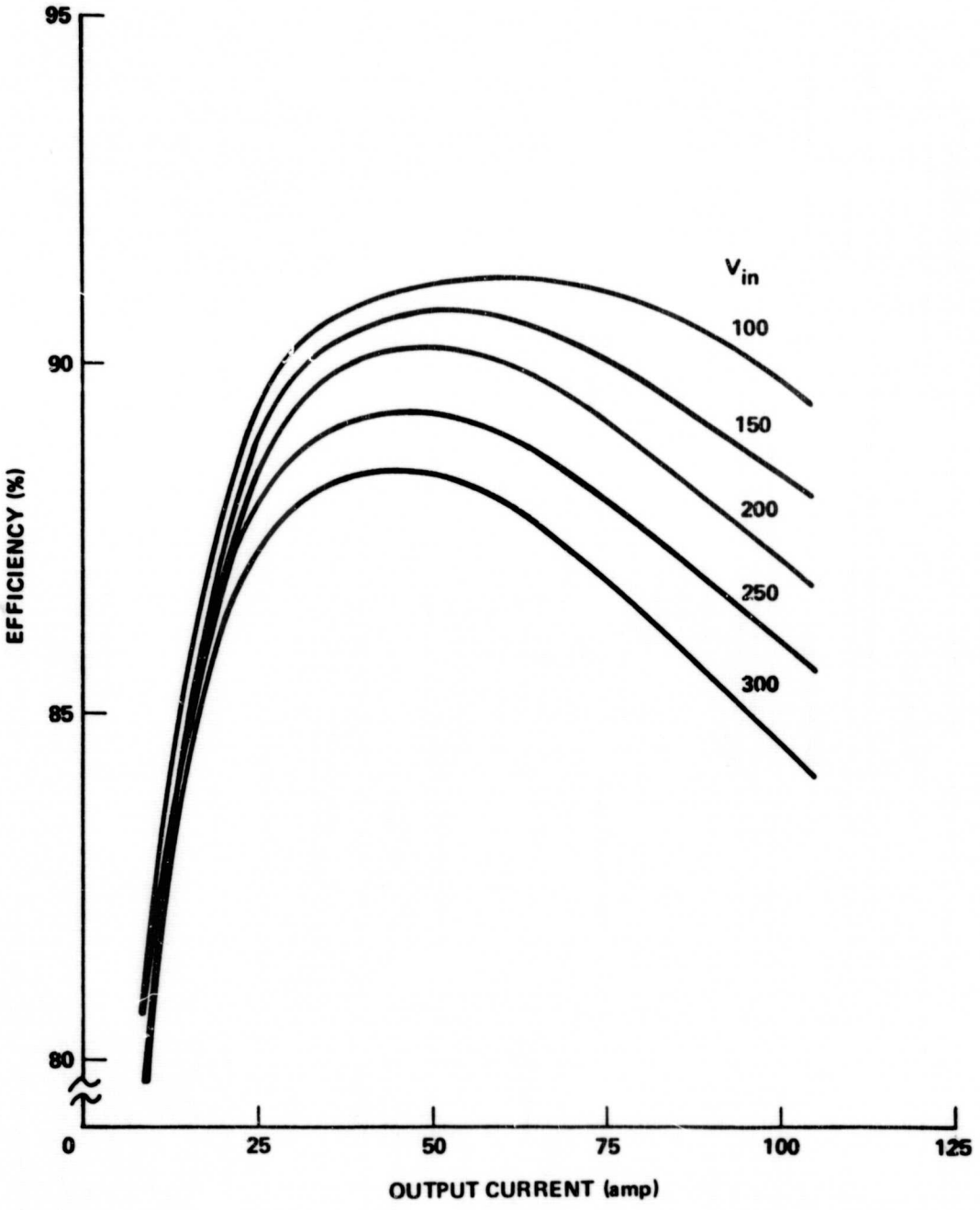

Figure 6. Efficiency versus output current at V_o = 30.0 Vdc.

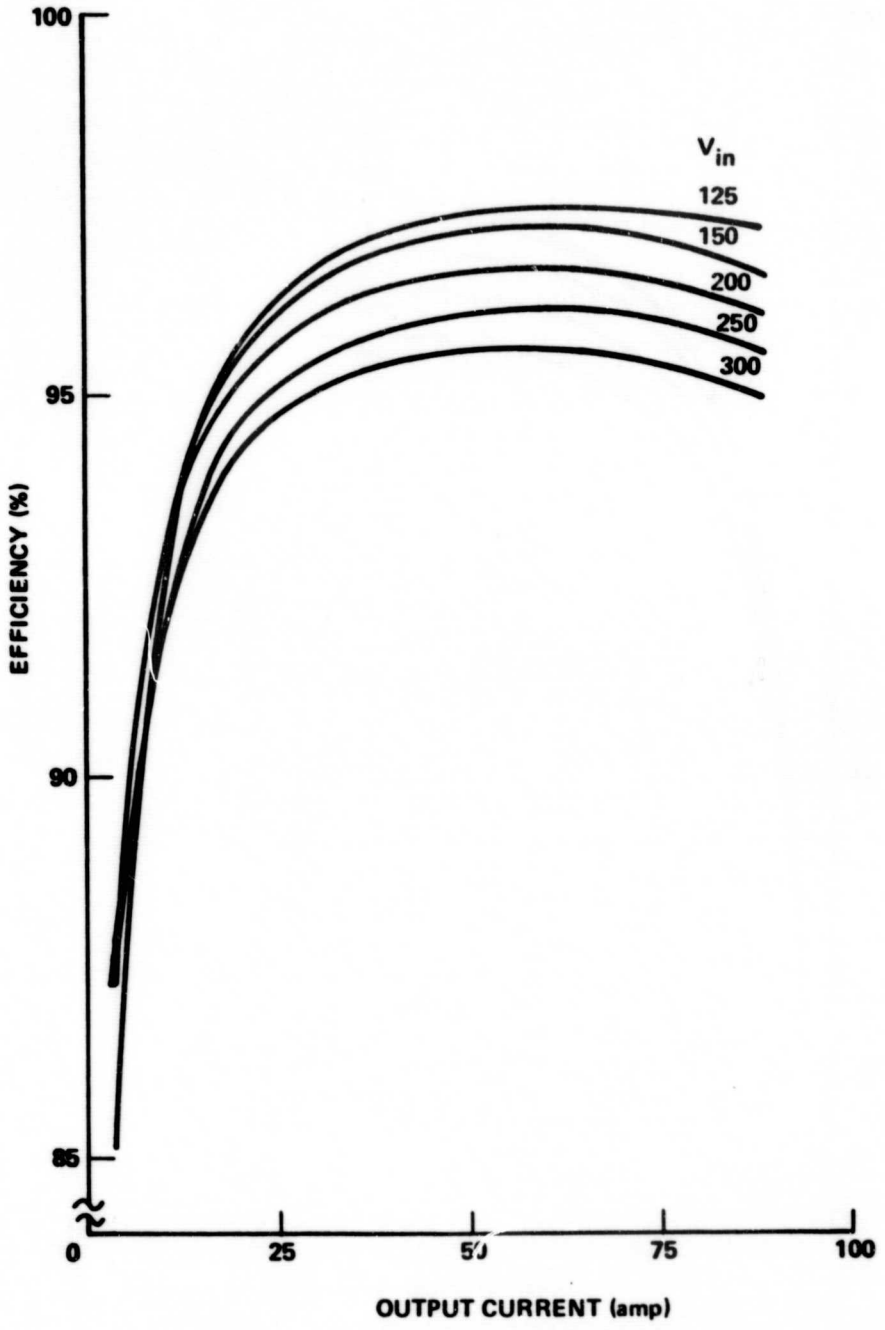

Figure 7. Efficiency versus output current at V_o = 115 Vdc.

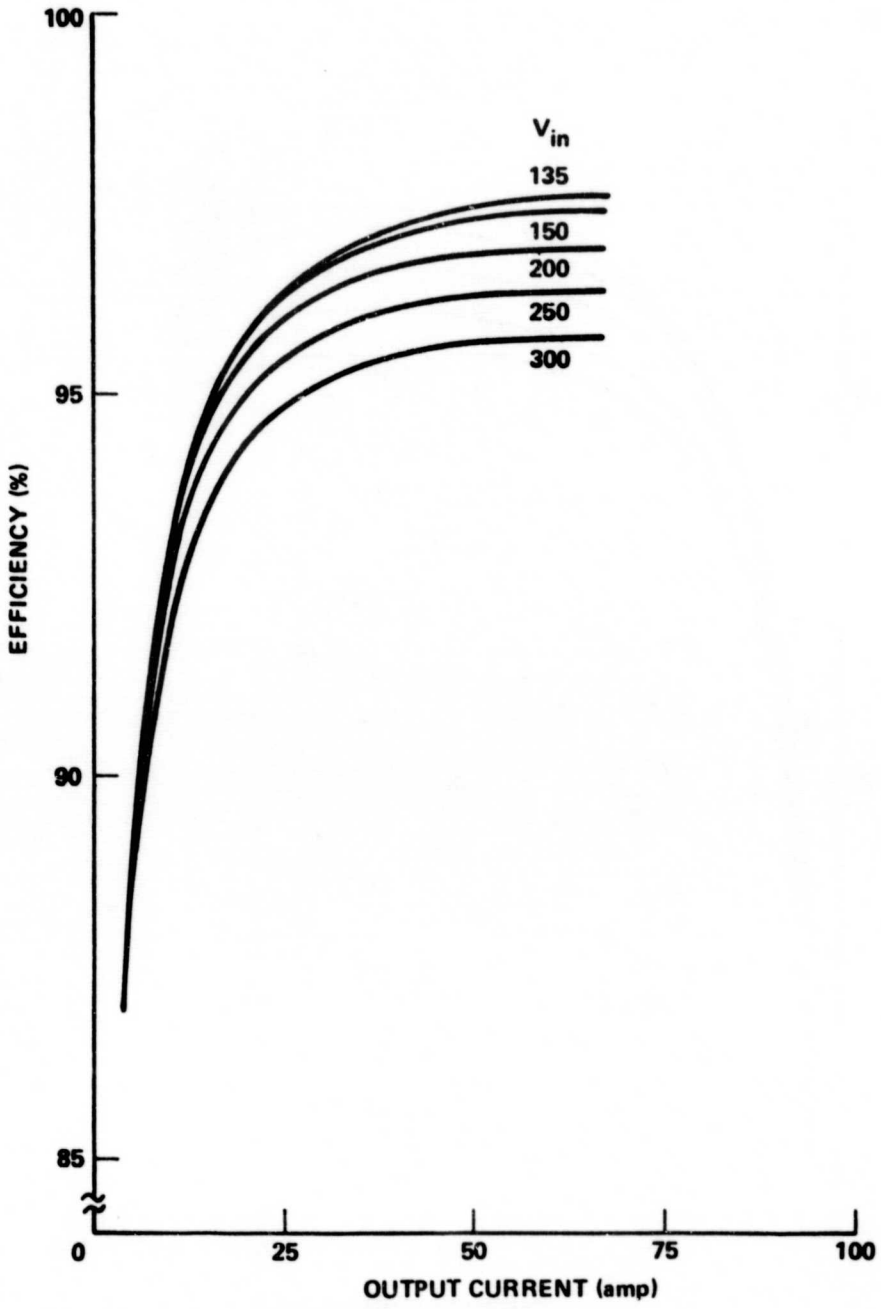

Figure 8. Efficiency versus output current at V_o = 125 Vdc.

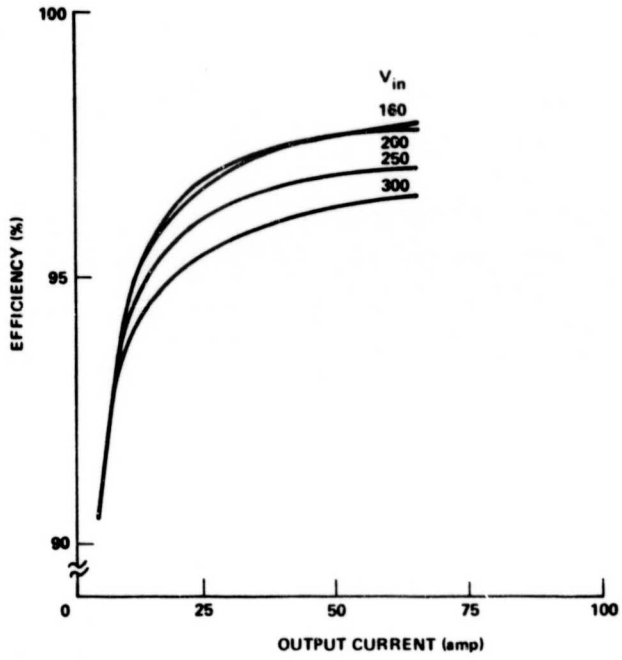

Figure 9. Efficiency versus output current at V_o = 150 Vdc.

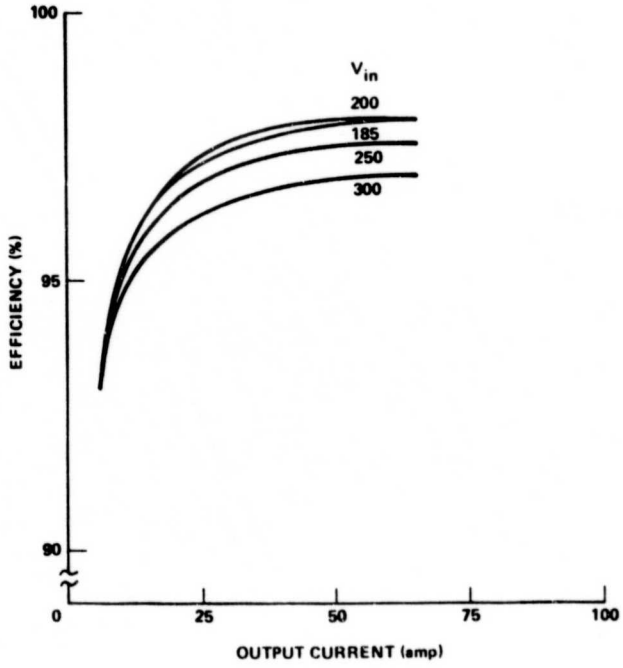

Figure 10. Efficiency versus output current at V_o = 175 Vdc.

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2. Green, David: Charger and Regulator Software for a Breadboard Programmable Power Processor. October 26, 1978.

APPROVAL

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The information in this report has been reviewed for technical content. Review of any information concerning Department of Defense or nuclear energy activities or programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

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