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DRL No. 82/DRD No. MA-3
Line Item No. 8

DOE/JPL - 955217 - 79/4
Distribution Category UC-63

DEVELOPMENT OF HIGH EFFICIENCY (14%) SOLAR CELL ARRAY MODULE

FIRST QUARTERLY REPORT

FOR PERIOD COVERING

29 NOVEMBER 1978 TO 15 MARCH 1979

BY

P.A. ILES, S. KHEMTHONG, S. OLAH,
W.J. SAMPSON, AND K.S. LING

JPL CONTRACT NO. 955217

OPTICAL COATING LABORATORY, INC.
PHOTOELECTRONICS DIVISION
15251 EAST DON JULIAN ROAD
CITY OF INDUSTRY, CA 91746

"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effect toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

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ABSTRACT

The development of the high efficiency, P/N solar cells has begun. The best efficiency achieved to date on the 3" diameter cell was 15.6% at AM1 and 28°C, slightly below that of 16.5% required for the fabrication of 14% efficiency module. Work is continuing on the cell development, with efforts concentrating on junction formation and back surface field application.

The design of the module was completed utilizing 120 3" diameter cells, Sunadex glass as the superstrate, polyvinyl butyral as the encapsulant, extruded aluminum channel for framing, and Teflon insulated flexible leads as the electrical terminals.

The design of the production tooling has been submitted for design review. The tooling consists of (1) back contact soldering machine, (2) vacuum pickup, (3) anti-reflective coating tooling, and (4) test fixture.

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1.0 INTRODUCTION

The initial phase of this program is to design and develop 3" diameter, P/N solar cells with the conversion efficiency of 16.5% or better at AM1 and 28°C. Upon completion of the cell development phase, OCLI is to design, fabricate, and deliver six (6) high efficiency modules, approximately 2' x 4', with a minimum output of 90 watts at AM1 and 28°C and with the design goal of 14% overall efficiency.

The second phase of this program is to design and fabricate production tooling for the manufacture of the high efficiency cells and modules. Twenty (20) verification modules are to be fabricated and delivered to JPL.

2.0 TECHNICAL DISCUSSION

The initial phase of the program is to optimize the processing parameters to produce a 3" diameter P/N solar cell with the conversion efficiency in excess of 16.5% at AM1 and 28°C. In parallel to the cell development, a low cost module is to be designed.

2.1 Description of the P/N Cell

The size of the solar cells is 3 inches in diameter by 0.015 inches in thickness. The bulk silicon is CZ grown, phosphorus doped, N-type single crystal with resistivity range between 7 and 14 ohm-cm. The wafers are chemically polished. Phosphorus is diffused onto the backside of the wafer to form a back surface field. The junction is formed by thermal diffusion using boron nitride as the source material.

The center contact and the grid pattern are applied by photolithography. The contact system is evaporated titanium-palladium-silver. A two layer (TiOx and Al_2O_3) anti-reflection coating is applied to the active surface of the cell to reduce the reflection loss. A final sintering cycle completes the fabrication of the cell. The major process steps are shown in the Flow Chart.

The front contact of the cell has a radial pattern as shown in Figure 1 (OCLI Drawing No. A-202337). It was found that the center contact design improved the collection efficiency and minimized the shadow loss of the active area.

2.2 Discussion of Key Parameters

2.2.1 Silicon Preparation

In order to make high efficiency solar cells the starting silicon must have certain properties, mostly good perfection (as indicated by minority carrier diffusion length) and controlled impurity addition to provide the required resistivity range (7-14 ohm-cm) which will give best output.

This is achieved by growing large (>6 Kg) well controlled N-type single crystals by the Czochralski process. To preserve as much material as possible, and maintain crystal perfection, these ingots are sliced by ID saws, and etch-polished.

FLOW CHART

HIGH EFFICIENCY P+ N N+ CELLS

1. Grow Ingot, N-Type, 7-14 ohm-cm.
2. Prepare Wafers.
3. Apply Diffusion Mask to Front.
4. Diffuse N+ on Back to Form Back Surface Field.
5. Apply Diffusion Mask to Back.
6. Diffuse P+ to Form Junction.
7. Evaporate Back Contact (Al, Ti-Pd-Ag).
8. Apply Front Contact Mask (Photoresist).
9. Evaporate Front Contact (Ti-Pd-Ag).
10. Evaporate AR Coating.
11. Sinter.
12. Electrical Test.

2.2.2 P+ Layer

The heart of the solar cell is the charge collecting barrier which serves as the voltage-source. At present these barriers are PN junctions formed by P-type impurity diffusion into N-silicon. The junction is kept shallow to increase carrier collection from shorter wavelength sunlight, absorbed very near the front surface. This junction is confined to one face of the slice by masking the other side during diffusion. To maintain crystal perfection, the slices are annealed after diffusion.

2.2.3 N+ BSF Layer

High output can be obtained if the minority carriers generated deeper within the silicon are prevented from travelling to the back surface and recombining. This is achieved by building-in a BSF which electrically opposes the movement of minority carriers to the back surface; an incidental advantage of this process for 7-14 ohm-cm silicon is an accompanying V_{OC} increase. Here this N+ BSF is provided by diffused phosphorus.

2.2.4 Contacts

An important contribution to high output cells is an effective contact system. The front contact grid pattern must be selected to cope with the high sheet resistance from the shallow PN junction, and the lines must also be highly conducting to minimize resistive losses. The back contact must provide some reflection for longer wavelength (lightly absorbed) sunlight. Array contactability must be easy. These contacts

are applied by vacuum evaporation, with careful control of thickness, and cleanliness, to enhance adhesion and moisture resistance. The grid pattern mask is formed by photolithographic technology.

2.2.5 Coating

Bare silicon reflects ~35% of sunlight. An AR coating is required to reduce reflection as much as possible. Here a multilayer AR coating is used, where net reflectance is <5%.

2.3 Status of Cell Development

In accordance to the module output analysis in section 4.0, the minimum average of the 120 solar cells must be 16.5% at AM1 and 28°C to achieve the overall module efficiency of 14%. To date, the highest efficiency attained on a 3" cell is 15.6%. The I-V curve is shown in Figure 2. The main areas of investigation are the optimization of the junction formation and the back surface field. During the reporting period, three groups of experiments were conducted.

2.3.1 Group I

At the beginning of the P/N cell development, the resistivity for the available N-type silicon was 20 ohm-cm. Twelve (12) experiments varying the N+ diffusion and the P+ diffusion were performed. The data are presented in Table I. To expedite accumulation of data, most of the experiments were performed on 2x2 cm cells. To achieve an efficiency of 16.5%, the short circuit current density, the open circuit voltage and the fill factor must be 37 mA/cm^2, 600 mV, and 75%, respectively.

TABLE I

TEST NO.	SAMPLE SIZE	CELL SIZE	N+ DIFFUSION			P+ DIFFUSION			TEST RESULTS AT AM1, 28°C			
	(Tested)	(cm^2)	Temp. (°C)	Diffusion Time (Min.)	Drive-In Time (Min.)	Temp. (°C)	Diffusion Time (Min.)	Drive-In Time (Min.)	Average V_{OC} (mV)	Average J_{SC} (mA/cm^2)	Average Efficiency (%)	Best Efficiency (%)
1	12	4	875	30	60 Slow Pull	900	45	30 Slow Pull	550	35.6	13.2	14.5
2	14	4	875	30	60 Slow Pull	900	45	0	592	35.6	15.5	16
3A	6	4	875	30	60 Slow Pull	900	45	0	596	36.6	16.5	16.6
3B	8	45.6	875	30	60 Slow Pull	900	45	0	590	34	15.2	15.6
4	6	45.6	875	30	60 Slow Pull	900	30	0	540	31.1	11.9	12.4
5A	14	4	875	5	2 Slow Pull	900	40	Shut Off Furnace To Below 725°C	582	36.2	14.8	15.1
5B	10	4	875	30	2 Slow Pull	900	40	Shut Off Furnace To Below 725°C	586	36.1	15.1	15.5
5C	9	4	875	30	60 Slow Pull	900	40	Shut Off Furnace To Below 725°C	583	36.1	14.9	15.5
5D	15	4	875	30	120 Slow Pull	900	40	Shut Off Furnace To Below 725°C	580	36	14.2	15.2
5E	16	4	1000	5	Shut Off Furnace To Below 500°C	900	40	Shut Off Furnace To Below 725°C	587	36	14.9	15.6
5F	12	4	1000	30	Shut Off Furnace To Below 500°C	900	40	Shut Off Furnace To Below 725°C	---	----	----	----
5G	12	4	875	30	60 Slow Pull	900	30	Shut Off Furnace To Below 725°C	580	36.2	14.3	15.2

These values were achieved on Test No. 3A. However, when the test was repeated on 3" wafers, both the I_{SC} and the V_{OC} were lower than expected, indicating either the inadequacy of the BSF formation or the degradation of the diffusion length due to the high temperature process of applying the N+ layer. In addition, the P+ diffusion also required examination for current density improvement.

Cells in the Test No. 5F showed very low V_{OC} ($\sim$200 mV). It was suspected that the cells were damaged due to high temperature (1000°C).

2.3.2 Group II

When the baseline silicon wafers of 7-14 ohm-cm became available, a group of eight (8) experiments was designed and performed simultaneously. Half of the experiments assessed junction formation, the other half assessed back surface field. The experimental parameters and the test results are shown in Table II, which shows that none of the tests is adequate to provide the 16.5% cell.

2.3.3 Group III

This group of nine (9) experiments was designed to assess the merit of forming P+ junction prior to the application of the back surface field. If this approach is successful, it has the advantage of deleting the identification flats on the wafers, thus increasing the active area of the cell. The matrix of experiments and the test results are tabulated in Table III, which clearly demonstrates that the performance of the cells are still below the requirements.

TABLE II

TEST NO.	SAMPLE SIZE	CELL SIZE	N+ DIFFUSION			P+ DIFFUSION			TEST RESULTS AT AM1, 28°C			
	(Tested)	(cm^2)	Temp. (°C)	Diffusion Time (Min.)	Drive-In Time (Min.)	Temp. (°C)	Diffusion Time (Min.)	Drive-In Time (Min.)	Average V_{OC} (mV)	Average J_{SC} (mA/cm^2)	Average Efficiency (%)	Best Efficiency (%)
1A	12	4	0	0	0	900	10	Shut Off Furnace To Below 725°C	520	34.9	12	12.5
1B	12	4	0	0	0	900	20	↓	525	34.6	12.4	12.9
1C	12	4	0	0	0	900	30	↓	520	34.6	12.1	12.5
1D	12	4	0	0	0	900	40	↓	520	31.1	12.4	12.8
2A	17	4	875	5	2	900	40	↓	582	37.2	15.9	16.5
2B	23	4	875	30	2	900	40	↓	588	36.6	16.1	16.5
2C	18	4	875	30	60	900	40	↓	588	36.6	15.7	16.1
2D	12	4	875	30	120	900	40	↓	587	36.5	15.4	15.9

TABLE III

TEST NO.	SAMPLE SIZE	CELL SIZE	P+ DIFFUSION			N+ DIFFUSION			TEST RESULTS AT AM1, 28°C			
	(Tested)	(cm^2)	Temp. (°C)	Diffusion Time (Min.)	Drive-In Time (Min.)	Temp. (°C)	Diffusion Time (Min.)	Drive-In Time (Min.)	Average V_{OC} (mV)	Average J_{SC} (mA/cm^2)	Average Efficiency (%)	Best Efficiency (%)
3A	10	4	900	10	Shut Off Furnace To Below 800°C	875	5	Shut Off Furnace To Below 725°C	561	36.6	15	15.2
3B	12	4	900	10	↓	875	30	↓	560	36.3	14.8	15.2
3C	12	4	900	10		875	90		555	36.1	14.2	14.5
3D	12	4	900	20		875	90		575	36.3	15.2	15.3
3E	12	4	900	20		875	30		574	36.4	15.2	15.4
3F	12	4	900	20		875	90		574	35.9	14.9	15.2
3G	12	4	900	30		875	5		563	36.4	14.9	15.3
3H	12	4	900	30		875	30		557	35.9	14.7	14.9
3I	8	4	900	30	↓	875	30	↓	570	36.6	15.4	15.6

2.4 Module Design

The detailed module design is shown in Figure 3 (OCLI Drawing No. D-202400) The module consists of a piece of 3/16" thick Sunadex glass as the superstrate, a 120-cell assembly, polyvinyl butyral encapsulation, Mylar film for moisture barrier, "Proglaze" silicone sealant for edge sealing, extruded aluminum channel for framing, and two flexible leads secured by Heyco strain relief as electrical terminals. Each module has 120 cells connected four (4) cells in parallel and thirty (30) cells in series. Each key component will be discussed in the following paragraphs.

2.4.1 Superstrate

OCLI has chosen 3/16" thick annealed, edge-ground Sunadex glass as the superstrate mainly due to the results published in JPL Report 5101-62 entitled, "Photovoltaic Solar Panel Resistance to Simulated Hail". Annealed glass upon impact would only crack but the module would still function with very small electrical degradation. Tempered glass would shatter upon impact resulting in loss of power output. Even though the mechanical strength of the annealed glass is less than that of tempered glass it is more than sufficient to satisfy the hail test requirement.

Because grinding the edges of the glass improves the performance of the steel ball drop test, OCLI decided to use edge-ground glass superstrate.

2.4.2 Module Frame

The module frame is made of 6063-T5 extruded aluminum channel which will be cut to length. The frame is made up by spot welding four (4) triangular plates to the aluminum channels as shown in Figure 4 (OCLI Drawing No. D-202399).

2.4.3 Cell Assembly

The cell assembly, as shown in Figure 5 (OCLI Drawing No. D-202393), consists of 120 3" cells connected four (4) cells in parallel and thirty (30) cells in series. The interconnectors are made of the high conductivity expanded copper plated with 1 mil thick of 60/40 solder. The mesh provides the stress relief necessary for operating the module over wide temperature variations.

2.4.4 Encapsulation

The cell assembly will be encapsulated in a conventional autoclave machine. The system consists of a piece of Sunadex superstrate, a sheet of .015" thick PVB, the cell assembly, a sheet of .020" thick PVB, and a sheet of .020" thick Mylar. The second sheet of PVB may be white in color or the Mylar may be white to provide the white reflecting surface to achieve the electrical gain, a phenomenon discovered by the General Electric Company under JPL/DOE contract.

2.4.5 Edge Sealing

A commercial silicone sealant named "Proglaze" which has been in use in the construction industry for many years has been selected as the edge sealant. It remains elastic at low temperatures, eliminating the possibility of cracking the glass superstrate.

2.4.6 Electrical Terminals

For cost effectiveness, the relatively expensive socket will be replaced with two (2) Teflon insulated No. 16 AWG stranded wires secured by two Heyco strain relief clamps as shown in Figure 6 (OCLI Drawing No. C-202392) as electrical terminals.

2.4.7 Interface Control

The maximum module dimensions and the locations of the mounting holes are shown in Figure 7 (OCLI Drawing No. D-202398).

2.5 Module Output Analysis

The objective of this program is to fabricate a 22.25" x 48" solar module with a minimum power output of 90 watts at AM1 and 28°C and with a design goal of 14% overall module efficiency. The module will have 120 3" diameter high efficiency solar cells. The gain due to the Sunadex and the back reflecting surface is estimated to be 7%.

TOTAL MODULE AREA = 22.25 in. x 2.54 cm/in. x 48 in. x 2.54 cm/in.

= 6890 cm^2

2.5.1 Ninety (90) Watt Module

$$\text{CELL OUTPUT} = \frac{90\ W}{120 \times 1.07} = 0.701\ \text{Watt}$$

$$\text{CELL EFFICIENCY} = \frac{0.701\ W}{45.6\ cm^2 \times 0.1\ W/cm^2} = 15.4\%$$

$$\text{MODULE EFFICIENCY} = \frac{90\ W}{6890\ cm^2 \times 0.1\ W/cm^2} = 13.1\%$$

2.5.2 Fourteen Percent (14%) Efficiency Module

MODULE OUTPUT = 6890 cm^2 x 0.1 W/cm^2 x 14% = 96.4 Watts

$$\text{CELL OUTPUT} = \frac{96.4\ W}{120 \times 1.07} = 0.751\ \text{Watt}$$

$$\text{CELL EFFICIENCY} = \frac{0.751\ W}{45.6\ cm^2 \times 0.1\ W/cm^2} = 16.5\%$$

2.5.3 Packing Factor

$$\text{PACKING FACTOR} = \frac{120 \times 45.6\ cm^2}{6890} = 79.4\%$$

2.6 Production Tooling

The following tooling has been designed.

2.6.1 AR Coating Tooling

The center contact of the cell must be shielded during AR coating evaporation to provide solderability. Small, high power magnets were found to work satisfactorily. The tooling consists of five (5) pie-shaped sections which fit inside the AR coating evaporator. Pins will be provided for cell locations. A plastic template with holes aligned with the center of the cells will fit over the section for loading the magnets. The template will be removed upon completion of loading.

2.6.2 Test Fixture

The test fixture is designed so that a narrow probe will reach the center contact of the cell. It includes the usual features such as temperature control, thermocouple for temperature monitoring, four point connections, etc.

2.6.3 Vacuum Pick-Up

The vacuum pick-up is designed to remove the cell assembly from the soldering fixture and transfer it to a cleaning rack. It consists of two sheets of aluminum honeycomb, separated by spacers and sealed around edges to form a vacuum chamber. Soft rubber cups are inserted into one side of the honeycomb while a vacuum valve is attached to the opposite side. The in-house vacuum line will be used to operate the pick-up.

3.0 MILESTONE

3.1 The program is slightly behind schedule due to the difficulty encountered in cell development. The impact on the schedule is being assessed. The following work has been accomplished.

3.1.1 The design of the low cost, solar module has been completed. Detailed drawings have been prepared.

3.1.2 Development of high efficiency P/N cell is proceeding. The best efficiency achieved on 3" cell is 15.6%, below the requirement of 16.5% at AM1 and 28°C.

3.1.3 Detailed tooling design has been completed. At the request of OCLI the tooling design review was postponed.

3.2 Planned for the next reporting period.

3.2.1 Continue cell development.

3.2.2 Conduct tooling design review meeting.

3.3 A milestone chart is attached.

APPLICATION		REVISIONS				
NEXT ASSY	USED ON	LTR	DCN	DESCRIPTION	DATE	APPROVED
		N/C	4574	NEW	11/27/78	

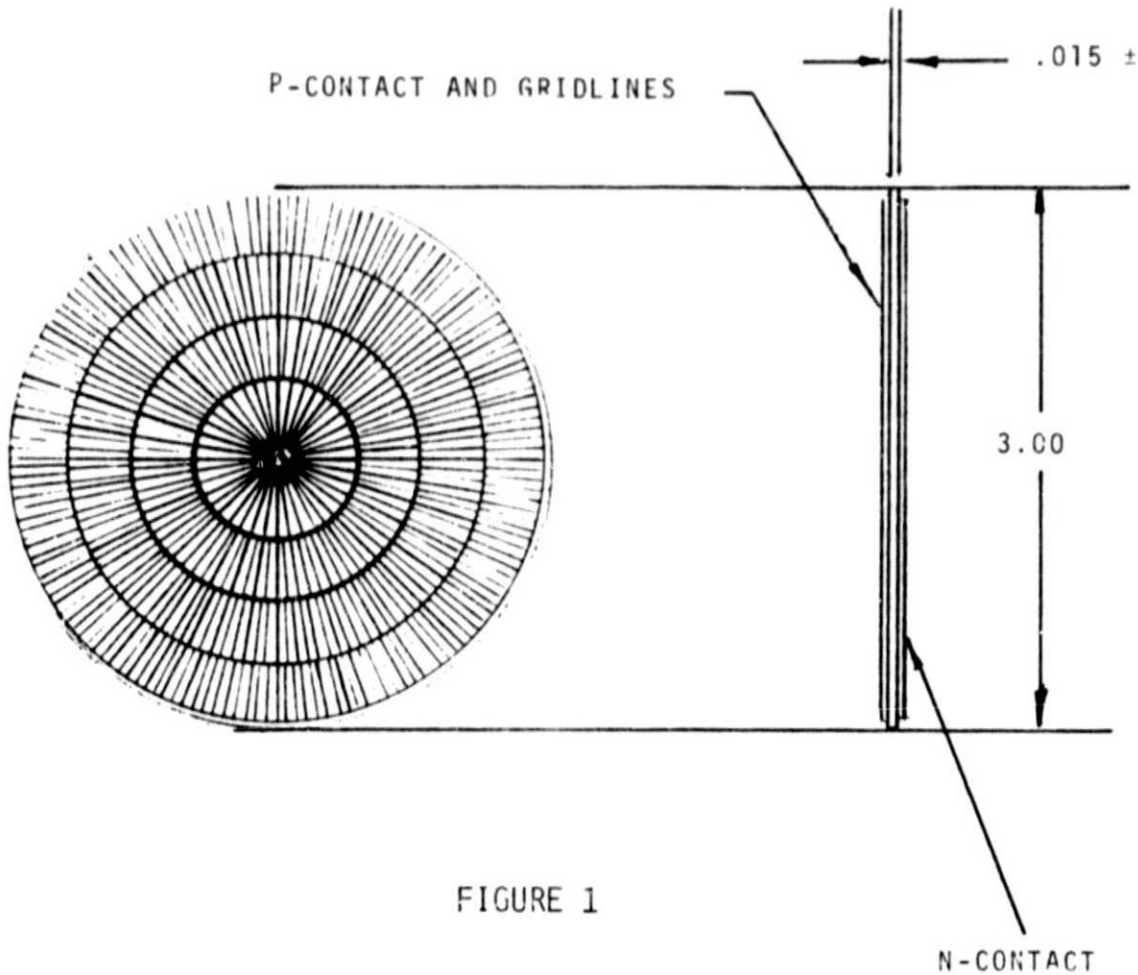


FIGURE 1

1.0 P-CONTACT OF .25 DIAMETER IS AT CENTER OF CELL

2.0 BOTH CONTACT-METALS ARE VACUUM DEPOSITED TITANIUM-PALLADIUM-SILVER

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .X ±
.XX ± .010
.XXX ±
FRACTIONS ±
ANGLES ±
DO NOT SCALE DRAWING

DRAWN	S.Khemthong	11/27/78
CHECK		
ENGR	S.Khemthong	11/27/78
PROD		
QA		

OCLI
OPTICAL COATING LABORATORY, INC.
PHOTOELECTRONICS GROUP
15251 Don Julian Rd. • City of Industry, Calif. 91746

HIGH EFFICIENCY 3" TERRESTRIAL CELL

MATERIAL
SILICON SOLAR TERRESTRIAL CELL

SIZE	CODE IDENT NO.	DWG NO.
A		A-202337

SCALE	REV	SHEET
NONE	N/C	1 OF 1

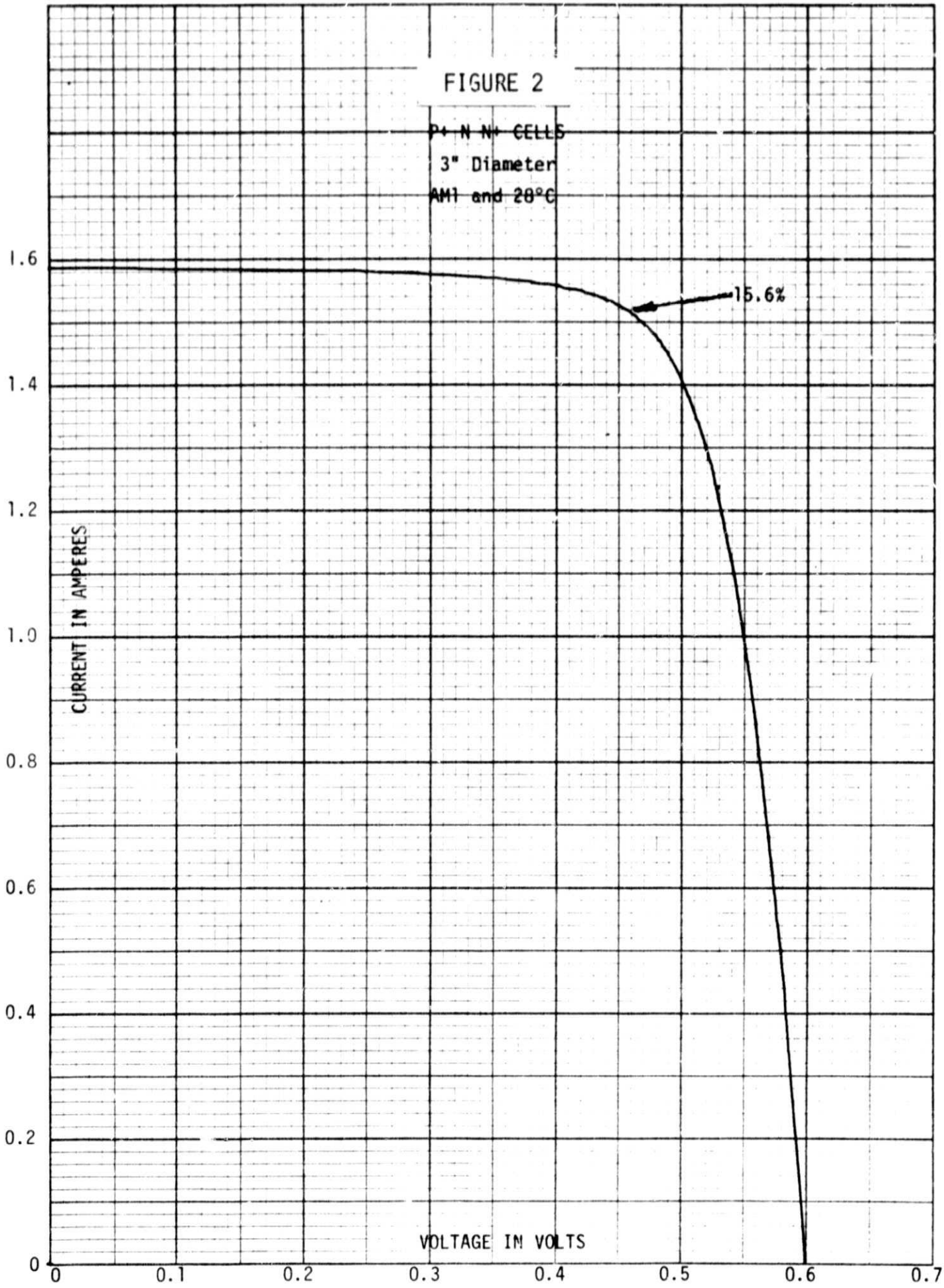


FIGURE 2
P+ N N+ CELLS
3" Diameter
AM1 and 28°C
15.6%
CURRENT IN AMPERES
VOLTAGE IN VOLTS
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7

FIGURE 3

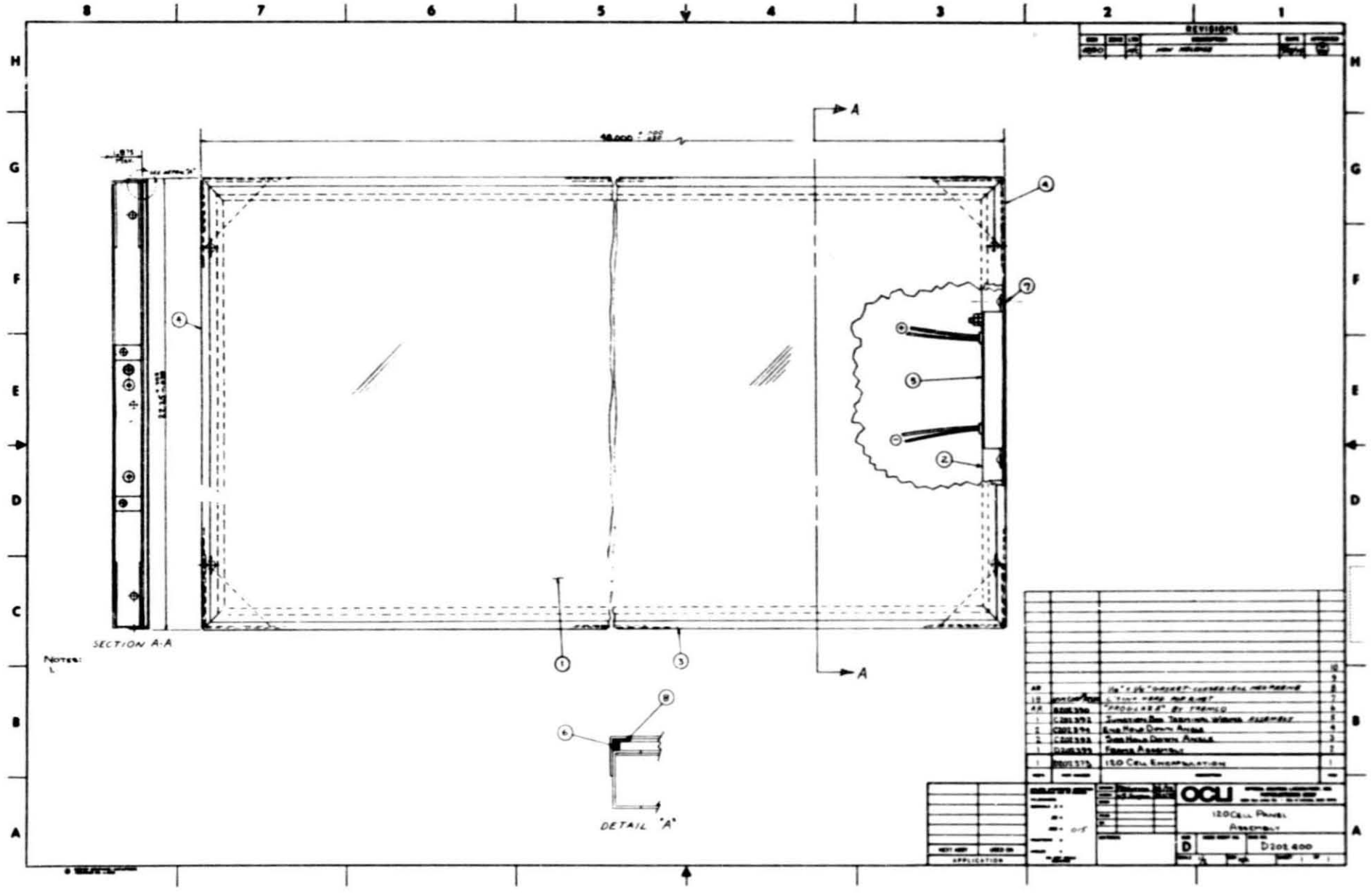


FIGURE 4

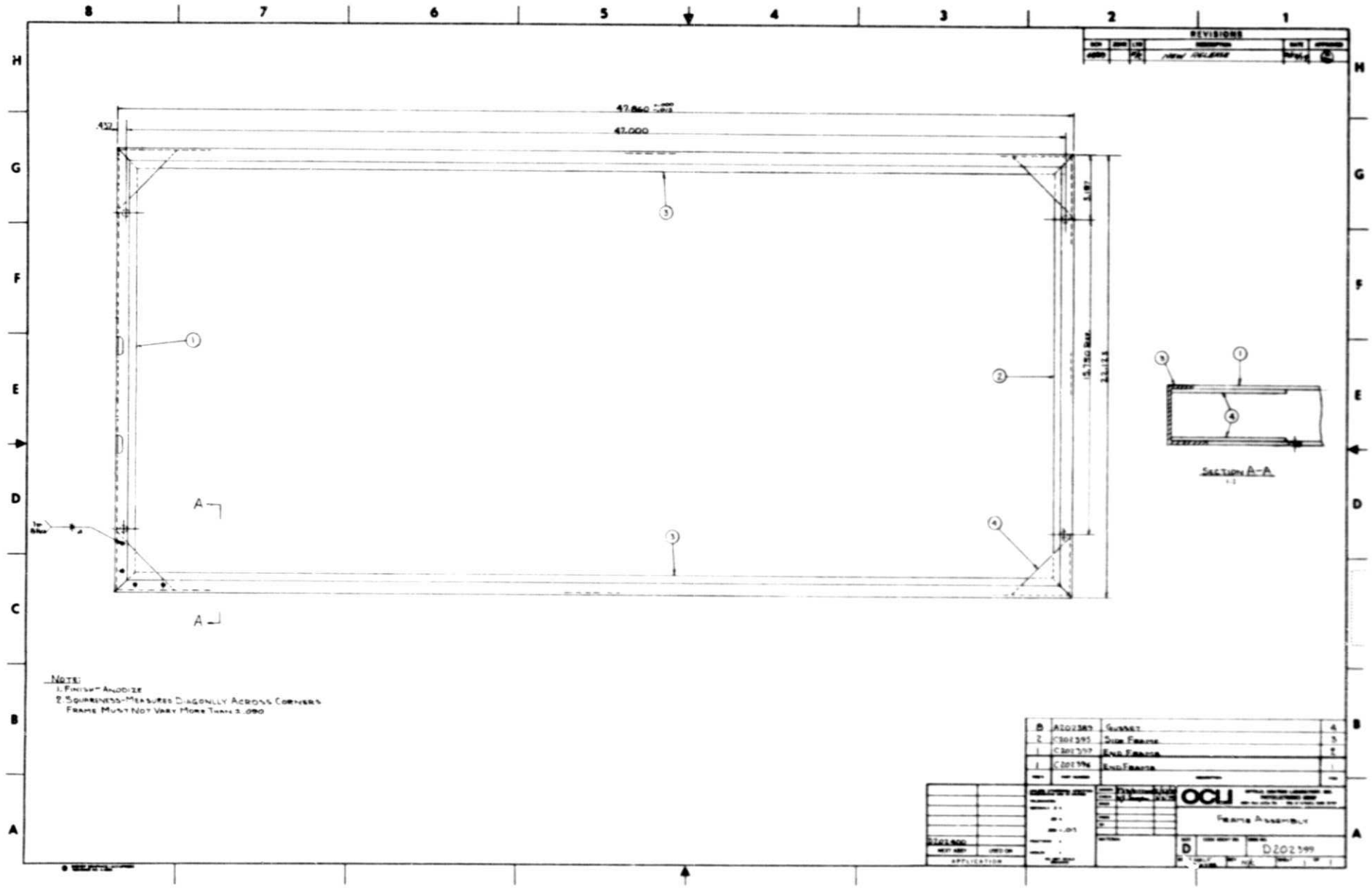

REVISIONS
42.000
.432
A
A
SECTION A-A
NOTE:
1. FINISH= ANODIZE
2. SQUARENESS-MEASURED DIAGONLLY ACROSS CORNERS FRAME MUST NOT VARY MORE THAN .090
OCLI
FRAME ASSEMBLY
D
D202399

FIGURE 5

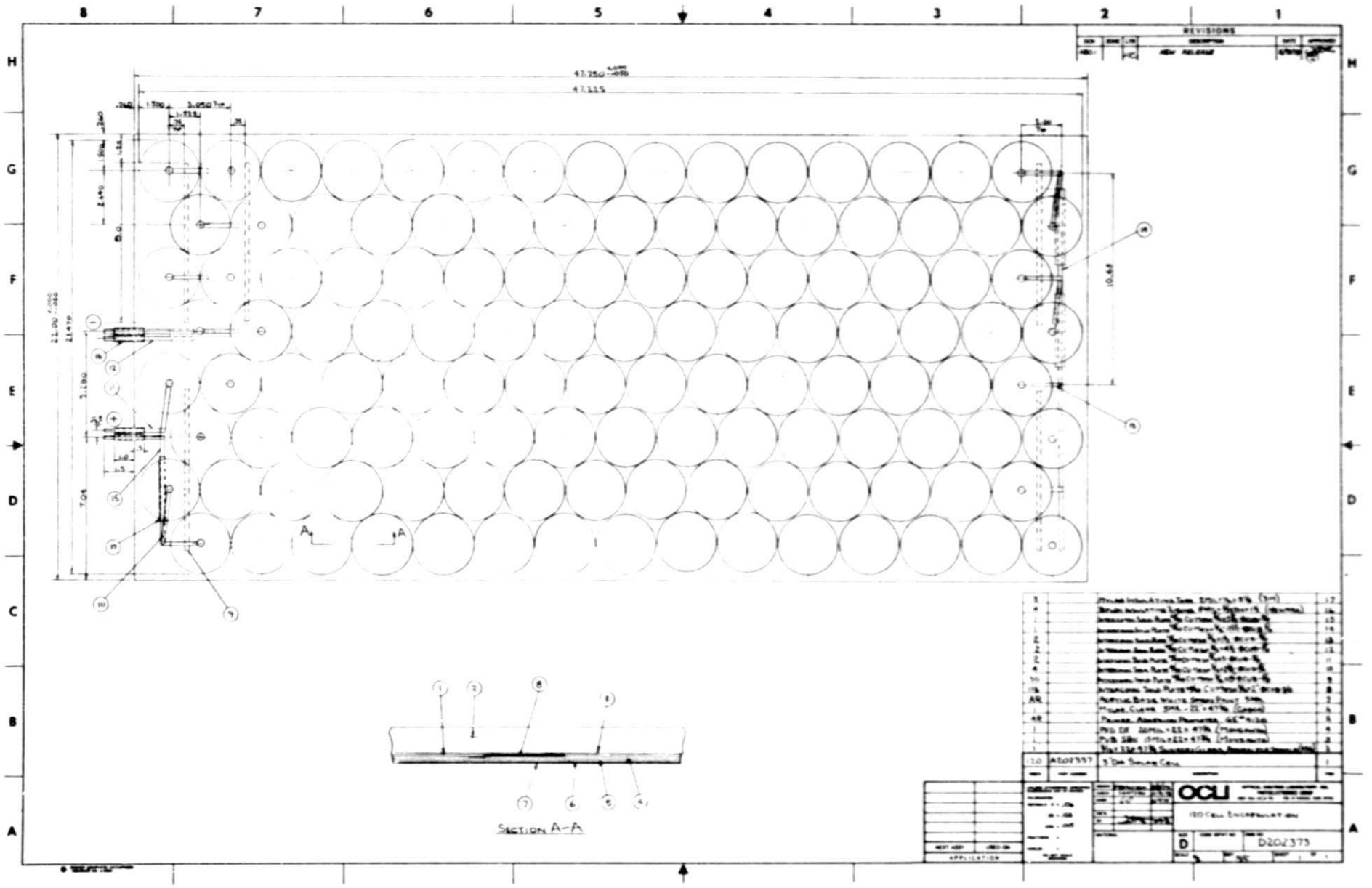
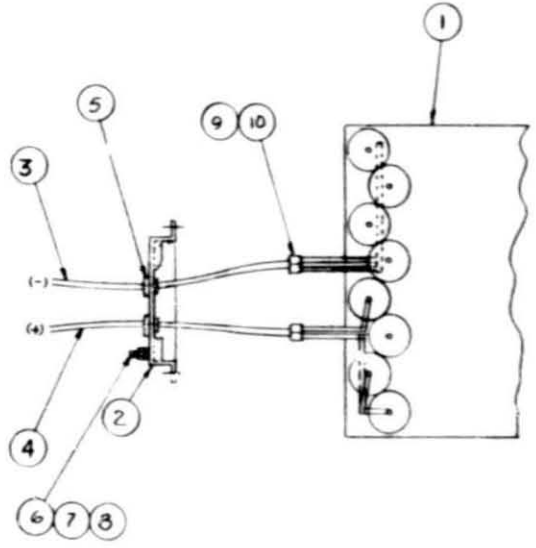


FIGURE 6



REVISIONS					
DCN	ZONE	LTR	DESCRIPTION	DATE	APPROVED
488		N/C	NEW RELEASE	3/9/79	

AR		SOLDER JOINT ALLOY 60/40	10
4		TEFLON HEAT SHRINK INSUL. 3/16" I.D.	9
2		#8-32 HEX NUT (SST)	8
1		#8-32 x 1/2 R.H. MACH. SCR. (SST)	7
2		#8 STAR LOCK WASHER	6
2		STRAIN RELIEF - HEYCO SP-1	5
2		16 AWG TEFLON INSUL. HOOK-UP WIRE / 48" (WHITE)	4
2		16 AWG TEFLON INSUL. HOOK-UP WIRE / 48" (BLACK)	3
1	C202391	JUNCTION BOX	2
1	D202373	LAMINATED CELL ASSEMBLY	1
REQ'D	PART NUMBER	DESCRIPTION	ITEM

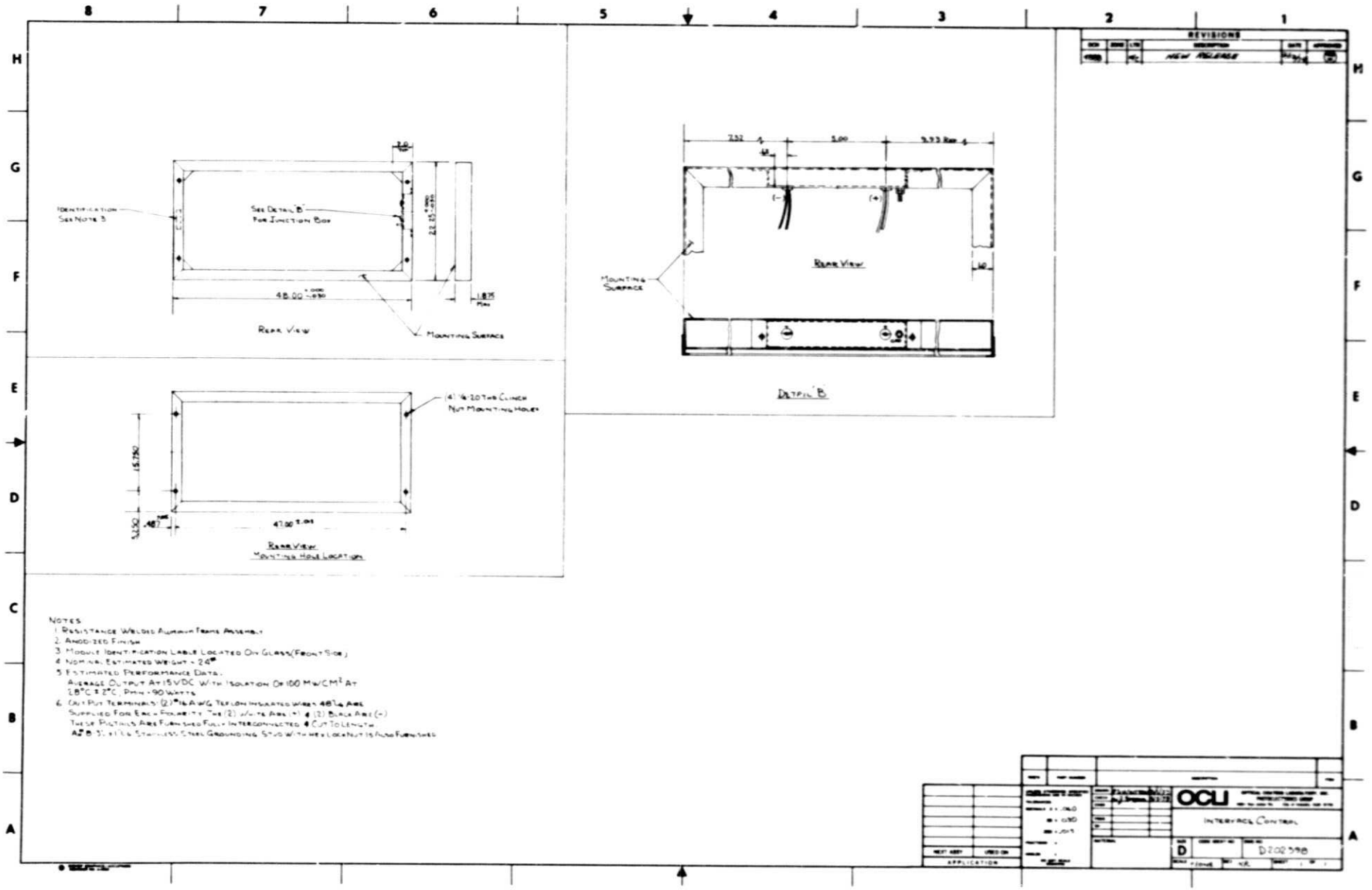
D202490
NEXT ASSY | USED ON
APPLICATION

OCLI — OPTICAL COATING LABORATORY, INC. PHOTOELECTRONICS GROUP

JUNCTION BOX
TERMINAL WIRING

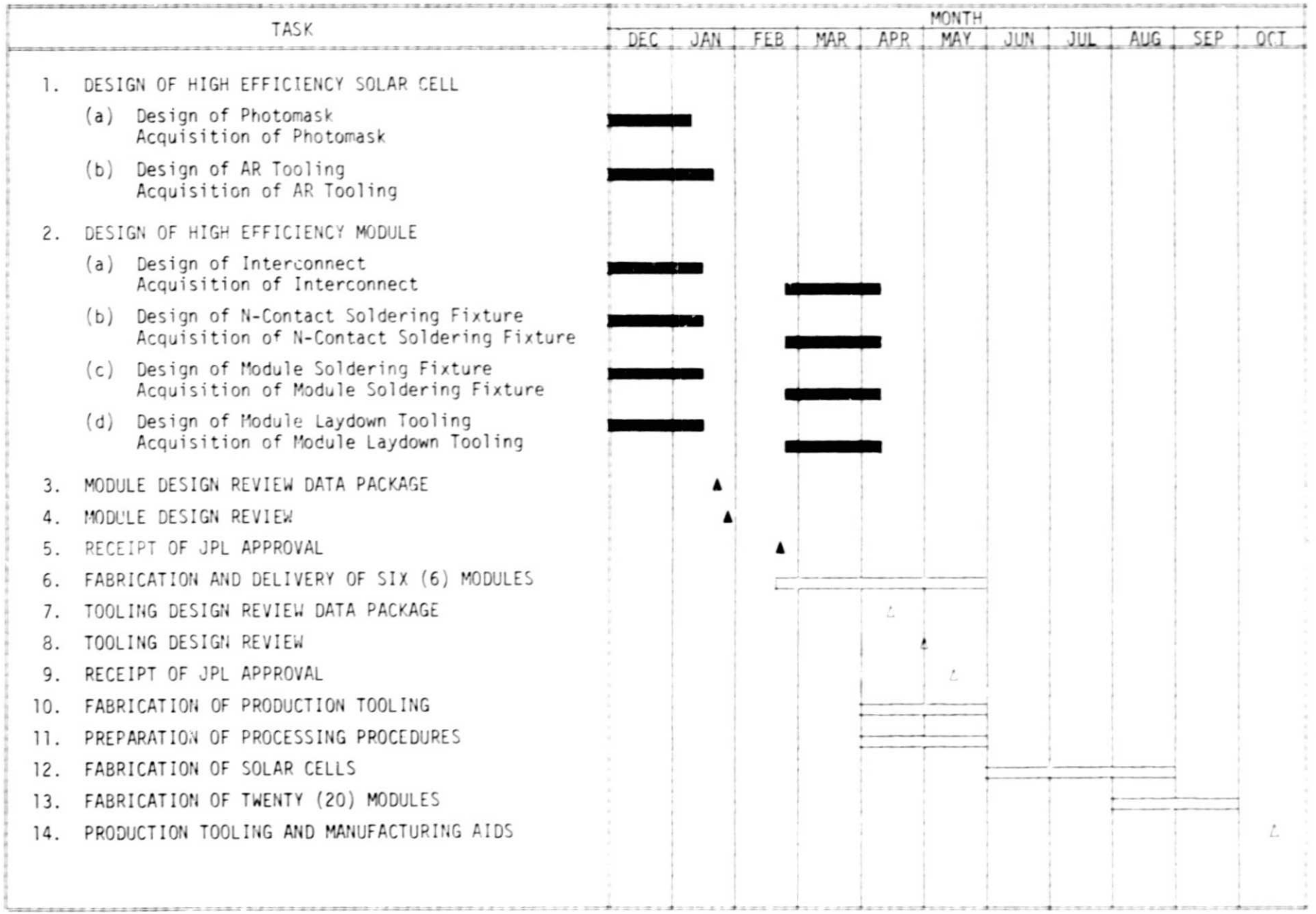
SIZE C | CODE IDENT NO | DWG NO C202392
SCALE NONE | REV N/C | SHEET 1 OF 1

FIGURE 7


REVISIONS
IDENTIFICATION SEE NOTE 3
SEE DETAIL 'B' FOR JUNCTION BOX
48.00
1.875 Max
REAR VIEW
MOUNTING SURFACE
DETAIL 'B'
REAR VIEW
MOUNTING SURFACE
(4) 1/4-20 THD CLINCH NUT MOUNTING HOLES
47.00
REAR VIEW
MOUNTING HOLE LOCATION
NOTES
1. RESISTANCE WELDED ALUMINUM FRAME ASSEMBLY
2. ANODIZED FINISH
3. MODULE IDENTIFICATION LABLE LOCATED ON GLASS(FRONT SIDE)
4. NOMINAL ESTIMATED WEIGHT = 24#
5. ESTIMATED PERFORMANCE DATA.
AVERAGE OUTPUT AT 15VDC WITH ISOLATION OF 100 MW/CM² AT 28°C ± 2°C. PMIN = 90 WATTS
6. OUTPUT TERMINALS: (2) #16 AWG TEFLON INSULATED WIRES 48" LG ARE SUPPLIED FOR EACH POLARITY. THE (2) WHITE ARE (+) & (2) BLACK ARE (-)
THESE PIGTAILS ARE FURNISHED FULLY INTERCONNECTED & CUT TO LENGTH.
AZ 8 3/4-11 LG STAINLESS STEEL GROUNDING STUD WITH HEX LOCK NUT IS ALSO FURNISHED
OCLI
INTERFACE CONTROL
D
D208598

9/18/78
Revised: 12/22/78

PROGRAM PLAN



KSL/js

9/18/78
Revised: 12/22/78

PROGRAM PLAN

TASK	MONTH										
	DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT
15. COST DATA FOR 5, 25, 50 KW										△	
16. COST DATA PER SAMICS											△
17. BASELINE COST ESTIMATE	▲										
18. PROGRAM PLAN	▲										
19. MONTHLY FINANCIAL REPORT	▲		▲	▲	△	△	△	△	△	△	△
20. MONTHLY STATUS REPORT	▲		▲		△	△		△	△		
21. QUARTERLY REPORT				▲			△			△	
22. INTERIM TECHNICAL REPORT	2 WEEKS AFTER RECEIPT OF R&D TESTING DATA FROM JPL										
23. FINAL TECHNICAL REPORT											
(a) Draft	2 WEEKS AFTER RECEIPT OF TESTING DATA FROM JPL										
(b) Final	30 DAYS AFTER RECEIPT OF JPL WRITTEN COMMENTS OF THE DRAFT FINAL REPORT										
24. PARTICIPATION IN TECHNICAL REVIEW ACTIVITIES											
(a) Program Review Meetings	AS REQUIRED										
(b) Program Design Review Meetings	AS REQUIRED										
(c) Project Integration Meetings	AS REQUIRED				▲						
(d) Workshops	AS REQUIRED										

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