Report No. 78-113
Contract No. NAS8-33244

STANDALONE ENGINE SIMULATOR (SAES)
ENGINE DYNAMICS SIMULATOR (EDS)
XEROX SIGMA 5
INTERFACE HARDWARE MANUAL

July 17, 1979

Prepared for:

George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Marshall Space Flight Center, Alabama 35812

M&S COMPUTING, INC.

PREFACE

Presented in this document are hardware descriptions of the Engine Dynamics Simulator (EDS) - Engine Sensor Simulator (ESS) and EDS - Xerox Sigma 560 (Sigma) interfaces. Development of these interfaces was performed by M&S Computing, Inc., under Contract No. NAS8-33244 for the Engineering Management Office of the Shuttle Projects Office of George C. Marshall Space Flight Center (MSFC). The NASA COR for this contract is Mr. B. J. Funderburk, SA23.

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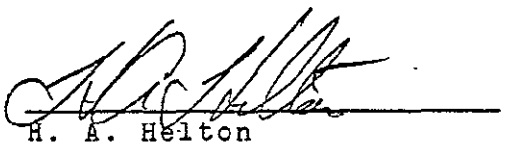

H. A. Helton

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LIST OF FIGURES

LIST OF ACRONYMS

DEC	Digital Equipment Corporation
EDS	Engine Dynamics Simulator
ESS	Engine Sensor Simulator
HEF	High External Function
HEFA	High External Function Acknowledge
HOA	High Output Acknowledged
HODR	High Output Data Ready
MSFC	Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
SAES	Standalone Engine Simulator
UDIF	Unibus DMA Interface

1. SCOPE OF DOCUMENT

This document is intended as a description of the ESS-EDS and EDS-Sigma interfaces within the Standalone Engine Simulator (SAES).

The operation of these interfaces, including the definition and use of special function signals and data flow paths within them during data transfers, is presented along with detailed schematics and circuit layouts of the described equipment.

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2. APPLICABLE DOCUMENTS

The following is a list of documents which describe hardware connected to these interfaces and software used to communicate through them.

- Standalone Engine Simulator, Engine Sensor Simulator Hardware Manual, Report No. 78-112, dated April 16, 1979.
- Model 7902 Extended Device Subcontroller Technical Specifications, XDS 98 03 93A.
- Standalone Engine Simulator Engine Dynamic Simulator Simulation Program Detailed Design Specification/Software User Manual, Report No. 78-118, dated April 16, 1979.
- Unibus DMA Interface Manual, Report No. 79-014, dated April 25, 1979.

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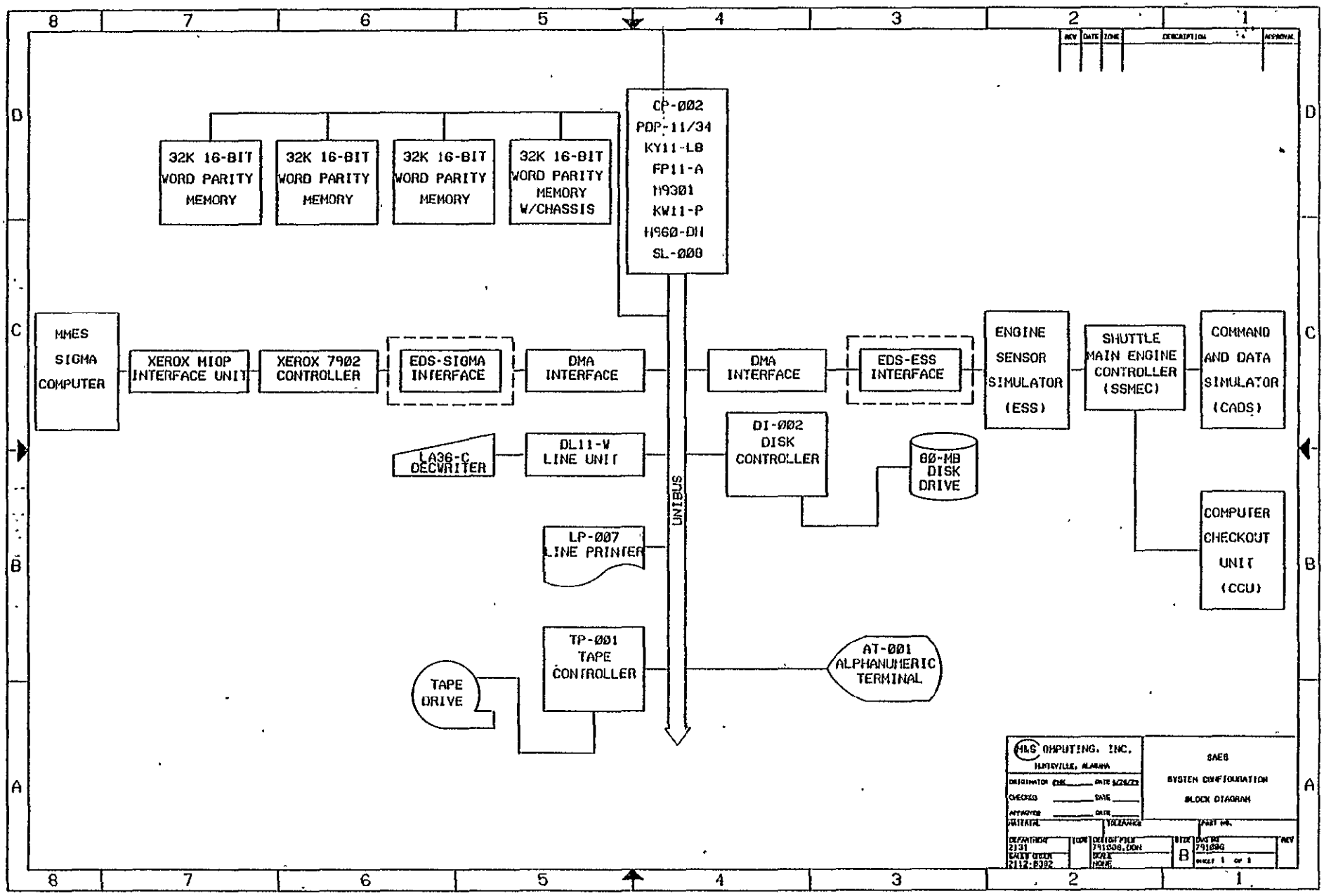
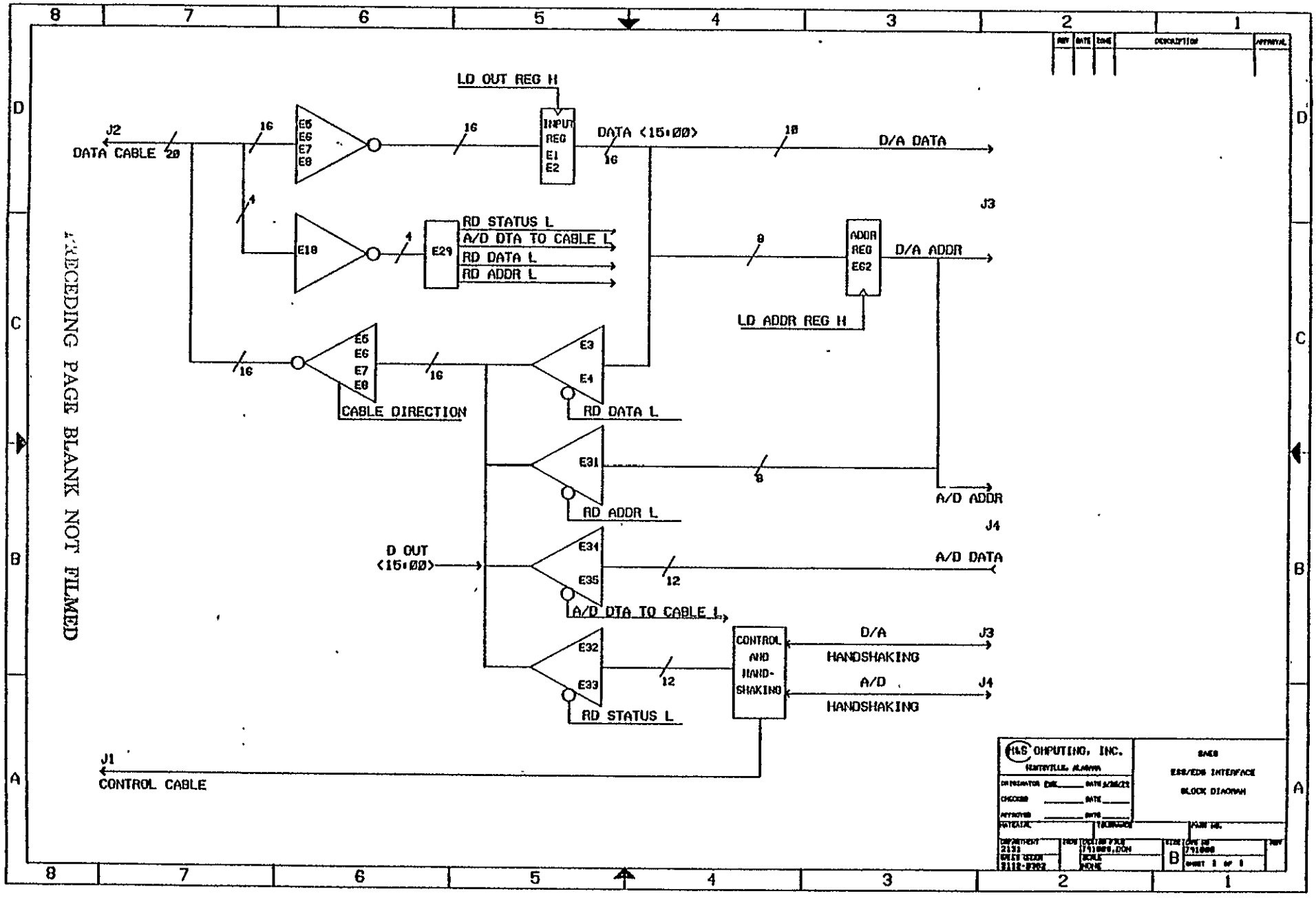


FIG. 3.1-1



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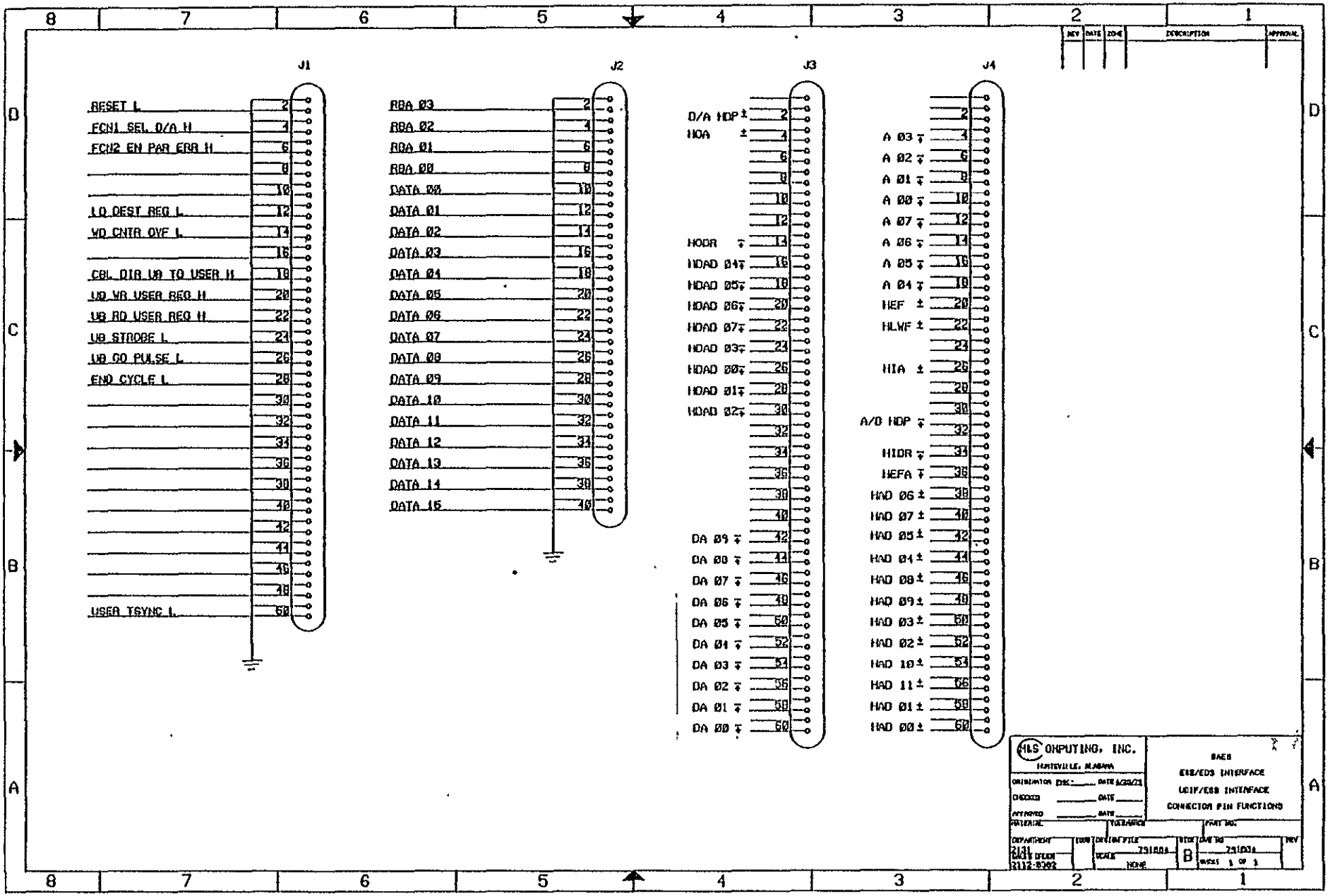
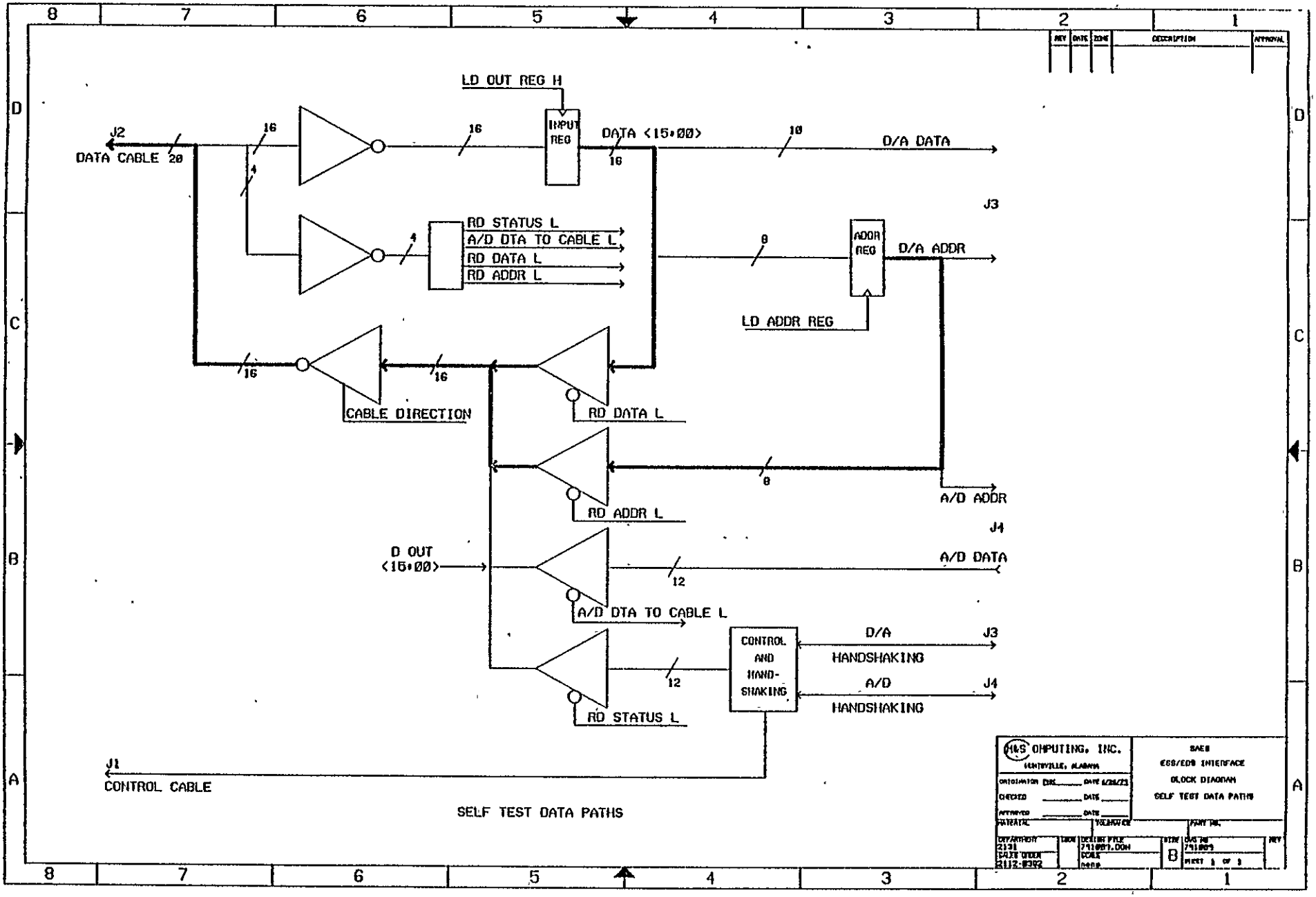

J1
RESET L
FCN1 SEL D/A H
FCN2 EN PAR ERR H
LQ DEST REQ L
WD CNTR OVF L
CBL DIR UB TO USER H
UB WR USER REQ H
UB RD USER REQ H
UB STROBE L
UB GO PULSE L
END CYCLE L
USER TSYNC L
J2
RBA Ø3
RBA Ø2
RBA Ø1
RBA Ø0
DATA Ø0
DATA Ø1
DATA Ø2
DATA Ø3
DATA Ø4
DATA Ø5
DATA Ø6
DATA Ø7
DATA Ø8
DATA Ø9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
J3
D/A HDP ±
HOA ±
HODR ∓
HDAD Ø4∓
HDAD Ø5∓
HDAD Ø6∓
HDAD Ø7∓
HDAD Ø3∓
HDAD Ø0∓
HDAD Ø1∓
HDAD Ø2∓
DA Ø9 ∓
DA Ø8 ∓
DA Ø7 ∓
DA Ø6 ∓
DA Ø5 ∓
DA Ø4 ∓
DA Ø3 ∓
DA Ø2 ∓
DA Ø1 ∓
DA Ø0 ∓
J4
A Ø3 ∓
A Ø2 ∓
A Ø1 ∓
A Ø0 ∓
A Ø7 ∓
A Ø6 ∓
A Ø5 ∓
A Ø4 ∓
HEF ±
HLWF ±
HIA ±
A/D HDP ∓
HIDR ∓
HEFA ∓
HAD Ø6 ±
HAD Ø7 ±
HAD Ø5 ±
HAD Ø4 ±
HAD Ø8 ±
HAD Ø9 ±
HAD Ø3 ±
HAD Ø2 ±
HAD 10 ±
HAD 11 ±
HAD Ø1 ±
HAD Ø0 ±
HLS COMPUTING, INC.
BAEB
E8B/EDS INTERFACE
UBIF/E8B INTERFACE
CONNECTOR PIN FUNCTIONS
751034
751034
NONE
B

FIG.3.1-3



SELF TEST DATA PATHS

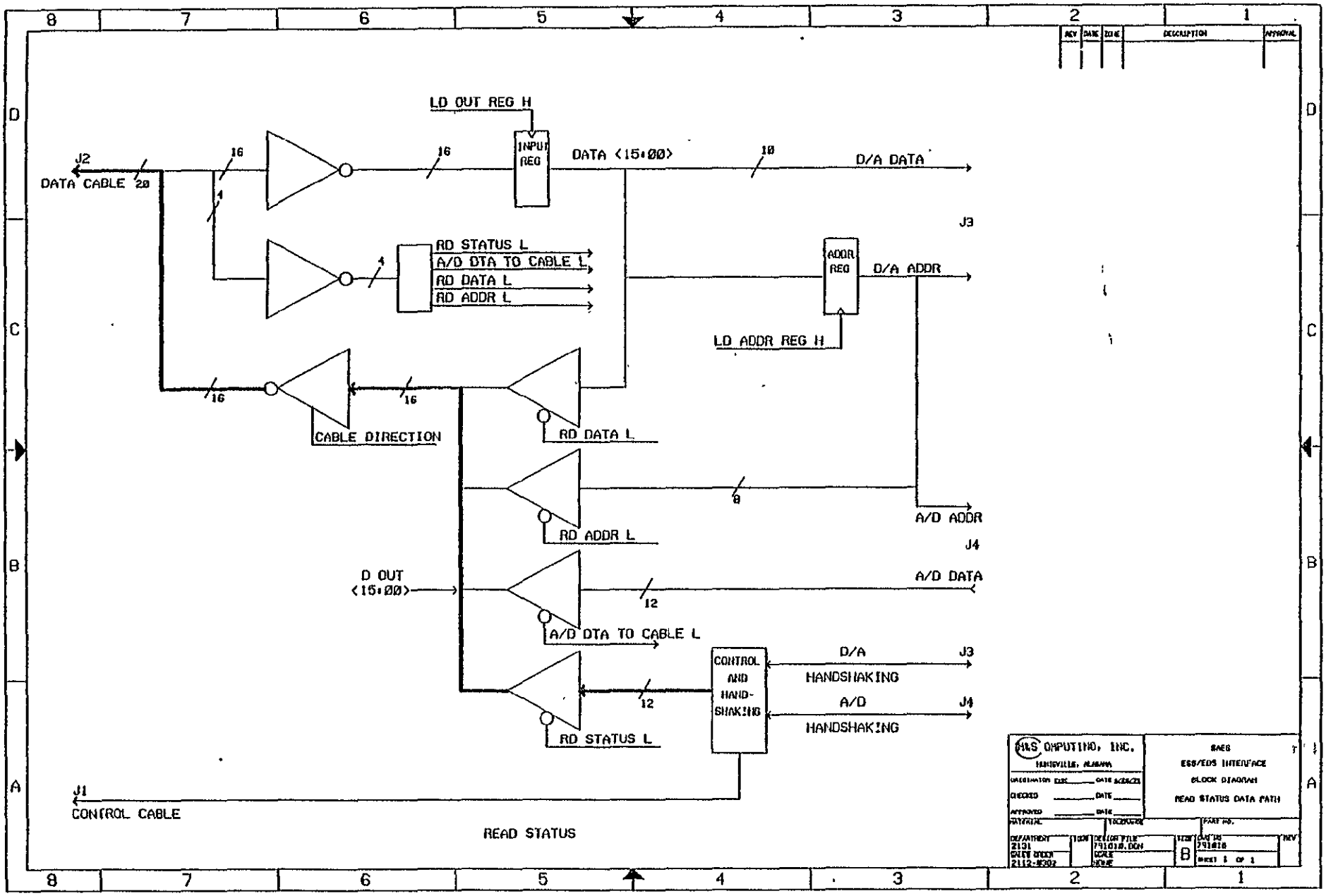

LD OUT REG H
J2
DATA CABLE
20
16
16
INPUT REG
DATA <15:00>
16
D/A DATA
J3
RD STATUS L
A/D DTA TO CABLE L
RD DATA L
RD ADDR L
ADDR REG
D/A ADDR
LD ADDR REG H
16
16
CABLE DIRECTION
RD DATA L
8
RD ADDR L
A/D ADDR
J4
D OUT
<15:00>
12
A/D DATA
A/D DTA TO CABLE L
CONTROL AND HAND-SHAKING
D/A
J3
HANDSHAKING
12
A/D
J4
HANDSHAKING
RD STATUS L
J1
CONTROL CABLE
READ STATUS
REV
DATE
ZONE
DESCRIPTION
APPROVAL
HAS COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAEB
ESS/EDS INTERFACE
BLOCK DIAGRAM
READ STATUS DATA PATH
DEPARTMENT
2131
SALES ORDER
2112-9202
DESIGN FILE
791018.DGN
SCALE
NONE
SIZE
B
DWG NO
791018
SHEET 1 OF 1
REV

FIG.3.2.3-1

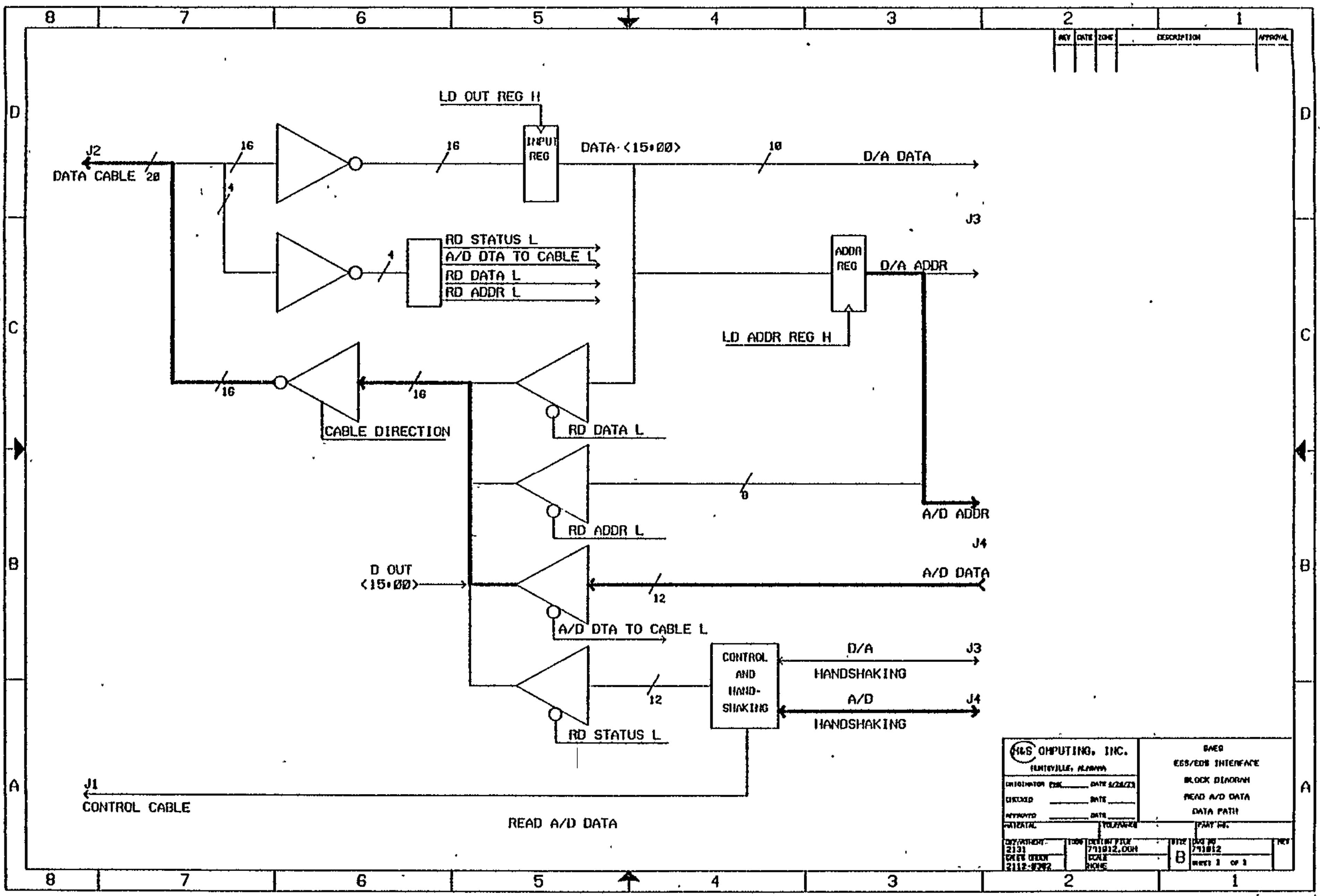

LD OUT REG H
J2
DATA CABLE
20
16
16
INPUT REG
DATA <15:00>
10
D/A DATA
4
RD STATUS L
A/D DTA TO CABLE L
RD DATA L
RD ADDR L
J3
ADDR REG
D/A ADDR
LD ADDR REG H
16
16
CABLE DIRECTION
RD DATA L
8
A/D ADDR
RD ADDR L
J4
D OUT <15:00>
A/D DATA
12
A/D DTA TO CABLE L
CONTROL AND HAND-SHAKING
D/A
J3
HANDSHAKING
12
A/D
J4
HANDSHAKING
RD STATUS L
J1
CONTROL CABLE
READ A/D DATA
H&S COMPUTING, INC.
EES/EDS INTERFACE
BLOCK DIAGRAM
READ A/D DATA
DATA PATH
2131
2112-0302
NONE
B
SHEET 1 OF 1

FIG.3.2.0-1

3.2.2-1). Both loops require that the input register, E1 and E2, be loaded from the data bus. The first loop provides for reading the contents of the input register through tristate buffers E3 and E4 (RD DATA L). The second loop requires that the address register E62 be loaded with data contained in the input register. (Note, this is an 8-bit register). In this case, the self-test loop is completed through E31, (RD ADDR L).

In either self-test loop, the data read back from a register should match, bit for bit with the data loaded into that register.

3.2.3 Reading Interface Status

The status of the interface and the ESS may be read by the UDIF through tristate buffers E32 and E33 (RD STATUS L). See Figure 3.2.3-1. All interface/ESS handshaking signals may be read through this path.

3.2.4 Loading the Address Register

The ESS address register may be loaded with data on J2 by first loading the input register with the desired data (LD OUT REG H) and then loading the address register with that data from the input register. See Figure 3.2.4-1. This process is done for both ESS analog-to-digital (A/D) and digital-to-analog (D/A) addresses.

3.2.5 Transferring D/A Data to the ESS

To transfer data to the ESS, the device address in the ESS for which the data is intended must first be loaded into the interface address register (see Figure 3.2.5-1). After the address register has been loaded, the interface input register is loaded with the new data for the ESS. Handshaking then takes place between the interface and the ESS. High Output Data Ready (HODR) is activated, and remains high until the ESS responds with High Output Acknowledged (HOA).

3.2.6 Transferring A/D Data from the ESS

To transfer A/D data from the ESS, the device address in the ESS from which data is required must first be loaded into the interface address register (see Figure 3.2.6-1). After the address register has been loaded, handshaking takes place between the interface and the ESS. High External Function HEF) goes high and remains high until High External Function Acknowledge (HEFA) is received from the ESS.

3.3 Control, Signals, and Logic

3.3.1 Control Signals

User-defined signals from the UDIF are used in the interface for three functions:

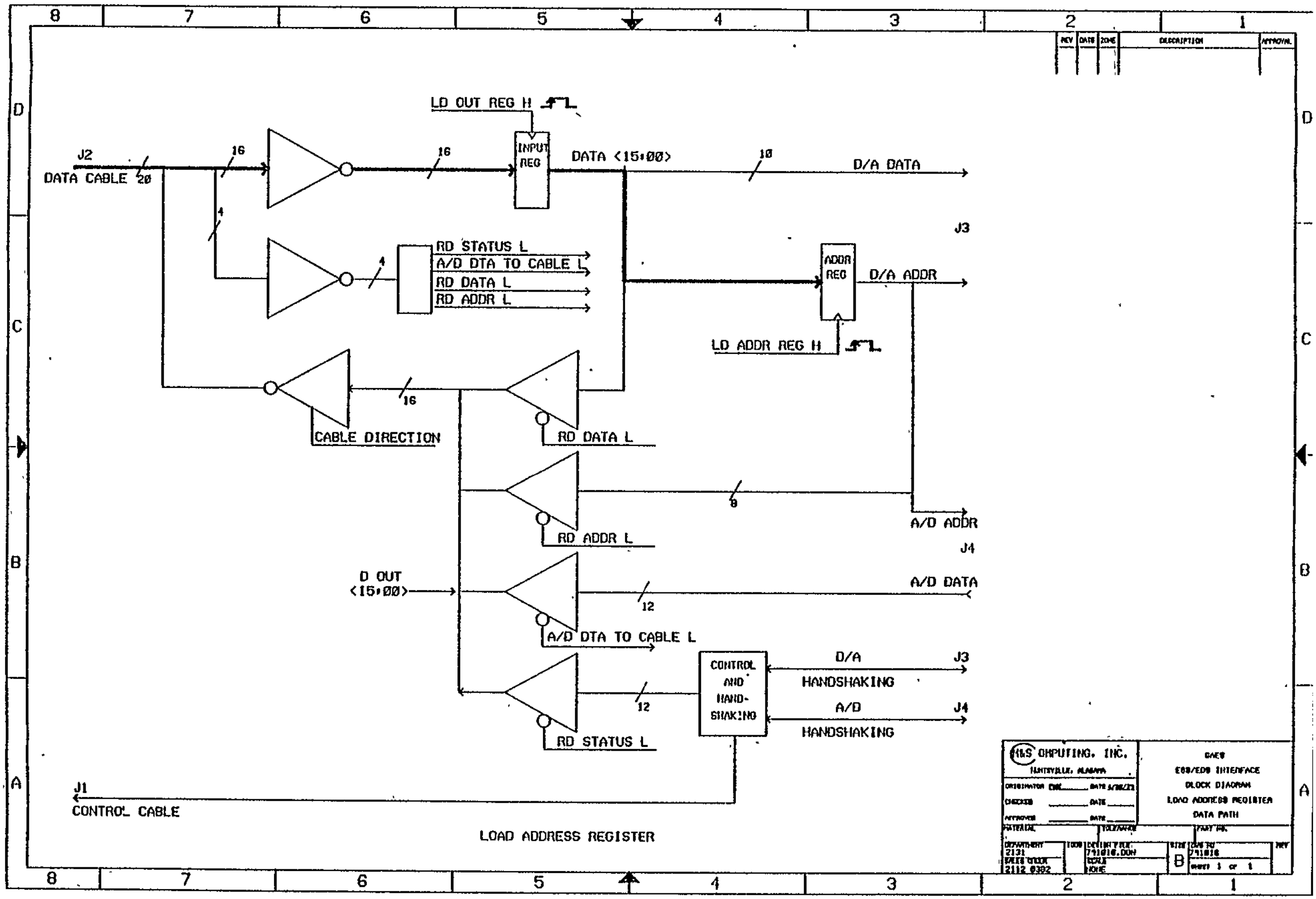

LD OUT REG H
J2
DATA CABLE
20
16
16
INPUT REG
DATA <15:00>
10
D/A DATA
J3
4
4
RD STATUS L
A/D DTA TO CABLE L
RD DATA L
RD ADDR L
ADDR REG
D/A ADDR
LD ADDR REG H
16
CABLE DIRECTION
RD DATA L
8
A/D ADDR
RD ADDR L
J4
D OUT
<15:00>
12
A/D DATA
A/D DTA TO CABLE L
CONTROL AND HAND-SHAKING
D/A
J3
HANDSHAKING
A/D
J4
HANDSHAKING
12
RD STATUS L
J1
CONTROL CABLE
LOAD ADDRESS REGISTER
DATA PATH
BLOCK DIAGRAM
DATA PATH
B
2131
2112 0392

FIG.3.2.4-1

4. EDS SIGMA 560 INTERFACE

4.1 General Information

The EDS Sigma 560 interface (referred to as the interface in Section 4) is composed of two boards: one DEC hex high wirewrap card (W9500), card 1, located in the EDS memory cabinet, and one Xerox wirewrap card, card 2, located remotely in a model 7902 Extended Device Controller. Power for card 1 is supplied from the memory backplane in which it is installed. Card 2 contains a +5 volt regulator and obtains +8 volts from the 7902 in which it is installed.

Communication with the interface from the EDS end takes place through two ribbon cables connected to an M&S Computing MI-018 PDP-11 Unibus DMA Interface also located in the EDS memory cabinet. For UDIF replacement information, see Appendix C. Communication between interface card 1 and card 2 takes place through a single 50-conductor ribbon cable. Interface card 2 communicates with the Sigma 560 through the model 7902 subcontroller (the model 7902 will be considered as part of the Sigma 560 hereafter). Data paths are wirewrapped on the 7902 backplane.

Interface cards 1 and 2 are completely isolated from each other by optical means. Figure 3.1-1 shows how this interface fits into the P6 SAES configuration. Figure 4.1-1 shows the interconnect between this interface and adjacent subsystems. Figure 4.1-2 shows the connector pin function for this interface.

4.2 Data Paths Provided for Different Modes of Operation

4.2.1 Block Diagram Information

Figure 4.2.1-1 is an operational block diagram of the interface. All blocks in this diagram except for the control and handshaking blocks contain designators referring to integrated circuits comprising that block. Bus and signal names used on the block diagram are the same as those used on the schematic, Appendix B.

The number of lines in each bus on the block diagram is designated by a slash mark adjacent to which is a number specifying the number of lines in that bus.

4.2.2 Self-Test Data Path

Figure 4.2.2-1 shows the built-in interface self-test path. Data which has been latched in input register E7 of card 1 is wrapped back around to card 1 as D OUT by E10 and E11 on card 2. This wrapped around data should match bit for bit with the data that was latched in the input register of card 1. EN CSL H is not asserted for this function.

1 FCN 1 Select D/A (active low).

2. FCN 2 Enable parity error (active high).

3. FCN 3 Reset (active high).

NOTE: The parity error bit is connected; however, the parity error circuitry in the interface is not connected back to the UDIF.

3.3.2 D/A Control Logic

Figure 3.3.2-1 shows a timing diagram of signals used in a D/A transfer. The transfer shown is for a single address and data word. If more than one word of data is to be sent to the ESS, the sequence followed by LD DEST REG L, LD ADDR H, TSYNC H, HOA, and HODR will be repeated, transferring one word, address and data, for every cycle as shown until WD CNTR OVF L is asserted by the UDIF. The timing diagram begins in an interface reset state.

3.3.3 A/D Control Logic

Figure 3.3.3-1 shows a timing diagram of signals used in an A/D transfer. The sequence shown is for two words of data, from consecutive addresses in the ESS, being transferred to the EDS. The starting ESS address is loaded when HEF is asserted. After conversion in the ESS (time-dependent on address), HIDR is received, initiating a cycle which will be repeated until WD CNTR OVF H is received from the UDIF ending the block transfer.

The ESS A/D controller reset (HLWF) is asserted by the interface as the inverse of SEL D/A L. The timing diagram begins in an interface reset state.

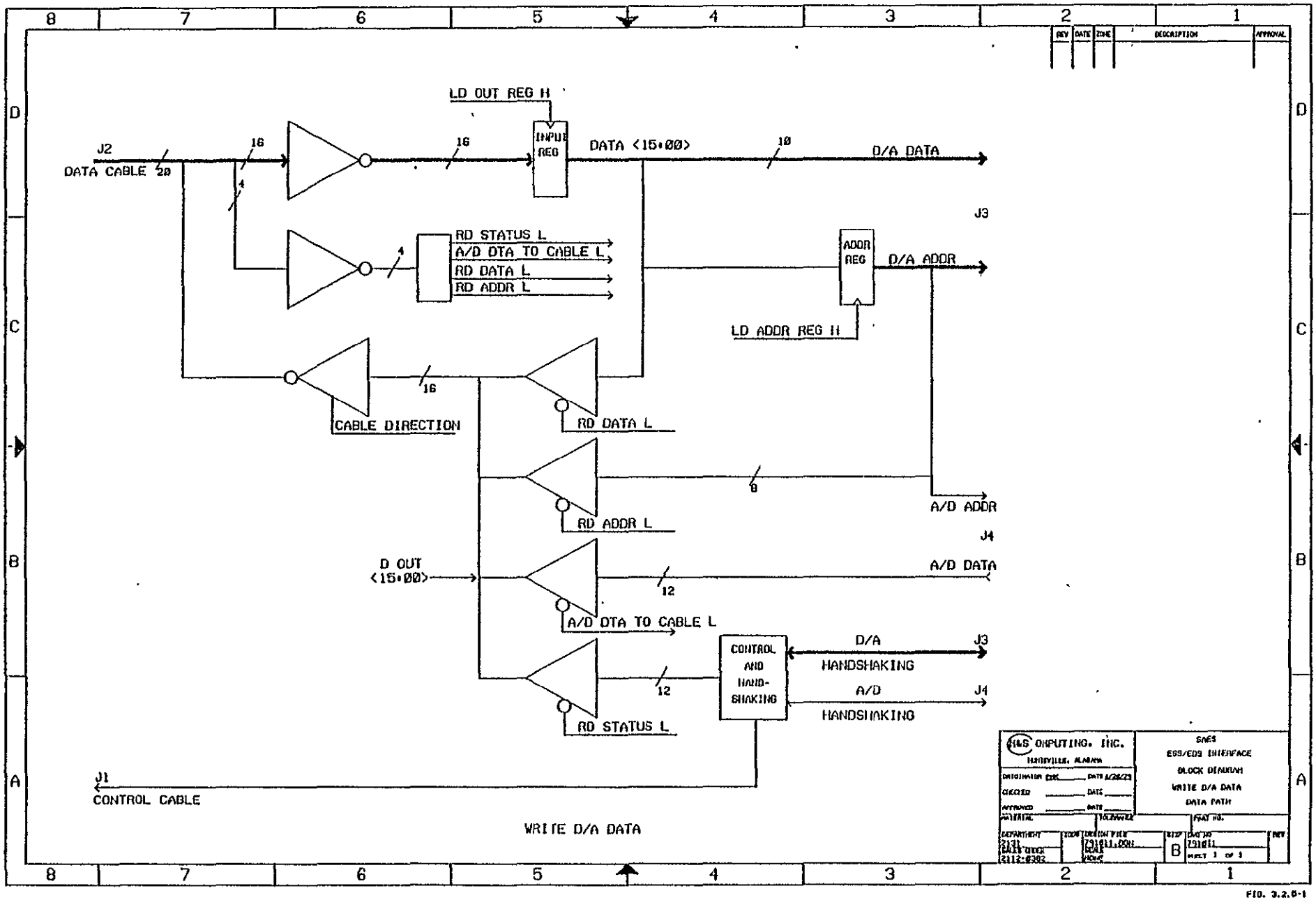
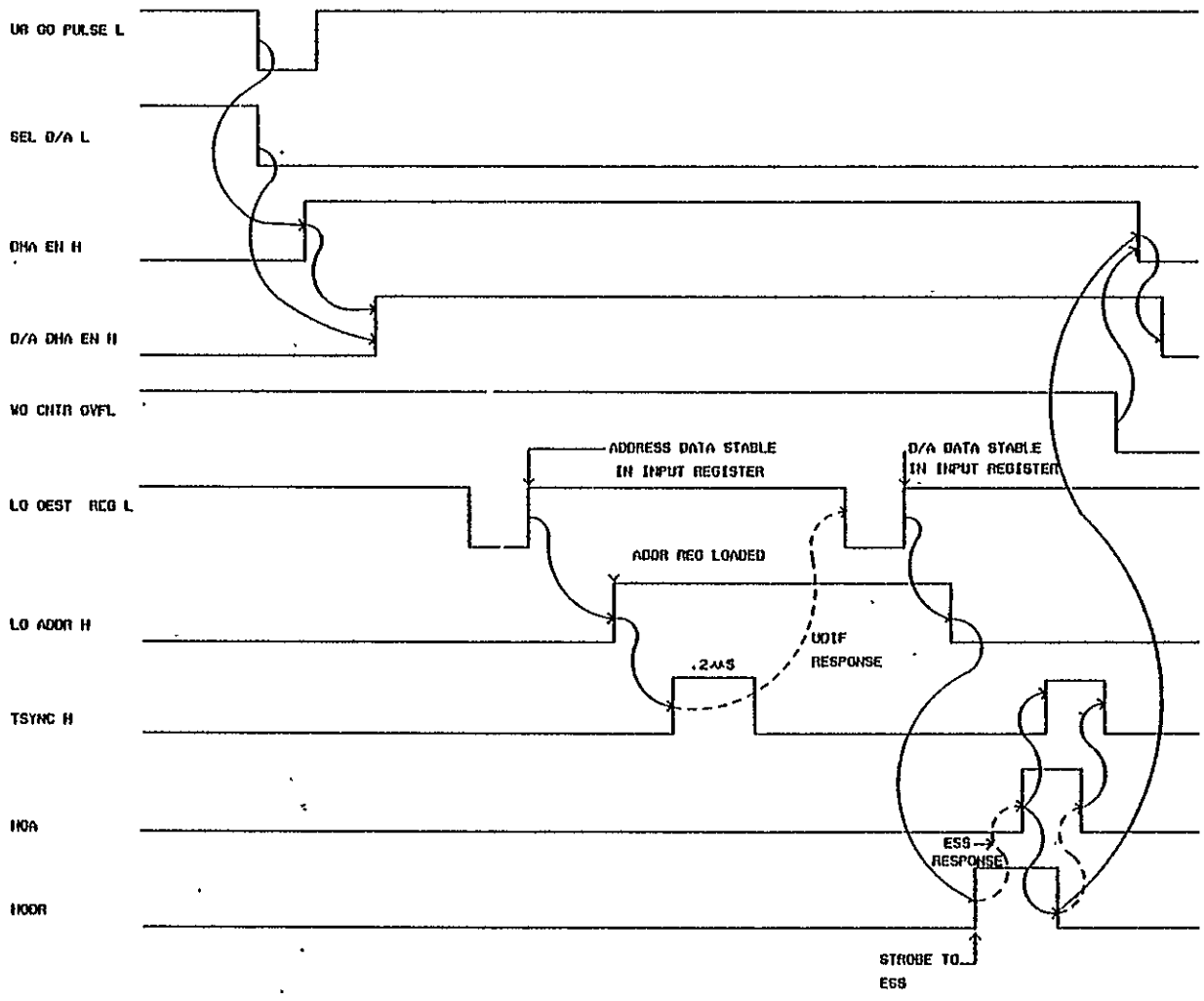

LD OUT REG H
J2
DATA CABLE 20
16
16
INPUT REG
DATA <15:00>
10
D/A DATA
J3
RD STATUS L
A/D DTA TO CABLE L
RD DATA L
RD ADDR L
ADDR REG
D/A ADDR
LD ADDR REG H
CABLE DIRECTION
16
RD DATA L
8
RD ADDR L
A/D ADDR
J4
D OUT <15:00>
A/D DATA
12
A/D DTA TO CABLE L
CONTROL AND HAND-SHAKING
D/A
J3
HANDSHAKING
A/D
J4
HANDSHAKING
12
RD STATUS L
J1
CONTROL CABLE
WRITE D/A DATA
SAES
ESS/EDS INTERFACE
BLOCK DIAGRAM
WRITE D/A DATA
DATA PATH
B

FIG. 3.2.6-1



D/A CONTROL TIMING DIAGRAM

REV	DATE	ZONE	DESCRIPTION	APPROVAL

H&S COMPUTING, INC.
HUNTSVILLE, ALABAMA

ORIGINATOR ENG. _____ DATE ACCEPTED _____
CHECKED _____ DATE _____
APPROVED _____ DATE _____
MATERIAL _____ TOLERANCE _____ PART NO. _____

BAFB
ESS/EDS INTERFACE
D/A CONTROL
TIMING DIAGRAM

DEPARTMENT	TECH	DRAWING TITLE	SIZE	DATE	REV
2131		791813.DGN	B	791813	
CAGE CODE 2112.0302		SCALE NONE		SHEET 1 OF 1	

FIG.3.3.2-1

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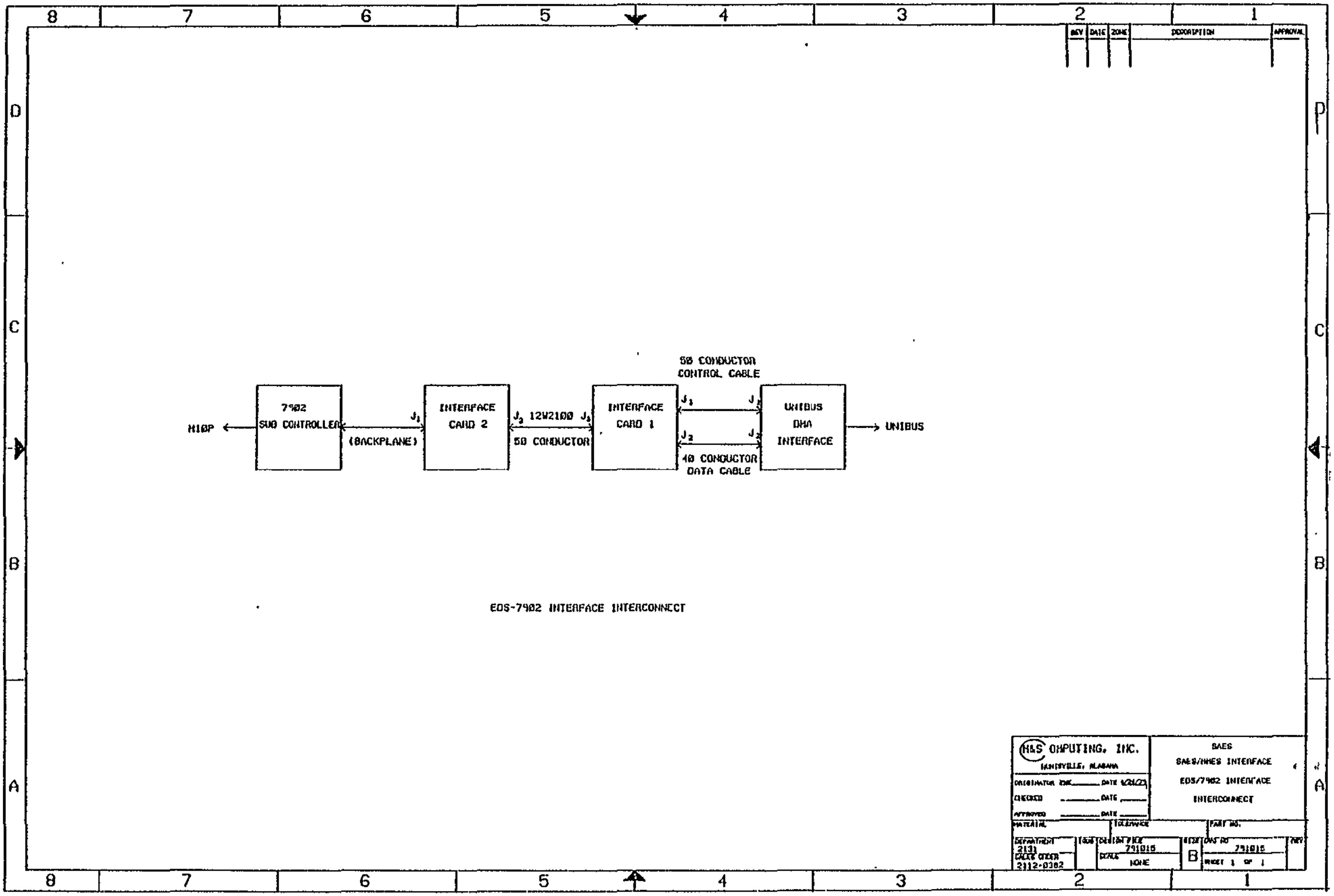


FIG.4.1-1

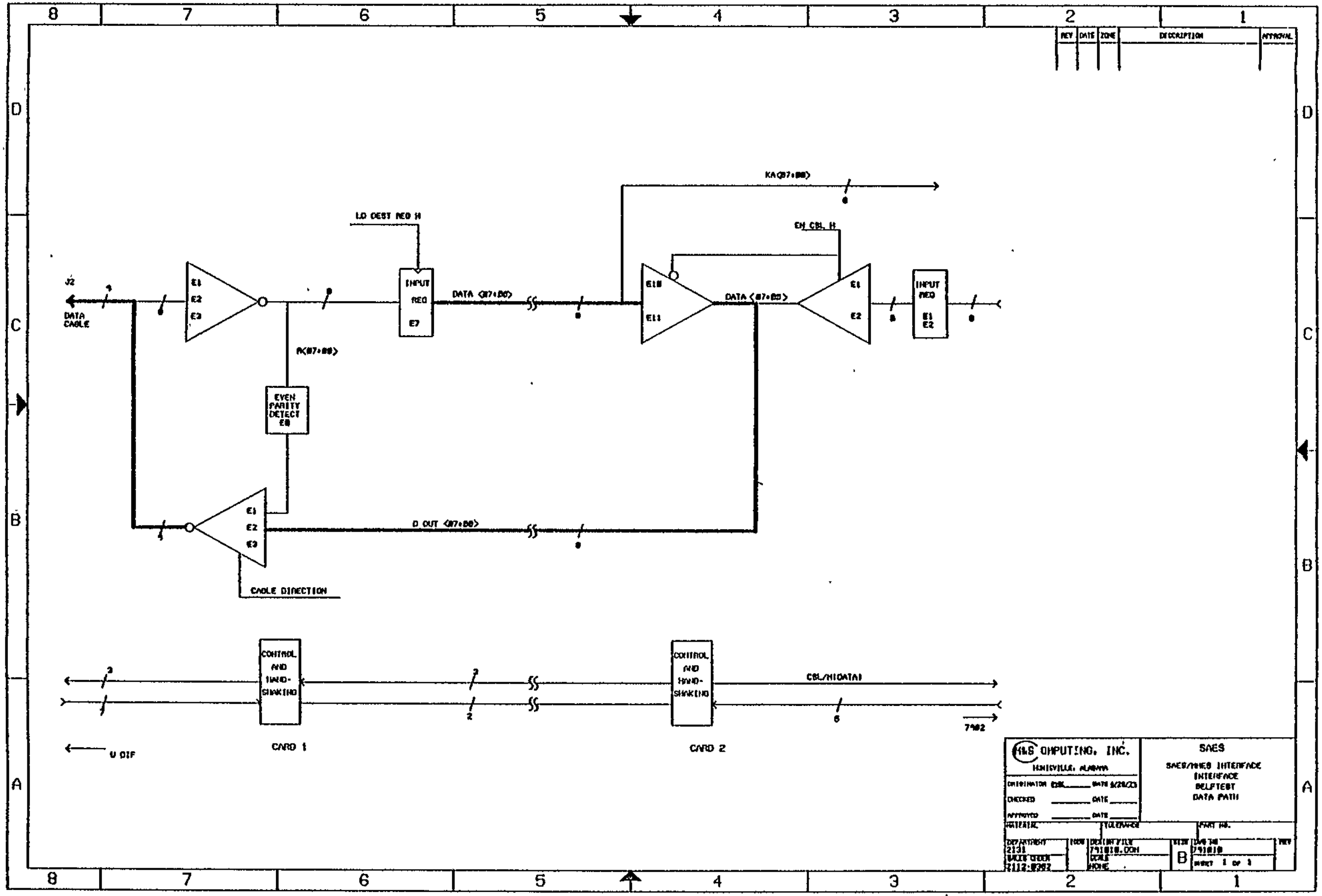

J2
DATA CABLE
LD DEST REG H
INPUT REG
DATA (07÷00)
KA(07÷00)
EN CBL H
DATA (07÷00)
INPUT REG
EVEN PARITY DETECT
D OUT (07÷00)
CABLE DIRECTION
CONTROL AND HAND-SHAKING
CARD 1
CONTROL AND HAND-SHAKING
CARD 2
CBL/HIDATA
SAES
SAES/MHES INTERFACE
INTERFACE
SELFTEST
DATA PATH
SIZE B
SHEET 1 OF 1

FIG. 4.2.2-1

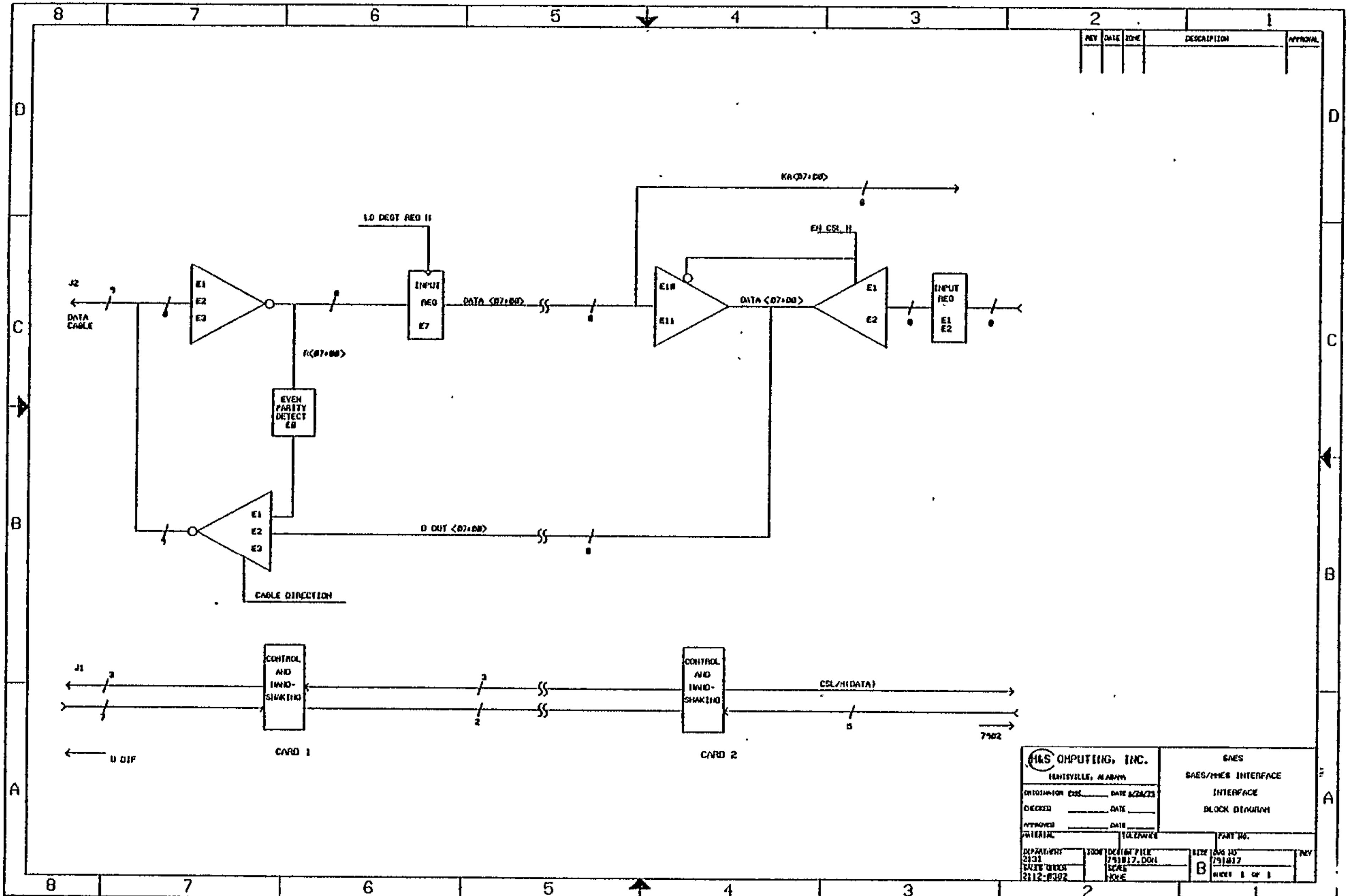

J2
DATA CABLE
E1
E2
E3
LO DEST REQ H
INPUT REG
E7
DATA <D7:D0>
EVEN PARITY DETECT E8
KA<D7:D0>
EN CSL H
E10
E11
DATA <D7:D0>
INPUT REG
D OUT <D7:D0>
CABLE DIRECTION
J1
CONTROL AND HAND-SHAKING
CARD 1
CONTROL AND HAND-SHAKING
CARD 2
CSL/H(DATA)
7902
D DIF
H&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/MMES INTERFACE
INTERFACE
BLOCK DIAGRAM
DEPARTMENT 2131
DESIGN FILE 791817.DGN
SCALE NONE
SIZE B
DWG NO 791817
SHEET 1 OF 1

FIG. 4.2.1-1

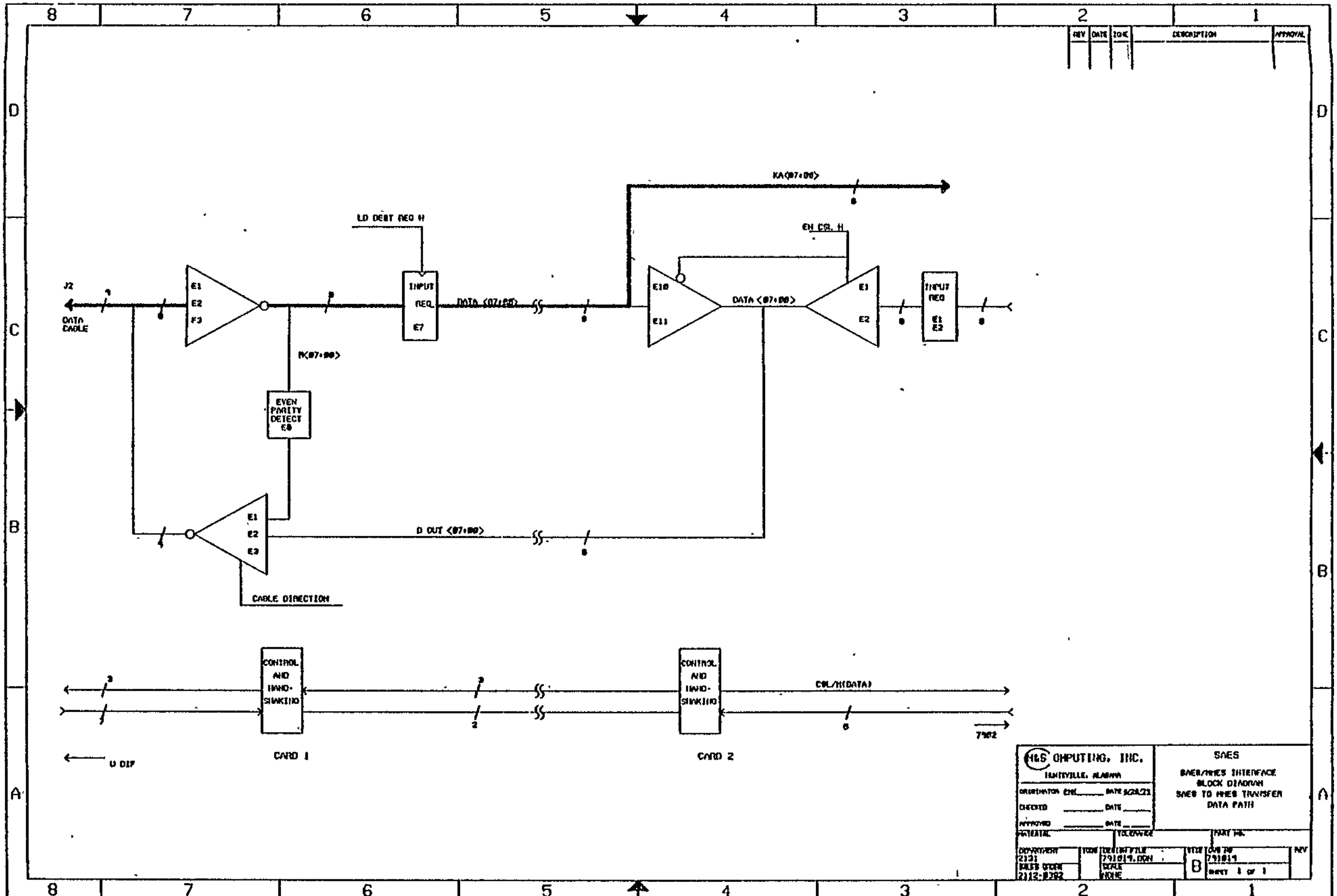

J2
DATA CABLE
INPUT REG
E7
DATA <07:00>
KA<07:00>
EN CSL H
DATA <07:00>
E10
E11
E1
E2
INPUT REG
EVEN PARITY DETECT E8
D OUT <07:00>
CABLE DIRECTION
CONTROL AND HAND-SHAKING
CARD 1
CONTROL AND HAND-SHAKING
CARD 2
7902
SAES
SAES/MHES INTERFACE
BLOCK DIAGRAM
SAES TO MHES TRANSFER
DATA PATH
791019.DGN
791019
SHEET 1 OF 1

Fig. 4.2.3-1

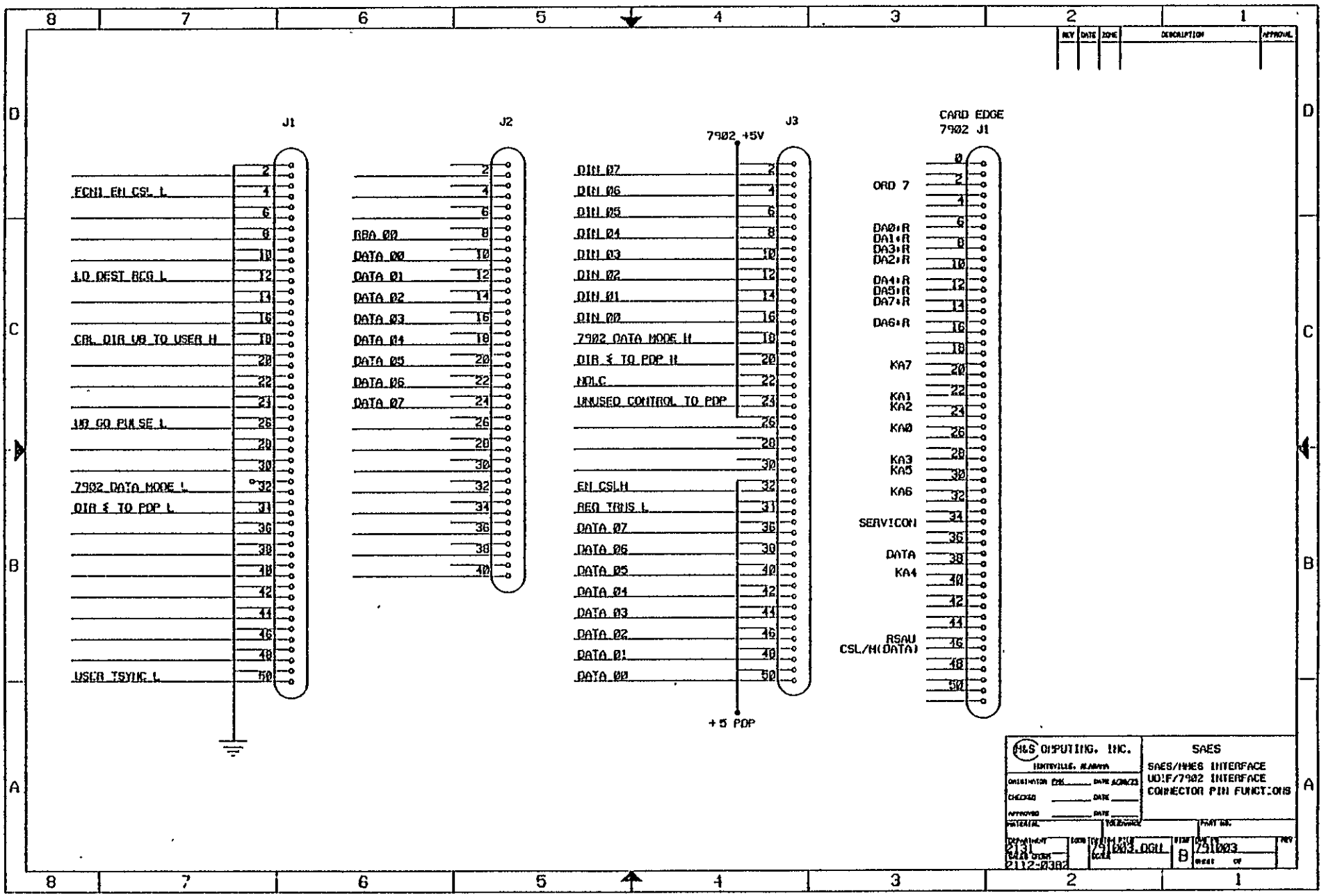

J1
J2
J3
CARD EDGE
7902 J1
7902 +5V
+5 PDP
FCN1 EN CSL L
LD DEST REG L
CBL DIR UB TO USER H
UB GO PULSE L
7902 DATA MODE L
DIR $ TO PDP L
USER TSYNC L
RBA 00
DATA 00
DATA 01
DATA 02
DATA 03
DATA 04
DATA 05
DATA 06
DATA 07
DIN 07
DIN 06
DIN 05
DIN 04
DIN 03
DIN 02
DIN 01
DIN 00
7902 DATA MODE H
DIR $ TO PDP H
NOLC
UNUSED CONTROL TO PDP
EN CSLH
REG TRNS L
DATA 07
DATA 06
DATA 05
DATA 04
DATA 03
DATA 02
DATA 01
DATA 00
ORD 7
DA0:R
DA1:R
DA3:R
DA2:R
DA4:R
DA5:R
DA7:R
DA6:R
KA7
KA1
KA2
KA0
KA3
KA5
KA6
SERVICON
DATA
KA4
RSAU
CSL/H(DATA)
H&S COMPUTING, INC.
SAES
SAES/HHES INTERFACE
UDIF/7902 INTERFACE
CONNECTOR PIN FUNCTIONS
751003.DGU
751003
B

FIG 4.1-2

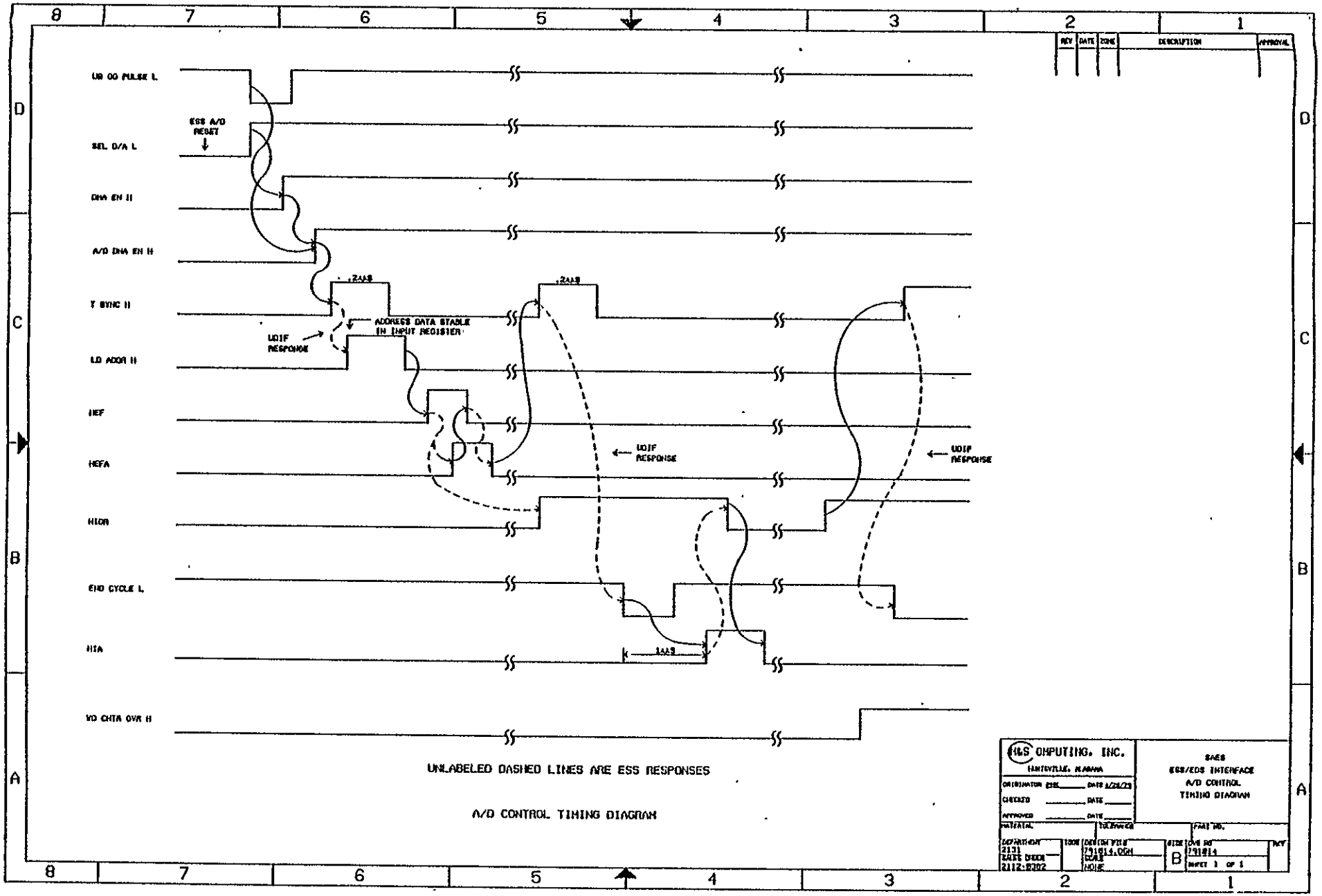

UB 00 PULSE L
ESS A/D RESET
SEL D/A L
DHA EN H
A/D DHA EN H
T SYNC H
LD ADDR H
HEF
HEFA
HIOR
END CYCLE L
HIA
VD CHTA OVR H
.2AS
ADDRESS DATA STABLE IN INPUT REGISTER
UDIF RESPONSE
UDIF RESPONSE
UDIF RESPONSE
1AS
UNLABELED DASHED LINES ARE ESS RESPONSES
A/D CONTROL TIMING DIAGRAM
REV
DATE
ZONE
DESCRIPTION
APPROVAL
MS COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
ESS/EDS INTERFACE
A/D CONTROL
TIMING DIAGRAM
SIZE
B

Fig. 3.3.3-1

4.2.3 Transferring Data to the Sigma 560

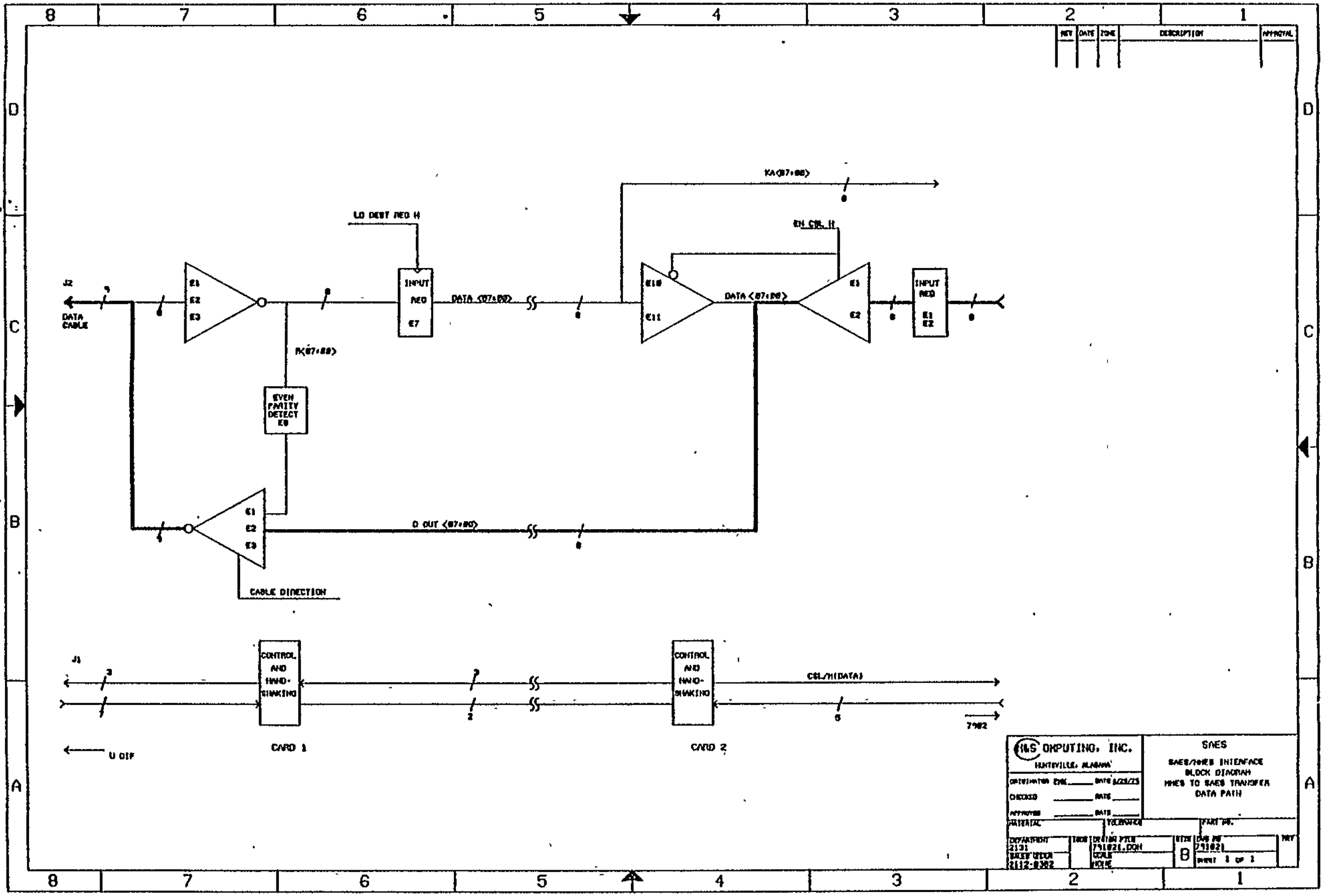
Figure 4.2.3-1 shows the path data takes when being transferred from the EDS to the Sigma 560. It should be noted that the EDS is slaved to the Sigma 560 as far as transfers are concerned; that is, the Sigma 560 sets the direction in which a transfer is to take place and then initiates the transfer.

Figure 4.2.3-2 shows a timing diagram of two transfers from EDS to Sigma 560. The transfer is initiated by the 7902 subcontroller asserting DATA. The direction which the transfer is to take place is present when this signal is sent. The UDIF will respond to this DATA interrupt by loading one byte of data in the interface card 1 input register. The LD DEST REG H pulse which latches data in the input register also triggers a chain of events which connect service to the 7902 and latch the data there. A transfer is completed when the signal DATA is dropped. Point A on the timing diagram marks where one transfer ends and the next begins.

4.2.4 Transferring Data from the Sigma 560 to the EDS

Figure 4.2.4-1 shows the data path for transferring data from the Sigma 560 to the EDS. In this mode, there may only be one byte of data processed per transfer.

Figure 4.2.4-2 shows a timing diagram of a transfer from the Sigma 560 to the EDS. The transfer is initiated by the 7902 subcontroller asserting DATA. The direction in which the transfer is to take place is present when this signal is sent. The UDIF will respond to this DATA interrupt with a UB GO PULSE H which triggers a chain of events latching data from the 7902 in the interface card 2 input register and then in the UDIF destination register. After data has been latched in the card 2 input register, the transfer is ended by DATA dropping to a low state.

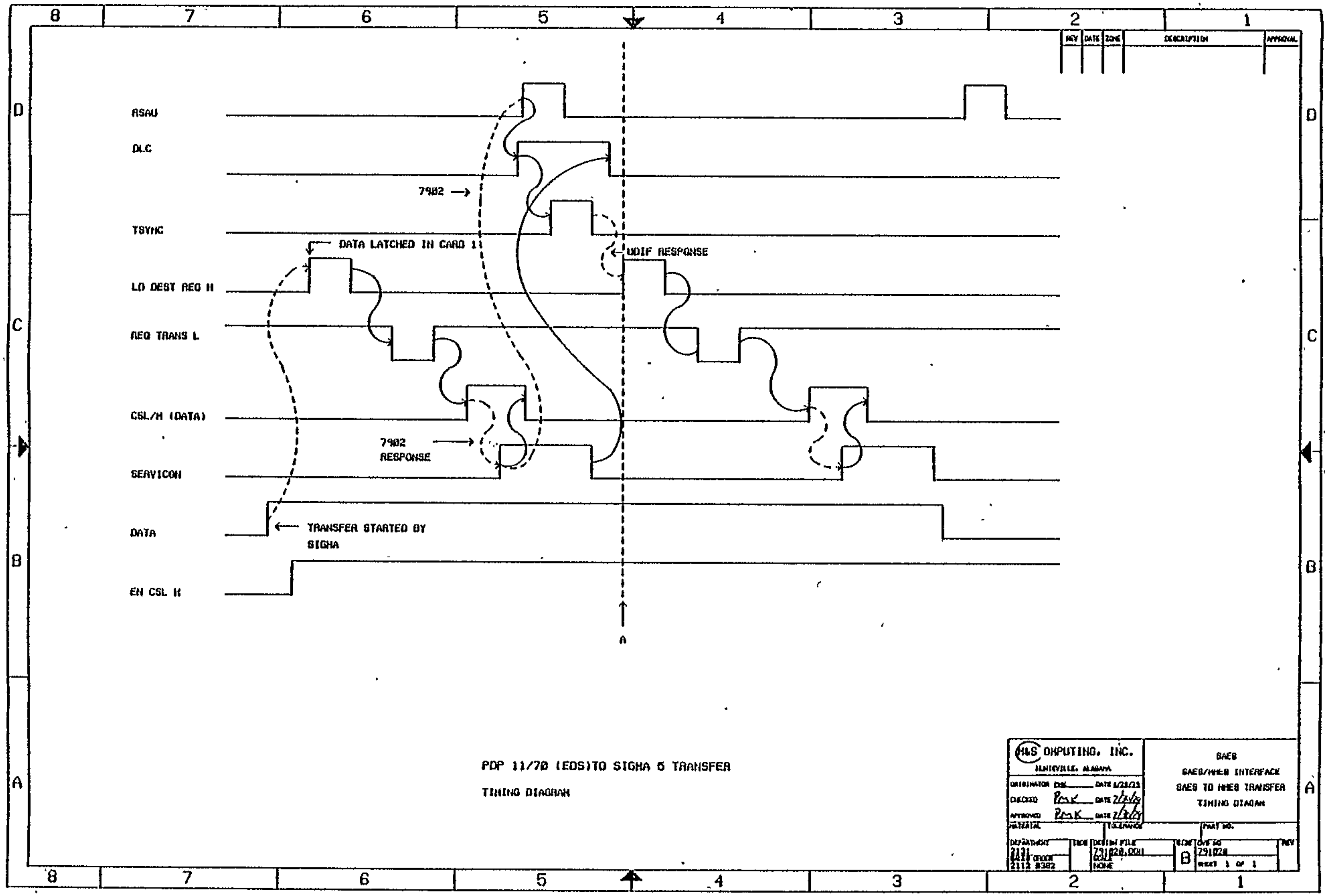


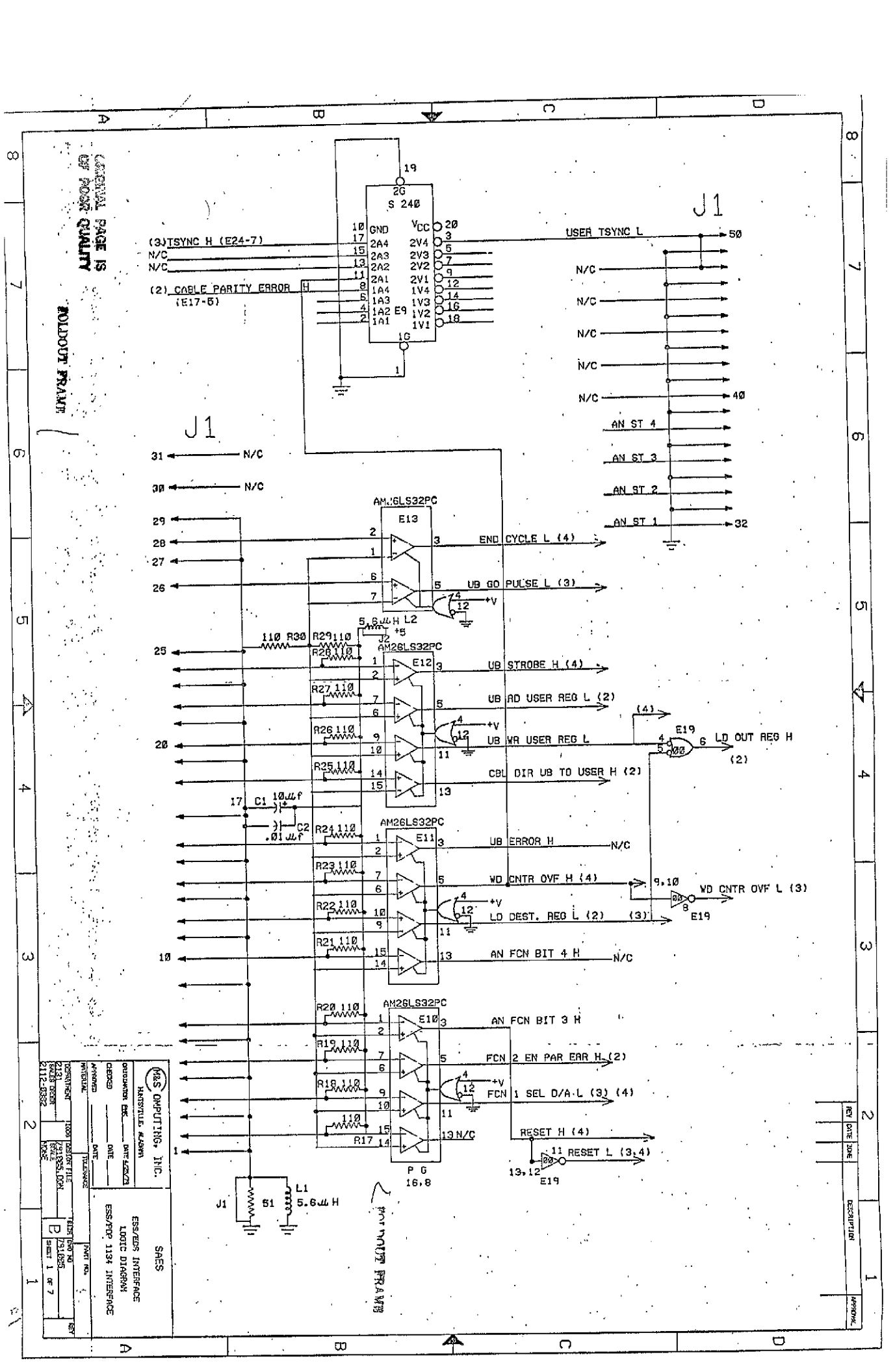
J2
DATA CABLE
INPUT
REG
E7
LD DEST REG H
DATA <07:00>
EVEN PARITY DETECT E8
D OUT <07:00>
CABLE DIRECTION
EN CBL H
E10
E11
INPUT REG
E1
E2
J1
CONTROL AND HAND-SHAKING
CARD 1
CARD 2
SAES
BLOCK DIAGRAM
DATA PATH
DEPARTMENT 2131
SIZE B
SHEET 1 OF 1

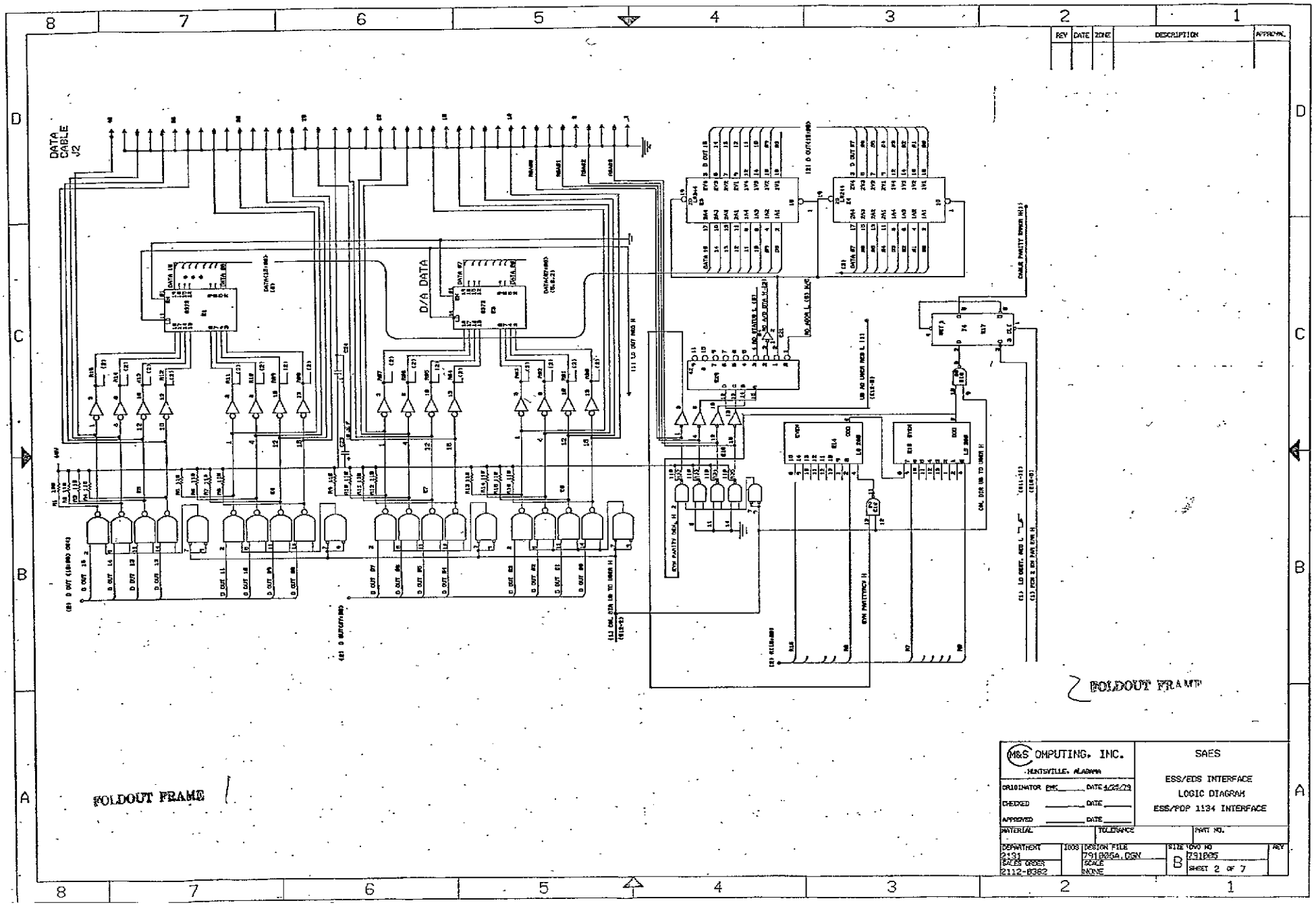
FIG. 4.2.4-1

APPENDIX A

SCHEMATICS AND WIREWRAP LIST


RSAU
DLC
TSYNC
LD DEST REQ H
REQ TRANS L
CSL/H (DATA)
SERVICON
DATA
EN CSL H
7902 →
DATA LATCHED IN CARD 1
UDIF RESPONSE
7902 RESPONSE
TRANSFER STARTED BY SIGMA
A
PDP 11/70 (EOS) TO SIGMA 5 TRANSFER
TIMING DIAGRAM
H&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
ORIGINATOR
CHECKED
APPROVED
MATERIAL
TOLERANCE
PART NO.
DEPARTMENT
2131
DESIGN FILE
791020.001
SCALE
NONE
B
791020
SHEET 1 OF 1
REV
SAES
SAES/HMES INTERFACE
SAES TO HMES TRANSFER
TIMING DIAGRAM
FIG.4.2.3-2


ORIGINAL PAGE IS OF POOR QUALITY
FOLDOUT FRAME
J1
(3)TSYNC H (E24-7)
N/C
N/C
(2) CABLE PARITY ERROR H (E17-6)
S 240
USER TSYNC L
N/C
AN ST 4
AN ST 3
AN ST 2
AN ST 1
AM26LS32PC
E13
END CYCLE L (4)
UB GO PULSE L (3)
L2
J2
E12
UB STROBE H (4)
UB RD USER REG L (2)
UB WR USER REG L
CBL DIR UB TO USER H (2)
C1 10uf
C2 .01uf
E11
UB ERROR H
WD CNTR OVF H (4)
LD DEST. REG L (2)
AN FCN BIT 4 H
E10
AN FCN BIT 3 H
FCN 2 EN PAR ERR H (2)
FCN 1 SEL D/A L (3) (4)
RESET H (4)
E19
LD OUT REG H
WD CNTR OVF L (3)
RESET L (3,4)
L1 5.6uH
R1
P G 16,8
M&S COMPUTING, INC.
SAES
ESS/EDS INTERFACE
LOGIC DIAGRAM
ESS/EDP 1134 INTERFACE



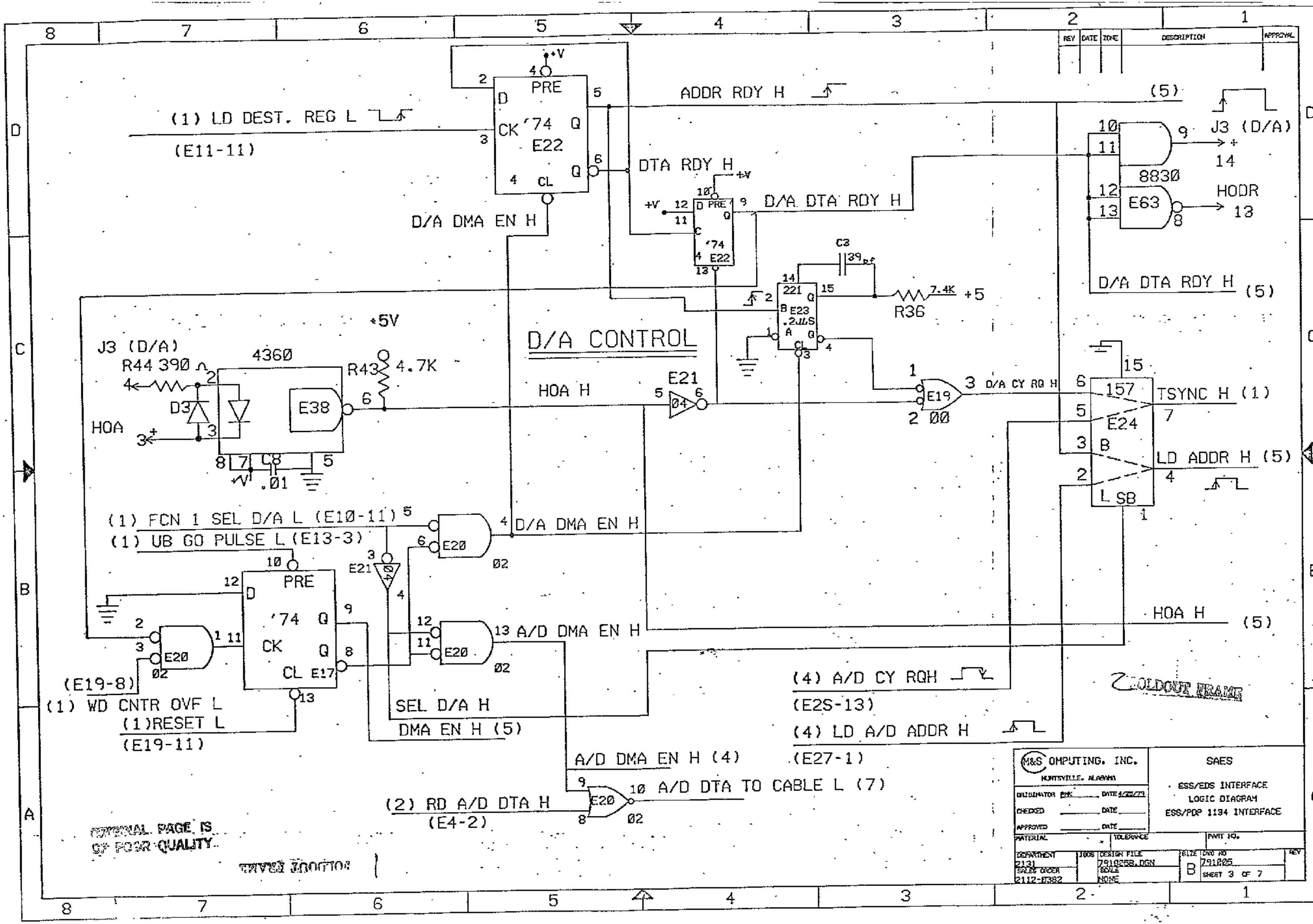
REV	DATE	ZONE	DESCRIPTION	APPROVAL

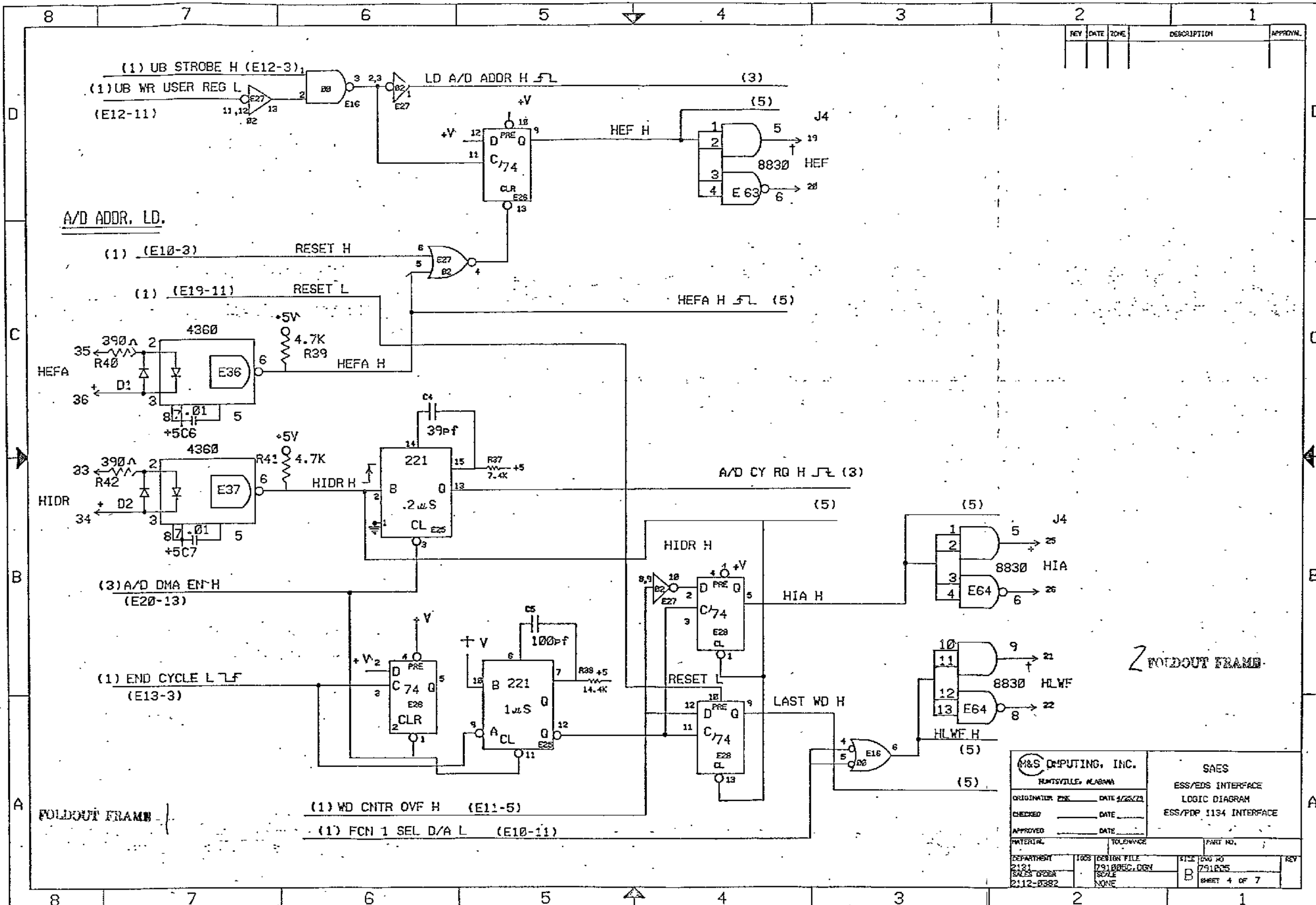
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA

SAES

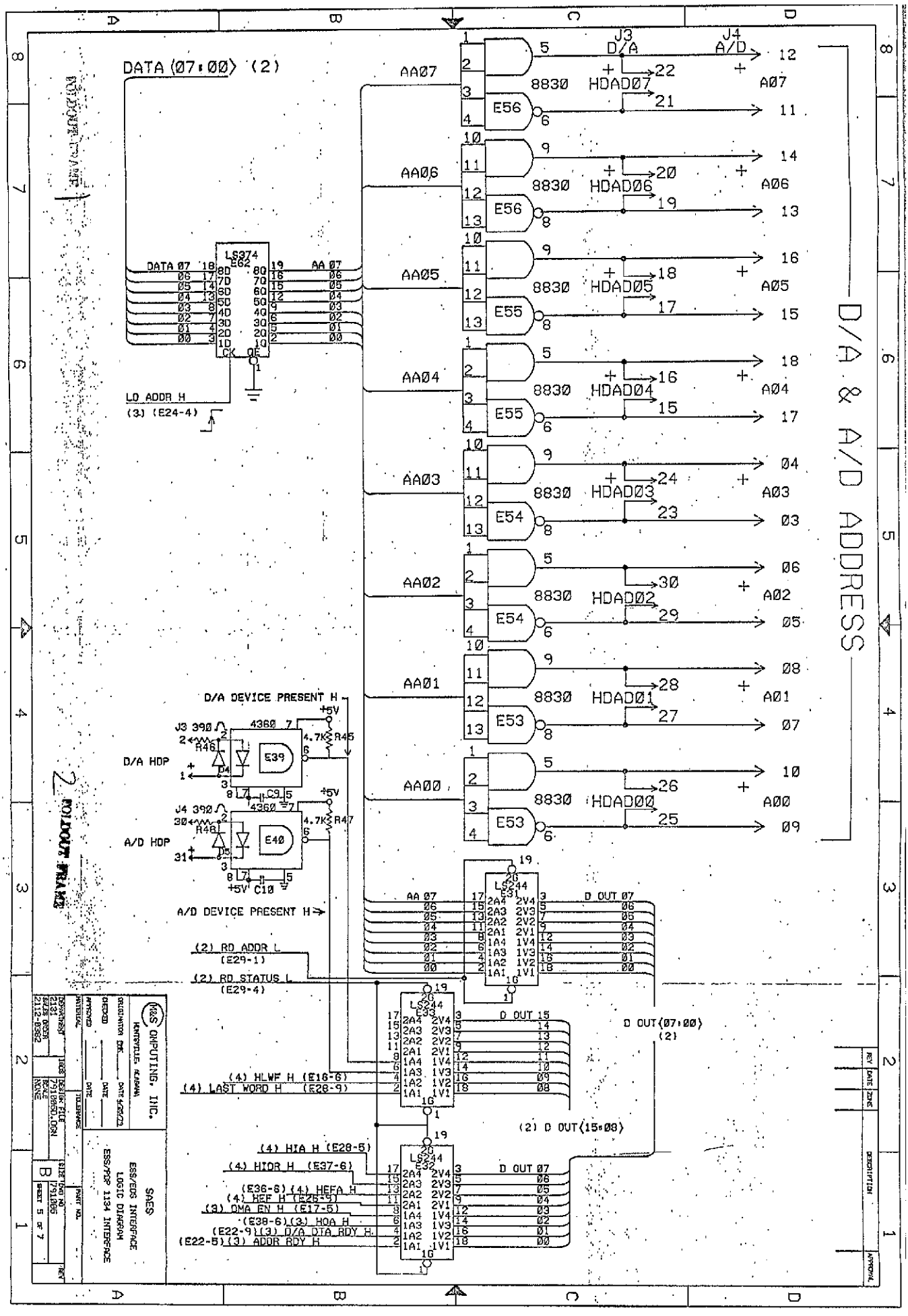
ESS/EDS INTERFACE
LOGIC DIAGRAM
ESS/PDP 1134 INTERFACE

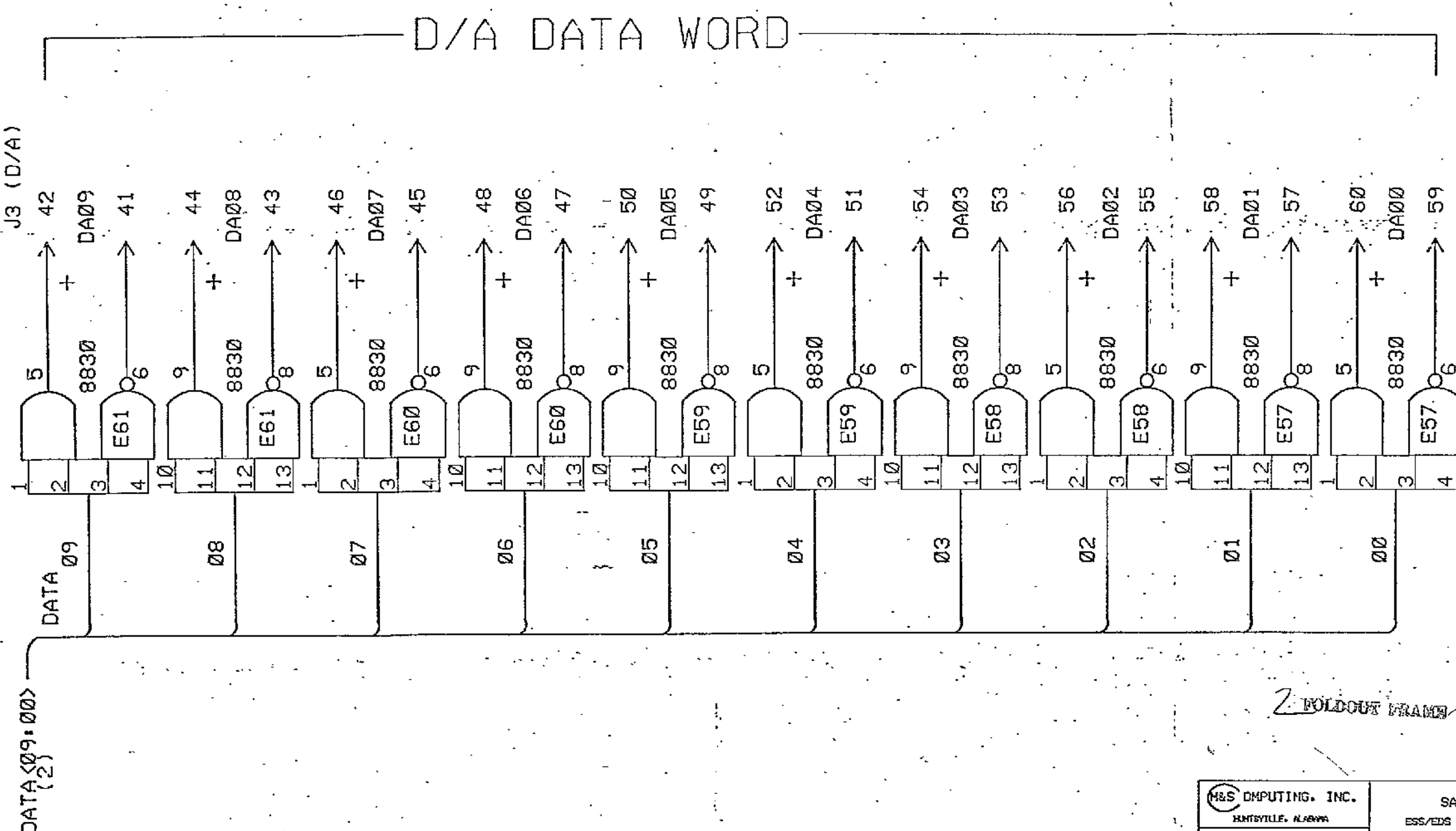
ORIGINATOR EMS	DATE 4/25/79		
CHECKED	DATE		
APPROVED	DATE		
MATERIAL	TOLERANCE	PART NO.	
DEPARTMENT 2131	1003	DESIGN FILE 791805A.DGN	SIZE B
SALES ORDER 2112-8362		SCALE NONE	DWG NO 791805
			SHEET 2 OF 7
			REV


D/A CONTROL
(1) LD DEST. REG L
(E11-11)
PRE
CK '74 E22
CL
D/A DMA EN H
ADDR RDY H
DTA RDY H
D/A DTA RDY H
(5)
J3 (D/A)
14
8830
E63
HODR
13
D/A DTA RDY H (5)
C3
39pf
221
E23
.2µS
R36
7.4K
+5
+5V
J3 (D/A)
R44 390 Ω
4360
R43
4.7K
E38
D3
HOA
C8
.01
HOA H
E21
04
E19
00
D/A CY RQ H
157
E24
TSYNC H (1)
LD ADDR H (5)
SB
(1) FCN 1 SEL D/A L (E10-11)
(1) UB GO PULSE L (E13-3)
E20
02
D/A DMA EN H
A/D DMA EN H
HOA H (5)
E17
(E19-8)
(1) WD CNTR OVF L
(1)RESET L
(E19-11)
SEL D/A H
DMA EN H (5)
(4) A/D CY RQH
(E25-13)
(4) LD A/D ADDR H
(E27-1)
A/D DMA EN H (4)
(2) RD A/D DTA H
(E4-2)
A/D DTA TO CABLE L (7)
FOLDOUT FRAME
ORIGINAL PAGE IS OF POOR QUALITY
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
ESS/EDS INTERFACE LOGIC DIAGRAM
ESS/PDP 1134 INTERFACE
DESIGN FILE 791025B.DGN
SCALE NONE
SIZE B
DWG NO 791025
SHEET 3 OF 7
DEPARTMENT 2131
SALES ORDER 2112-0382



A/D ADDR. LD.
(1) UB STROBE H (E12-3)
(1) UB WR USER REG L
(E12-11)
LD A/D ADDR H
(3)
(5)
+V
HEF H
J4
8830
HEF
E63
(1) (E10-3)
RESET H
E27
(1) (E19-11)
RESET L
HEFA H
(5)
4360
390Ω
R40
D1
HEFA
E36
+5V
4.7K
R39
+5C6
C4
39pf
221
.2µS
R37
7.4K
R41
R42
D2
HIDR
E37
HIDR H
A/D CY RQ H
(3)
(5)
+5C7
(3) A/D DMA EN H
(E20-13)
HIDR H
HIA H
8830
HIA
E64
C5
100pf
221
1µS
R38
14.4K
(1) END CYCLE L
(E13-3)
RESET L
LAST WD H
E16
HLWF H
8830
HLWF
(1) WD CNTR OVF H (E11-5)
(1) FCN 1 SEL D/A L (E10-11)
FOLDOUT FRAME
FOLDOUT FRAME
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
ORIGINATOR PHK DATE 4/25/73
CHECKED DATE
APPROVED DATE
SAES
ESS/EDS INTERFACE
LOGIC DIAGRAM
ESS/PDP 1134 INTERFACE
MATERIAL
TOLERANCE
PART NO.
DEPARTMENT 2121
SALES ORDER 2112-0382
DESIGN FILE 791005C.DGN
SCALE NONE
SIZE B
DWG NO 791005
SHEET 4 OF 7
REV
DATE
ZONE
DESCRIPTION
APPROVAL


D/A & A/D ADDRESS
DATA (07:00) (2)
J3 D/A
J4 A/D
AA07
AA06
AA05
AA04
AA03
AA02
AA01
AA00
8830 HDAD07
8830 HDAD06
8830 HDAD05
8830 HDAD04
8830 HDAD03
8830 HDAD02
8830 HDAD01
8830 HDAD00
A07
A06
A05
A04
A03
A02
A01
A00
E56
E55
E54
E53
LS374 E62
LD ADDR H
(3) (E24-4)
D/A DEVICE PRESENT H
A/D DEVICE PRESENT H
D/A HDP
A/D HDP
E39
E40
4360
4.7K R45
4.7K R47
R46
R48
C9
C10
LS244 E31
LS244 E33
LS244 E32
(2) RD ADDR L (E29-1)
(2) RD STATUS L (E29-4)
(4) HLWF H (E18-6)
(4) LAST WORD H (E28-9)
(4) HIA H (E28-5)
(4) HIOR H (E37-6)
(E36-6)(4) HEFA H
(4) HEF H (E28-5)
(3) DMA EN H (E17-5)
(E38-6)(3) HOA H
(E22-9)(3) D/A DTA RDY H
(E22-5)(3) ADDR RDY H
D OUT 07
D OUT 15
D OUT (07:00) (2)
(2) D OUT (15:08)
ONPUTING, INC.
ESS/EDS INTERFACE
LOGIC DIAGRAM
ESS/PDP 1134 INTERFACE
SAES



FOLDOUT FRAME

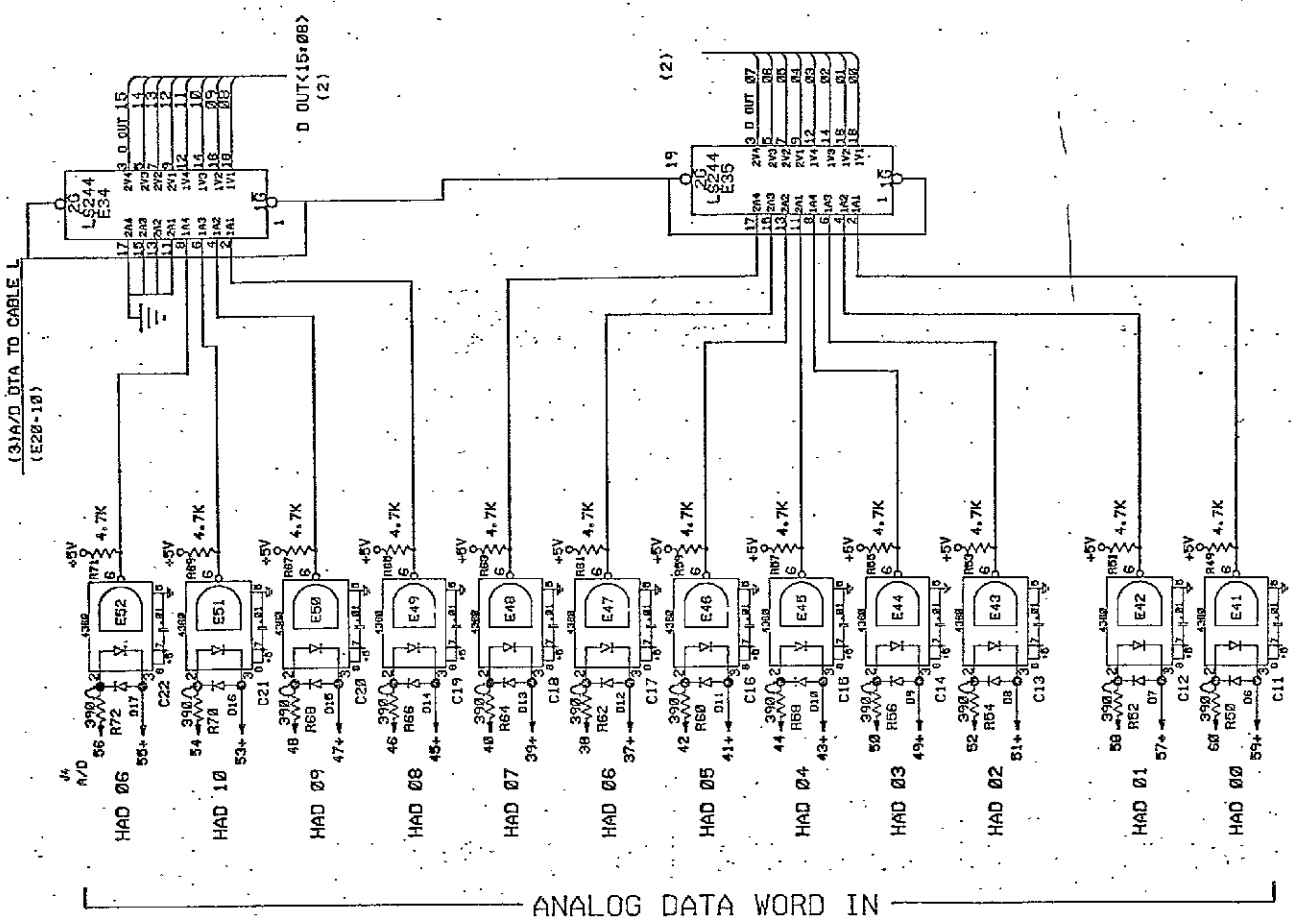
2 FOLDOUT FRAME

M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA

ORIGINATOR PHK DATE 6/25/79
CHECKED DATE
APPROVED DATE

SAES
ESS/EDS INTERFACE
LOGIC DIAGRAM
ESS/PDP 1134 INTERFACE

MATERIAL	TOLERANCE	PART NO.
DEPARTMENT 2131 / SALES ORDER 2112-0302	DESIGN FILE 791005E.DGN / SCALE NONE	SIZE B / DWG NO 791005 / SHEET 6 OF 7



FOLDOUT FRAME

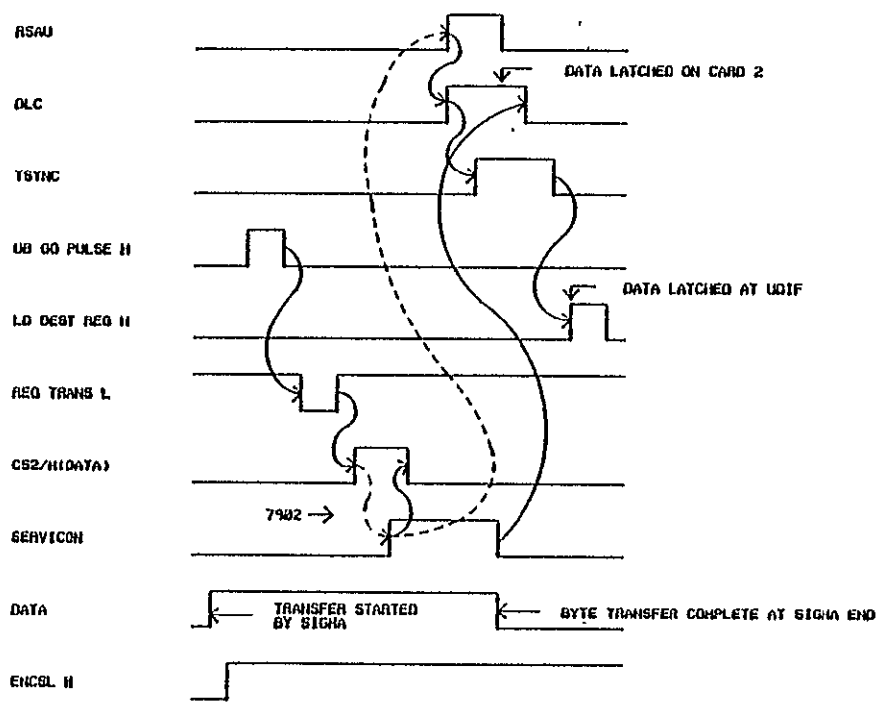
ORIGINAL PAGE IS
OF POOR QUALITY

2 FOLDOUT FRAME

M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA

SAES
ESS/EDS INTERTERFACE
LOGIC DIAGRAM
ESS/PDP 1134 INTERFACE

DESIGNATOR ENG	DATE 5/23/79		
CHECKED	DATE		
APPROVED	DATE		
MATERIAL	TOLERANCE	PART NO.	
DEPARTMENT 2131 SCALE NONE 2112-6382	DESIGN FILE 7910855F.DGN SCALE NONE	SIZE B	DWG NO 7910855 SHEET 7 OF 7



PDP 11/70 (EDS)TO SIGMA 6 TRANSFER

TIMING DIAGRAM

FIG. 4.2.4-2

SAES
ESS/EDS INTERFACE
LAYOUT
WIREWRAP LIST

PARTS LIST

ESS/UDIF IF

PAGE #1

QUANTITY	DESCRIPTION
2	74LS373
1	74S240
7	74LS244
1	74LS374
4	AM26LS32PC
5	8641
2	74S280
1	7442
4	7474
3	7400
1	7404
2	7402
1	74157
2	74221
11	8830
17	4360, IC (HP OPTO ISOLATOR)
1	W9500, DEC WIREWRAP BOARD
17	4484, HP LED
1	50 PIN 3M WW HEADER
2	60 PIN 3M WW HEADER

PARTS LIST

ESS/UDIF IF

QUANTITY	DESCRIPTION
33	110Ω 5% 1/4wt
1	180Ω 5% 1/4wt
17	4.7K 5% 1/4wt
17	340Ω 5% 1/4wt
2	7.15K 1% 1/8 WT
1	15K 5% 1/4wt
2	39 pf 200V, DISC CAP
1	100pf 200V, DISC CAP
37	.1μf 200V, DISC CAP
26	10μf 25V, TANT CAP

PART NO.	VALUE / TYPE	LOCATION
E1	74LS373	LL-1
E2	74LS373	LL-13
E3	74LS244	LL-25
E4	74LS244	LL-37
E5	8641	JJ-1
E6	8641	JJ-16
E7	8641	JJ-32
E8	8641	JJ-48
E9	74S240	LL-49
E10	AM26LS32 PC	FF-1
E11	AM26LS32PC	FF-16
E12	AM26LS32PC	FF-32
E13	AM26LS32PC	FF-48
E14	74S280	DD-1 *
E15	74S280	DD-10
E16	7400	DD-A
E17	7474	DD-28
E18	8641	DD-46
E19	7400	FF-57
E20	7402	DD-37
E21	7404	BB-58
E22	7474	BB-49
E23	74221	BB-39
E24	74157	BB-26
E25	74221	BB-13
E26	7474	BB-1
E27	7402	Z-1
E28	7474	Z-10
E29	7442	Z-19
E30	———	———
E31	74S244	W-1
E32	74S244	W-13
E33	74S244	W-25
E34	74S244	W-37

PART NO.	VALUE / TYPE	LOCATION
E35	74S244	W-49
E36	4360	U-18 (U-59)
E37	4360	U-28 (U-49)
E38	4360	U-38 (U-39)
E39	4360	U-48 (U-29)
E40	4360	U-58 (U-19)
E41	4360	K-58
E42	4360	K-48
E43	4360	K-38
E44	4360	K-28
E45	4360	K-18
E46	4360	K-Ø8
E47	4360	H-58
E48	4360	H-48
E49	4360	H-38
E50	4360	H-28
E51	4360	H-18
E52	4360	H-Ø8
E53	8830	M-57
E54	8830	M-49
E55	8830	M-41
E56	8830	M-33
E57	8830	M-25
E58	8830	M-17
E59	8830	M-9
E60	8830	M-1
E61	8830	P-1
E62	74LS374	E-1
E63	8830	Z-38
E64	8830	Z-29

SEE NOTE

* INSTALLED BACKWARDS ON SN 1

NOTE: PINS ARE INDICATED FOR SN 2, SN 1 DIFFERS AS NOTED

PART NO.	VALUE / TYPE	LOCATION
R1	180	JJ-10
R2	110	JJ-11
R3		JJ-12
R4		JJ-13
R5		JJ-26
R6		JJ-27
R7		JJ-28
R8		JJ-29
R9		JJ-42
R10		JJ-43
R11		JJ-44
R12		JJ-45
R13		JJ-57
R14		JJ-58
R15		JJ-59
R16	110	JJ-60
R17		FF-10
R18		FF-11
R19		FF-12
R20		FF-13
R21		FF-26
R22		FF-27
R23		FF-28
R24		FF-29
R25		FF-42
R26		FF-43
R27		FF-44
R28		FF-45
R29		JJ-61
R30	110	JJ-62
R31	51	JJ-64
R32	110	DD-56
R33		DD-57
R34		DD-58

PART NO.	VALUE / TYPE	LOCATION
R35	110	DD-59
R36	7.15K 1% 1/8wt	BB-37
R37	7.15K 1% 1/8wt	BB-24
R38	15K 1% 1/8wt	BB-11
R39	4.7K	U-23(U-64)
R40	390	U-16(U-57)
R-41	4.7K	U-33(U-54)
R42	390	U-26(U-47)
R43	4.7K	U-43(U-44)
R44	390	U-36(U-37)
R45	4.7K	U-53(U-34)
R46	390	U-46(U-27)
R47	4.7K	U-63(U-24)
R48	390	U-56(U-17)
R49	4.7K	K-63
R50	390	K-56
R51	4.7K	K-53
R52	390	K-46
R53	4.7K	K-43
R54	390	K-36
R55	4.7K	K-33
R56	390	K-26
R57	4.7K	K-23
R58	390	K-16
R59	4.7K	K-13
R60	390	K-06
R61	4.7K	H-63
R62	390	H-56
R63	4.7K	H-53
R64	390	H-46
R65	4.7K	H-43
R66	390	H-36
R67	4.7K	H-33
R68	390	H-26

SEE ALSO

PART NO.	VALUE / TYPE	LOCATION
R69	4.7K	H-23
R70	390	H-16
R71	4.7K	H-13
R72	390	H-Ø6
D1	4484	U-17 (U-58)
D2		U-27 (U-48)
D3		U-37 (U-38)
D4		U-47 (U-28)
D5		U-57 (U-18)
D6		K-57
D7		K-47
D8		K-37
D9		K-27
D10		K-17
D11		K-Ø7
D12		H-57
D13		H-47
D14		H-37
D15		H-27
D16		H-17
D17		H-07
C1	10µf 25V TANT	NN-64
C2	.1µf 200V disc	NN-62
C3	39pf 200V disc	BB-35
C4	39pf 200V disc	BB-22
C5	100pf 200V disc	BB-9
C23	10µf 25V TANT	DD-64
C24	.1µf 200V disc	DD-62

SEE NOTE

PART NO.	VALUE / TYPE	LOCATION
bypass	.1µf 200V	LL-11
		LL-35
		JJ-25
		JJ-41
		FF-25
		FF-41
		BB-8
		BB-34
		BB-56
		Z-17
		Z-36
		W-23
		W-47
		U-24
		U-34
		U-44
		U-54
		U-64
		M-16
		M-32
		M-48
		K-14
		K-24
		K-34
		K-44
		K-54
		K-64
		H-14
		H-24
		H-34
		H-44
		H-54
		H-64
		DD-17
		DD-35

PART NO.	VALUE / TYPE	LOCATION
bypass	10uf 25V TANT	LL-0
		LL-65
		JJ-0
		JJ-65
		FF-0
		FF-65
		DD-0
		DD-65
		BB-0
		BB-65
		Z-0
		Z-65
		W-0
		W-65
		U-0
		U-65
		P-0
		M-0
		M-65
		K-0
		K-65
		H-0
		H-65
		E-0
J1	50 pin WW Header	NN-57
J2	INSTALLED	NN-26 *
J3	60 pin WW Header	A-29
J4	60 pin WW Header	F-64

PART NO.	VALUE / TYPE	LOCATION

START: To: PAGE #7

GROUND BUS

J1 (33, 35, 37, 39, 41, 43, 45, 47, 49)

J2 (ODD)

E1-1, E1-10, LL-11, E2-1, E2-10, E3-10, LL-35, E4-10, E9-19, E9-1, E9-10

E5-8, E6-8, JJ-25, E7-8, JJ-41, E8-8, JJ-64

E10-12, E10-8, E11-12, E11-8, FF-25, E12-12, E12-8, E13-12, E13-8, E19-7

E14-7, E15-7, DD-17, E16-7, E17-12, E17-7, DD-35, E20-7, E18-14, E18-11

E18-8, E18-5

E26-7, BB-8, E25-1, E25-8, E24-15, E24-8, BB-34, E23-1, E23-8

E22-7, BB-56, E21-7

E27-7, E28-7, Z-17, E29-8, E64-7, Z-36, E63-7

E31-10, E32-10, W-23, E33-10, E34-17, E34-15, E34-13, E34-11

E34-10, W-47, E35-10

START: To: PAGE #8

GROUND BUS : CONTINUED

E36-5, U-24, E37-5, U-34, E38-5, U-44, E39-5, U-54

E40-5, U-64

E61-7

E60-7, E59-7, M-16, E58-7, E57-7, M-32, E56-7, E55-7, M-48,

E54-7, E53-7

E46-5, K-14, E45-5, K-24, E44-5, K-34, E43-5, K-44, E42-5,

K-54, E41-5, K-64

E52-5, H-14, E51-5, H-24, E50-5, H-34, E49-5, H-44, E48-5, H-54

E47-5, H-64

E62-1, E62-10

START:	TO:	PAGE #9
	+5 BUS	
	E1-20, MM-11, E2-20, E3-20, MM-35, E4-20, E9-20	
	E5-16, KK-10, KK-11, KK-12, KK-13, E6-16, KK-25, KK-26, KK-27, KK-28, KK-29,	
	E7-16, KK-41, KK-42, KK-43, KK-44, KK-45, E8-16, KK-57, KK-58, KK-59	
	KK-60, KK-61	
	NN-64, NN-62	
	E10-16, E10-4, HH-10, HH-11, HH-12, HH-13, E11-16, E11-4, HH-25, HH-26	
	HH-27, HH-28, HH-29, E12-16, E12-4, HH-41, HH-42, HH-43, HH-44,	
	HH-45, E13-16, E13-4, E19-14	
	E14-14, E15-14, EE-17, E16-14, E17-14, EE-35, E20-14, E18-16,	
	EE-56, EE-57, EE-58, EE-59, EE-62, EE-64	
	E26-2, E26-4, E26-14, E26-12, E26-10, CC-8, CC-11, E25-16, E25-10	
	CC-24, E24-16, CC-34, CC-37, E23-16, E22-4, E22-14, E22-12,	
	E22-10, CC-56, E21-14	
	E27-14, E28-4, E28-14, AA-17, E29-16, E64-14, AA-36, E63-14	
	E31-20, E32-20, Y-23, E33-20, E34-20, Y-47, E35-20	

START:	TO:	PAGE #10
	+5 BUS: CONTINUED	
	E36-8, E36-7, V-23, V-24, E37-8, E37-7, V-33, V-34, E38-8, E38-7	
	V-43, V-44, E39-8, E39-7, V-53, V-54, E40-8, E40-7, V-63, V-64	
	E61-14	
	E60-14, E59-14, N-16, E58-14, E57-14, N-32, E56-14, E55-14,	
	N-48, E54-14, E53-14	
	E46-8, E46-7, L-13, L-14, E45-8, E45-7, L-23, L-24, E44-8, E44-7,	
	L-33, L-34, E43-8, E43-7, L-43, L-44, E42-8, E42-7, L-53, L-54	
	E41-8, E41-7, L-63, L-64	
	E52-8, E52-7, J-13, J-14, E51-8, E51-7, J-23, J-24, E50-8, E50-7, J-33,	
	J-34, E49-8, E49-7, J-43, J-44, E48-8, E48-7, J-53, J-54,	
	E47-8, E47-7, J-63, J-64	
	E62-20	

R-E15

EDS-ESS I/F

PAGE # 11/30

START:	TO:
R00 E15-4	E8-13 , E2-3
R01 E15-2	E8-10 , E2-4
R02 E15-1	E8-6 , E2-7
R03 E15-13	E8-3 , E2-8
R04 E15-12	E7-13 , E2-13
R05 E15-11	E7-10 , E2-14
R06 E15-10	E7-6 , E2-17
R07 E15-9	E7-3 , E2-18
R08 E14-2	E6-13 , E1-3
R09 E14-1	E6-10 , E1-4
R10 E14-13	E6-6 , E1-7
R11 E14-12	E6-3 , E1-8
R12 E14-11	E5-13 , E1-13
R13 E14-10	E5-10 , E1-14
R14 E14-9	E5-6 , E1-17
R15 E14-8	E5-3 , E1-18

DATA

Sheet 3 5, 6

PAGE # 12

START:	To:
E4-2	E2-2, E57(1,2,3,4), E62-3
E4-4	E2-5, E57(10,11,12,13), E62-4
E4-6	E2-6, E58(1,2,3,4), E62-7
E4-8	E2-9, E58(10,11,12,13), E62-8
E4-11	E2-12, E59(1,2,3,4), E62-13
E4-13	E2-15, E59(10,11,12,13), E62-14
E4-15	E2-16, E60(10,11,12,13), E62-17
E4-17	E2-19, E60(1,2,3,4), E62-18
E3-2	E1-2, E61(10,11,12,13).
E3-4	E1-5, E61(1,2,3,4)
E3-6	E1-6,
E3-8	E1-9,
E3-11	E1-12,
E3-13	E1-15
E3-15	E1-16,
E3-17	E1-19,

LATCHED ADDR BUS

START:	To:	PAGE# 13
AA Ø0 E62-2	E53(1,2,3,4), E31-2	Sht. 5
AA Ø1 E62-5	E53(10,11,12,13), E31-4	
AA Ø2 E62-6	E54(1,2,3,4), E31-6	
AA Ø3 E62-9	E54(10,11,12,13), E31-8	
AA Ø4 E62-12	E55(1,2,3,4), E31-11	
AA Ø5 E62-15	E55(10,11,12,13), E31-13	
AA Ø6 E62-16	E56(10,11,12,13), E31-15	
AA Ø7 E62-19	E56(1,2,3,4), E31-17	

D-OUT BUS

2.5.7

PAGE # 14

START:	To:
D-OUT-00 E4-18	E8-14, E31-18, E32-18, E35-18
D-OUT-01 E4-16	E8-11, E31-16, E32-16, E35-16
D-OUT-02 E4-14	E8-5, E31-14, E32-14, E35-14
D-OUT-03 E4-12	E8-2, E31-12, E32-12, E35-12
D-OUT-04 E4-9	E7-14, E31-9, E32-9, E35-9
D-OUT-05 E4-7	E7-11, E31-7, E32-7, E35-7
D-OUT-06 E4-5	E7-5, E31-5, E32-5, E35-5
D-OUT-07 E4-3	E7-2, E31-3, E32-3, E35-3
D-OUT-08 E3-18	E6-14, E33-18, E34-18
D-OUT-09 E3-16	E6-11, E33-16, E34-16
D-OUT-10 E3-14	E6-5, E33-14, E34-14
D-OUT-11 E3-12	E6-2, E33-12, E34-12
D-OUT-12 E3-9	E5-14, E33-9, E34-9
D-OUT-13 E3-7	E5-11, E33-7, E34-7
D-OUT-14 E3-5	E5-5, E33-5, E34-5
D-OUT-15 E3-3	E5-2, E33-3, E34-3

A/D DATA IN

START:	TO:
00 E41-6	R49-K, E35-2
01 E42-6	R51-K, E35-4
02 E43-6	R53-K, E35-6
03 E44-6	R55-K, E35-8
04 E45-6	R57-K, E35-11
05 E46-6	R59-K, E35-13
06 E47-6	R61-H, E35-15
07 E48-6	R63-H, E35-17
08 E49-6	R65-H, E34-2
09 E50-6	R67-H, E34-4
10 E51-6	R69-H, E34-6
11 E52-6	R71-H, E34-8

Control / UB (J2)

START:	TO: PAGE # 16
R1-JJ	E5-1, J2/40
R2-JJ	E5-4, J2/38
R3-JJ	E5-12 J2/36
R4-JJ	E5-15 J2/34
R5-JJ.	E6-1, J2/32
R6-JJ	E6-4 J2/30
R7-JJ	E6-12, J2/28
R8-JJ	E6-15, J2/26
R9-JJ	E7-1, J2/24
R10-JJ	E7-4 J2/22
R11-JJ	E7-12 J2/20
R12-JJ	E7-15, J2/18
R13-JJ	E8-1, J2/16
R14-JJ	E8-4, J2/14
R15-JJ	E8-12, J2/12
R16-JJ	E8-15, J2/10
R32-DD	E18-1, J2/8.
R33-DD	E18-4 J2/6
R34-DD	E18-12, J2/4
R35-DD	E18-15, J2/2
C24-DD	C23-DD, J2/23
NN-31	J2/1 thru 39 (ODD)
	ERD
	COL/PIN

A/D & D/A ADDR.

START:	TO:	
E56-5	J4/12, J3/22 ✓ —	A07
E56-6	J4/11, J3/21 ✓ —	
E56-9	J4/14, J3/20 ✓ —	A06
E56-8	J4/13, J3/19 ✓ —	
E55-9	J4/16, J3/18 ✓ —	A05
E55-8	J4/15, J3/17 ✓ —	
E55-5	J4/18, J3/16 ✓ —	A04
E55-6	J4/17, J3/15 ✓ —	
E54-9	J4/4, J3/24 ✓ —	A03
E54-8	J4/3, J3/23 ✓ —	
E54-5	J4/6, J3/30 ✓ —	A02
E54-6	J4/5, J3/29 ✓ —	
E52-9	J4/8, J3/28 ✓ —	A01
E53-8	J4/7, J3/27 ✓ —	
E53-5	J4/10, J3/26 ✓ —	A00
E53-6	J4/9, J3/25 ✓ —	

D/A DATA

START:	TO:	
E57-6	J3/59 ✓	DA00
E57-5	J3/60 ✓	
E57-8	J3/57 ✓	DA01
E57-9	J3/58 ✓	
E58-6	J3/55 ✓	DA02
E58-5	J3/56 ✓	
E58-8	J3/53 ✓	DA03
E58-9	J3/54 ✓	
E59-6	J3/51 ✓	DA04
E59-5	J3/52 ✓	
E59-8	J3/49 ✓	DA05
E59-9	J3/50 ✓	
E60-8	J3/47 ✓	DA06
E60-9	J3/48 ✓	
E60-6	J3/45 ✓	DA07
E60-5	J3/46 ✓	
E61-8	J3/43 ✓	DA08
E61-9	J3/44 ✓	
E61-6	J3/41 ✓	DA09
E61-5	J3/42 ✓	

ANALOG DATA WORD IN

START:	TO:	
D6-L	E41-3, J4/59	
R50-L	J4/60	HAD ØØ
R50-K	D6-K, E41-2	
D7-L	E42-3, J4/57	
R52-L	J4/58	HAD Ø1
R52-K	D7-K, E42-2	
D8-L	E43-3, J4/51	
R54-L	J4/52	HAD Ø2
R54-K	D8-K, E43-2	
D9-L	E44-3, J4/49	
R56-L	J4/50	HAD Ø3
R56-K	D9-K, E44-2	
D10-L	E45-3, J4/43	
R58-L	J4/44	HAD Ø4
R58-K	D10-K, E45-2	
D11-L	E46-3, J4/41	
R60-L	J4/42	HAD Ø5
R60-K	D11-K, E46-2	
D12-J	E47-3, J4/37	
R62-J	J4/38	HAD Ø6
R62-H	D12-H, E47-2	
D13-J	E48-3, J4/39	
R64-J	J4/40	HAD Ø7
R64-H	D13-H, E48-2	
D14-J	E49-3, J4/45	
R66-J	J4/46	HAD Ø8
R66-H	D14-H, E49-2	

ANALOG DATA WORD IN (Cont'd)

START:	TO:		PAGE # 20
D15-J	E50-3, J4/47		
R68-J	J4/48	HAD Ø9	
R68-H	D15-H, E50-2		
D16-J	E51-3, J4/53		
R70-J	J4/54	HAD 1Ø	
R70-H	D16-H, E51-2		
D17-J	E52-3, J4/55		
R72-J	J4/56	HAD 11	
R72-H	D17-H, E52-2		

A/D & D/A I/F CONTROL

START:	To:		PAGE # 21
D5-V	E40-3, J4/31		
R48-V	J4/30	A/D HDP	
R48-U	D5-U, E40-2		
D4-V	E39-3, J3/1		
R46-V	J3/2	D/A HDP	
R46-U	D4-U, E39-2		
D3-V	E38-3, J3/3		
R44-V	J3/4	HOA (D/A)	
R44-U	D3-U, E38-2		
D2-V	E37-3, J4/34		
R42-V	J4/33	HIDR	
R42-U	D2-U, E37-2		
D1-V	E36-3, J4/36		
R40-V	J4/35	HEFA	
R40-U	D1-U, E36-2		
E63-8	J3/13	HODR (D/A)	
E63-9	J3/14		
E63-6	J4/20	HEF (A/D)	
E63-5	J4/19		
E64-8	J4/22	HLFW	
E64-9	J4/21		
E64-6	J4/26	HIA	
E64-5	J4/25		

CONTROL LOGIC

START:	TO:	PAGE # 22
	END CYCLE L	
E13-3	E26-3 ✓	Sht 1,4
	UB GO PULSE L	Sht 1,3
E13-5	E17-10 ✓	
	UB STROBE H	Sht 1,4
E12-3	E16-1 ✓	
	UB RD USER REG. L	Sht 1,2
E12-5	E29-12 ✓	
	UB WR USER REG L	Sht 1,4
E12-11	E19-4, E27-11, E27-12 ✓	
	CBL DIR UB TO USER H	Sht. 1,2
E12-13	E18-7, E18-9, E16-12, E16-9, E8-7, E8-9, E7-7, E7-9	
	E6-7, E6-9, E5-7, E5-9 ✓	
	WD CNTR OVF H	Sht 1,4
E11-5	E19-9, E19-10, E28-12, E27-8, E27-9	
	WD CNTR OVF L	Sht. 1,3
E19-8	E31-3 ✓	
	LD OUT REG H	Sht. 1,2
E19-6	E1-11, E2-11 ✓	

CONTROL LOGIC Cont'd

START:	TO:	PAGE# 23
	LD DST REG L	[illegible] 1,2,3
E11-11	E19-5, E17-3, E22-3 ✓	
	FCN 2 EN PAR ERR H	[illegible] 1,2
E10-5	E17-1 ✓	
	FCN 1 SEL O/A L	[illegible] 1,3,4
E10-11	E20-5, E21-3, E16-5 ✓	
	RESET H	[illegible] 1,4
E10-3	E19-13, E19-12, E27-6 ✓	
	RESET L	[illegible] 1,3,4
E19-11	E17-13, E28-10 ✓	
	T SYNCH H	[illegible] 1,3
E9-17	E24-7 ✓	
	CABLE PARITY H	[illegible] 1,2
E9-8	E17-5	

UB CONTROL (1)

Sheet 1

START:	To:	PAGE # 24
R30-KK	R31-KK, L1-MM, C1-PP, C2-PP, J1/17	
	J1/15, J1/13, J1/11, J1/9, J1/7, J1/5, J1/3, J1/1	
	J1/19, J1/21, J1/23, J1/25, J1/27, J1/29	
C2-NN	C1-NN, L2-LL, R29-KK, R17 thru R28 (HH)	
R30-JJ	R29-JJ, E13-1, E13-7, E12-2, E12-6, E12-10, E12-15, E11-2	
	E11-6, E11-9, E11-14, E10-2, E10-6, E10-10, E10-14	
E13-2	J1/28	
E13-6	J1/26	
E10-15	R17-FF, J1/2	
E10-9	R18-FF, J1/4	
E10-7	R19-FF, J1/6	
E10-1	R20-FF, J1/8	
E11-15	R21-FF, J1/10	
E11-13	R22-FF, J1/12	
E11-7	R23-FF, J1/14	
E11-1	R24-FF, J1/16	
E12-14	R25-FF, J1/18	
E12-9	R26-FF, J1/20	
E12-7	R27-FF, J1/22	
E13-1	R28-FF, J1/24	

UB CONTROL (3):

Sheet 1

START:	To:	PAGE # 25
RR-31	J1/33, J1/35, J1/37, J1/39, J1/41, J1/43, J1/45, J1/47, J1/49	
	GRD BUS	
	COLUMN/PIN	
E9-3	J1/50 ✓	
E9-12	J1/32 ✓	CABLE Parity ERROR LINE TO UDIF, NOT INSTALLED
L1-LL	L1-MM ✓	intentional shorting of components
L2-LL	L2-MM ✓	

START:	TO:	PAGE # 26
	EVEN PARITY RCV H	
E18-3	E16-13	
E18-6	E29-15	
E18-10	E29-14	
E18-13	E29-13	
E18-2	E16-10, E15-6	
E16-8	E17-2	
E14-6	E15-8	
E29-3	E21-1	
E17-6	E17-4	
E29-2	E3-19, E3-1, E4-19, E4-1	
	RD A/D DATA H	
E21-2	E20-8	
	RD ADDR L	
E29-1	E21-1, E31-19	
	RD STATUS L	
E29-4	E33-19, E33-1, E32-19, E32-1	

A/D ADDR LD

START:	To:	PAGE # 27
	UB WR USER REG L	Blk 4
E27-13	E16-2	
E16-3	E27-2, E27-3, E26-11	3
E27-4	E26-13	Blk 4
E27-10	E28-2	Blk 4
E28-3	E28-11, E25-12	Blk 4
	HEF H	Blk. 4, 5
E26-9	E32-11, E63-(1,2,3,4)	
	HEFA H	Blk. 4, 5
R39-U	E36-6, E32-13, E27-5	
	HIOR H	Blk. 4, 5
R41-U	E32-15, E28-1, E28-13, E25-2, E37-6	
	A/D CY RQ H	Blk. 4, 3
E25-13	E24-5	

A/D addr LD
Sht 1 Cont'd

Sht 6

PAGE # 28

START:	To:	
	LAST WD H.	Sh. 6 5
E28-9	E33-2 ✓	
	HLWF H	Sh. 4, 5
E16-6.	E33-4, E64(10, 11, 12, 13) ✓	
	HIA H	Sh. 4, 5
E28-5	E32-17, E64-(1,2,3,4) ✓	
C5-BB	R38-BB, E25-7 ✓	Sh. 6
C5-CC	E25-6 ✓	
C4-BB	R37-BB, E25-15 ✓	Sh 6
C4-CC	E25-14 ✓	
	LD A/D ADDR H	Sh. 4 3.
E27-1	E24-2 ✓	
	A/D DMA EN H	Sh 4, 3
E20-13	E20-9, E25-3, E25-11, E26-1	

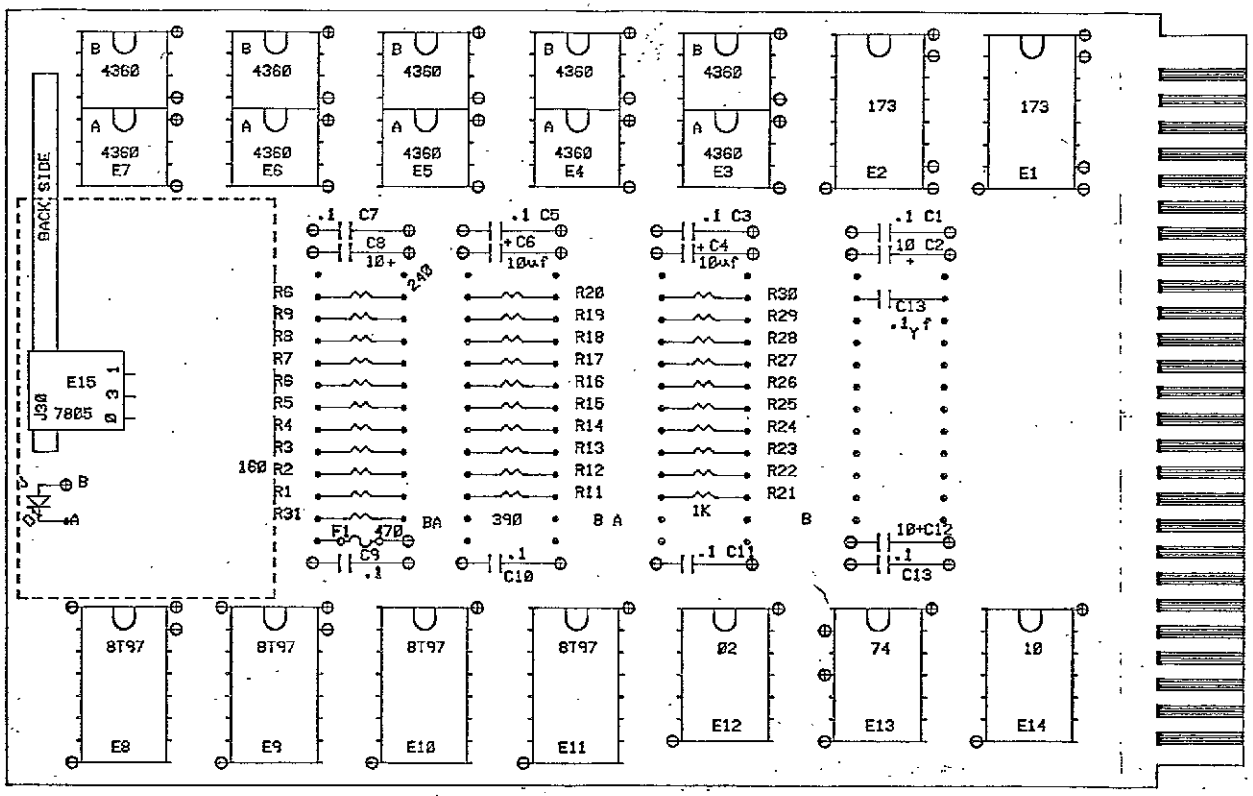
Cont'd

START:	TO:	PAGE #27
	A/D DTA TO CABLE L	24. 3, 7
E20-10	E35-19, E35-1, E34-1, E34-19 ✓	
	DATA RDY H	22. 3
E22-2	E22-6, E22-11 ✓	
	D/A DMA EN H	8K. 3
E20-4	E22-1, E23-3 ✓	
E21-6	E22-13, E19-2 ✓	8K. 5
E20-11	E20-6, E17-8 ✓	8K. 3
E20-12	E21-4, E24-1 ✓	8K. 5
	DMA DATA RDY H	
E20-2	E22-9, E63-(10,11,12,13), E32-4 ✓	24. 3 5
	HOA H	
R43-U	E38-6, E21-5, E32-6 ✓	8D 3,5
	DMA EN H	24 3,5
E17-9	E32-8 ✓	
	LD ADDR H	8K. 3,5
E24-4	E62-11 ✓	
	ADDR RDY H	24. 3,5
E22-5	E23-2, E24-3, E32-2 ✓	

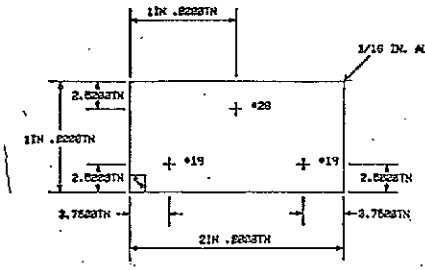
START:	TO:	PAGE# 30
R47-U	E40-6, E33-6 ✓	
R45-U	E39-6, E33-8 ✓	
E19-3	E24-6 ✓ D/A CYC RQT H	
C3-BB	R36-BB, E23-15 ✓	
C3-CC	E23-14 ✓	
E23-4	E19-1 ✓	
E20-1	E17-11	
E16-11	E14-4	
E2-H3	E12-13	
E21-12	E21-11 E21-9	
J1-50	J1-48	
REMOVE	E26-5 to E25-10	
"	E28-8 to E16-4	
"	GND from E25-9	
ADD	E26-3 to E25-9	
	E25-10 to VCC	
	E16-4 to E16-5	
	J1-34 to E9-9	
	E9-11 to E19-9	
	D-K2 to D-L2	
	D-M2 to D-N2	
	D-R2 to D-P2	
	D-S2 to D-T2	
	C-F1 to C-B1	

APPENDIX B

SCHEMATICS
AND
WIREWRAP LIST



COMPONENT SIDE



1/16 IN. ALUMINUM

FASTEN HEAT SINK TO 7805
WITH 6X32X1/4 PANHEAD & NUT
USE SILICON GREASE
MOUNT ON BOARD WITH 6X32X1/2 STANDOFFS

FOLDOUT FRAME

2 FOLDOUT FRAME

REV	DATE	ZONE	DESCRIPTION	APPROVAL

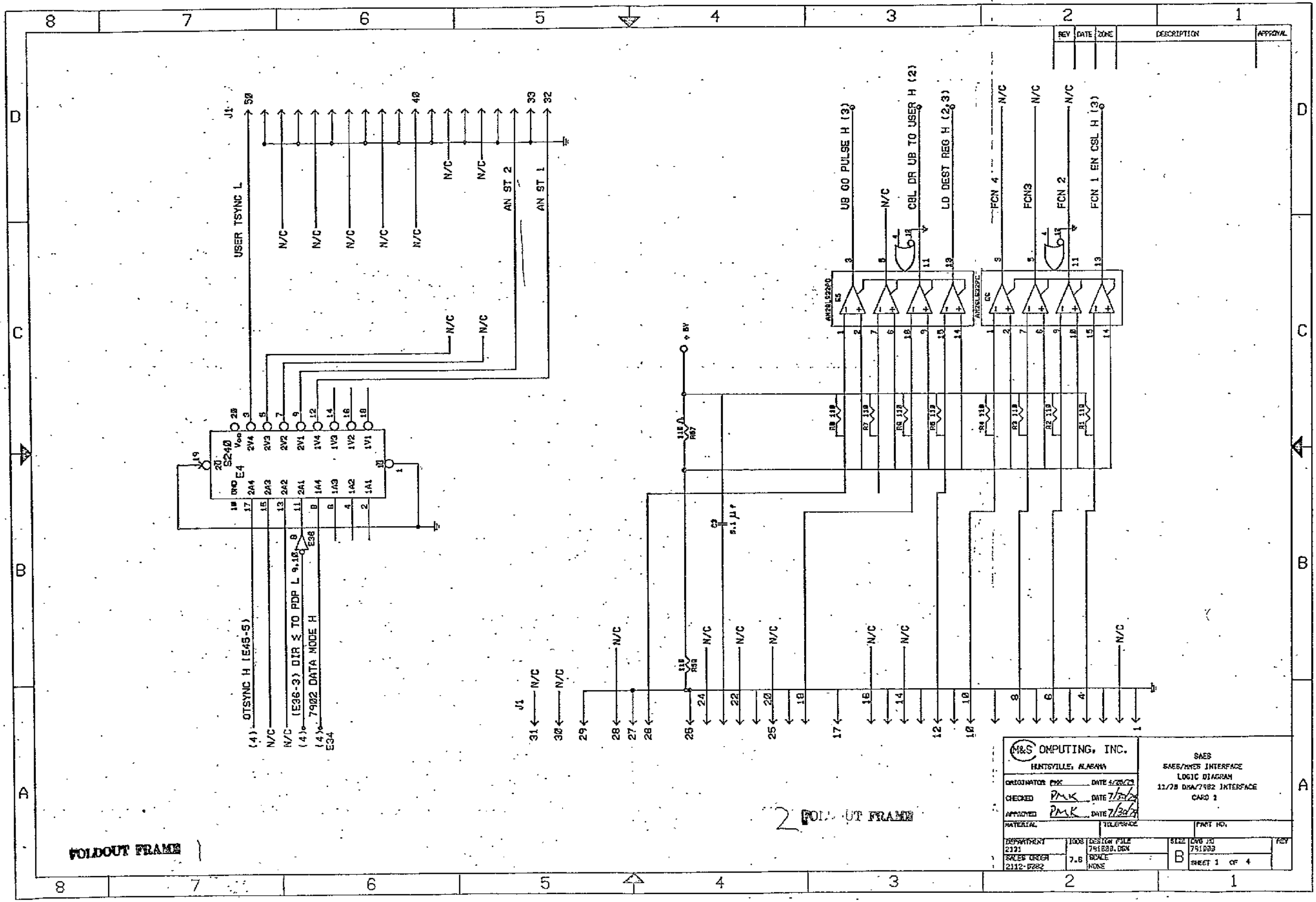
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA

ORIGINATOR PSC DATE
CHECKED DATE
APPROVED DATE

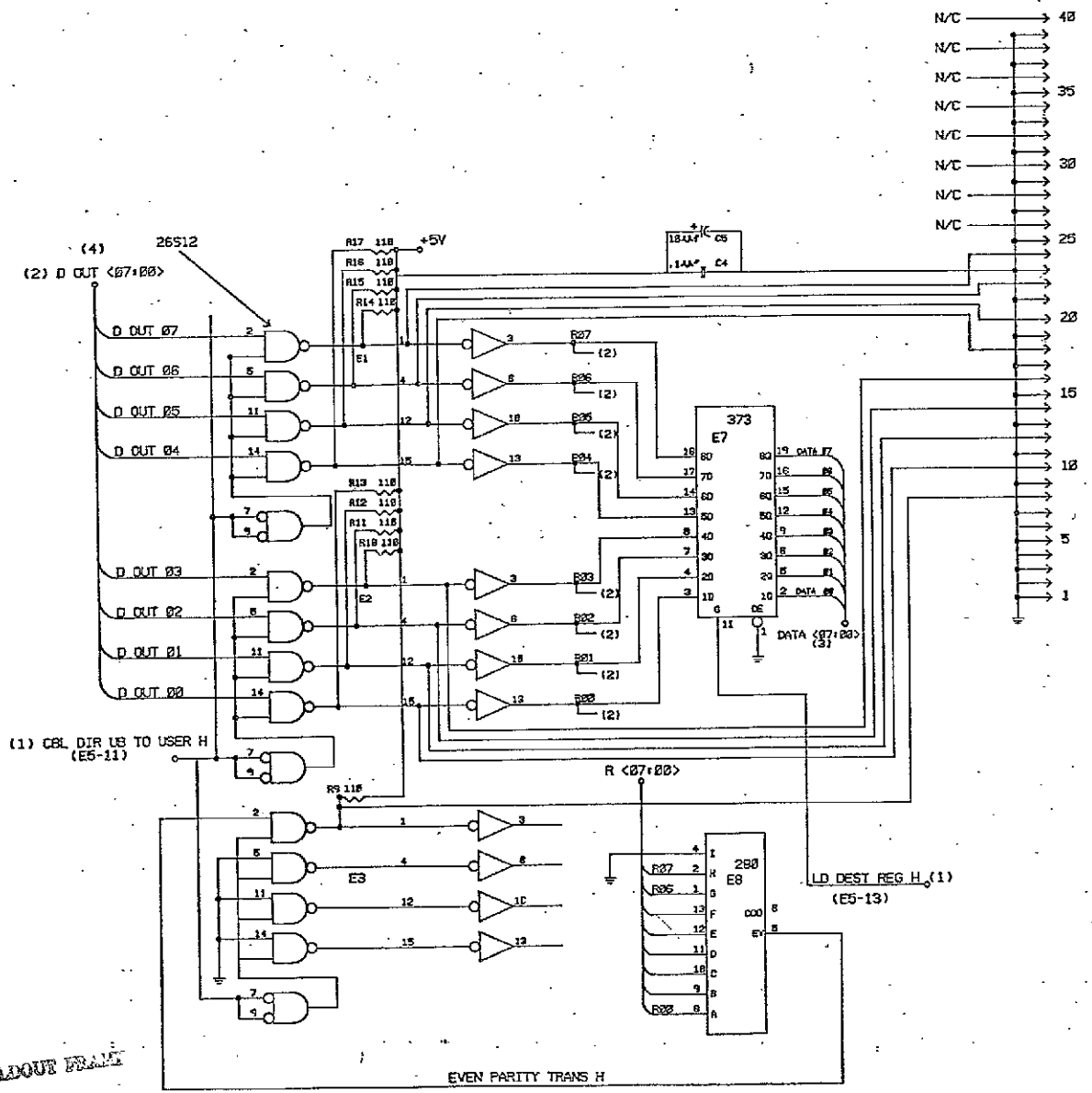
SAES
SAES/MMES INTERFACE
COMPONENT ARRANGEMENT
11/70 DMA/7932 INTERFACE

MATERIAL TOLERANCE PART NO.

DEPARTMENT 2131
SALES ORDER 2112-0382
LOCK DESIGN FILE 791002.DGN
SCALE 1" = 1"
SIZE B DWG NO 791002 REV
SHEET 1 OF 1



J1
USER TSYNC L
N/C
AN ST 2
AN ST 1
S240
E4
E38
DTSYNC H (E45-5)
(E36-3) DIR ≤ TO PDP L
7902 DATA MODE H
E34
+5V
R67
R59
C3
0.1 μf
UB GO PULSE H (3)
CBL DR UB TO USER H (2)
LD DEST REG H (2,3)
FCN 4
FCN3
FCN 2
FCN 1 EN CSL H (3)
E5
E6
AM26LS32PC
R8 110
R7 110
R6 110
R5 110
R4 110
R3 110
R2 110
R1 110
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/MMES INTERFACE
LOGIC DIAGRAM
11/70 DMA/7902 INTERFACE
CARD 2
ORIGINATOR
CHECKED PMK
APPROVED PMK
MATERIAL
TOLERANCE
PART NO.
DEPARTMENT 2131
SALES ORDER 2112-0282
DESIGN FILE 791880.DGN
SCALE NONE
SIZE B
DWG NO 791880
SHEET 1 OF 4
REV
DATE
ZONE
DESCRIPTION
APPROVAL
FOLDOUT FRAME

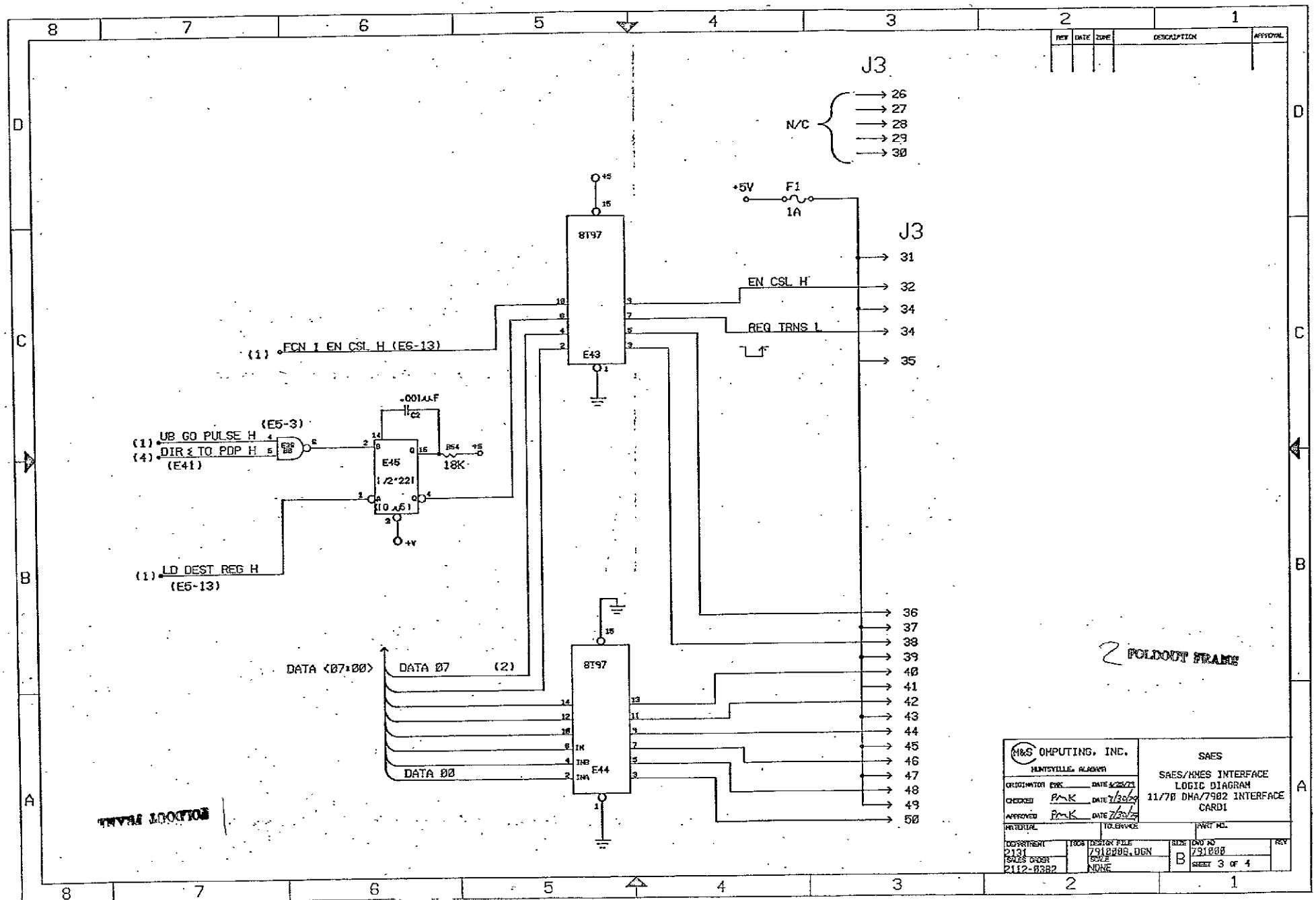


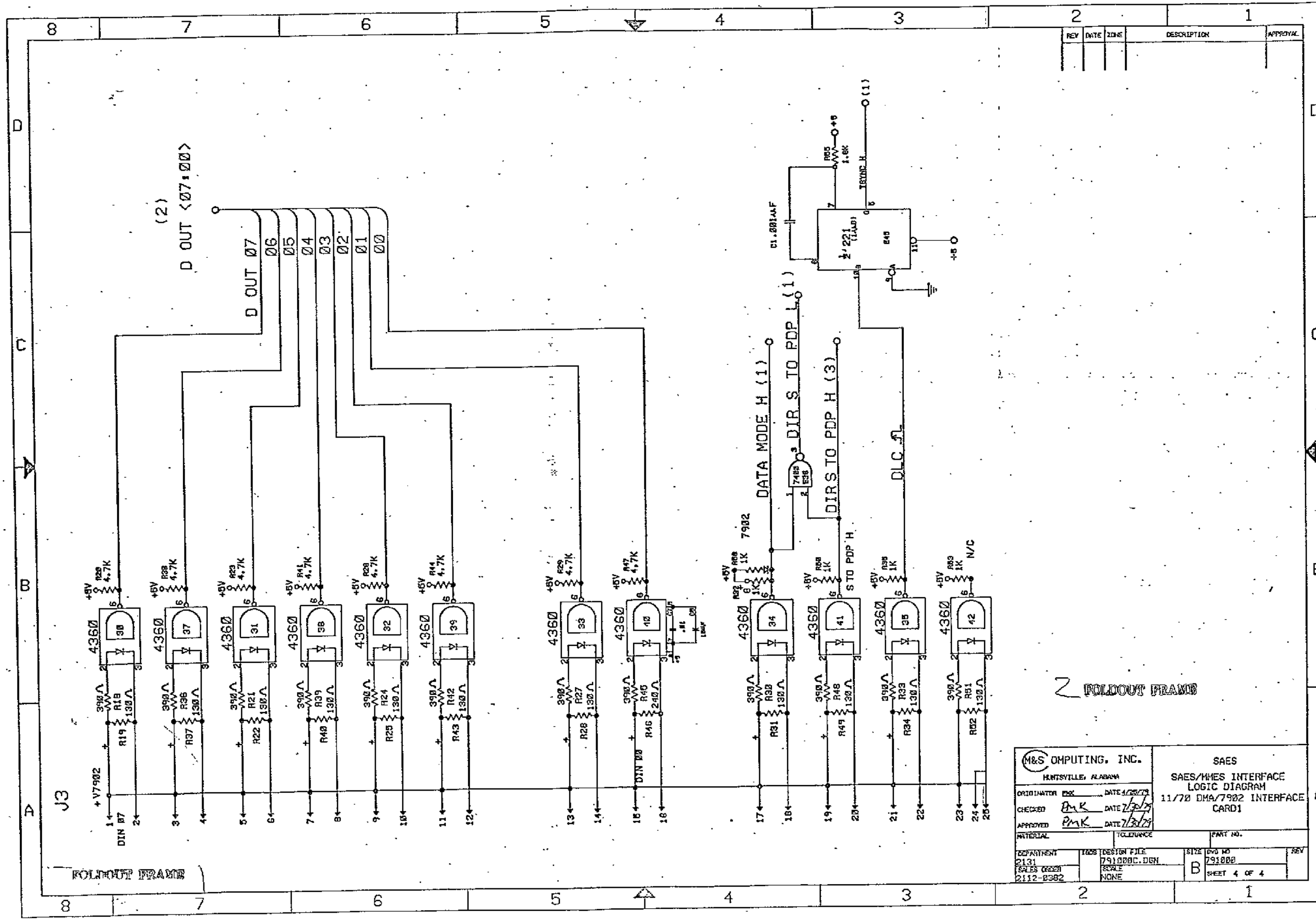
REV	DATE	ZONE	DESCRIPTION	APPROVAL

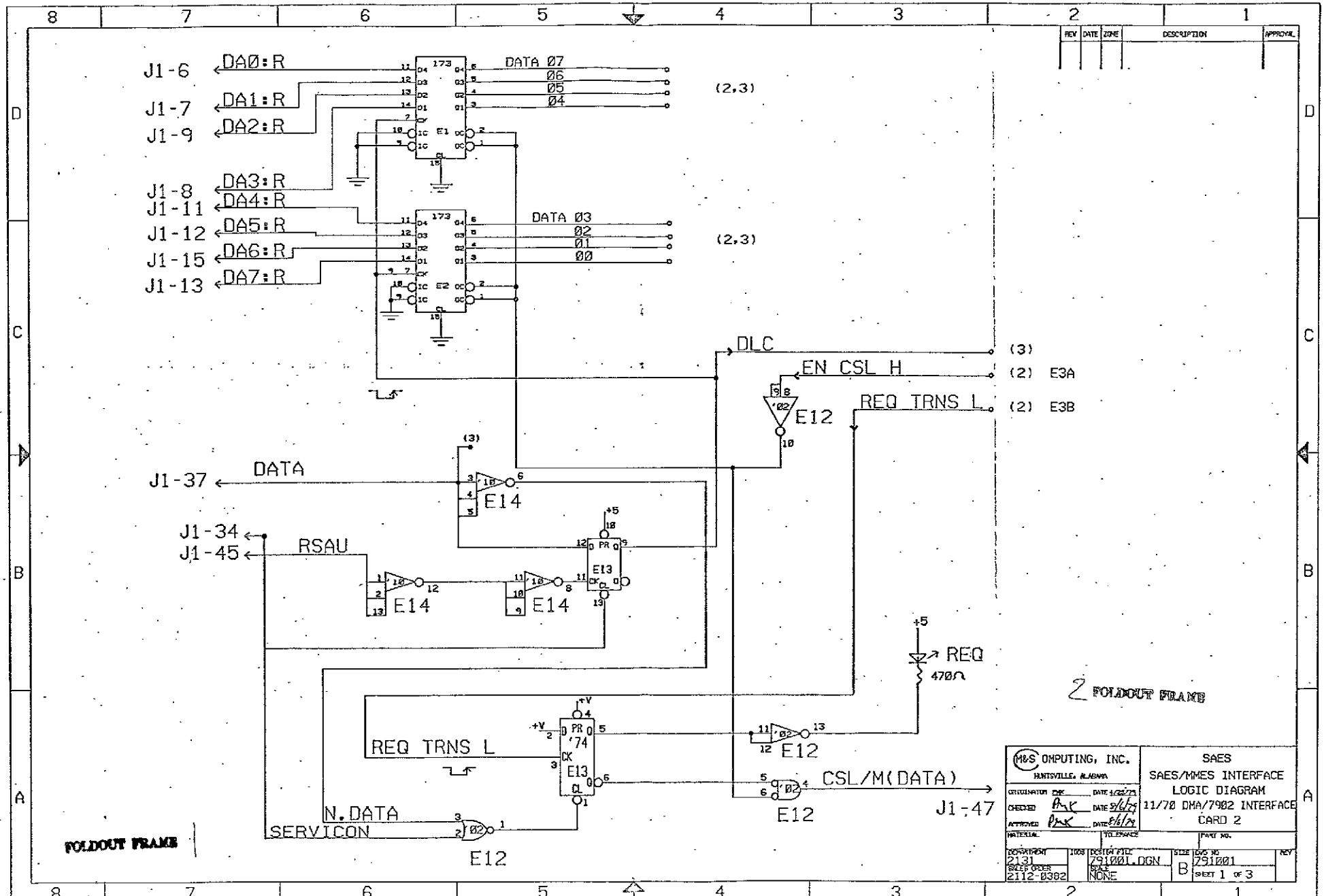
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA

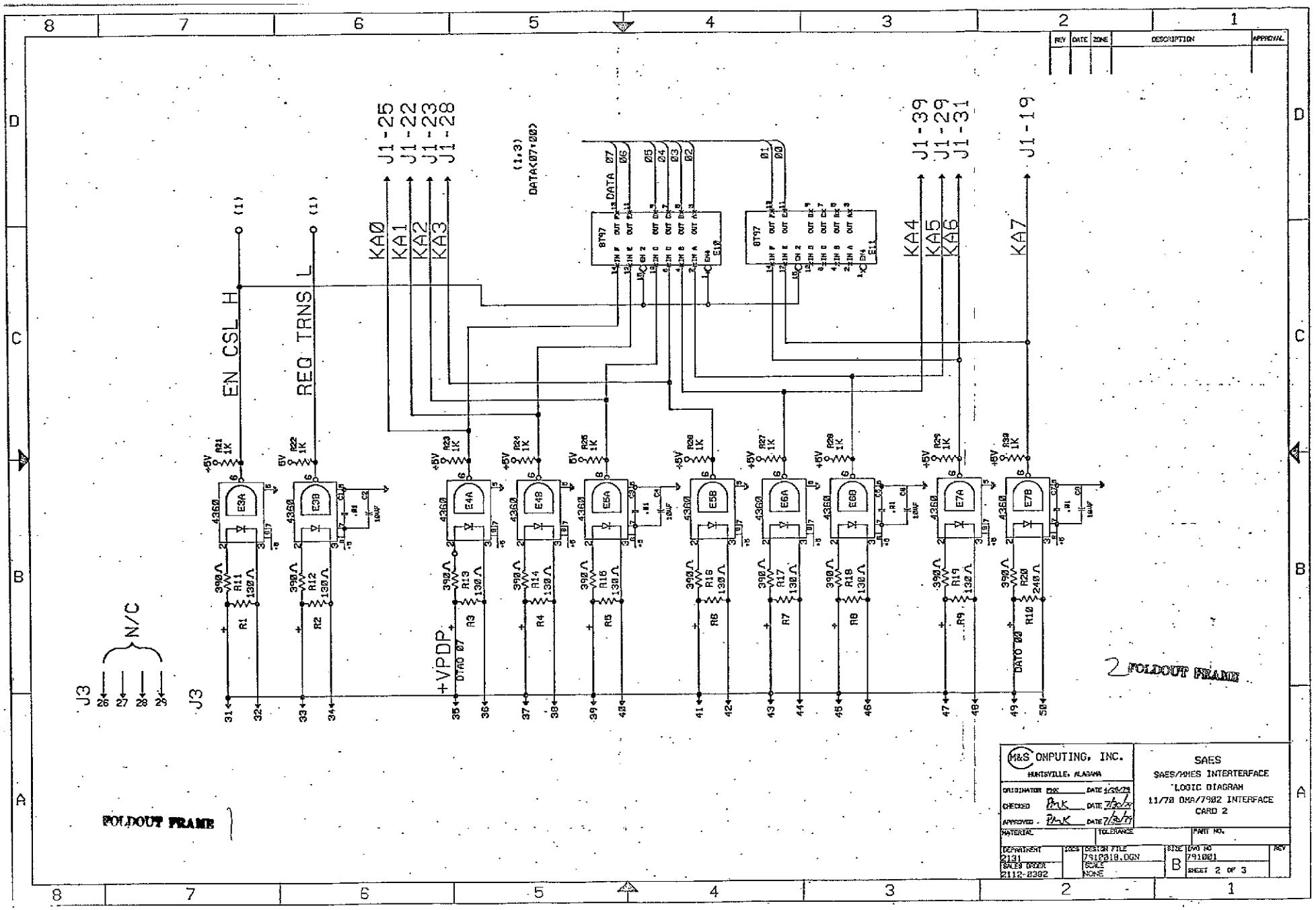
SAES
SAES/MAES INTERFACE
LOGIC DIAGRAM
11/70 DMA/7902 INTERFACE
CARD1

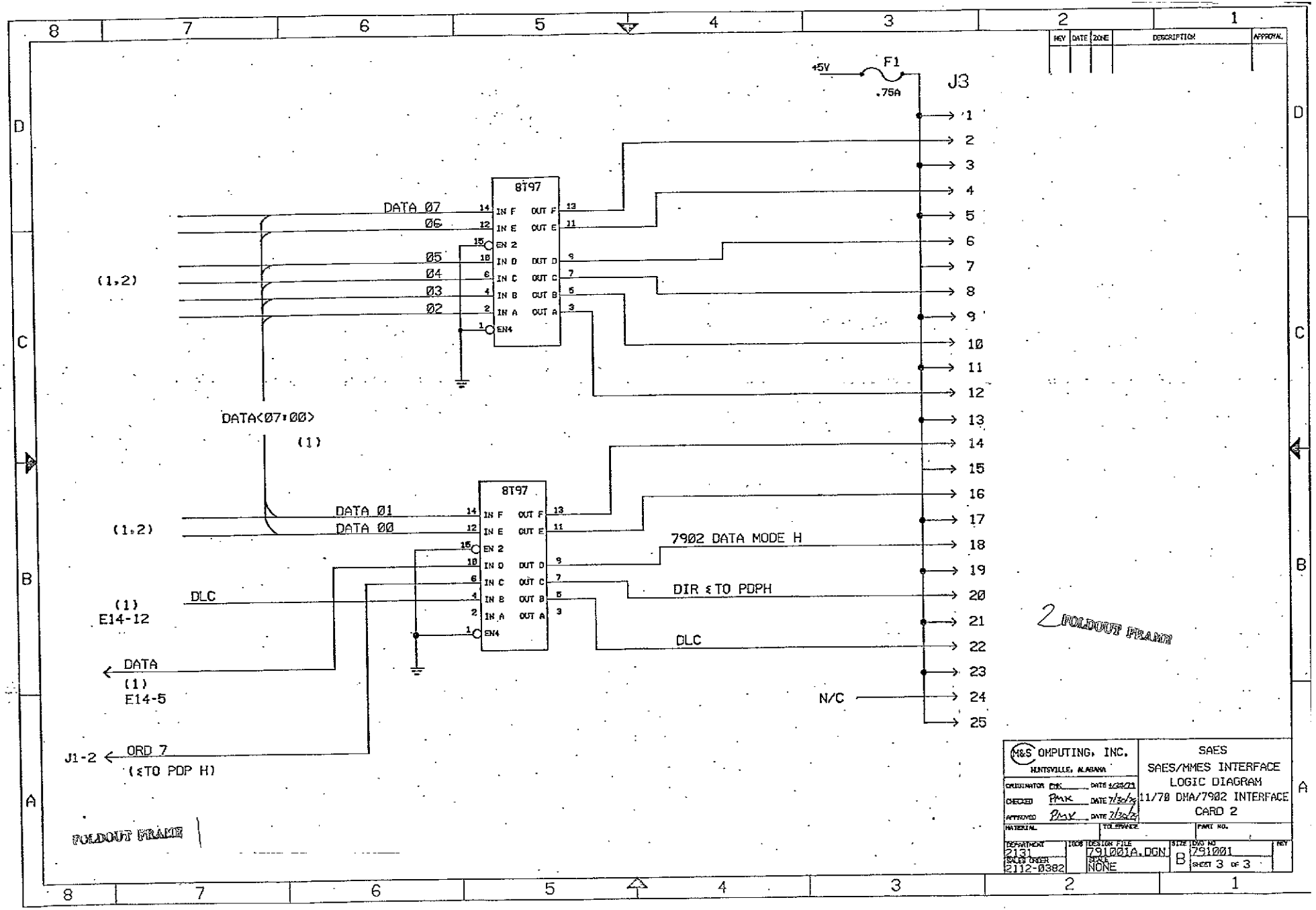
DESIGNATOR PMK	DATE 1/25/79		
CHECKED PMK	DATE 7/25/79		
APPROVED PMK	DATE 7/25/79		
MATERIAL	TOLERANCE	PART NO.	
DEPARTMENT 2131	TOOL	DESIGN FILE 7912002A.DGN	SIZE B
DRAWN BY 2112-0382		SCALE NONE	DWG NO 791202 SHEET 2 OF 4


J3
N/C
26
27
28
29
30
+5V
F1
1A
J3
31
EN CSL H
32
34
REQ TRNS L
34
35
8T97
E43
(1) FCN 1 EN CSL H (E6-13)
.001uF
C2
(E5-3)
(1) UB GO PULSE H
(4) DIR ≤ TO PDP H
(E41)
E45
/2'221
854
18K
+V
(1) LD DEST REG H
(E5-13)
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
DATA <07:00>
DATA 07
(2)
8T97
E44
DATA 00
2 FOLDOUT FRAMES
FOLDOUT FRAME
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/KNES INTERFACE
LOGIC DIAGRAM
11/70 DNA/7902 INTERFACE
CARD1
ORIGINATOR ERK DATE 4/25/79
CHECKED PMK DATE 7/30/79
APPROVED PMK DATE 7/30/79
MATERIAL
TOLERANCE
PART NO.
DEPARTMENT 2121
SALES ORDER 2112-8382
TOOL
DESIGN FILE 7918000.DGN
SCALE NONE
SIZE B
DWG NO 791800
SHEET 3 OF 4
REV
REV DATE ZONE DESCRIPTION APPROVAL


(2) D OUT <07:00>
D OUT 07
06
05
04
03
02
01
00
DATA MODE H (1)
DIR S TO PDP L (1)
DIR S TO PDP H (3)
DLC
S TO PDP H
7902
N/C
221
C1 .001uF
R55 1.6K
4360
J3
+V7902
DIN 07
DIN 00
FOLDOUT FRAME
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/MMES INTERFACE
LOGIC DIAGRAM
11/70 DMA/7902 INTERFACE
CARD1
ORIGINATOR
CHECKED
APPROVED
MATERIAL
TOLERANCE
PART NO.
DEPARTMENT
2131
SALES ORDER
2112-0382
DESIGN FILE
791000C.DGN
SCALE
NONE
SIZE
B
DWG NO
791000
SHEET 4 OF 4
REV
DATE
ZONE
DESCRIPTION
APPROVAL


J1-6 DA0:R
J1-7 DA1:R
J1-9 DA2:R
J1-8 DA3:R
J1-11 DA4:R
J1-12 DA5:R
J1-15 DA6:R
J1-13 DA7:R
DATA Ø7
Ø6
Ø5
Ø4
DATA Ø3
Ø2
Ø1
Ø0
(2,3)
(2,3)
E1
E2
DLC
(3)
EN CSL H
(2) E3A
REQ TRNS L
(2) E3B
E12
J1-37 DATA
E14
J1-34
J1-45 RSAU
E13
E14
E14
+5
REQ
470Ω
REQ TRNS L
E13
E12
CSL/M(DATA)
J1-47
E12
N.DATA
SERVICON
E12
2 FOLDOUT FRAME
FOLDOUT FRAME
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/MMES INTERFACE
LOGIC DIAGRAM
11/70 DMA/7902 INTERFACE
CARD 2
2131
2112-0382
791001.DGN
NONE
B
791001
SHEET 1 OF 3


REV | DATE | ZONE | DESCRIPTION | APPROVAL
J1-25
J1-22
J1-23
J1-28
J1-39
J1-29
J1-31
J1-19
KA0
KA1
KA2
KA3
KA4
KA5
KA6
KA7
EN CSL H
REQ TRNS L
DATA(07:00)
(1,3)
+VPDP
N/C
J3
FOLDOUT FRAME 1
FOLDOUT FRAME 2
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/MMES INTERFACE
LOGIC DIAGRAM
11/70 DMA/7902 INTERFACE
CARD 2
DWG NO 791001
SHEET 2 OF 3
SIZE B
DESIGN FILE 791010.DGN
SCALE NONE


+5V
F1
.75A
J3
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
8T97
DATA 07
06
05
04
03
02
(1,2)
IN F
IN E
EN 2
IN D
IN C
IN B
IN A
EN4
OUT F
OUT E
OUT D
OUT C
OUT B
OUT A
DATA<07:00>
(1)
DATA 01
DATA 00
(1,2)
7902 DATA MODE H
DIR ε TO PDPH
DLC
DLC
(1)
E14-12
DATA
(1)
E14-5
J1-2
ORD 7
(ε TO PDP H)
N/C
2 FOLDOUT FRAME
FOLDOUT FRAME
M&S COMPUTING, INC.
HUNTSVILLE, ALABAMA
SAES
SAES/MMES INTERFACE
LOGIC DIAGRAM
11/70 DMA/7902 INTERFACE
CARD 2
ORIGINATOR
CHECKED
APPROVED
MATERIAL
TOLERANCE
PART NO.
DEPARTMENT 2131
SALES ORDER 2112-0382
CODE
DESIGN FILE 791001A.DGN
SCALE NONE
SIZE B
DWG NO 791001
SHEET 3 OF 3
REV
DESCRIPTION
APPROVAL
ZONE
DATE

SAES
SAES/MMES INTERFACE
WIREWRAP LAYOUT LIST

CARD 1

Reference Drawing
Logic Diagram 791000

PARTS LIST

SAES/MMES IF CARD1 PAGE #1

QUANITY	DESCRIPTION
1	W9500, DEC WIREWRAP BOARD
2	8T97, IC
12	4360, IC (HP OPTO ISOLATOR)
1	74221, IC
1	7400, IC
1	74S280, IC
1	74S240, IC
1	74LS373, IC
3	AM26LS12, IC
2	AM26LS32, IC
18	.1μf 200V, DISC CAP
2	.001 200V, DISC CAP
13	10μf 25V, TANT CAP
12	390Ω 5% 1/4wt
12	130Ω 5% 1/4wt
19	110Ω 5% 1/4wt
8	4.7K 5% 1/4wt
5	1K 5% 1/4wt
1	1.8K 5% 1/4wt
1	18.2K 1% 1/8wt
2	50PIN 3M WW Header
1	4484 (HP LED)

PART NO.	VALUE / TYPE	W9500 LOCATION
E1	26S12	LL-5
E2	26S12	LL-15
E3	26S12	LL-25
E4	74S240	LL-35
E5	AM26LS32 PC	LL-47
E6	AM26LS32 PC	LL-57
E7	74LS373	JJ-20
E8	74S280	JJ-32
E30	4360	K-4
E31	4360	K-13
E32	4360	K-22
E33	4360	K-31
E34	4360	K-40
E35	4360	K-49
E36	7400	K-57
E37	4360	H-4
E38	4360	H-13
E39	4360	H-22
E40	4360	H-31
E41	4360	H-40
E42	4360	H-49
E43	8T97	E-32
E44	8T97	E-45
E45	74221	E-56
D1	LED	M-1 =A
F1	1A PICO FUSE	H-59

PART NO.	VALUE / TYPE	W9500 LOCATION
R1	110Ω 5% 1/4wt	JJ-63
R2	110Ω 5% 1/4wt	JJ-62
R3	110Ω 5% 1/4wt	JJ-61
R4	110Ω 5% 1/4wt	JJ-60
R5	110Ω 5% 1/4wt	JJ-58
R6	110Ω 5% 1/4wt	JJ-57
R7	110Ω 5% 1/4wt	JJ-56
R8	110Ω 5% 1/4wt	JJ-55
R9	110Ω 5% 1/4wt	JJ-53
R10	110Ω 5% 1/4wt	JJ-52
R11	110Ω 5% 1/4wt	JJ-51
R12	110Ω 5% 1/4wt	JJ-50
R13	110Ω 5% 1/4wt	JJ-48
R14	110Ω 5% 1/4wt	JJ-47
R15	110Ω 5% 1/4wt	JJ-46
R16	110Ω 5% 1/4wt	JJ-45
R17	110Ω 5% 1/4wt	JJ-43
R56	110Ω 5% 1/4wt	JJ-41
R57	110Ω 5% 1/4wt	JJ-42
R18	390Ω 5% 1/4wt	K-1
R19	130Ω 5% 1/4wt	K-2
R20	4.7K 5% 1/4wt	K-9
R21	390Ω 5% 1/4wt	K-10
R22	130Ω 5% 1/4wt	K-11
R23	4.7K 5% 1/4wt	K-18
R24	390Ω 5% 1/4wt	K-19
R25	130Ω 5% 1/4wt	K-20
R26	4.7K 5% 1/4wt	K-27
R27	390Ω 5% 1/4wt	K-28
R28	130Ω 5% 1/4wt	K-29
R29	4.7K 5% 1/4wt	K-36
R30	390Ω 5% 1/4wt	K-37
R31	130Ω 5% 1/4wt	K-38
R32	1K 5% 1/4wt	K-45

PART NO.	VALUE / TYPE	W9500 LOCATION
R33	390Ω 5% 1/4wt	K-46
R34	130Ω 5% 1/4wt	K-47
R35	1K 5% 1/4wt	K-54
R36	390Ω 5% 1/4wt	H-1
R37	130Ω 5% 1/4wt	H-2
R38	4.7K 5% 1/4wt	H-9
R39	390Ω 5% 1/4wt	H-10
R40	130Ω 5% 1/4 wt	H-11
R41	4.7K 5% 1/4wt	H-18
R42	390Ω 5% 1/4wt	H-19
R43	130Ω 5% 1/4wt	H-20
R44	4.7K 5% 1/4 wt	H-27
R45	390Ω 5% 1/4wt	H-28
R46	130Ω 5% 1/4wt	H-29
R47	4.7K 5% 1/4wt	H-36
R48	390Ω 5% 1/4wt	H-37
R49	130Ω 5% 1/4wt	H-38
R50	1K 5% 1/4wt	H-45
R51	390Ω 5% 1/4wt	H-46
R52	130Ω 5% 1/4wt	H-47
R53	1K 5% 1/4wt	H-54
R54	18.7K 1% 1/4wt	H-58
R55	1.8K 5% 1/4wt	H-60
R58	1K 5% 1/4wt	M-2

PART NO.	VALUE / TYPE	W9500 LOCATION

PART NO.	VALUE / TYPE	W9500 LOCATION
C1	.001μf 1KV	H-61
C2	.001μf 1KV	H-57
C3	.1μf 200V	JJ-40
C4	.1μf 200V	JJ-7
C5	10μf 25V TANT.	JJ-4
BYPASS	10μf 25V TANT	E-0
		E-65
		H-0
		H-65
		K-0
		K-65
		M-0
		JJ-0
		JJ-65
		LL-0
		LL-65
		NN-65
	.1μf 200V	LL-14
		LL-34
		LL-56
		JJ-31
		JJ-44
		JJ-49
		JJ-54
		JJ-59
		K-8
		K-21
		K-39
		K-56
		H-12
		H-30
		H-48
		E-43

PART NO.	VALUE / TYPE	W9500 LOCATION
J3	50pin WW HEADER	F/E-27
	INSTALL ON BACK	
	CUT RUNS	
J1	50pin WW HEADER	NN/PP-57
	INSTALL ON BACK	
	CUT RUNS	
J2	40 pin Header	
	ON BOARD	

START: To: PAGE # 5

GROUND BUSS

J2 (ODD) , J1 (ODD)

E1-8, LL-14, E2-8, E3-14, E3-11, E3-5, E3-8, LL-34

E4-1, E4-19, E4-10, E5-12, E5-9, LL-56, E6-12, E6-8

E7-1, E7-10, JJ-31, E8-4, E8-7, JJ-44, JJ-49, JJ-54, JJ-59

E30-5, K-8, E31-5, K-21, E32-5, E33-5, K-39, E34-5, E35-5, K-56

E37-5, H-12, E38-5, E39-5, H-30, E40-5, E41-5, H-48, E42-5

E43-1, E43-8, E-43, E44-1, E44-15, E44-8, E45-8, E45-9

START:	TO:
	+5 Buss
	E1-16, MM-14, E2-16, E3-16, MM-34, E4-20, E5-16, E5-4
	MM-56, E6-16, E6-4
	KK-4, KK-7, E7-20, KK-31, E8-14, KK-40, (KK-42 ⇒ KK-63)
	M-2
	E30-8, L-8, L-9, E31-8, L-18, L-21, E32-8, L-27, E33-8
	L-36, L-39, E34-8, L-45, E35-8, L-54, L-56, E36-14
	E37-8, J-9, J-12, E38-8, J-18, E39-8, J-27, J-30, E40-8
	J-36, E41-8, J-45, J-48, E42-8, J-54, J-58, J-60, J-64
	E43-16, E43-15, F-43, E44-16, E45-16, E45-3, E45-11

J3 SHEET 4 11/34 / SIGMA IF
CARD 1

PAGE # 7

START:	TO:
R19-L	R18-L, J3-1 ✓
R22-L	R21-1, J3-5 ✓
R25-L	R24-L, J3-9 ✓
R28-L	R27-L, J3-13 ✓
R31-L	R30-L, J3-17 ✓
R34-L	R33-L, J3-21 ✓
R37-J	R36-J, J3-3 ✓
R40-J	R39-J, J3-7 ✓
R43-J	R42-J, J3-11 ✓
R46-J	R45-J, J3-15 ✓
R49-J	R48-J, J3-19 ✓
R52-J	R51-J, J3-23 ✓
J3-2	R19-K, E30-3 ✓
J3-4	R37-H, E37-3 ✓
J3-6	R22-K, E31-3 ✓
J3-8	R40-H, E38-3 ✓
J3-10	R25-K, E32-3 ✓
J3-12	R43-H, E39-3 ✓
J3-14	R28-K, E33-3 ✓
J3-16	R46-H, E40-3 ✓
J3-18	R31-K, E34-3 ✓
J3-20	R49-H, E41-3 ✓
J3-22	R34-K, E35-3 ✓
J3-24	R52-H, E42-3 ✓

START:	TO:		
J3-1	J3-3, J3-5, J3-7, J3-9, J3-11, J3-13, J3-15, J3-17, J3-19		
	J3-21, J3-23, J3-25, IN RTN	SHEET 4	✓
F1-H	J3-31, J3-33, J3-35, J3-37, J3-39, J3-41, J3-43, J3-45		
	J3-47, J3-49 ✓ out RTN	SHEET 3	
E43-9	J3-32	EN CSL H	✓
E43-7	J3-34	REQ TRNS L	✓
E43-5	J3-36		✓
E43-3	J3-38		✓
E44-13	J3-40		✓
E44-11	J3-42	DATA OUT	SHEET 3 ✓
E44-9	J3-44		✓
E44-7	J3-46		✓
E44-5	J3-48		✓
E44-3	J3-50		✓

START:	TO:	
E44-2	E7-2	✓
E44-4	E7-5	✓
E44-6	E7-6	✓
E44-10	E7-9	✓
E44-12	E7-12	✓
E44-14	E7-15	✓
E43 2	E7-16	✓
E43-4	E7-19	✓
E2-13	E8-8, E7-3	✓
E2-10	E8-9, E7-4	✓
E2-6	E8-10, E7-7	✓
E2-3	E8-11, E7-8	✓
E1-13	E8-12, E7-13	✓
E1-10	E8-13, E7-14	✓
E1-6	E8-1, E7-17	✓
E1-3	E8-2, E7-18	✓
R20-K	E30-6, E1-2	✓
R38-H	E37-6, E1-5	✓
R23-K	E31-6, E1-11	✓
R41-H	E38-6, E1-14	✓
R26-K	E32-6, E2-2	✓
R44-H	E39-6, E2-5	✓
R29-K	E33-6, E2-11	✓
R47-H	E40-6, E2-14	✓

DATA <07:00>

R <07:00>

START:	TO:	
R58-N	D1-M ✓	
D1-N	E34-6, R32-K, E36-1, E4-8 ✓	DATA MODE H
E41-6	R50-H, E36-5, E36-2 ✓	DIRE TO PDP H
E35-6	R35-K, E45-10 ✓	N DLC
C1-H	E45-6 ✓	
R55-H	C1-J, E45-7 ✓	
E45-5	E4-17 ✓	T SYNC H
E36-3	E36-9, E36-10 ✓	DIRE TO PDP L
E36-8	E4-11	H
E6-13	E43-10 ✓	FCN 1 ENCSL H
E5-3	E36-4 ✓	UB GO PULSE H
E45-1	E5-13, E7-11 ✓	LD DEST REG H
E1-7	E1-9, E2-7, E2-9, E3-7, E3-9, E5-11 ✓	CBL DIR WB TO USER H

U 2

START:	To:		PAGE # 11
E1-1	R17-JJ ,	J2-24 ✓	
E1-4	R16-JJ ,	J2-22 ✓	
E1-12	R15-JJ ,	J2-20 ✓	
E1-15	R14-JJ ,	J2-18 ✓	
E2-1	R13-JJ ,	J2-16 ✓	J2
E2-4	R12-JJ ,	J2-14 ✓	
E2-12	R11-JJ ,	J2-12 ✓	
E2-15	R10-JJ ,	J2-10 ✓	
E3-1	R9-JJ ,	J2-8 ✓	
E8-5	E3-2 ✓	EVEN PARITY TRANS H	
E45-4	E43-6 ✓		
C2-H	E45-14 ✓		
C2-J	R54-H, E45-15 ✓		
C4-JJ	C5-JJ, J2-23 ✓		

J1 WIRING

START:	TO:			PAGE # 12
R56-JJ	C3-JJ, J1-25 (BURIED)	✓		
R57-JJ	R56-KK, E5-2, E5-6, E5-9, E5-14, E6-2, E6-6, E6-10, E6-14			
R1-JJ	E6-15, J1-4	✓		
R2-JJ	E6-9, J1-6	✓		
R3-JJ	E6-7, J1-8	✓		
R4-JJ	E6-1, J1-10	✓		
R5-JJ	E5-15, J1-12	✓		
R6-JJ	E5-10, J1-18	✓		
R7-JJ	E5-7	✓		
R8-JJ	E5-1, J1-26	✓		
E4-12	J1-32			
E4-9	J1-34	✓		
E4-3	J1-50	✓		
	CONTINUITY COMPLETION			
CARD	EDGE CONNECTOR PINS			
D-K2	D-L2	✓	B67	
D-M2	D-N2	✓	B66	
D-P2	D-R2	✓	B65	
D-S2	D-T2	✓	B64	
C-A1	C-B1		NPG	

1154 / SIGMA F

CARD 1

START:	TO:	PAGE # 13
R36-H	E37-2	
R39-H	E38-2	
R42-H	E39-2	
R45-H	E40-2	
R48-H	E41-2	
R51-H	E42-2	
R18-K	E30-2	
R21-K	E31-2	
R24-K	E32-2	
R27-K	E33-2	
R30-K	E34-2	
R33-K	E35-2	
E36-6	E45-2	

SAES
SAES/MMES INTERFACE
WIREWRAP LIST

CARD 2

Parts List

SAES/MMES IF Card 2

Quanity	Description
1	Zerox Wirewrap Board
4	8T97 , IC
10	4360 , IC (HP Opto Isolator)
2	74173 , IC
1	7474 , IC
1	7402 , IC
1	7410 , IC
1	7805 , IC Voltage Reg.
1	4484 , HP LED
1	240Ω 5% 1/4wt
9	160Ω 5% 1/4wt
1	470Ω 5% 1/4wt
10	390Ω 5% 1/4wt
10	1K 5% 1/4wt
9	.1μf 200V , CAP
5	10μf 25V , TANT CAP.
11	16 pin WW Socket - Augat
3	14 pin WW Socket - Augat
1	50 pin 3M WW Header

START:	TO:	
J1-2	E1-15, E1-10, E1-9, E1-8, C1-A, C2-A, E2-15, E2-10, E2-9	
	E2-8, C3-A, C4-A, E3A-5, E3B-5, E4A-5, E4B-5	
	C5-A, C6-A, E5A-5, E5B-5, E6A-5, E6B-5	GROUND
	C7-A, C8-A, E7A-5, E7B-5, E15-3, E8-1, E8-8, E9-8, E8-15, E9-1,	
	C9-A, E9-15, E10-8, E11-8, C10-A, E12-7, E13-7, C11-A, E14-7,	
	C13-A, C12-A	
J1-51	E15-1	+8V
E15-2	D1-B, E8-16, E9-16, C9-B, F1-B, E10-16, E11-16, C10-B, E12-14,	+5V
	E13-2, E13-4, C11-B, E13-14, E14-14, C13-B, C12-B, E13-10	
E15-2	E7A-8, E7B-8, E6B-8, E6A-8, C7-B, C8-B, E5A-8, E5B-8,	
	E4B-8, E4A-8, C3-B, C4-B, E3A-8, E3B-8, E2-16, E1-16,	
	C1-B, C2-B	
F1-A	J3-{1,3,5,7,9,11,13,15,17,19,21,23,25}	

START:	TO:	
J1-6	E1-11	DAØ: R
J1-7	E1-12	DA1: R
J1-9	E1-13	DA2: R
J1-8	E1-14	DA3: R
J1-11	E2-11	DA4: R
J1-12	E2-12	DA5: R
J1-15	E2-13	DA6: R
J1-13	E2-14	DA7: R
J1-37	E14-3, E14-4, E14-5, E9-10, E13-12	DATA
J1-34	E13-13, E12-2	SERVICON
J1-45	E14-2, E14-1, E14-13	RSAU
E14-6	E12-3	N DATA
E12-1	E13-1	DATA+N SERVICON
E13-8	E12-5	NREQ
E12-10	E12-6, E2-1, E2-2, E1-1, E1-2	EN CSL L
E14-12	E14-11, E14-10, E14-9	NRSAU
E3B-6	E13-3	REQ TRNS L
E1-6	E10-13, E8-14	DATA Q7
E1-5	E10-11, E8-12	DATA Q6
E1-4	E10-9, E8-10	DATA Q5
E1-3	E10-7, E8-6	DATA Q4
E2-6	E10-5, E8-4	DATA Q3
E2-5	E10-3, E8-2	DATA Q2
E2-4	E11-13, E9-14	DATA Q1
E2-3	E11-11, E9-12	DATA QQ
E14-8	E13-11	RSAUU
E2-7	E1-7, E13-9, E9-4	DLC

START:	TO:	PAGE # 4
J1-2	E9-6	ORO 7
E8-13	J3-2	DATA Ø7 OUT
E8-11	J3-4	DATA Ø6 OUT
E8-9	J3-6	DATA Ø5 OUT
E8-7	J3-8	DATA Ø4 OUT
E8-5	J3-10	DATA Ø3 OUT
E8-3	J3-12	DATA Ø2 OUT
E9-13	J3-14	DATA Ø1 OUT
E9-11	J3-16	DATAØØ OUT
E9-9	J3-18	7902 DATA MODE H
E9-7	J3-20	DIR ≤ TO POP H
E9-5	J3-22	DLC OUT
E3A-6	E10-15, E10-1, E11-15, E12-8, E12-9	EN CSL H

START:	TO:	PAGE # 5
J3-31	J3-33, J3-35, J3-37, J3-39, J3-41, J3-43, J3-45, J3-41, J3-49 ✓	
J3-31	R1-B, R11-A ✓	
J3-33	R2-B, R12-A ✓	
J3-35	R3-B, R13-A ✓	
J3-37	R4-B, R14-A ✓	
J3-39	R5-B, R15-A ✓	
J3-41	R6-B, R16-A ✓	
J3-43	R7-B, R17-A ✓	
J3-45	R8-B, R18-A ✓	
J3-47	R9-B, R19-A ✓	
J3-49	R10-B, R20-A	
J3-32	R1-A, E3A-3 ✓	
J3-34	R2-A, E3B-3 ✓	
J3-36	R3-A, E4A-3 ✓	
J3-38	R4-A, E4B-3 ✓	
J3-40	R5-A, E5A-3 ✓	
J3-42	R6-A, E5B-3 ✓	
J3-44	R7-A, E6A-3 ✓	
J3-46	R8-A, E6B-3 ✓	
J3-48	R9-A, E7A-3 ✓	
J3-50	R10-A, E7B-3 ✓	

START:	TO:
R11-B	E3A-2 ✓
R12-B	E3B-2 ✓
R13-B	E4A-2 ✓
R14-B	E4B-2 ✓
R15-B	E5A-2 ✓
R16-B	E5B-2 ✓
R17-B	E6A-2 ✓
R18-B	E6B-2 ✓
R19-B	E7A-2 ✓
R20-B	E7B-2 ✓
C12-B	R21-B, R22-B, R23-B, R24-B, R25-B, R26-B, R27-B, R28-B, R29-B, R30-B
R21-A	E3A-6 ✓
R22-A	E3B-6 ✓
R23-A	E4A-6 ✓
R24-A	E4B-6 ✓
R25-A	E5A-6 ✓
R26-A	E5B-6 ✓
R27-A	E6A-6 ✓
R28-A	E6B-6 ✓
R29-A	E7A-6 ✓
R30-A	E7B-6 ✓

SIGNAL	IF PIN	DCJ902
DA0:R	6	24-5
DA1:R	7	24-8
DA2:R	9	24-23
DA3:R	8	24-29
DA4:R	11	24-41
DA5:R	12	24-17
DA6:R	15	24-26
DA7:R	13	24-44
DATA	37	22-35
SERVICON	34	23-38
RSAU	45	28-06
PHTO	21	29-11
CSC/m (DATA)	47	23-37
KA0	25	21-47
KA1	22	21-24
KA2	23	21-43
KA3	28	21-36
KA4	39	21-21
KA5	29	21-02
KA6	31	21-12
KA7	19	21-11
ORD 7	2	21-9

M10P M005 TO 7902 + IF

APPENDIX C

UDIF REPLACEMENT

The UDIF boards used in the SAES Engine Dynamics Simulator for the EDS/ESS and the EDS/MMES interfaces differ in two ways:

1. The vector interrupt address for the ESS interface is 0260 while the MMES interface uses address 0264 as an interrupt vector.

2. The UDIF register addresses for the ESS interface begin at octal address 17764000 while the MMES interface UDIF register addresses begin at octal address 17764040.

The vector interrupt address for the ESS interface is obtained by setting positions 2, 4, and 5 of the dip switch on board 2 to the on state (away from the side marked open).

The vector interrupt address for the MMES interface is obtained by setting positions 2, 4, 5, and 7 to the on state.

The starting address for the UDIF registers is set with jumpers at the lower left-hand corner of board 1. For the ESS interface, jumper number 8 is connected to G. For the MMES interface, jumpers number 8 and 5 are connected to G.