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REPORT NO. FR79-76-934R
HAC REF. NO. E1954

FINAL REPORT
(CONTRACT NO NAS 8-33075)

FEASIBILITY STUDY OF SILICON NITRIDE PROTECTION OF PLASTIC ENCAPSULATED SEMICONDUCTORS

AUGUST 1979

AEROSPACE GROUPS

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

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Contract NAS 8-33075

FINAL REPORT
15 July 1978 to 30 June 1979

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FOREWORD

This final report presents the results of work performed during the period 24 July 1978 through 21 June 1979 under Contract NAS 8-33075 with George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Alabama. The study was undertaken within the Advanced Technology Laboratory of the Technology Support Division of the Aerospace Groups of the Hughes Aircraft Company. The Advanced Technology Laboratory is under the management of Mr. R. Y. Scapple.

The program, entitled "Feasibility Study of Silicon Nitride Protection of Plastic Encapsulated Semiconductors", involved evaluating the compatibility of depositing low temperature silicon nitride protective layers on wire-bonded integrated circuits. The objective of the current program was the determination of the mechanical and electrical compatibility of both plasma and photochemical silicon nitride protection of integrated circuits followed by plastic encapsulation. The ultimate objective is the development of a military qualified, high reliability plastic packaged device in which stability is imparted by the silicon nitride passivation process.

The contract was administered by the Electronics and Control Laboratory of the Marshall Space Flight Center, with Dr. A. M. Holladay and Mr. L. C. Hamiter serving as the Contracting Officer Representative and Alternate C.O.R. respectively. The Program Manager was Dr. J.W. Peters and the Senior Consultant on the Program was Dr. T.C. Hall. Low temperature silicon nitride processing was coordinated by Dr. F.L. Gebhart. Electrical parametric testing and environmental testing were coordinated by Mr. A.P. Arquero and Mr. J.K. Takayesu respectively. Failure Analysis was performed by Dr. D.A. Demeo and J.J. Erickson. Technical consultation also was provided by Mr. R.Y. Scapple, Dr. W.G. Brammer and G.A. Dryer.

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ABSTRACT

This final report summarizes the results of a feasibility study for the application of low temperature silicon nitride protective layers on wire-bonded integrated circuits mounted on lead frame assemblies. The program included an evaluation of the mechanical and electrical compatibility of both plasma nitride and photochemical silicon nitride (photonitride) passivations (parallel evaluations) of integrated circuits which were then encapsulated in plastic. The ultimate objective of the silicon nitride packaging approach is the development of a military qualified, high reliability plastic encapsulated device.

The results of the feasibility study demonstrate that photonitride passivation is compatible with all wire bonded lead frame assemblies, with or without initial chip passivation. Plasma nitride passivation of lead frame assemblies is possible only if the chip is passivated before lead frame assembly.

The survival rate after the environmental test sequence of devices with a coating of plasma nitride on the chip and a coating of either plasma nitride or photonitride over the assembled device is significantly greater than that of devices assembled with no nitride protective coating over either chip or lead frame.

The survival, after the application of photonitride to lead frame assemblies, of devices with no chip passivation suggests the possibility of simplifying the device fabrication process by eliminating the chip passivation operation. Such a simplification would not be possible if the lead frame assemblies were passivated with plasma nitride.

Experimental test results demonstrated that there were no permanent device failures in the accelerated environmental test which could be attributed to corrosion. Based on this result, the inference can be made that the test sequence was not sufficiently severe to separate the various passivation processes. Therefore, based on the overall results of the feasibility study, a comprehensive follow-on program to allow an in-depth evaluation to be carried out is recommended. The recommended follow-on program would incorporate a significantly more severe accelerated environmental test sequence utilizing a total of 5000 devices including a linear and a digital device type.

1.0 INTRODUCTION

1.1 PREVIOUS WORK ON THE PHOTOCHEMICAL DEPOSITION OF Si_3N_4

The present program is a direct result of work carried out for the Air Force Materials Laboratory under Contract F33615-76-C-5081. In that work, summarized in Technical Report AFML-TR-77-74 on Low Temperature Photochemical Deposition of Silicon Nitride Passivation Layers, a statically operated photochemical deposition reactor was developed and used successfully to (1) evaluate the characteristics of photochemically deposited silicon nitride ("photonitride") and to (2) coat selected monolithic devices with a protective layer of silicon nitride. The process employed a mercury vapor sensitized reaction between silane and ammonia or silane and hydrazine vapor. Low temperature photonitride films of good quality were prepared at temperatures ranging from 100°C to 300°C. This initial R&D effort resulted in the development and construction of a low pressure, continuous gas flow production reactor for the photochemical vapor deposition of silicon nitride passivation layers for microelectronic applications.

1.2 PROGRAM OBJECTIVES

The principal objective of the program was the determination of the effectiveness of the silicon nitride passivation process in inhibiting the corrosion due to moisture at wire interconnect sites, thus leading to overall enhanced reliability of the plastic molded IC devices. A corollary objective of this program was the prevention, by prior nitride passivation of IC assemblies, of semiconductor surface state shifts due to moisture and ion permeability of typical plastic encapsulants. A secondary objective of the program was to establish the necessary handling and processing procedures to allow silicon nitride passivation of parts in a practical production-like manner.

The photonitride film potentially constitutes a hermetic seal for hybrid microcircuits by providing a barrier to contamination from mobile ions and moisture. The enhanced reliability referred to above is a direct consequence of the conformal nature of the film and further, that the film can be applied after assembly of the device (but before encapsulation) and thus protect and insulate the entire wire bonded microcircuit assembly. The possibility of a system malfunction due to electrical short circuits caused by corrosion induced by mobile ions or moisture can thus be eliminated.

The silicon nitride passivation of integrated circuits prior to plastic molding could provide both NASA and the DoD with long-term benefits with respect to eventual development of a military-qualified, high-reliability plastic packaged device. The silicon nitride passivated integrated circuit followed by plastic encapsulation is a concept which can ultimately lead to a high-reliability packaging technique surpassing that of the conventional glass-metal hermetic package. The passivation process can also eliminate the need for a complex trimetallization system at the chip level thus permitting the highly desirable use of a simple wire-chip metallization combination (e. g., aluminum). The cost reductions associated with nitride coated plastic ICs in terms of both enhanced reliability and packaging processing compared to conventional plastic and hermetic packaging would be significant.

1. 3 PROGRAM SUMMARY

This program was designed and executed to provide an evaluation of the overall protection given to plastic encapsulated devices containing charge sensitive microcircuits (CMOS 4001B) by several passivation processes. These were plasma nitride, photonitride and no nitride (bare).* Two pre-assembly chip preparations were included: plasma nitride, and no nitride. A number of chips mounted in unsealed metal flat packs were subjected to the identical passivation processes as the plastic encapsulated chips.

Passivation of the devices (distinguished from passivation of the chip alone) was accomplished while the devices were still attached to the lead frames.

*No passivation coating, SiO_2 or otherwise.

After assembly the devices were given a sequence of electrical and environmental tests. These were 1) temperature cycling, 2) high temperature electrical stress (HTRB), and 3) temperature and humidity exposure. Electrical parametric measurements were made of all devices initially and then at intervals in the course of each test.

The results of the electrical screening of all the devices after the completed accelerated test sequence demonstrate that the photonitride process is compatible with all wire bonded lead frame assemblies irrespective of chip passivation. The survival after the application of photonitride of devices with no chip passivation suggests the possibility of simplifying the fabrication process by eliminating the chip passivation operation. At the present time, with current plasma nitride passivation processes, this does not seem possible since a failure rate of 80 percent or greater was observed for devices with no chip passivation but with plasma nitride passivation on the wire-bonded lead frames assemblies.

Evaluation by optical scanner and by electrical microprobe were used to establish the accumulation of positive charge in the passivation film as the probable cause of failure of the plasma nitride coated devices. All the photonitride coated devices exhibited the predicted photoresponse image (optical spot scanner) characteristic of a completely functional device.

1.4 ADVANTAGES OF THE PHOTONITRIDE PASSIVATION COATING

Several significant advantages exist for the photochemical process over competing plasma and sputtering processes in the deposition of low temperature silicon nitride on microelectronic devices.

The photochemical process is initiated solely by the absorption of radiant energy in discrete amounts (quanta) by a mercury photosensitizer, which, upon collision of the activated mercury with the reactive gas molecules, results in the chemical bond disassociation of the reactant gases necessary for the formation of the passivating film. A low pressure mercury arc lamp is the sole source of radiant energy in the process. The single by-product of the reaction is hydrogen. Mercury, after playing the role of intermediary

(sensitizer) in the reaction between silane and ammonia, has no further part in the reaction, except to reabsorb the radiant (2537Å) energy and repeat its catalytic role in the process.

Since the photochemical method of silicon nitride deposition is free of both charged species and high energy radiation, shifts in device characteristics due to these causes are eliminated.

The sputtering process, by comparison, relies fundamentally on high energy ionization processes. The working gas, typically argon, is ionized by an applied electric field. Positively charged argon ions are accelerated toward the cathode, the source of material to be sputtered. Primary and secondary electrons are also accelerated, but in the opposite direction, impacting with high energy on the objects to be coated. Elaborate cooling devices are sometimes necessary to protect sensitive substrates from excessive increases in temperature.

In contrast to the radiant energy at a single, sharply defined wavelength employed by the photochemical process, the radiant spectrum of both the sputtering process and the plasma process extends from the IR to the far UV and into the X-ray region.

1.5 BACKROUND AND DEVELOPMENT OF PHOTOCHEMICALLY DEPOSITED SILICON NITRIDE PASSIVATING FILM

Low temperature photochemical silicon nitride (LTPN) films deposited for the present work are prepared by the mercury photosensitized gas phase reaction of silane (SiH_4) and ammonia (NH_3). The overall stoichiometry for the reaction is represented by the following equation:

$$3\ SiH_4 + 4\ NH_3 \xrightarrow[Hg]{h} Si_3N_4 + 12\ H_2$$

Only radiation which is absorbed, either by the reactants or the photosensitizer, can lead to a photochemical reaction. Silane and ammonia absorb UV radiation only at wavelengths below 2200Å. The most convenient source of UV light for photochemical processes is the quartz mercury arc lamp. The radiation from this type of lamp is limited by the quartz UV cut off wavelength of approximately 2000Å, leaving only a very narrow "window" between 2000Å and 2200Å for light activation of the NH_3 molecule.

This limitation may be overcome by resorting to photosensitization techniques. A convenient means of photosensitizing a gas phase chemical reaction is to saturate the system with mercury vapor at room temperature ($\sim 10^{-3}$ torr) and to irradiate the system with mercury resonance radiation. A strong resonance line in the mercury spectrum occurs at 2537Å, nearly all of which is absorbed by the mercury vapor contained within the reactive chemical system.

Ultraviolet energy is absorbed by the mercury vapor, raising it from a singlet ground state ($S_o^{1/2}$) to a triplet excited state ($P^{3/2}$) as follows:

$$h\frac{c}{\lambda} + Hg\ (S_o^{1/2}) \rightarrow Hg\ (P^{3/2})$$

or more simply:

$$h\frac{c}{\lambda} + Hg^\circ \rightarrow Hg^*$$

where

Hg° = Ground state mercury atom
Hg^* = Excited state mercury atom
h = Planck's constant = 6.62×10^{-27} erg-sec
c = Velocity of light = 3×10^{10} cm/sec
λ = Wavelength of radiation = 2537Å

The excited Hg^* atom then transfers its energy by collision to the chemical reactants within the system, generating free radicals which initiate chain reactions eventually leading to the final Si_3N_4 product. This process is illustrated below:

$$Hg^* + SiH_4 \rightarrow SiH_3 + H + Hg^\circ$$

These species, by interaction with other unexcited reactants, lead to the desired final product, silicon nitride. The efficiency with which the ultraviolet energy is conveyed to the chemical system is thus greatly enhanced by photosensitization.

The earlier work of Collett[1] and also the work of v. d. Brekel and Severin[2] illustrated the practicality of employing such a photosensitized chemical reaction to produce useful thicknesses of Si_3N_4 films for microelectronic device applications. However, the quality of these earlier photochemically produced silicon nitride coatings was diminished by the presence of pinholes in the films.

The photochemical deposition process for silicon nitride will provide challenging competition with the thermal process and with the plasma process in the application of passi ation coatings to semiconductor devices. The advantages of the photochemical process, low deposition temperature, zero stray radiation and ion levels, have been mentioned previously.

In the thermal process a mixture of silane and ammonia at 1 to 10 torr is brought in contact with the object to be coated which is held at a temperature between 700 and 1000°C, typically 900°C. In the resulting thermally activated reaction silicon nitride is deposited on the object to be coated. The by-product, hydrogen, is pumped out of the reaction chamber along with any unreacted ammonia or silane. While deposition rates for the thermal method are relatively high and film uniformity and reproducibility are good, the high deposition temperatures make the thermal method impractical for the after-assembly passivation of devices containing relatively low melting point metallization and bonding wire.

In the plasma process for the deposition of silicon nitride, an r.f. discharge is established in a low pressure mixture of silane and ammonia contained in a chamber which also contains the devices to be coated. The effect of the discharge is to create an abundance of ionized chemical species not only from the dissociation of silane and ammonia but also in some cases by direct sputtering from the walls of the chamber. Devices within the chamber receive not only the desired coating of silicon nitride but also large amounts of both ionic and radiative bombardment, both of which can lead to the destruction of charge-sensitive devices. These destructive processes are entirely absent from the photonitride process.

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1. Collett, M. G., J. Electrochem. Soc., 116, 110 (1969)
2. v. d. Brekel, C. H. J., and Severin, P. J., J. Electrochem Soc., 119, 372 (1972)

1.6 TECHNICAL APPROACH

This program was a feasibility study which evaluated and compared the mechanical and electrical compatibility of photochemical and plasma silicon nitride with wire bonded integrated circuits. A specific feature of the program was the requirement that the passivation coatings be applied while the chips were still attached to the lead frames. After passivation the ICs were encapsulated in epoxy and given a series of standard environmental tests. The results of these tests provide a measure by which the relative abilities of plasma nitride and photonitride are able to protect plastic encapsulated wire bonded integrated circuit chips.

The program addressed the following subjects:

1. Device Selection
2. Selection of Parameters of Passivation Process
3. Mechanical and Electrical Compatibility with Passivation Process.

1.6.1 Device Selection

The CMOS 4001B, a simple complementary transistor array, was chosen as the vehicle by which to achieve the goals of the feasibility study. This device is an exemplary surface sensitive device and is relatively easy to analyze for electrical deterioration caused by the passivation or the encapsulation process.

A small number of 4001Bs, mounted in metal flat packs, were included in the study to provide information on the effect of the nitride passivation process on the lead and chip surfaces of the devices. The metal flat pack was chosen because it lends itself to rapid optical and scanning electron microscope analysis.

The following general specifications were established for the devices assembled from the 4001B chips:

1. Lead Frames - Alloy 42
2. Chip Metallization - Aluminum
3. Lead Wires - Gold
4. Encapsulation - Morton Anhydride-Cured Epoxy 526A

1.6.2 Selection of Parameters of Passivation Process

The fully mounted and bonded ICs were nitride passivated at 150°C. The following passivation processing parameters were selected. Plasma nitride processing was conducted between 250 and 350°C.

1. Area of device to be passivated
2. Thickness of passivation coating
3. Prepassivation surface treatment
4. Handling procedures

1.6.2.1 Area to be Passivated

The entire IC-lead frame or IC-flat pack assembly including wire bonds was passivated. After nitride processing metal leads were welded onto the flat packs and then the lead frames were plastic molded.

1.6.2.2 Thickness of Passivation Coating

Passivation layers of silicon nitride, ranging in thickness from 2000Å to 5000Å, are sufficient to provide a "hermetic barrier" against moisture and mobile ions. The thickness of the passivation layer was adjusted to provide optimal mechanical compatibility with the lead frames and flexible wire leads.

1.6.2.3 Prepassivation Surface Treatment

Special cleaning of the parts was only considered if recommended by the manufacturer or if cleaning appeared desirable based on prior processing history.

1.6.2.4 Device Handling Procedures

All devices were passivated in routine clean room conditions. Precautions were taken during the plastic molding process to avoid yield loss of parts. Special carriers to prevent contamination of the unmolded ICs from the atmosphere were employed to transport the devices between the manufacturer and the Hughes facility. The devices were handcarried in all transport operations.

1.6.3 Mechanical and Electrical Compatibility of Devices with Passivation Processing

Protective coatings of photochemical nitride and of plasma nitride were applied to identical sets of devices in parallel evaluation efforts. Application of photonitride was conducted within the Hughes facility. All plasma nitride coatings were applied in a plasma nitride reactor at the chip manufacturer's facility. All plasma nitride processes were directed and monitored by Hughes personnel.

1.6.3.1 Processing Matrix Rationale and Processing Sequence

The processing matrix shown in Table 1 was devised to determine if the CMOS 4001B has been irreversibly damaged during either plasma nitride or photonitride processing. The numbers in parentheses are the group identification numbers.

TABLE 1. PHASE I PROCESSING MATRIX

CMOS 4001B - Plastic Molded			
	Passivation		
Chip Preparation	Photo-nitride	Plasma Nitride	None
Plasma Nitride on Chip	40 (1)	40 (2)	40 (3)
No Plasma Nitride on Chip	40 (4)	40 (5)	40 (6)
CMOS 4001B - Metal Flat Pack			
	Passivation		
Chip Preparation	Photo-nitride	Plasma Nitride	None
Plasma Nitride on Chip	12 (7)	12 (8)	12 (9)
No Plasma Nitride on Chip	12 (10)	12 (11)	12 (12)

Half of the CMOS 4001B ICs were obtained from the manufacturer with plasma nitride over the chip. The other half had received no coating of any kind. Plasma nitride is an alternate phosphor silicate glass (PSG) which is the routine passivation layer on the CMOS 4001B now employed elsewhere in the industry. Passivation of the chip and lead frames with low temperature silicon nitride may provide sufficient protection and enhanced reliability irrespective of the initial chip passivation. The plasma nitride or PVX glass deposition step would then be eliminated. An evaluation of the nitride passivation of CMOS 4001B without plasma nitride or PVX glass was included in the processing matrix.

1.6.3.2 Testing and Evaluation

Phase I tests were designed to provide immediate information on the mechanical and electrical compatibility of the devices with the passivation process. Electrical measurements to determine device integrity after nitride passivation and to detect electrical defects and excess yield loss due to either plasma induced charge and radiation damage or photochemically induced damage were conducted. The plastic molded parts were subjected to temperature cycling with post-stress electrical testing and decapped visual inspection to insure that bonding and adhesion integrity had not been degraded. All electrical testing was conducted on a "go (pass operating specifications) - no go (fail operating specifications) basis."

The circuits were evaluated according to the sequence outlined below:

a. Initial visual inspection of the plastic encapsulated units.

b. Initial electrical measurement and analysis of all units.

c. Temperature cycling (-55°C to 125°C), nonoperating for 50 cycles, with electrical measurements taken at 10, 25 and 50 cycles.

d. Units surviving temperature cycling are then subjected to the HTRB at 125°C for 240 hours, with electrical measurements taken at 10, 50, 168 and 240 hours.

e. Units surviving HTRB tested at 85°C at 85 percent relative humidity for 250 hours, with electrical measurements at 10, 50, 168 and 240 hours.

f. Inspection/analysis of failed units.

g. Determination of nitride adhesion and wire bond strength on flat packs.

h. Determination of glass transition temperature of the plastic encapsulant.

Based on the overall results of the feasibility study, a follow-on plan for the comprehensive investigation of low temperature nitride coated, plastic encapsulated integrated circuits will be prepared.

2.0 RESULTS

2.1 DEVICE FABRICATION AND TEST PROCEDURES

2.1.1 Device Fabrication and Processing

An agreement was established with Texas Instruments, Inc., by which that company would supply a set of 312 devices, part of which would be coated with plasma nitride according to the matrix in Table 1. Photo-nitride processing was conducted at Hughes Aircraft Company.

In the fabrication process plasma nitride was applied to half (156) of the chips while still at the wafer stage. The other half received no coating of any kind.

The two groups of 156 each were subdivided into two groups of 36 and two groups of 120, the former being designated for mounting in flat packs, the latter for plastic encapsulation. Each of the two groups of 36 was divided into three groups of 12 and assigned to receive passivation coatings of photo-nitride, plasma nitride or no coating at all. The two groups of 120, intended for plastic encapsulation, were similarly divided into three groups of 40.

Devices intended for eventual plastic encapsulation were assembled onto lead frames of alloy 42. The remaining devices were assembled into one-quarter by one-eighth inch metal flat packs. Chip-to-lead frame and chip-to-flat pack connections were made with 0.001 inch gold wire.

Plasma nitride was applied to 24 flat pack devices and to 80 plastic molded devices at Texas Instruments and all devices (312) handcarried to the site of the photochemical reactor where 24 flat pack-mounted devices

(12 with plasma nitride on the chip, 12 with no coating)* and 80 lead frame-mounted devices (40 with plasma nitride on the chip, 40 with no coating) were passivated in a production photochemical reactor with approximately 3600Å of silicon nitride at a deposition temperature of 150°C (Figures 1 through 4).

The deposition chamber of this equipment is designed to accommodate substrates occupying a total surface area greater than 200 square inches. The reactant gasses, SiH_4 and NH_3, enter at one end of the deposition chamber through mass flow controllers. After passing the length of the chamber the depleted gasses are removed through exhaust ports at the opposite end from the inlet. In routine operation, the devices to be coated are placed within the chamber on a heated tray (Figure 3) and the chamber is evacuated through a mechanical pump to an acceptable base pressure. The flow of reactant gases is initiated, followed by adjustment of total pressure, gas flow rates,

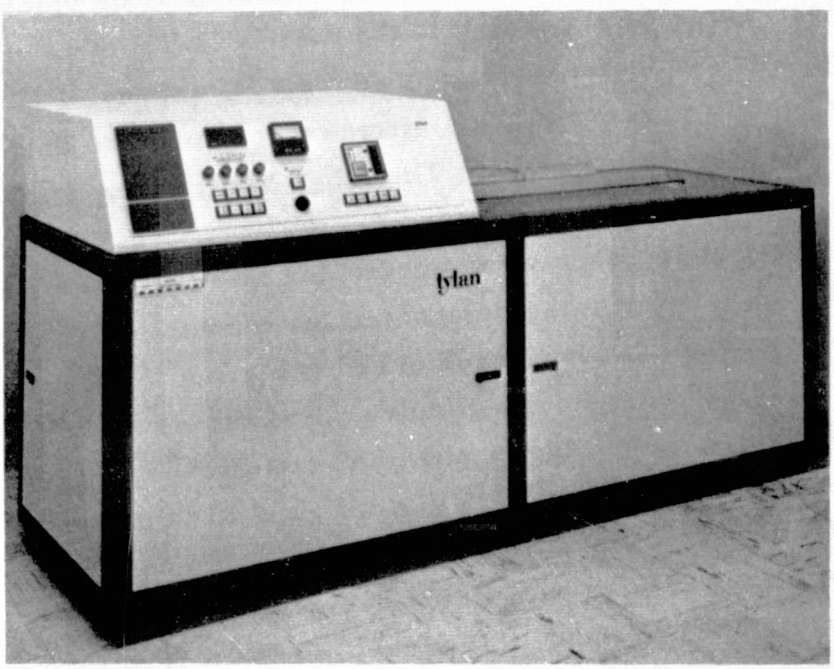


Figure 1. General view of silicon nitride reactor.

*Two groups, mounted in flat packs, with plasma nitride on the lead frames, contained fifteen devices each.

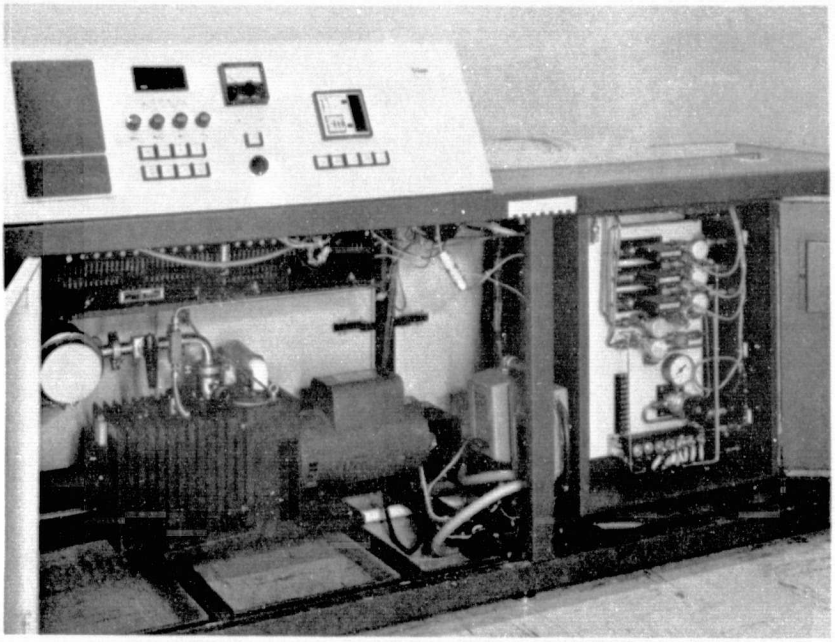


Figure 2. View of silicon nitride reactor showing controls and pumping system.

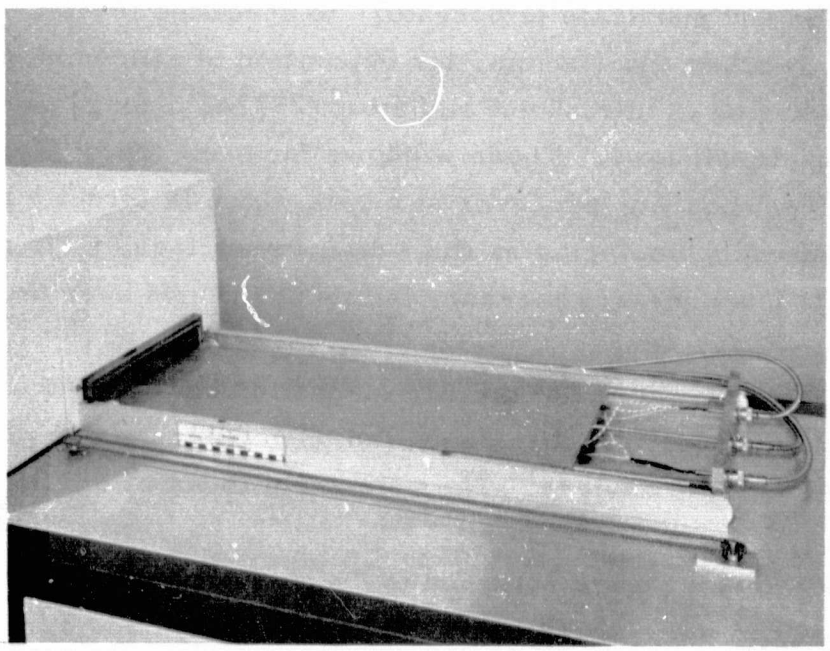


Figure 3. Heated substrate carrier in retracted position ready to be loaded.

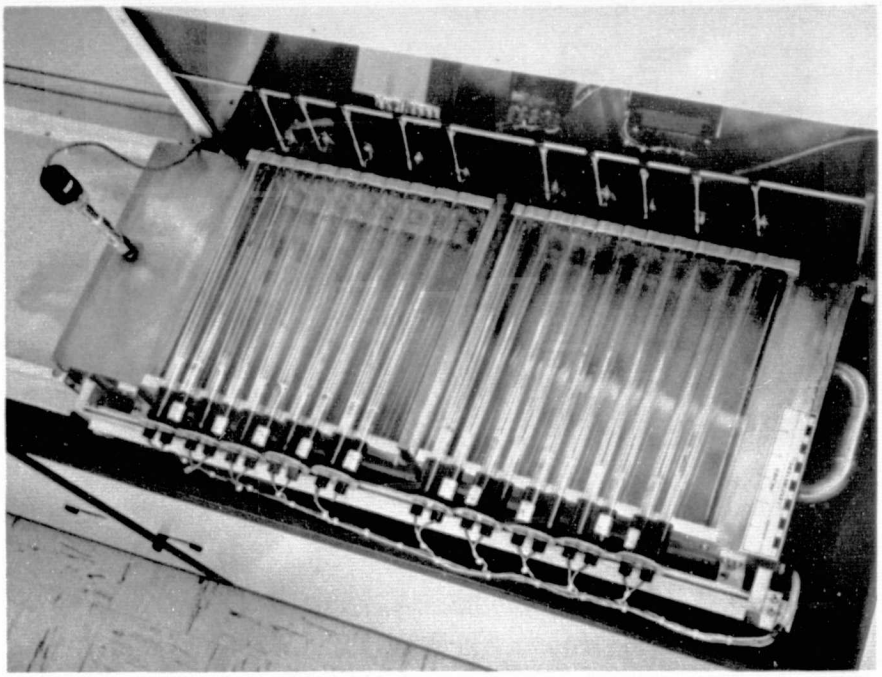


Figure 4. Mercury vapor lamps in positions over fused quartz window.

gas flow ratios and substrate temperature to specified levels. When the complete system reaches equilibrium, the deposition of silicon nitride is initiated by the transmission of ultraviolet radiation (2537Å) through two 12 x 12 x 3/4 inch fused quartz windows. These windows form the top of the deposition chamber. The deposition proceeds at a rate which is directly proportional to the light intensity impinging on the substrate surface and is terminated by turning off the low pressure mercury lamps positioned over the fused quartz window (Figure 4).

The refractive index of the film deposited on the devices was monitored utilizing the identical film deposited on a silicon wafer placed in the reactor along with the devices. The refractive index of the film on the wafer was 1.98.

All 312 devices were returned to Texas Instruments where the appropriate 240 devices were encapsulated in Morton anhydride cured epoxy 526A. Measurements at the Hughes facility showed the glass transition temperature of this formulation to be 347°C. A typical plot obtained from the measurement of the glass transition temperature is shown in Figure 5. The remaining devices, those mounted in one-quarter by one-eighth inch metal flat

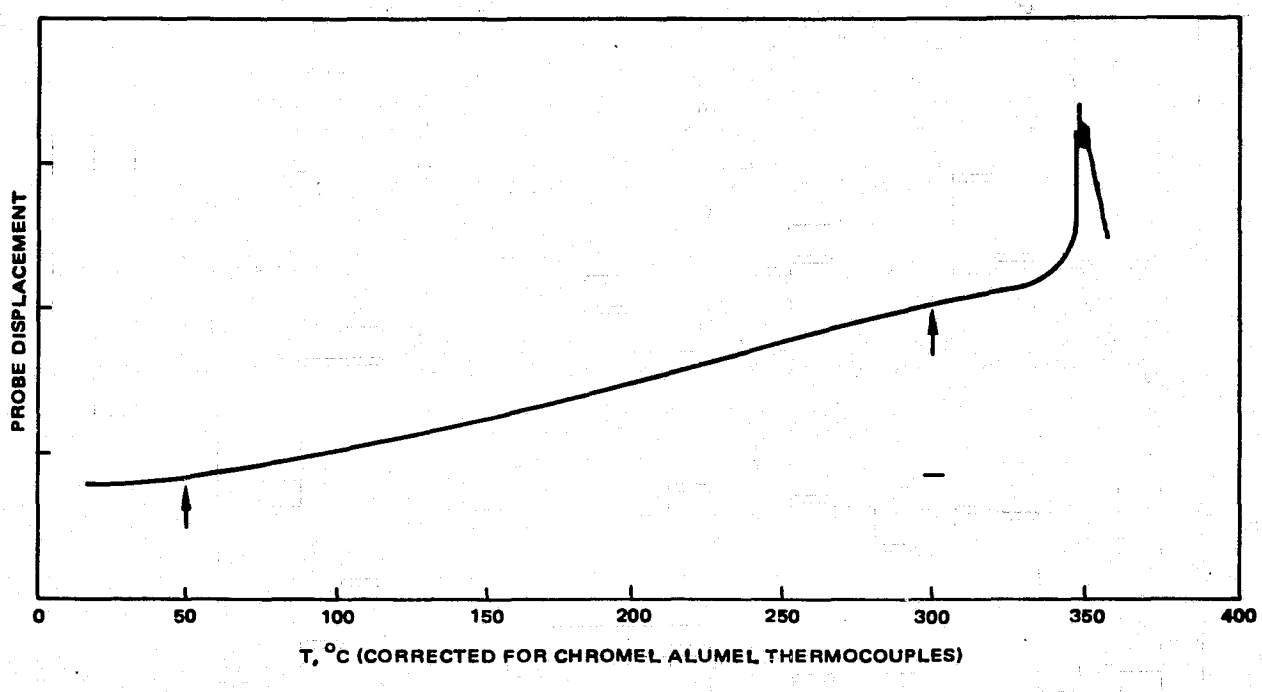


Figure 5. Typical curve of probe displacement versus temperature obtained from measurement of glass transition temperature of Morton 526A epoxy.

packs, had lids tack welded in place in such a way as to protect the devices from accidental mechanical abuse without shielding them from the environments of the temperature-humidity and the HTRB tests.

2.1.2 Device Electrical and Environmental Tests

2.1.2.1 Initial Electrical Evaluation

All devices were given an initial electrical parametric evaluation on a Tektronix 3260 test system located at the Hughes Culver City facility. Results of this test are given in Table 2A in which groups given a specific chip and lead frame or chip and package passivation are identified by numbers from 1 to 12.

Where no chip passivation was employed prior to lead frame assembly and passivation (groups 4, 5, 6) a difference in device yield was noted which points in favor of photonitride for lead frame passivation over plasma nitride. In group 4 thirty-five devices passed and five failed whereas in group 5 only seven passed and thirty-three failed. From comparison of groups 1 and 4 and 5 and 6 several other inferences can be made.

TABLE 2A. SUMMARY OF ELECTRICAL SCREENING RESULTS

DEVICE EXPOSURE: Initial/As Received

PLASTIC DIP									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	36	-1-	4	38	-2-	2	32	-3-	8
None	35	-4-	5	7	-5-	33	26	-6-	14

METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	1	15	-8-	0	11	-9-	1
None	10	-10-	1	0	-11-	15	12	-12-	0

1. If photonitride is used to passivate the lead frame (groups 1 and 4), plasma nitride passivation of the chip only marginally increases the device yield over the use of no chip passivation at all.
2. If no chip passivation is employed (groups 5 and 6) no lead frame passivation is preferable to plasma nitride passivation.

For those devices assembled in metal flat packs and with the exception of one group (group 11), the initial electrical screening does not distinguish between the two types of chip passivation and the three types of package passivation. In groups 7, 8, 9, 10 and 12 no more than one device failed in any group and 10 to 15 devices passed. In group 11, characterized by no chip passivation and plasma nitride lead frame passivation, 15 out of 15 devices failed. This result is similar to that obtained for group 5 illustrating the incompatibility of plasma nitride protection of wire bonded circuits containing chips not initially passivated.

In this initial electrical screening there was little to distinguish plastic encapsulated devices with plasma nitride passivated chips which had received either plasma nitride (group 2) or photonitride (group 1) over the lead frames. In the first case thirty-eight devices passed and two failed whereas in the second case thirty-six devices passed and four failed. Both groups were superior to group 3 which had no lead frame passivation. In this group thirty-two devices passed the initial electrical evaluation and eight failed.

The results of an examination by Optical Scanner and by Electrical Microprobe of a failed and of a good device are given in Section 2.2.

2.1.2.2 Accelerated Environmental and Electrical Testing

The accelerated test sequence consisted of 1) fifty temperature cycles between -55°C and 125°C with electrical evaluation after 10, 25 and 50 cycles; 2) electrical stress at elevated temperature (HTRB) for 240 hours with evaluations at 12, 52, 168 and 240 hours; and 3) temperature/humidity exposure at 85 percent R.H. and 85°C for 240 hours with electrical evaluations at 10, 50, 160 and 240 hours. A summary of the electrical evaluations obtained from the tests above is contained in Tables 2B through 2L.

TABLE 2B. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: Temp. Cycle -55 to 125°C, 10 Cycles

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	38	-1-	0	35	-2-	3	33	-3-	0
None	37	-4-	0	8	-5-	0	26	-6-	2
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	15	-8-	0	10	-9-	1
None	12	-10-	0	0	-11-	0	12	-12-	0

TABLE 2C. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: Temp Cycle -55 to 125°C, 25 Cycles

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	40	-1-	0	38	-2-	0	25	-3-	8
None	34	-4-	1	9	-5-	0	28	-6-	0
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	12	-8-	0	11	-9-	0
None	11	-10-	0	0	-11-	0	12	-12-	0

TABLE 2D. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: Temp. Cycle -55 to 125°C, 50 Cycles

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	39	-1-	0	37	-2-	0	33	-3-	0
None	35	-4-	0	7	-5-	0	24	-6-	0
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	15	-8-	0	11	-9-	0
None	13	-10-	0	0	-11-	0	12	-12-	0

TABLE 2E. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: HTRB, 8 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	33/5*	-1-	1	36	-2-	1	18	-3-	13
None	30	-4-	4	7	-5-	1	27	-6-	1
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	6	-7-	5	11	-8-	4	9	-9-	1
None	12	-10-	0	0	-11-	0	8	-12-	4

*5 marginal parametric failures.

TABLE 2F. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: HTRB, 52 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	39	-1-	0	38	-2-	0	32	-3-	0
None	33	-4-	1	7	-5-	0	27	-6-	1

METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	15	-8-	0	11	-9-	0
None	10*	-10-	0	0	-11-	0	11	-12-	0

*2 devices removed for optical and SEM examination.

TABLE 2G. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: HTRB, 168 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	37	-1-	2	33	-2-	4	33	-3-	0
None	26	-4-	7	8	-5-	0	27	-6-	1
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	9	-8-	2	9	-9-	0
None	9	-10-	0	0	-11-	0	6	-12-	5

TABLE 2H. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: HTRB, 240 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	38	-1-	0	33	-2-	0	31	-3-	2
None	29	-4-	4	5	-5-	3	25	-6-	2

METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	9	-8-	0	11	-9-	0
None	10	-10-	0	0	-11-	0	10	-12-	1

TABLE 21. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: 85% RH/85°C, 8 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	40	-1-	0	37	-2-	0	34	-3-	0
None	29	-4-	4	7	-5-	0	24	-6-	3
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	15	-8-	0	11	-9-	0
None	9	-10-	0	0	-11-	0	10	-12-	0

TABLE 2J. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: 85% RH/85°C, 52 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	40	-1-	0	37	-2-	0	31	-3-	2
None	28	-4-	5	7	-5-	0	23	-6-	1

METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	14	-8-	1	11	-9-	0
None	9	-10-	0	0	-11-	0	11	-12-	0

TABLE 2K. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: 85% RH/85°C, 168 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	39	-1-	0	37	-2-	0	29	-3-	0
None	25	-4-	8	7	-5-	0	24	-6-	2

METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	15	-8-	0	11	-9-	0
None	9	-10-	0	0	-11-	0	11	-12-	0

TABLE 2L. SUMMARY OF ELECTRICAL SCREENING RESULTS

Device Exposure: 85% RH/85°C, 240 hrs.

PLASTIC MOLDED									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	39	-1-	0	37	-2-	0	32	-3-	0
None	28	-4-	5	8	-5-	0	23	-6-	1
METAL FLAT PACK (Tack-Welded Lids)									
Chip Passivation	Lead Frame/IC Passivation								
	Photonitride			Plasma Nitride			None		
	Pass	Group	Fail	Pass	Group	Fail	Pass	Group	Fail
Plasma Nitride	11	-7-	0	15	-8-	0	11	-9-	0
None	10	-10-	0	0	-11-	0	11	-12-	0

As noted and discussed above, only two groups of devices exhibited catastrophic failure (groups 5 and 11) and these failures were the result of plasma nitride processing before the device saw any environmental or electrical stresses. There were no catastrophic failures of any devices in any group due to the accelerated test sequence although many devices, in all groups, exhibited marginal failures in certain parameters, principally in the propagation delay time. Discrepancies in pass/fail numbers observed in Tables 2B through 2L can be attributed to device parameters being marginally within specification at one test and marginally out of specification at the next test.

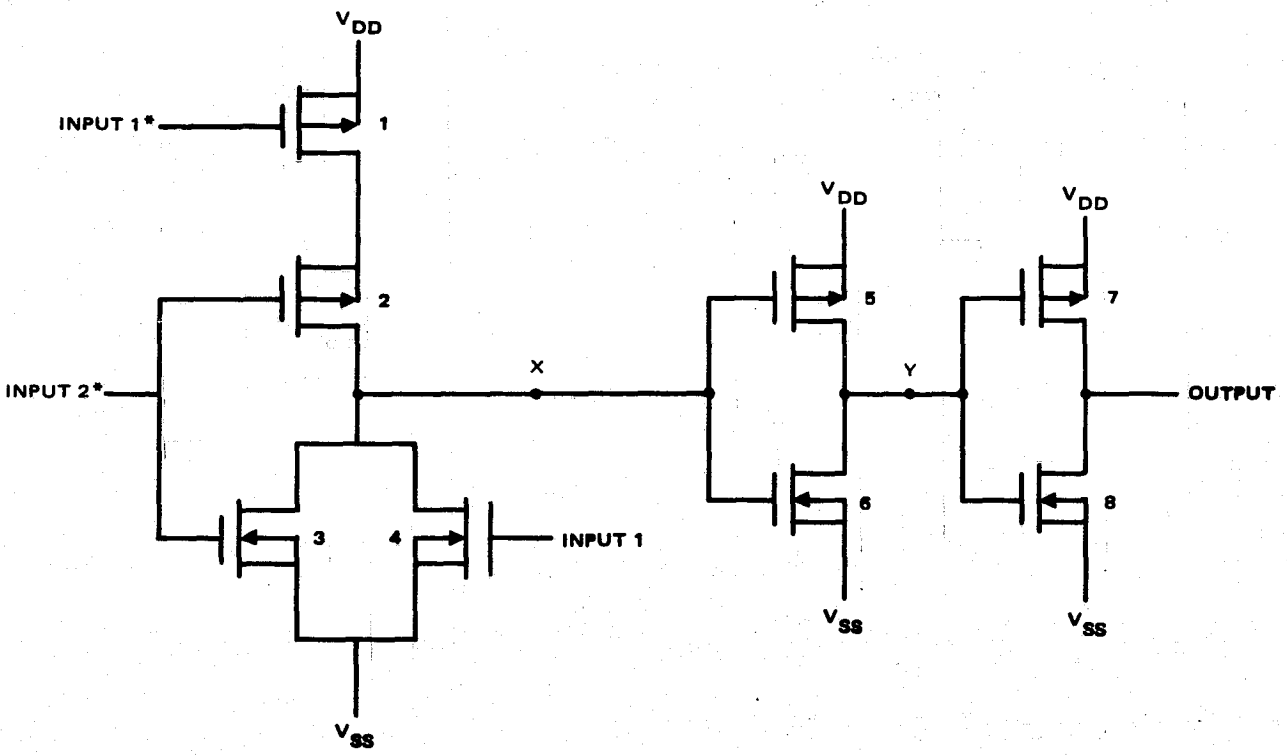
Alternatively, electrical testing of those devices without initial chip passivation which were subject to plasma nitride processing of the wire bonded assemblies revealed 100 percent functional failure for those devices in metal flat packs and greater than 80 percent failure for the plastic encapsulated devices. Thus, as noted above, plasma processing is incompatible with wire bonded circuits which do not incorporate an initial chip passivation. The photonitride process is the only process compatible with wire bonded circuits regardless of initial chip passivation.

2.2 FAILURE ANALYSIS; EXAMINATION AND COMPARISON OF FAILED AND OF GOOD DEVICES BY OPTICAL SCANNER AND BY ELECTRICAL MICROPROBE

Optical scanner examination has revealed significant differences in the photoresponse images from a good device and from a failed device. These differences have been attributed to an anomalous condition in the failed device which causes the n-channel MOSFETs to be permanently biased "ON". The MOSFETs in question are labeled 3, 4, 6 and 8 in Figures 6 and 7 which show a circuit schematic for a typical NAND gate and a photomicrograph of the corresponding section of a CMOS 4001B chip.

Reflected light images of the good and of the failed devices are shown in Figures 8a and 9a. The corresponding photovoltage images from the two devices are shown in Figures 8b and 9b.

Comparison of the photovoltage images of the two devices reveals significant differences. As is appropriate for a good device, the only area that appears in the photovoltage image (Figure 8b) is the p-well diffusion. On the



*INDICATES CONNECTION TO COS/MOS PROTECTION NETWORK SHOWN BELOW

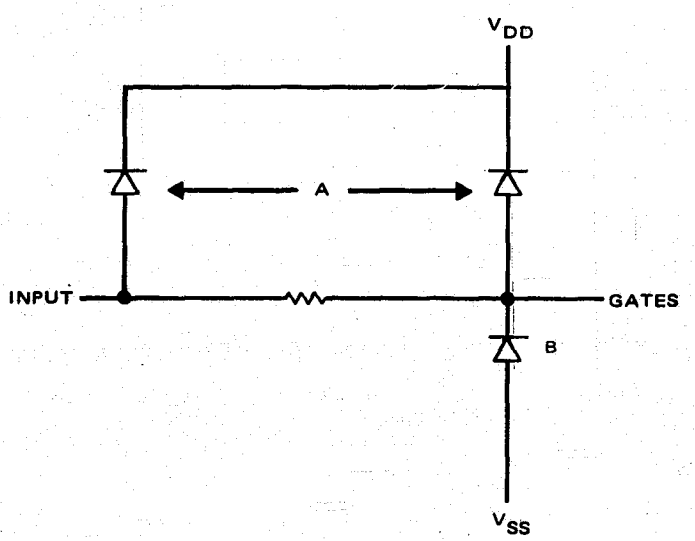


Figure 6. Circuit schematic of a 4001B NAND gate.

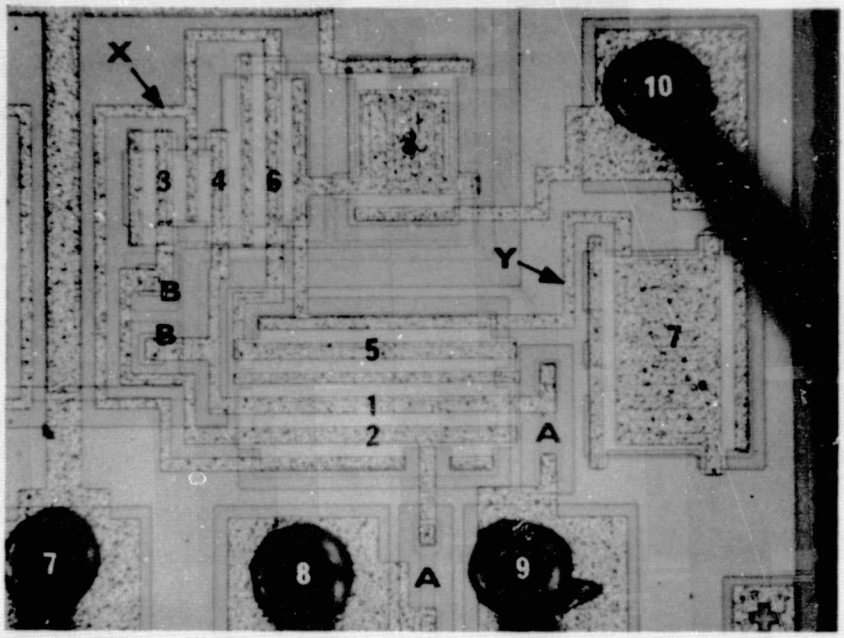
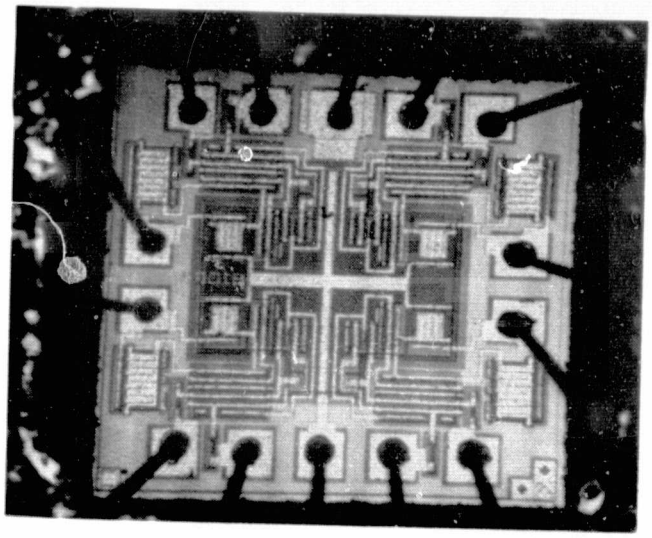


Figure 7. Photomicrograph of a NAND gate on the 4001B chip. Numbers on the bonds are external pin numbers. The numbers and letters on the chip correspond to the numbers and letters on the circuit diagram in Figure 6. Magnification = 115X.

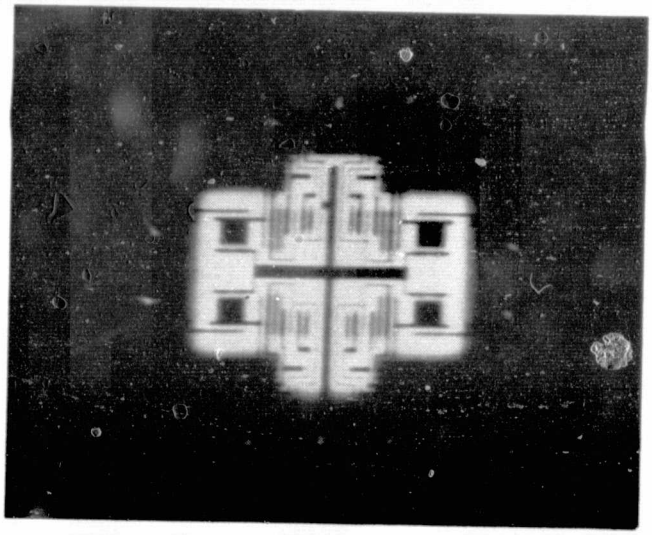
failed device, however, not only does the p-well diffusion appear but also all of the p-channel MOSFETs (Figure 9b). For the set of test conditions employed this implies that the n-channel MOSFETs are "ON" or are in the conducting state in the failed device whereas for the test conditions the MOSFETs should properly be "OFF".

The photocurrent images of the two devices under equivalent bias and input conditions were also significantly different. Figures 8c and 9c show the photocurrent images of the two devices with all of the inputs "low" (0 volts). Figure 8d and 9d show the same images with all of the inputs "high" (five volts). The differences between the photocurrent images again imply that all of the n-channel transistors on the failed device are always in the "ON" or conducting state.

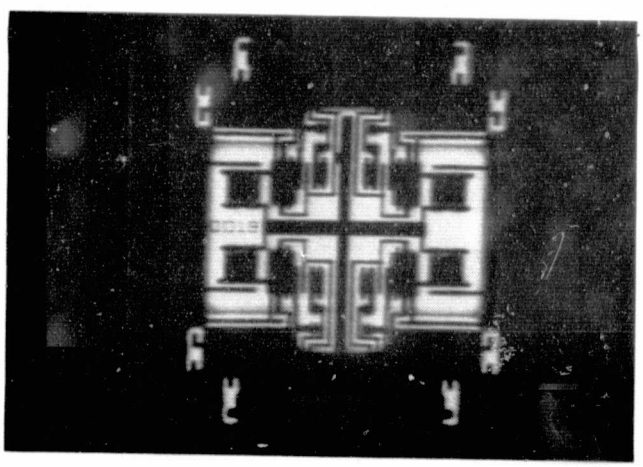
In order to substantiate the conclusion above, points on the device chips were probed while the device was under power in order to determine the voltages present for different input conditions. The two points that were



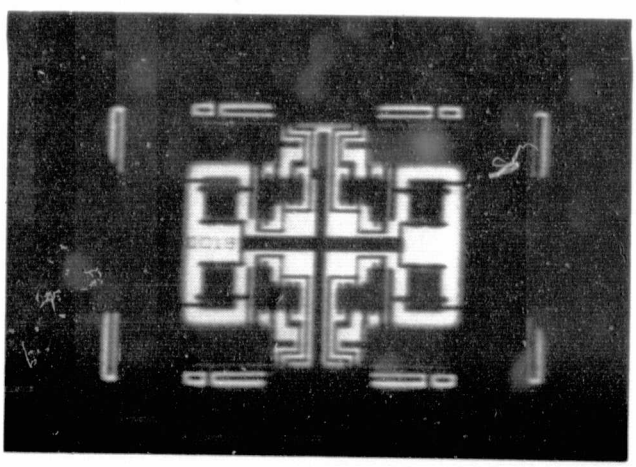
a. Reflected light image.



b. Photovoltage between V_{DD} and V_{SS} leads - no biases applied (all that is imaged is the P-well).

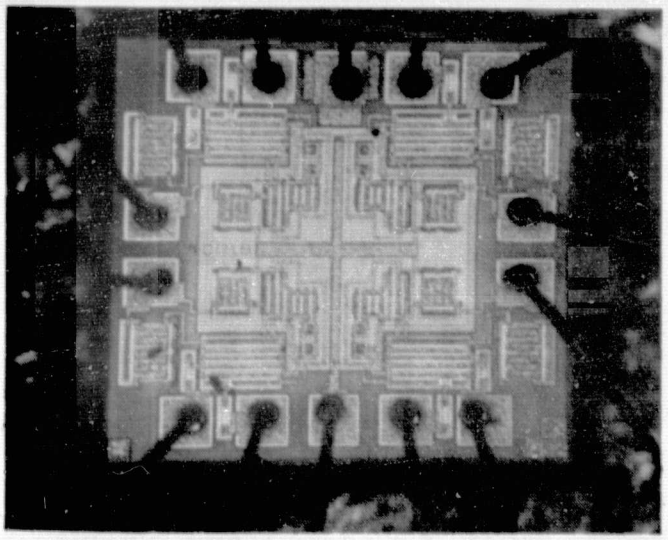


c. V_{DD} = 5V; V_{SS} = 0V = Ground; all inputs = 0V ("LOW"); (Photocurrent induced on ground lead).

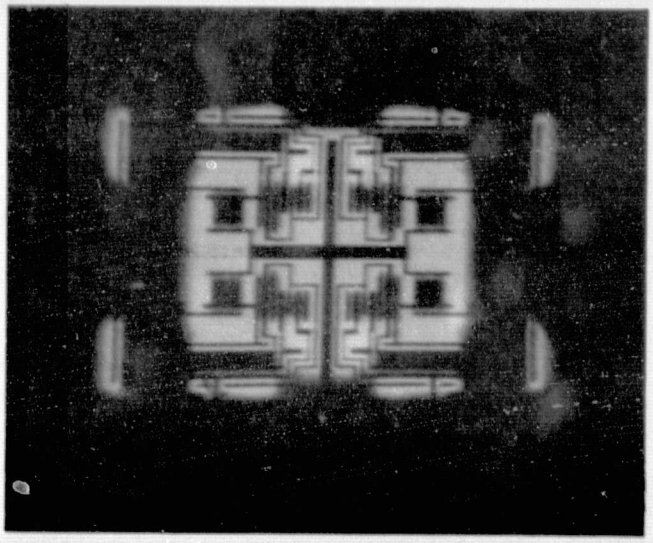


d. V_{DD} = 5V; V_{SS} = 0V = Ground; all inputs = 5V ("HIGH"); (Photocurrent induced on ground lead).

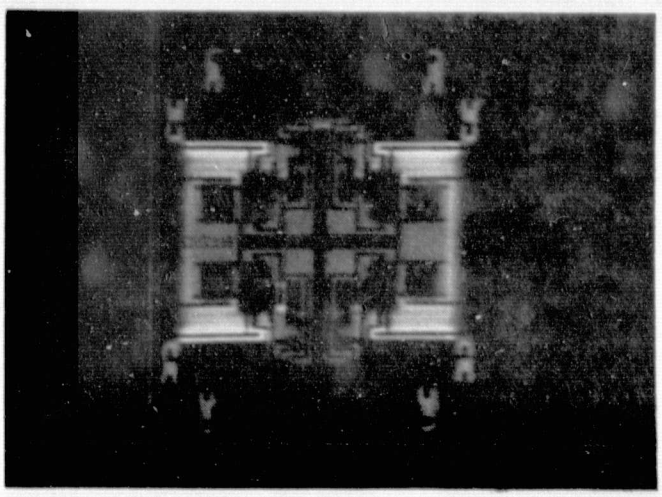
Figure 8. Reflected light image and photovoltage images of a good device obtained on the optical scanner.



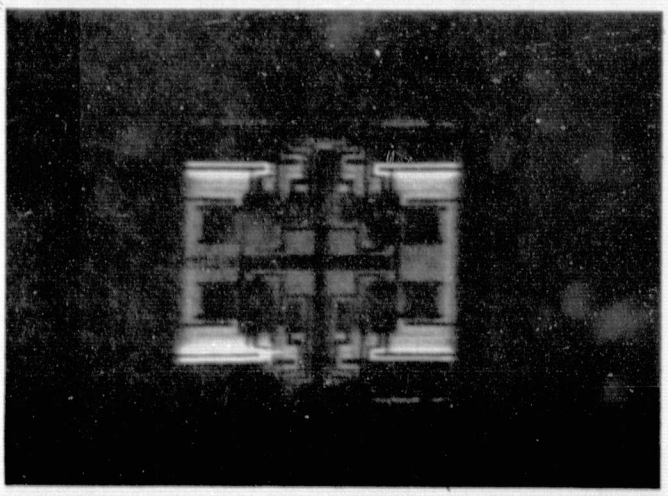
a. Reflected light image.



b. Photovoltage between V_{DD} and V_{SS} leads - no biases applied (the P-well and all P-channel MOSFET's are imaged).



c. V_{DD} = 5V; V_{SS} = 0V = Ground; All inputs = 0V ("LOW"); (Photocurrent induced on ground lead).



d. V_{DD} = 5V; V_{SS} = 0V = Ground; All inputs = 5V ("HIGH"); (Photocurrent induced on ground lead).

Figure 9. Reflected light image and photovoltage images of a failed device obtained on the optical scanner.

probed on each of the NAND gates on each of the two devices are labeled X and Y on the circuit diagram in Figure 6 and on the photomicrograph of the NAND gate in Figure 7.

Results are shown in Table 3. It can be seen that the voltages at points X and Y in each of the NAND gates on the good device are values that are expected for a good device whereas the values from the failed device confirm that the n-channel MOSFETs are always in the "ON" condition.

There is also some evidence that the p-channel MOSFETs on the failed device are not switching completely "ON" when in the conducting state.

The results of the tests above suggest that there is an anomalous positive charge in the surface passivation or trapped in the gate dielectric of the failed device which is most probably an effect of the lead frame plasma nitride passivation process on devices containing chips not previously passivated. The presence of the positive charge causes the n-channel MOSFETs

TABLE 3. VOLTAGES OBTAINED FROM ELECTRICAL MICROPROBE INVESTIGATION OF GOOD AND FAILED DEVICES

"Good" Device				
NAND Gate	All Inputs = 5V		All Inputs = 0V	
	X	Y	X	Y
No. 1	0.0V	5.0V	5.0V	0.0V
No. 2	0.0V	5.0V	5.0V	0.0V
No. 3	0.0V	5.0V	5.0V	0.0V
No. 4	0.0V	5.0V	5.0V	0.0V
Failed Device				
NAND Gate	All Inputs = 5V		All Inputs = 0V	
	X	Y	X	Y
No. 1	0.0V	2.6V	0.3V	0.6V
No. 2	0.0V	1.1V	0.3V	0.4V
No. 3	0.0V	0.7V	0.4V	0.4V
No. 4	0.0V	0.9V	0.3V	0.3V

to be permanently biased "ON" and also results in the failure of the p-channel MOSFETs to turn completely "ON" with the usual applied biases.

An effort was made to detect contamination on the failed device using the energy dispersive X-ray (EDAX) capability of the Hughes scanning electron microscope (SEM). No contamination was found.

2.3 SELECTED PROPERTIES OF PHOTONITRIDE FILM

2.3.1 Flexibility of Photonitride Films

Results indicate that leads 75 mils in length can be laterally displaced by more than 25 mils at the point of maximum curvature without damage to the nitride film.

In the work leading to the conclusion above, a two by one inch ceramic package containing sixty-eight leads each approximately 75 mils long was assembled and coated with approximately 2500Å of photonitride following standard deposition procedures. The leads were then divided into seven groups which were flexed 0, 5, 10, 15, 20, 25, and 30 mils.

Each group of leads was examined with a scanning electron microscope for evidence of film cracking or other deterioration. Photomicrographs were taken of the least favorable appearing lead and of a typical lead in each group.

No evidence of mechanical damage to any flying lead was observed for flexures up to and including 25 mils. A typical lead flexed 25 mils is shown in Figure 10.

Inspection by SEM indicates that the threshold for cracking lies between twenty-five and thirty mils for flying leads for the geometry of the present test and for 2500Å photonitride films. Three of the six leads flexed thirty mils developed moderate to severe cracking of the nitride film in the vicinity of the bond where the lead experiences the most severe mechanical distortion. Figure 11 shows the lead bond which experienced the most severe cracking and loss of adhesion.

The ability of photonitride films to withstand flexure stresses of the magnitude encountered in this experiment is a good indication of the protection afforded the device upon being subjected to severe mechanical handling or circuit repair procedures.

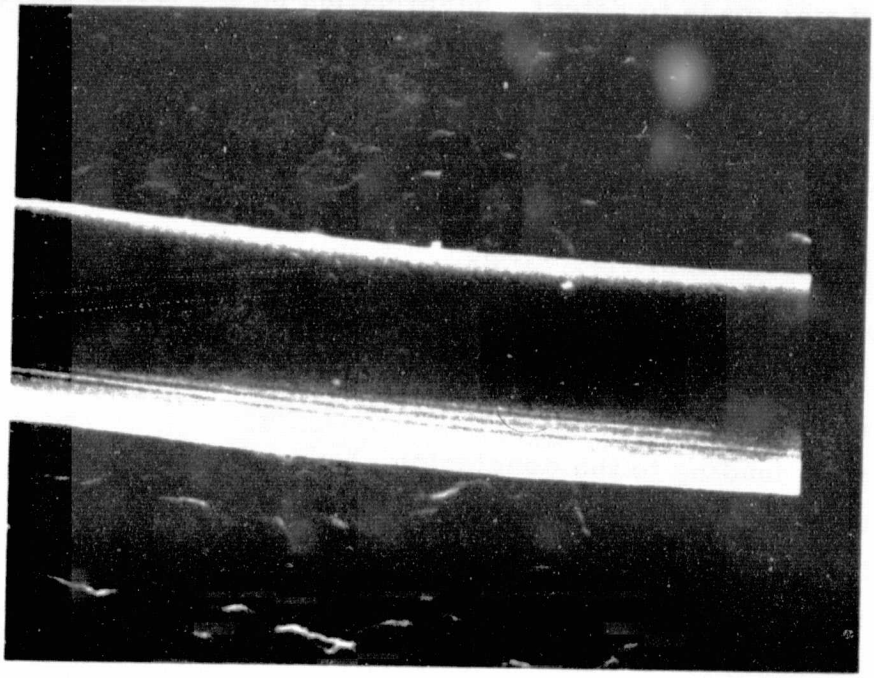


Figure 10. Typical lead flexed 25 mils.

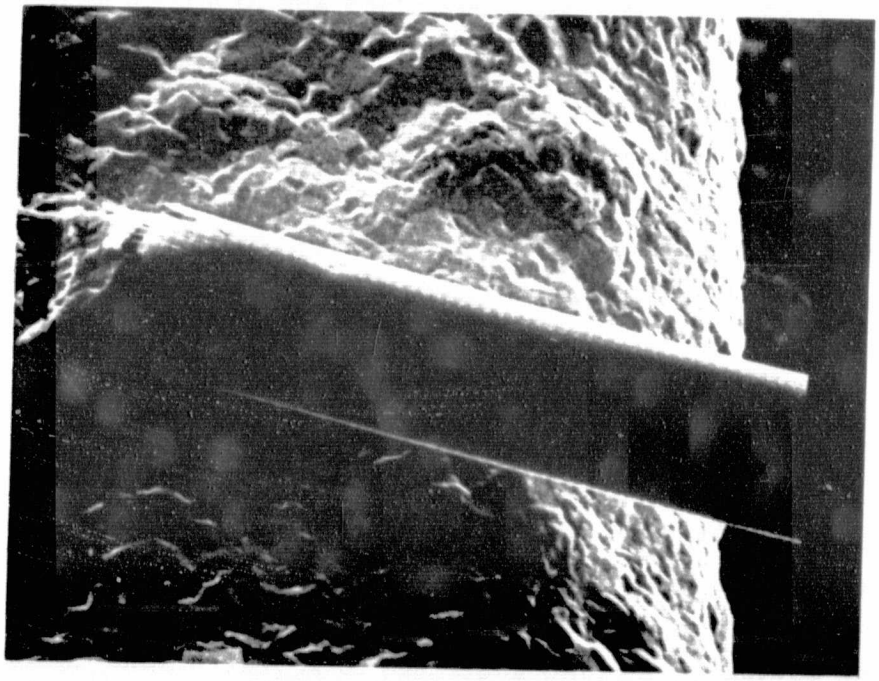


Figure 11. Cracking and loss of adhesion on lead flexed 30 mils. Most severe case.

In work prior to the experiment above a 2 inch by 1 inch ceramic package was assembled with thirty-four 1 mil diameter flying leads bonded between the gold pad and the external terminals of the package. The wire bonded assembly was coated with approximately 2000Å of photonitride in the production reactor operated at standard conditions. The leads were then divided into eight groups and each lead was mechanically stressed by laterally displacing the midpoint of the lead. Displacements of the eight groups were 0, 1, 2, 3, 4, 6, 8 and 10 mils, respectively.

Each group of mechanically stressed leads was examined by scanning electron microscope, photomicrographs being taken of any cracking or deterioration of the film which was observed. In those groups where no mechanical damage to the film was evident, a photomicrograph was taken of the least favorably appearing lead. Thirty-three of the thirty-four leads survived the test very well, showing no evidence of cracking. Pictures obtained from the group flexed 10 mils are shown in Figures 12 and 13. No evidence of cracking was observed even though the die marks on the wire are potential sources of stress concentration when the wire is flexed.

Figure 12. Three of the test leads which were flexed 10 mils. Arrow points to section in Figure 13.

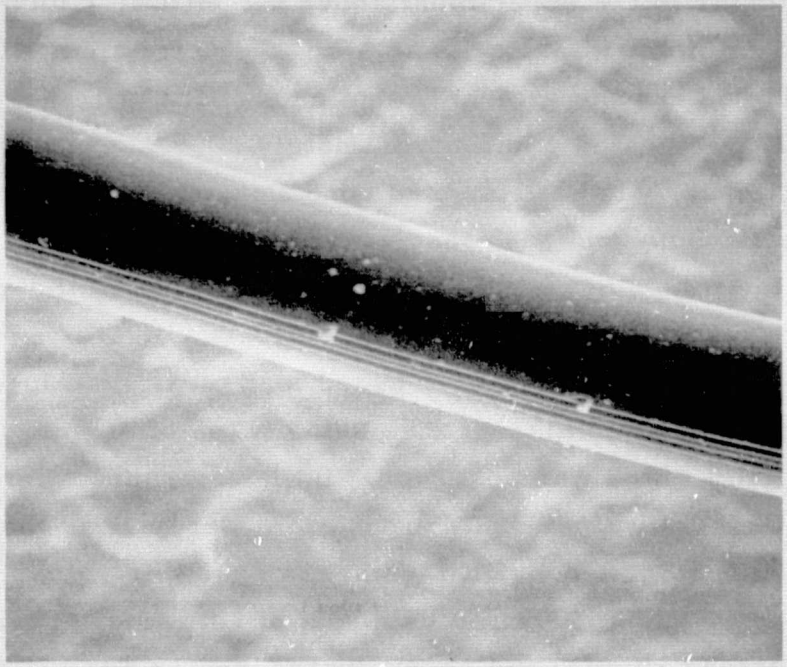


Figure 13. Least favorably appearing of leads flexed 10 mils.

Cracking of the film was observed on only one lead, that coming from the group flexed 4 mils. The evidence from Figures 14 and 15 suggests that the wire may have been stressed more severely than through a mere flexure of 4 mils. It appears from the angular shape of the lead (Figure 14) and from the notch in the lead at the point of cracking (Figure 15), that it was inadvertently hooked and pulled upward, perhaps by the tool used to flex it.

The experiments above were the outcome of observations on photonitride flexibility made on special test circuits consisting of three 2N222 bipolar transistors mounted on an alumina base contained within a 1" x 1" metal flat pack. Approximately 2000Å (0.2μ) of silicon nitride was photochemically deposited on the wirebonded devices. After a total of 100 temperature cycles designed to test the survivability of the bipolar transistors, each of the twelve 1 mil wires shown in Figure 16 were laterally displaced a maximum of five mils at the point of maximum curvature of the wire. SEM examination of the twelve wire bonds on the chip and on the ceramic substrate demonstrated that the photonitride film exhibits a high degree of flexibility.

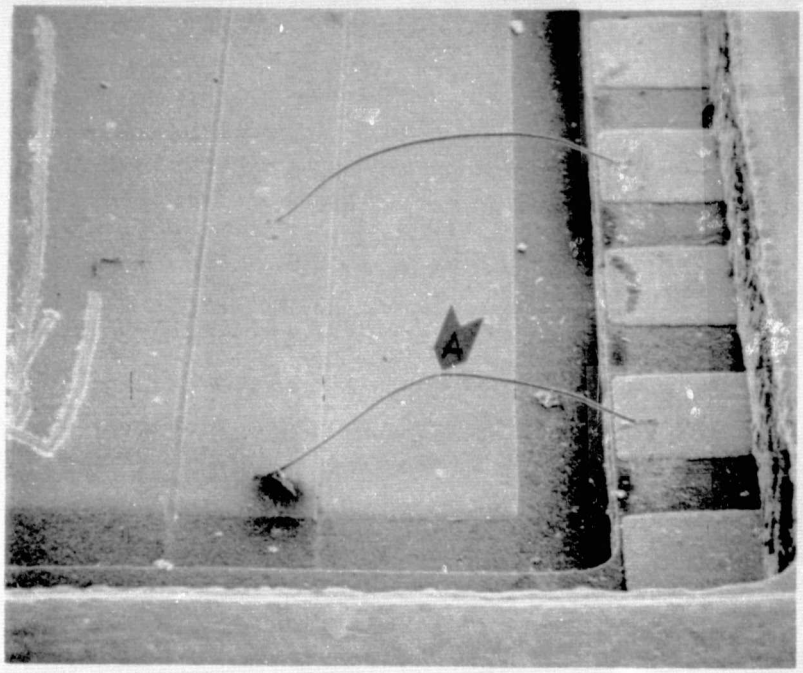


Figure 14. Two leads from group four showing site of probable mechanical damage to lead.

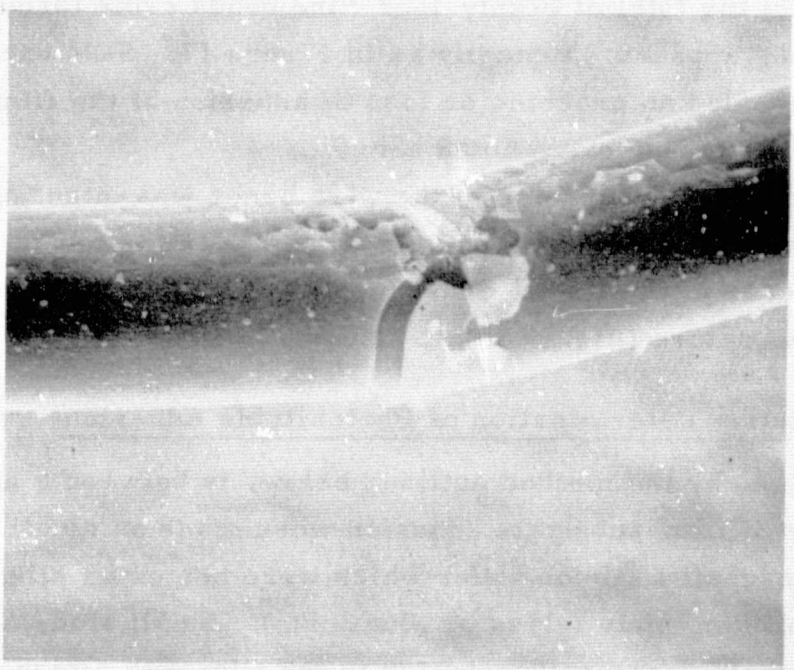


Figure 15. Closeup of damaged area of lead in Figure 14 indicated by arrow.

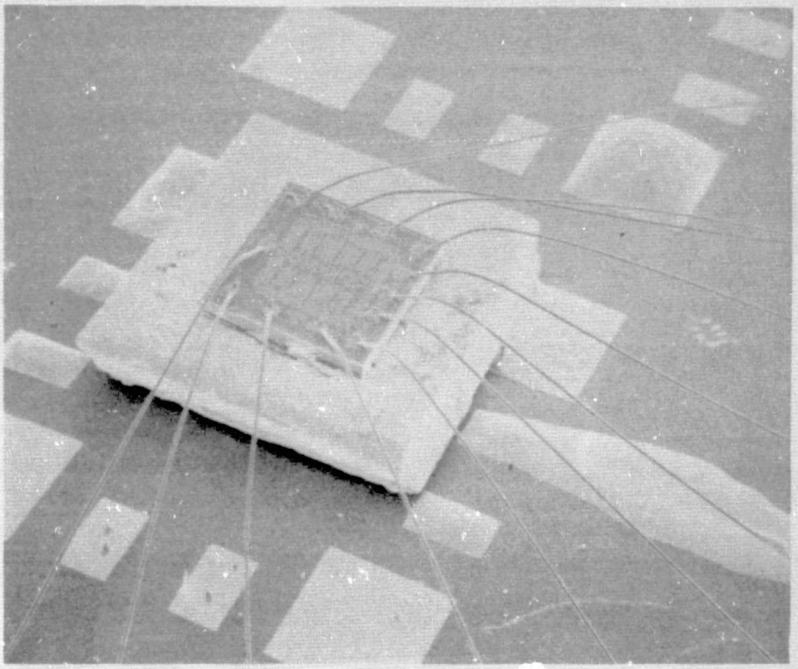


Figure 16. Device used to demonstrate the ability of photochemical silicon nitride to protect hybrid circuits from electrical and mechanical deterioration.

Twenty-three of the total of twenty-four wire bonds came through the flexure test undamaged, appearing typically as in Figure 17. SEM examinations of the devices revealed no cracking or loss of adhesion of the film to the wire bonds except for the one event noted above.

After the tests above one of the wire bonds was intentionally over-stressed so as to induce cracking of the film. Examination by optical microscopy unequivocally reveals the presence of the film on the wire and indicates its thick, dense nature (Figure 18).

2.3.2 Quantitative Determination of Photonitride Adhesion

Adhesion, by the method outlined below, is between 6 and 10 KSI. Measurements of film-substrate adhesion were made on small (1 cm^2) sections of nitride-coated silicon wafer which were cemented silicon side down to a suitable backing plate (glass or aluminum). Small studs (1/2 inch long by 0.110 inch diameter) were cemented to the film with a high strength, low shrinkage epoxy and the resulting tensile specimen was pulled to failure in a tensile tester.

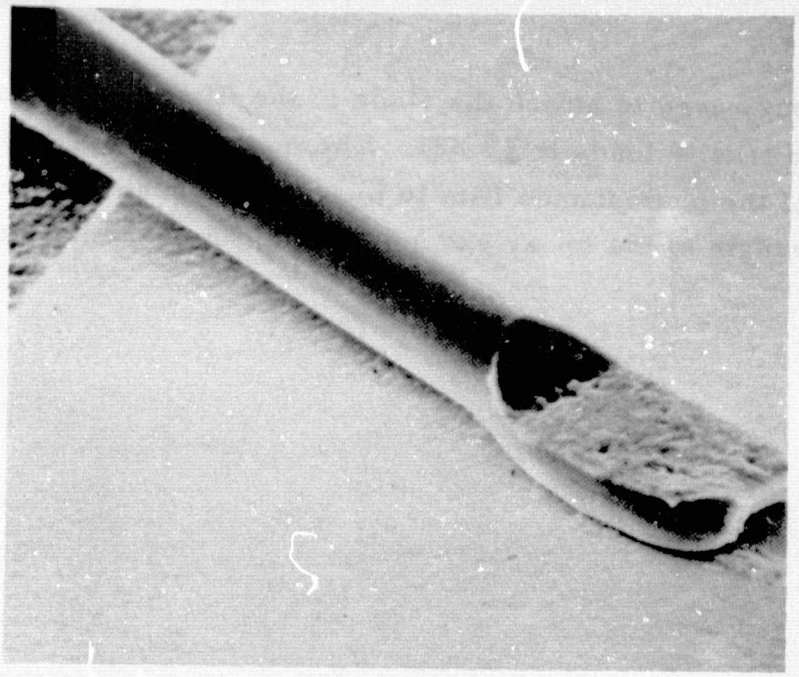


Figure 17. Typical example of coated wire bond after temperature cycling and mechanical flexing (650X).

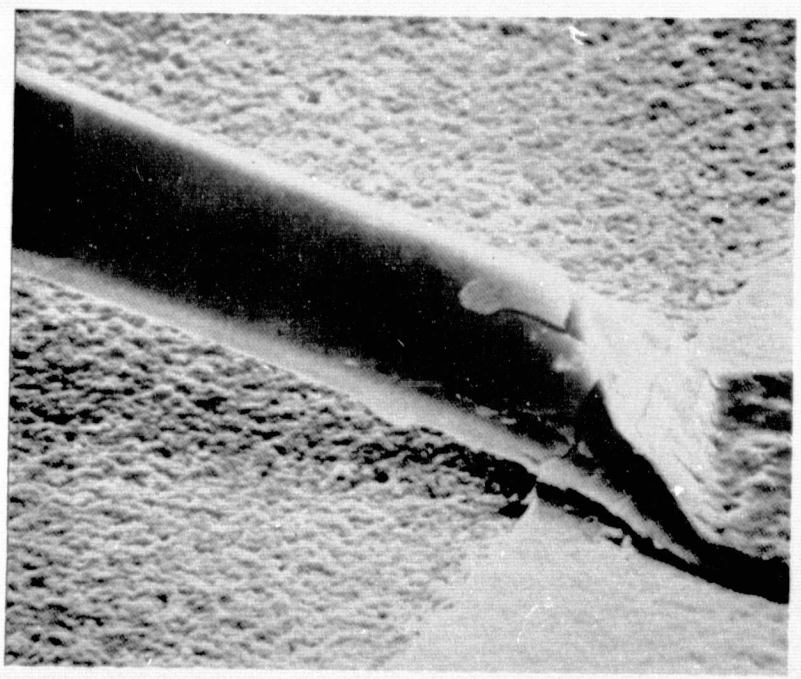


Figure 18. One of 24 wire bonds which exhibited evidence of coat cracking after severe flexing.

The epoxy used to attach the studs to the film will, when properly cured, sustain tensile loads to 10 KSI. The method is useful for measuring the adhesion of the photonitride film to the silicon substrate only so long as the tensile strength of the epoxy exceeds that of the photonitride-silicon interface.

3.0 CONCLUSIONS

The results of the accelerated environmental and electrical tests lead to the following conclusions:

1. Photonitride is compatible with all wire bonded lead frame assemblies tested, with or without initial chip passivation.
2. Plasma nitride passivation of lead frame assemblies is possible only if the chip is passivated before assembly.
3. The survival rate after the environmental test sequence of devices with a coating of plasma nitride on the chip and a coating of either plasma nitride or photonitride over the assembled device is significantly greater than that of devices assembled with no nitride protective coating over either chip or lead frame.
4. The majority of devices with unpassivated chips and with photonitride over the lead frames survived the environmental test sequence.
5. Neither the coated or uncoated devices subjected to the environmental test sequence exhibited any evidence of corrosion.
6. Plastic encapsulated circuits incorporating a photonitride protective coating exhibited the highest survival rate after the accelerated test sequence.

The survival after the application of photonitride to lead frame assemblies of devices with no chip passivation suggests the possibility of simplifying the device fabrication process by eliminating the chip passivation operation. Such a simplification would not be possible if the lead frame assemblies were passivated with plasma nitride.

From the fact that there were no permanent device failures in any of the groups exposed to the accelerated environmental test, including group 12,

it can be inferred that the test sequence was not sufficiently severe to separate the various passivation processes, including that in which no coating was employed, on the basis of the degree of hermiticity given to the device. Based on the results of the feasibility study, a comprehensive follow-on program is recommended. This program is discussed in Section 4.0.

4.0 RECOMMENDATIONS

Based on the results of the feasibility study and the apparent superiority of the photonitride process for the passivation of lead frame assemblies compared with plasma nitride, a follow-on program is recommended. The recommended production-oriented program will encompass an evaluation of 5000 devices (2500 CMOS and 2500 Op Amps) which have been subjected to plasma or photonitride protection of the lead from assemblies (a control group will be uncoated) prior to plastic encapsulation. A significantly more severe environmental test sequence is recommended to bring about corrosion of the metallization and wire bonds of the uncoated devices. No evidence of corrosion was exhibited by any of the devices (protected or unprotected) in the feasibility study. Devices which incorporate aluminum wires will be processed, if possible, to enhance the probability of corrosion of the unprotected devices.

The results of the feasibility study convincingly demonstrated that plasma processing of lead frame assemblies was not compatible with unpassivated chips. In the new program unpassivated chips have been eliminated from the processing structure and chips with either plasma nitride or PSG (glass) passivation will be evaluated with the photonitride and plasma nitride processing of the lead frame. This will represent the first evaluation of photonitride and plasma nitride processing of lead frame assemblies with chips passivated with P.S.G. The recommended device processing matrix and schedule of environmental tests for the new program are summarized in Tables 4 and 5.

TABLE 4. RECOMMENDED PHASE II DEVICE PROCESSING MATRIX

Chip Passivation	CMOS/Plastic DIP					
	Lead Frame/IC Passivation					
	Photonitride		Plasma Nitride		None	
	Group No.	Quantity	Group No.	Quantity	Group No.	Quantity
Plasma Nitride	1	400	2	400	3	400
Vapox	4	400	5	400	6	400
	Linear/Plastic DIP					
Chip Passivation	Lead Frame/IC Passivation					
	Photonitride		Plasma Nitride		None	
	Group No.	Quantity	Group No.	Quantity	Group No.	Quantity
Plasma Nitride	7	400	8	400	9	400
Vapox	10	400	11	400	12	400

TABLE 5. RECOMMENDED PHASE II ACCELERATED ENVIRONMENTAL TEST SCHEDULE

Test Condition	Device Quantities (Total - 400/group)				
	50 Cycles				250 Cycles
1. Temperature Cycling -55 to 125°C	80	80	80	80	80
2. Humidity a. 85°C/85%R.H. EM: 50, 100, 250, 500 hours	80				
b. Moisture Resistance 25-65°C/90%R.H. EM: 50, 100, 250, 500 hours		80			
c. Bias/Humidity at 85°C/85%R.H. EM: 50, 100, 250, 500 hours			80		
3. Reverse Bias a. HTRB at 125°C EM: 50, 100, 250, 500 hours	40	40	40	40	
b. Room Temp. Rev. Bias EM: 50, 100, 250 500 hours		40	40	40	40

EM = electrical measurements