HIGH EFFICIENCY CELL GEOMETRY

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SUMMARY

A new silicon solar cell is described which has an array of small-area conduction paths to transport current directly through the wafer to metal electrodes on the back. This design eliminates grid shadowing and many of the other losses inherent in conventional cells. Early experimental units without texturing or antireflection coatings have shown 13.3% efficiency under AM1 insolation.

INTRODUCTION

The front surface grid of a conventional solar cell causes losses in efficiency due to shadowing and series resistance along the grid lines. Furthermore, it requires high-resolution patterning and yields a non-planar front surface. These problems are eliminated in the "Polka Dot Cell" described below in which the current collected at the front junction is carried through the cell via an array of small-area interconnects to a junction of the same type which covers most of the rear surface.

DESCRIPTION

The geometry of this cell is shown in figure 1, which illustrates the N^+P configuration. The cells are made by patterning the backs of <100> silicon wafers and anisotropically etching to produce pyramidal indentations which barely penetrate through the front surface. The wafer is diffused to produce a thin N^+ junction on the front surface and a deeper one over the back except for areas which are masked and ion implanted P^+ to make contact with the substrate. The cell is completed by depositing metallization over the entire back of the cell and patterning it to separate the N^+ and P^+ contact areas. The front can be textured and AR coated to reduce reflection losses.

The power delivered by the cell, expressed as $P = I_{sc}V_{oc}f$, is expected to be increased relative to that of a conventional cell through improvements in each of these cell coefficients. The short-circuit current I_{sc} will be increased by elimination of grid shadowing. A larger open-circuit voltage V_{oc} due to improved emitter efficiency is expected through elimination of the $S = \infty$ boundary condition that would exist under a metallized grid area. The

absence of junction degradation caused by impurities coming from the grid metallization should further increase both of these parameters. The rear junction is made deep enough to avoid such degradation.

The fill factor f is mainly determined by the product R_sA, where R_s is the series resistance of the cell and A is its area. R_s has two principal components, one caused by spreading resistance in the front N^+ region around the interconnect openings, and the other associated with lateral current flow in the substrate.

SERIES RESISTANCE ANALYSIS

The spreading resistance can be evaluated by imagining the cell to be divided into squares of side "a" surrounding each interconnect opening, as illustrated in figure 2. These openings are squares of side "b". We will approximate the performance of this subcell by that of a circular cell of the same area, so its inner and outer radii are $b/\sqrt{\pi}$ and $a/\sqrt{\pi}$ respectively. We assume that photocurrent density J is generated uniformly over the surface of the subcell and flows radially inward to the interconnect opening through the N^+ layer which has a sheet resistance $\rho_\square$. R_s will be evaluated by expressing the power lost in the N^+ region in the form, $P = I^2R_s$. The power dissipated in each circular zone of length dr is caused by photocurrent collected in the annular area outside r, so the total power lost in each subcell is given by

$$P = \int \left[\pi J \left(\frac{a^2}{\pi} - r^2\right)\right]^2 \frac{\rho_\square dr}{2\pi r}$$

$$= \frac{\rho_\square J^2 a^4}{2\pi} \left[\ln \frac{a}{b} - \frac{3}{4} + \frac{b^2}{a^2} - \frac{b^4}{4a^4}\right]$$

from which R_s can be evaluated. Multiplying by a^2 to get the R_sA product, we find

$$R_sA \approx (\rho_\square a^2/2\pi)[\ln(a/b) - 3/4]$$

To indicate the magnitude to be expected for this resistance loss, we take a 0.6 mm (appropriate for a 200 μ thick cell), a/b = 20, and $\rho_\square$ = 200 ohm/square, which gives R_sA = 0.26 ohm-cm^2. This loss would reduce the output of a silicon cell by less than 2%.

The loss due to current flow in the substrate can be calculated similarly. For a wafer of thickness t and resistivity ρ having an array of parallel line contacts a distance d apart, we find

$$R_sA = \rho d^2/12t$$

Substrate contacts could conveniently be placed between every other interconnect row, giving d = 2a. However, for initial experiments we have chosen to omit every 8th row and place the contacts there, corresponding to d = 8a. For a wafer resistivity of 0.25 ohm-cm this gives R_sA = 0.24 ohm-cm^2.

The combined effect of these two R_s components would be to reduce the fill factor from its ideal value of 0.83 to 0.80, assuming V_{oc} = 0.6 volts and J_{sc} = 40 mA/cm^2.

EXPERIMENTAL RESULTS

Early experimental cells have been made by T.J. Soltys of this laboratory in both the N^+P and P^+N configurations. Cells made without texturing or antireflection coatings have shown J_{sc} = 29.3 mA/cm^2, V_{oc} = 0.588 volts, and f = 0.77 under 100 mW/cm^2 of AM1 illumination, corresponding to a conversion efficiency of 13.3%.

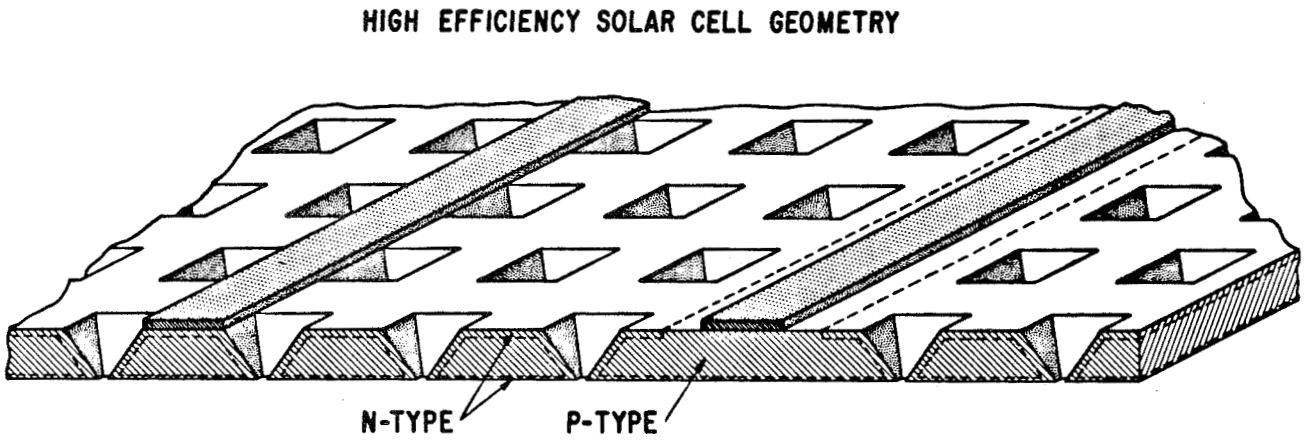

Figure 1. Cross-section of the Polka Dot solar cell, shown upside down. The N^+ metallization actually covers most of the back surface of the cell.

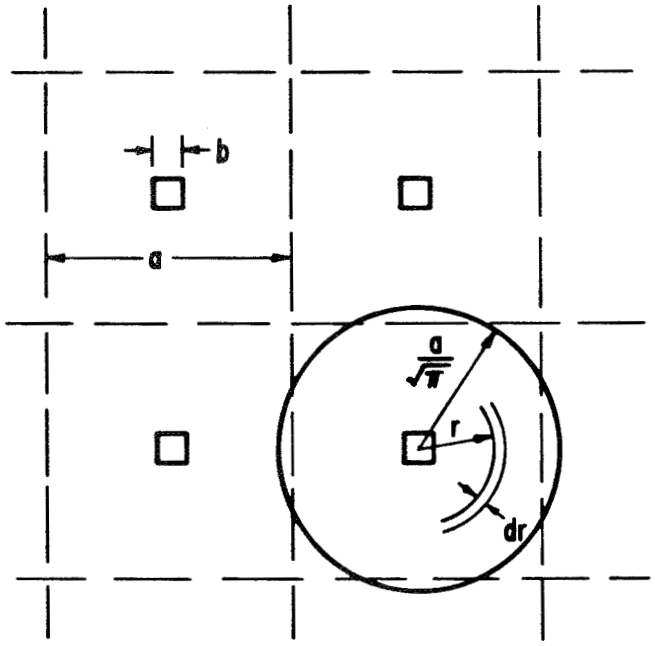

Figure 2. Subcell used for calculating series resistance.