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DIGITAL PSK TO BiØ-L DEMODULATOR FOR 2^N_x(BIT RATE) CARRIER

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SUMMARY

A PSK to BiØ-L demodulator composed of standard digital integrated circuits has been developed for use in the ground support equipment of the Shuttle Bay Environment Measurements (SBEM) experiment. This device is used to change digital PSK modulated PCM data to BiØ-L for decommutation and display during ground tests. In PSK modulation the information is contained in the carrier signal transitions. The demodulator locks onto the carrier transitions to generate NRZ-L data and an associated clock. The NRZ-L is then converted to BiØ-L for further processing. The occurrence of a single "one – zero" data bit pattern is all that is required for the device to become synchronized. Twenty percent jitter or frequency variation in the carrier is allowed before synchronization is lost. The device can easily be adapted to handle various carrier frequencies and PSK rates as long as the carrier is a 2^N multiple of the PCM bit rate. Three demodulators were built for SBEM to accommodate three carrier frequencies.

INTRODUCTION

One of the experiments being developed for the Long Duration Exposure Facility (LDEF) is the Shuttle Bay Environment Measurements (SBEM). The data gathered by this experiment is pulse code modulated (PCM) for recording on magnetic tape. During different data taking periods the recorder is run at different speeds. In order to be compatible with the changing bandwidth of the recorder the data is allowed to digitally phase-shift-key (PSK) a square wave carrier having three selectable frequencies. To test the SBEM experiment a PSK demodulator is needed to convert the data from PSK to BiØ-L for decommutation and display. Because general laboratory instrument demodulators, being quite complex, are costly, and since the PSK carrier and PCM bit rate are fixed for SBEM, a simple dedicated PSK demodulator was designed to perform the necessary conversion. The same basic design was used for all three carrier frequencies and three demodulators were built. This paper describes the basic PSK demodulator and explains how it operates. Adjusting the basic design for different carrier frequencies is also described. One of the demodulators built for SBEM is presented as an example.

OPERATION

Figure 1 is a functional schematic diagram of the digital PSK demodulator.
Figure 2 illustrates the PSK input waveform, internal signals and Bi$\emptyset$-L output
waveform produced when the carrier is four (2^2) times the bit rate. A pair of
one-shots (monostable multivibrator) and a flip-flop perform the PSK to NRZ-L
demodulation function. The remainder of the circuit is used to produce and
synchronize the bit clock and then convert the NRZ-L to Bi$\emptyset$-L. The one-shots
are connected to the input, one triggering on rising edges (i.e., low to high
transitions), the other on falling edges (i.e., high to low transitions) of the
input. The one-shot output pulse widths (t) are set to 3/4 of the expected
carrier period (T). The one-shots are cross coupled through their reset inputs
so that if an input transition causes either one-shot to pulse, a transition
1/2 a period later is ignored. As can be seen in Figure 2 for a "one - zero"
or "zero - one" bit pattern there is no transition at the data bit edge. This
allows enough time (a whole period) to pass so that the pulsing one-shot's
output can return to normal. The next transition is a function of the data bit
value. Thus by detecting which one-shot is pulsed, the value of the data bit
is determined. The one-shot outputs, Q0 and Q1, are connected to the set (S)
and reset (R) inputs of a flip-flop (FF1) for this purpose. The output of the
flip-flop is the NRZ-L representation of the data contained within the input
signal. This process results in a 1/2 carrier period delay in the formulation
of the NRZ-L signal. The demodulator should theoretically tolerate up to $\pm25\%$
jitter or frequency variation in the carrier before the one-shots make incorrect
indications. Any jitter or frequency variation in the carrier will be reflected
to some degree in the demodulator output.

To generate the clock to go with the NRZ-L data, a binary counter is used. The
modulus of the counter is selected to be the number (2^N) of carrier cycles
within a PCM bit period. This use of a binary counter requires the carrier to
be a 2^N multiple of the bit rate. If NRZ-L is all that is required from the
demodulator, the 2^N restriction can be removed. The one-shot outputs are "OR"ed
by gate G1 to produce the clock (CCK) for the counter. This clock period is the
same as that of the carrier. Since the counter performs a divide by 2^N
function, the Nth output Q_N of the counter is the bit rate clock BTCK. In order
to synchronize the counter (bit rate clock) to the NRZ-L bit edges, a reset
pulse (RST) is generated at every "one - zero" bit transition. FF2 is used to
create an NRZ-L signal delayed by the one-shot pulse width. This delayed NRZ-L
signal QA is "AND"ed with the inverse of NRZ-L by gate G2 to provide a reset
pulse.

Bi-phase data Bi$\emptyset$-L is produced from the NRZ-L and clock using a conventional
AND-OR gating technique. Since this technique may create "glitches" at the bit
edges, a flip-flop (FF3) is included prior to output. The Q_{N-1} counter output
is used to clock this final flip-flop. This produces an additional 1/4 bit
delay in the deglitched bi-phase output Bi$\emptyset$-L. If Bi$\emptyset$-L is not required, G3-5
and FF3 are not required.

EXAMPLE

Figure 3 is a schematic diagram for a 2^2 PSK demodulator built for SBEM. For the SBEM application a line receiver is used at the input and a line driver at the output. The demodulator is composed of a CMOS dual one-shot, 5 TTL integrated circuit packages and several discrete components on a standard wire wrap board. The PCM bit rate for this application is 14×10^3 bits/sec and the carrier frequency is 56×10^3 Hertz which is 2^2 times the bit rate. The carrier period is $1/(56 \times 10^3)$ or 17.9×10^{-6} seconds. So the one-shot pulse widths are set to approximately 13×10^{-6} second. During checkout this demodulator stayed synchronized for carrier frequencies ranging from 39×10^3 to 70×10^3 Hertz, a greater than ± 20 percent variation.

CONCLUSION

A PSK to Bi∅-L demodulator has been constructed using standard digital integrated circuits. The demodulator produces NRZ-L, bit clock, and Bi∅-L outputs from digital PSK input signals for which the carrier is a 2^N multiple of the bit rate. If NRZ-L is all that is required, a carrier which is any multiple of the bit rate can be accepted. Various carrier and bit rates can be accommodated by changing various component values within the demodulator. A ± 20 percent jitter or frequency variation in carrier can be tolerated before the demodulator loses synchronization. The unit was built for digital inputs but could be used for sinusoidal inputs with the inclusion of a waveshaping circuit at the input.
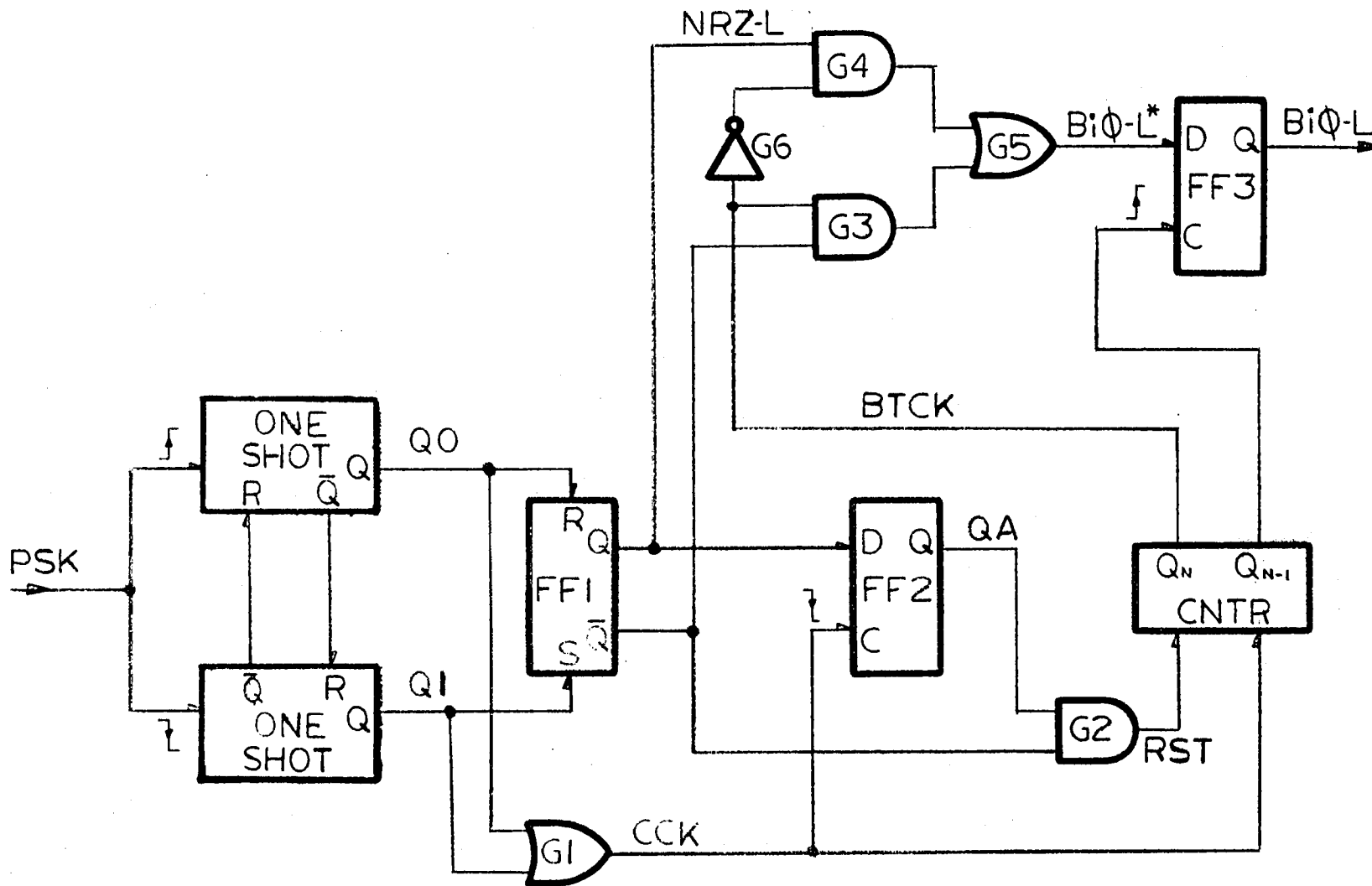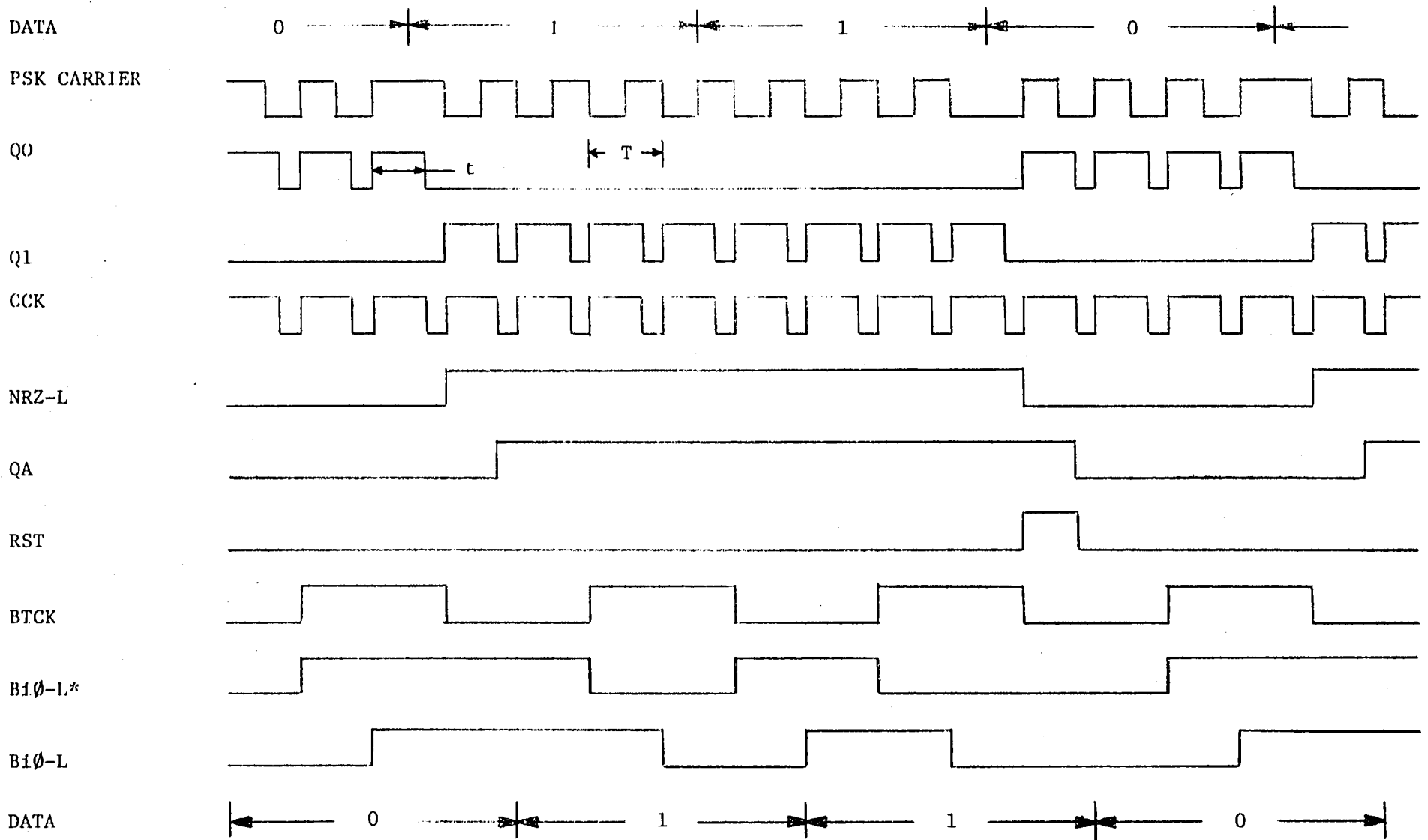
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FIGURE 1 – 2^N PSK DEMODULATOR BLOCK DIAGRAM
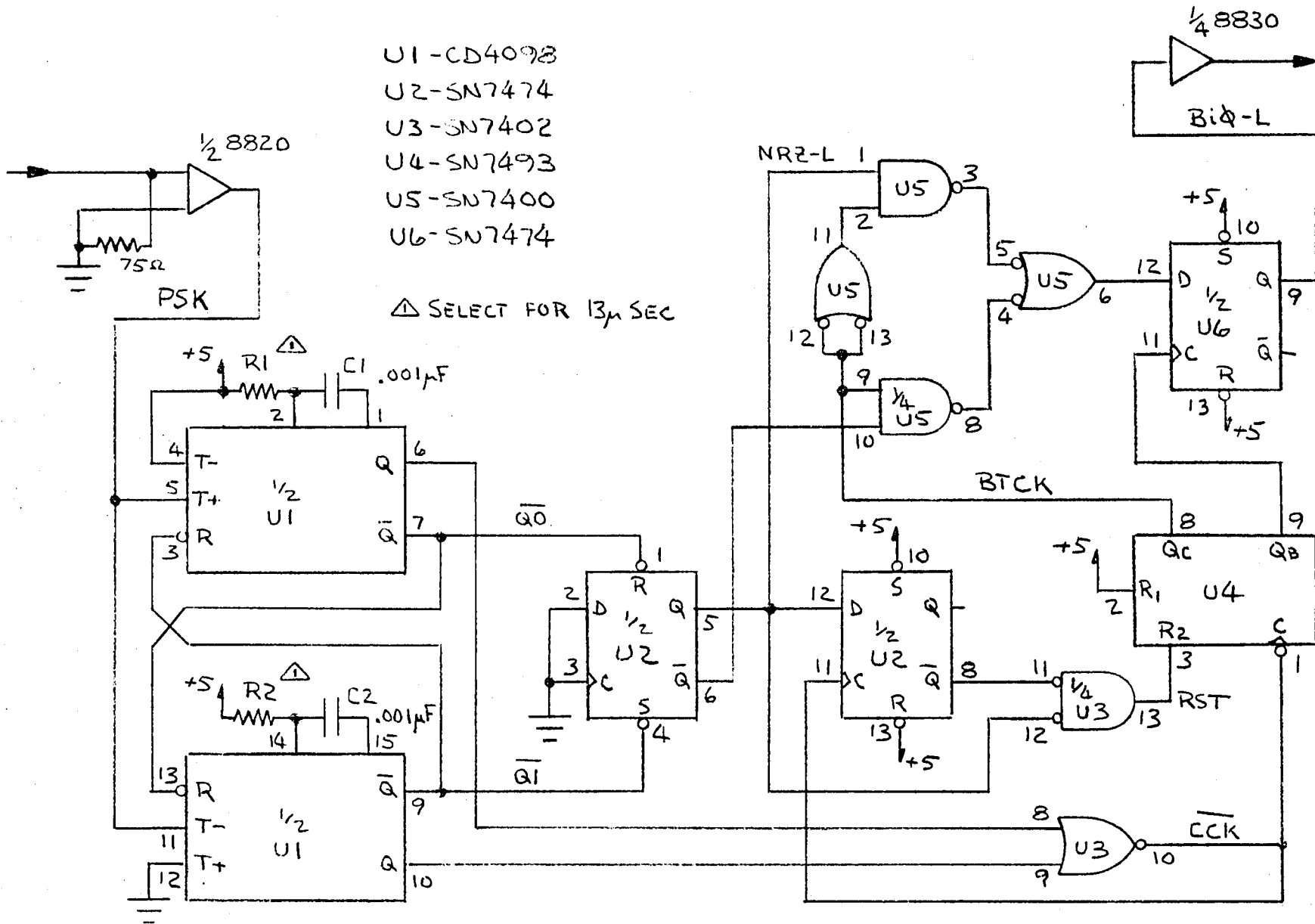
FIGURE 2 – TIMING FOR 2^2 CARRIER

FIGURE 3 - PSK DEMODULATOR 2^2

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15. Supplementary Notes

16. Abstract

A digital demodulator to convert PCM data from PSK to BiØ-L has been developed for ground support applications. The demodulator is composed of standard integrated logic circuits. Up to twenty percent jitter or variation in the carrier frequency can be tolerated without loss of sync. The key to the demodulation function is a pair of cross coupled one-shots which produce NRZ-L. In order to generate BiØ-L the PSK carrier is constrained to be 2^N times the data bit rate. If NRZ-L is all that is required, the circuitry is greatly simplified and the 2^N times bit rate constraint can be removed from the carrier.

A schematic and timing diagram for a 2^2 times bit rate carrier are included. Three demodulators have been built.

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