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LORAN DIGITAL PHASE-LOCKED LOOP AND RF FRONT-END SYSTEM ERROR ANALYSIS

Various experiments have been performed to determine the system error of the DPLLs and RF front-end currently being used in a Loran receiver prototype. This paper documents those experiments and their results.

by

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I. INTRODUCTION

The NASA Tri-University Program at Ohio University is currently involved in developing a low-cost Loran-C navigation system for use in general aviation aircraft.

Presented is the analysis of the system performance of the digital phase-locked loops (DPLL)[1] and RF front-end [2,3] that are currently being implemented in the Ohio University MINI-L4 Loran Receiver. Three of the four experiments deal solely with the performance of the digital phase-locked loops. The last of the four experiments deals with the RF front-end and DPLL system error (i.e., the problems that arise in the front-end due to poor signal-to-noise ratios, and the ability of the DPLLs to track those offsets).

Basic conclusions drawn from these experiments are as follow:

1. The physical parameters of the DPLLs (i.e., board placement on the mother board and chips exchanged among the individual boards) revealed an error of ± 1 micro-second. This error has been proved, in Section V, to be the accuracy of the DPLLs.

2. The addition of monostable outputs[1] to the circuitry within the DPLLs significantly improves the performance of the loops. This was judged upon loop accuracy and performance for a range of signal-to-noise ratios.

3. A high clock offset, driving the DPLLs, will reduce the capability for the loops to operate at low signal-to-noise ratios and also decrease the accuracy of the resulting Loran-C time delays.

4. The DPLLs give a true representation (± 1 micro-second) of the data received from the Loran-RF front-end. Offsets, formerly thought to be injected by the DPLLs, are shown to be created by the RF front-end.

Overall, these tests prove that the DPLLs designed for the MINI-L5 function properly with at least an accuracy of ± 1 microsecond and that the precision of the MINI-L4 Loran Receiver is based upon the precision of the RF front-end.

II. EFFECTS DUE TO CHANGING THE PHYSICAL PARAMETERS OF THE DPLL

A. Purpose. The purpose of this experiment was to see if the inherent differences that exist between similar CMOS chips and the different positions of the DPLL on the mother board[1] effect the time delays derived from the DPLLs.

B. Initial Conditions. The signals used in this experiment were taken off the air, using the 9960 U.S. Northeast Chain. The master and slave assignments were as follow:

Master	M - Seneca
Slave	Y - Carolina Beach
Slave	Z - Dana

Loop No. 1 = Improved loop with the monostable outputs.
Loop No. 2 = Unimproved loop.
Loop No. 3 = Improved loop with the monostable outputs.

Weather - Clear, sunny, and cold.

Loran equipment used: Ohio University MINI-L4 Loran Receiver with the complementary preamp and antenna coupler unit. The receiver's gain control was set to produce the best possible numbers for the known time delays of slaves Y and Z. This gain setting is marked on the face of the MINI-L4 Receiver and is referred to as gain setting number two.

The chips on loop boards No. 2 and No. 3 were marked with one and two dots respectively, so that no confusion would arise when the chips were exchanged between the loop boards.

C. Explanation. The parameters listed under "Initial Conditions" were kept constant throughout the data collection. Data points obtained in the results were procured by taking the mean of thirty time delays that were recorded every other ten GRIs from the MINI-L4 Loran Receiver. The experiment was conducted in the shortest time possible so that ionospheric condition changes could be kept to a minimum.

The parameters that were assigned as variables included loop position on the mother board, loop-chip assignments (components were exchanged chip for chip between the boards), and loop-slave assignments (after a set of data was recorded for a particular set of conditions, the stations assigned to loops No. 2 and No. 3 were switched and another set of data was taken for the otherwise identical parameters).

D. Results. The mean time delay (TD) of each set of thirty TDs can be seen in Table 1. By visual inspection, one can see that the values reveal a deviation error of ± 1 microsecond. The source of this error will be revealed in a later section of this paper.

This experiment proves that no significant error is produced by changing any of the following conditions:

1. The position of the DPLLs on the mother board.
2. Chips on the individual loop boards.
3. Station assignments among the loops.

III. THE EFFECT OF THE MONOSTABLE OUTPUTS

A. Purpose. After the DPLLs were first developed, some problems arose with the length of some critical pulses produced by the internal systems of the DPLL. A method was found by which pulse width control could be obtained by implementing an RC and diode circuit (monostable outputs). The purpose of this experiment was to see what effect these circuits had on the TDs produced by the MINI-L4 Loran Receiver.

B. Initial Conditions. The MINI-L4 Loran Receiver was driven by an Epsco Loran-C Simulator. An interface capacitor of .01 μF was used to simulate an antenna.

	Loop Position	Chip No.*	TDY	TDZ
Loop No. 2	2	1	42593.71	56773.12
"	3	1	42594.86	56773.08
"	2	2	42594.71	56772.98
"	3	2	42594.63	56772.79
Loop No. 3	2	1	42597.90	56774.78
"	3	1	42597.99	56774.41
"	2	2	42597.32	56774.16
"	3	2	42598.01	56774.67
Total Time of Experiment - 1 hour 1 minute				

*1 denotes the single dotted chips and 2 denotes the double dotted chips.

Table 1. Numerical Results of the Physical Parameter Tests.

The simulator and receiver controls were set with these values:

Rate: SS 4 (9960)
ATD: 14115.0
BTD: 26029.0

Signal Reference Level: 100 mV

Noise Level: 100 μV

Signal Attenuation: M - 30 dB
A - 30 dB
B - 30 dB

Receiver Gain Setting: No. 2

Clock Offset: +3 cycles

The time delays were simulated to produce those TDs encountered at Hanscom Field, Massachusetts. This was done as a matter of convenience so that this report could serve as a reference for a future report covering flight data collected in that area.

The 30 dB setting for the simulator signal attenuation was selected as it produced the best representation of an ideal Loran station received from the air.

C. Explanation. The parameters listed under "Initial Conditions", with the exception of Signal Attenuation, were kept constant. Using three loops without the monostable outputs (referred to hereafter as the unimproved loops), thirty TDs were taken at a rate of one TD every other ten GRIs. The thirty TDs were used to produce one mean TD per slave. Then the signal attenuation settings of the master and the A slave (14115.0) were incremented by 2 dB and two more sets of the thirty TDs were collected (one set of thirty for each slave). This process of incrementing the attenuation and collecting data was continued until one of the attenuated loops lost lock. Next, the initial conditions were reset and the entire experiment was rerun with the loops using the monostable outputs (hereafter denoted as the improved loops).

For every set of thirty TDs, a signal-to-noise ratio was taken from the RF front-end of the MINI-L4 Loran Receiver (using test point B).[2,3]

D. Results. The collected data points (1440 TDs) were used to obtain four DPLL characteristic plots, two for the unimproved loops and two for the improved loops. Definitions for the X-Y axes are:

DEVIATION FROM SIMULATED TD (DEV.) - This is the absolute difference between the TD programmed into the Epsco Loran-C Simulator and the mean obtained from every thirty TDs. (Simulated TD) - (Mean of Thirty TDs) = DEV.

SIGNAL-TO-NOISE RATIO (S/N) - This is the absolute ratio between the peak-to-peak voltage levels of the simulated Loran signals and the peak-to-peak voltage levels of the random noise generated by the simulator. These values were read from the RF front-end test point B in the MINI-L4 Loran Receiver using a T922 Tektronix oscilloscope.
(Signal V_{p-p}) / (Noise V_{p-p}) = S/N

SIGNAL-TO-SIGNAL RATIO (S/S) - This is the absolute ratio of the peak-to-peak voltage of Slave B to the peak-to-peak voltage of the Master. This value can be obtained by dividing the S/N of Slave B by the S/N of the Master. Because the noise levels of both stations are equal, the noise-to-noise ratio has a value of one. The S/S is derived from the S/N described above.
$(S/N)_B \div (S/N)_M = S/S$

Figure 1 is a graph of the receiver's deviation from the programmed TDs versus the signal-to-noise ratio. By inspection, it is seen that the improved loops operate over a broader range of S/N and offer better tracking accuracy than the unimproved loops.

Figure 2 is a representation of how the loops operate when the S/N of the master station decreases and the S/N of the slave station (Slave B = 26029.0) remains constant. It is evident that the deviations of both types of loops are approximately the same, but the improved loops show the capability of operating over a broader range of dissimilar signal levels. This characteristic is important as there are very few places in the world that have three Loran-C stations of identical strength.

IV. THE EFFECT OF A HIGH CLOCK OFFSET

A. Purpose. The effects of the high and low clock offsets (+6 cycles and +3 cycles respectively) driving the DPLLs and how those offsets relate to the TDs produced by the MINI-L4 are investigated.

B. Initial Conditions. Loop No. 1 = Loop No. 2 = Loop No. 3 = Improved loop with the monostable output modifications.

All of the initial conditions of Section III hold true with the exception of the clock offset.

C. Explanation. The parameters listed under "Initial Conditions", with the exception of "Signal Attenuation", were kept constant and the clock offset was set to +3 cycles. For each slave, thirty TDs were taken (at a rate of one TD every other ten GRI) to produce one data point (the mean of the thirty TDs). Then the signal attenuation settings of the Master and Slave A (14115.0) were incremented by 2 dB, allowing two more sets of data to be collected. This process was continued until one of the attenuated loops lost lock.

The intial conditions were reset and the clock offset was set to +6 cycles. The process was then repeated exactly as the experiment with the clock offset +3 cycles.

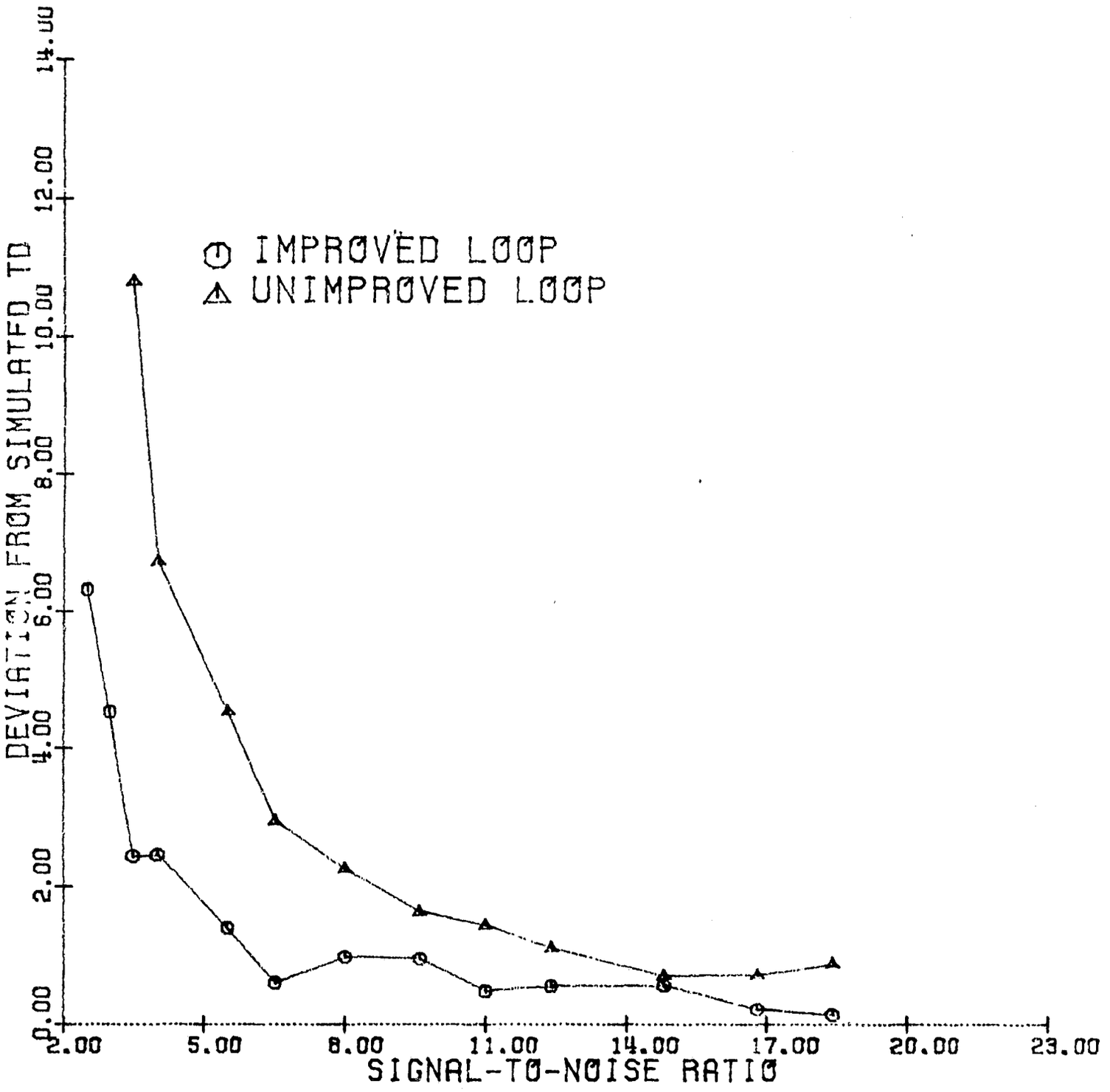

Figure 1. Improved and Unimproved DPLL Characteristic Curves Vs. S/N.

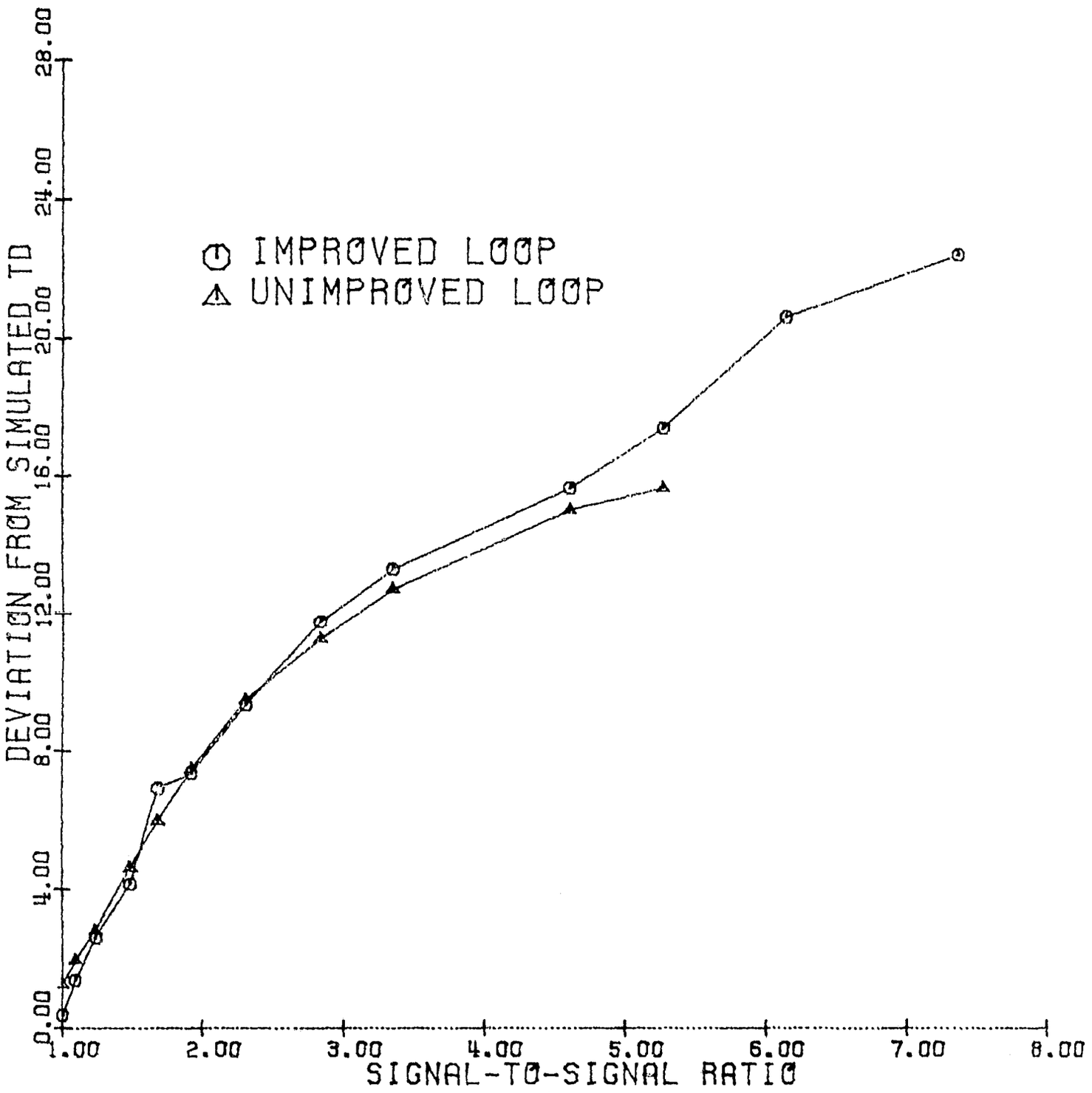

Figure 2. Improved and Unimproved DPLL Characteristic Curves Vs. S/S.

As in the experiments in Section III, signal and noise levels were taken for each set of thirty TDs. The levels were measured from the RF front-end test point B using a T922 Tektronix oscilloscope.

D. Results. The collected data points (1380 TDs) were used to obtain four characteristic curves of the improved loop's performance using two different clock offsets. The definitions of the X-Y axes can be found in Section II, under "Results".

By inspecting Figure 3, it can be seen that the loops operating with the low clock offset offered better accuracy (approximately 1 microsecond better precision) and a slightly wider range of operation with respect to S/N. Figure 4 offers similar results with respect to S/S.

It is important to note that when considering clock offset, the velocity of the receiver system must be taken into account. An offset of +1 microsecond would produce a drift rate of 1 microsecond per second. Since 1 microsecond in Loran equals approximately 750 feet, by simple algebra, the velocity of the Loran receiver system would be limited to about 500 mph. This offset would be well-suited for a general aviation aircraft but not for commercial airline jets whose speeds exceed 500 mph.

V. THE SYSTEM ERROR OF THE DIGITAL PHASE-LOCKED LOOPS AND THE LORAN RF FRONT-END

A. Purpose. Past flight test data has shown that the MINI-L4 Loran Receiver could produce a time delay error up to 19 microseconds. This experiment was conducted to see how much of this error is created by the DPLLs and how much is by the RF front-end.

B. Initial Conditions. The MINI-L4 Loran Receiver was driven by an Epsco Loran-C Simulator. The simulator and receiver controls were set with these values:

Rate: SS 4 (9960)
ATD: 14115.0
BTD: Not Used.

Signal Reference Level: 100 mV

Noise Level: 0 V (Off)

Signal Attenuation: M - 30 dB
A - 30 dB
B - Not used.

Sync: Master (M)

Receiver Gain Setting: No. 2

Loop Clock Offset: +3 cycles

The interface capacitor used to simulate an antenna at the RF input of the Loran Receiver was .01μF.

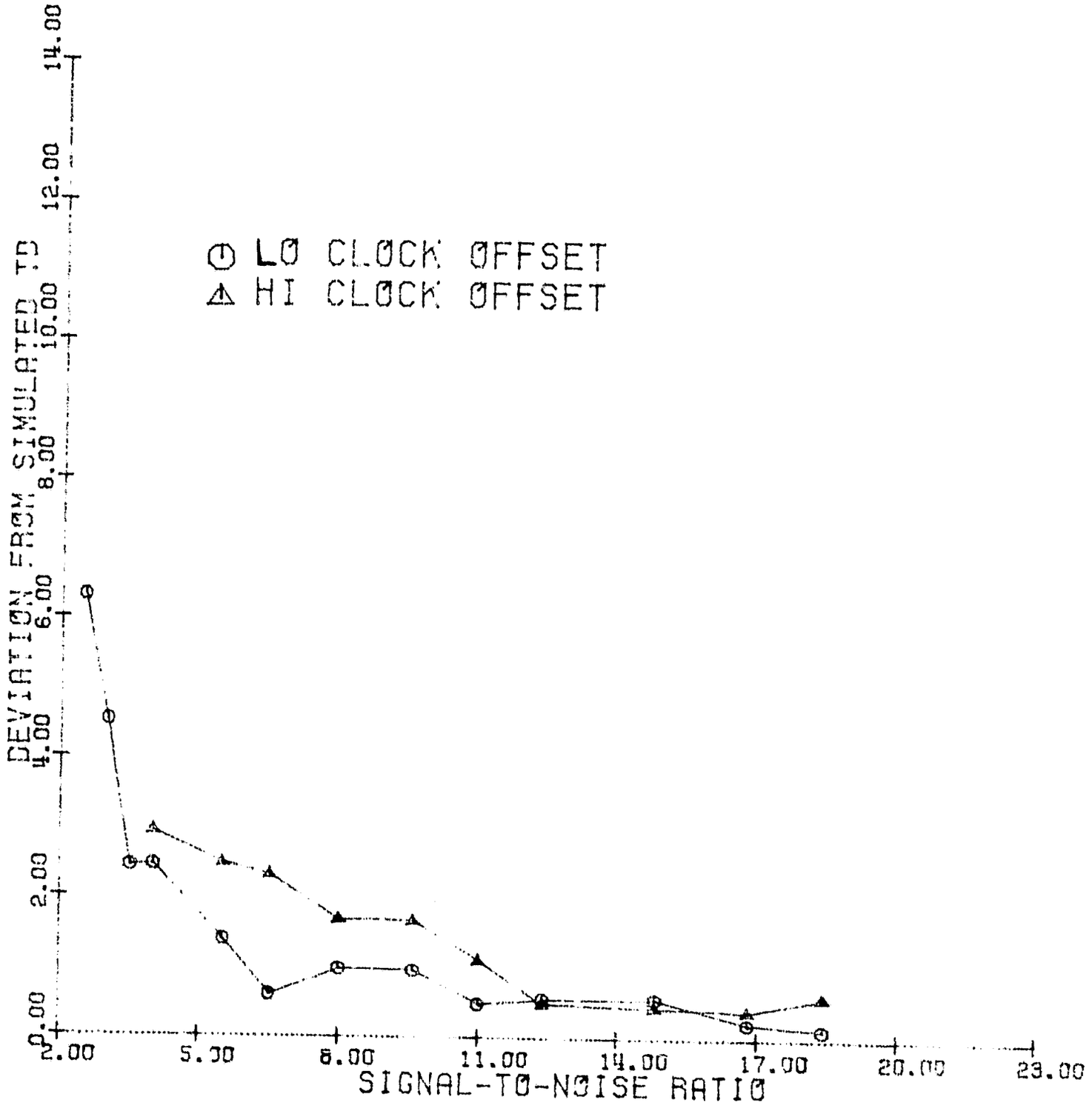

Figure 3. DPLL Characteristic Curves with Different Clock Offsets Vs. S/N.

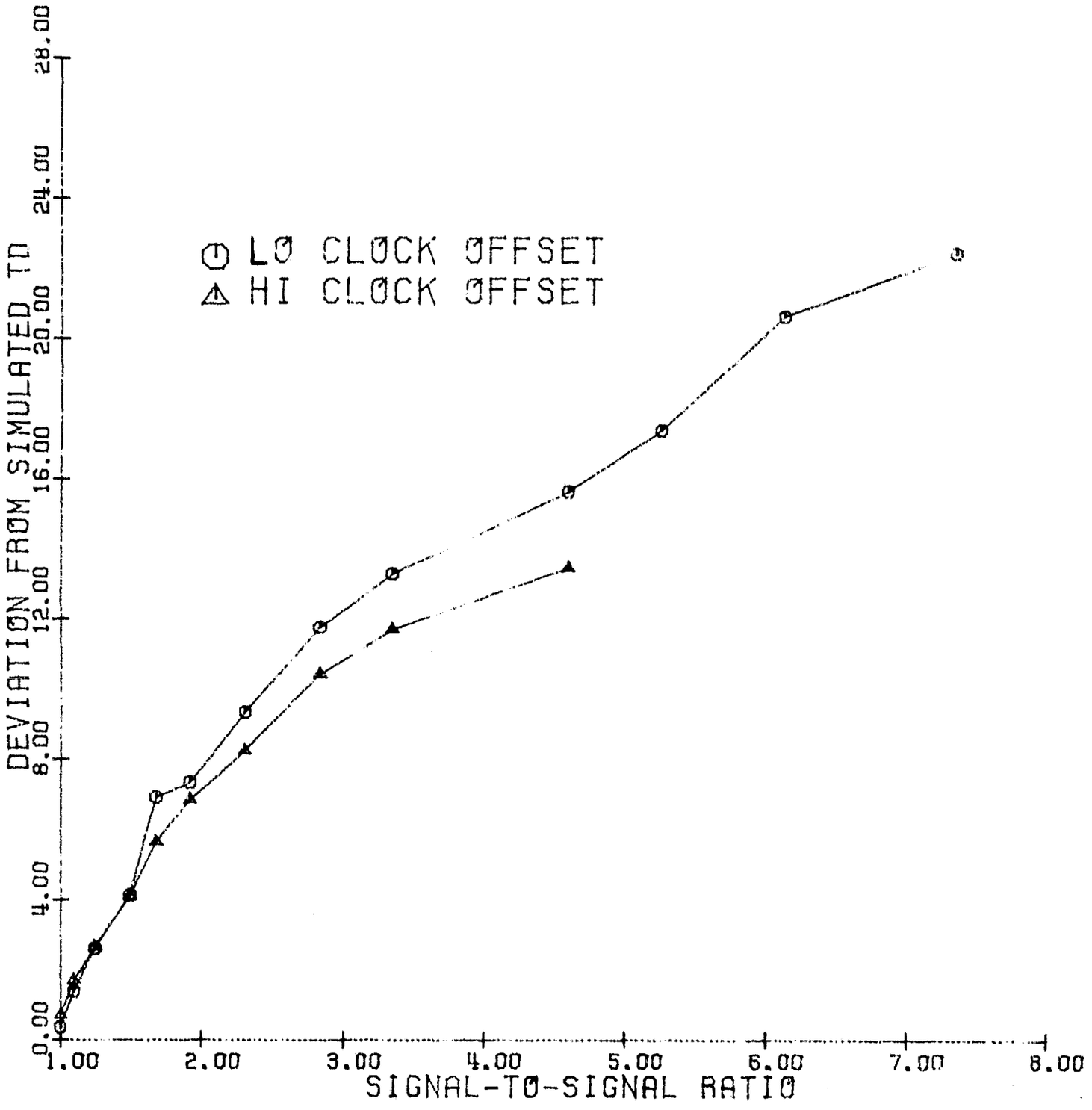

Figure 4. DPLL Characteristic Curves with Different Clock Offsets Vs. S/S.

C. Explanation. All the parameters listed under "Initial Conditions" were kept constant, with the exception of the "Signal Attenuation" of Slave A. Slave A's attenuation setting was incremented by 2 dB for each set of thirty TDs. TD data and signal levels were collected in increments of 2 dB until Slave A lost lock. Since no noise was injected into this experiment, S/S was calculated directly from the recorded signal levels. The mean values of the TDs produced a number of deviations or offsets that could be compared with the offsets recorded from the front-end. This data, compared together, would reveal the amount of offset created by the DPLLs.

The RF front-end ... pulses[2,3], which drive half of the phase detector in the DPLL [1], were monitored with a Tektronix 465 oscilloscope. By using the delay option and the external sync, driven by the sync output of the simulator, the effective deviation of Slave A's IRQ pulse could be measured with respect to the master sync. These deviations and their corresponding S/S could then be compared with the deviations and S/S of the DPLL. (Note: The noise injections had to be eliminated from this experiment so that the deviations of the RF front-end would be well-defined on the oscilloscope.)

D. Results. Figure 5 shows an overlay of the RF front-end and DPLL deviations plotted against signal-to-signal ratios. The signal-to-signal ratio represents the V_{p-p} of the master devided by the V_{p-p} of Slave A. The plot shows that the loops track the RF front-end IRQ pulses with an accuracy of ± 1 microsecond. The plot also shows that as the S/S increases, a considerable offset is produced by the front-end.

VI. CONCLUSIONS AND SUMMARY

The following conclusions can be drawn from the preceding experiments:

1. The DPLLs are capable of tracking the IRQ pulses from the Loran RF front-end with a precision of at least ± 1 microsecond.

2. Changing the physical parameters, listed in Section II, have little or no effect on the TDs displayed by the Loran receiver. The proved tolerance of ± 1 microsecond is the only noticeable error.

3. The addition of the monostable circuit definitely improves the tracking ability of the DPLLs, especially for signal-to-noise ratios greater than 3 (9.54 dB).

4. In the initial stages of testing the DPLL, it was thought that an offset of +5 cycles would offer optimum operation. Clearly, Section IV proves that this is not necessarily the case. The offset of +3 cycles performed better than the +6 cycle offset. It would then appear correct to assume that an offset of +1 microsecond would offer better results, certainly in the case of general aviation. Future tests will have to be performed in order to properly justify this statement.

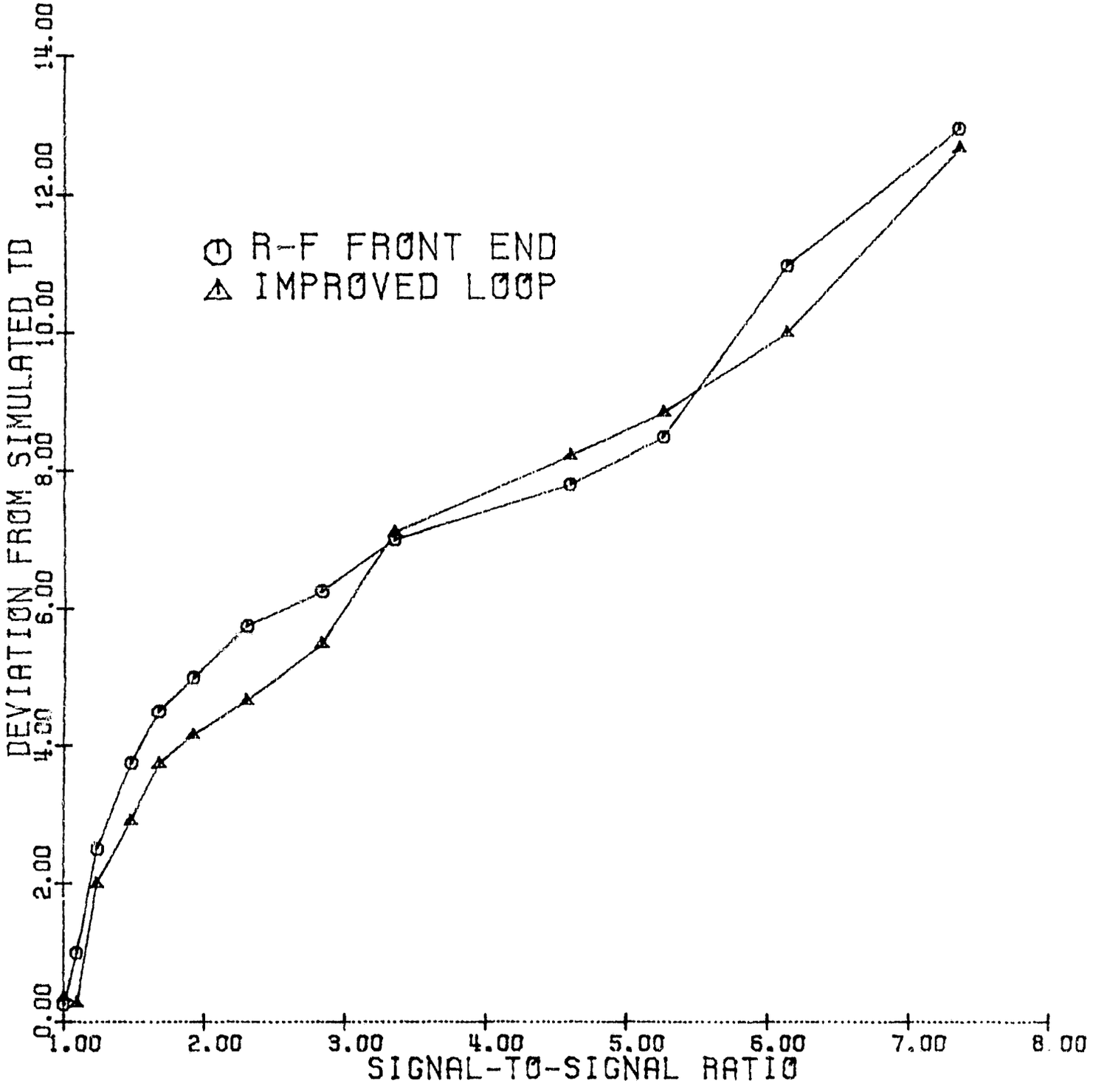

Figure 5. DPLL and RF Front-End Characteristic Curves Vs. S/N.

Section V reveals that there is a definite problem with the current Loran RF front-end. The problem is already being researched by the NASA Tri-University team at Ohio University and some progress has been made. Future papers will be published as significant results develop.

VII. ACKNOWLEDGEMENTS

The work presented in this analysis was funded by the NASA Tri-University Program at Ohio University. The author would like to thank Dr. Robert W. Lilley, Project Consultant, and Mr. Ralph W. Burhans, Project Engineer, for their technical advice. Additional thanks must go to Mr. Stanley M. Novacki, a fellow student intern, whose computer work produced all of the graphs presented in this paper.

VIII. REFERENCES

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[2] Burhans, Ralph W., "Mini-L Loran-C Receiver", NASA TM-48, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, March 1977.

[3] Burhans, Ralph W., "A Low-Cost Loran-C Envelope Processor", NASA TM-57, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, April 1978.

[4] Burhans, Ralph W., "Phase-Locked Tracking Loops for Loran-C", NASA TM-60, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, August 1978.

IX. APPENDICES

A. Data for Figures 1 and 2.

Loop Type	Slave	Deviation	S/N	S/S
Unimproved	A	0.87	18.4	-
"	"	0.71	16.8	-
"	"	0.69	14.8	-
"	"	1.10	12.4	-
"	"	1.43	11.0	-
"	"	1.63	9.6	-
"	"	2.25	8.0	-
"	"	2.95	6.5	-
"	"	4.53	5.5	-
"	"	6.71	4.0	-
"	"	10.80	3.5	-
"	B	1.24	-	1.000
"	"	1.96	-	1.095
"	"	2.81	-	1.243
"	"	4.60	-	1.484
"	"	5.96	-	1.673
"	"	7.46	-	1.917
"	"	9.47	-	2.300
"	"	11.24	-	2.831
"	"	12.70	-	3.345
"	"	15.00	-	4.600
"	"	15.65	-	5.257
Improved	A	0.13	18.4	-
"	"	0.21	16.8	-
"	"	0.56	14.8	-
"	"	0.55	12.4	-
"	"	0.48	11.0	-
"	"	0.95	9.6	-
"	"	0.97	8.0	-
"	"	0.60	6.5	-
"	"	1.39	5.5	-
"	"	2.45	4.0	-
"	"	2.44	3.5	-
"	"	4.53	3.0	-
"	"	6.32	2.5	-
"	B	0.36	-	1.000
"	"	1.38	-	1.095

Continued on next page.

A. Data for Figures 1 and 2 continued.

Loop Type	Slave	Deviation	S/N	S/S
Improved	B	2.61	-	1.243
"	"	4.13	-	1.484
"	"	6.92	-	1.673
"	"	7.36	-	1.917
"	"	9.34	-	2.300
"	"	11.76	-	2.831
"	"	13.29	-	3.345
"	"	15.65	-	4.600
"	"	17.38	-	5.257
"	"	20.65	-	6.133
"	"	22.46	-	7.360

B. Data Points for Figures 3 and 4.

Clock Offset = +3
See data in Appendix A for the improved loop.
Clock Offset = +6

Loop Type	Slave	Deviation	S/N	S/S
Improved	A	0.60	18.4	-
"	"	0.39	16.8	-
"	"	0.43	14.8	-
"	"	0.48	12.4	-
"	"	1.10	11.0	-
"	"	1.66	9.6	-
"	"	1.68	8.0	-
"	"	2.32	6.5	-
"	"	2.48	5.5	-
"	"	2.93	4.0	-
"	B	0.69	-	1.000
"	"	1.70	-	1.095
"	"	2.67	-	1.243
"	"	4.11	-	1.484
"	"	5.66	-	1.673
"	"	6.86	-	1.917
"	"	8.25	-	2.300
"	"	10.42	-	2.831
"	"	11.71	-	3.345
"	"	13.47	-	4.600

C. Data Points for Figure 5.

Device	Deviation	S/S
Front-end	0.25	1.000
"	1.00	1.095
"	2.50	1.243
"	3.75	1.484
"	4.50	1.673
"	5.00	1.917
"	5.75	2.300
"	6.25	2.831
"	7.00	3.345
"	7.80	4.600
"	8.50	5.257
"	11.00	6.133
"	13.00	7.360
DPLL	0.35	1.000
"	0.27	1.095
"	1.99	1.243
"	2.91	1.484
"	3.73	1.673
"	4.16	1.917
"	4.66	2.300
"	5.49	2.831
"	7.10	3.345
"	8.22	4.600
"	8.86	5.257
"	10.02	6.133
"	12.71	7.360