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Final Report

THE IDENTIFICATION AND CORRECTION OF CHANNEL-TO-CHANNEL PHASE DIFFERENCES WITHIN A DATA PROCESSING SYSTEM

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Prepared for:

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PREFACE

The purpose of this document is to report the results of an investigation of channel-to-channel phase errors that are occuring during the data reduction process at the Data Reduction Laboratory, George C. Marshall Space Flight Center. The thrust of the investigation was to characterize these errors, and to develop techniques that effect their correction. The data reduction process is presented and discussed to allow potential sources of phase error to be identified. Each hardware subsystem that was tested for its contribution to the total end-to-end phase error is discussed and the testing procedure given.

Once the sources and characteristics of the phase delay are identified, possible solutions for correcting or nullifying the phase delay differences are considered. One solution is recommended and presented in detail along with a detailed description of the means of implementation. To verify the ability of the solution to detect and correct phase delay differences with an acceptable degree of accuracy, analog test tapes were created and used as imput to the data reduction process.

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1. INTRODUCTION

The instrumentation technique, considered in this report, for accumulating and then later processing data, is shown in block diagram form in Figure 1-1. The data signals are generated by monitoring sources of interest with various types of transducers. The low power signals are then amplified and band-limited, if necessary, by the signal conditioners. Next, each data signal is used to frequency modulate a unique carrier and all the modulated carriers are summed to produce a composite FM multiplex output signal. This composite signal is recorded on one track of a flight recorder. The recorder tape contains 14 tracks and can therefore accommodate up to 14 such FDM (Frequency Division Multiplexer) composite signals.

To obtain the desired data information, the proper carrier frequencies are individually extracted, processed and analyzed. An example of information obtainable is the phase difference between data signals monitored by two or more transducers. As an illustration, suppose the phase difference between signals from several mechanical-to-electrical transducers placed at different locations within a space craft is known. Then the time required for a shock wave to travel throughout the craft could be computed and the source and direction of propagation could be extrapolated. The relationship between a time difference and phase difference for a given frequency, f, is

$$\Delta\phi = \Delta t \; f \; 360°$$

and $$\Delta t = \Delta\phi / (f \; 360^{\circ}).$$

Therefore, if the phase difference between two signals can be accurately measured, a data user can calculate the corresponding time of travel between mechanical-to-electrical transducers that generated the signals. Any time difference (propagation time) between two date signals at two transducers is carried as a phase difference between the two signals through the electronic channels and could be extracted by the computer in the data reduction process. It is a simple matter for the data user to convert back to time difference if required.

However, there is a potential problem in extracting phase information. If, during the data reduction process one signal is delayed more than another, the delay is interpreted as additional phase difference. The data user may unknowingly interpret the additional phase difference as additional propagation time and would arrive at an incorrect conclusion. This is illustrated in Figure 1-2. The balance of this report:

1. Presents results of tests done on the data processing hardware in order to determine the sources of channel time delay differences and to mathematically characterize the differences.

2. Develops a procedure to detect and correct for the introduction of these delay differences into the phase calculations. The procedure developed was subjected to test data to verify its capability, and the results are presented.

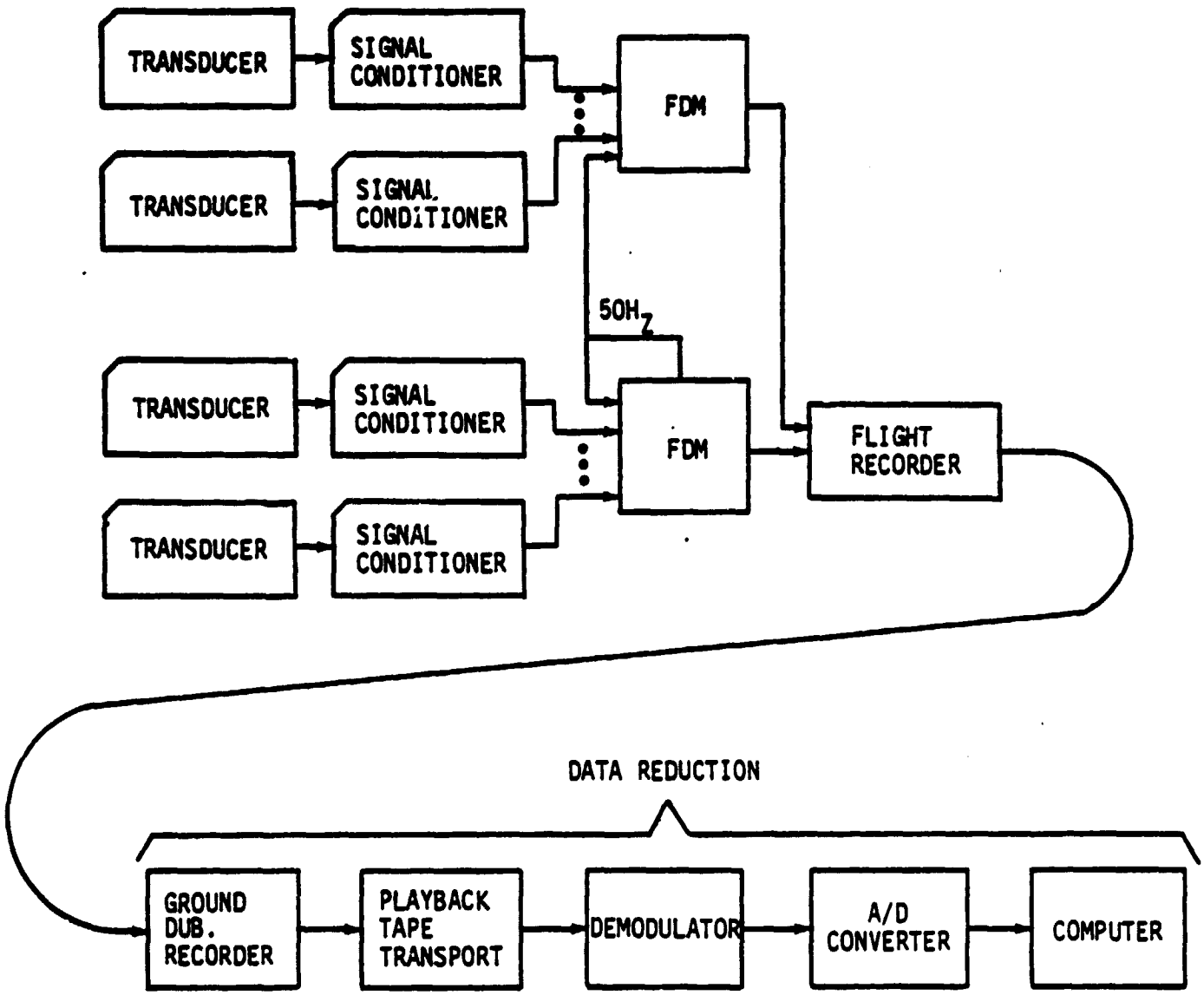
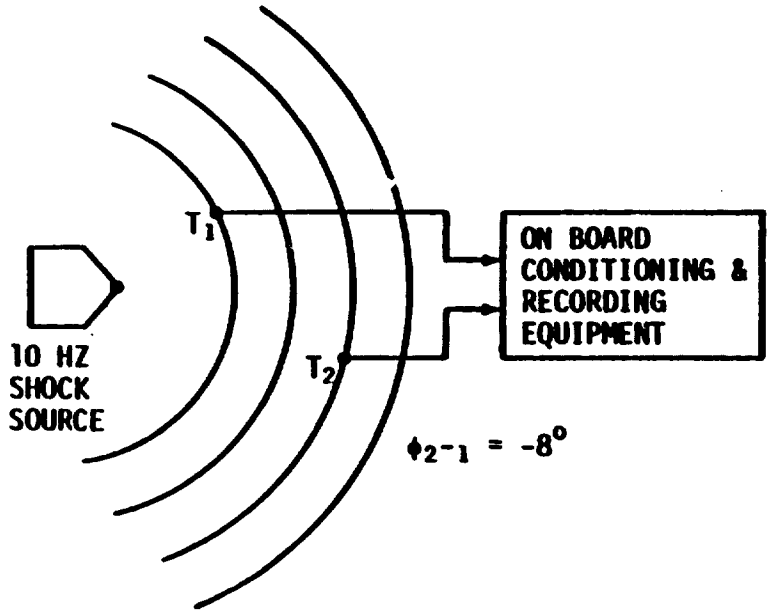
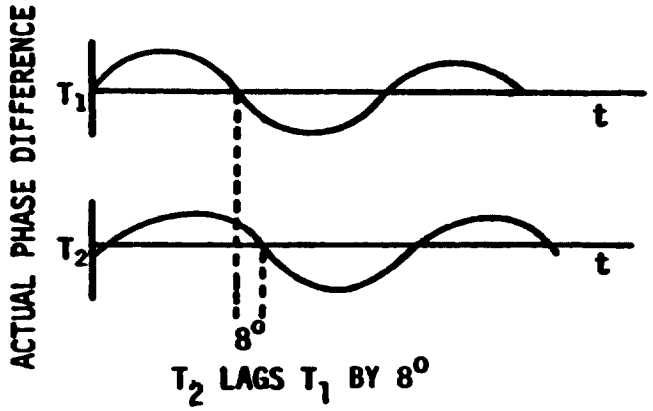
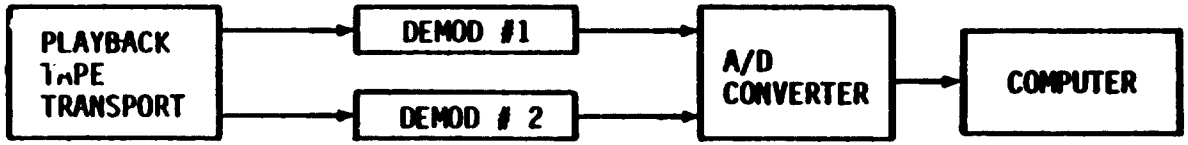


FIGURE 1-1 END-TO-END DATA PATH SHOWING POSSIBLE SOURCES OF PHASE SHIFT





CHANNEL NO. 1, PROCESSING TIME = 7.0 ms



CHANNEL No. 2, PROCESSING TIME = 4.5 ms

CHANNEL PHASE DIFFERENCE

$\Delta\phi_{2-1} = (\Delta t)\ (f)\ (360^o)$

$= (+2.5 ms)(10Hz)(360^o)$

$\Delta\phi_{2-1} = +9^o$

IT APPEARS THAT THE SIGNAL REACHES T_2 BEFORE T_1!

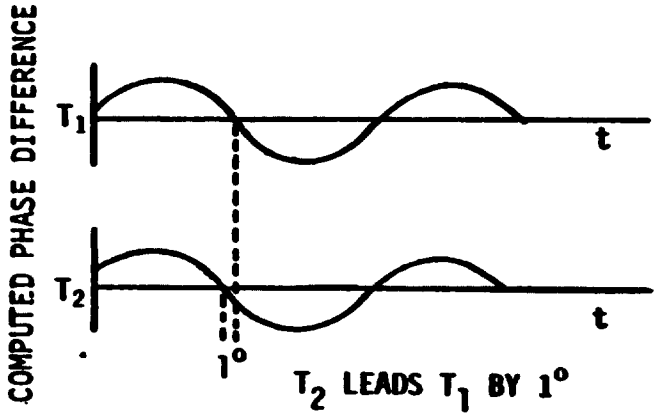


FIGURE 1-2 HYPOTHETICAL EXAMPLE OF PHASE ERROR

2. HARDWARE TESTING

As was shown in Figure 1-1, the major hardware components of the data reduction process are:

1. Analog tape recorders
2. Frequency demodulators
3. An A/D converter to create a digital tape
4. A Digital computer

These subsystem components were examined individually to determine what effect each had on signal propagation time.

2.1 Analog Tape Recorders

All the analog tape records and transports that are normally used in the data reduction process have allowable headstack time delay tolerances. At least one of each model was tested and found to be in, or close to, the acceptable tolerance which was 0.3 microseconds between any adjacent tracks on a headstack and 1.5 microseconds between other tracks on a headstack. Figure 2-1 shows the test setup used to determine the time delay differences among tracks. To show the effect of time delay difference on phase difference, two examples are given for a range of data frequencies. To insure that no error was introduced due to the testing procedure, a special skew tape supplied by the Bell and Howell Company was used. It contained test signals recorded continuously across the tape from edge to edge and not segmented for each track as is usually the case. This procedure guarantees commonality of the input signals for each track. The time difference measured is ususally due to a skewing (misalignment) of the headstack and is manually adjustable through an azimuth control. It is desirable that this be done shortly before an analog data tape is processed. The electronics associated with each track contributes a negligible time delay difference if they are operating properly since all are identical in design and calibration.

It can be concluded from the phase difference ($\Delta\phi$) calculations in Figure 2-1 that very little phase difference will be contributed by a properly functioning tape transport and playback electronics.

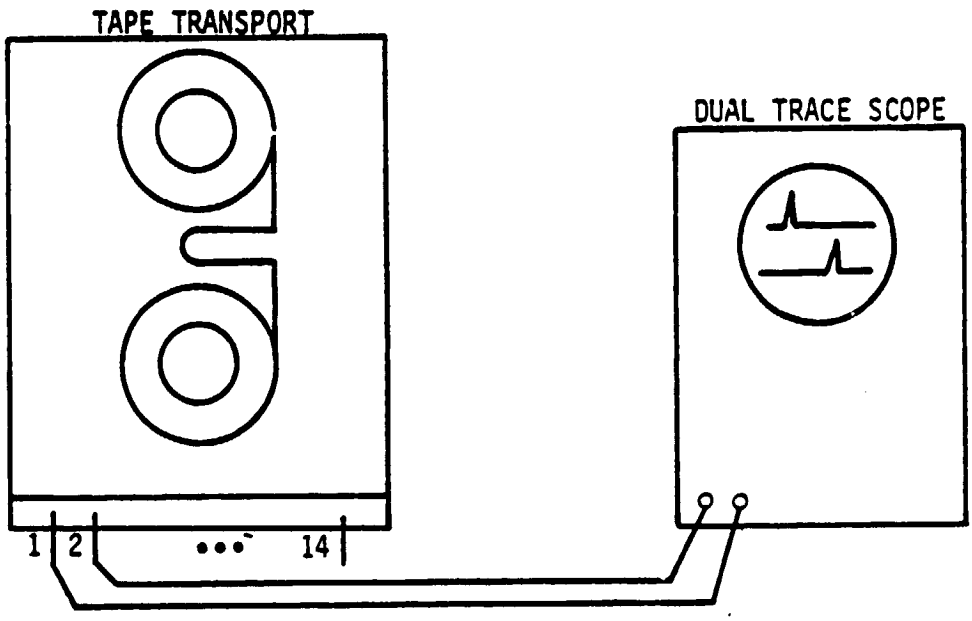
2.2 Frequency Demodulators

Three different groups of FM demodulators were tested for data phase delay difference. They included:

EMR Universal tunable discriminators

DCS Universal tunable discriminators

Metroplex nontunable discriminators



TEST SETUP USING SKEW TAPE

FREQ	10 Hz	50 Hz	200 Hz
$\Delta\phi$ (Δt = 2μSEC)	0.007°	0.036°	0.145°
$\Delta\phi$ (Δt = 10μSEC)	0.036°	0.18°	0.72°

$\Delta t \equiv$ TIME DELAY

$\Delta\phi = \Delta t$ F 360°

FIGURE 2-1 ANALOG TAPE RECORDERS

The approach taken in testing these devices was to determine the phase delay of a demodulator's output signal referenced to the demodulators input signal over a data frequency range of 2Hz to 200Hz. This test was performed for a number of units of each type using the test setup shown in Figure 2-2. The sweep source linearly swept the data VCO from 2Hz to 200Hz while driving the X-Y recorder from left to right. The data VCO frequency modulated the carrier VCO. The demodulator under test detected the data which was then compared in phase with the original data by the phase meter. The phase meter produced a voltage which was directly proportional to the phase difference, which was used to drive the X-Y recorder from bottom to top. This test actually determined the phase difference due to the time delay contributed by the demodulator plus that contributed by the carrier VCO. The time delay due to the carrier VCO was only a few microseconds which translates to less than one degree for the data frequency range considered. The phase delay caused by the demodulator was many times larger than the phase delay produced by the carrier VCO.

The EMR demodulators were the first to be tested. Figure 2-3 shows the demodulator phase delay as a function of data frequency for a set of center frequencies and FM deviations. The EMR demodulators are unique in that if the deviation selected is less than four percent of the center frequency selected, a frequency translation process, in addition to that which is normal, takes place. This requires additional time and hence creates additional phase delay and is exhibited in the figure by the 14KHz, 16KHz, 28KHz, and 32KHz center frequency curves.

To determine the large effects the discriminator output Low Pass Filter (LPF) cutoff frequency selection has in determining the phase delay, Figure 2-4 was generated. As the cutoff frequency is decreased, there is a very noticable increase in phase delay. The small circles on some of the curves mark the point at which the data frequency value equals the cutoff frequency. The significance of Figures 2-3 and 2-4 is that for a typical data reduction process in which one demodulator is set up to one center frequency, deviation , and LPF conbination; and another is setup differently, the phase difference computed for the two data signals will be in error by a considerable amount if the demodulator phase differences are not accounted for. The curves of Figures 2-3 and 2-4 were taken from one demodulator. Five other such units were tested and produced almost identical results. Therefore, their data are not included since one set is typical of this class of discriminators.

The next demodulators tested were the DCS universal models. Figures 2-5 and 2-6 contain results simular to that of the EMR's, but there is a significant difference. The DCS's do not undergo the frequency translation process discussed for the EMR's, and the resulting curves are well grouped according to deviation. The consequences of using different center frequencies, deviation, and LPF selections while processing data are, however, the same as that for the EMR's.

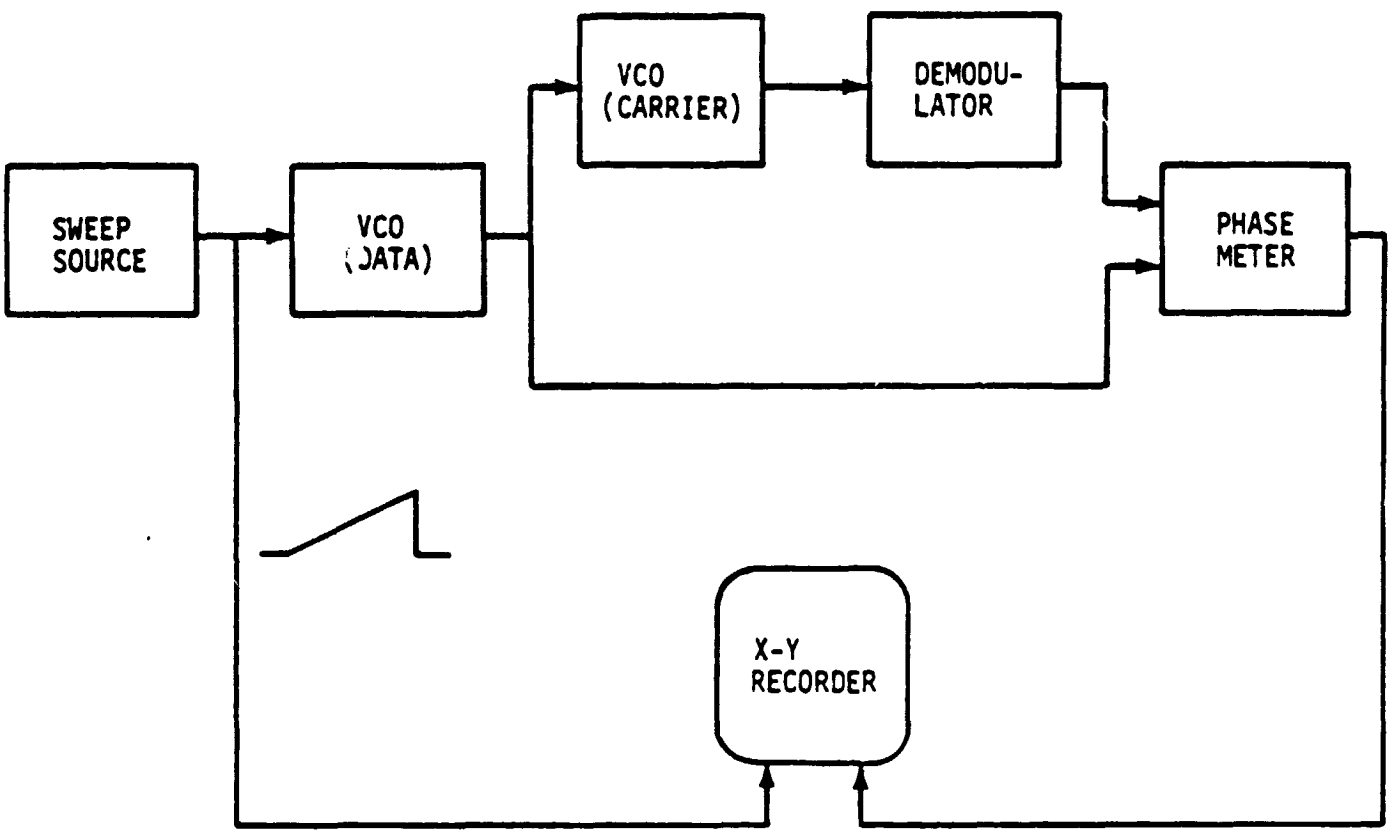


FIGURE 2-2 TEST SETUP FOR DEMODULATORS

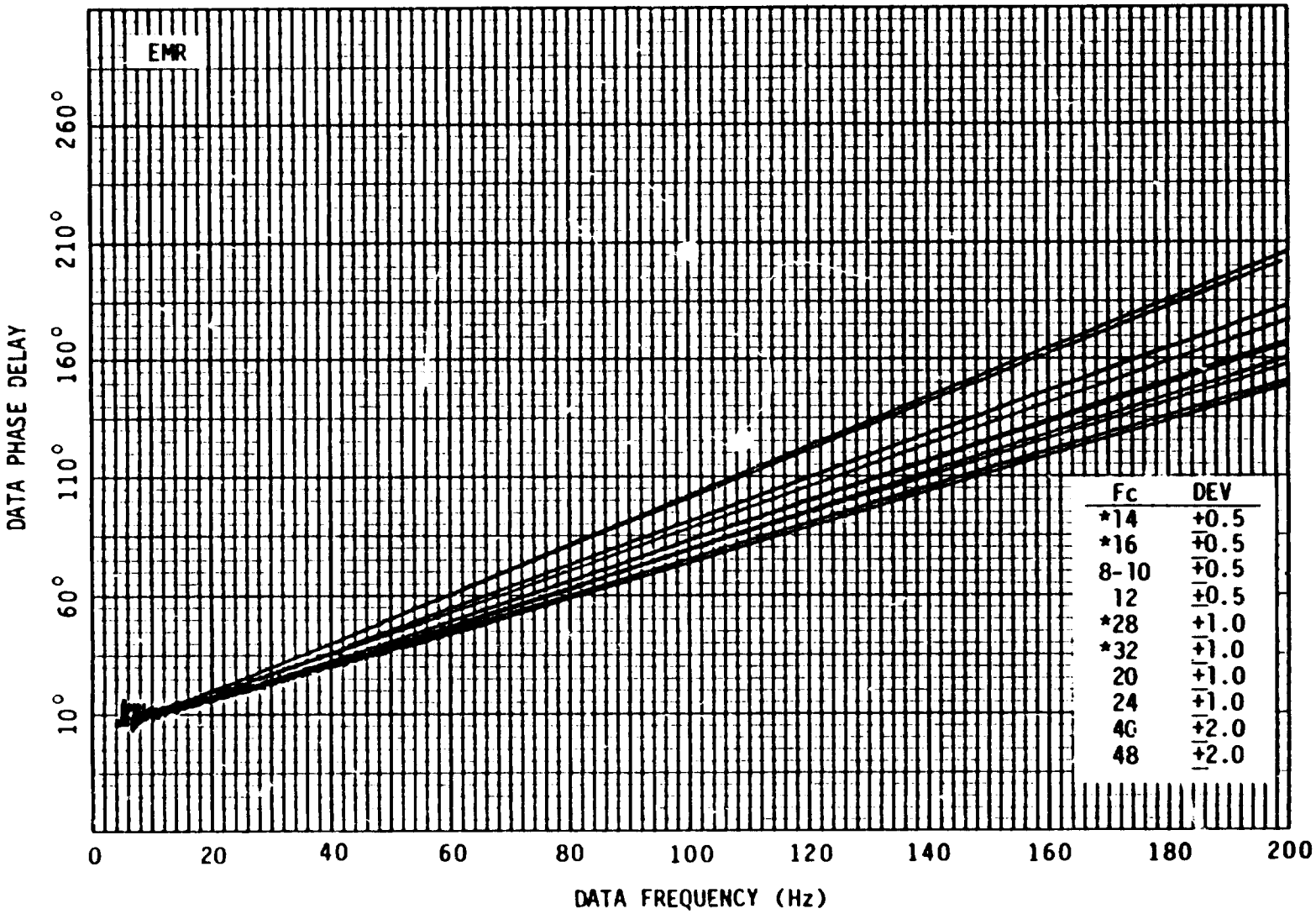


FIGURE 2-3 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR SET OF CENTER FREQUENCIES AND DEVIATIONS

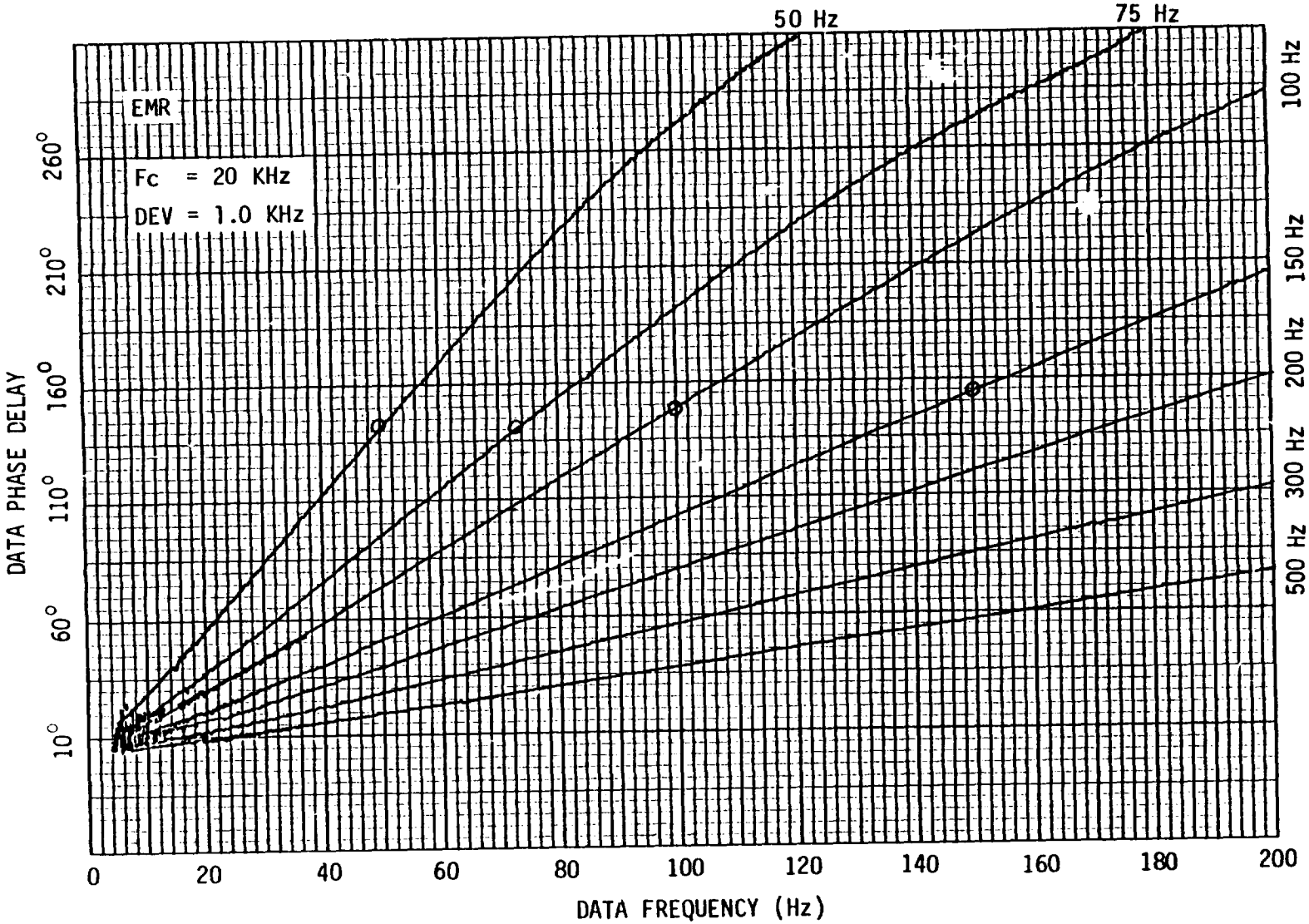


FIGURE 2-4 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR A SET OF LPF CUTOFF FREQUENCIES

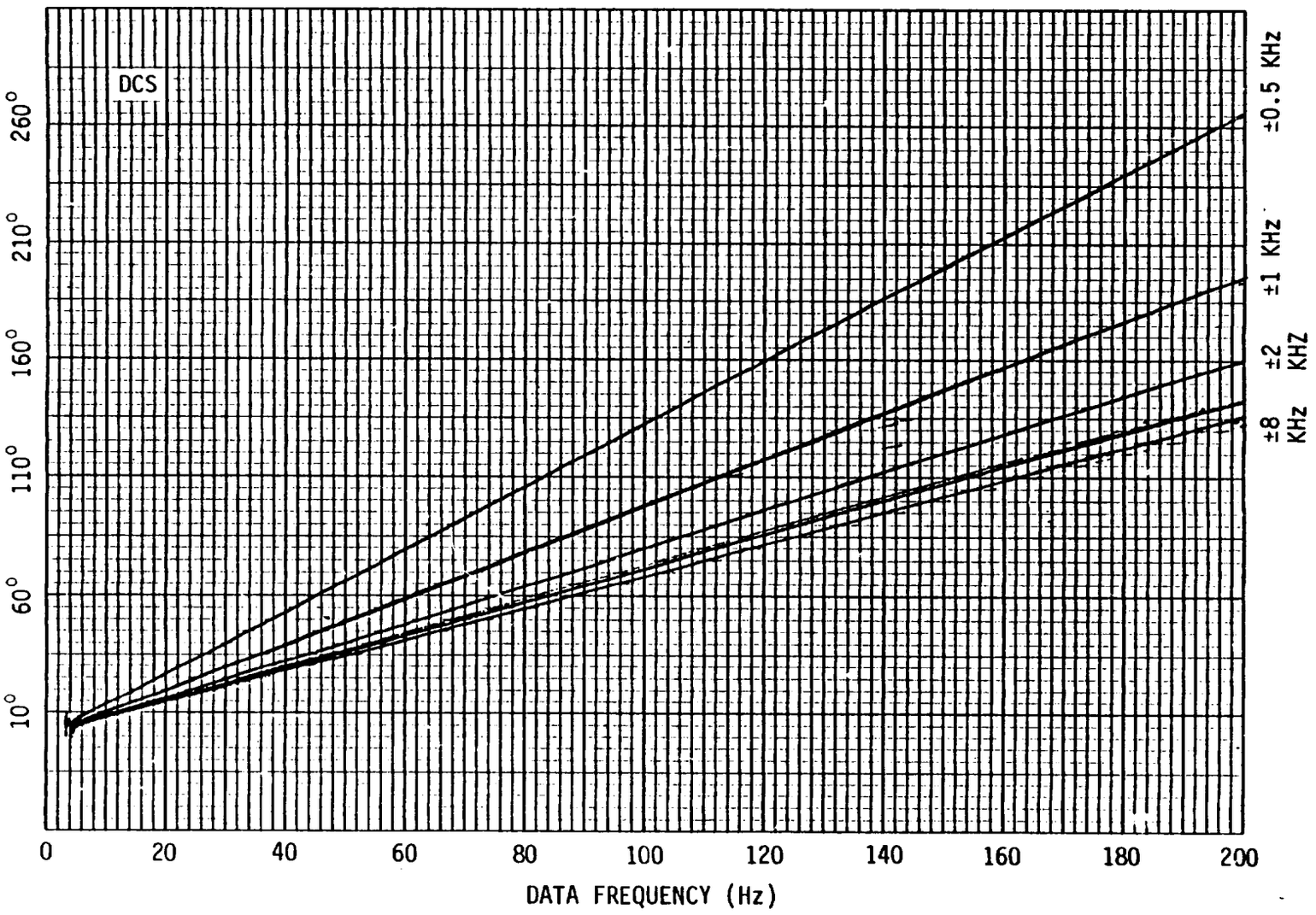


FIGURE 2-5 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR SET OF CENTER FREQUENCIES AND DEVIATIONS

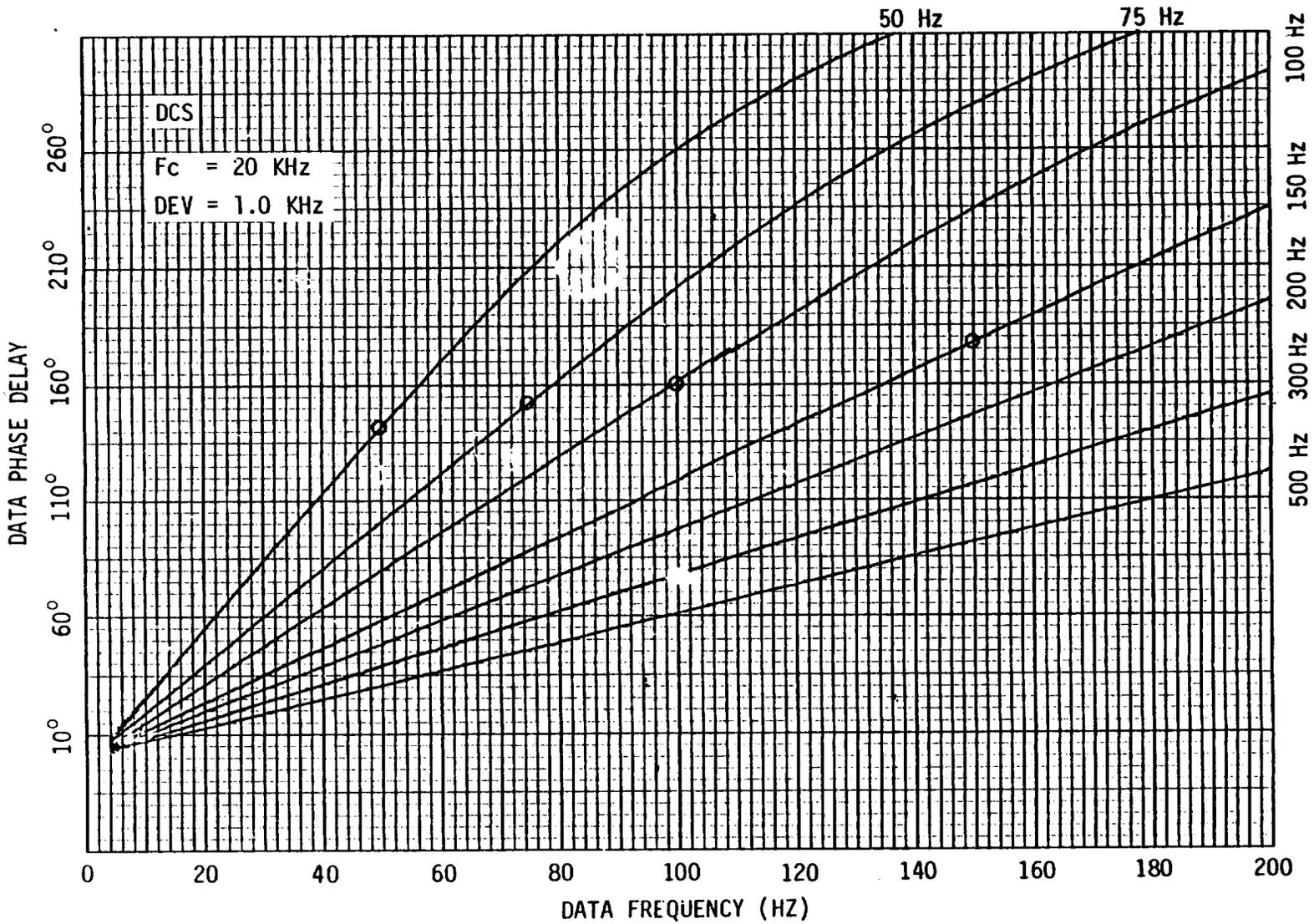


FIGURE 2-6 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR A SET OF LPF CUTOFF FREQUENCIES

During these tests, it was discovered that all units within the DCS group did not produce the same phase delay even when they were programmed the same. To document this, three families of curves were plotted showing phase delay for 23 demodulators. All demodulators were programmed as indicated in Figures 2-7 and 2-8, and 2-9 and resulting phase delay were plotted for each unit, one at a time. It is likely that the discrepancies among units are attributable to the fact that when a demodulator is programmed, mechanical relays which are supposed to open or close to select the required electronic components and thereby produce the correct cutoff frequency, deviation, etc., are not functioning properly. These variances between selected values and actually achieved values add additional burden in the effort to nullify the demodulator phase delay, since they are difficult to characterize once it is not clear if the malfunctions are systematic or random in nature.

The last demodulator group tested was the metroplex nontuneable units. Again, the phase delay grouped according to the deviation and LPF cutoff frequency as seen in Figure 2-10. Each curve drawn in the figure is actually many curves laying on top of each other. Every Metroplex demodulator in the group was tested. As with the other two groups, it is seen that there is considerable phase delay for the higher data frequencies, and the delay between any two channels can be as great as 140 degrees.

2.3 A/D Converter

Once the data signals leave the demodulators they are digitized. If sample and hold amplifiers are used in the digitizing process, no additional time delay differences should be created between data signals. This was verified by injecting a common signal at the input of four channels of the A/D converter and by creating a digital tape. A dump of this tape revealed that the resulting data counts for all channels were within plus or minus one of each other. This represents an insignificant phase difference between channels.

Without sample and hold, there is a time delay difference between data channels, which is a function of the number of data signals being digitized, the juxtaposition of these signals, and the sampling rate.

This is illustrated in Table 2-1 which is a partial listing of the counts representing the amplitudes of four variables (analog data signals) that have been digitized. The data in this case was a single 100Hz sine wave applied directly to the four variable inputs of the digitizer. The four variables were scanned at a rate of 5,000 times a second. Therefore, each variable was sampled 1250 times a second, and since the data was a 100Hz sine wave, each cycle was sampled for an average of 12.5 times. This is more than adequate for most data analysis process.

Since a total of 5,000 samples are taken each second, the time between each sample and the next is the reciprocal of 5,000 or 0.2 msec. This small time difference between sampling

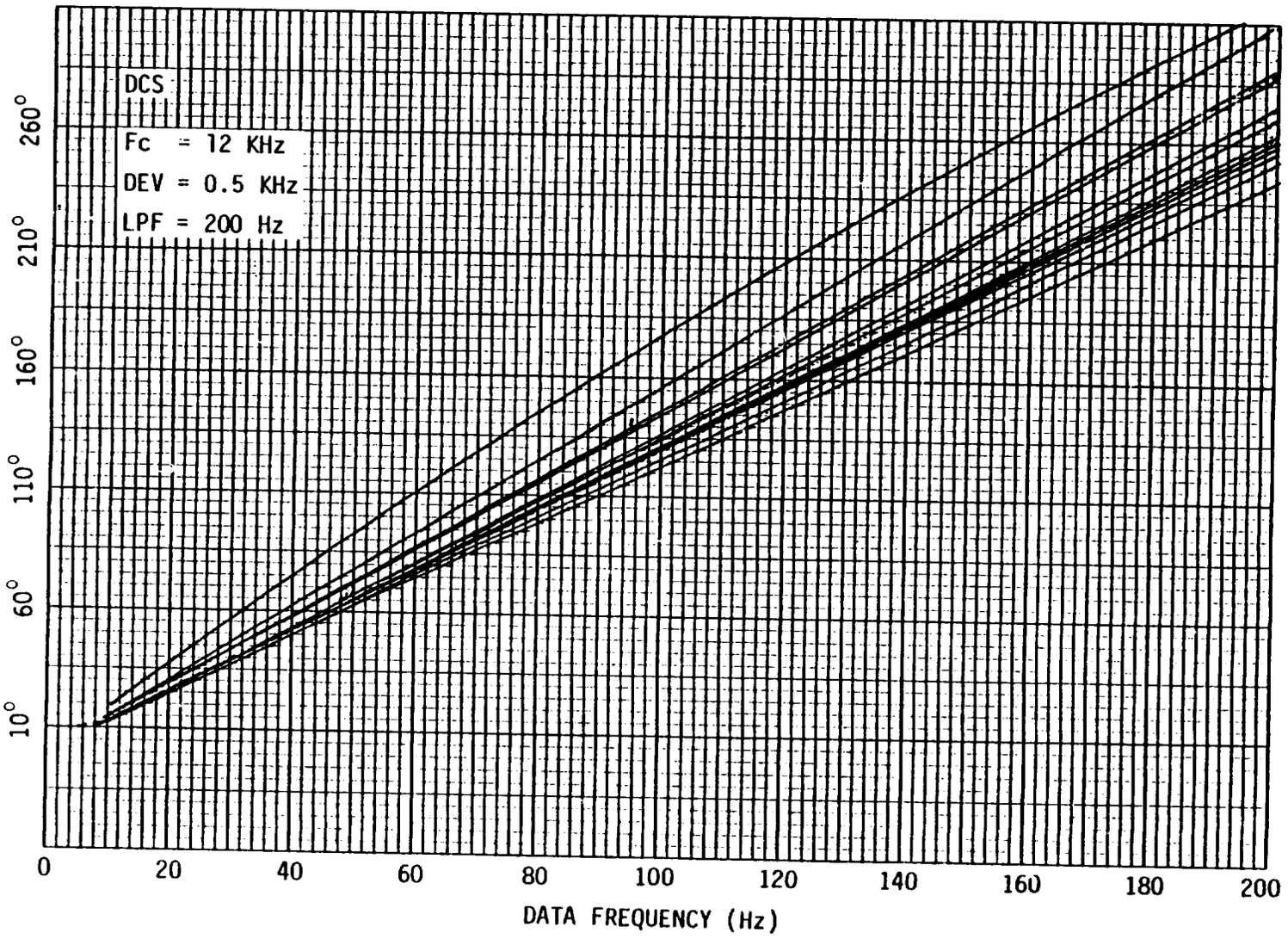


FIGURE 2-7 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR 23 DCS DEMODULATORS

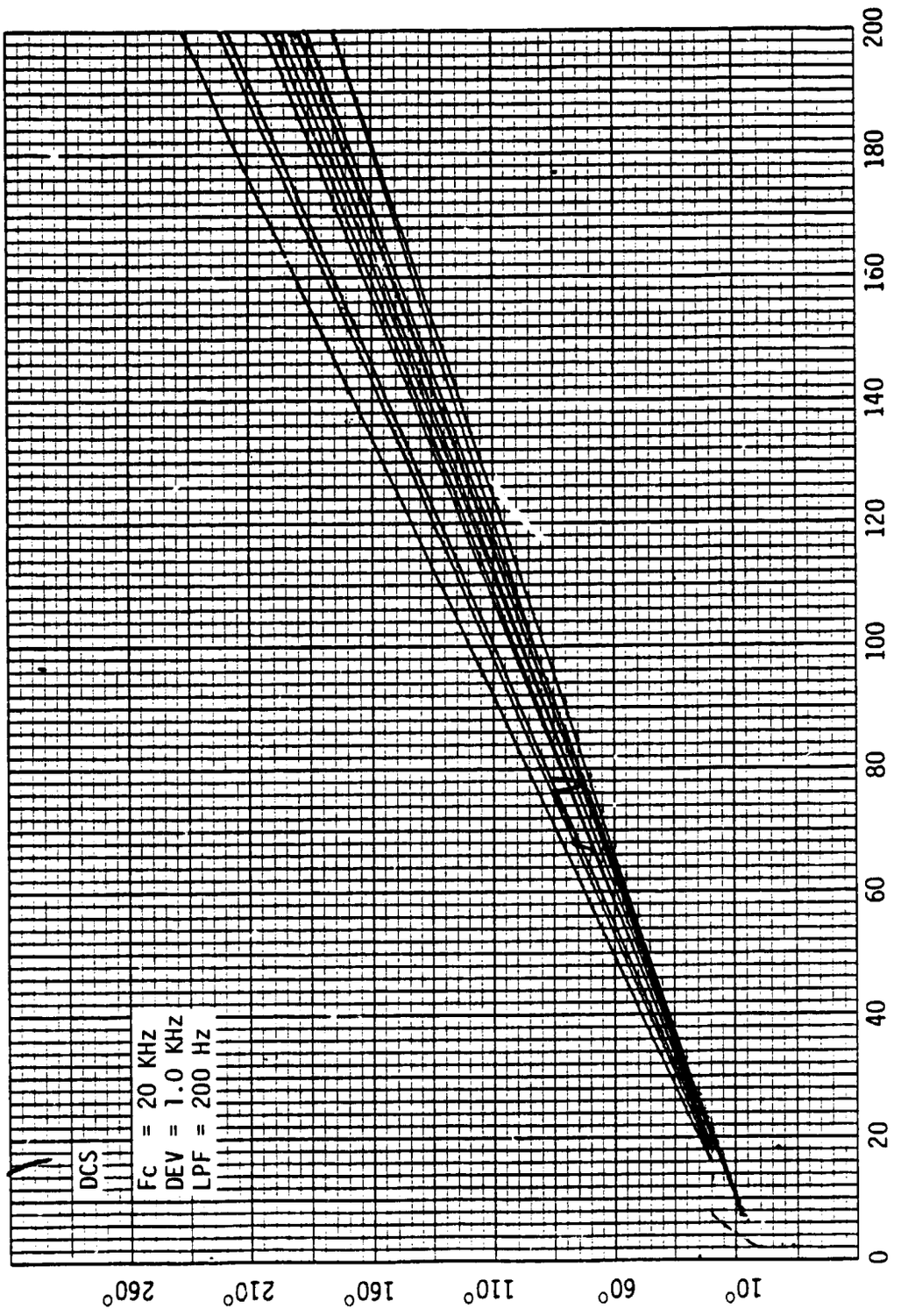


FIGURE 2-8 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR 23 DCS DEMODULATORS

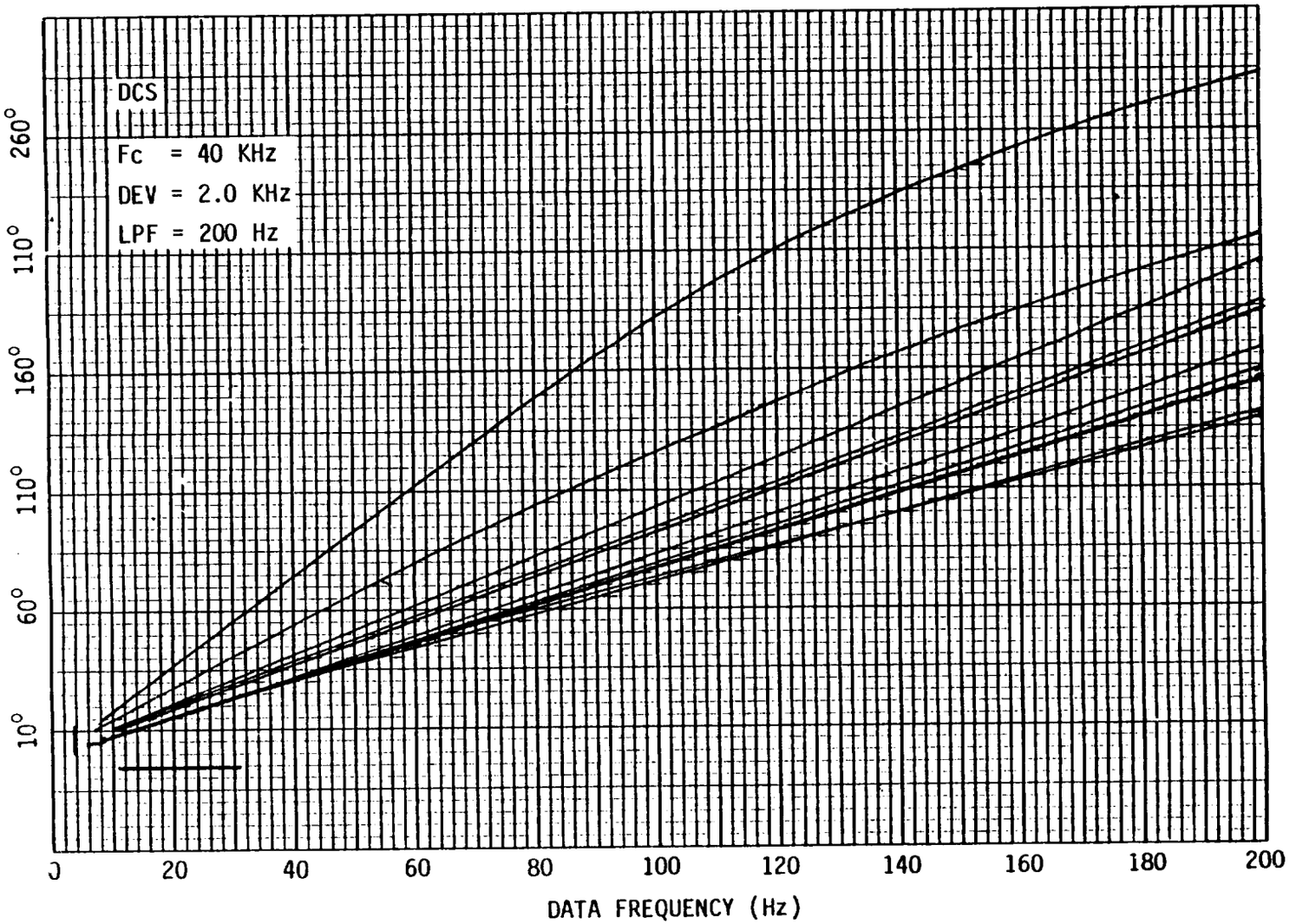


FIGURE 2-9 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR 23 DCS DEMODULATORS

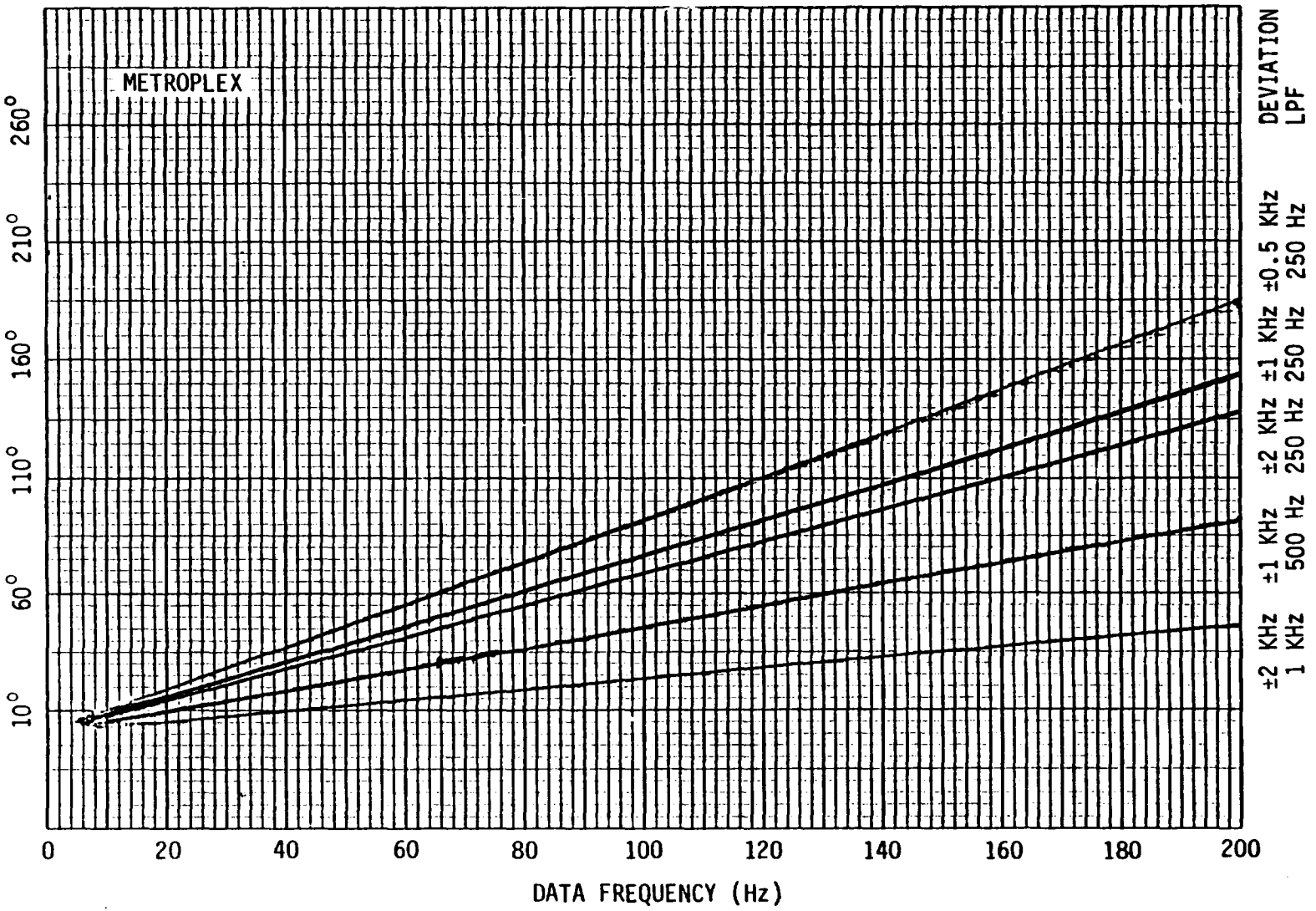


FIGURE 2-10 PHASE DELAY AS A FUNCTION OF DATA FREQUENCY FOR SET OF CENTER FREQUENCIES AND DEVIATIONS

SCAN	V 1	V 2	V 3	V 4
1	22	-14	-51	-85
2	-120	-153	-183	-209
3	-234	-255	-270	-281
4	-288	-292	-291	-283
5	-273	-260	-241	-217
6	-191	-165	-132	-93
7	-62	-27	7	46
8	80	114	145	177
9	204	227	248	265
10	277	283	289	289
11	282	270	256	239
12	215	188	160	127
13	92	56	19	-15
14	-52	-88	-123	-153
15	-183	-210	-235	-253
16	-268	-280	-285	-285
17	-283	-279	-268	-253
18	-234	-212	-186	-155
19	-124	-91	-57	-19
20	19	49	84	120
21	151	180	206	232
22	252	266	278	289
23	292	289	282	273
24	259	239	215	190
25	161	125	90	56
26	18	-18	-56	-89
27	-125	-160	-189	-215
28	-239	-260	-275	-285
29	-291	-294	-291	-283
30	-272	-259	-240	-215
31	-189	-162	-128	-93
32	-58	-23	11	49
33	84	117	148	180
34	206	229	249	265
35	278	284	290	291
36	283	271	257	240
37	217	190	162	130
38	98	59	22	-12
39	-49	-86	-121	-151
40	-183	-211	-235	-254

TABLE 2-1 COUNT LISTING FOR FOUR VARIABLES. SCAN RATE EQUALS 5 KHz

variable and sampling the next indroduces an apparant phase difference of

$$\Delta\phi = \Delta t \; f \; 360^{\circ}$$

$$\Delta\phi = 0.2 \; (10)^{-3} \; 100 \; 360^{\circ}$$

$$\Delta\phi = 7.2^{\circ}$$

Thus, in this typical example, if V1 is considered a reference, the following phase differences between data signals appear due to the sequential sampling process:

$$\phi_{2-1} = 7.2^{\circ}$$

$$\phi_{3-1} = 14.4^{\circ}$$

$$\phi_{4-1} = 21.6^{\circ}$$

A decrease in the scan rate or an increase in the number of variables would increase the phase differences.

3. SUMMARY OF SOURCES AND CHARACTERISTICS OF PHASE DELAY

It was found that the t e delay difference originating in the analog tape recorders was relatively small and constant leading to phase delay differences which vary linearly between approximately zero degrees to less than two tenths of a degree within the data frequency range of interest.

The demodulators exhibited phase delays that were linear functions (in the constant delay mode) of the center frequency, deviation, and output filter cutoff frequency. The actual maximum value could vary from unit to unit but usually fell within the range of 50 degrees to 250 degrees. This means that the phase delay difference between two demodulators can be as much as 200 degrees for a 200 Hz data frequency.

The digitizing process with sample and hold amplifiers (simultaneous sampling of each channel) introduced negligible phase delay differences, while processing without the sample and hold amplifiers (sequential sampling of each channel) produced linear delays within the range of five degrees to 40 degrees depending on the number of variables and the sampling rates. This phase delay was a result of the time required for the commutator within the digitizer to switch from one measurement channel to another.

4. POSSIBLE SOLUTIONS

The following properties were considered as important while seeking possible methods of removing or nullifying the phase errors introduced by the data reduction process. To be acceptable, a solution should:

- be efficient
- be economical
- have minimum impact on the existing system
- be able to function under large and intense work loads
- maintain a high degree of reliability

Five possible solutions worthy of investigation were considered. Each one requires a common reference signal to be applied to each data channel that will process signals requiring phase correlation. This reference signal must be present at these channels during a period of time long enough to allow adequate computer processing. Since the input reference signals applied to each channel start out in phase, any phase difference measured by the computer of a channel pair will be due to the time delays being unequal for those two channels. This phase difference information represents the "error" caused by the data reduction process, and this data is required for each of the following possible solutions.

4.1 Add Time Delay at Each Demodulator Output

With the phase difference between two channels known for one frequency, the time delay difference can be calculated. Since it has been demonstrated that the channels have linear phase delay with respect to frequency, the time delay is constant and is calculated by:

$$\Delta t = \Delta\phi/(f\ 360^{\circ})$$

It is therefore possible to place analog type time delay networks between the demodulators and the digitizer with values such that each data channel has the same net time delay. The delay networks could be adjustable to accommodate all possible needs due to different combinations of center frequencies, deviations, and LPF cutoff frequencies. Such a solution would be very expensive and would require manual adjustment before each data processing task is performed.

One type of analog time delay network is the low pass filter such as that in the demodulator. The lower the cutoff frequency, the greater the time delay (hence phase delay) through it. This was varified in Figures 2-4 and 2-6. To use this approach, the demodulators would be programmed as normal with the low pass cutoff frequency value somewhat higher than the highest data frequency to be analyzed. Then the channels with the greatest time delay would have their LPF cutoff frequency increased,

thereby decreasing their time delay to equal that with the smallest time delay. This equalizing process would be carried out to match all channels. The limitations of this approach is that it is a manual process, it must be done each time the demodulators are programmed, and the amount of reduction in phase delay resulting from additional increases in the LPF cutoff frequency diminishes as the cutoff frequency gets larger. There would be situations in which some channels have filters with cutoff frequencies so high that noise, adjacent channel signals, as well as unwanted data would be passed to the digitizer. The analysis on the desired data could be rendered useless.

4.2 Shift Count Position of Raw Data

This technique would require determining the amount of time all other channels lag behind the leading channel, by using the reference signal. A computer program would be written to read the raw data from the digital tape, write the first scan value for the data of the leading channel as is, and for each other channel look ahead a number of scans equal to its relative time delay for that channel and write that value. This would be repeated until all scans were processed. The data on the digital tape would probably be handled in large blocks, and the resulting processed data would be written onto a new digital tape for later analysis.

This alignment process would result in a loss of an amount of data equal to the number of scans represented by the time difference between the leading channel and the channel with greatest time lag. Two other disadvantages are that this process is time consuming and requires operator performance.

4.3 Hardware-Commutator or Delay Registers

This approach accomplishes data alignment in a manner similar to the previous approach. The output of the digital tape would go to an electronic commutator which cycles at a speed that allows it to read the leading data channel first, the second leading data channel next, after a time period equal to the time between it and the leading channel; and so forth, until all channels were read and rewritten onto a new digital tape. This could also be accomplished by dumping a scan for all channels into long delay registers (one for each channel) and shifting the values by an amount equal to that required for time equalization.

In either case extensive electronics would be required with variable timing control that could be automatically adjusted for each analog tape processed.

4.4 Discrete Fourier Transform of Raw Data

One correction procedure would be to add or subtract amplitude correction terms to all count values representing each data signal. However, this is not mathematically possible in the time domain. What can be done, however, is that the digital data repre-

senting each data signal can be Fourier transformed to the frequency domain, a phase correction term can be added which will be a function of data frequency and then be inverse transformed back to the time domain. Again a new digital tape would be generated to hold the modified raw data. Due to the large amount of data normally processed during frequency analysis, this approach would be very time consuming and must be done prior to analysis.

4.5 Add Correction Terms During Analysis

During the normal frequency analysis process the data is transformed to the frequency domain, to obtain information such as cross correlation, power spectral density, co-spectral density, and quadrature spectral density. It is therefore reasonable to consider employing this program to first determine a set of phase correction terms which use the reference input data, then adding them to the phase calculations done on normal data. This would increase the computational time by an amount approximately equal to that required to process one slice of data. It could be accomplished completely within the computer requiring no operator assistance other than identifying the reference data for the computer by a control card or command from a console. It would, however, require some modification to the present frequency analysis program.

5. RECOMMENDED SOLUTION

Of the five solutions proposed, only the last one meets all the properties listed at the beginning of Section 4. The hardware solution would be expensive, require a major modification to the existing system, and would be time consuming. The others would be time consuming and require considerable attention from personnel.

5.1 Implementing the Solution

As a result of the extensive measurements made, it is known that due to the constant time delay in the demodulator, and other hardware to a lesser extent, the phase delay from input to output of two channels for in-phase imput signals will be similar to that of Figure 5-1. "Signal ε" represents the phase difference: sometimes referred to as phase error. "Signal 2" has been designated as the reference channel signal. The equation for this error as a function of frequency is:

$$\phi_\varepsilon(f) = \frac{\phi_1\ (f_R) - \phi_2\ (f_R)}{f_R} f$$

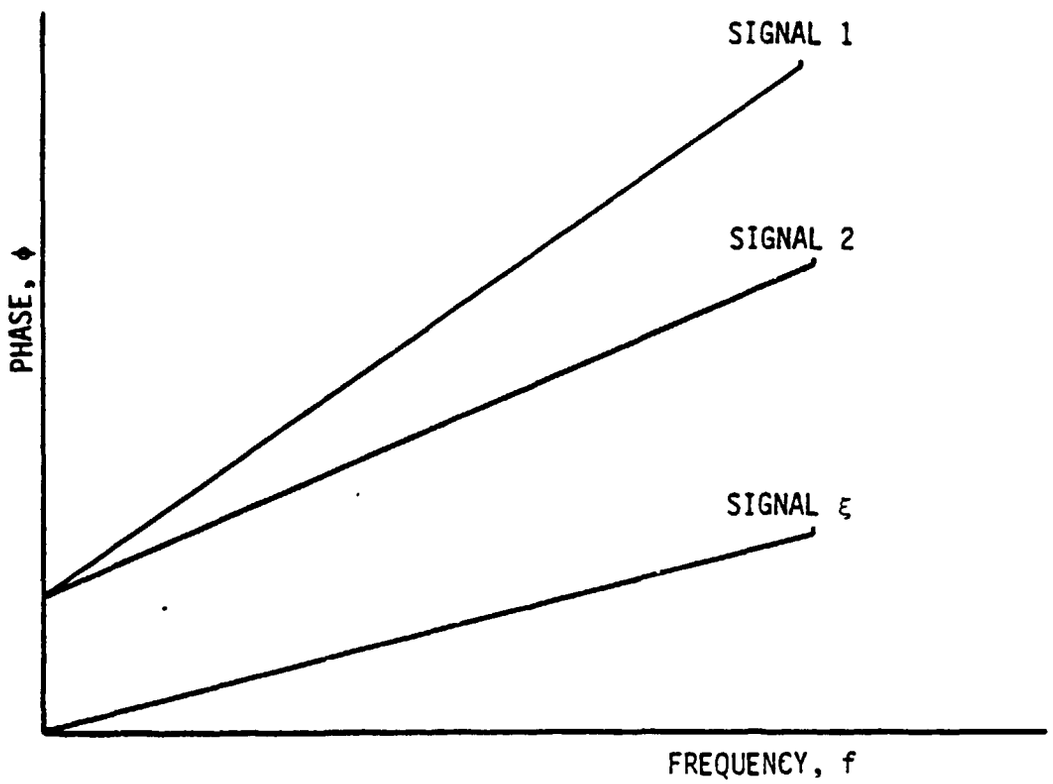
$$\phi_\varepsilon\ (f) = \frac{\phi_{1-2}\ (f_R)}{f_R} f$$

Where f_R is a single, designated reference frequency.

Therefore, if the channel phase difference is known for one frequency (f_R), it can be calculated for all other frequencies and used as a phase correction term.

The procedure for correcting the channel phase difference will be as follows: The frequency analysis computer program will be modified so that an input parameter value will indicate that a particular incoming data slice contains the common, in-phase input reference signals. The exact frequency value f_R of the input reference signal will be calcuated and stored. Next, the phase difference between the incoming single frequency reference signals will be calculated and stored. Since the data started out in-phase, any phase difference cacu1ated between two signals will be the result of the time delay difference between the two channels. With the channel phase error for one frequency determined and stored, the phase error for any other frequency can be calculated by using the previous equation.

When normal data is processed and the phase angle is computed as a function of frequency for two variables, the phase error resulting from the two channels will be calculated for the same frequency and subtracted from the data phase in order to cancel out the differences between channels.



SIGNAL ξ = SIGNAL 1 - SIGNAL 2

FIGURE 5-1 TYPICAL PHASE VERSUS FREQUENCY RESPONSE CURVES

6. VERIFICATION OF SOLUTION

To exercise the phase correction procedure and demonstrate its capability, an analog tape containing the Shuttle SRB FDM carrier frequencies was created. The data was composed of a dc level step calibration signal, a 10 seconds of 50 Hz ac calibration signal, and a 10 Hz square wave signal. All of the above data were applied to the SRB FDM channels in phase (0 degree phase difference). The channels chosen to be used in the verification test are listed in Table 6-1. They were selected so that each channel deviation and output filter value of interest would be represented.

The data phase angle of these channels was determined in two processes. First, the DCS discriminators were used during digitizing, but without using sample and hold amplifiers. Second, the EMR discriminators were used with sample and hold amplifiers during digitizing.

6.1 DCS Discriminator/Without Sample and Hold

As previously demonstrated, there will be relatively large channel-to-channel phase differences introduced in this process due to the discriminators and as a result of digitizing without sample and hold amplifiers. These errors can be additive or subtractive.

The data slice selected for processing contained the 10 Hz square wave. Using the first channel data as a reference, the relative phase angles of the other channel's data were computed with and without the phase correction procedure. The results for the 10 Hz and the first nine harmonics are listed in Table 6-2.

6.2 EMR Discriminator/With Sample and Hold

The same data slice as used previously was redigitized with sample and hold amplifiers. The discriminators used were EMR Universal turnables. Again the relative phase angles were computed with and without the phase correction procedure. The results are given in Table 6-3.

6.3 Conclusion

Upon examination, Table 6-2 and Table 6-3 reveal that to ignore the time delays of the individual data channels results in large errors in relative phase angles between the data signals in these channels. The employment of the channel phase error correction procedure does result in a very significant improvement.

The residual error after correction is most likely a combination of errors caused by:

a. small phase differences between signals at the input to the FDM even though they were generated by a common source and started out in phase;

b. small nonlinear phase delay components of the channel hardware causing the computer's calculations to be off;

CHANNEL NO.	CENTER FREQUENCY	DEVIATION	OUTPUT FILTER
1	12 KHz	±0.5 KHz	250 Hz
2	14 KHz	±0.5 KHz	250 Hz
4	20 KHz	±1.0 KHz	500 Hz
8	40 KHz	±2.0 KHz	1.0 Hz

TABLE 6-1 CHANNELS USED IN VERIFICATION TEST

FREQUENCY Hz	PHASE DIFFERENCE 14-12 UNC	14-12 C	20-12 UNC	20-12 C	40-12 UNC	40-12 C
10	+ 0.89	+0.07	- 1.89	+0.09	- 3.61	+0.06
30	+ 2.66	+0.20	- 5.68	+0.25	-10.84	+0.16
50	+ 4.45	+0.34	- 9.48	+0.41	-18.01	+0.32
70	+ 6.27	+0.53	-13.39	+0.46	-25.27	+0.39
90	+ 7.93	+0.54	-17.26	+0.57	-32.32	+0.71
110	+ 9.80	+0.76	-21.34	+0.44	-39.63	+0.73
130	+11.80	+1.12	-25.32	+0.42	-46.62	+1.08
150	+13.41	+1.09	-29.66	+0.04	-53.96	+1.07
170	+15.49	+1.54	-33.71	-0.06	-60.92	+1.44
190	+17.17	+1.58	-38.10	-0.48	-68.11	+1.58

TABLE 6-2 RESULTS OF THE DCS DISCRIMINATOR/WITHOUT SAMPLE AND HOLD PROCESS

FREQUENCY Hz	PHASE DIFFERENCE 14-12		20-12		40-12	
	UNC	C	UNC	C	UNC	C
10	+ 2.17	-0.02	-0.36	+0.01	- 0.92	+0.03
30	+ 6.48	-0.09	-1.06	+0.02	- 2.80	+0.03
50	+10.77	-0.18	-1.78	+0.02	- 4.70	+0.01
70	+15.01	-0.32	-2.53	+0.00	- 6.58	-0.03
90	+19.27	-0.43	-3.28	-0.04	- 8.31	-0.02
110	+23.48	-0.60	-4.10	-0.13	-10.51	-0.13
130	+27.50	-0.95	-5.03	-0.34	-12.58	-0.32
150	+31.53	-1.31	-5.92	-0.51	-14.57	-0.42
170	+35.78	-1.44	-6.91	-0.77	-16.65	-0.62
190	+39.70	-1.89	-7.84	-0.98	-18.78	-0.85

TABLE 6-3 RESULTS OF THE EMR DISCRIMINATOR/WITH SAMPLE AND HOLD PROCESS

c. the computer's limitations in how exact it can calculate frequency and hence parameters which are functions of frequency.

In the calculations for Table 6-2 the bandwidth was specified to be 0.20 Hz. In the calculation for Table 6-3 it was specified to be 1.0 Hz. The actual frequency will be somewhere within a range which has a width equal to one-half the specified bandwidth. The accuracy of calculating frequency could be improved by decreasing the bandwidth (while still meeting all other program restrictions); but this would be costly in computation time.