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STUDY PROGRAM TO IMPROVE THE OPEN-CIRCUIT VOLTAGE OF LOW RESISTIVITY SINGLE CRYSTAL SILICON SOLAR CELLS

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SPIRE CORPORATION

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

FOREWORD

Contributions to this program have been made by many individuals at Spire Corporation. The Program Manager was J. A. Minnucci and the Principal Investigator was K. W. Matthei. The project team was staffed as follows:

R. C. Thomas, Solar Cell Processing
A. C. Greenwald, Electron Beam Processing
V. Sils, Epitaxial CVD

The contributions and support of personnel at NASA-LeRC, particularly T. Klucher, the Technical Manager, are gratefully acknowledged.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF FIGURES (Concluded)

LIST OF TABLES

SUMMARY

This is the final report under Contract NAS-3-20823, "A Study Program to Improve the Open-Circuit Voltage of Low-Resistivity, Single Crystal Silicon Solar Cells", performed for NASA Lewis Research Center as a part of LeRC's effort to achieve 18% (AM0-25°C) efficient cells. The objective of the program was to fabricate high-efficiency, low-resistivity solar cells by ion implantation and state-of-the-art annealing methods. The open-circuit voltage goal was 0.70V, and cells with voltages as high as 645 mV (AM0-25°C) were produced.

The development effort was based on ion implantation as a processing method to introduce spectroscopically pure dopants into the silicon material in a controlled manner. Phosphorus, arsenic, and combinations of phosphorus and arsenic ions were implanted according to a parametric junction layer optimization. Both furnace annealing and pulsed electron beam annealing were investigated as a means to remove the lattice damage caused by low-energy ion implantation. A wide range of implant parameters and annealing process parameters were investigated in this effort to improve open-circuit voltage above the existing state-of-the-art values. The best electrical performance results were attained using furnace annealing.

Eighty solar cells were fabricated and delivered to NASA using both (111) and (100) float-zone silicon substrates. The cells were ion implanted and processed with and without SiO_2 surface passivation to determine the effects of dopant concentration. Measurements of AM0 cell performance showed that higher open-circuit voltage and higher fill factors are attained with increasing junction doping concentration. The best cells processed under this contract had open-circuit voltages of 645 mV, short-circuit currents of 140 mA (35 mA/cm^2), and fill factors of 0.78.

SECTION 1

INTRODUCTION

This program to improve the open-circuit voltage of low-resistivity silicon solar cells was initiated as a part of NASA-LeRC's overall objectives to increase silicon solar cell efficiency to 18% under AM0 conditions. Recent NASA-LeRC workshops[1] on high-efficiency solar cells for spacecraft application have concluded that 18% efficient silicon cells are possible if the following parameters are attained simultaneously:

$$I_{sc} \quad - \quad 180 \text{ mA } (45 \text{ mA/cm}^2)$$
$$V_{oc} \quad - \quad 0.70V$$
$$F.F. \quad - \quad 0.80$$

The only cell performance parameter not yet realized for existing cell structures is open-circuit voltage. The goal of this contract was improvement of V_{oc} from 0.600-0.605V, typical of cells manufactured by any process, to 0.70V by utilizing ion implantation for junction introduction.

A number of physical mechanisms have been proposed to model open-circuit voltage limitations of silicon solar cells.[2,3,4] The device structure included in these models is either n^+pp^+ (or p^+nn^+) with back surface fields (BSF's) or simple n^+p (or p^+n) devices. Many of these models contain analysis which indicate that dopant profile, dopant concentration, and recombination-generation rates in the emitter layer are critical factors.

Also, calculations of device performance by Dunbar and Hauser[5] have shown the importance of reducing surface recombination velocity for obtaining high open-circuit voltage cells.

Therefore, emphasis for both process development and device development was placed on low-resistivity silicon material because recent models have predicted that 0.1-ohm-cm silicon has the potential for the required 0.70V open-circuit voltage if bandgap narrowing effects are minimized. Ion implantation was selected as a processing tool because junction dopant profiles as well as peak dopant concentration can be independently varied over a wide range, thereby custom tailoring the emitter layer.

Initial device structures were fabricated to assess the effects of dopant concentration and dopant profile on open-circuit voltage. Concurrent efforts were also directed at optimization of both pulsed electron beam annealing and furnace annealing, since all annealing mechanisms are dependent on implant dose levels. Subsequent efforts were then directed at reduction of surface recombination. Finally, the processing procedures developed during assessment phase of this effort were applied to fabrication of solar cells utilizing the best features of the parameter assessment.

SECTION 2
TECHNICAL DISCUSSION

2.1 BACKGROUND

Ion implantation is a processing tool which has been available for approximately 10 years to the semiconductor industry. The technique allows the device designer precise control of ion species, ion energy, dopant concentration, and dopant profile when properly utilized. Recently[5] the processing method has been applied to the requirements of high-efficiency solar cells with considerable success, and higher throughput, production machines are now becoming available. Typical machine performance is 200 - 300 wafers per hour for solar cell implant parameters. These rates are compatible with most of the other semiconductor process equipment now in use.

The basic objective of this contract was to apply state-of-the-art ion implantation processing, implant equipment, and suitable annealing procedures to high-efficiency solar cell fabrication.

2.1.1 Ion Implantation Facilities

The general requirements for utilization of ion implantation for p-n junction formation include a mass resolution of better than 1 amu, ion energy within a range of 25 - 200 keV, and the ability to transport wafers in and out of the vacuum chamber.

Solar cell implants require implant parameters that are somewhat different from other semiconductor devices. First, lower ion energy is desirable to maintain shallow junctions and adequate blue response. To date, the best solar cells have been processed with ion energies of 5 - 10 keV. Second, higher implant doses are required for solar cells than for most integrated circuit technology to allow reasonably low sheet resistance for the large-area diodes.

The specific machine requirements of this effort included the ability to employ multiple implant parameters, assessment of implantation into wafers at $77^{\circ}K$, and implantation of ions at very large angles of incidence. Each of these modifications to standard practice was evaluated for tailored junction solar cells.

Figure 2-1 shows a photograph of the Extrion Model 200-20A ion implanter that was used for the junction studies under this contract. The machine has a deceleration option for operation within the 5- to 25-keV range. The major components of the medium current ion implanter are shown in Figure 2-2. Figure 2-3 shows a photograph of
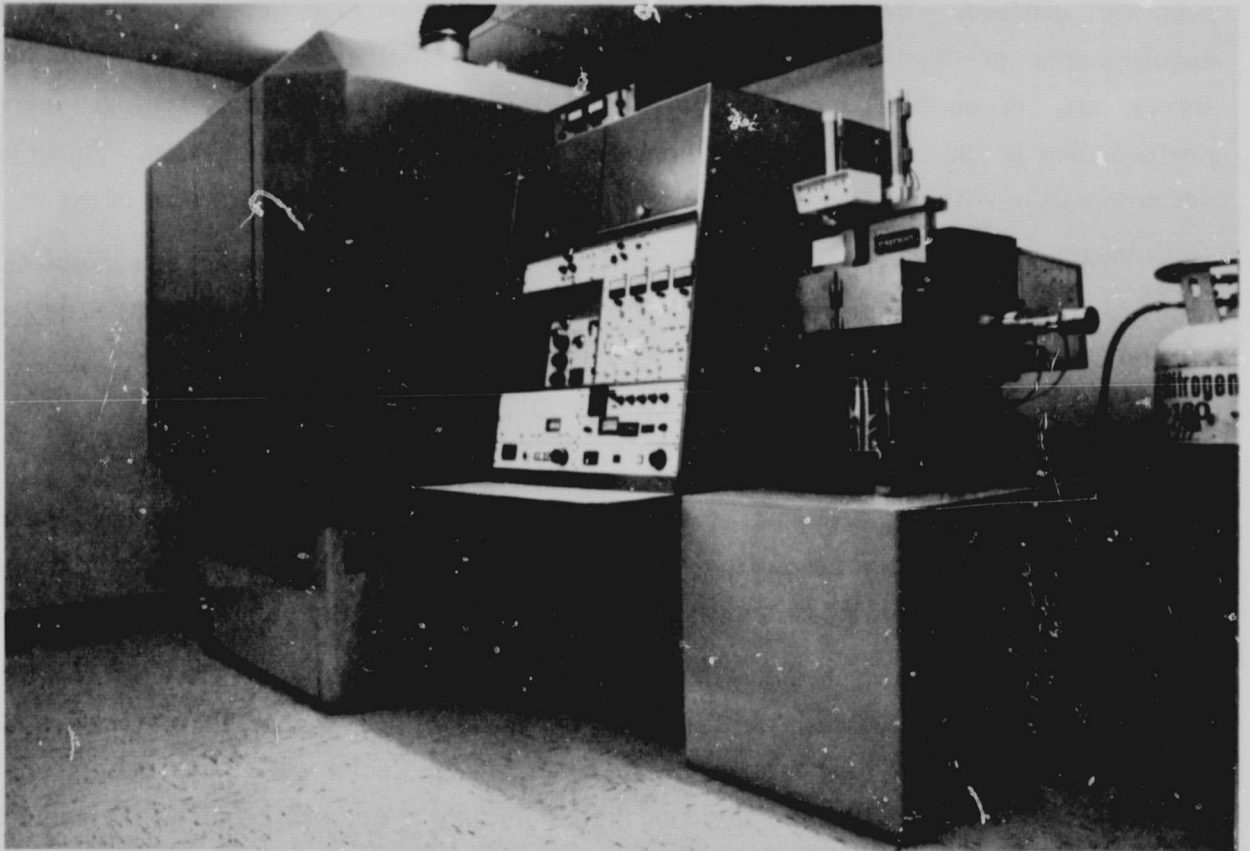
FIGURE 2-1. SPIRE R&D ION IMPLANTER — EXTRION MODEL 200-20A

ANALYZING
MAGNET

BEAM
SCANNER

END STATION
FOR
WAFER PROCESSING

ACCELERATION
OR
DECELERATION
POTENTIAL

ACCELERATION
POTENTIAL

−

+

ION
SOURCE

SOURCE
GAS
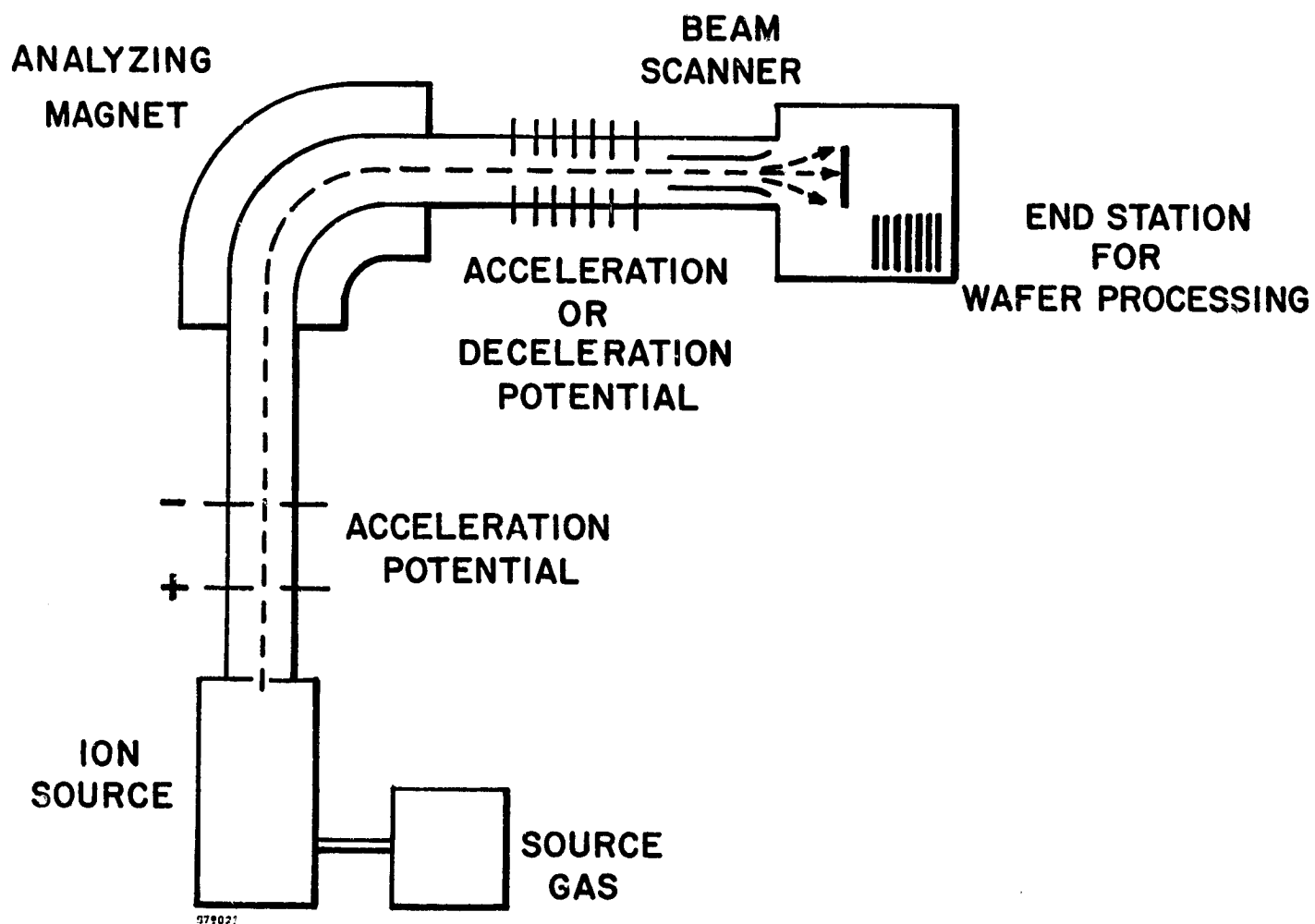
FIGURE 2-2. SYSTEM SCHEMATIC FOR MEDIUM CURRENT ION IMPLANTER
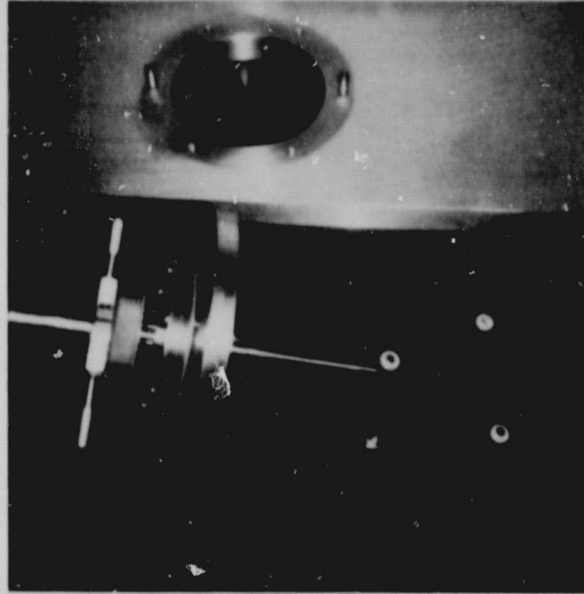
FIGURE 2-3.   WAFER HOLDER FOR HIGH-ANGLE, LOW-TEMPERATURE
ION IMPLANTATION

a modification made to this machine which allows implantation at room temperature or at77°K (cooling by liquid nitrogen) with the ion beam directed at any angle to the wafer surface. The standard end station for the Extrion 200-20A employs only ambient temperatures and beam angles between normal and a few degrees off normal relative to the wafer.

2.1.2   Pulsed Electron Beam Annealing Facilities

An alternative method to furnace annealing of ion implantation radiation damage in silicon and other semiconductor devices is pulsed energy deposition.[6] The method utilizes a high-intensity, short-duration, directed-energy source to produce surface temperature transients sufficient for annealing by the liquid-phase epitaxial regrowth mechanism. Suitable directed-energy sources include pulsed lasers and pulsed electron beams; both are line-of-sight processes that can be applied to selected regions of the semiconductor.

The necessary hardware for electron beam generation and propagation is shown in Figure 2-4 and described in more detail elsewhere[7]. The typical electron beam energy spectrum for this anode-cathode configuration is shown in Figure 2-5; the average electron energy is only 12 keV. A calculated depth-dose profile for the average electron energy is shown in Figure 2-6, and the typical diode current and voltage time

① TRANSMISSION LINE ⑤ SAMPLE ⑨ VACUUM CHAMBER
② CATHODE ⑥ SAMPLE WAFER
③ ANODE GRID ⑦ GROUND PLANE
④ BEAM MASK ⑧ VERTICAL POSITIONER

TO PULSE GENERATOR AND VACUUM PUMP
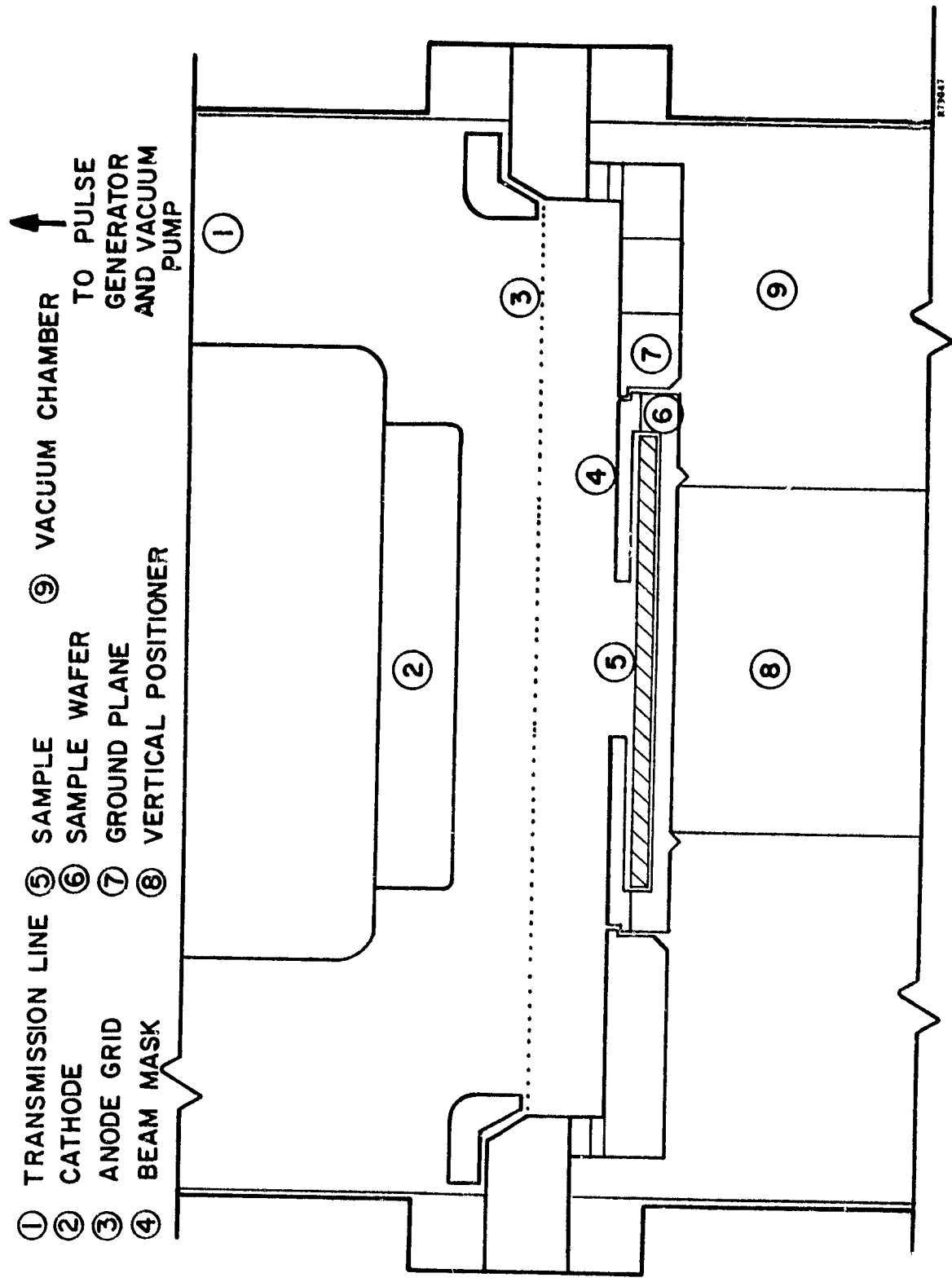
FIGURE 2-4. SCHEMATIC OF PULSED ELECTRON BEAM ANODE-CATHODE GEOMETRY FOR ANNEALING ION-IMPLANTED WAFERS

2-5
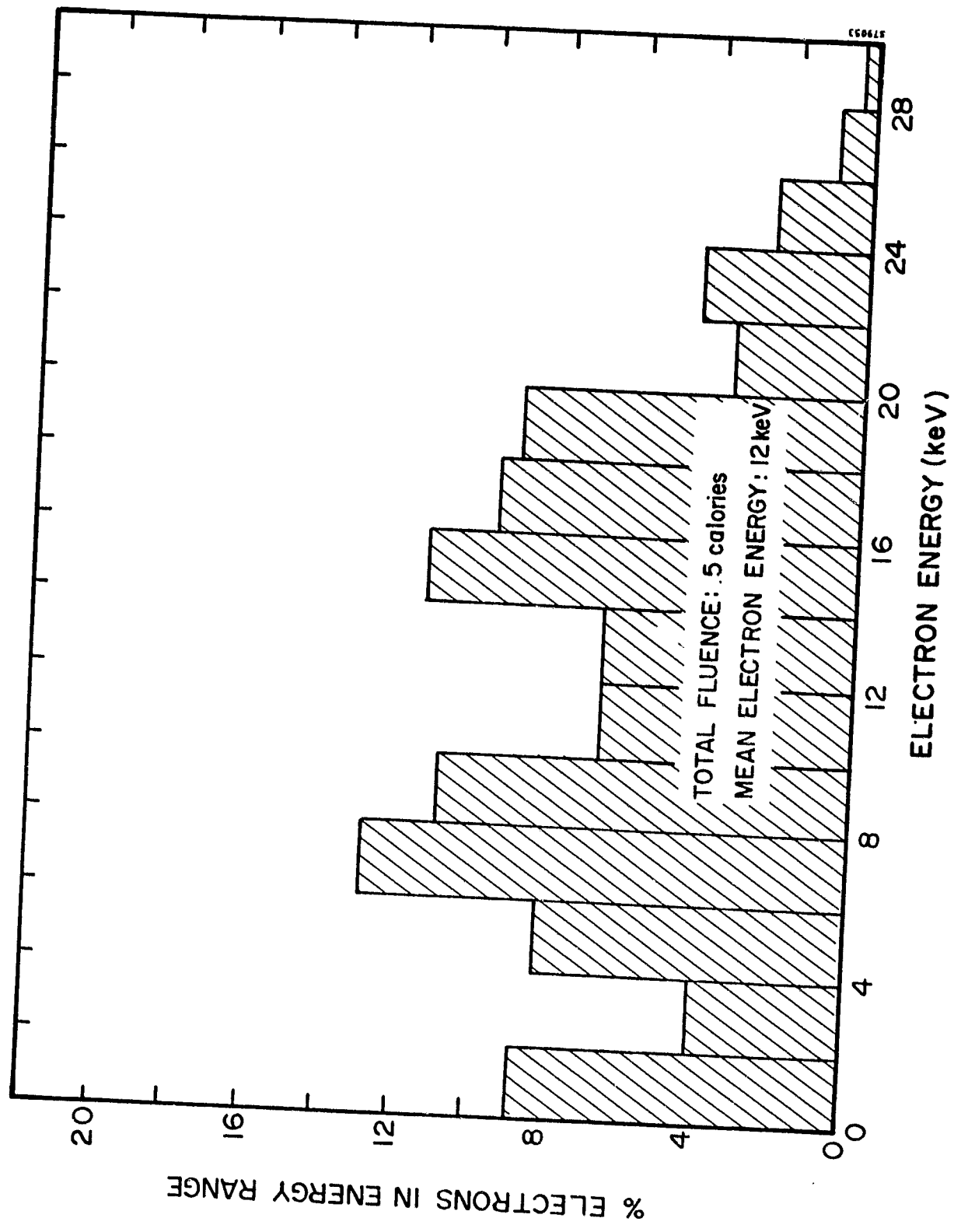
FIGURE 2-5. PULSED ELECTRON BEAM ENERGY SPECTRUM
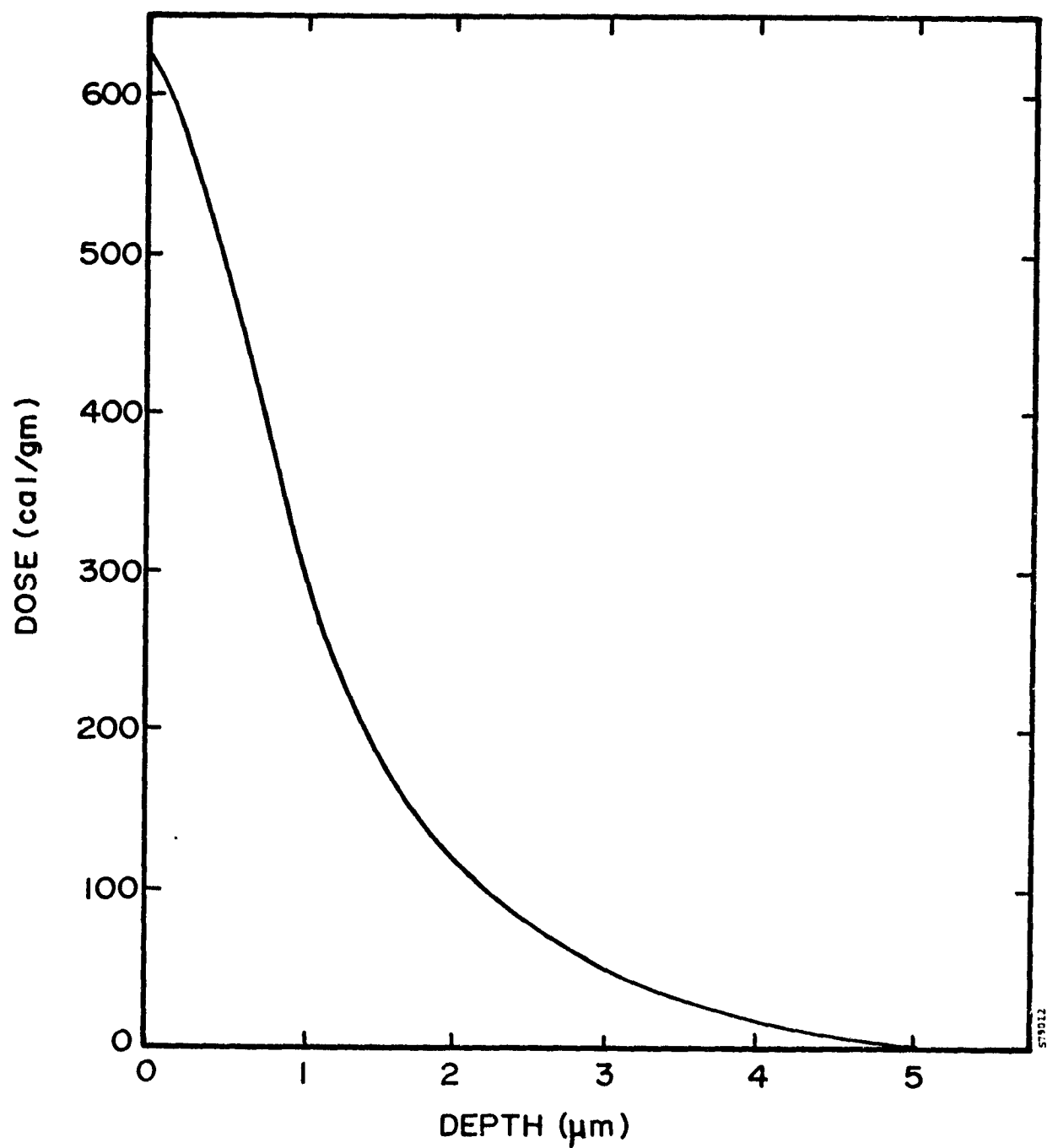
FIGURE 2-6. CALCULATED ENERGY DEPTH-DOSE PROFILE FOR
PULSED ELECTRON BEAM IN SILICON

dependence is shown in Figure 2-7. A VXTEMP[8] computer program was used to determine the temperature profile as a result of pulsed electron beam deposition at a fluence of 0.2 cal/cm^2. Figure 2-8 shows the results of this calculation plotted as a function of time following deposition of the electron beam. Note that the front surface is predicted by this model to rise above its melting point for 300 nanoseconds. After 200 nanoseconds the deposited energy is lost by heat transfer to the unmelted, single-crystal substrate, and crystal growth occurs epitaxially with excellent structure.

2.2   PROCESS DEVELOPMENT AND OPTIMIZATION

2.2.1   Preliminary Evaluation of Low Dose Ion Implantation and Annealing Processes

The efforts described here were directed at understanding the limitation of simple low-dose implanted junctions with emphasis on improving the annealing methods. During this phase of the investigation, single ion energies were employed for junction introduction.

The phosphorus-implanted junction studies consisted of low-dose $^{31}P^+$ implants with various furnace- and pulse-annealing methods. To determine the sensitivity of V_{oc} on annealing technique, isochronal furnace annealing, pulse annealing, and combined pulse-/furnace-annealing processes were assessed. The implant doses for the tests were calculated based on a simple bandgap narrowing model:[4]

$$dEg = 3.4 \times 10^{-8} (N_d^{1/3} - 2.65 \times 10^6) \, eV$$

where dEg, the change in bandgap energy, is only 0.035 eV for N_d, the dopant concentration, of 5×10^{19} cm^{-3}. To achieve this dopant concentration in the junction, the implant dose is 5×10^{14} $^{31}P^+$ cm^{-2} at 5 keV. Following implantation into wafer resistivities within the range of 0.1- through 10.0-ohm-cm, the slices were furnace annealed with an isochronal test matrix as follows:

1. 550°C – 2 hours
2. 750°C through 950°C in 50°C increments – 30 minutes
3. 550°C – 2 hours
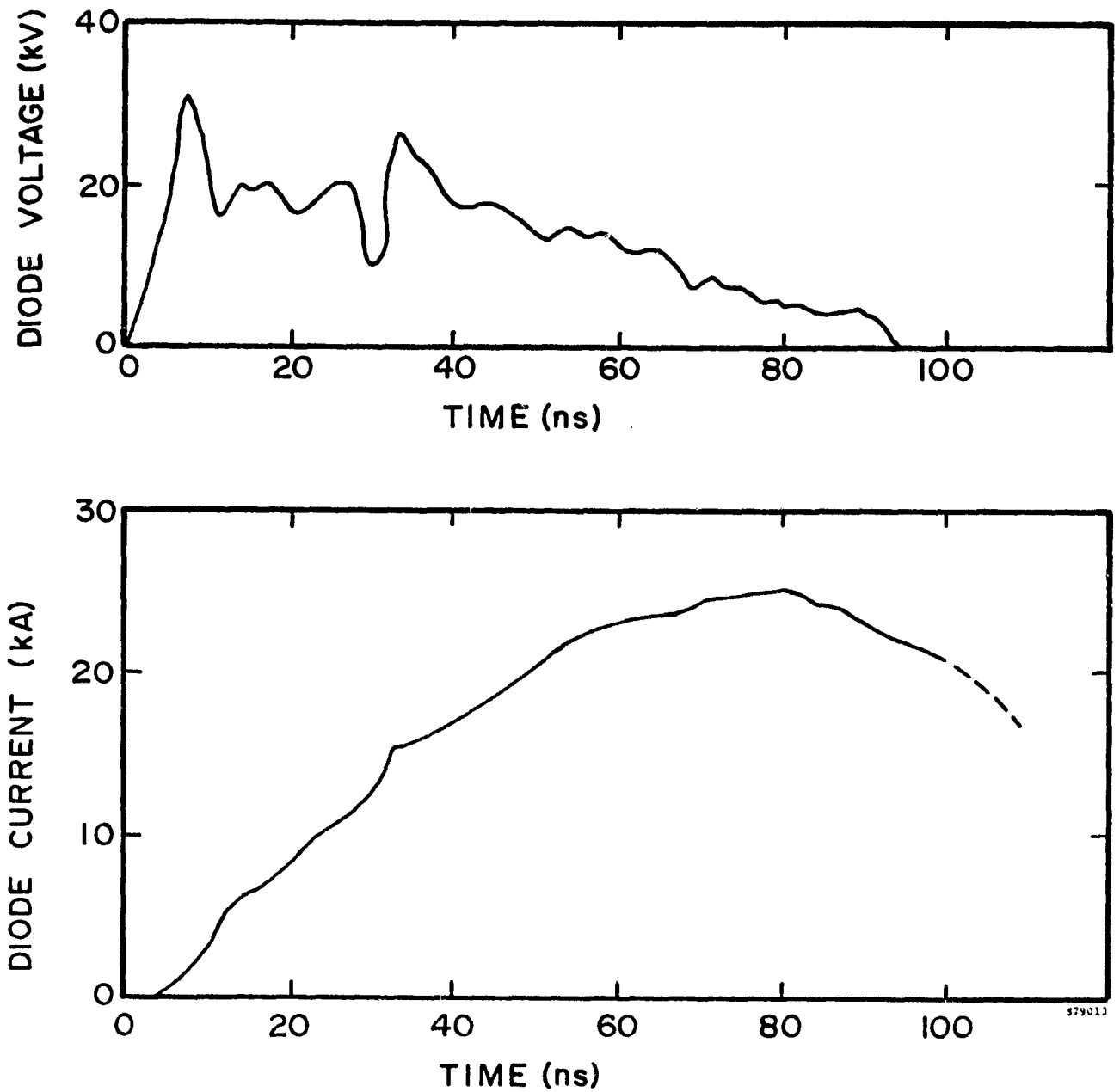
FIGURE 2-7. VOLTAGE (CORRECTED FOR di/dt) AND CURRENT
ACROSS CATHODE-ANODE GAP
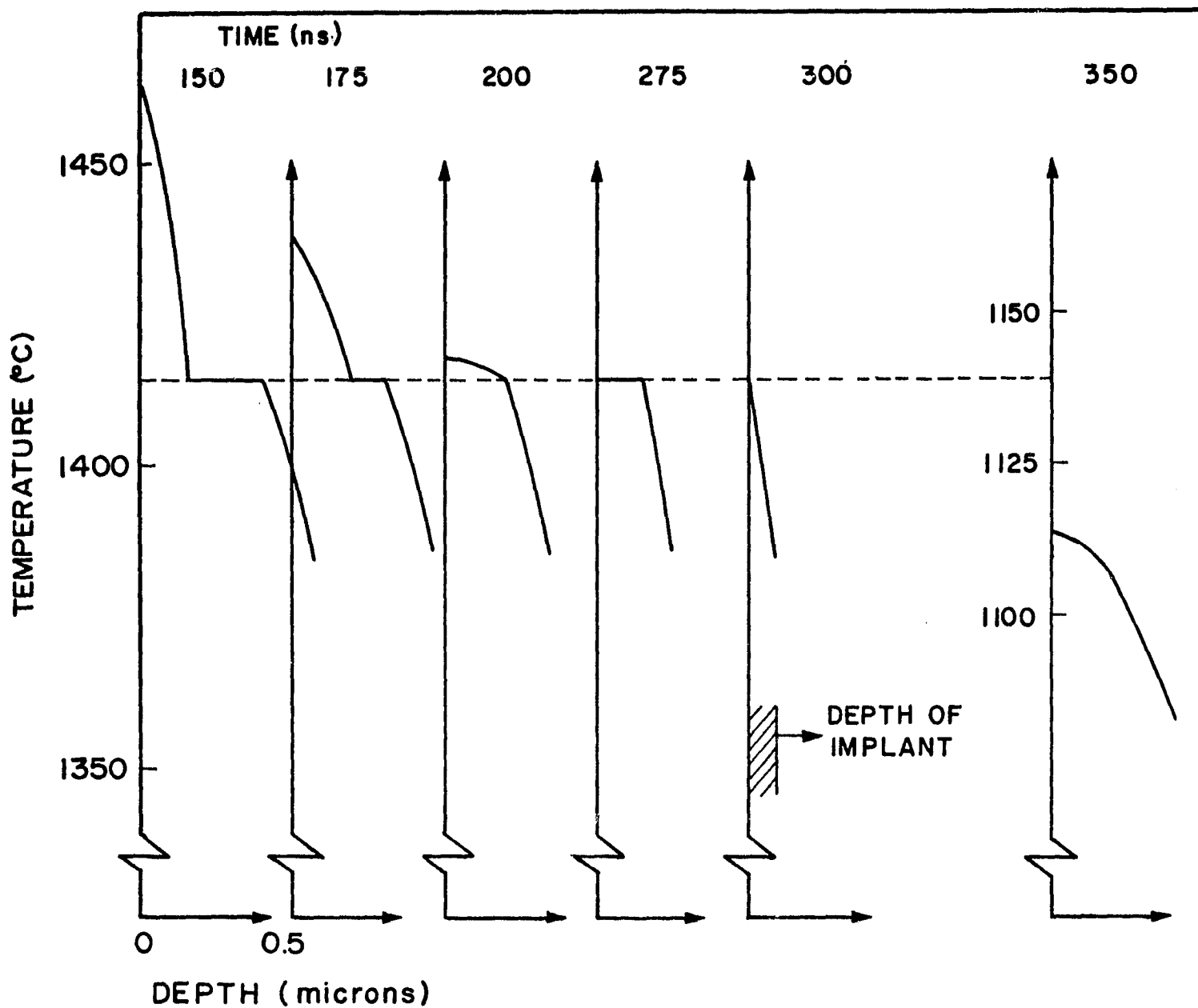
FIGURE 2-8.   CALCULATED TEMPERATURE PROFILE DURING PULSED
ELECTRON BEAM ANNEALING FROM VXTEMP OUTPUT

Figure 2-9 shows the results of this low-dose test following furnace annealing. The measured open-circuit voltage still did not exceed 600 mV, even with decreased junction layer doping concentration and a wide range of annealing conditions. Either of two voltage-limiting mechanisms can explain these results: incomplete annealing or surface recombination.

Because of the initially low V_{oc} results achieved in the first low-dose phosphorus anneal matrix, the use of $^{28}Si^+$ predamage implants was investigated. By first implanting the silicon lattice with silicon ions, the junction layer can be made amorphous prior to actual dopant implantation with phosphorus. The advantage of first making the layer amorphous is that the presently optimized furnace-anneal procedure, developed for relatively high dose levels, can be used. Pulsed electron beam annealing parameters are also dependent upon the degree of amorphization of the implant region, with best results achieved with higher implant levels.

Furnace Annealing

The second low-dose, furnace-anneal test matrix utilized two wafers each with resistivities of 0.1, 0.3, 0.5, 1.0, and 10 ohm-cm. The cell structure was processed as follows:

Predamage Implant: 2×10^{15} $^{28}Si^+$ cm^{-2} at 10 keV

n^+ Implant: 5×10^{14} $^{31}P^+$ cm^{-2} at 10 keV

or

1×10^{14} $^{31}P^+$ cm^{-2} at 10 keV

p^+ Implant: 5×10^{15} $^{11}B^+$ cm^{-2} at 25 keV

Anneal: $550^{\circ}C$ for 2 hours
$850^{\circ}C$ for 15 minutes
$550^{\circ}C$ for 2 hours

The maximum dopant concentration predicted for implants of 5×10^{14} $^{31}P^+$ cm^{-2} is approximately 1×10^{20} cm^{-3}. For implants of 1×10^{14} $^{31}P^+$ cm^{-2}, peak concentration is estimated at 5×10^{19} cm^{-3}.

2-11
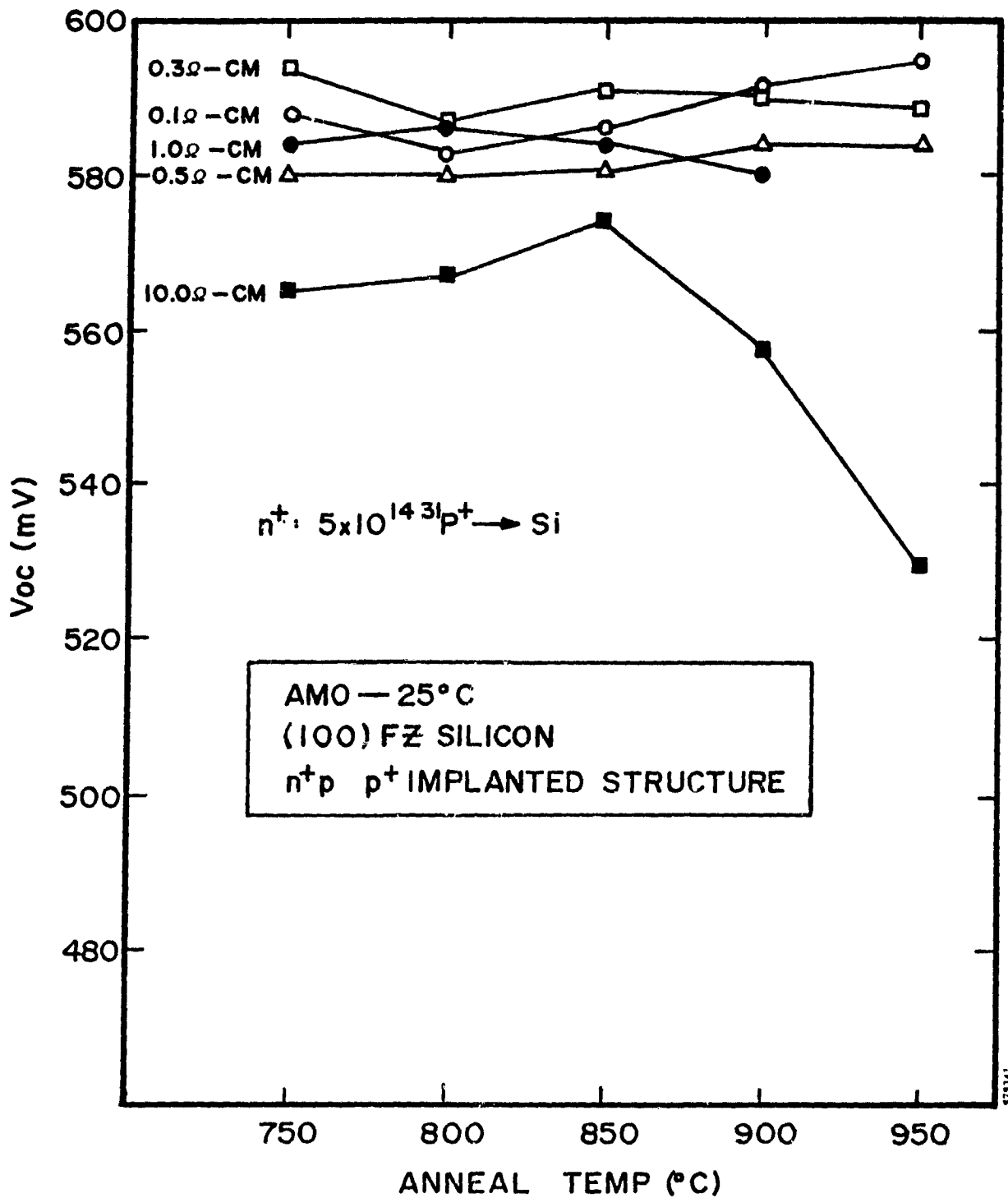
FIGURE 2-9. ISOCHRONAL ANNEALING BEHAVIOR OF LOW-DOSE JUNCTION
IMPLANTS IN SILICON OF VARIOUS RESISTIVITIES

Sheet resistance and open-circuit voltage measurements under AM0-25°C conditions were made. Test results are summarized in Figure 2-10. These results show that the lower dose phosphorus implants, with silicon ion predamage, have a lower V_{oc} performance when compared to both the high-dose 2×10^{15} $^{31}P^{+}$ cm^{-2} and low-dose, 5×10^{14} $^{31}P^{+}$ cm^{-2} implants without silicon predamage.

Pulsed Electron Beam Annealing

Additional low-dopant-concentration experiments were performed using silicon ion predamage to make the front surface of the wafer amorphous before implanting a relatively small amount of phosphorus. It is believed that amorphous silicon will regrow into single-crystal silicon epitaxially during the PEBA anneal in a more controlled manner than nonamorphous material. Initially the wafers received a 2×10^{15} $^{28}Si^{+}$ cm^{-2}, 10-keV implant to make an amorphous layer on the front surface. The wafers were then implanted with various doses of 5-keV phosphorus ions, PEBA annealed, and post-PEBA furnace annealed at 675°C for 2 hours. V_{oc} point-probe measurements were done under AM0-25°C conditions. The results are shown in Figure 2-11. Again, these results show increasing V_{oc} with higher implant doses, even with a high-concentration silicon implant to assure amorphization.

Furnace Annealing of Arsenic Implants

In addition to the detailed investigation of low-dose phosphorus implants, arsenic implantation was assessed for low-dose application to n^{+} layers. The differences between arsenic-implanted junctions and phosphorus-implanted junctions are twofold. First, arsenic has a much shorter projected range in the silicon lattice, so that the peak dopant concentration is much higher than the equivalent phosphorus concentration. Second, arsenic atoms in the silicon lattice have a lower diffusion coefficient, which means less redistribution during furnace annealing within the 850-950°C temperature range.

The first of these experiments was conducted to address the effect of doping concentration on open-circuit voltage. Twenty-four 0.1-ohm-cm wafers were implanted as follows:

a) 1×10^{14} $^{75}As^{+}$ cm^{-2}, 25 keV, 10°

b) 2.5×10^{14} $^{75}As^{+}$ cm^{-2}, 25 keV, 10°
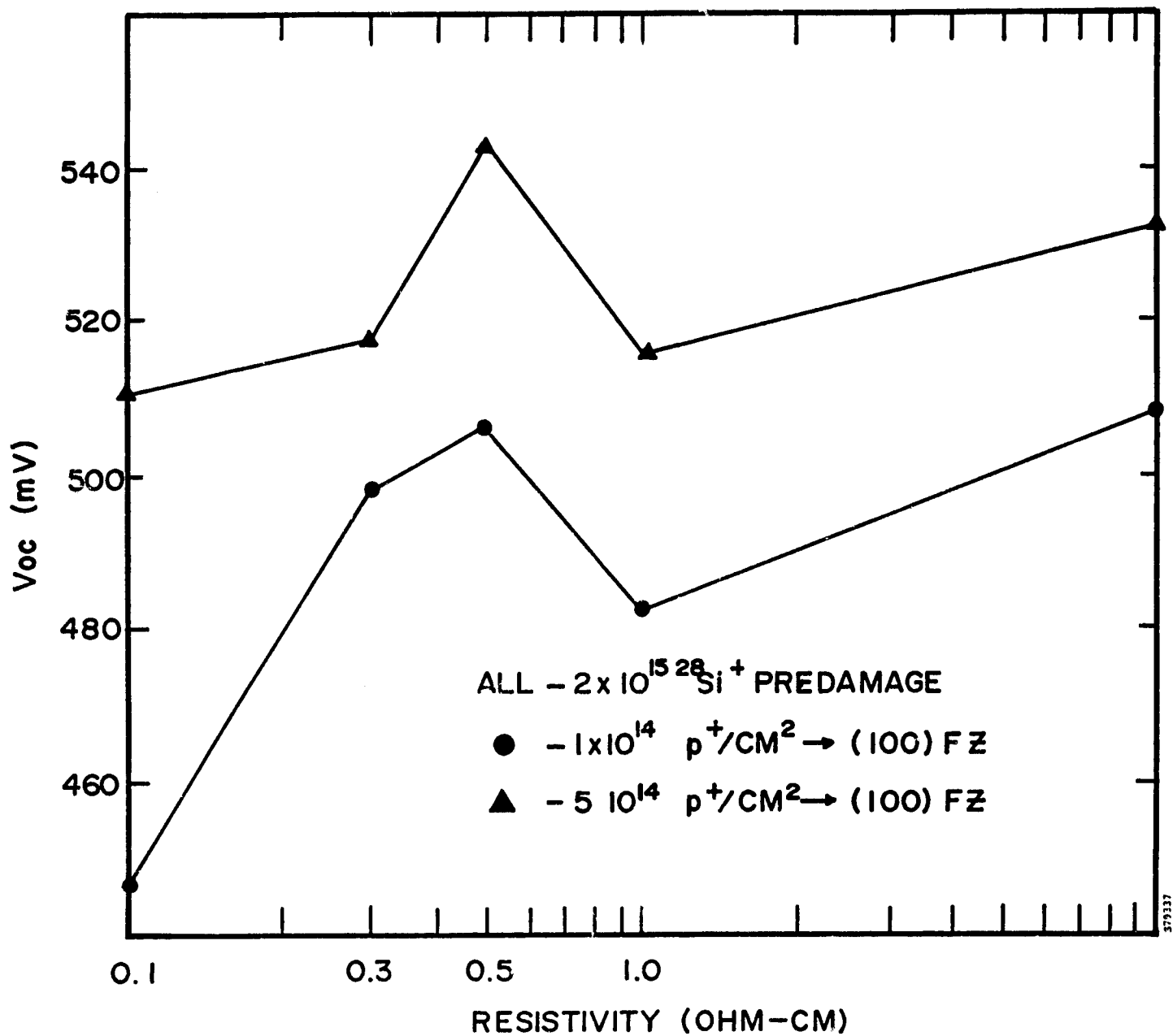
FIGURE 2-10. AVERAGE OPEN-CIRCUIT VOLTAGE (AM0-25°C) FOR
LOW-DOSE $^{31}P^+$ IMPLANTS FOLLOWING SILICON
PREDAMAGE IMPLANTATION
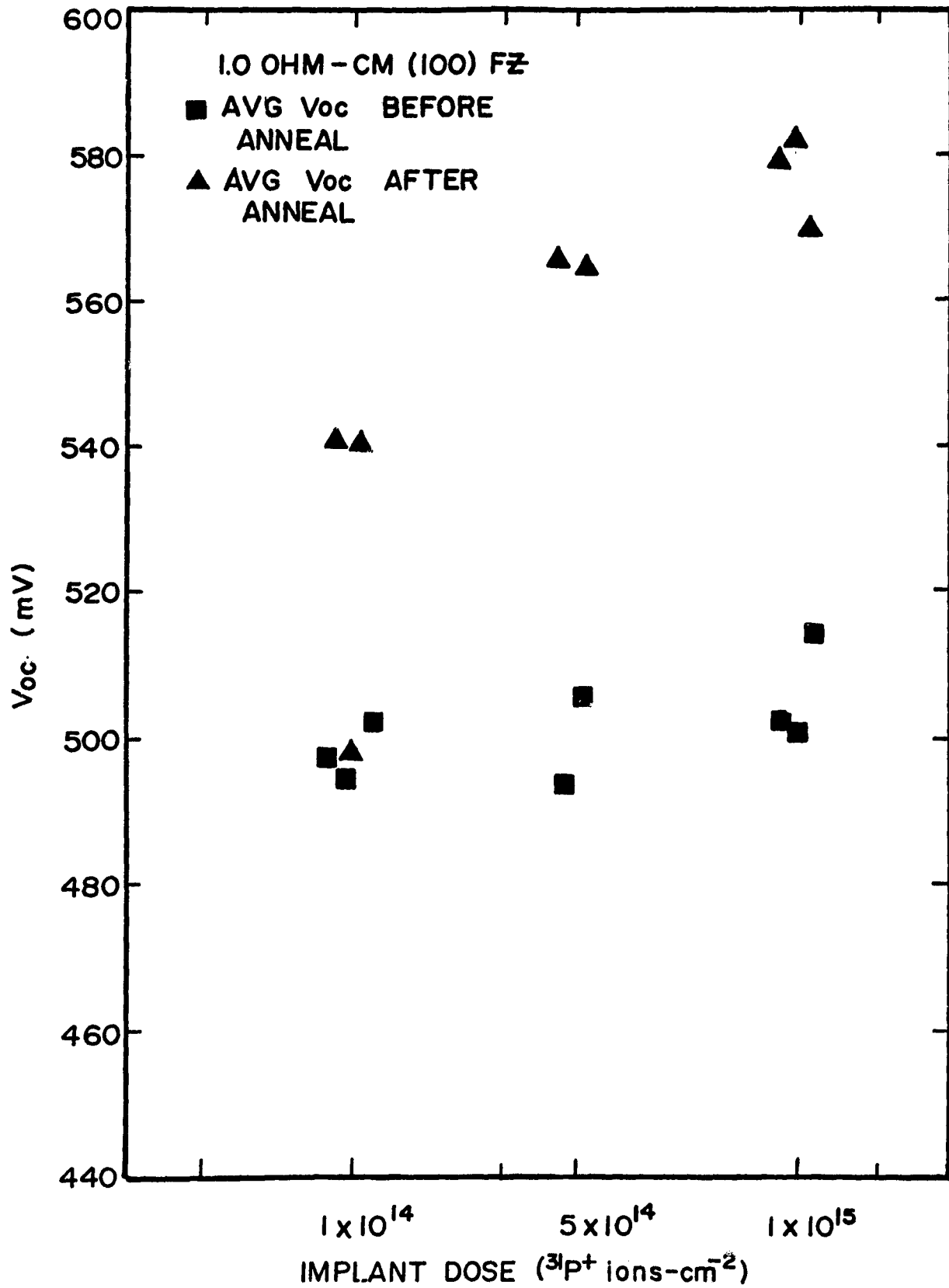
FIGURE 2-11.   OPEN-CIRCUIT VOLTAGE AS A FUNCTION OF IMPLANT DOSE
AFTER PEBA AND AFTER 675°C - 2-hr POST-PEBA ANNEAL
(Note: All wafers received 2×10^{15} $^{28}Si^+$ cm^{-2}
predamage prior to $^{31}P^+$ implant.)

c) 5×10^{14} $^{75}As^+$ cm^{-2}, 25 keV, 10°

d) 1×10^{15} $^{75}As^+$ cm^{-2}, 25 keV, 10°

All the wafers were then annealed at 500^oC for 3 hours, which, according to results by Nishi[9], will result in nearly complete activation of the implanted arsenic. The test results, as shown in Figure 2-12, are in agreement with trends observed for phosphorus implants. The test matrix demonstrates that simply decreasing implant dose, and therefore dopant concentration, will not improve the junction open-circuit voltage.

The investigations discussed above evaluated low-temperature, long-period annealing of arsenic implants. A secondary experiment was designed to test the applicability of Nishi's[9] results to the improvement of V_{oc}. Both crucible grown and float-zone 0.1-ohm-cm silicon wafers were implanted wth 2.5×10^{14} $^{75}As^+$ cm^{-2}. The wafers were then annealed isochronally at various temperatures. All anneals were within 450 to 650^oC in 50^oC increments for 3 hours. The tests results are shown in Figures 2-13 and 2-14. From these annealing test data, it is apparent that higher temperatures improve V_{oc} performance. Although 500^oC - 3-hour anneals can completely activate implanted arsenic into the lattice, the higher V_{oc} values were achieved after 650^oC annealing. The higher temperature anneals do not necessarily increase the percentage of activated arsenic ions, but probably cause enough arsenic diffusion in silicon to change the dopant profile slightly, perhaps to a more optimized shape.

2.2.2 Optimization of Ion Implantation Annealing Processes

High-efficiency solar cell fabrication based on ion implantation of the dopants requires adequate annealing of the crystal lattice damage. The characteristics of the lattice damage depend on implant energy, dose, ion species, and the temperature of the wafer during implantation.[10] The substrate temperature is a function of the beam current and the wafer holder temperature, so that the general trend with increasing beam current density is more difficult annealing.

Three generalized cases with different annealing requirements can be distinguished, and are shown in Figure 2-15 and summarized below:

Low-dose implants, less than 10^{14} ions-cm^{-2}, result in isolated defect clusters which can be effectively annealed by solid-state epitaxial regrowth at temperatures below 550^oC. Under some conditions, the implant can be annealed in situ with elevated substrate temperatures.
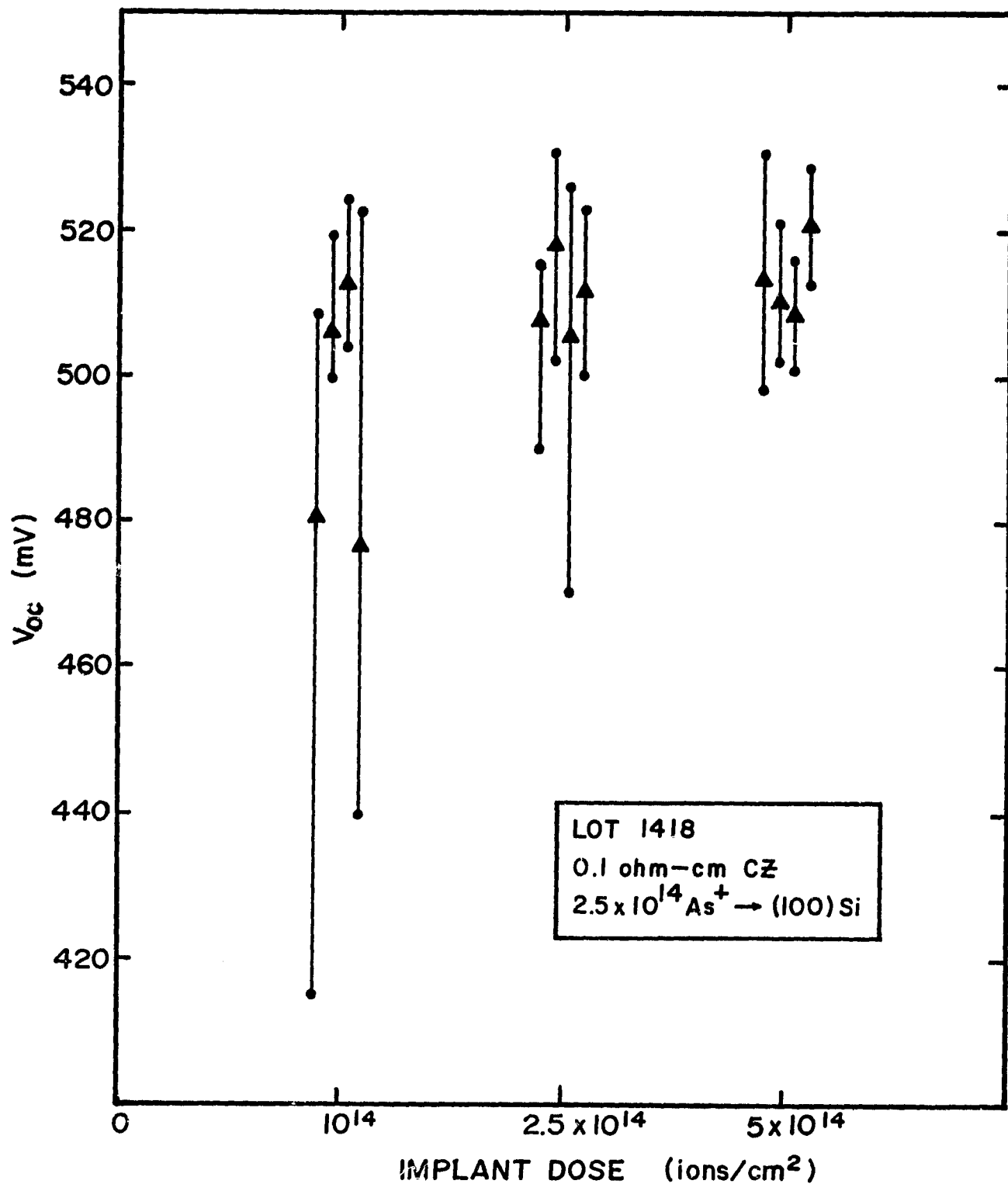
FIGURE 2-12. OPEN-CIRCUIT VOLTAGE FOR LOW-DOSE ^{75}As$^+$ IMPLANTED JUNCTIONS FOLLOWING 500°C – 3-hr ANNEAL
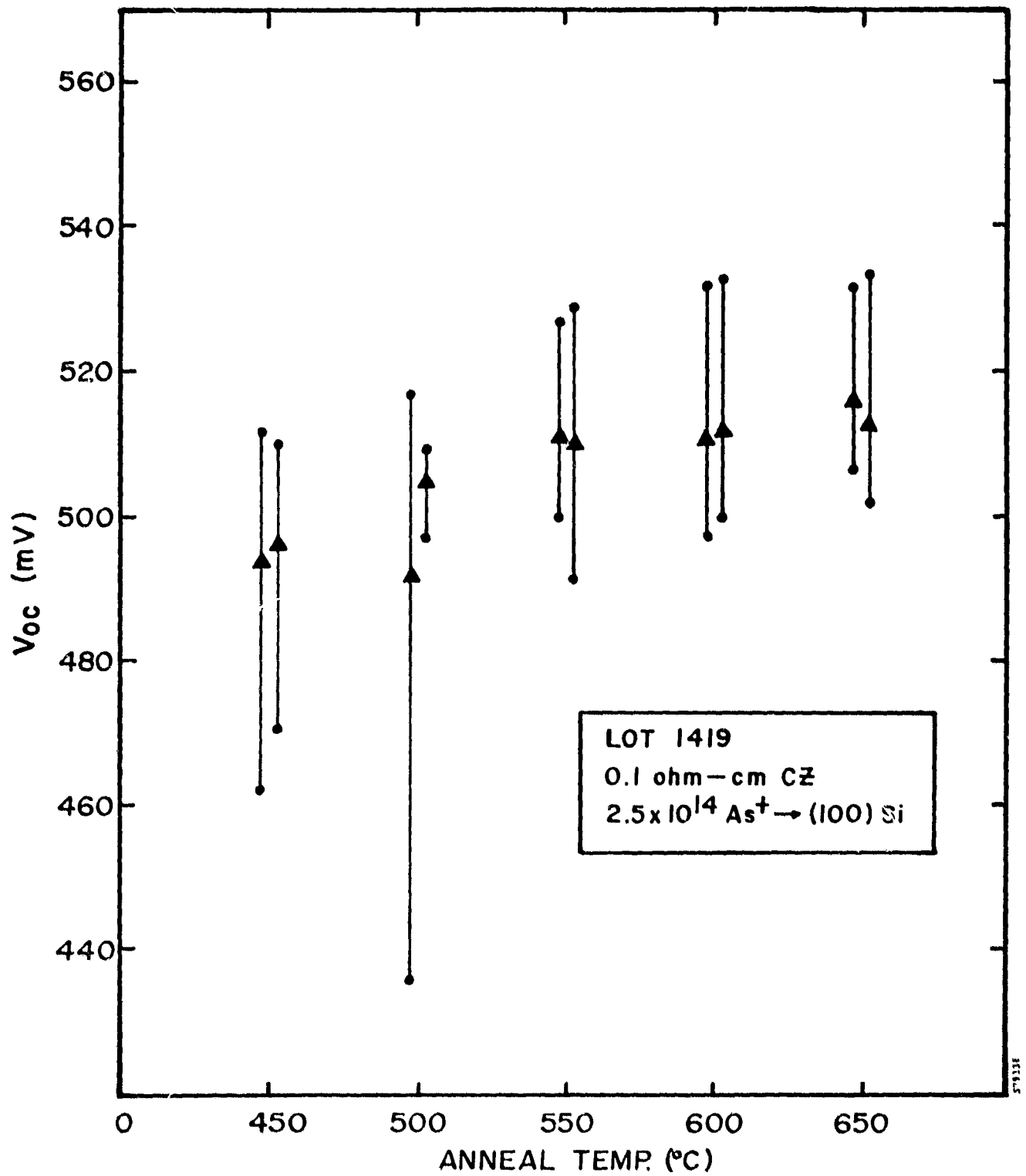
FIGURE 2-13. OPEN-CIRCUIT VOLTAGE FOR LOW-DOSE ^{75}As$^+$ IMPLANTED JUNCTIONS IN CRUCIBLE GROWN SILICON FOLLOWING VARIOUS ANNEALING TEMPERATURES
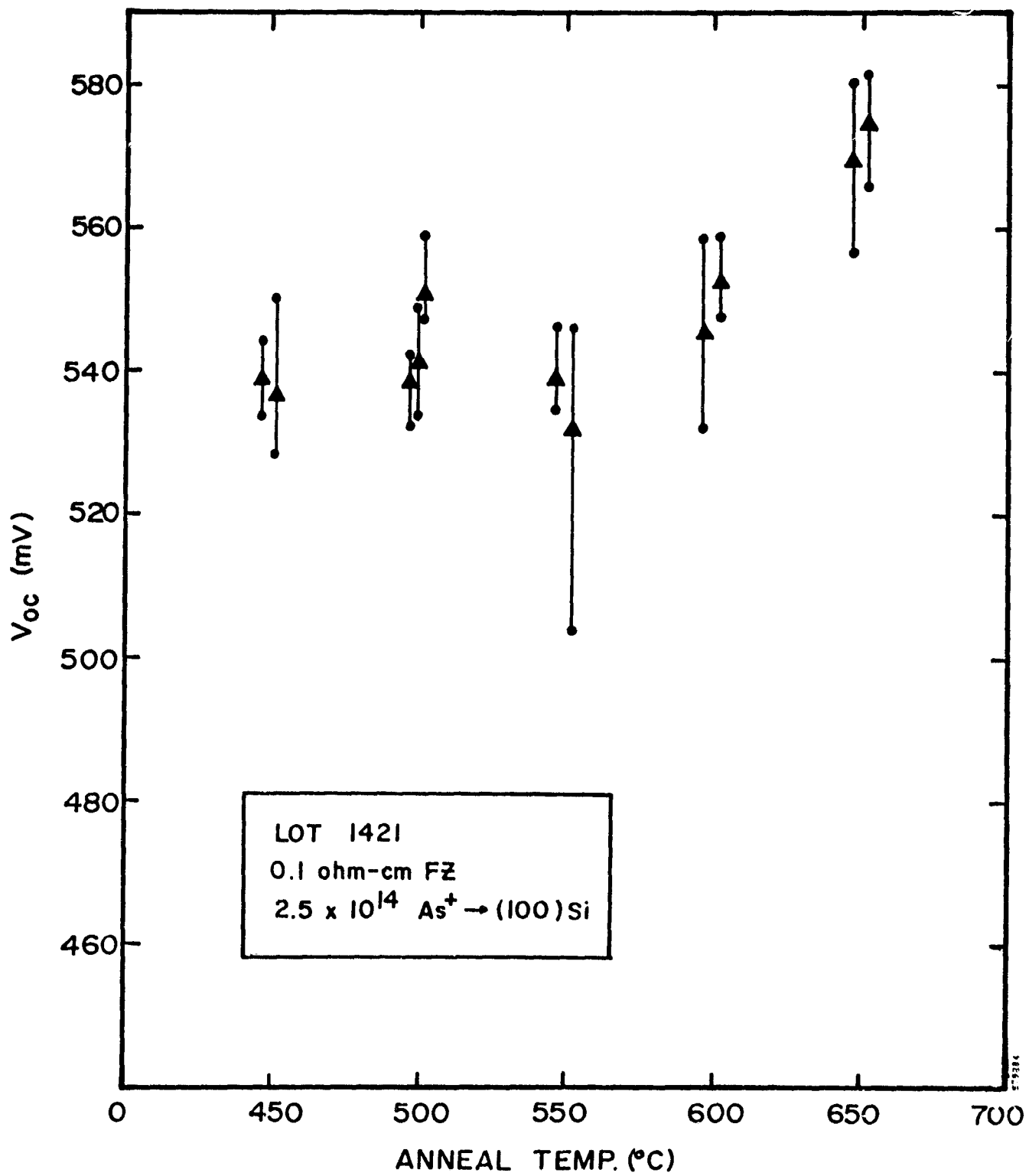
FIGURE 2-14. OPEN-CIRCUIT VOLTAGE FOR LOW-DOSE $^{75}As^+$ IMPLANTED JUNCTIONS IN FLOAT-ZONE SILICON FOLLOWING VARIOUS ANNEALING TEMPERATURES
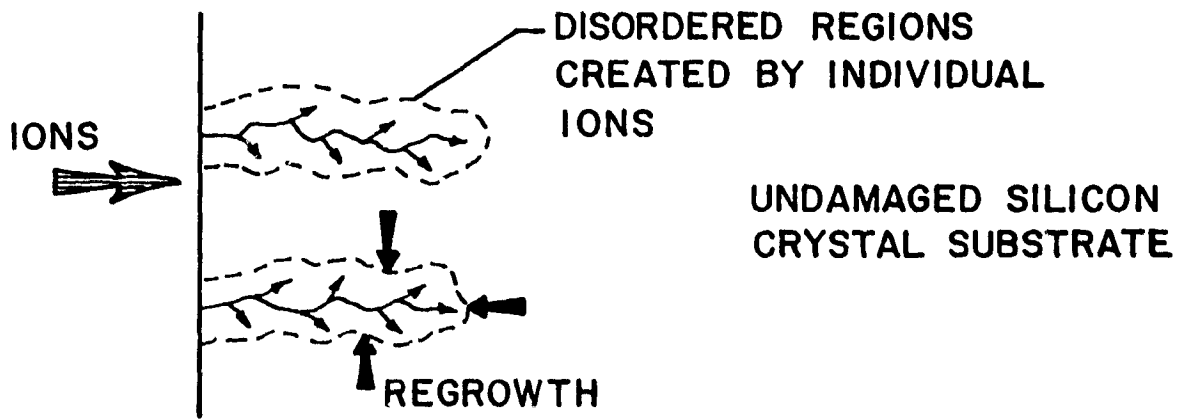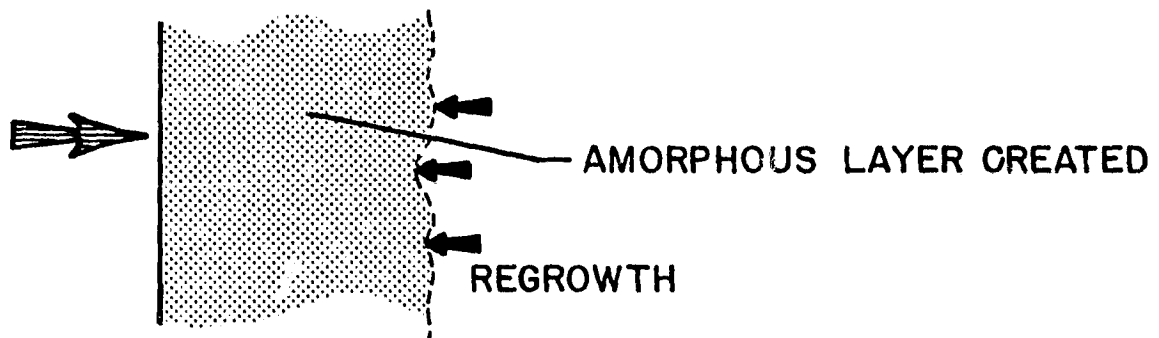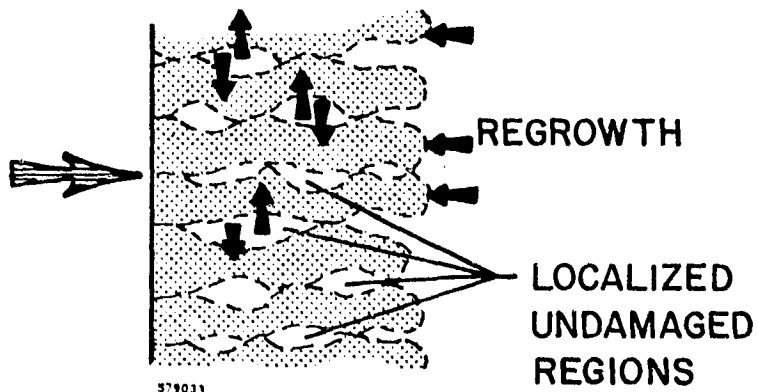
FIGURE 2-15. TYPICAL IMPLANT DAMAGE FOR VARIOUS IMPLANT DOSES

Intermediate-dose implants, at the 10^{15} ions-cm^{-2} level, result in localized undamaged regions from which competing regrowth fronts propagate; however, intermediate-dose implants can lead to polycrystallite formation unless carefully annealed by either multistep furnace methods (described in Section 2.1.4) or by pulsed electron beams.

High-dose implants, greater than 5×10^{15} ions-cm^{-2}, result in amorphous layers provided the substrate temperature does not rise above ambient. Temperature increases can result in high-current, high-energy implants when the incident power density becomes excessive. Solar-cell implant doses have so far been in the intermediate range described, and much effort has been required to develop furnace-annealing parameters that promote single-crystal, solid-phase epitaxial regrowth. The following sections describe the results of studies performed to optimize both furnace- and pulse-annealing for low-resistivity silicon.

Typical solar cell implant parameters fall within the intermediate dose range and careful procedures are necessary to properly anneal the implant damage in a furnace. By using liquid nitrogen cooling of the wafer, completely amorhous layers can be produced, making good epitaxial regrowth easier; however, such low-temperature implants are not amenable to automation. Low-temperature substrates also act as cryopanels within the vacuum system and as a result, considerable hydrocarbon condensation occurs.

Requirements for annealing room-temperature implants can be summarized as:

1. To restore the silicon crystal lattice while minimizing defect sites which increase minority carrier recombination rates

2. To activate the implanted dopant ions for achieving the required sheet resistance, by causing them to take positions within the crystal lattice.

This must be achieved while:

3. Maintaining a shallow junction depth for adequate blue response

4. Preserving or enhancing the bulk silicon minority carrier lifetime.

Furnace Annealing

Much effort has been expended in developing furnace annealing parameters that promote single-crystal epitaxial regrowth and minimize defect concentration. Figure 2-16 shows results from a helium ion backscattering and channeling analysis for multi-step furnace annealing with resultant lattice structures[11]. The absence of backscattering signal is due to channeling, which depends upon the quality of the regrowth. The data shows that better lattice recovery results from multi-step anneals. Multi-step annealing schedules have been developed, such as the following:

1. First-step anneal: Temperature range between 450 and 600°C; time of 1 hour. This step causes slow, single-crystal epitaxial regrowth to occur. Figure 2-17 shows typical regrowth rates for (100) and (111) oriented silicon.[12]

2. Second-step anneal: Temperature range between 800 and 900°C; time of 15 - 30 minutes. This step causes the substitution of the dopant atoms into the lattice and allows minor redistribution of the as-implanted dopant concentration.

3. Third-step anneal: Temperature range between 450 and 550°C; time of 1 hour. This step causes bulk lifetime recovery by complexing any residual defects, such as point defects, to carbon or oxygen impurities inherent in any silicon.

Development and optimization of any anneal schedule requires consideration of heating and cooling rates between anneal steps.

Using the annealing approach summarized above, a test matrix for optimization was designed in which 1- and 10-ohm-cm (100) float zone materials were used. Test procedures consisted of 60-minute, isochronal, first-step anneals for all samples at either 450° or 550°C; and 30-minute, high-temperature, second-step anneals over a range of 650° to 850°C, using a new specimen from the samples of the first step at each 50°C temperature increment. The second-step anneal approach differs from earlier attempts by others in which the same samples were used for progressively higher temperatures steps. In effect, these earlier schedules were equivalent to two- or more-step anneals. Results from the optimization test matrices, as shown in Figure 2-18 through 2-21, indicate that a first-step 450° to 550°C anneal does not change the final sheet resistance following a second high-temperature anneal, for either the 1- or 10-ohm-cm float-zone
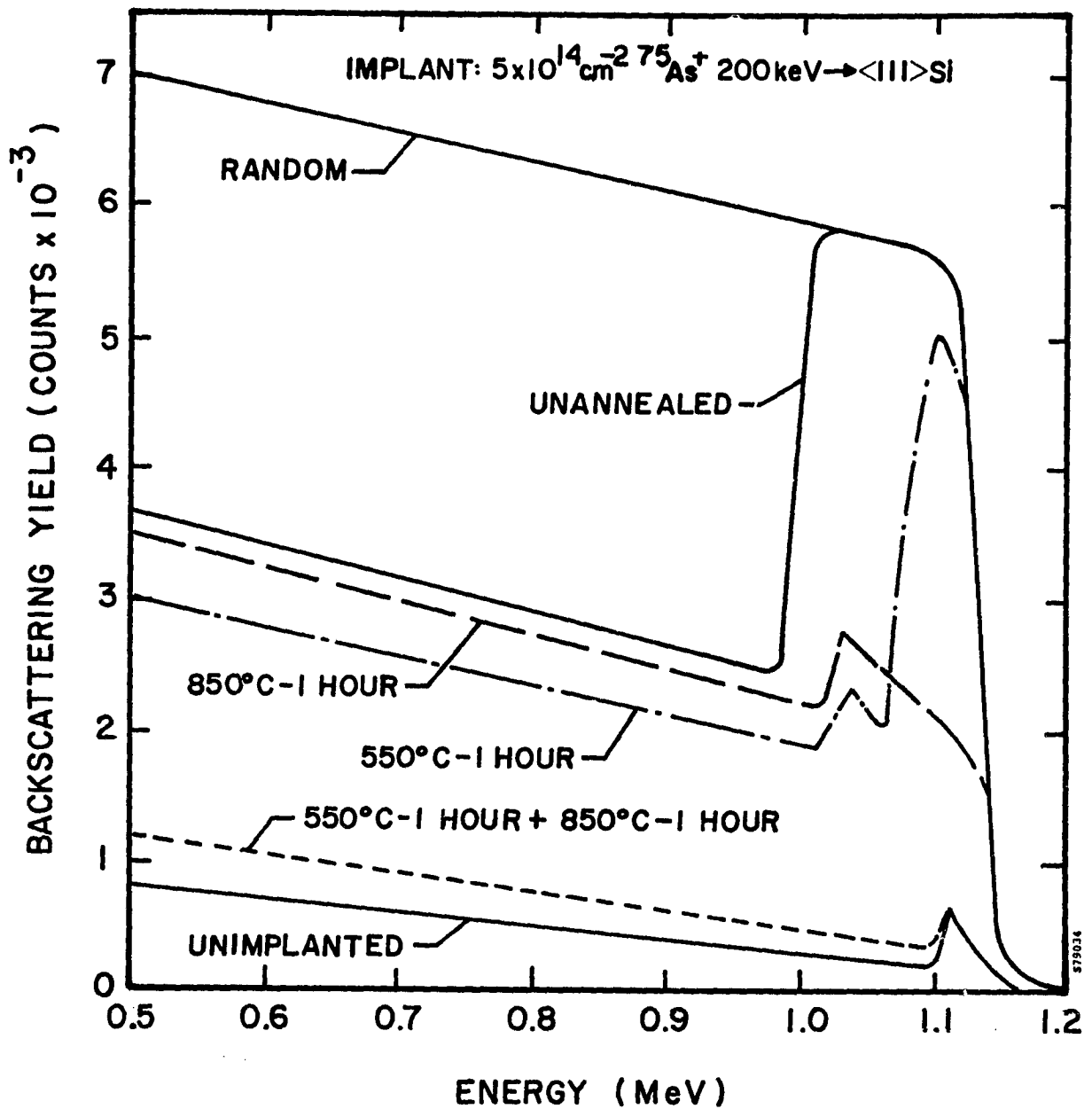
FIGURE 2-16. HELIUM ION BACKSCATTERING AND CHANNELING ANALYSIS
OF IMPLANTED AND ANNEALED LAYER(S)
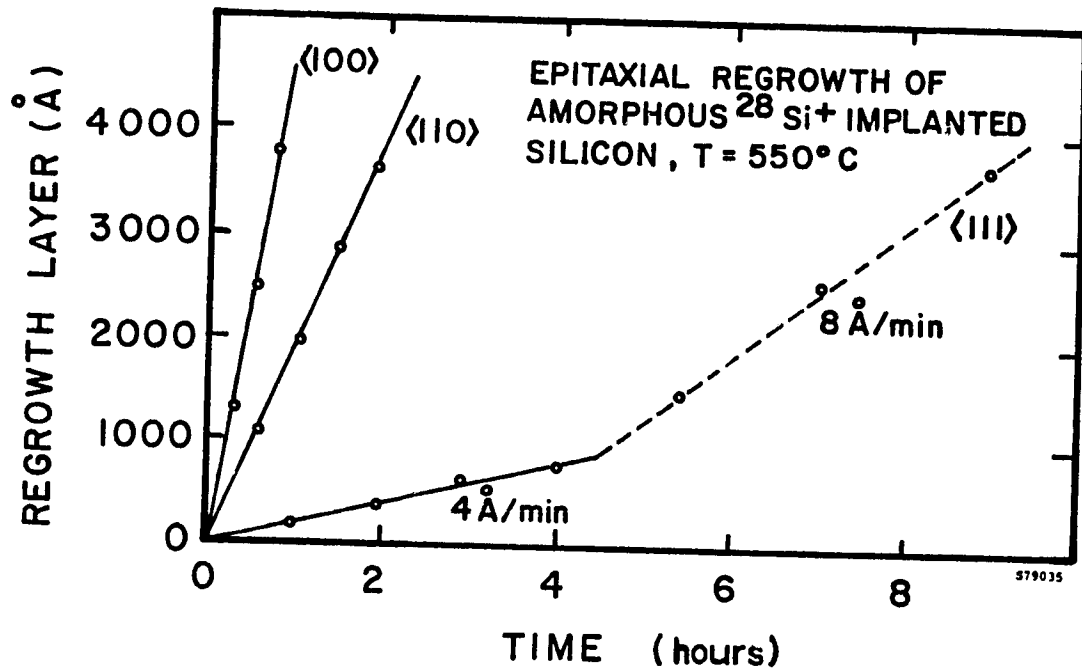
FIGURE 2-17. EPITAXIAL REGROWTH BEHAVIOR FOR IMPLANTED
LAYERS AT 550ºC
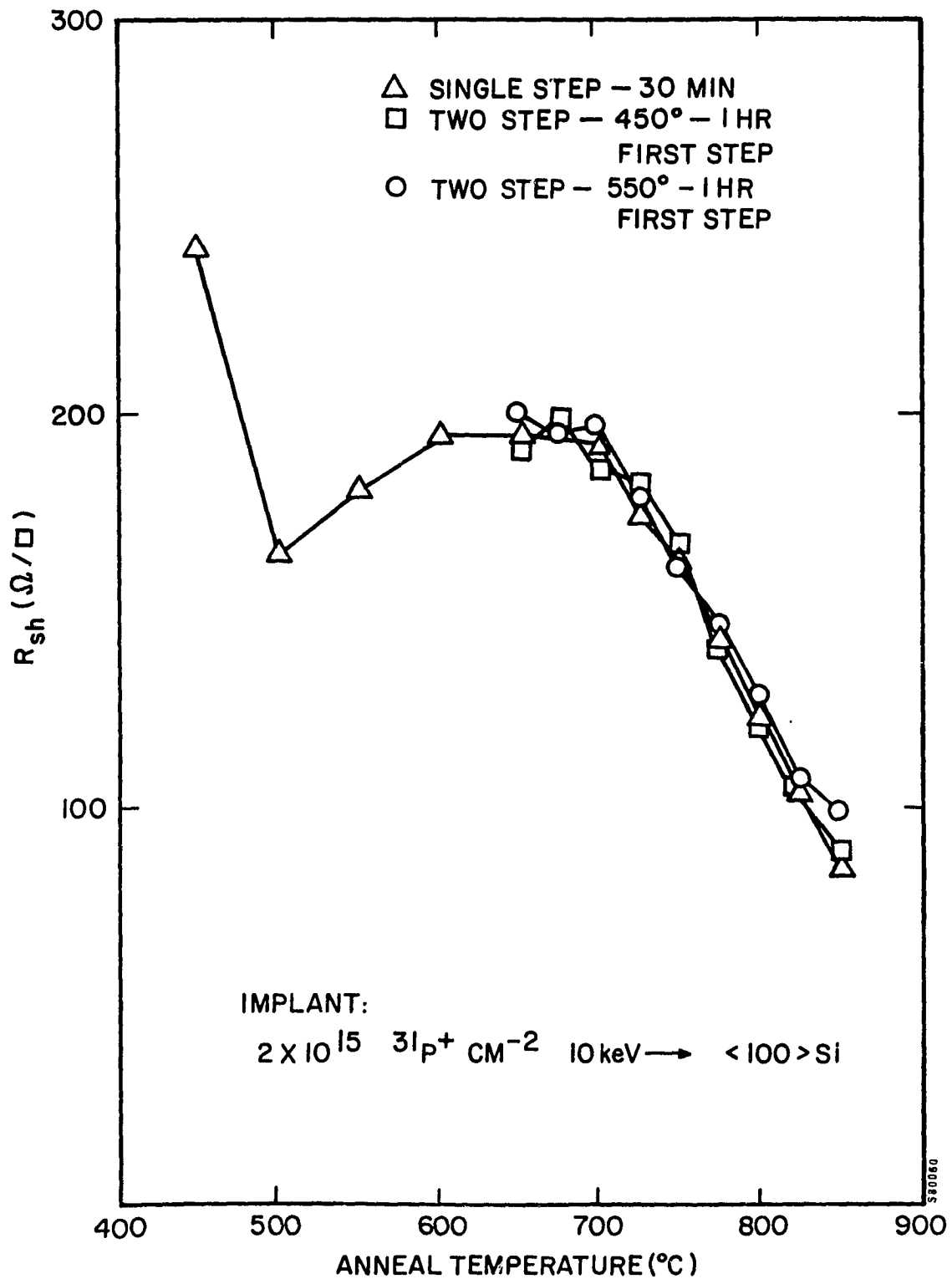
FIGURE 2-18. ISOCHRONAL ANNEALING OF 10-ohm-cm FZ SILICON
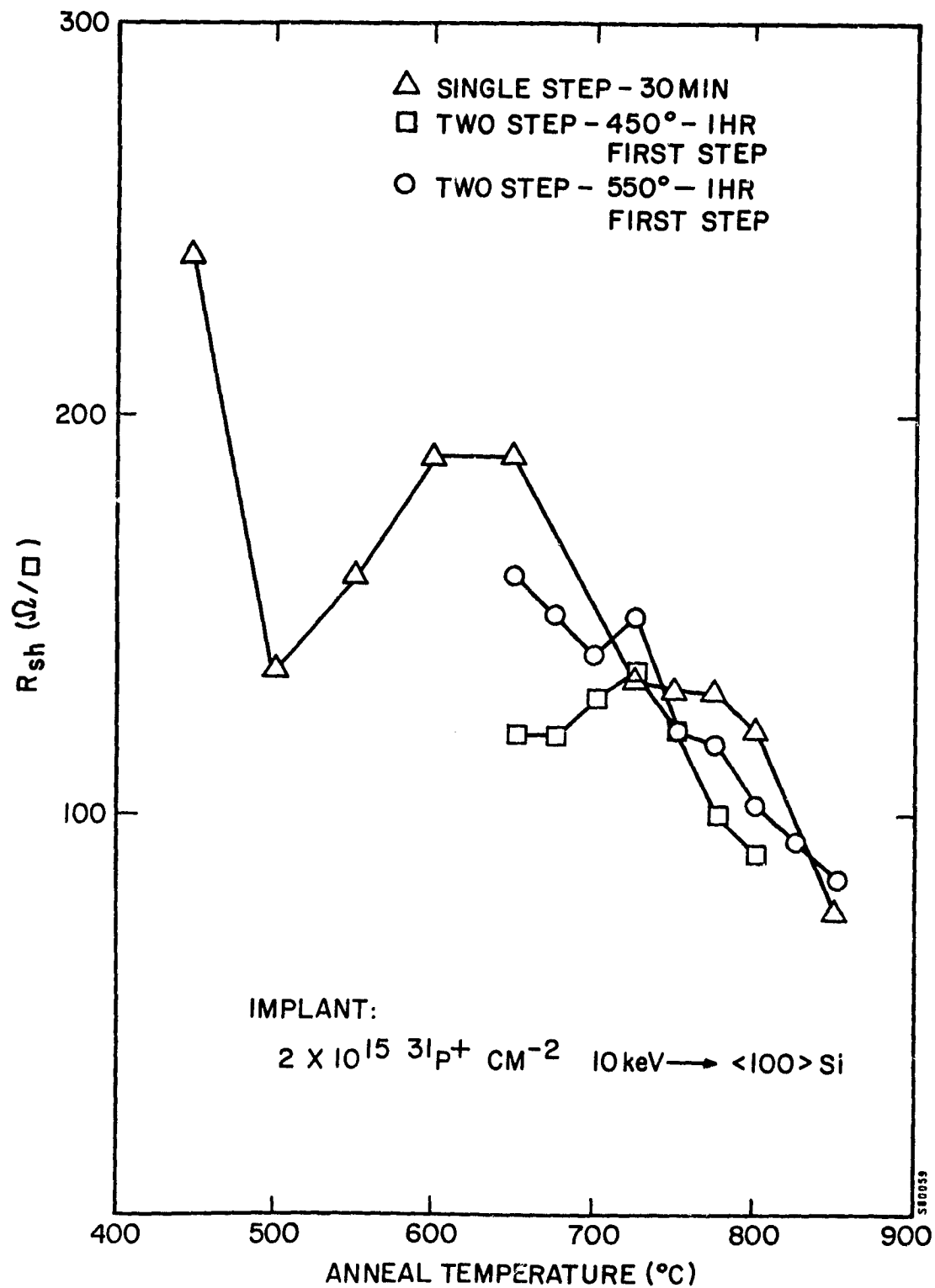
FIGURE 2-19. ISOCHRONAL ANNEALING OF 1-ohm-cm FZ SILICON
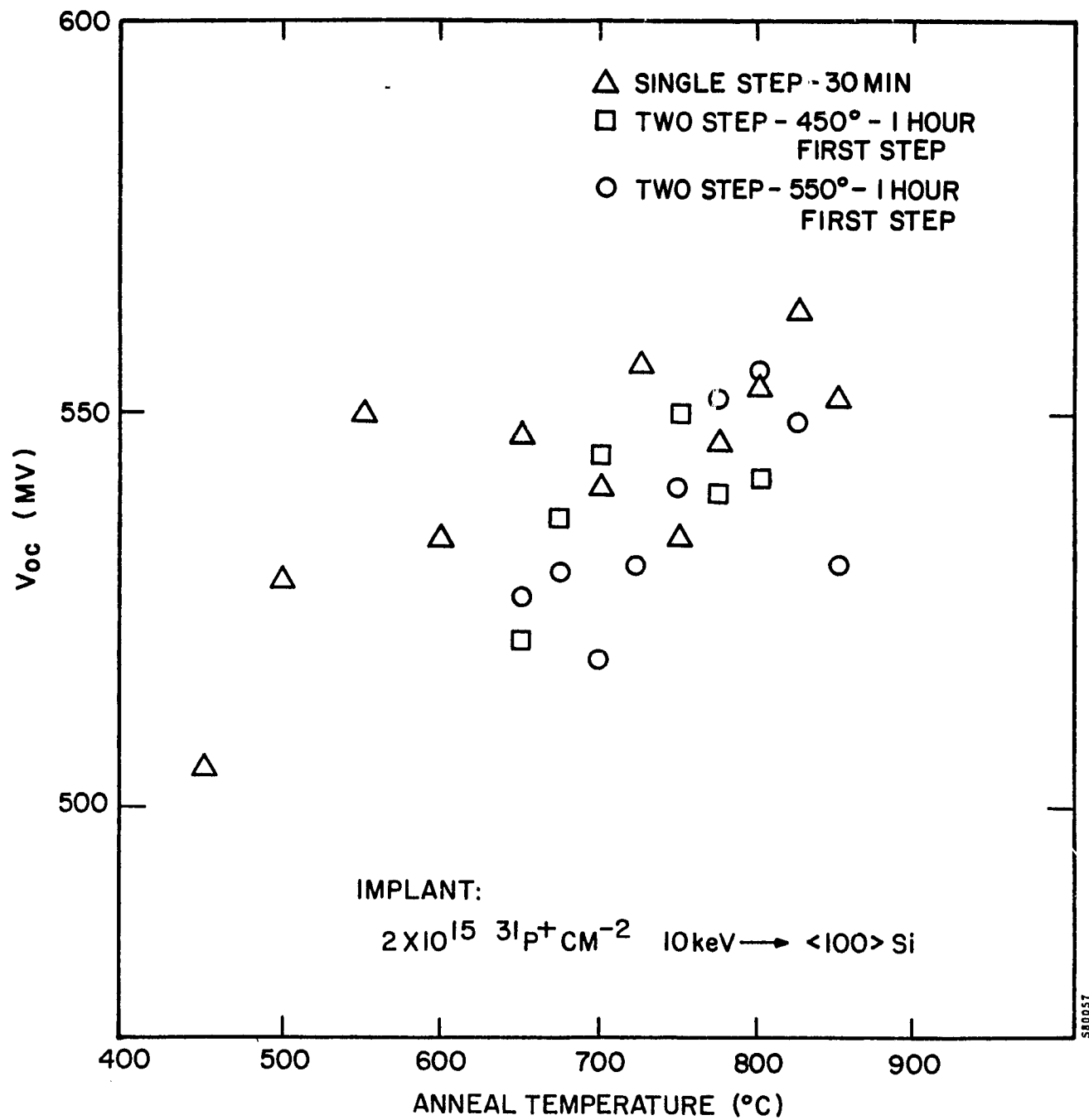
FIGURE 2-20. ISOCHRONAL ANNEALING OF 1-ohm-cm FZ SILICON
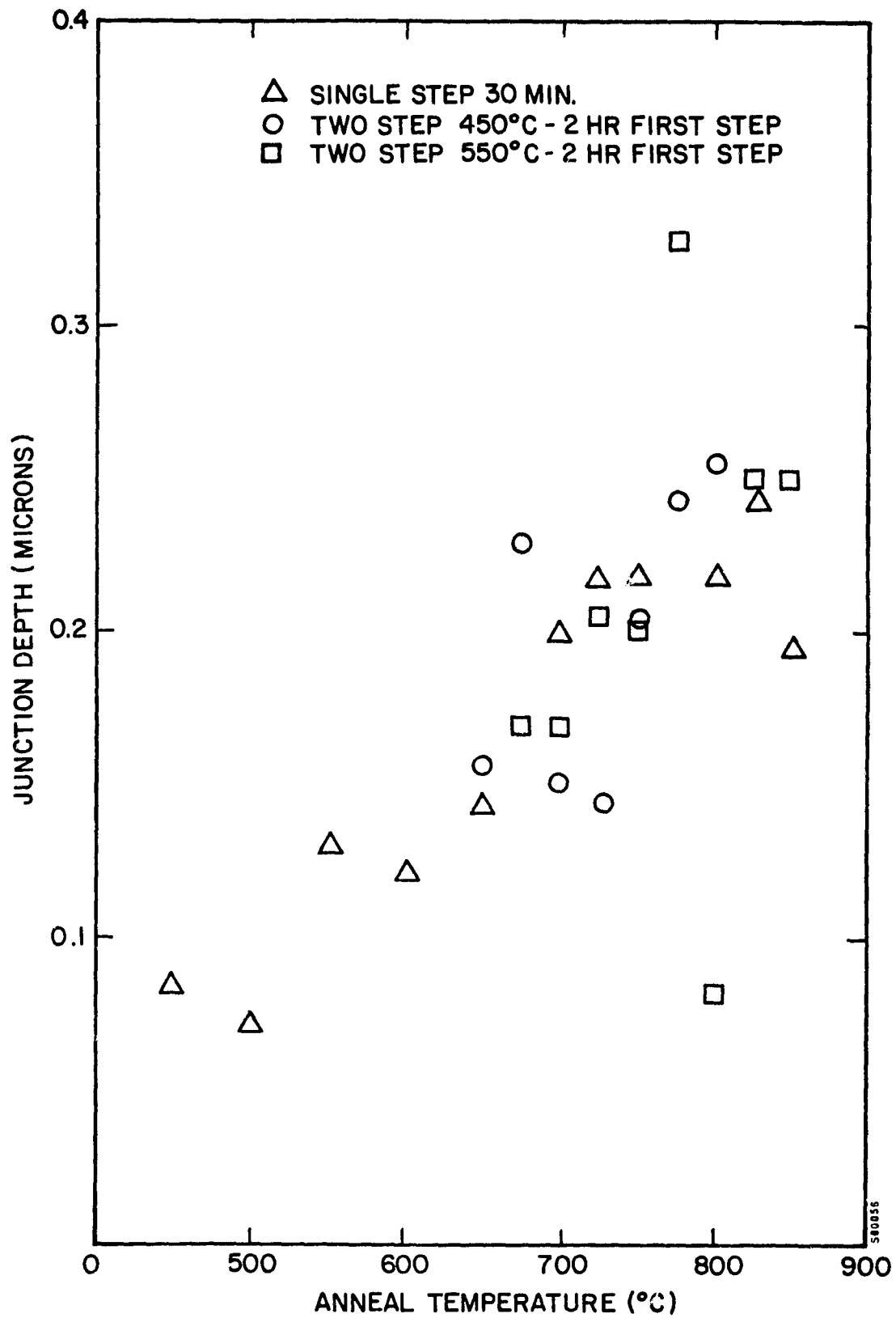
FIGURE 2-21. ISOCHRONAL ANNEALING OF 1-ohm-cm FZ SILICON

silicon. It was also determined, as shown in these figures, that the final junction depth is not significantly deeper if 450° or $550^{\circ}C$, 1-hour first-step anneals are used as shown in Figure 2-22.

2.2.3 Optimization of Furnace Annealing

A three-step[5] furnace-anneal test, in the form of a matrix, was conducted with 40 wafers each of resistivity 0.1, 0.3, 0.5, 1.0, and 10.0 ohm-cm. Half the wafers of each resistivity were implanted with 2×10^{15} $^{31}P^+$ cm^{-2} at 10 keV and half with 2×10^{15} $^{75}As^+$ cm^{-2} at 25 keV. Ion energies were chosen to give 0.3-micron junction depths after annealing. All wafer backs were implanted with 5×10^{15} $^{11}B^+$ at 25 keV for p^+ layers.

After implantation the wafers were annealed by the following three-step schedule:

(i)   2-hour anneal at $500^{\circ}C$ or $550^{\circ}C$

(ii) 30-minute isochronal anneal at $750^{\circ}C$ to $850^{\circ}C$ in $25^{\circ}C$ increments

(iii) 2-hour anneal at 500 or $550^{\circ}C$

Sheet-resistance and open-circuit-voltage measurements were made under AM0-$25^{\circ}C$ conditions; R_{sh} and V_{oc} measurements for each wafer are given in the appendix as Figures A-1 through A-20. Matrix results, summarized in Figure 2-23, show better V_{oc} performance with $550^{\circ}C$ first- and third-step anneals when compared to $500^{\circ}C$ values. The highest V_{oc} values, for all arsenic-implanted wafers, are probably due to a lower diffusion coefficient for the arsenic over the $750^{\circ}C$ to $850^{\circ}C$ temperature range, which may result in retrograde fields. Finally, BSF effects due to the back surface boron implants were obtained for wafer resistivities greater than 0.5 ohm-cm. The BSF effect improves V_{oc} as wafer resistivity increases, as shown in Figure 2-23.

Pulse Annealing

The application of ion implantation in solar cell processing requires an annealing method to remove the inherent radiation damage to the silicon lattice to a depth of a few tenths of microns. As discussed, considerable effort over the last 10 years has been expended on furnace annealing methods. More recently, pulsed electron beam annealing has been under development at Spire for replacement of furnace processing. In the pulse anneal process, an intense electron beam is directed onto the surface of an implanted wafer which causes a momentary temperature transient at the wafer surface. The temperature excursion is believed to be high enough to melt previously implanted, amorphous layers to a depth of approximately 0.2 to 0.3 microns.
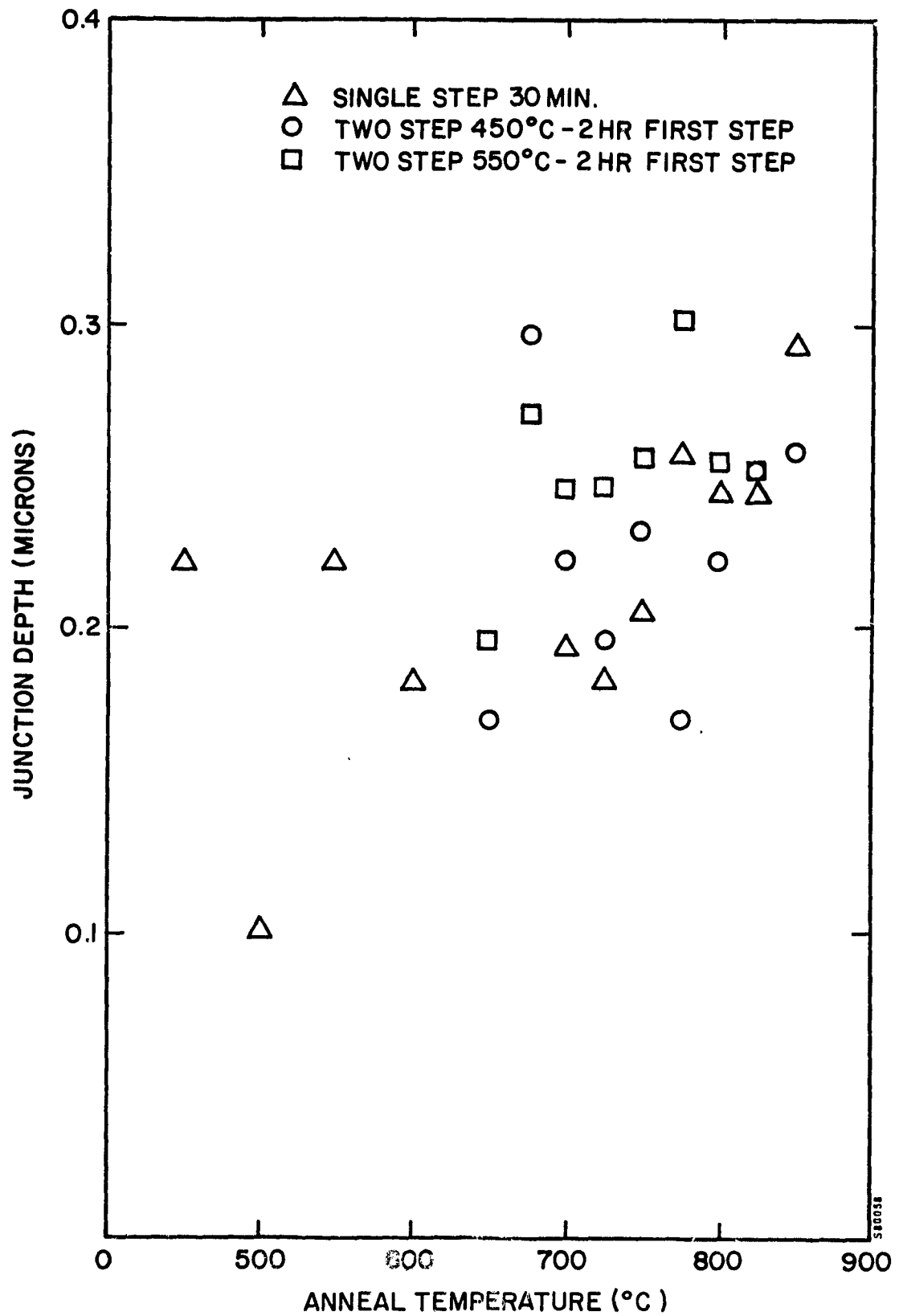
FIGURE 2-22. ISOCHRONAL ANNEALING OF 10-ohm-cm FZ SILICON
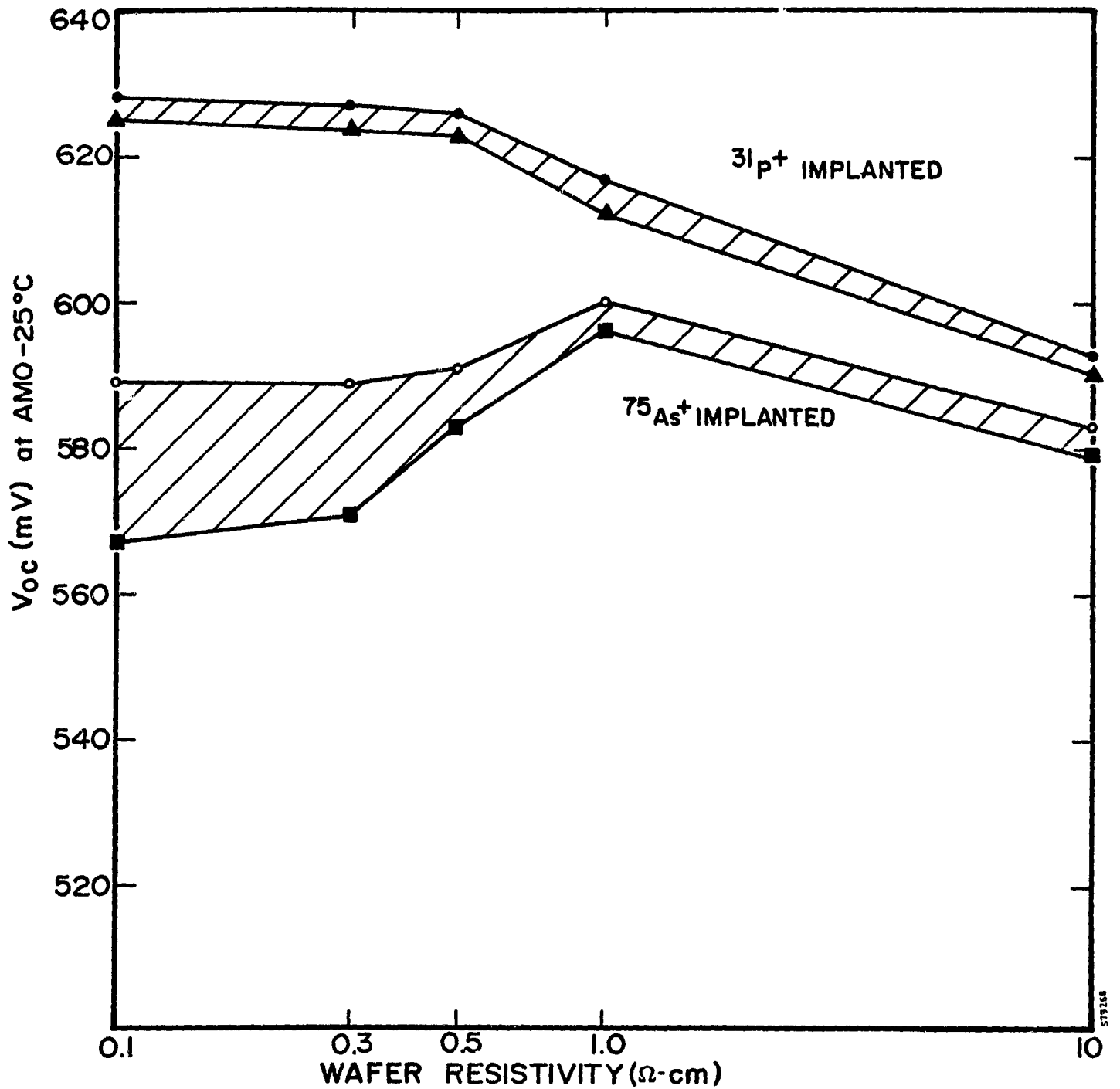
FIGURE 2-23. SUMMARY OF THREE-STEP FURNACE ANNEAL TEST MATRIX
FOR ARSENIC- AND PHOSPHORUS-IMPLANTED JUNCTIONS

A physical model which describes the mechanism of pulse annealing was developed under contract to JPL[8]. The model predicts the temperature transients and temperature profile histories for high-dose implanted layers on single crystal substrates. The pulse anneal mechanism is believed to be similar to liquid phase epitaxy where only the surface region is in the liquid phase. During the cool-down cycle following pulse deposition, the liquid to solid phase transition proceeds from the single crystal substrate with essentially perfect crystal structure.

Material analysis by TEM and helium ion backscattering-channeling has shown that these liquid-phase epitaxial regrown layers have backscattering characteristics similar to virgin, unimplanted silicon. TEM analysis showed dislocation-free implanted layers when pulsed electron beam annealing was used while equivalent implants when furnace annealed showed dislocation loops typical of furnace processing.

Pulse annealing was also found to produce better electrical activation of the implanted phosphorus ions as well. One deficiency of the pulse anneal process was identified to be residual point defects within the junction and depletion region probably a result of rapid thermal quenching following pulse deposition. These point defects were found to anneal within the $400^{\circ}C$ to $500^{\circ}C$ range and are consequently removed during contact sintering processing near the final steps of device fabrication.

Prior to this contract, pulsed electron beam annealing parameters had been established only for 10-ohm-cm silicon material. An important phase of this effort was to investigate the advantages of pulsed electron beam annealed junctions in low-resistivity material. Implanted and pulse-annealed junctions are characterized by dislocation-free crystal structure which should be important in achieving the maximum possible open-circuit voltage of highly doped semiconductors. During pulse processing the base region is never brought to high temperatures, precluding lifetime degradation by thermally induced defects.

The liquid-phase, epitaxially regrown junction is characterized by a flat dopant profile because of the extremely rapid diffusion rates in the liquid state. For example implant parameters of

1. 1×10^{15} $^{31}P^+$ cm^{-2}, 10 keV, 10° incidence
2. 1×10^{15} $^{75}As^+$ cm^{-2}, 25 keV, 10° incidence

result in peak dopant concentrations of 1×10^{20} atoms-cm^{-3} with junction depths of approximately 0.3 micron. These implant parameters were included in a pulsed electron beam anneal test matrix to determine open-circuit voltage of pulse-annealed, defect-free junctions in a range of silicon materials. Following implantation, the wafers were annealed with the following electron beam parameters:

1. pulse duration: 0.1 microsecond
2. mean electron energy: 12 keV
3. peak electron energy: 30 keV
4. fluence: 0.3 cal/cm^2

AM0-25°C open-circuit voltages were measured for pulse-annealed and combined pulse- and furnace-annealed junctions. The results are shown in Figures 2-24 for phosphorus implants and in Figures 2-25 for arsenic implants. In general, a 70-mV increase was measured following low-temperature, post-pulse annealing. No temperature dependence was determined, but these temperatures are typical of requirements for point-defect annealing. Later experiments revealed that 250°C for a period of 15 seconds was sufficient to increase open-circuit voltage to furnace-annealed values. However, none of the pulse-annealed junctions measured higher than 600 mV. It is believed that this voltage limitation is due to the characteristically flat dopant profile of liquid-phase epitaxial pulse annealing. This effect is discussed further and included in a general model described in Section 2.1.2.

2.2.4 Back Surface Field Assessment

A p$^+$ BSF layer can be formed by implanting ^{11}B$^+$, ^{27}Al$^+$, or other p-type dopants into the back of an n$^+$ on p cell, if the proper annealing conditions are used. This layer has been formed in the past by alloying evaporated, or thick-film-paste, aluminum into the back of the cell. Ion implantation, which assures dopant purity, can give improved results. Under this contract, p$^+$ layers have been obtained by boron-ion implantation. Other ions such as ^{27}Al$^+$ or ^{70}Ga$^+$ can be used, but the small ion beam currents obtainable with existing ion implanters make these impractical choices.
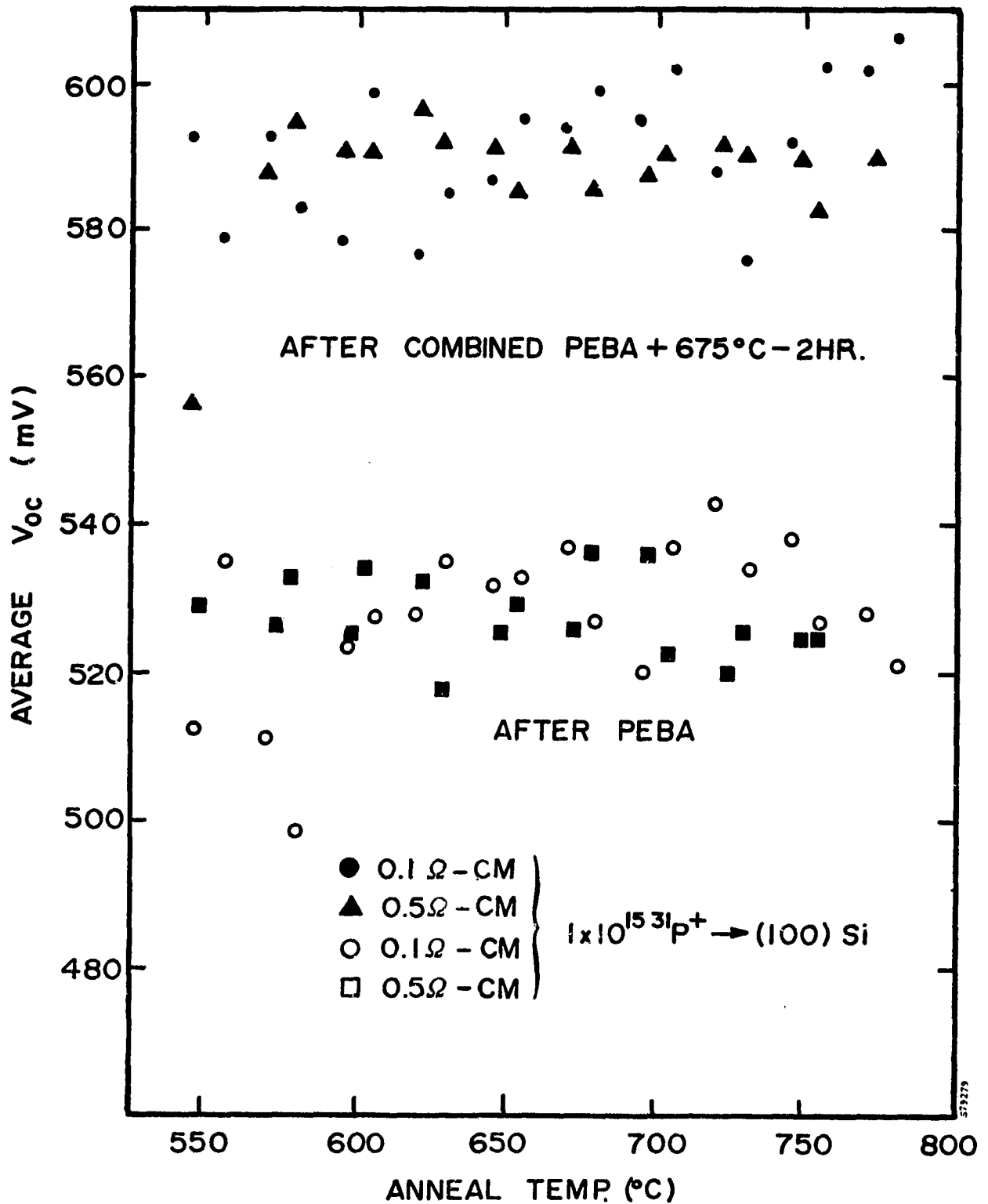
FIGURE 2-24.   MEASURED AM0-25°C OPEN-CIRCUIT VOLTAGE FOR
PHOSPHORUS-IMPLANTED/PULSE-ANNEALED JUNCTIONS
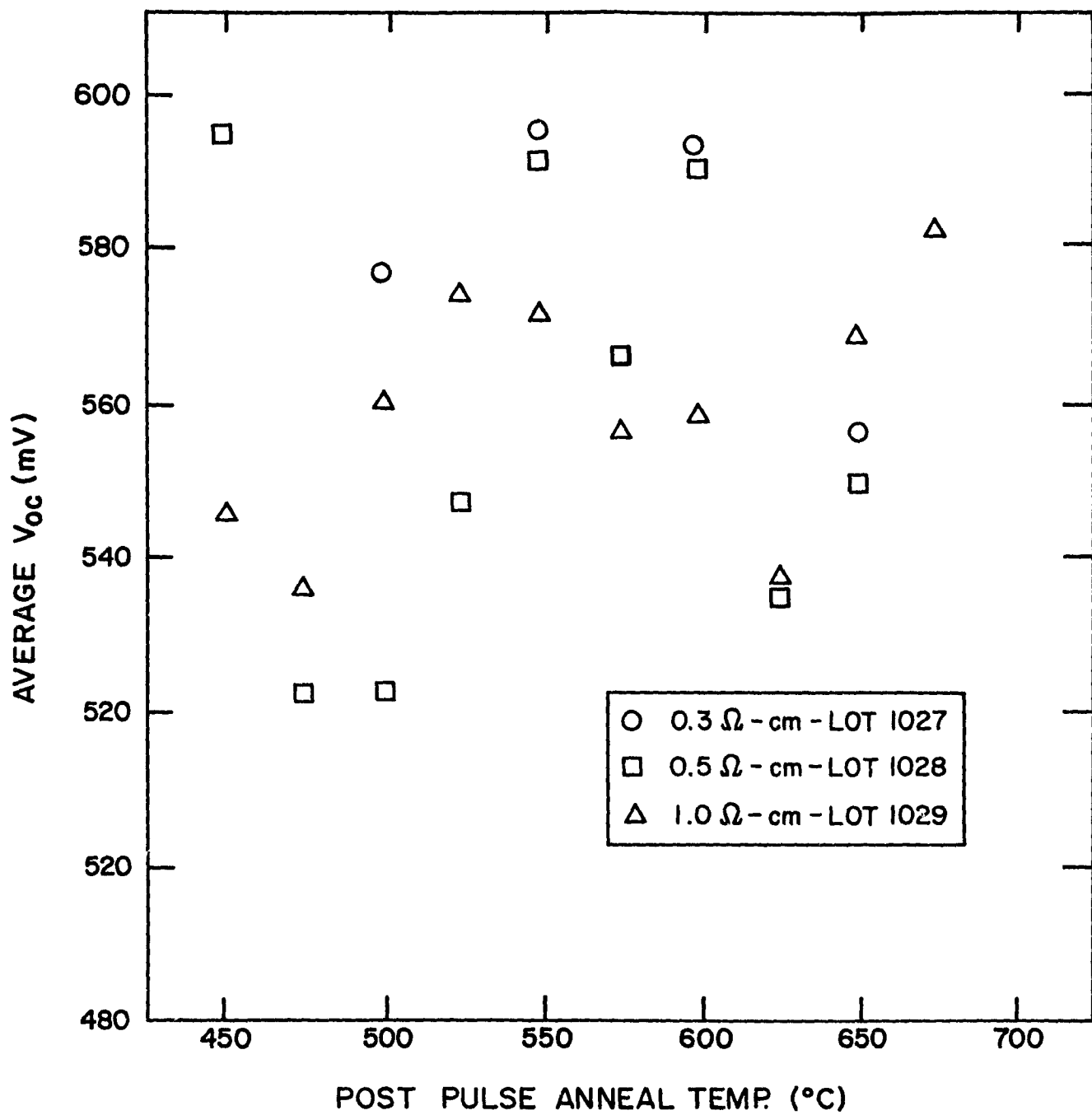
FIGURE 2-25. MEASURED AM0-25°C OPEN-CIRCUIT VOLTAGE FOR
ARSENIC-IMPLANTED/PULSE-ANNEALED JUNCTIONS

2-35

Several investigations of implanted-boron BSF's were conducted. The first was an isochronal, thermal-anneal matrix using 0.3-ohm-cm silicon. These wafers were prepared with 2×10^{15} $^{31}P^+$ cm^{-2}, 10-keV implanted junctions and 5×10^{15} $^{11}B^+$ cm^{-2}, 25-keV implanted back surfaces, then given a three-step thermal anneal as follows:

    (i) 550°C for 2 hours

    (ii) 800°C to 900°C in 25°C increments for 30 minutes

    (iii) 550°C for 2 hours

As shown in Figure 2-26, optimum BSF effect and simultaneous phosphorus-implant anneal occurs within the temperature range of 800°C to 875°C. The exact temperature within this range was determined to be noncritical.

Another comparison assessed the effect of boron concentration on implanted BSF's, and for reference, the control slices had an aluminum-alloyed p^+. All junctions were implanted with 2×10^{15} $^{31}P^+$ cm^{-2} or 1×10^{16} $^{11}B^+$ cm^{-2} at 25 keV, while the control cells had aluminum evaporated and alloyed onto the backs. The aluminum was alloyed at 580°C for 15 minutes. These implants were annealed in three steps: 550°C for 2 hours, 850°C for 15 minutes, and 550°C for 2 hours. The results are shown in Figure 2-27. This experiment was conducted to determine exactly the effectiveness of the BSF and to measure the dependence of the BSF on the $^{11}B^+$ implant dose. The aluminum-alloyed p^+ layer used is one which serves only to provide ohmic contact to the silicon; it does not increase V_{oc} by introduction of a high-low junction. The absence of BSF effect for the aluminum-alloyed p^+ layer is demonstrated in the 10-ohm-cm wafers. The boron-implanted p^+ layer shows a BSF increase in V_{oc} up to 595 mV. The usefulness of the p^+ layer only extends down to 1.0-ohm-cm resistivities, beyond which the BSF provides only an ohmic contact.

Because highest V_{oc} values for 0.1-ohm-cm material were achieved with alloyed aluminum layers as a non-BSF p^+ layer, the effect of alloying temperature was also evaluated. The results, as shown in Figure 2-28, indicate 620°C to be the optimum alloy temperature.
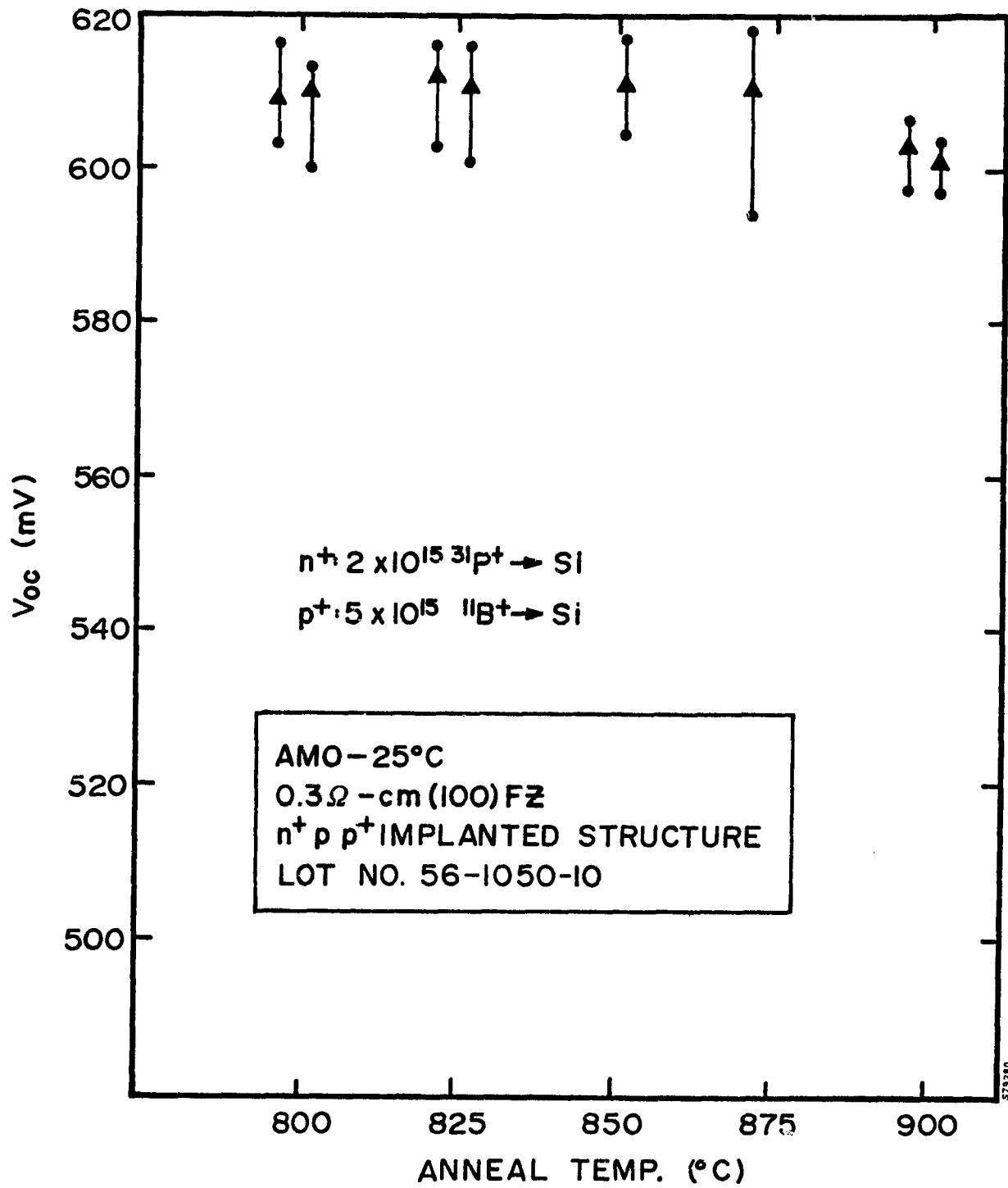
FIGURE 2-26. AM0 PERFORMANCE FOR ISOCHRONAL ANNEALS
OF ION-IMPLANTED n^+pp^+ SOLAR CELLS
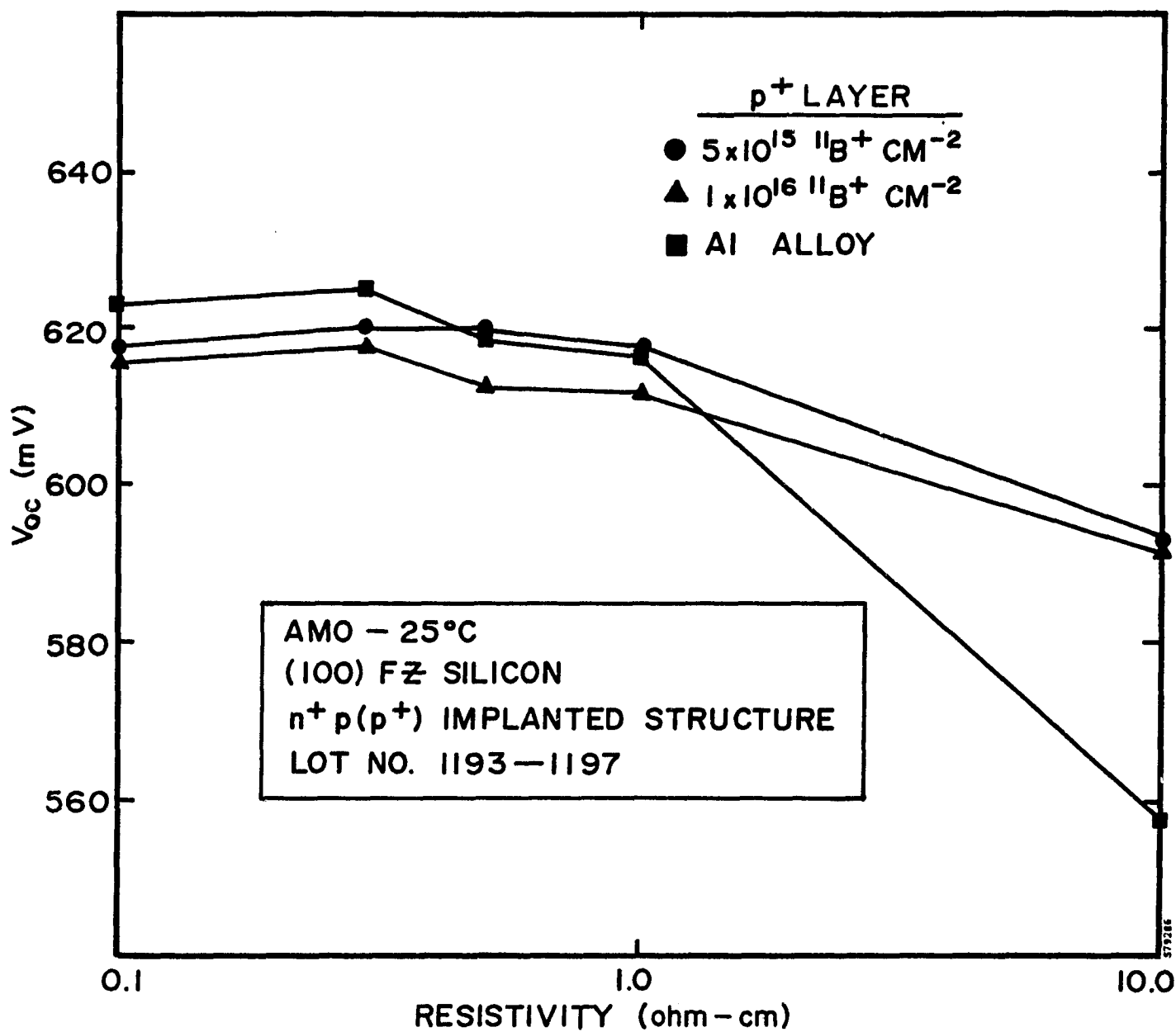
FIGURE 2-27.   AM0 PERFORMANCE OF IMPLANTED/FURNACE-ANNEALED
n⁺pp⁺ STRUCTURES IN 0.1- THROUGH 10.0-ohm-cm SILICON
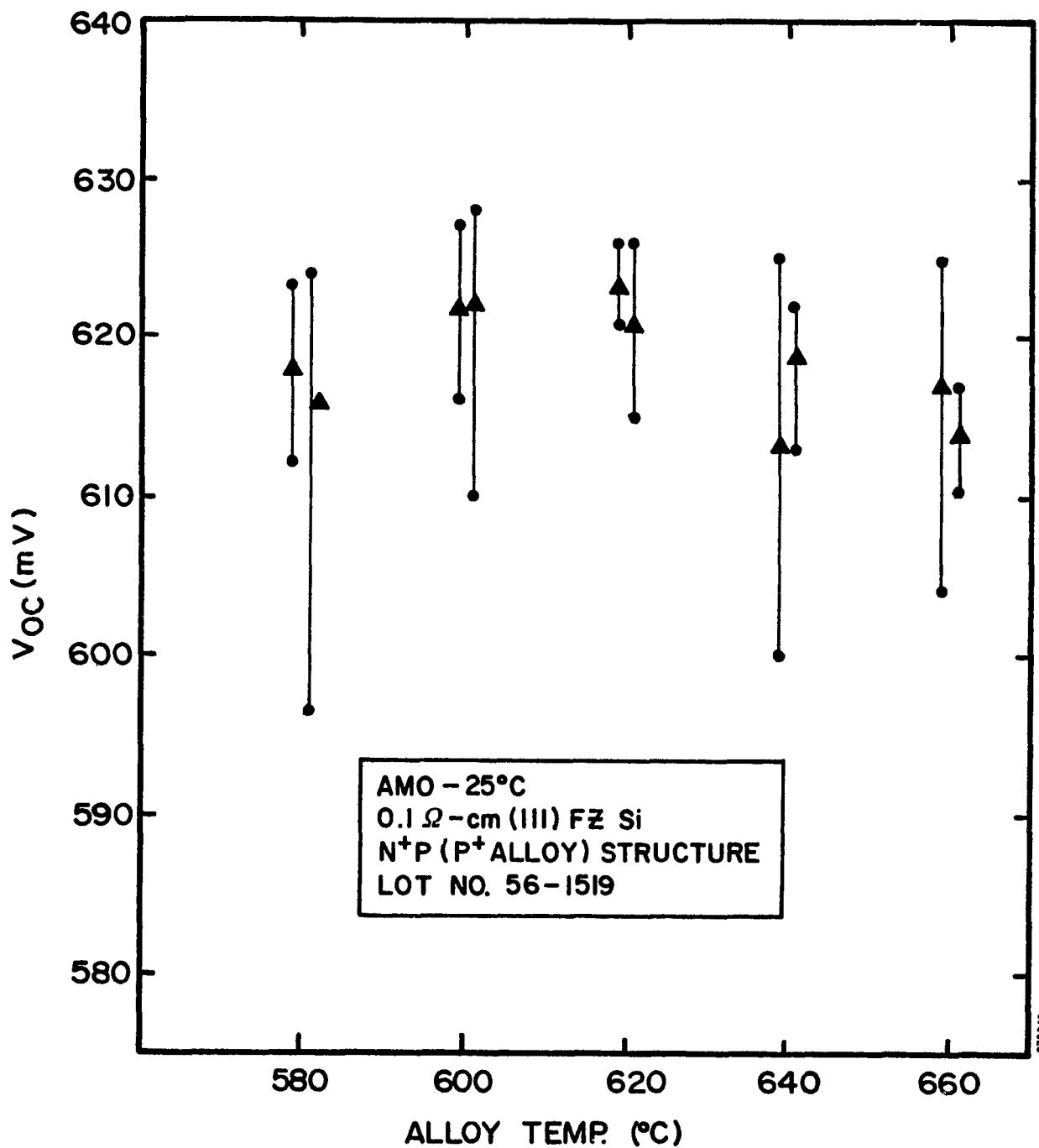
FIGURE 2-28. AVERAGE V_{OC} FOR FURNACE-ANNEALED AND IMPLANTED
JUNCTION SOLAR CELLS WITH AN ALUMINUM p^+ LAYER
AS A FUNCTION OF ALLOY TEMPERATURE

2-39

The possibilities of pulsed electron beam annealing of a boron-implanted BSF were also investigated. Wafers with 5×10^{15} $^{11}B^+$ cm^{-2} implanted into the back surface were PEBA annealed. Following PEBA anneal of the back surface, the junctions were implanted with 2×10^{15} P^{31+} cm^{-2} and also PEBA annealed. V_{oc} point-probe measurements were made under AM0-25°C conditions. Results, as shown in Figure 2-29, do not demonstrate an effective BSF effect on 10-ohm-cm silicon when $^{11}B^+$ implants are pulse annealed. An ohmic contact was achieved and is the only necessary p^+ function for cell performance with resistivities below 1.0 ohm-cm. Further electron beam parameter development is necessary to anneal $^{11}B^+$ implants adequately as deep as 25 keV.

2.2.5   Computer-Generated Implant Profiles

One of the more important tasks under this contract has been the evaluation of multiple junction profiles and dopant concentrations. Section 2.2.5 describes the results of a study conducted to examine these effects.

During the first quarter, a computer program called IMPLANT was written. The code identifies a series of implant energies and doses to "best fit" any desired junction profile shape. It models both phosphorus and arsenic implants. Up to 10 individual implants can be simultaneously optimized to provide the fit.

The program is designed to minimize the root-mean-square (RMS) difference between the sum of the implanted profiles and the final desired profile. The lower this RMS difference becomes, the closer the actual implants are to the desired profile. Implant energy and fluence are independently varied cyclically to optimize this fit.

The basic data for single ion energy implants is modeled by the program as a Gaussian shape. Ion range and Gaussian standard deviations are computed from the equations given as a simple function of implant energy. Thus, neither channeling nor diffusion during anneal is accounted for by the program.

A subroutine first determines a single implant for an arbitrary profile to be fit, given an initial "guess" at the best value. Fitting is then done by first optimizing the energy, then optimizing the fluence for a best fit. Finally, the cycle is repeated until sufficient closeness is obtained. A program flow chart for the energy optimization is shown in Figure 2-30. Fluence optimization is done by essentially the same technique.
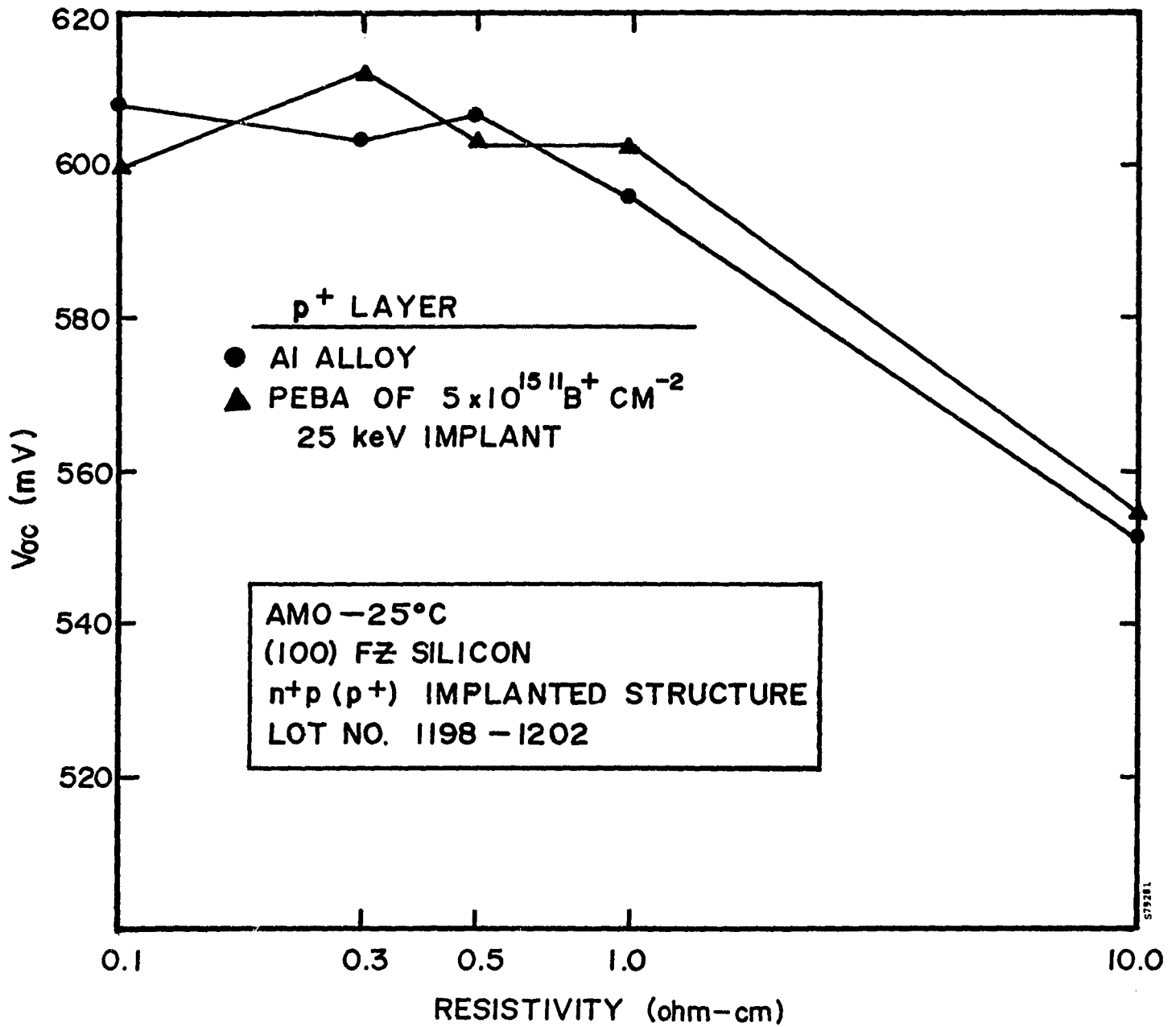
FIGURE 2-29. AVERAGE OPEN-CIRCUIT VOLTAGE FOR IMPLANTED/
PULSE-ANNEALED n^+pp^+ STRUCTURES
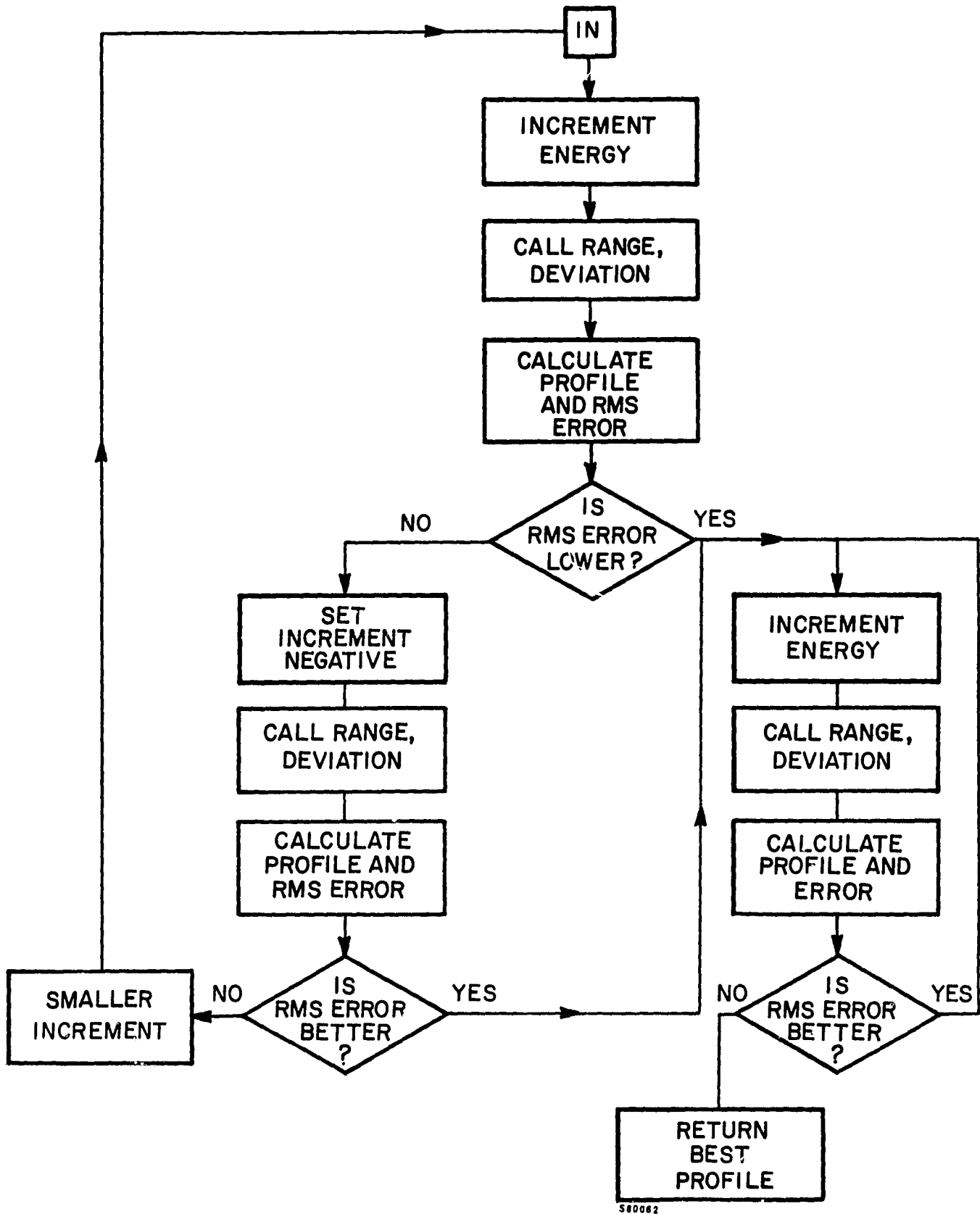
FIGURE 2-30. SUBROUTINE FOR ENERGY OPTIMIZATION WITHIN
IMPLANT PROGRAM

For practical considerations computations were limited to three sets of implant parameters. During the optimization routine two of the three implant parameter sets were made constant while the third set was optimized to the desired profile. This procedure was repeated for the remaining two implant parameter sets. The equations[13] for range and standard deviation are:

$^{75}As^+$ in Si:

$$R_p(E) = 8.96 \times 10^{-4} (E^{(0.92)})$$

$$dR_p(E) = 5.27 \times 10^{-4} (E^{0.83})$$

$^{31}P^+$ in Si:

$$R_p(E) = 1.3 \times 10^{-3} (E)$$

$$dR_p(E) = 0.15 \left[0.1 \, E^{1/2} - \ln(1 + 0.1 \, E^{1/2}) \right]$$

where

R_p = projected range in micrometers

dR_p = standard deviation

E = implant energy in kiloelectronvolts

The IMPLANT computer program was used to generate several sets of implant parameters. All the profiles calculated were for junction depths of 0.2 micron. Both arsenic- and phosphorus-implant parameters were determined for both exponential and linear profiles. Peak dopant concentrations used were $1 \times 10^{19} \, cm^{-3}$, $5 \times 10^{19} \, cm^{-3}$, and $2 \times 10^{20} \, cm^{-3}$. All profiles were limited to three implants, each giving a reasonably good approximation to the desired profile, especially since dopants will diffuse somewhat during annealing.

Figures 2-31 through 2-34 show the implant parameters required for phosphorus exponential and linear profiles and arsenic exponential and linear profiles. The parameters were calculated for the specific case of 10^{19}-cm^{-3} peak dopant concentration. Multiplying all fluences by five gave the parameters necessary for 5×10^{19}-cm^{-3} peak dopant concentration.

OPTIMIZED: RMS error after 11 iterations: 1.204766500E + 17

implant 1: Fluence = 1.1509375E + 13 Energy = 7.50227992938 keV
           Range = 0.010 micron   Deviation = 0.005
implant 2: Fluence = 2.965673828E + 13 Energy = 26.7874332041 keV
           Range = 0.035 micron   Deviation = 0.015
implant 3: Fluence = 5.105883789E + 13 Energy = 71.6739778805 keV
           Range = 0.093 micron   Deviation = 0.035
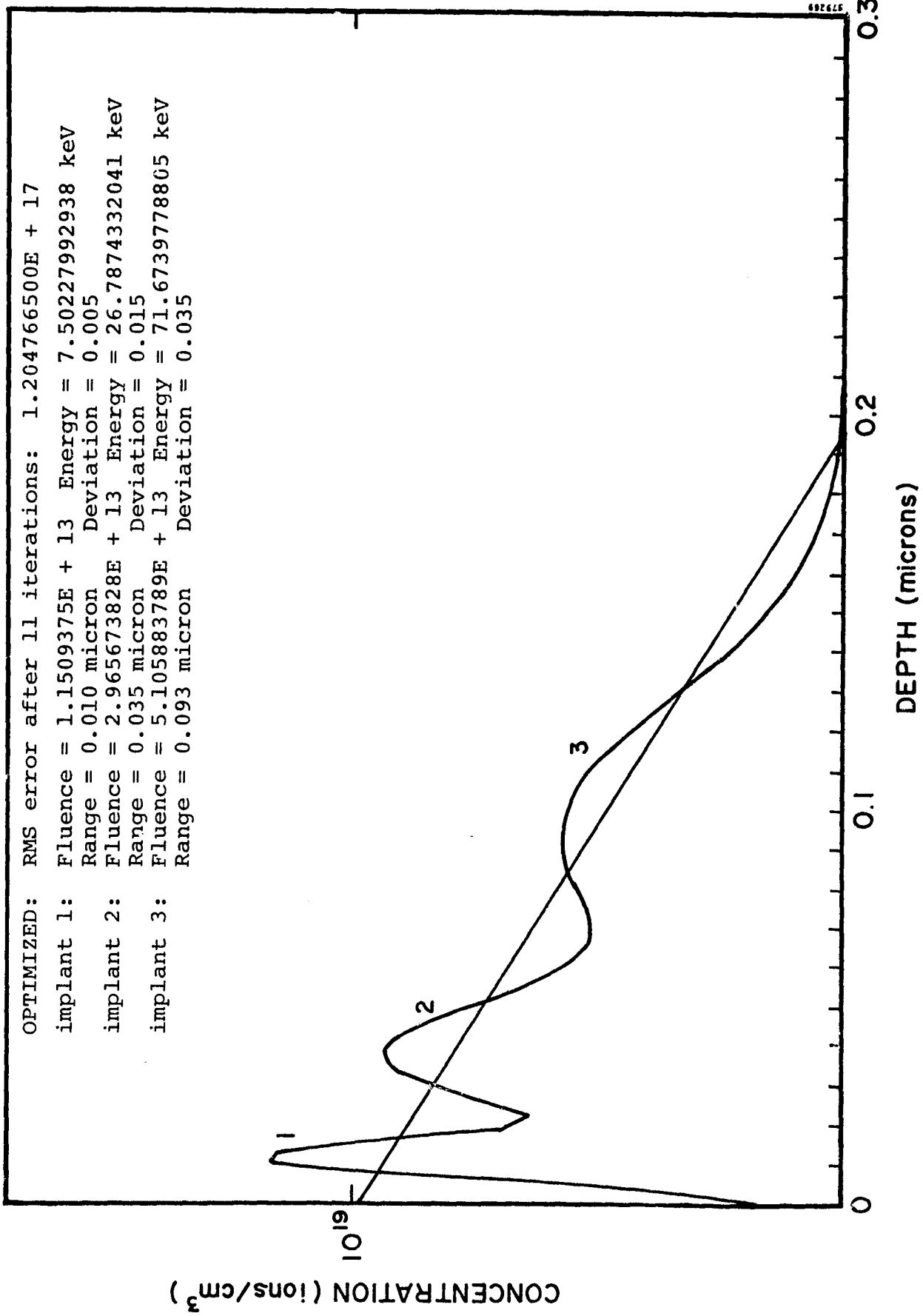
FIGURE 2-31. PREDICTED IMPLANTED PHOSPHORUS PROFILE FOR LINEAR GRADIENT AND 1×10^{19}-cm^{-3} MAXIMUM CONCENTRATION

OPTIMIZED: RMS error after 16 iterations: 9.81301728E + 16

implant 1: Fluence = 7.17692183E + 12 Energy = 5 keV
           Range = 0.006 micron Deviation = 0.003

implant 2: Fluence = 1.384104572E + 13 Energy = 15.7369404978 keV
           Range = 0.020 micron Deviation = 0.009

implant 3: Fluence = 1.738444171E + 13 Energy = 42.0475568286 keV
           Range = 0.055 micron Deviation = 0.022
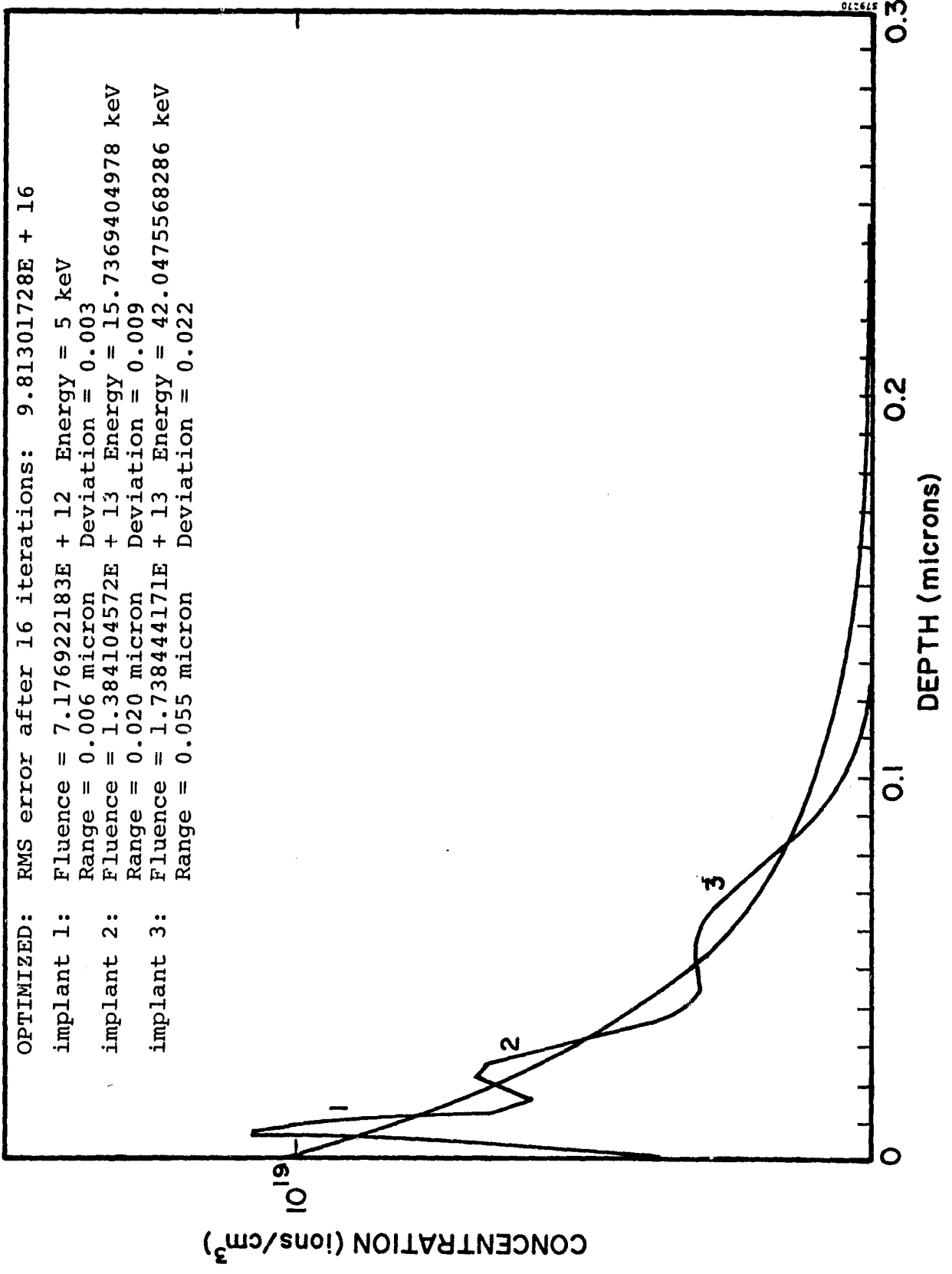
FIGURE 2-32. PREDICTED IMPLANTED PHOSPHORUS PROFILE FOR EXPONENTIAL GRADIENT AND 1×10^{19}-cm^{-3} MAXIMUM SURFACE CONCENTRATION

FIGURE 2-33. PREDICTED IMPLANTED ARSENIC PROFILE FOR LINEAR GRADIENT AND
1×10^{19}–cm^{-3} MAXIMUM SURFACE CONCENTRATION
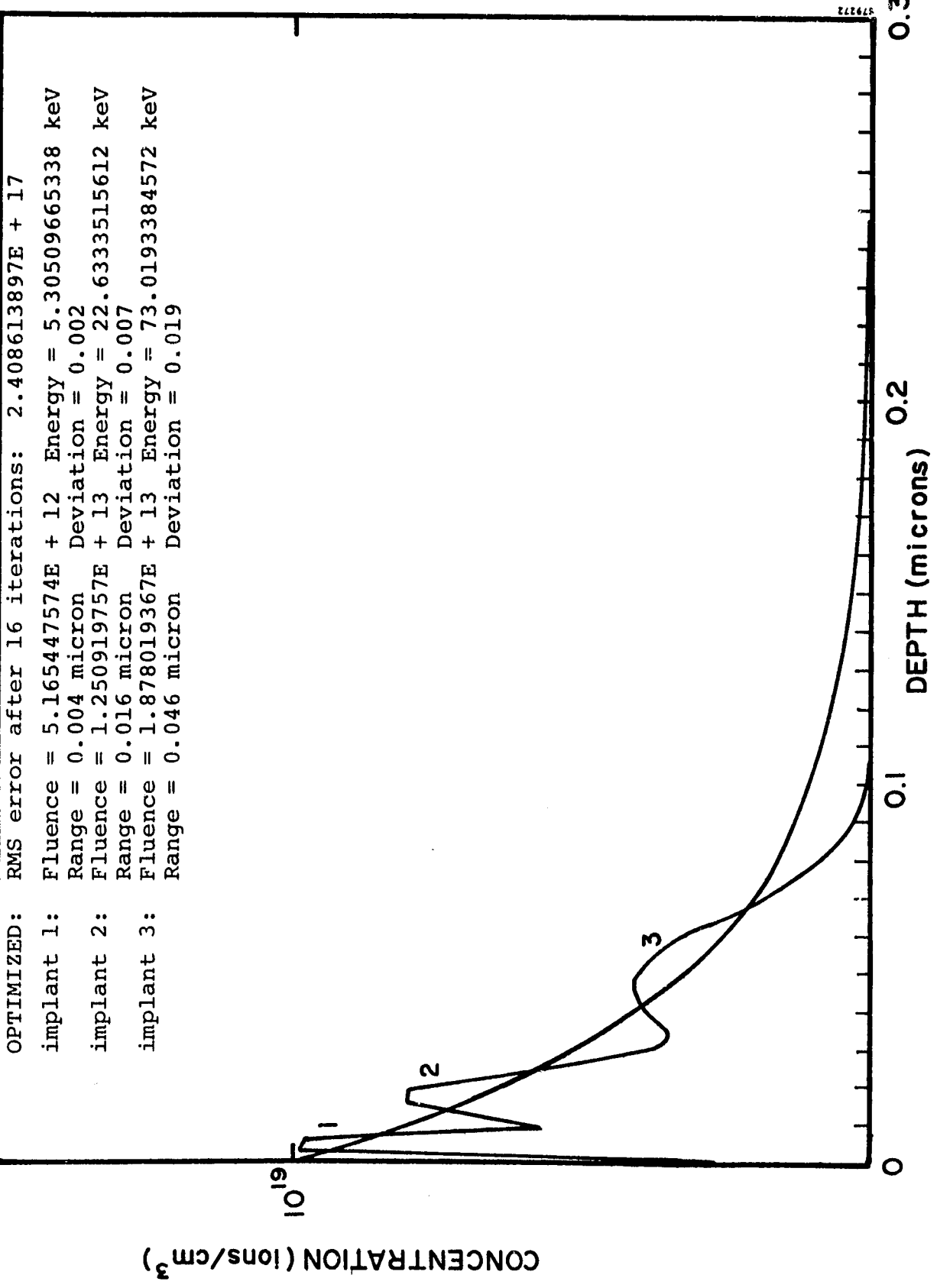
FIGURE 2-34. PREDICTED IMPLANTED ARSENIC PROFILE FOR EXPONENTIAL GRADIENT AND $1 \times 10^{19} \text{-cm}^{-3}$ MAXIMUM SURFACE CONCENTRATION

Combined phosphorus- and arsenic-implant parameters were also determined from the same profiles. Each set of ion-implant ion parameters was calculated separately to match the desired fraction of the total dose. For example, if a 1:1 phosphorus to arsenic exponential profile with a peak dopant concentration of 5×10^{19} cm^{-3} was required, the ^{31}P$^+$ and ^{75}As$^+$ doses were specified at half the implant dose which would normally give a 5×10^{19} cm^{-3} peak concentration.

2.2.6 Junction Profile Measurements

Actual implanted and annealed profiles were determined by the SIMS method of selected samples of both arsenic- and phosphorus-implanted junctions. Table 2-1 shows each of the junction types investigated and the selected junction profiles for SIMS measurements. Figures 2-35 through 2-38 show the SIMS measured profiles and include for reference the desired profiles generated by the IMPLANT program.

All the profiles calculated were for junction depths of 0.2 micron. Both arsenic- and phosphorus-implant parameters were determined for exponential and linear dopant profiles in the junction layer. Peak dopant concentrations were 1×10^{19} cm^{-3}, 5×10^{19} cm^{-3}, and 2×10^{20} cm^{-3}.

The resultant profiles were measured after either a 550°C – 3-hour anneal or the optimized thermal anneal cycle of 550°C – 3 hours, 850°C – 30 minutes, and 550°C – 3 hours. The single-step, low-temperature (550°C – 3-hour) anneal was used to activate the implanted ions electrically, so that repetitive anodic oxidation-layer stripping techniques could be used to compare profiles determined by SIMS and profiles determined by R$_{sheet}$ measurements. The high-temperature-anneal schedules were used so that the profiles representative of fully annealed devices could be compared with the as-implanted distribution. Additional implanted samples were prepared for pulsed electron beam annealing; one of the resultant profiles is shown in Figure 2-39.

Results from this SIMS analysis of the computer predicted implant profiles show that in all cases the actual dopant surface concentration was within a factor of two of the desired concentration entered as input data to the program. (Note that an exponential profile appears linear and a linear profile appears logarithmic when transformed on the semilog plots used for Figures 2-35 through 2-39.) The significance of achieving desired profiles which are non-Gaussian is major. By being able to control the profile near the metallurgical junction, the magnitude of the electric field can also be controlled.

TABLE 2-1. PROFILE SAMPLES FOR ANALYSIS OF COMPUTER GENERATED
IMPLANT PARAMETERS

Wafer No.	Junction Profile	Ion	Peak Concentration	$X_j(\mu m)$	Anneal Schedule	SIMS Samples
1217-1B	Linear	P^+	1×10^{19}	0.2	$550^{\circ}C/3$ hr	
1226-1B	Linear		5×10^{19}		$550^{\circ}C/3$ hr	x
1228-1B	Linear		2×10^{20}		$550^{\circ}C/3$ hr	x
1228-2B	Linear		2×10^{20}		550/850/550	x
1224-1B	Exp.	P^+	1×10^{19}	0.2	550/3 hr	−
1225-1B	Exp.		5×10^{19}		550/3 hr	−
1288-1B	Exp.		2×10^{20}		550/3 hr	−
1288-2B	Exp.		2×10^{20}		550/850/550	−
1231-1B	Linear	As^+	1×10^{19}	0.2	$550^{\circ}C/3$ hr	−
1232-1B	Linear		5×10^{19}		$550^{\circ}C/3$ hr	−
1233-1B	Linear		2×10^{20}		$550^{\circ}C/3$ hr	x
1233-2B	Linear		2×10^{20}		550/850/550	x
1227-1B	Exp.	As^+	1×10^{19}	0.2	$550^{\circ}C/3$ hr	−
1229-1B	Exp.		5×10^{19}		$550^{\circ}C/3$ hr	−
1230-1B	Exp.		2×10^{20}		$550^{\circ}C/3$ hr	x
1230-2B	Exp.		2×10^{20}		550/850/550	x
1268-1B	Step	P^+	1×10^{20}	0.2	550/3 hr	x
1268-2B	Step		1×10^{20}		550/850/550	x

FIGURE 2-35.   PREDICTED AND ACTUAL IMPLANTED PHOSPHORUS PROFILES FOR $2 \times 10^{20}-cm^{-3}$ SURFACE CONCENTRATION AND STEP FUNCTION GRADIENT
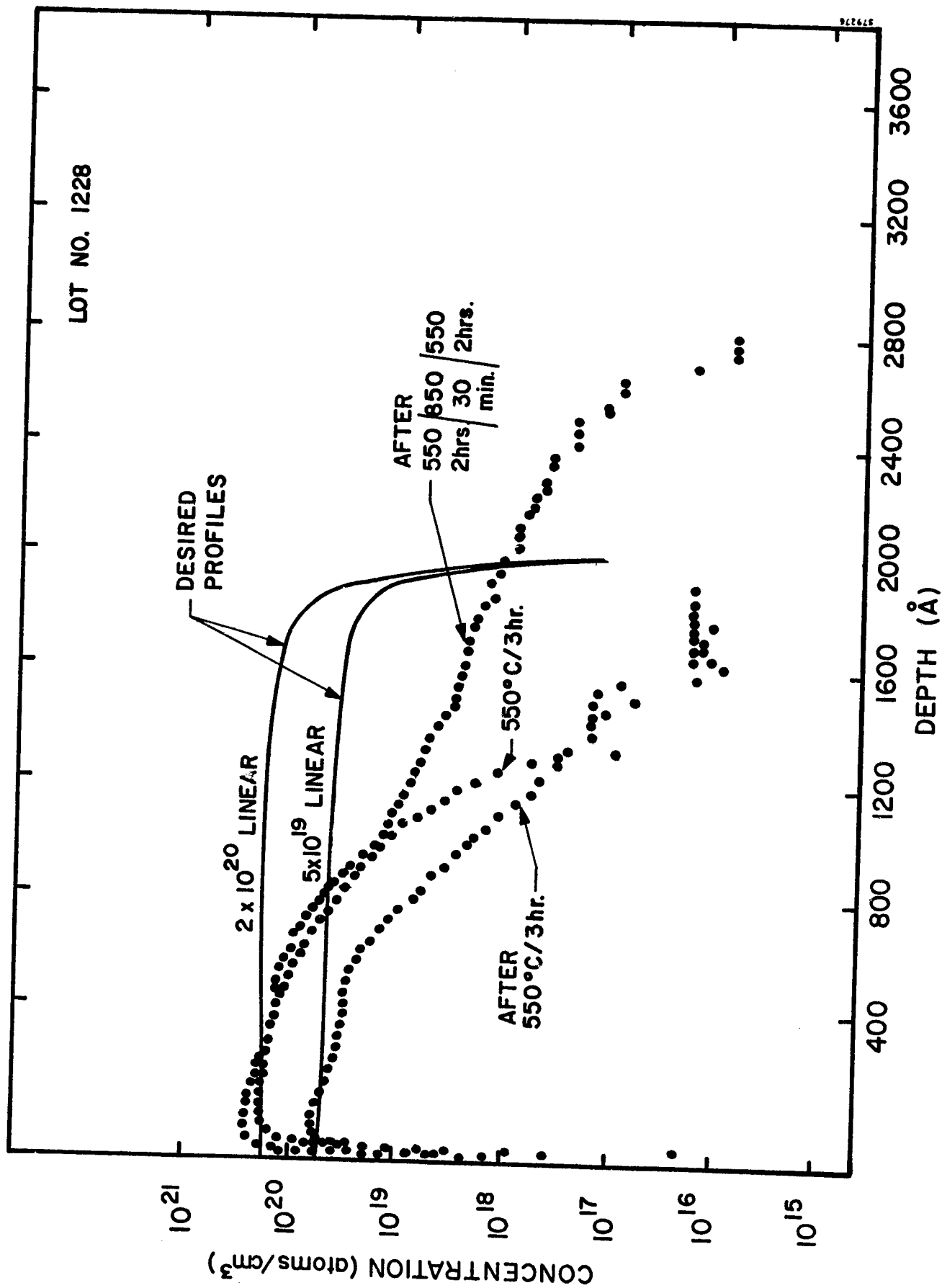
FIGURE 2-36. PREDICTED AND ACTUAL IMPLANTED PHOSPHORUS PROFILES FOR TWO
SURFACE CONCENTRATIONS AND LINEAR GRADIENTS
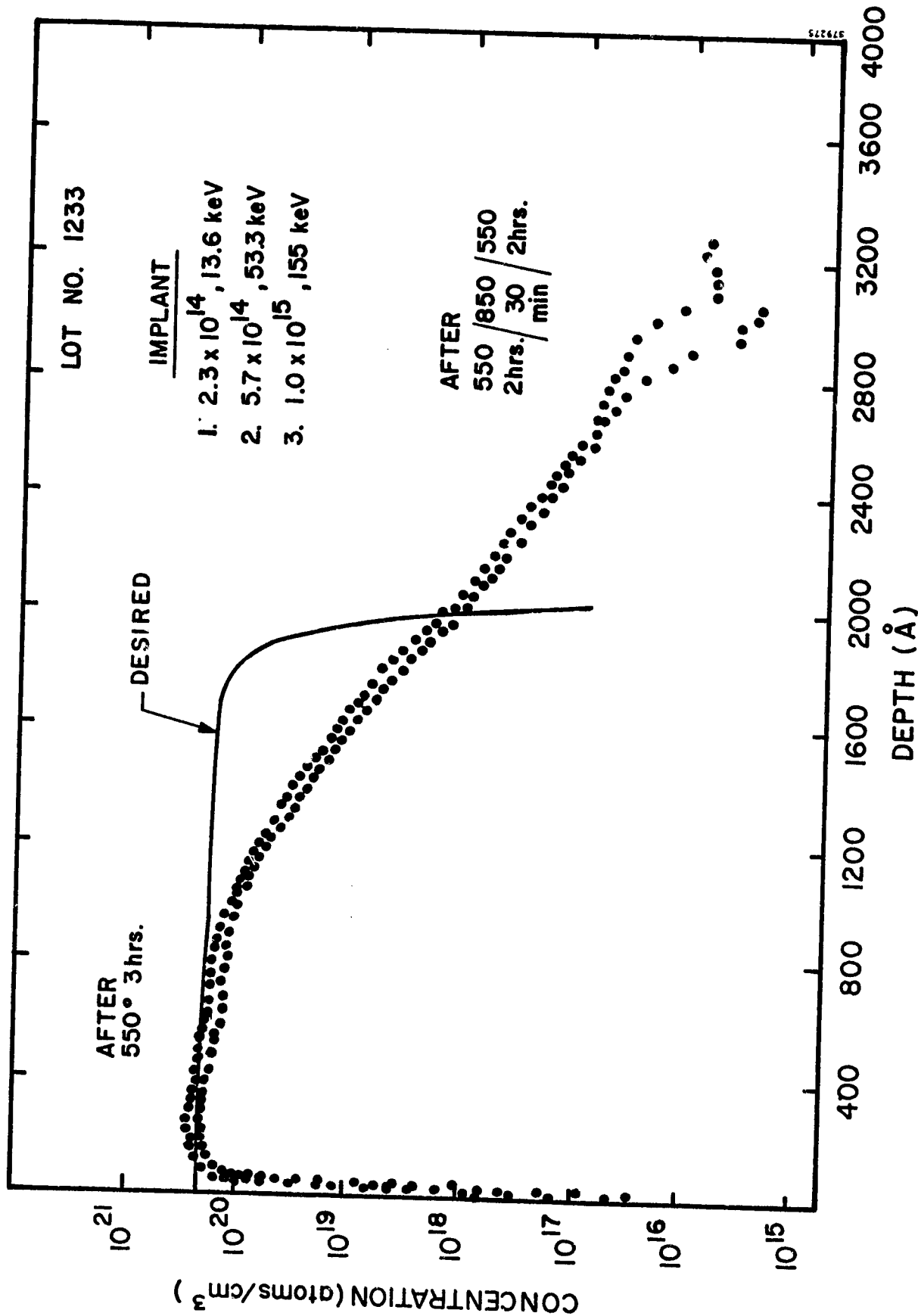
FIGURE 2-37. PREDICTED AND ACTUAL IMPLANTED ARSENIC PROFILES FOR $2 \times 10^{20}-cm^{-3}$ SURFACE CONCENTRATION AND LINEAR GRADIENT
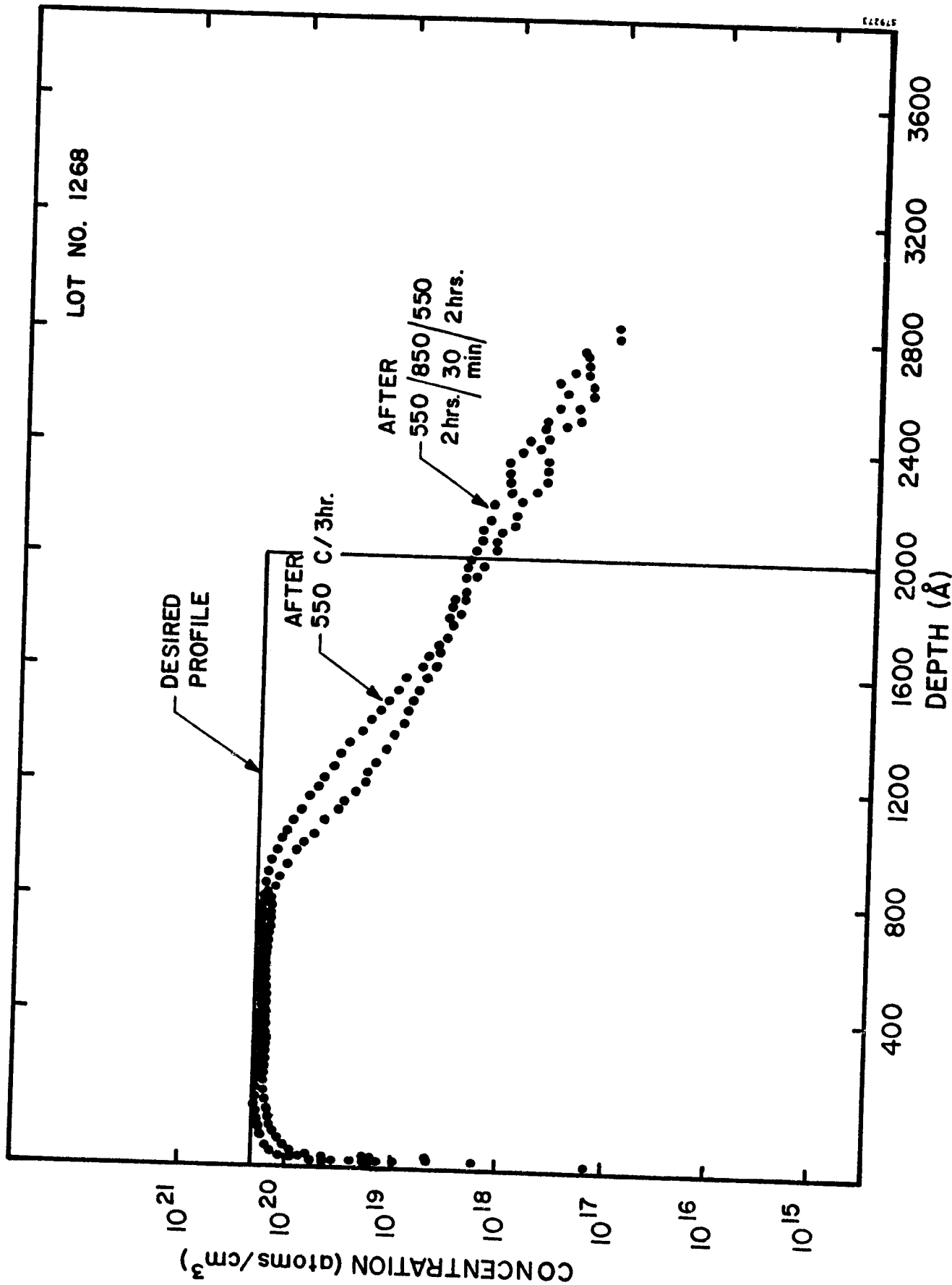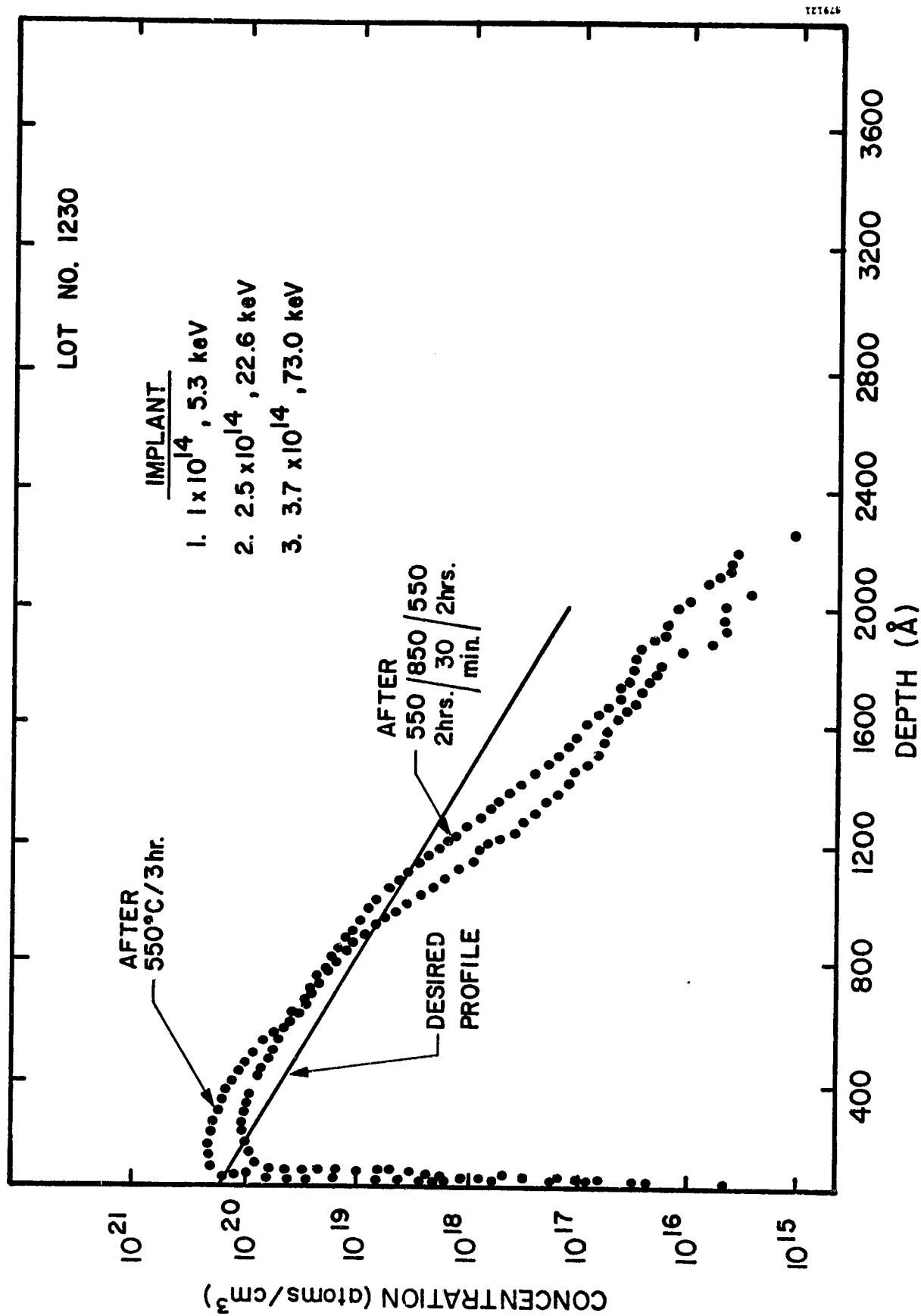
FIGURE 2-38. PREDICTED AND ACTUAL IMPLANTED ARSENIC PROFILES FOR $2 \times 10^{20} - cm^{-3}$ SURFACE CONCENTRATION AND EXPONENTIAL GRADIENT
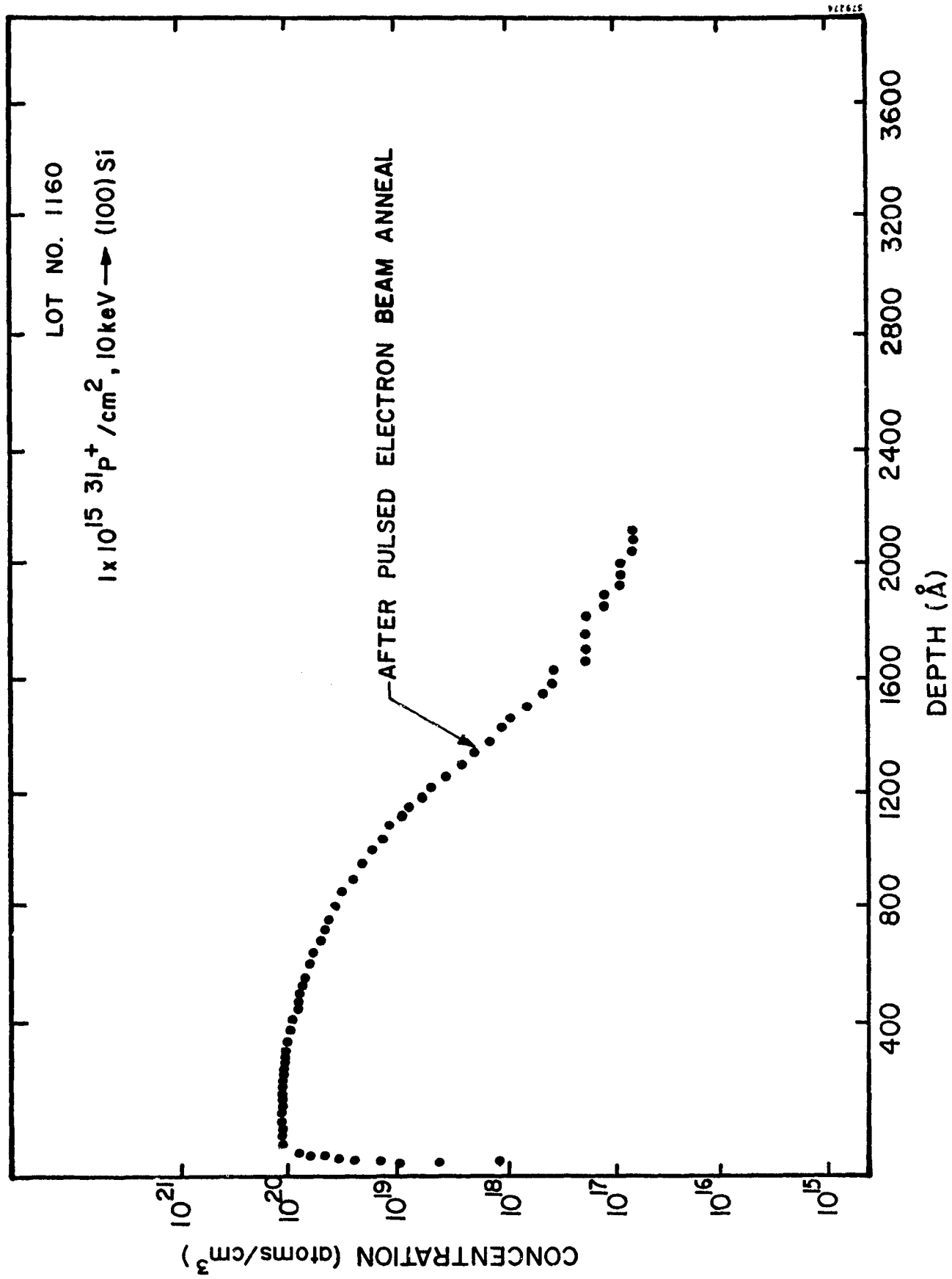
FIGURE 2-39. ACTUAL IMPLANTED PHOSPHORUS PROFILE FOLLOWING PULSED ELECTRON BEAM ANNEAL OF SINGLE IMPLANT

2.2.7 Tailored Emitter Process Evaluation

Fifteen junction types, as listed in Table 2-2, were implanted in 600 wafers (120 each of five resistivities). The implants included phosphorus, arsenic, and combined phosphorus-arsenic dopants. Half the wafers were given a standard furnace anneal, and half were pulsed electron beam annealed (PEBA), as shown in the processing schematic of Figure 2-40. Open-circuit voltages were measured by point probing, and a four-point probe was used for V/I sheet resistivity measurements. Actual implanted dopant profiles as measured by secondary ion mass spectroscopy (SIMS) are shown in Section 2.2.5.

None of the junctions in these experiments demonstrated open-circuit voltages higher than 600 mV. The highest voltages for furnace-annealed junctions averaged 590 mV, for phosphorus exponential profiles in 0.3- and 0.5-ohm-cm silicon. In almost all cases, the highest voltages were achieved with the highest doping levels, i.e., peak concentration of 2×10^{20} atoms/cm^3. For arsenic implants this trend is less noticeable, and the open-circuit voltages did not always increase with doping level. The highest voltages for PEBA-annealed junctions averaged 590 mV for linear profile phosphorus doping in 0.3-ohm-cm silicon.

2.2.8 Furnace Annealing/Oxidation Process Development

The effects of dopant concentration for ion-implanted junctions were investigated with a wide range of dopant concentrations and state-of-the-art annealing techniques, including furnace and pulsed electron beam annealing. Open-circuit voltage for all test devices did not exceed 0.60V. Further effort was then placed on optimizing furnace annealing techniques using the relatively high-dose phosphorus implants which had always given the best results. The important distinction for the newer furnance annealing studies was the incorporation of simultaneous oxidation of the silicon surfaces during furnace annealing of the ion implantation damage. A process was designed to anneal the implant damage at low temperature, then thermally grow an SiO$_2$ layer to reduce the number of dangling bonds and decrease the surface recombination velocity (SRV), which appears to be as important as bandgap narrowing in limiting the open-circuit voltage of nonoxide cells at 0.60V levels.

Initial test devices were prepared by implantation of 2.5×10^{15} ^{31}P$^+$ cm^{-2} at 5 keV and 10-degree angle of incidence into 0.1-ohm-cm float-zone silicon. The wafers were then annealed by a three-step process in an oxygen ambient, and oxide windows were etched by standard photoresist techniques. Measurements were performed under

TABLE 2-2. DESIRED JUNCTION CHARACTERISTICS AND COMPUTER GENERATED IMPLANT PARAMETERS

Ion(s)	Profile Shape	Surface Concentration (cm^{-3})	Junction Depth (μm)	Implant 1		Implant 2		Implant 3	
				E (keV)	Dose (cm^{-2})	E (keV)	Dose (cm^{-2})	E (keV)	Dose (cm^{-2})
P^{31+}	Exponential	10^{19}	0.2	5.00	7.18×10^{12}	15.74	1.38×10^{13}	42.05	1.74×10^{13}
P^{31+}	Exponential	5×10^{19}	0.2	5.00	3.59×10^{13}	15.74	6.90×10^{13}	42.05	8.70×10^{13}
P^{31+}	Exponential	2×10^{20}	0.2	5.00	1.44×10^{14}	15.74	2.76×10^{14}	42.05	3.48×10^{14}
P^{31+}	Linear	10^{19}	0.2	7.50	1.15×10^{13}	26.79	2.97×10^{13}	71.67	5.11×10^{13}
P^{31+}	Linear	5×10^{19}	0.2	7.50	5.75×10^{13}	26.79	1.49×10^{14}	71.67	2.56×10^{14}
P^{31+}	Linear	2×10^{20}	0.2	7.50	2.30×10^{14}	26.79	5.94×10^{14}	71.67	1.02×10^{15}
As^{75+}	Exponential	10^{19}	0.2	5.31	5.17×10^{12}	22.63	1.25×10^{13}	73.02	1.87×10^{13}
As^{75+}	Exponential	5×10^{19}	0.2	5.31	2.59×10^{13}	22.63	6.25×10^{13}	73.02	9.35×10^{13}
As^{75+}	Exponential	2×10^{20}	0.2	5.31	1.03×10^{14}	22.63	2.50×10^{14}	73.02	3.74×10^{14}
As^{75+}	Linear	10^{19}	0.2	13.60	1.14×10^{13}	53.28	2.85×10^{13}	154.65	5.14×10^{13}
As^{75+}	Linear	5×10^{19}	0.2	13.60	5.70×10^{13}	53.28	1.43×10^{14}	154.65	2.57×10^{14}
As^{75+}	Linear	2×10^{20}	0.2	13.60	2.28×10^{14}	53.28	5.70×10^{14}	154.65	1.03×10^{15}
P^{31+}/As^{75+} 1:1	Exponential	5×10^{19}	0.2	5.00	1.80×10^{13}	15.74	3.45×10^{13}	42.05	4.38×10^{13}
				5.31	1.30×10^{13}	22.63	3.12×10^{13}	73.02	4.68×10^{13}
P^{31+}/As^{75+} 3:1	Exponential	5×10^{19}	0.2	5.00	2.69×10^{13}	15.74	5.18×10^{13}	42.05	6.53×10^{13}
				5.31	6.48×10^{12}	22.63	1.56×10^{13}	73.02	2.34×10^{13}
P^{31+}/As^{75+} 1:3	Exponential	5×10^{19}	0.2	5.00	8.98×10^{12}	15.74	1.73×10^{13}	42.05	2.18×10^{13}
				5.31	1.94×10^{13}	22.63	4.69×10^{13}	73.02	7.01×10^{13}

```
-30  2" WAFERS  OF  EACH  RESISTIVITY

IMPLANT BACKS              EVAPORATE AND
WITH BORON                 ALLOY AI INTO
                           BACKS

SAW WAFERS                 SAW WAFERS
IN HALF                    IN HALF

60 SAMPLES OF              60 SAMPLES OF
EACH RESISTIVITY           EACH RESISTIVITY

                 IMPLANT
FOUR  WAFERS  OF  EACH  BACK  TYPE  AND  RESIS-
TIVITY  ARE  IMPLANTED  WITH  ONE  OF  THE  15
JUNCTION  TYPES.
379281

p⁺ IMPLANTED                        AI  ALLOYED
BACKS                                   BACKS

OPTIMIZED                  OPTIMIZED
THERMAL                    PEBA
ANNEAL                     ANNEAL

OXIDE
STRIP

              MEASUREMENTS
              Voc, V/I, SIMS
```
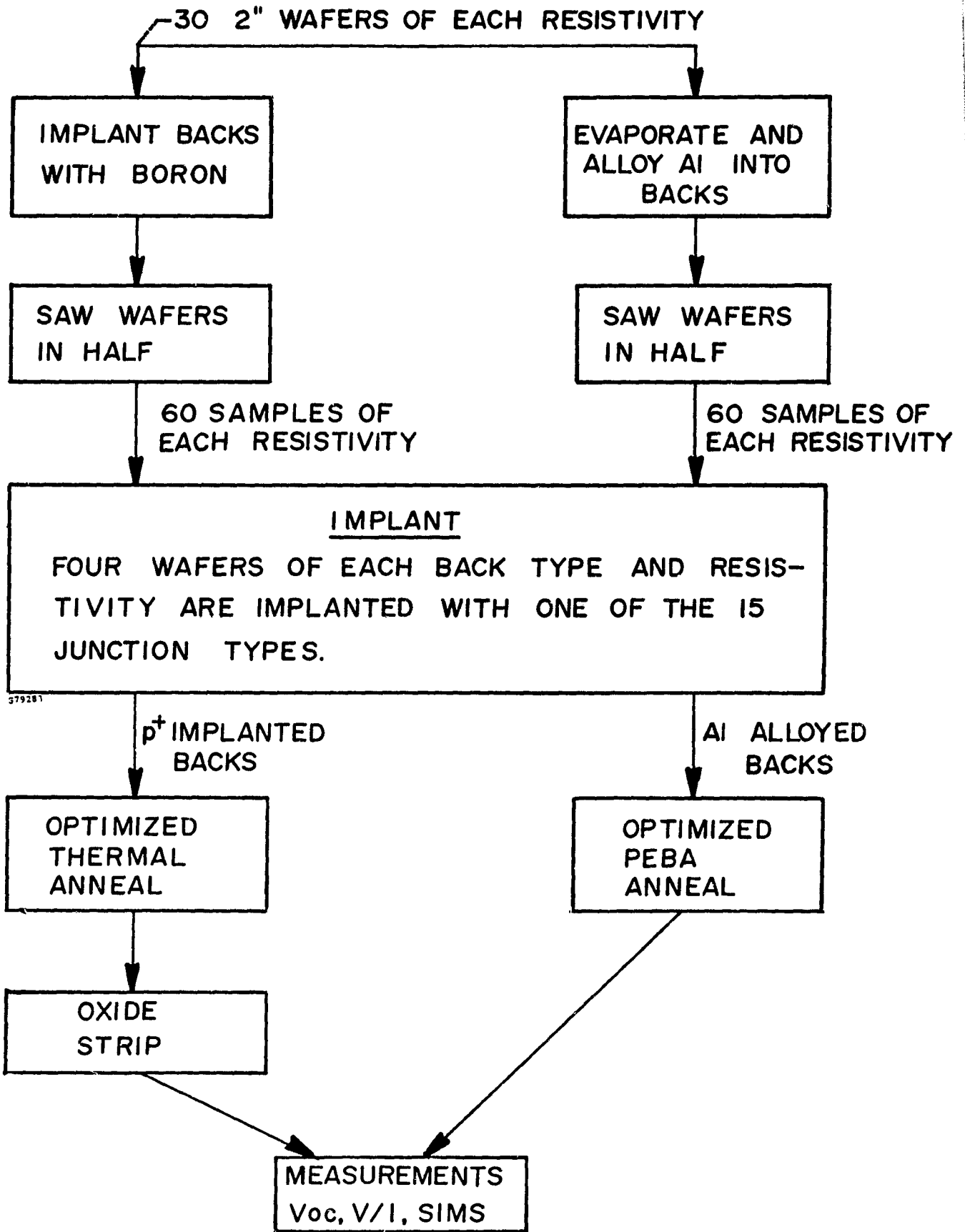
FIGURE 2-40. PROCESS SUMMARY FOR JUNCTION PROFILE STUDIES

AM0-25°C conditions by simply point probing each test device to determine open-circuit voltage. Preliminary results were then used to specify the process sequence for the 2 x 2-cm solar cells described in Section 2.3.

There are at least three physical mechanisms which control SRV on heavily doped semiconductors:

1. Doping level
2. Surface-state density
3. Radiation damage

The junction-layer doping level can influence solar cell performance by simple decrease in minority-carrier lifetime with increasing dopant concentration and by bandgap narrowing[4], as shown in Figure 2-41 and the following expression:

$$dE_g = 3.4 \times 10^{-8} (N_d - 2.65 \times 10^6) \text{ eV}$$

where

$$dE_g = \text{bandgap narrowing and}$$

$$N_d = \text{dopant concentration}$$

For typical junction layers, N_d is approximately 5×10^{20} phosphorus atoms-cm^{-3}, which leads to a 0.16-eV gap decrease. Without consideration of surface-state density (N_{st})[14] and radiation damage, open-circuit voltages of 684 mV are predicted for 0.1-ohm-cm silicon solar cells under AM0-25°C conditions using the bandgap narrowing model. However, both SRV and radiation damage (or lattice disorder from any source) are important factors in device performance.[15]

Calculations by others have shown the importance of reducing SRV in obtaining high open-circuit voltage[16], as shown in Figure 2-42. The techniques available include oxide growth and strong electric fields near the semiconductor surface to repel minority carriers and prevent recombination. The addition of strong electric fields to repel minority carriers has also been effective in obtaining low SRV values, as demonstrated by HLE cells.[17,18] This mechanism is similar to the BSF effect resulting from steep doping gradients and has been used previously to improve V_{oc} in high-resistivity silicon solar cells. Data from all the implant test matrices are consistent with this model. Each of the tests for bandgap narrowing performed to date has shown increasing V_{oc} with increasing dose level and phosphorus concentration.
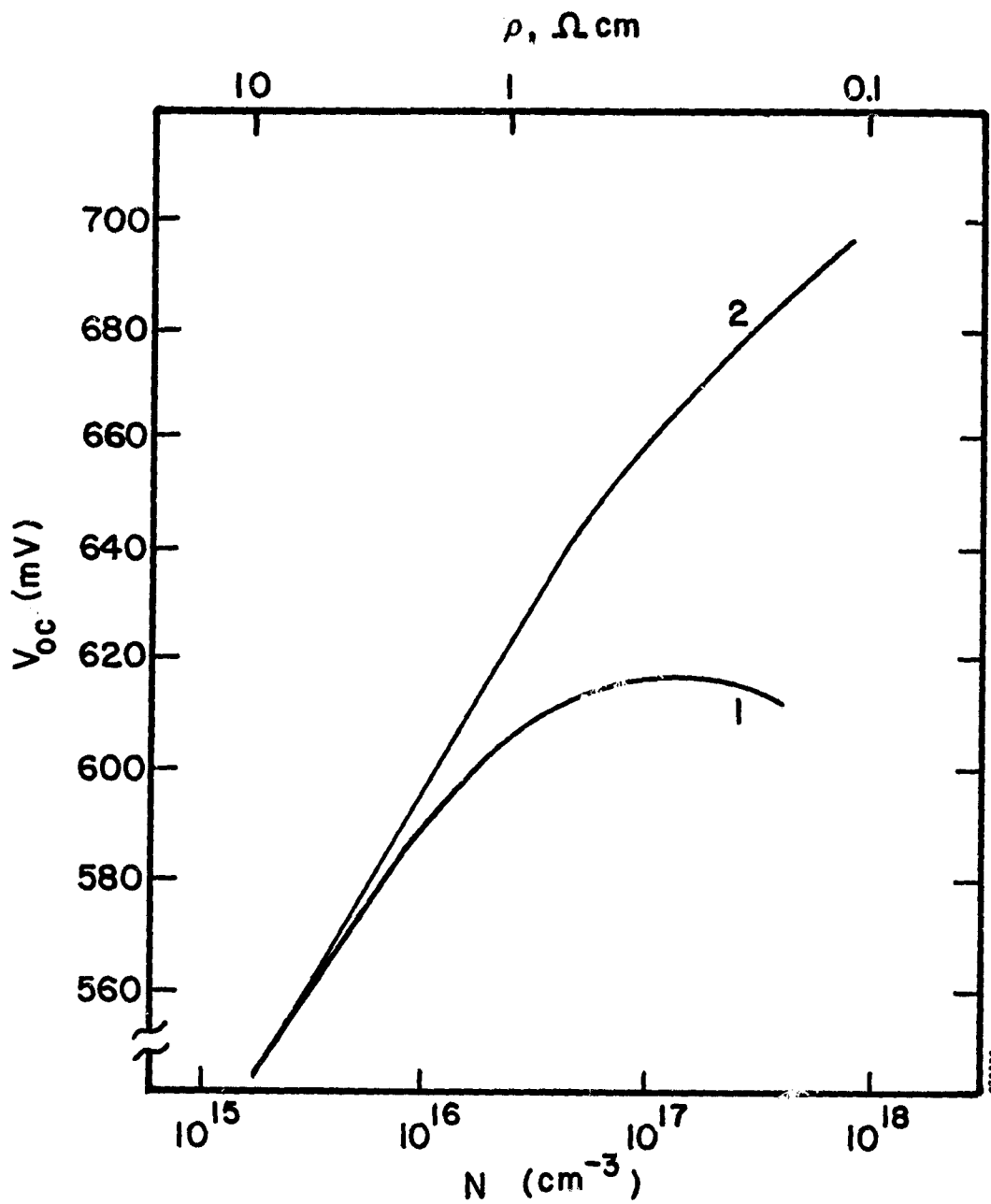
FIGURE 2-41. COMPUTED OPEN-CIRCUIT VOLTAGE, INCORPORATING
AUGER RECOMBINATION (1) WITH BANDGAP NARROWING
AND (2) WITHOUT BANDGAP NARROWING[4]
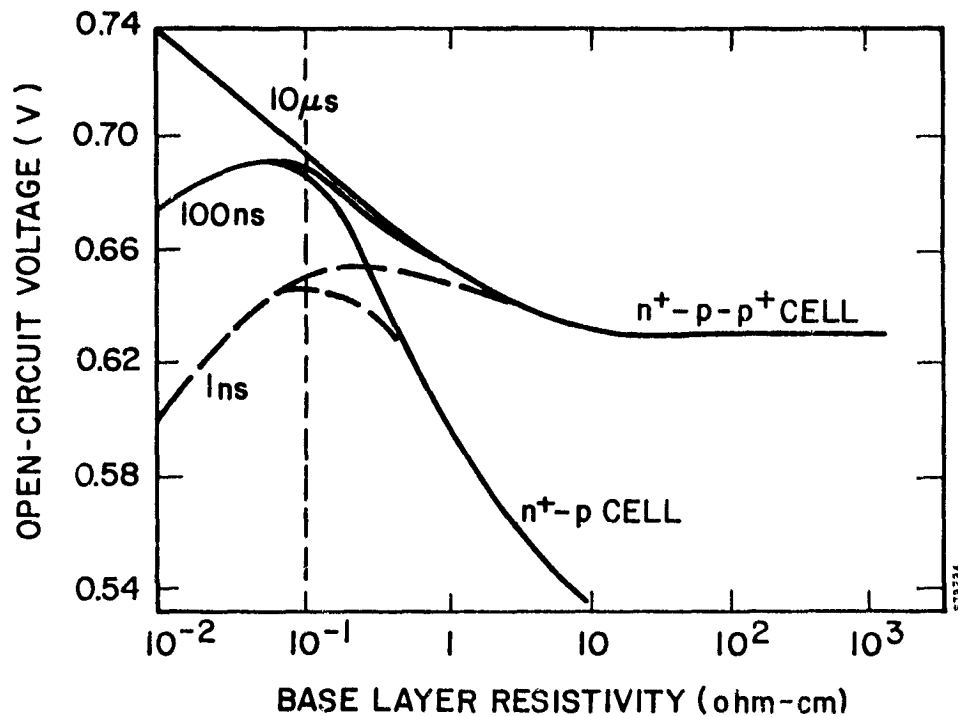
FIGURE 2-42. OPEN-CIRCUIT VOLTAGE AS A FUNCTION OF DOPANT
CONCENTRATION IN THE JUNCTION LAYER, WITH THE
JUNCTION LAYER LIFETIME AS A PARAMETER[16]

2.3 SOLAR CELL FABRICATION

Most of the material used in this program was vacuum float-zone; some crucible
grown material was also procured at the 0.1-ohm-cm level for comparison in the process
sequence.

The bulk minority-carrier lifetimes were measured using the A.C.
photoconductivity technique. Results are shown in Table 2-3. This method uses the light
output of a sinewave-modulated light emitting diode (LED) which emits at 900 nm. The
LED illuminates a silicon sample which has been prepared, at low temperature, with a
Schottky-barrier contact that is semitransparent. Upon illumination, a photocurrent is
generated with a characteristic phase shift between the sinewave-modulated LED and

TABLE 2-3. MINORITY-CARRIER LIFETIME FOR AS-RECEIVED SILICON

Resistivity	Orientation	Measured Lifetime (microseconds)
0.1	(100)	15
0.3	(100)	5
0.5	(100)	13
1.0	(100)	5
1.0	(111)	50
10.0	(100)	7

Note: All material — vacuum float-zone process; surfaces — polished front, etched back; thicknesses — 300 microns (0.012 inch).

Schottky diode output. This phase shift can then be related to carrier lifetime by the relationship, $\tan \phi = \omega \tau /2$, where ϕ is the measured phase shift, ω is the LED modulation frequency and τ is the desired minority-carrier lifetime. The phase shift was measured using a lock-in amplifier at various frequencies to improve the accuracy of the technique. A computer program then found the best linear fit to determine each sample's lifetime.

2.3.1   Solar Cell Performance Evaluation (Baseline Process)

Three low-resistivity silicon solar cell lots were fabricated to assess device characteristics. The cells were processed with 0.1-, 0.3-, 0.5- and 10.0-ohm-cm (100) float-zone silicon using the program baseline cell process listed in Table 2-4. The cell structure was n^+pp^+ with implanted n^+ and p^+ layers. Cells made by this process with 10-ohm-cm Czochralski silicon have resulted in efficiencies of 14.0% AMO. In this test, 10-ohm-cm float-zone silicon control wafers were used for process verification. Table 2-5 shows AMO cell performance data recorded for both low-resistivity cells and the control wafers for each lot. Results show that lower cell efficiencies were obtained using the 0.5-, 0.3-, and 0.1-ohm-cm material. Both P_{max} and I_{sc} decreased with decreasing substrate resistivity, as shown in Table 2-5 and summarized in Table 2-6. The best I-V characteristic from each resistivity is shown in Figure 2-43. One of the 10-ohm-cm control wafers showed a peak efficiency of 13.4% AMO, for cell number 1146-1B.

Cells processed using 0.1-ohm-cm silicon and the baseline process show a flat spot on the I-V curves near the P_{max} voltage. One cell, from an earlier process run, was submitted to NASA-LeRC for analysis. Spectral response, dark forward I-V, and AMO I-V characteristics were measured. Results from the NASA-LeRC spectral response measurements show unusually high blue efficiency, within the 0.45- to 0.65-micron wavelength band. Results from the dark forward I-V analysis show a junction A value of 0.99 and I_o of 3.28×10^{-12} A. Relatively high junction recombination-generation currents were measured for all low-resistivity cells with evaporated AR coatings.

2.3.2   Integration of Furnace Annealing and Oxidation

The thermal oxidation experiments (described in Section 2.2.8) resulted in a major increase in open-circuit voltage when measured by point-probe methods without contact metallization. The simultaneous annealing/oxidation process was then integrated into a solar cell process sequence, as shown in Table 2-7. The unique feature of the sequence is rapid oxidation of the junction surface during high-temperature, $850^\circ C$ annealing. Oxide growth is accelerated by water vapor and the presence of implanted phosphorus. The starting material was 0.1-ohm-cm, p-type, float-zone silicon, with mechanically polished front surfaces and brightly etched back surfaces. All wafers received a shallow, high-dose phosphorus implant designed to give an n+ region with a maximum impurity concentration of 4×10^{20} cm^{-3} and a junction approximately 0.2 micron deep. Thermal oxidation and annealing of the implant damage were performed simultaneously at $850^\circ C$

TABLE 2-4.   BASELINE PROCESS SPECIFICATION FOR
HIGH-EFFICIENCY IMPLANTED CELLS

Silicon Material   (100)   FZ p-type

Surfaces: Front - Polished

Back - Bright Etched

Process Sequence

Implant: Front - 2×10^{15} $^{31}P^+$/cm^2, 5 keV, 10° incidence

Back - 5×10^{15} $^{11}B^+$/cm^2, 25 keV, 10° incidence

Anneal: Simultaneous phosphorus and boron anneal in

nitrogen

550°C - 2 hours

850°C - 15 minutes

550°C - 2 hours

Clean: Buffered HF

HI rinse

Front Contact: Evaporate 400 A Cr + 400 A Au

Define pattern with Kodak KTFR process

Electroplate 12 microns Ag

Clean: Buffered HF

DI rinse

Back Contact: Evaporate 400 A Al + 1 micron Ag

AR Coat: Evaporate 700 A TiO$_2$

Sinter: 400°C - 10 minutes in nitrogen

TABLE 2-5.   AM0 CELL PERFORMANCE CHARACTERISTICS FOR 0.1-,
0.3-, 0.5- AND 10-ohm-cm STARTING MATERIAL

Cell No.	V_{oc} (mV)	I_{sc} (mA)	P_{max} (mW)	F.F.	Resistivity (ohm-cm)	
56-1144-1A	570	150	65.8	0.77	0.10	
1B	572	150	65.9	0.77	0.10	
2A	545	138	36.6	0.49	0.1	
2B	565	137	40.1	0.52	0.1	
3A	570	137	35.1	0.45	0.1	
3B	592	136	48.6	0.60	0.1	
4A	570	150	63.7	0.75	10	control
4B	570	148	65.3	0.77	10	control
5A	500	137	33.6	0.49	0.1	
5B	555	138	38.2	0.50	0.1	
6A	570	138	40.9	0.52	0.1	
6B	565	138	39.9	0.51	0.1	
8A	572	148	65.8	0.78	10	control
56-1145-1A	605	142	60.6	0.71	0.3	
1B	605	142	58.0	0.67	0.3	
2B	608	142	63.8	0.74	0.3	
3A	585	151	68.0	0.77	10	control
4A	545	142	36.7	0.47	0.3	
4B	580	143	39.9	0.48	0.3	
5A	595	142	52.4	0.62	0.3	
5B	595	142	55.1	0.65	0.3	
6A	585	152	67.7	0.76	10	control
6B	585	153	67.4	0.75	10	control
7A	578	150	67.0	0.77	10	control
7B	578	150	66.7	0.77	10	control
8A	580	142	45.1	0.55	0.3	
8B	600	142	57.8	0.68	0.3	
56-1146-1A	580	158	69.8	0.76	10	control
1B	585	158	72.5	0.78	10	control
2A	605	150	66.8	0.72	0.5	
2B	600	150	64.4	0.72	0.5	
5A	610	149	70.7	0.78	0.5	
5B	610	148	71.1	0.79	0.5	
6A	610	150	69.9	0.76	0.5	
6B	605	150	66.3	0.73	0.5	
7A	610	148	69.4	0.77	0.5	
7B	610	150	70.2	0.77	0.5	
8A	605	149	64.9	0.72	0.5	
8B	605	149	67.7	0.75	0.5	

TABLE 2-6. PERFORMANCE SUMMARY OF LOW-RESISTIVITY AND 10-ohm-cm CONTROL WAFERS USING BASELINE ION IMPLANTATION PROCESS

AM0-25°C Characteristics

Resistivity (ohm-cm)	V_{oc} (mV)	I_{sc} (mA)	P_{max} (mW)	Fill Factor	Number of Cells
10.0 (control)	578	152	67.0	0.77	12
0.5	607	149	68.1	0.75	10
0.3	590	142	52.2	0.62	9
0.1	558	137	39.1	0.51	8

Notes: TiO_2 AR

Ion-implanted junction and BSF

Multistep furnace anneal
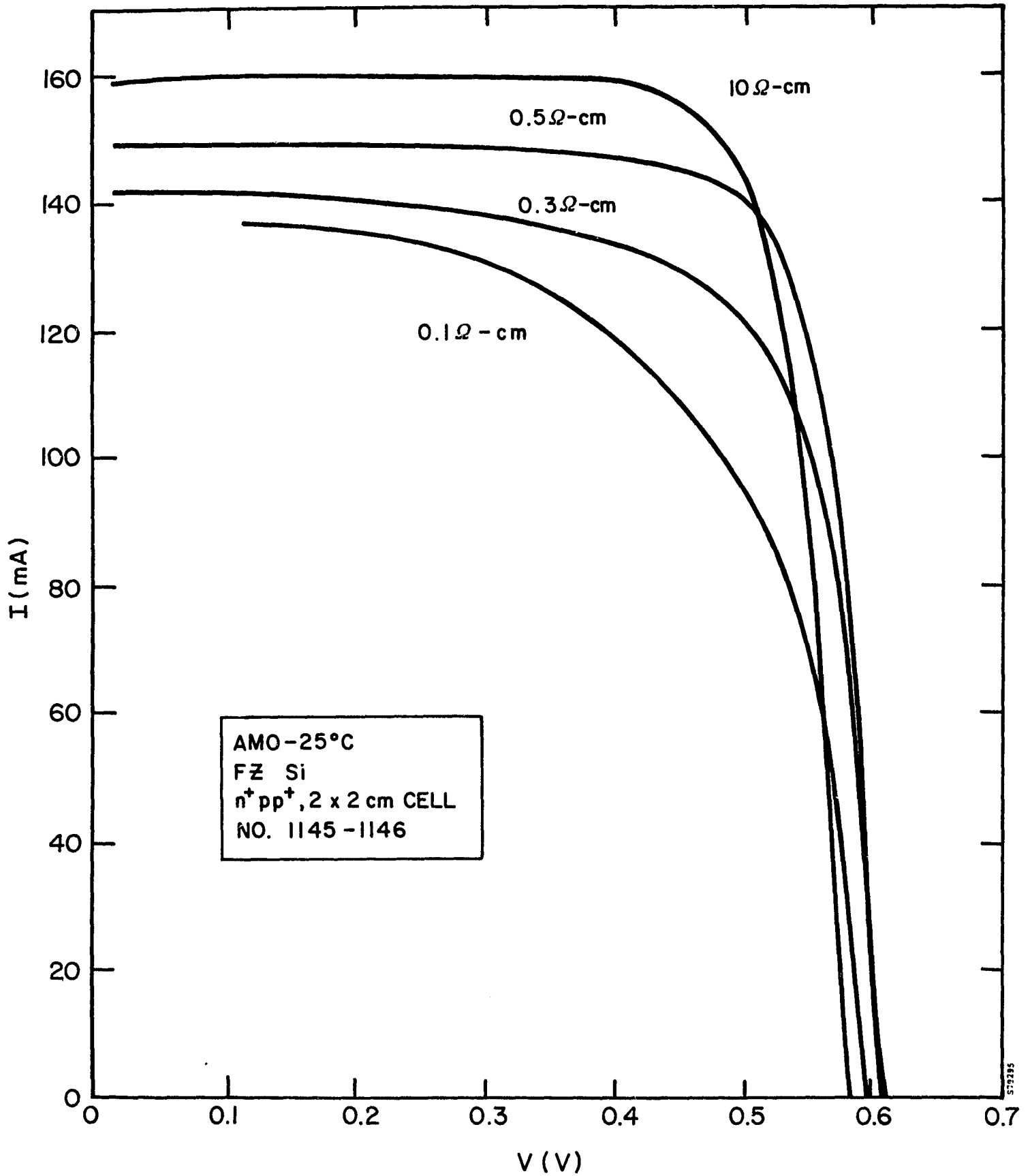
FIGURE 2-43. AM0-25°C CELL CHARACTERISTICS FOR 0.1-, 0.3-, 0.5-, AND 10.0-ohm-cm
IMPLANTED DEVICES FABRICATED WITH THE BASELINE PROCESS

TABLE 2-7. PROCESS SPECIFICATIONS FOR HIGH-EFFICIENCY,
ION-IMPLANTED CELLS

Silicon Material   FZ, 0.1 cm, p-type, 2" dia., (100) orientation

   Surfaces: Front polished, back bright etched

Process Sequence

   Implant Junction: 2×10^{15} $^{31}P^+$/cm^2, 5 keV, 10° incidence

   Anneal & Oxidize: 550°C - 2 hours in oxygen
                             850°C - 30 minutes in steam
                             700°C - 2 hours in oxygen
                             550°C - 2 hours in oxygen

   Etch Contact
   Windows in Oxide: Define pattern with Kodak KTFR process
                             Buffered HF oxide etch

   AR Coat: Etch remaining oxide until dark blue (1000A)

   Back Contact: Evaporate 400A Al
                             Alloy 620°C - 15 minutes in nitrogen

   Clean: 20:1 HF - 10 seconds

   Front Contact: Evaporate 500A Ti + 200A Pd + 1,000A Ag

   Back Contact: Evaporate 500A Ti + 200 Pd + 10,000A Ag

   Front Contact: Define pattern with Kodak KTFR process
                             Mask back side of wafer with KTFR
                             Electroplate 12 micrometers Ag

   Cut Cells: Saw two 2 x 2-cm cells from each 2" wafer

for 30 minutes in a steam-saturated oxygen atomsphere. A postanneal of 550°C for 2 hours in dry O_2 served to increase the density of the oxide. Contact windows were then etched in the oxide for contact metallization, and the entire oxide was etched to 1000A to provide antireflection characteristics. Aluminum was alloyed at 620°C to provide a thin back surface p+ layer for ohmic contact, not a BSF. Evaporated TiPdAg contact metallization was employed for both front and back contacts.

The best cell from one lot was measured by NASA-LeRc under AM0-25°C conditions, and was characterized by an open-circuit voltage of 644 mV. The short-circuit current was 138 mA, and the fill factor was 75.6%. Figure 2-44 shows the AM0 I-V characteristics of this cell, Figure 4-45 shows the spectral response, and Figure 2-46 shows the dark I-V characteristics; all were measured by NASA-LeRC. The remaining seven cells in this process lot had voltages between 638 mV and 640 mV, and currents ranging from 138 mA to 140 mA. The oxide thickness of the 644-mV cell was measured by an ellipsometer to be 1380°A, with an index of refraction of 1.48. SIMS profiles were also measured to characterize the junction for boron and phosphorus concentrations in the oxide and in the junction layer, as shown in Figure 2-47.

Incremental oxide stripping was used to investigate the effects of thermal oxides on cell voltage and current performance. One of the cells processed according to the specifications in Table 2-7 was subjected to successive oxide etching treatments of 30 seconds each in 5:1 H_2O:buffered HF solution. After each oxide etch step, the open-circuit voltage, short-circuit current, and fill factor were measured under AM0-25°C conditions; Figures 2-48 through 50 show the V_{oc}, I_{sc}, and fill-factor changes with reduced oxide thickness. The oxide thicknesses were not measured, but were calculated from buffered HF oxide etching rates. The thickness of oxide removed by isochronal etch periods was assumed to be the same for all steps.

The results of this layer stripping experiment show that the short-circuit current dropped predictably from 137 mA to 97 mA by stripping the AR coating off the cell. Our experience in the past has shown I_{sc} to increase by 40% when a good AR coating is added to an uncoated, bare silicon cell. The V_{oc} initially decreases as expected with decreasing current, according to the expression $V_{oc} = V'_{oc} - 26 \ln I/I'$, but falls off rapidly when the oxide within several hundred angstroms of the oxide/silicon interface is removed. This rapid falloff of V_{oc} with removal of the last few hundred angstroms of oxide suggests that the surface recombination velocity is greatly increased without an oxide layer. The layer stripping experiments also demonstrate that the improved V_{oc} is not due to an HLE junction, which might be inferred from the SIMS profile of Figure 2-47.
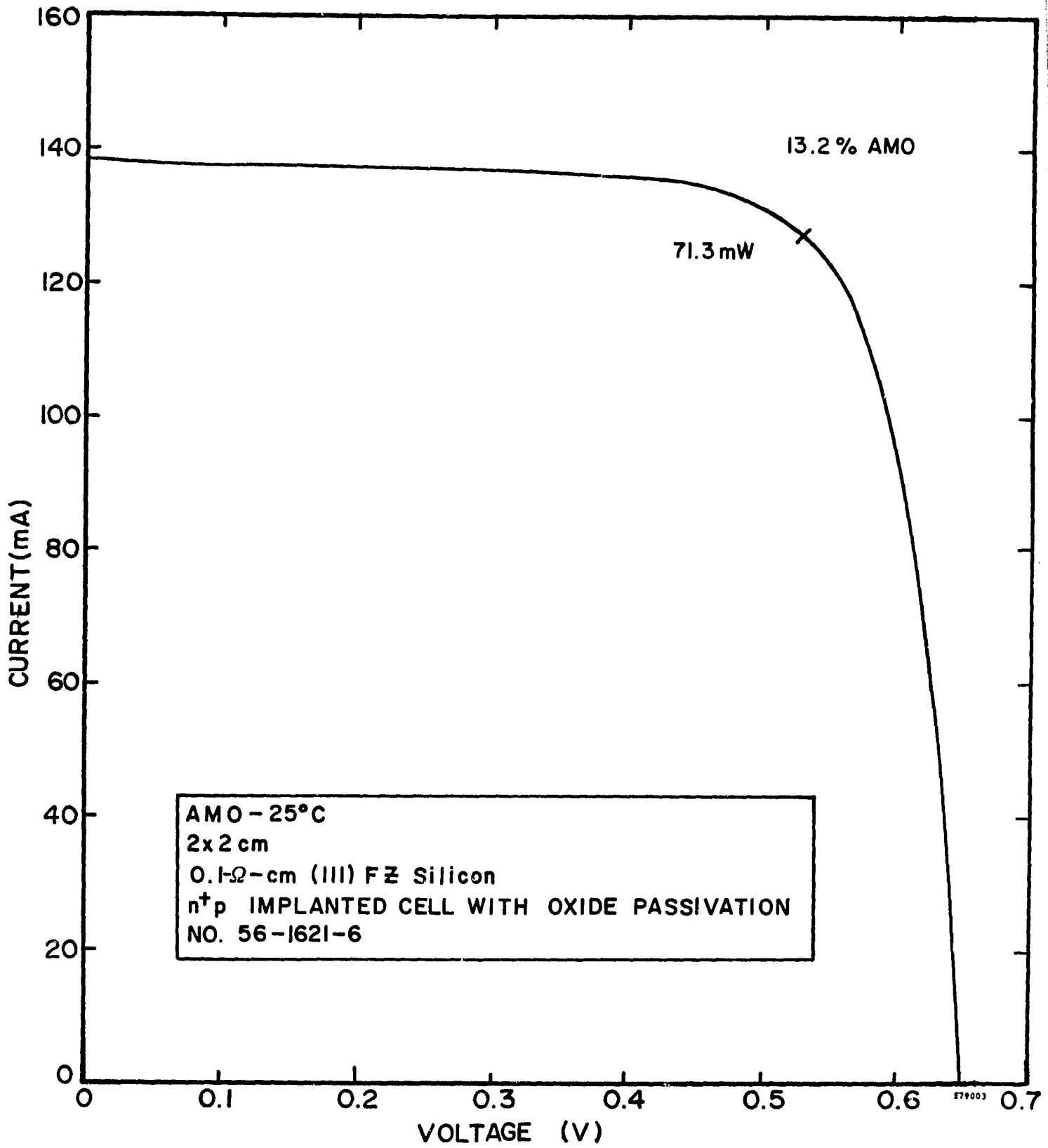
FIGURE 2-44.   AM0-25°C I-V CHARACTERISTICS FOR 0.1-ohm-cm, ION-IMPLANTED
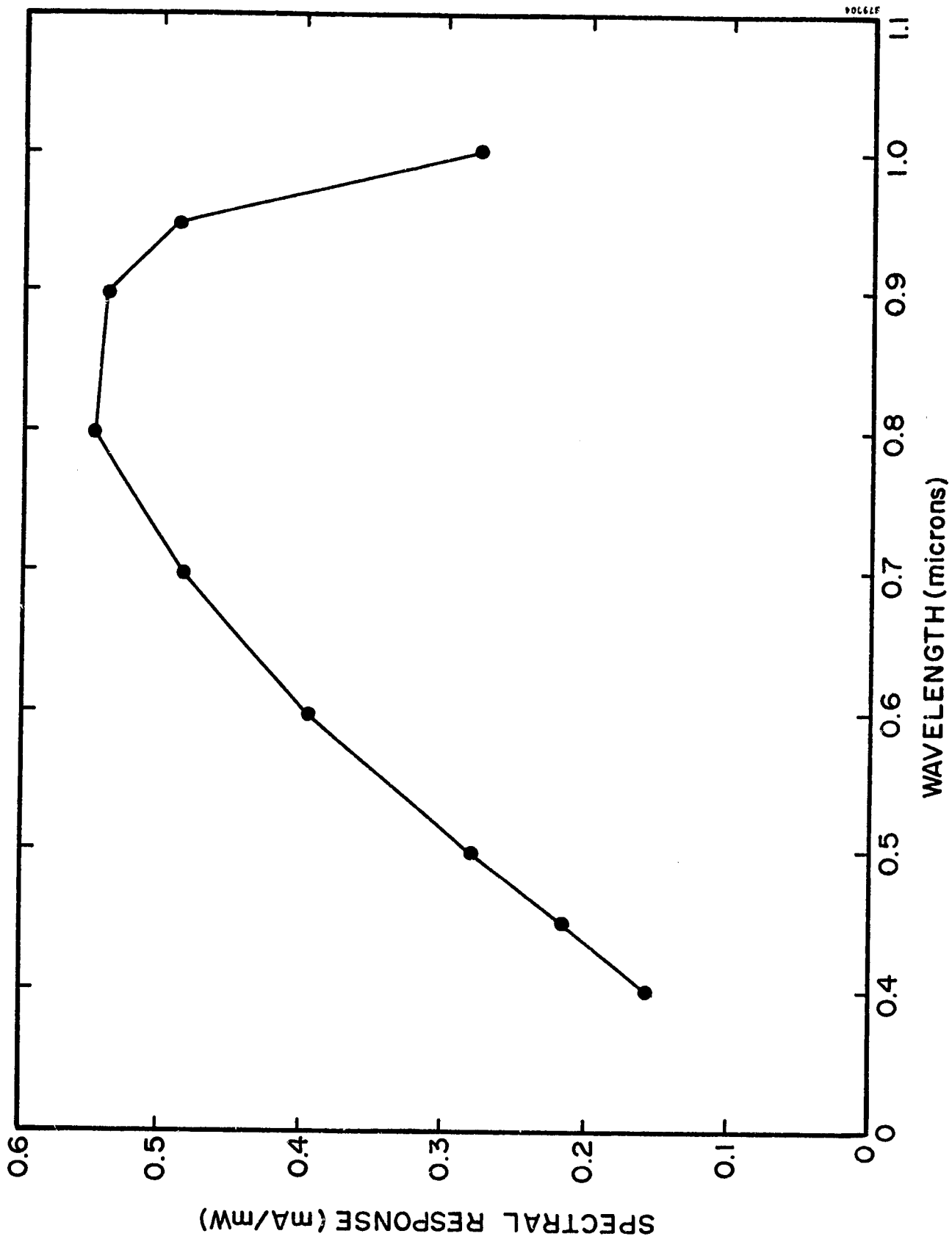SOLAR CELLS WITH OXIDE SURFACE PASSIVATION

FIGURE 2-45. ABSOLUTE SPECTRAL RESPONSE FOR 0.1-ohm-cm, ION-IMPLANTED SOLAR CELLS WITH OXIDE SURFACE PASSIVATION
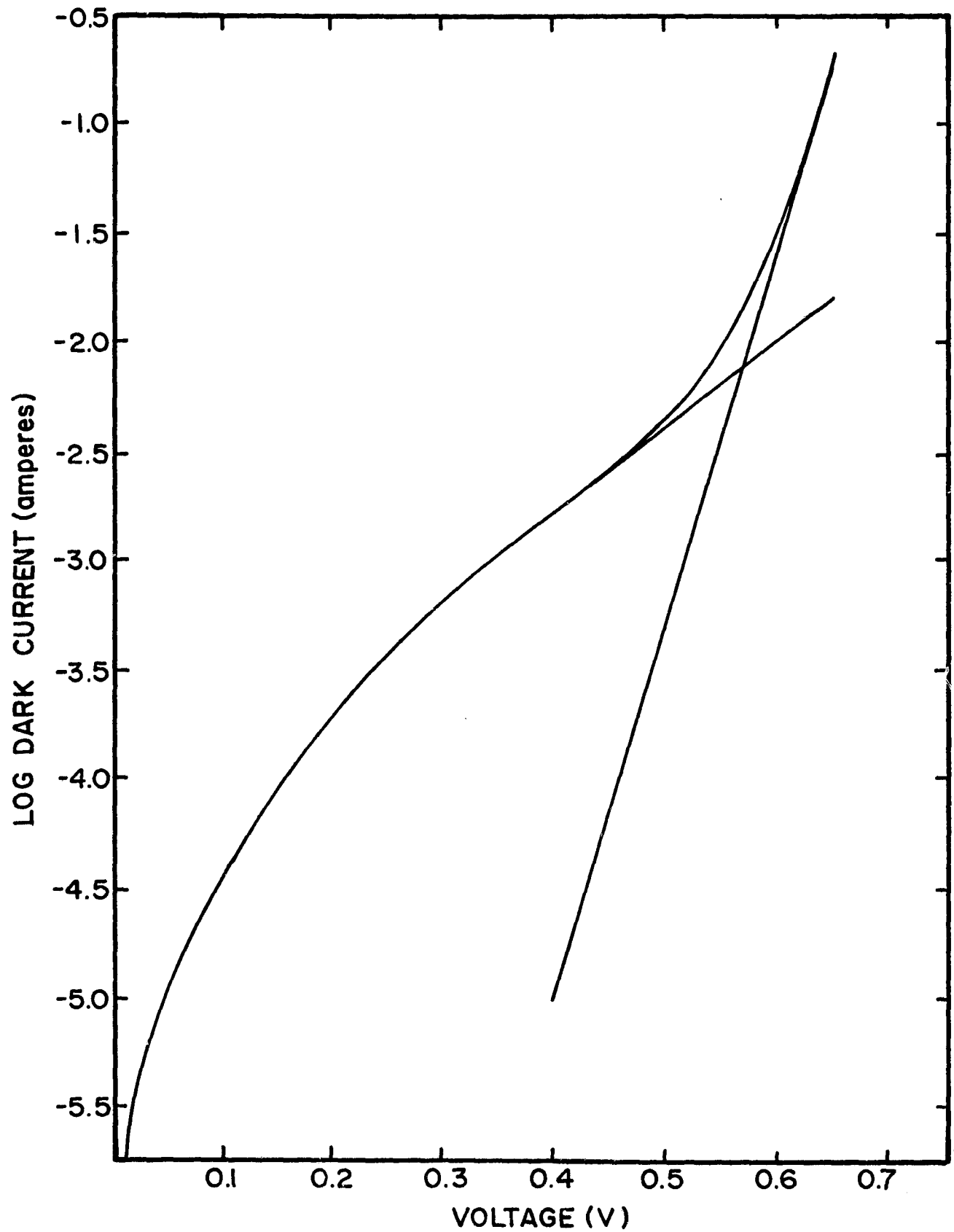
FIGURE 2-46. DARK-FORWARD I-V CHARACTERISTICS FOR 0.1-ohm-cm, ION-IMPLANTED SOLAR CELLS WITH OXIDE SURFACE PASSIVATION
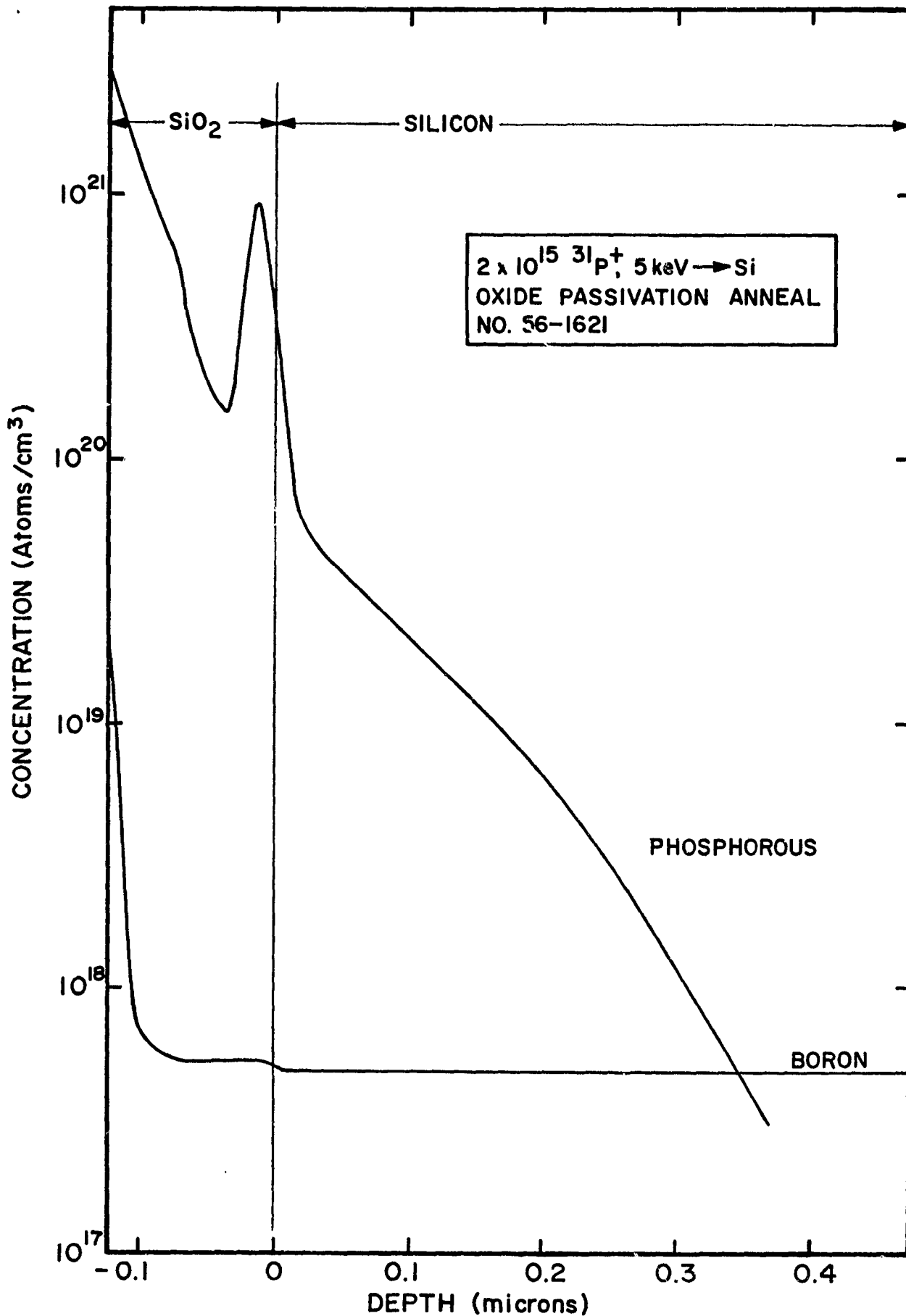
FIGURE 2-47.   MEASURED BORON AND PHOSPHORUS PROFILES FOR
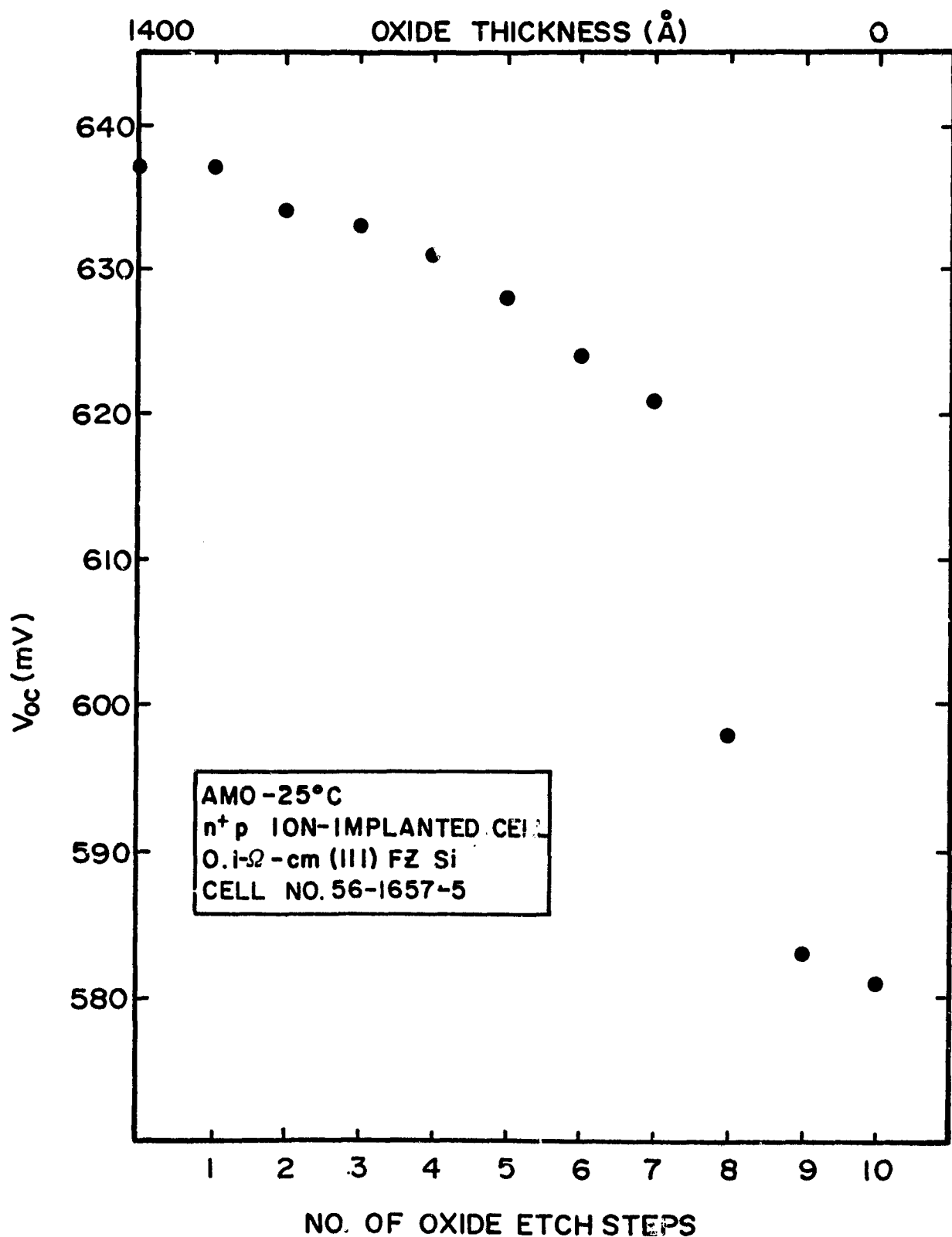ION-IMPLANTED, OXIDE-PASSIVATED SOLAR CELLS

FIGURE 2-48. AM0-25°C OPEN-CIRCUIT VOLTAGE MEASURED
AS A FUNCTION OF OXIDE THICKNESS FOR
0.1-ohm-cm, ION-IMPLANTED CELLS
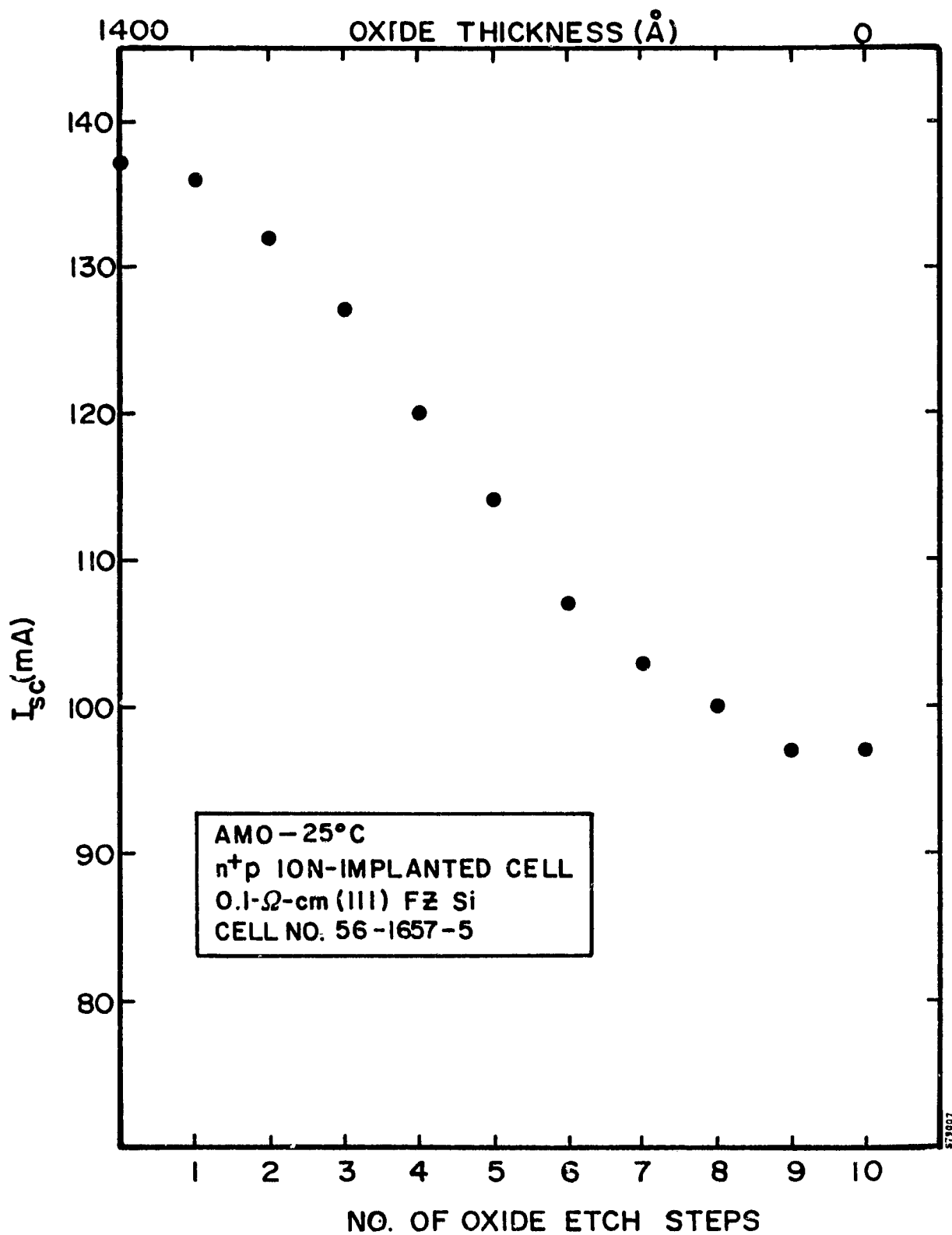
FIGURE 2-49. AM0-25°C SHORT-CIRCUIT CURRENT MEASURED
AS A FUNCTION OF OXIDE THICKNESS FOR
0.1-ohm-cm, ION-IMPLANTED CELLS
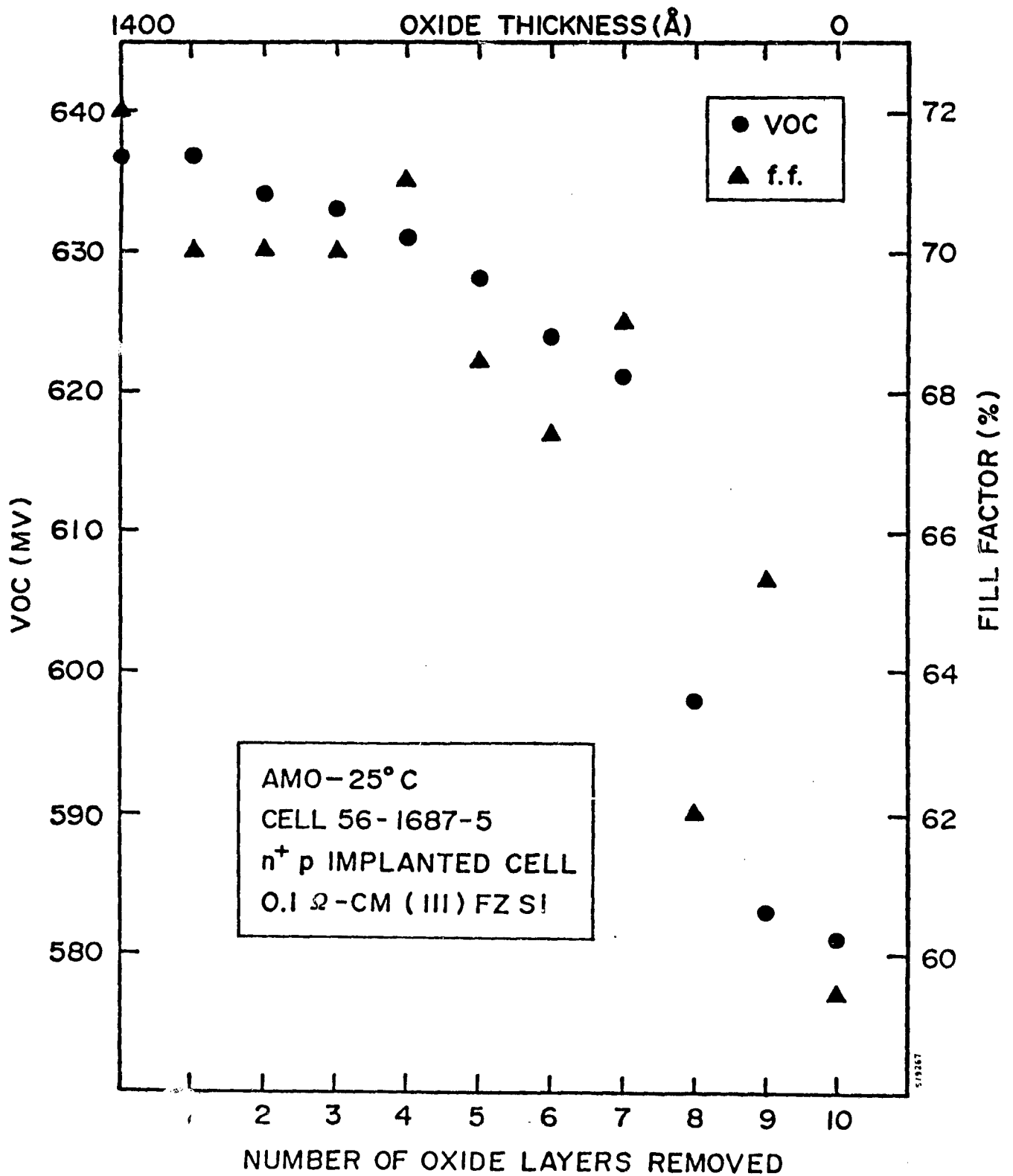
FIGURE 2-50. AM0-25ºC OPEN-CIRCUIT VOLTAGE AND FILL
FACTOR AS A FUNCTION OF OXIDE THICKNESS
FOR 0.1-ohm-cm, ION-IMPLANTED CELLS

2.3.3 Solar Cells With Tailored Emitters and Oxide Passivated Surfaces

The final effort of this program was to fabricate 2×2-cm solar cells with tailored n-type emitters in 0.1-ohm-cm, boron-doped silicon wafers. Half the cells fabricated had oxide passivation, and the other half had evaporated TiO_2 AR coatings only. Oxide passivated cells incorporated the thermal SiO_2 layer as an AR coating. Both (100) and (111) oriented silicon wafers were processed in this matrix. A block diagram of the processing matrix is shown in Figure 2-51.

The emitter profiles specified for the matrix included both exponential and linear doping gradients. Three different surface concentrations were specified, from which the various implants needed for each emitter profile were calculated by the computer program IMPLANT. All junction depths were specified to be at 0.2 micron, and all n-type emitters were phosphorus doped. Table 2-8 shows the implant parameters necessary for the emitter profiles of this matrix.

The expected exponential and linear profiles are shown in Figures 2-52 and 2-53, on both logarithmic and linear scales for clarity. Included as a comparison on the same scale are the calculated profiles for both diffusion from an unlimited source (an error function), and diffusion from an implanted, Gaussian distribution. For all profiles, the junction depth was specified as 0.2 micron in 0.1-ohm-cm silicon (base doping level of 5×10^{17} atoms/cm^3).

Following phosphorus ion implantation, all wafers received a multistep thermal anneal. The anneal sequence for the oxide process is as follows:

550°C – 2 hours in dry O_2
850°C – 30 minutes in wet O_2
700°C – 2 hours in dry O_2
550°C – 2 hours in dry O_2

For those wafers receiving the standard process sequence but without an oxide, the anneal temperatures and durations were identical, but all annealing was performed in dry N_2 atmosphere.
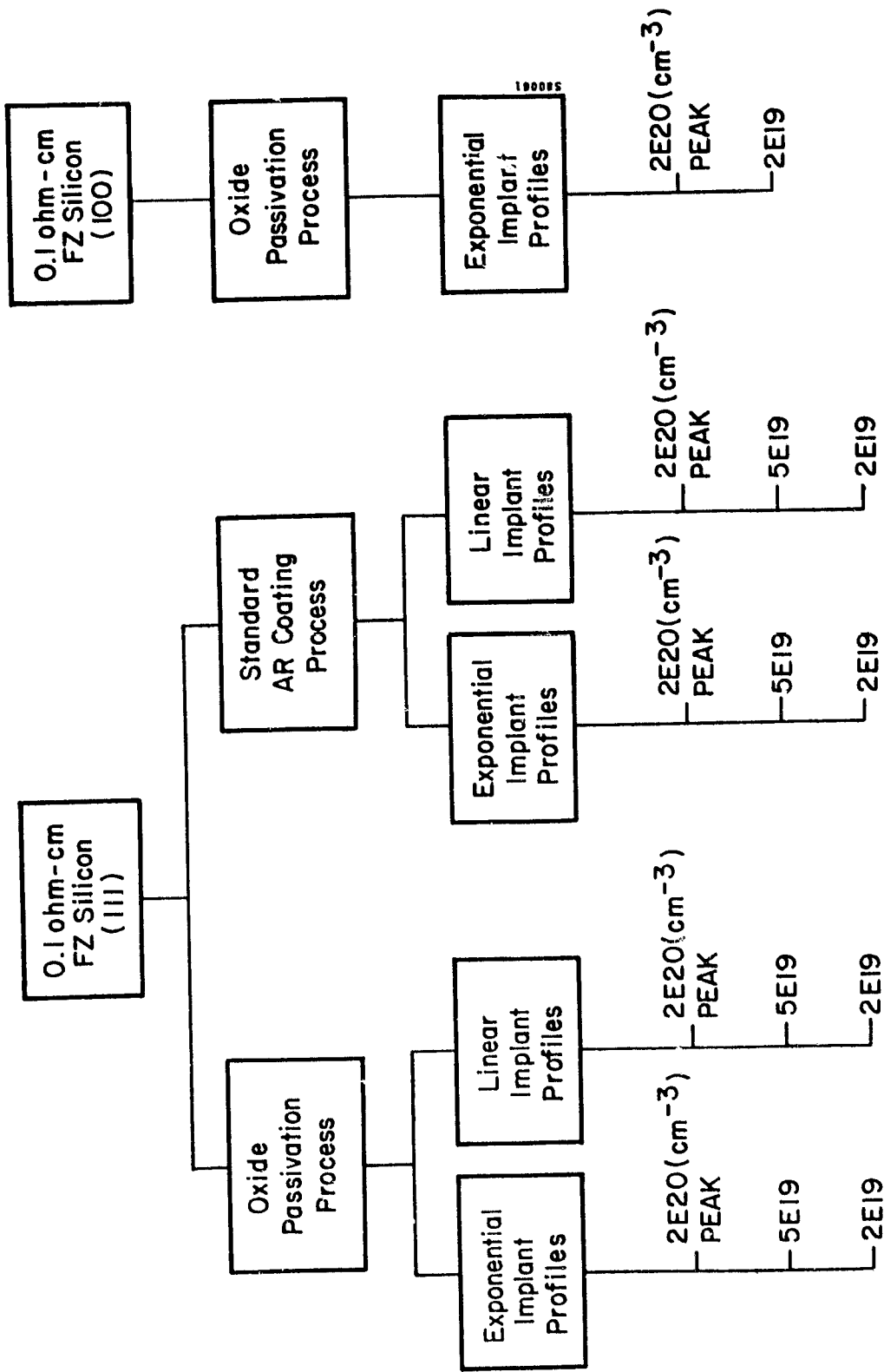
FIGURE 2-51. SUMMARY OF TAILORED EMITTER TEST MATRIX

2-77

TABLE 2-8. IMPLANT PARAMETERS FOR TAILORED EMITTER
TEST MATRIX

Peak Implant Profile	Concentration (cm^{-3})	X_j (microns)	Implant Energy (keV)	Implant Dose (ions cm^{-2})
Exponential	2E20	0.2	42	3.48×10^{14}
			16	2.76×10^{14}
			5	1.44×10^{14}
Exponential	5E19	0.2	42	8.7×10^{13}
			16	6.9×10^{13}
			5	3.6×10^{13}
Exponential	2E19	0.2	42	3.48×10^{13}
			16	2.76×10^{13}
			5	1.44×10^{13}
Linear	2E20	0.2	72	1.02×10^{15}
			27	5.94×10^{14}
			7.5	2.3×10^{14}
Linear	5E19	0.2	72	2.56×10^{14}
			27	1.49×10^{14}
			7.5	5.75×10^{13}
Linear	2E19	0.2	72	1.02×10^{14}
			27	5.94×10^{13}
			7.5	2.3×10^{13}
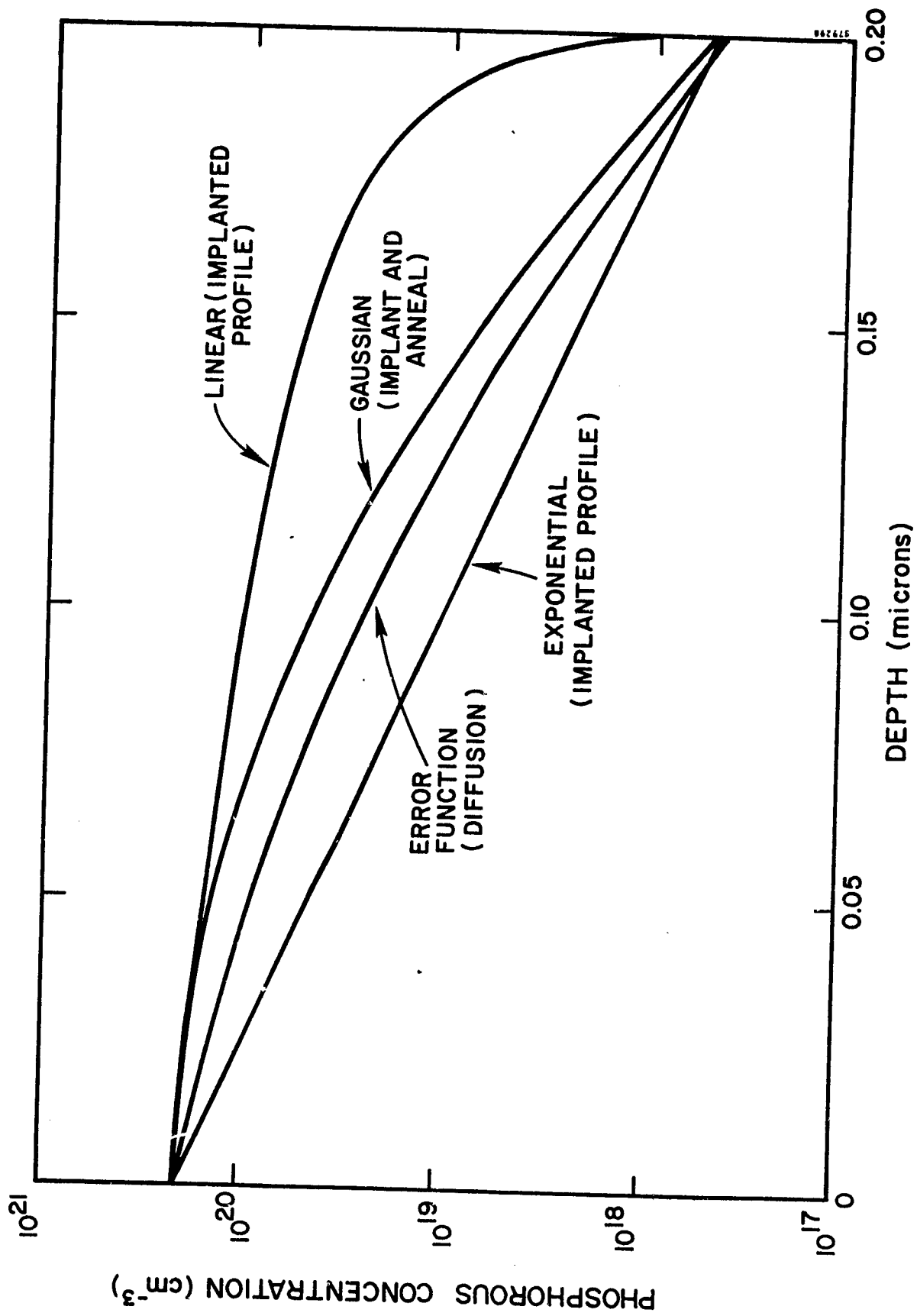
FIGURE 2-52. PREDICTED EMITTER PROFILES ON LOGARITHMIC SCALE
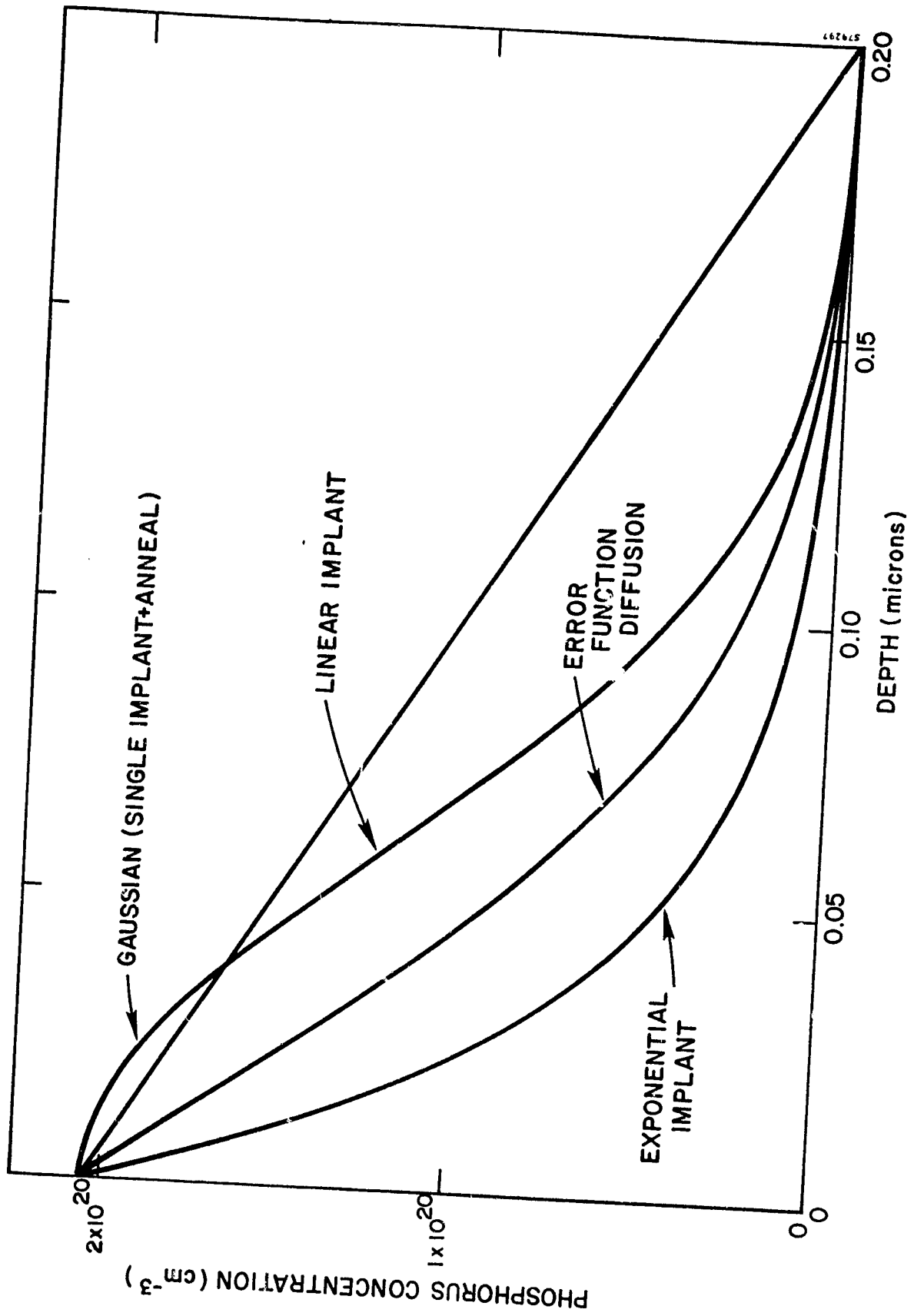
FIGURE 2-53. PREDICTED EMITTER PROFILES ON LINEAR SCALE

TiPdAg contacts were evaporated onto the wafers and silver plated to 10- to 15-micron thickness; two 2 x 2-cm cells were then saw cut from each 2-inch wafer. Cells not having an oxide passivating layer received an evaporated TiO_2 AR coating. AM0-25°C I-V characteristics were measured for all cells with Spire's Spectrosun X-25 Mark II solar simulator at 135.3 mW/cm^2.

Table 2-9 summarizes the measured cell performance data. As shown in Figure 2-54, the open-circuit voltage increases with doping concentration for all implanted emitter profiles tested. Oxide passivated cells also have significantly higher voltages for all emitter dopant concentrations and profile types than cells with TiO_2 AR coatings. Fill factors listed in Table 2-9 do not reflect optimized cell performance. The series resistance measured for the passivated, linear profile junctions increases for decreasing dopant concentration. This trend is a result of using the same front contact design for all cells in the matrix. Spire's 2 x 2-cm grid mask design, as shown in Figure 2-55, is optimized for emitter sheet resistance less than 100 ohms/square. The additional series resistance was not large enough to prevent accurate measurement of open-circuit voltages.

As discussed in Section 2.2.3, a model can be proposed to relate cell performance to the measured doping profiles. The proposed model suggests that only when SRV is sufficiently reduced can bandgap narrowing be a measurable effect. The physical properties which can influence SRV, and therefore obscure bandgap narrowing, include residual lattice damage from incomplete implantation annealing and dangling bonds as well as the quality of the Si-SiO_2 interface. The detailed investigation of these defects and surface states has yet to be investigated for solar cell applications.

TABLE 2-9. AM0-25°C SOLAR CELL PERFORMANCE FOR TAILORED EMITTER WITH AND WITHOUT OXIDE PASSIVATION

Cells Without Passivation (TiO_2 AR)

Emitter Profile	Si	No. of Cells	Avg. V_{oc} (mV)	Avg. I_{sc} (mA)	Avg. F.F. (%)
Exp. 2E20 Peak	(111)	7	591.1	137.7	73.8
Exp. 5E19 Peak	(111)	5	576.2	133.2	63.2
Exp. 2E19 Peak	(111)	5	558.8	128.4	56.4
Linear 2E20 Peak	(111)	6	596.2	134.0	77.1
Linear 5E19 Peak	(111)	5	588.6	132.4	70.8
Linear 2E19 Peak	(111)	6	581.6	128.1	66.7
Gaussian 4E20 Peak (single implant)	(111)	5	610.8	135.6	72.5

Oxide Passivated Cells (Thermal SiO_2)

Emitter Profile	Si	No. of Cells	Avg. V_{oc} (mV)	Avg. I_{sc} (mA)	Avg. F.F. (%)
Exp. 2E20	(111)	6	630.6	139.1	74.8
Exp. 5E19	(111)	6	616.J	137.8	67.2
Exp. 2E19	(111)	5	579.0	126.4	57.8
Linear 2E20	(111)	4	627.0	136.0	78.3
Linear 5E19	(111)	3	599.C	133.0	7?.5
Linear 2E19	(111)	4	590.9	130.0	67.0
Exp. 2E20 Peak	(100)	6	612.5	136.7	75.7
Exp. 2E19 Peak	(100)	5	605.6	114.8	61.4
Gaussian 3E20 Peak (single implant)	(100)	5	628.8	134.8	73.6
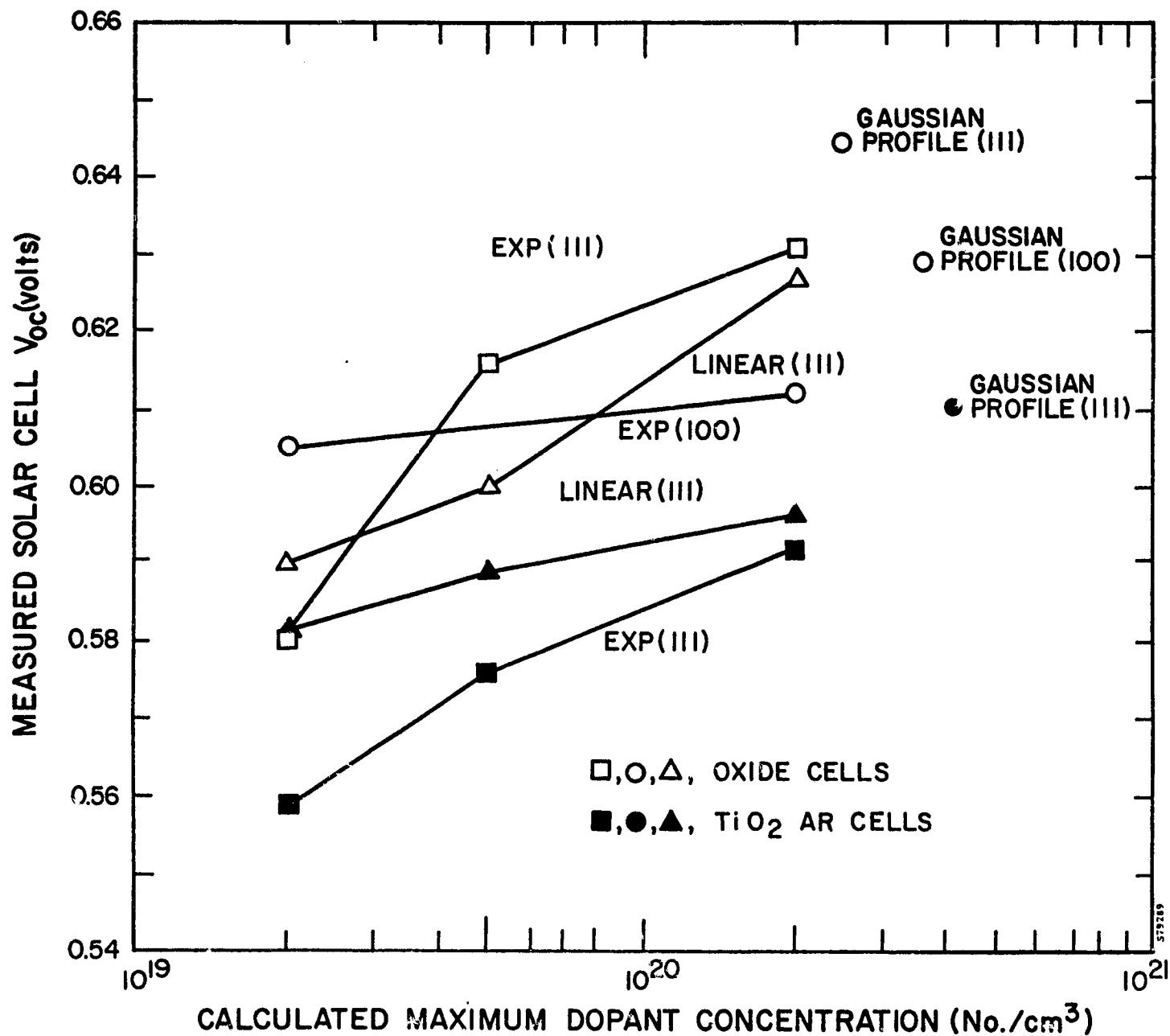
FIGURE 2-54. MEASURED AVERAGE AM0-25°C OPEN-CIRCUIT VOLTAGE FOR TAILORED EMITTER SOLAR CELLS
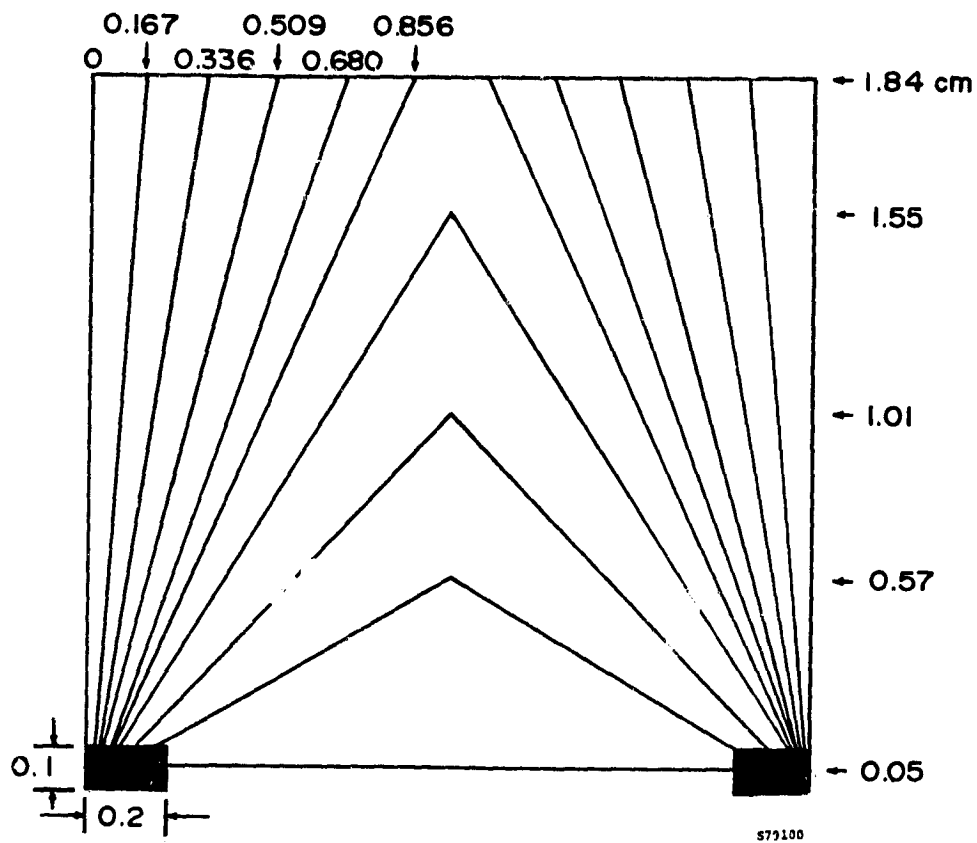
FIGURE 2-55.   BASELINE FRONT CONTACT GRID DESIGN FOR 2 x 2-cm
SOLAR CELLS WITH 100-ohm/square SHEET RESISTANCE

SECTION 3

CONCLUSIONS

This report has described the results of a 14-month program to improve the open-circuit voltage of low-resistivity silicon solar cells. Significant accomplishments during the contract include:

1. Reproducible fabrication of solar cells with open-circuit voltages as high as 645 mV (AM0-25°C) in a shallow junction device structure.

2. Addition of simultaneous oxide growth to optimized implant anneal cycles. The effect of the thermally grown oxide on cell performance is a reduction of surface recombination and the increase in cell open-circuit voltage.

3. Investigation and assessment of bandgap narrowing effects due to high dopant concentrations in solar cell junctions with and without oxide passivation has demonstrated higher open-circuit voltage with increased concentration.

4. High-efficiency cells, prepared by ion implantation of phosphorus, demonstrated with low-resistivity silicon. Cells processed with this process have efficiencies as high as 12.5% AM0 and fill factors of 0.78.

Further process and device development should now be directed toward investigation of ion implantation and furnace annealing with simultaneous oxidation. As part of this development, surface recombination should be minimized for both junction and BSF layers by oxidation. Such an investigation must include characterization of the oxide doping and dopant redistribution effects on cell performance.

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APPENDIX

FURNACE ANNEAL TEST DATA
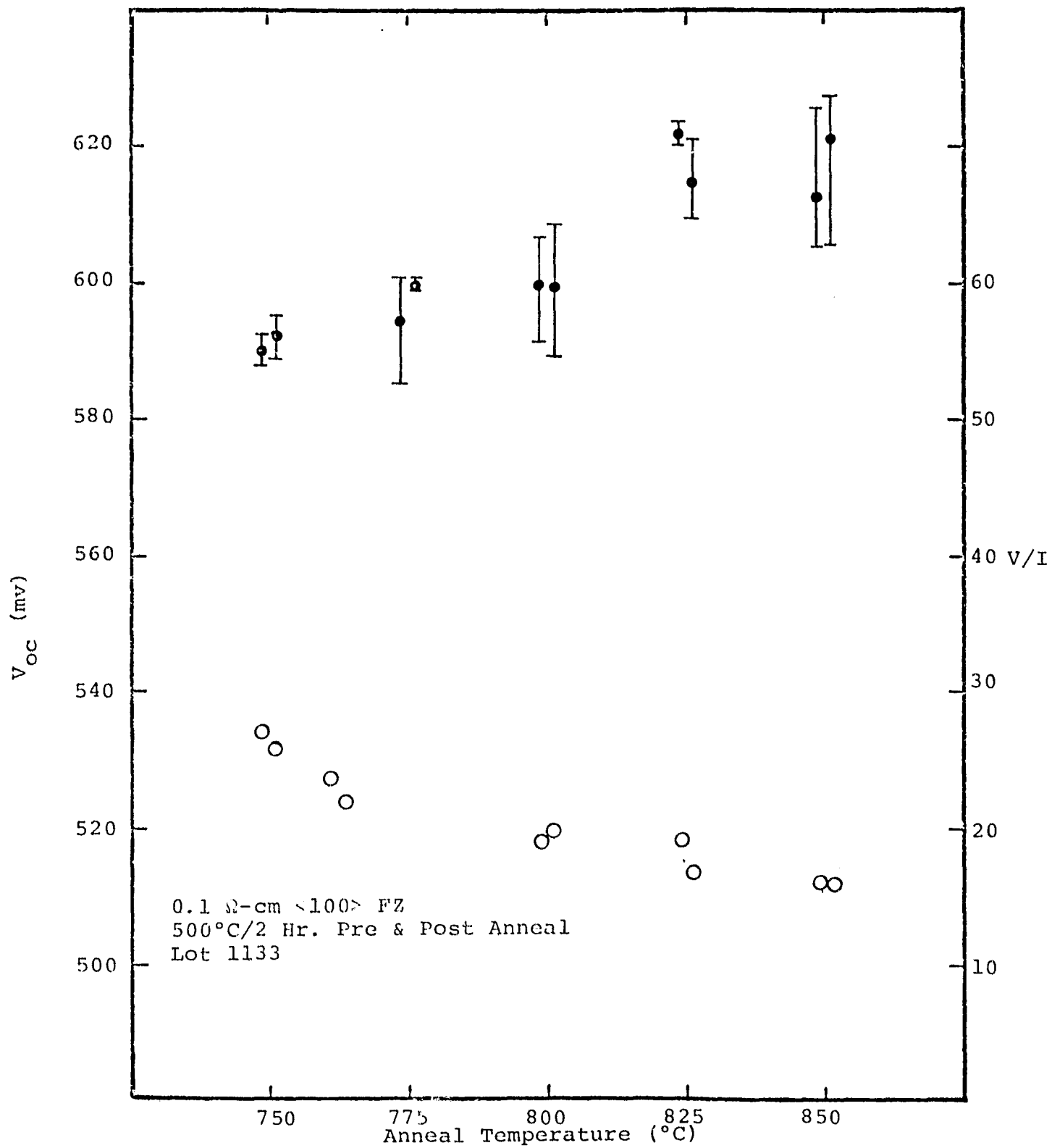
FIGURE A-1. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
0.1-ohm-cm SILICON

A-1
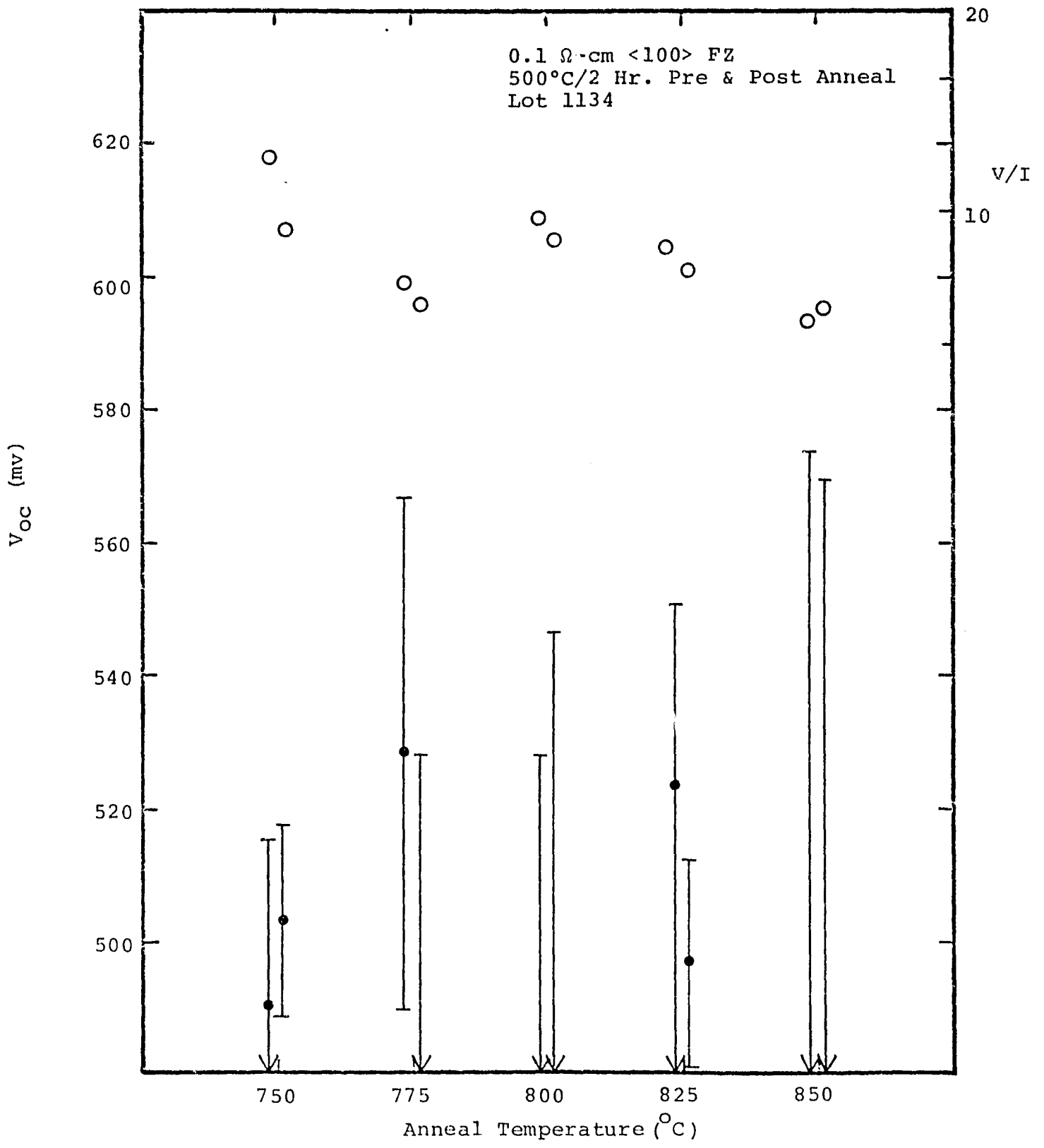
FIGURE A-2. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
0.1-ohm-cm SILICON
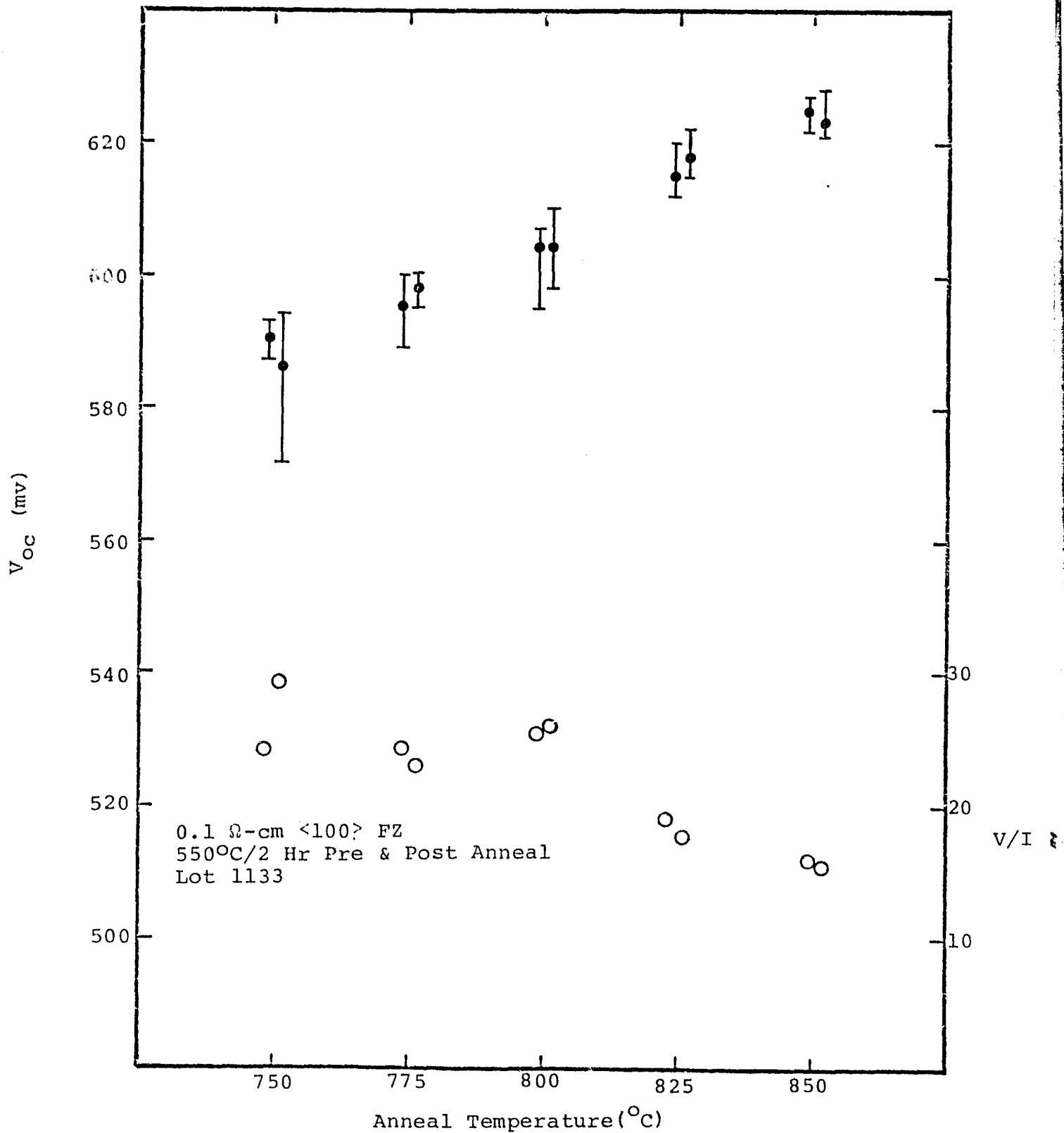
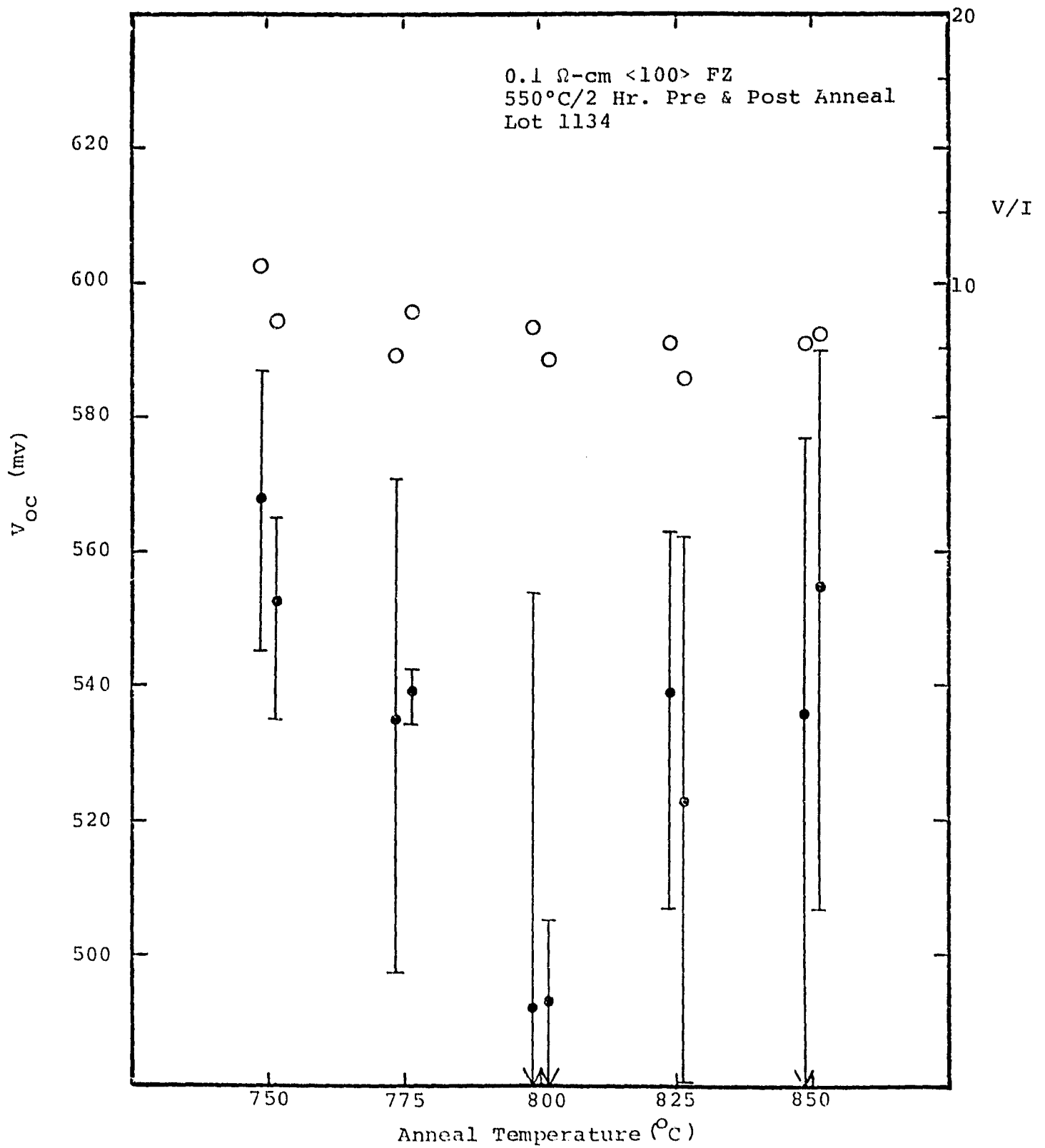FIGURE A-3. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
0.1-ohm-cm SILICON

FIGURE A-4. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
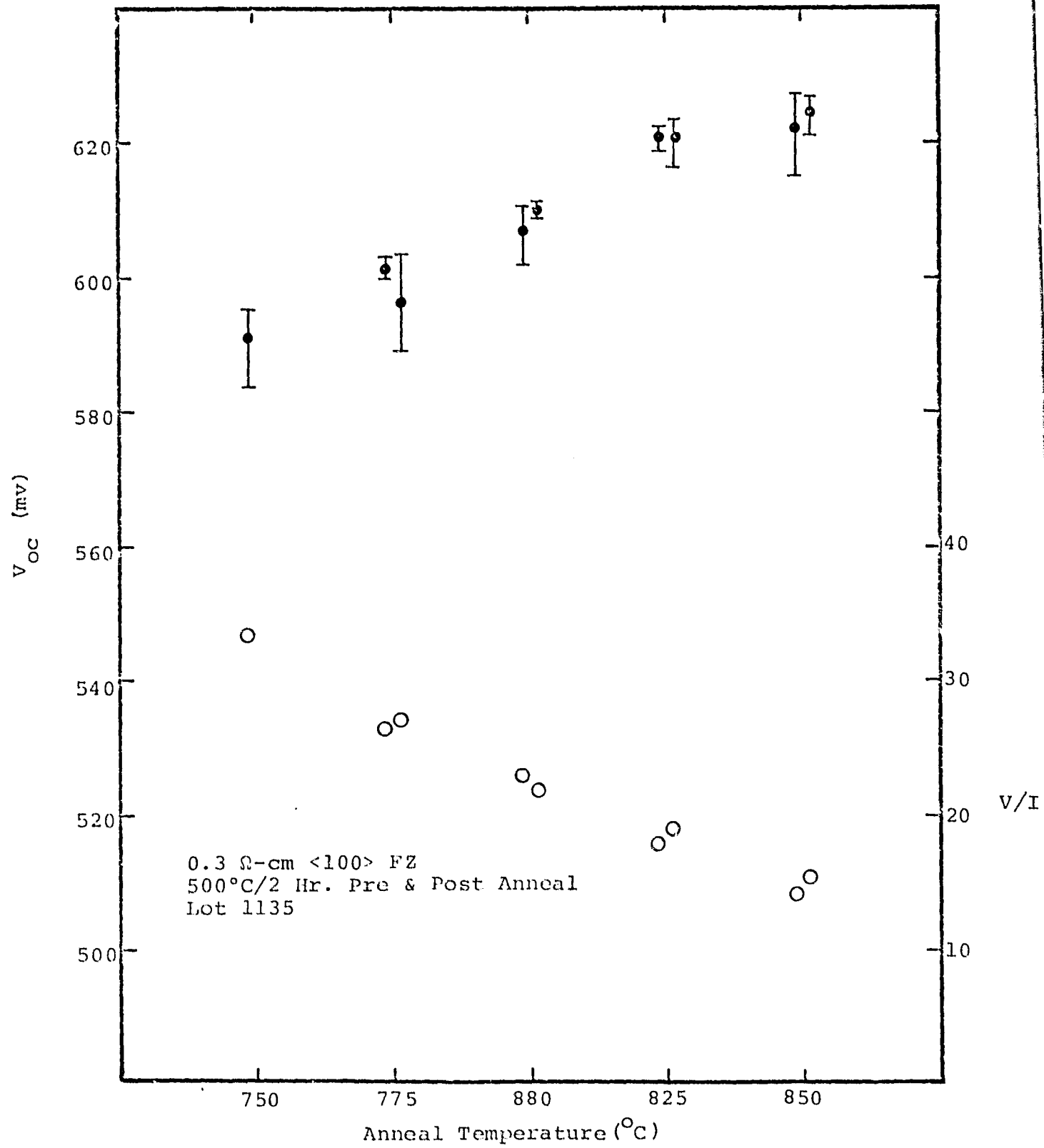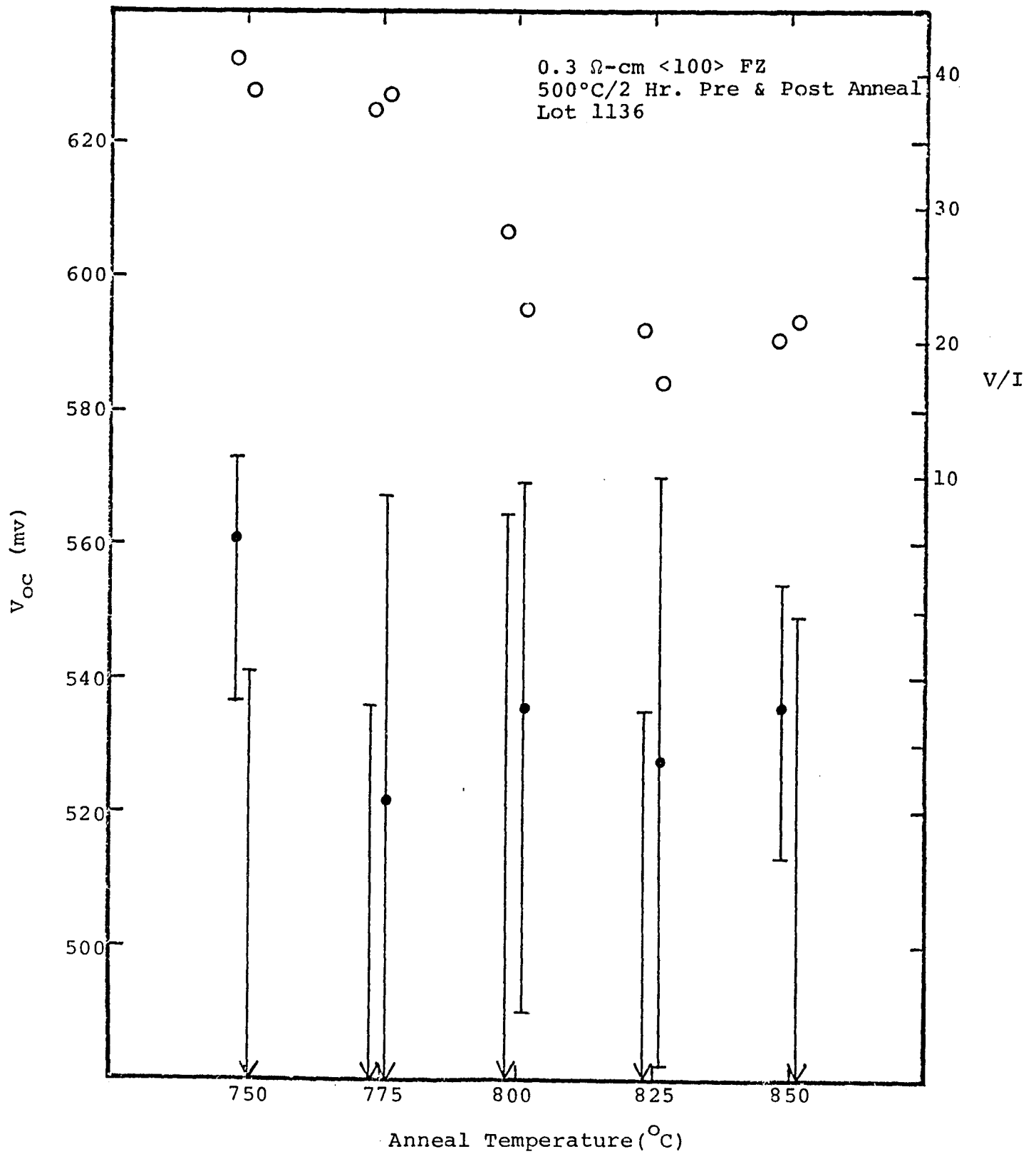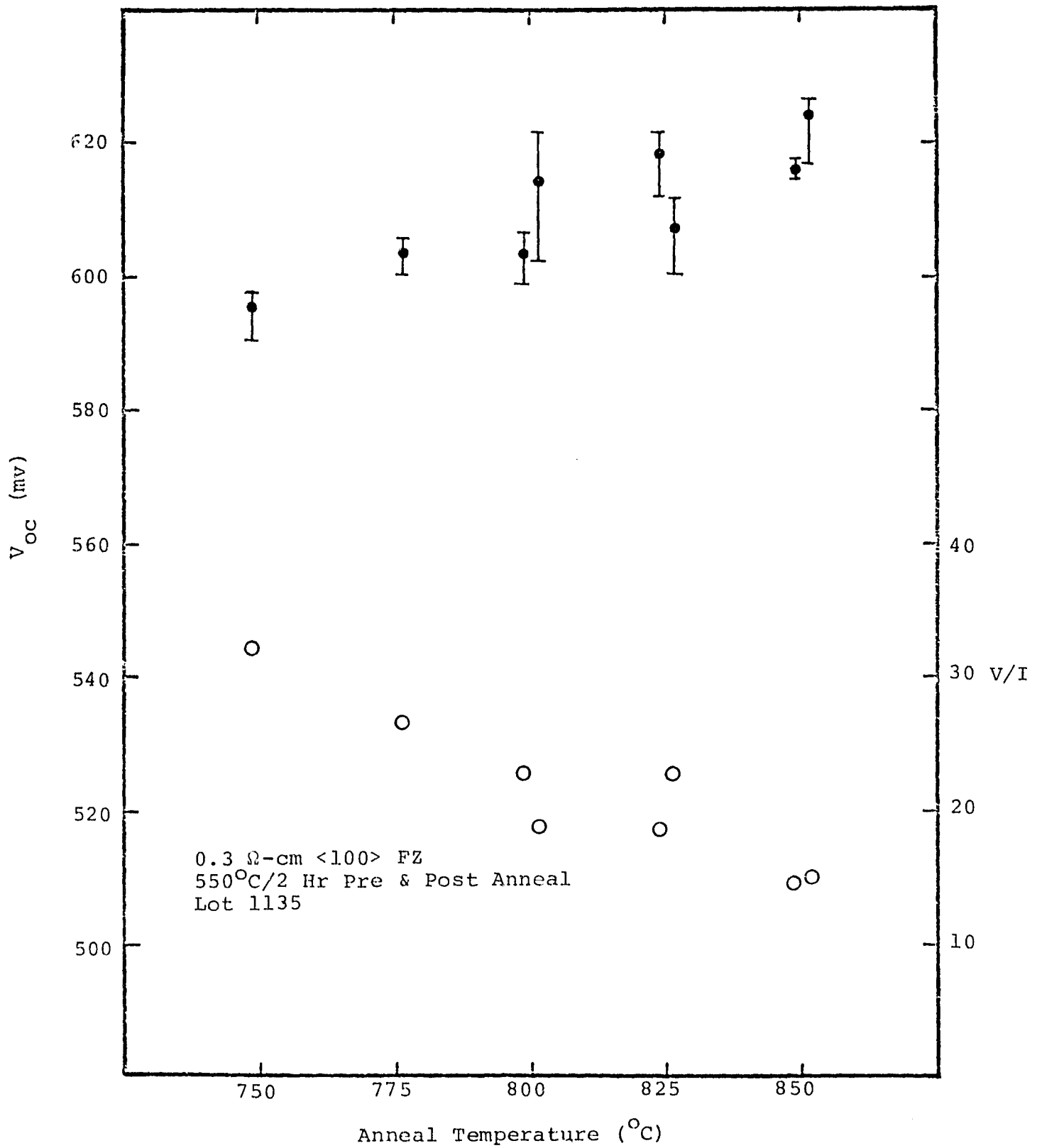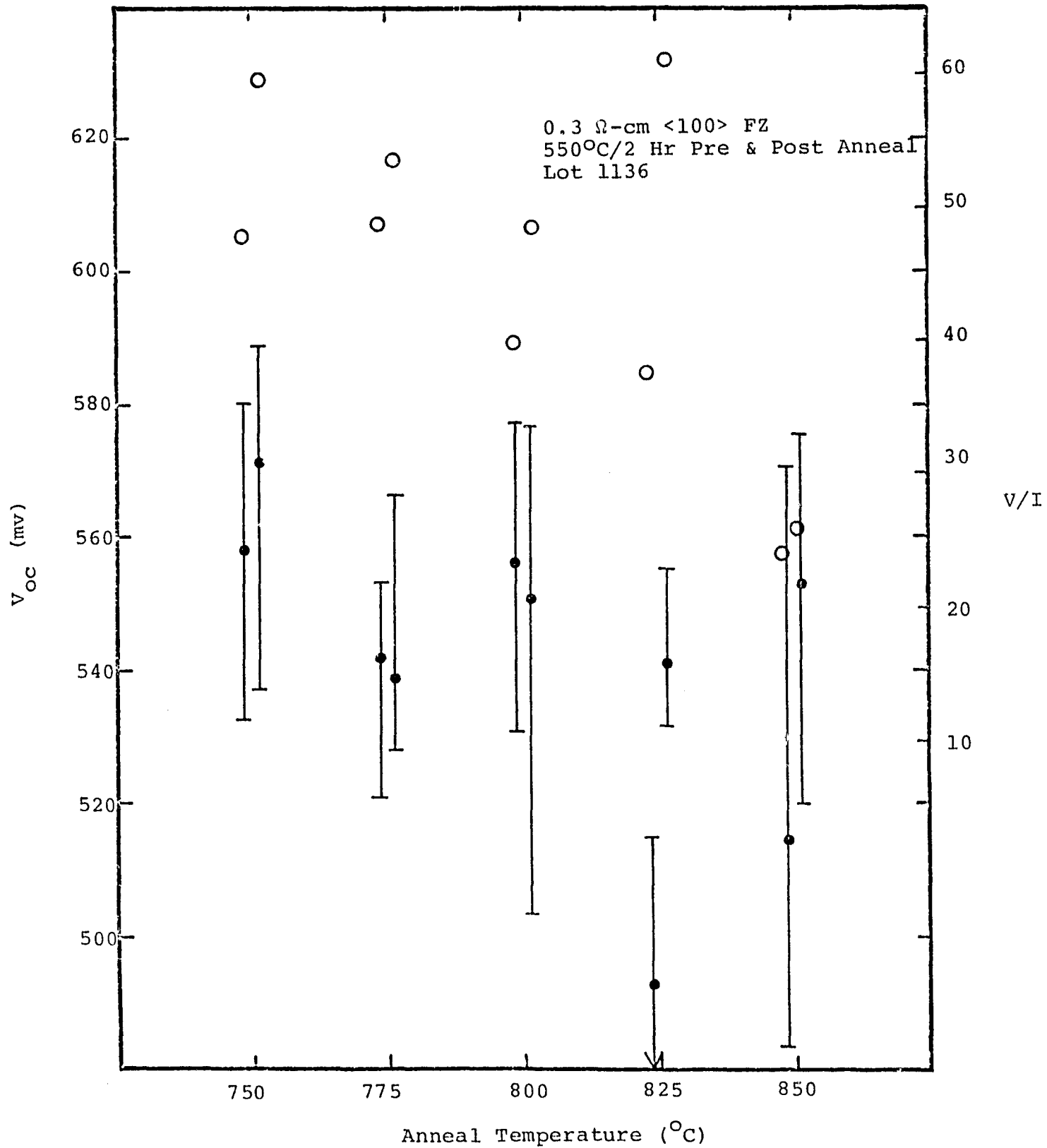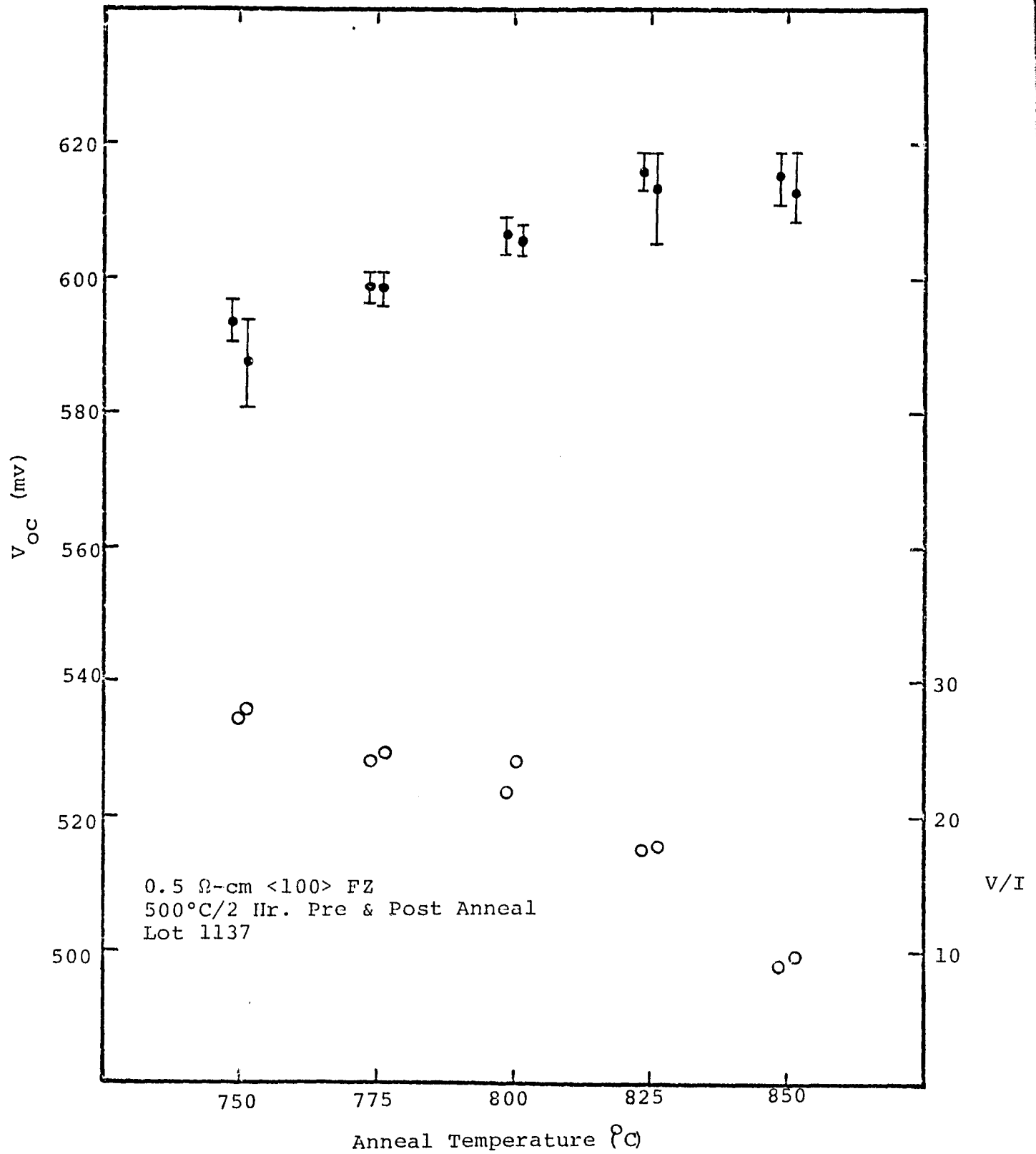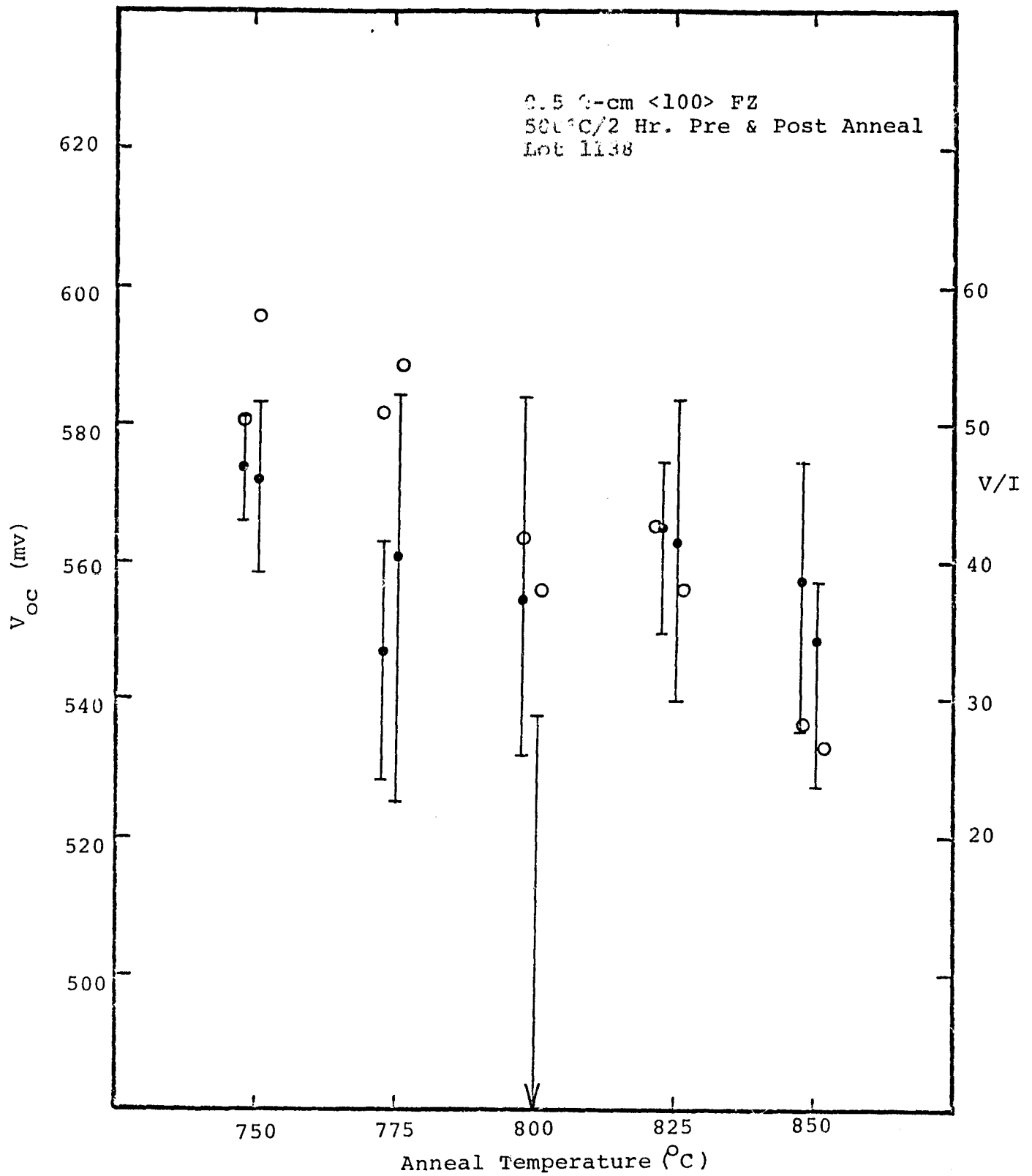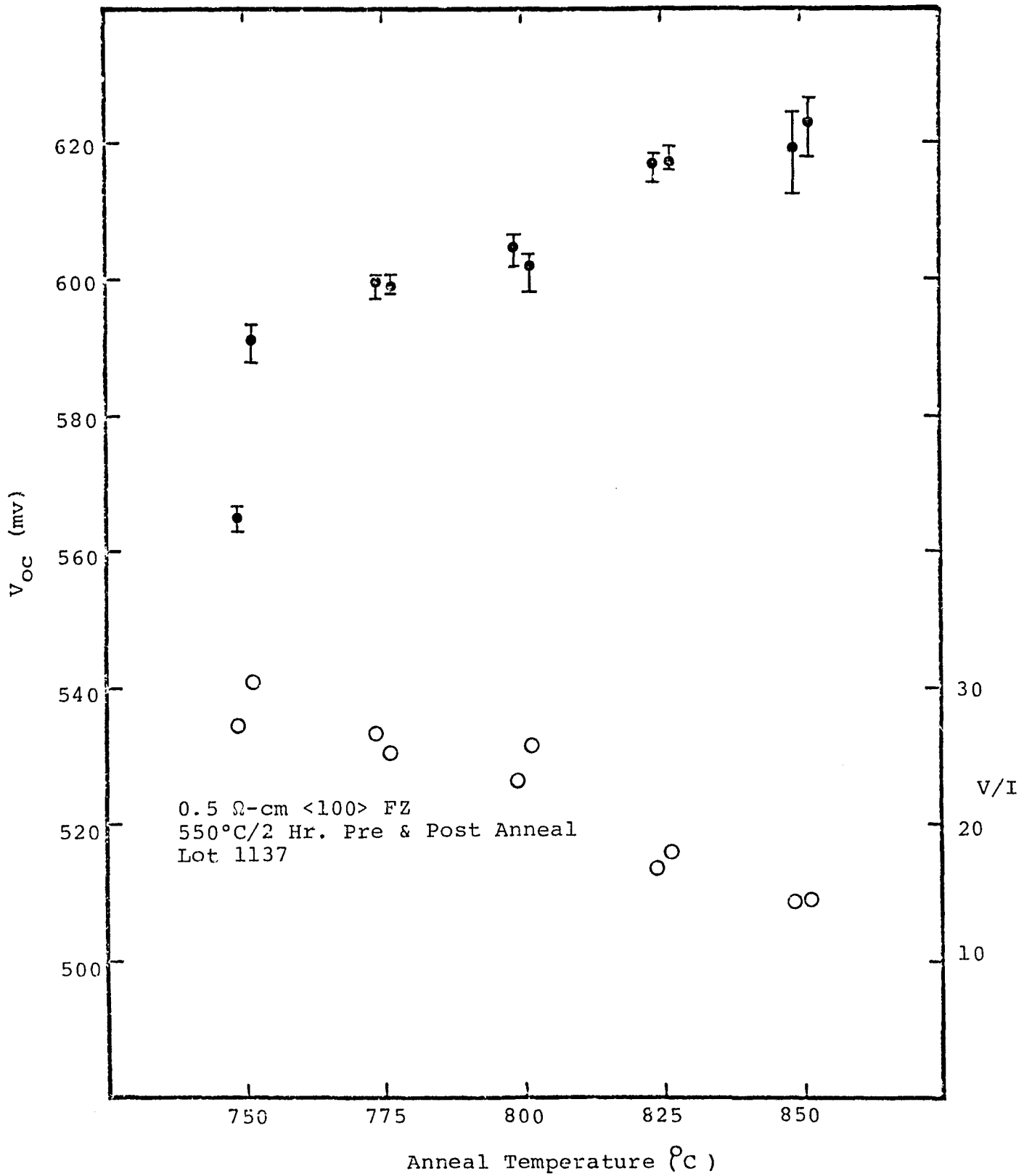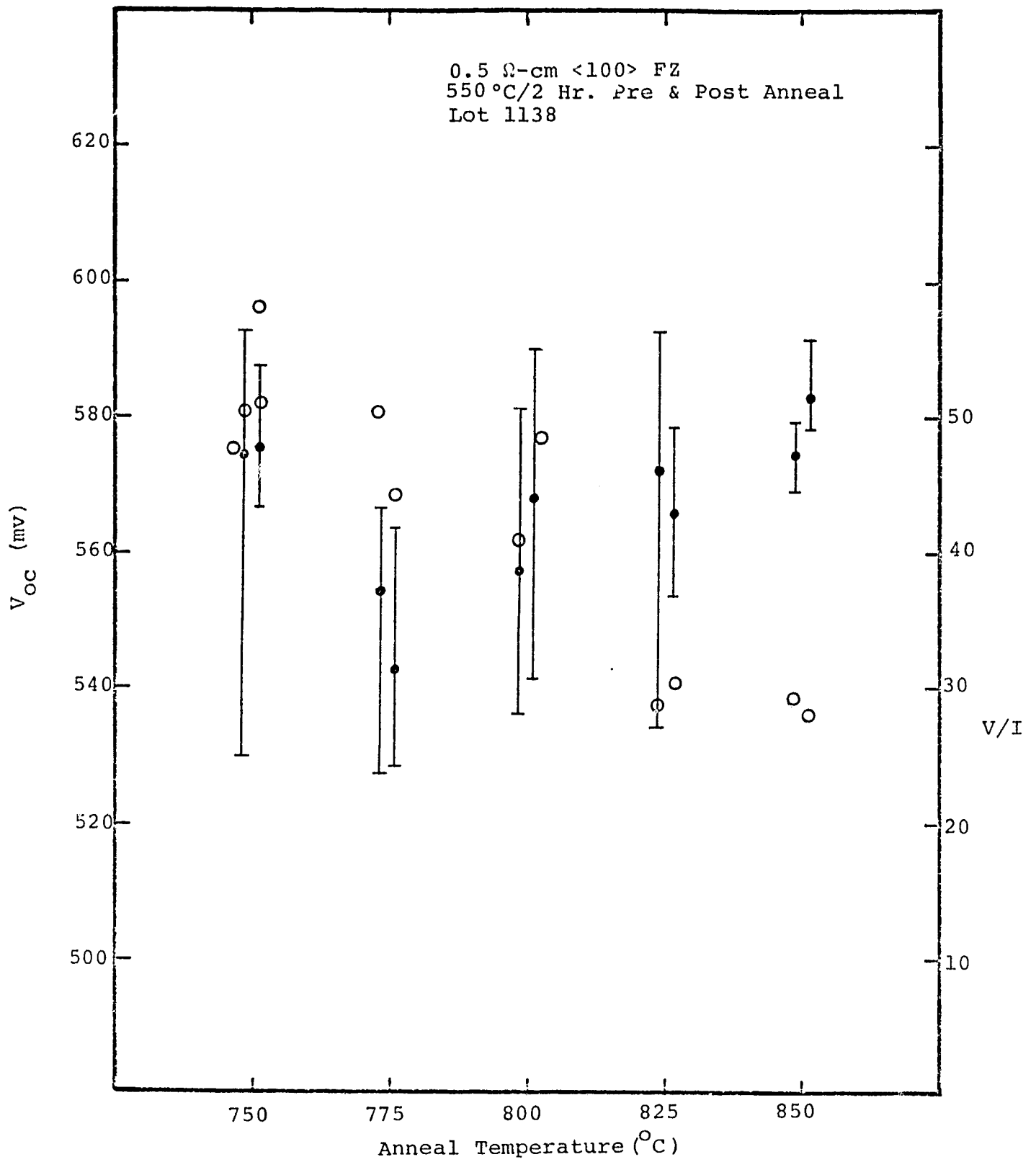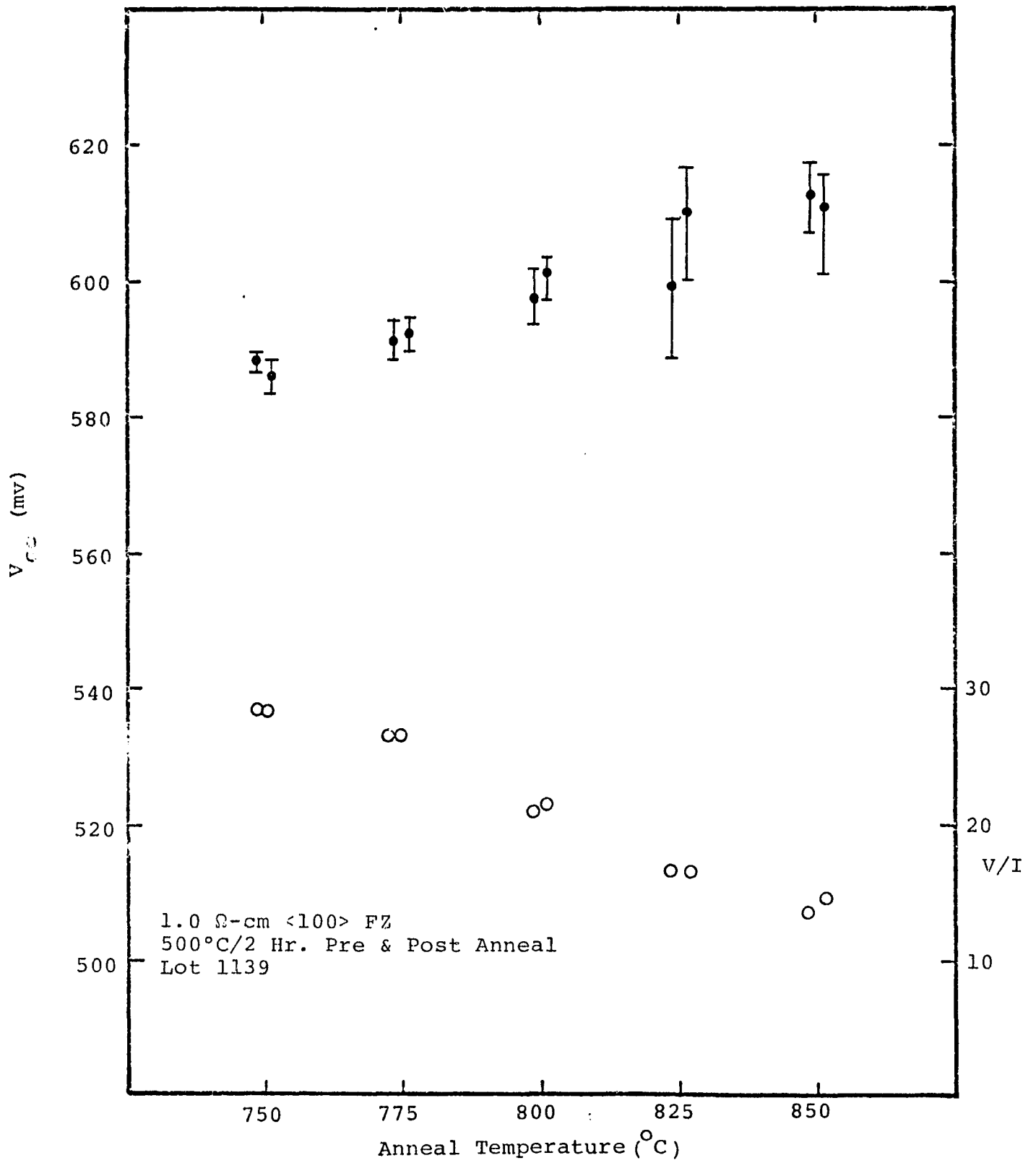0.1-ohm-cm SILICON

A-4

FIGURE A-5. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
0.3-ohm-cm SILICON

FIGURE A-6. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
0.3-ohm-cm SILICON

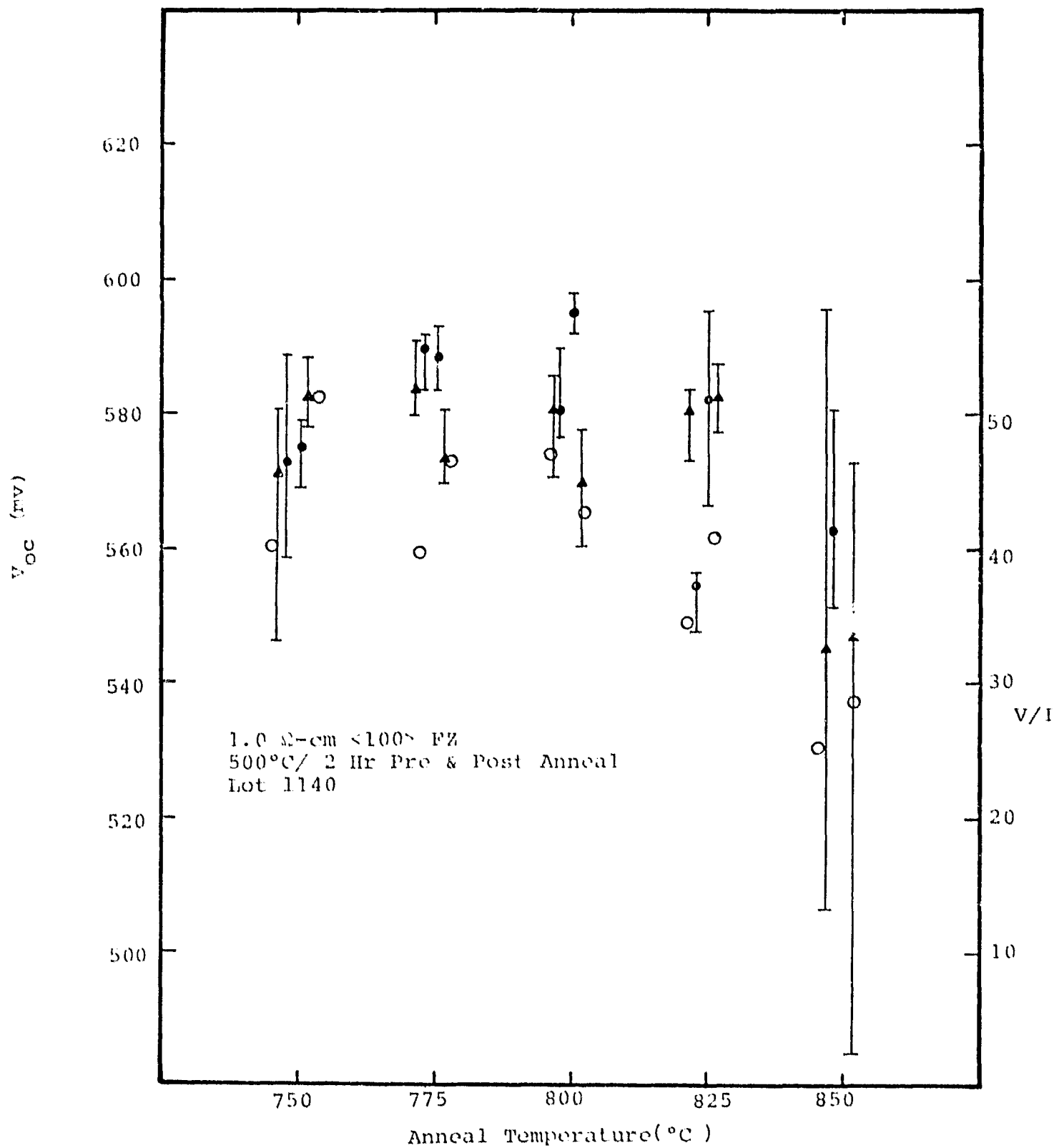FIGURE A-7. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
0.3-ohm-cm SILICON

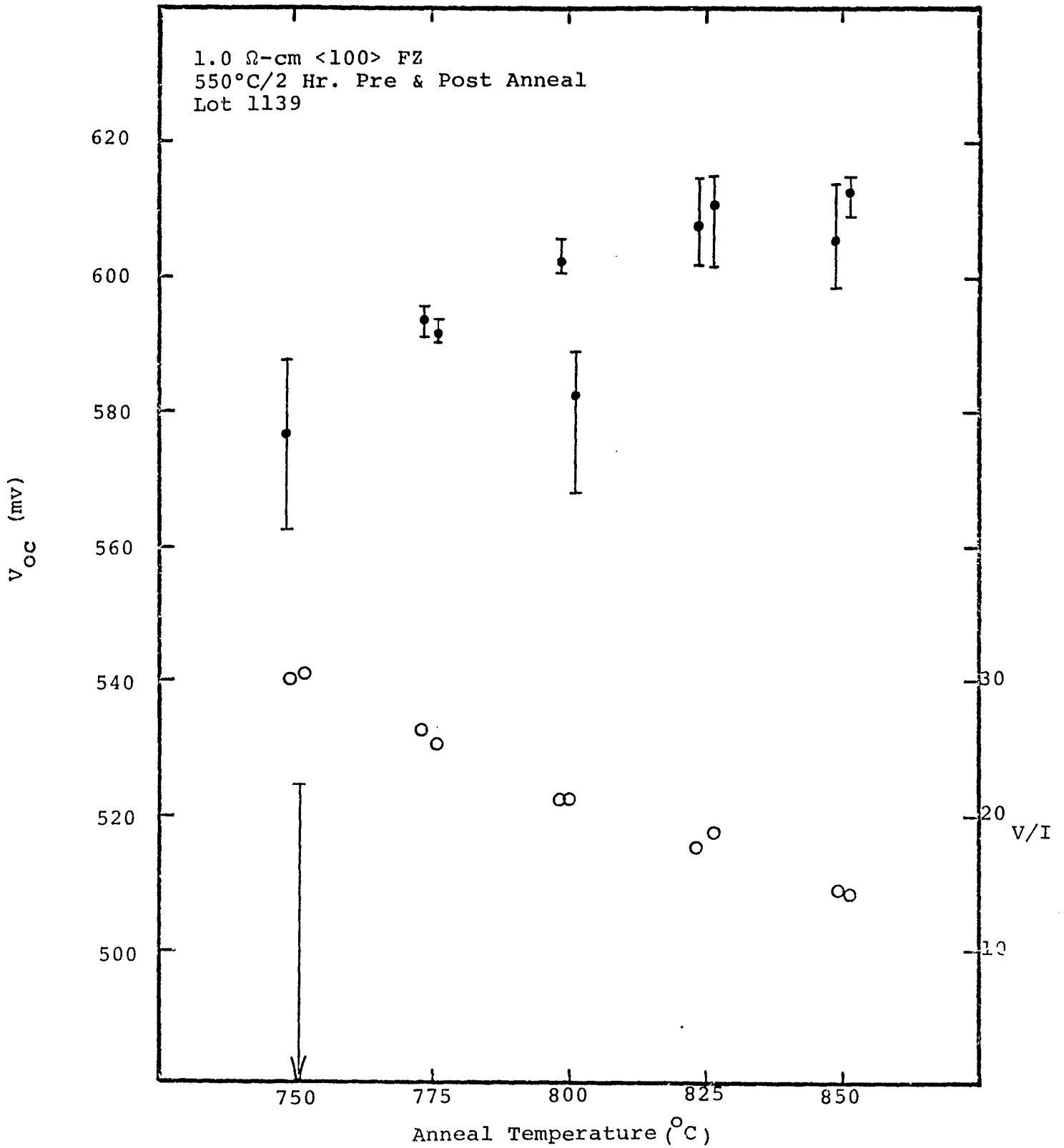FIGURE A-8. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
0.3-ohm-cm SILICON

FIGURE A-9. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
0.5-ohm-cm SILICON

A-9

FIGURE A-10. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
0.5-ohm-cm SILICON

FIGURE A-11. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
0.5-ohm-cm SILICON

A-11

FIGURE A-12. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
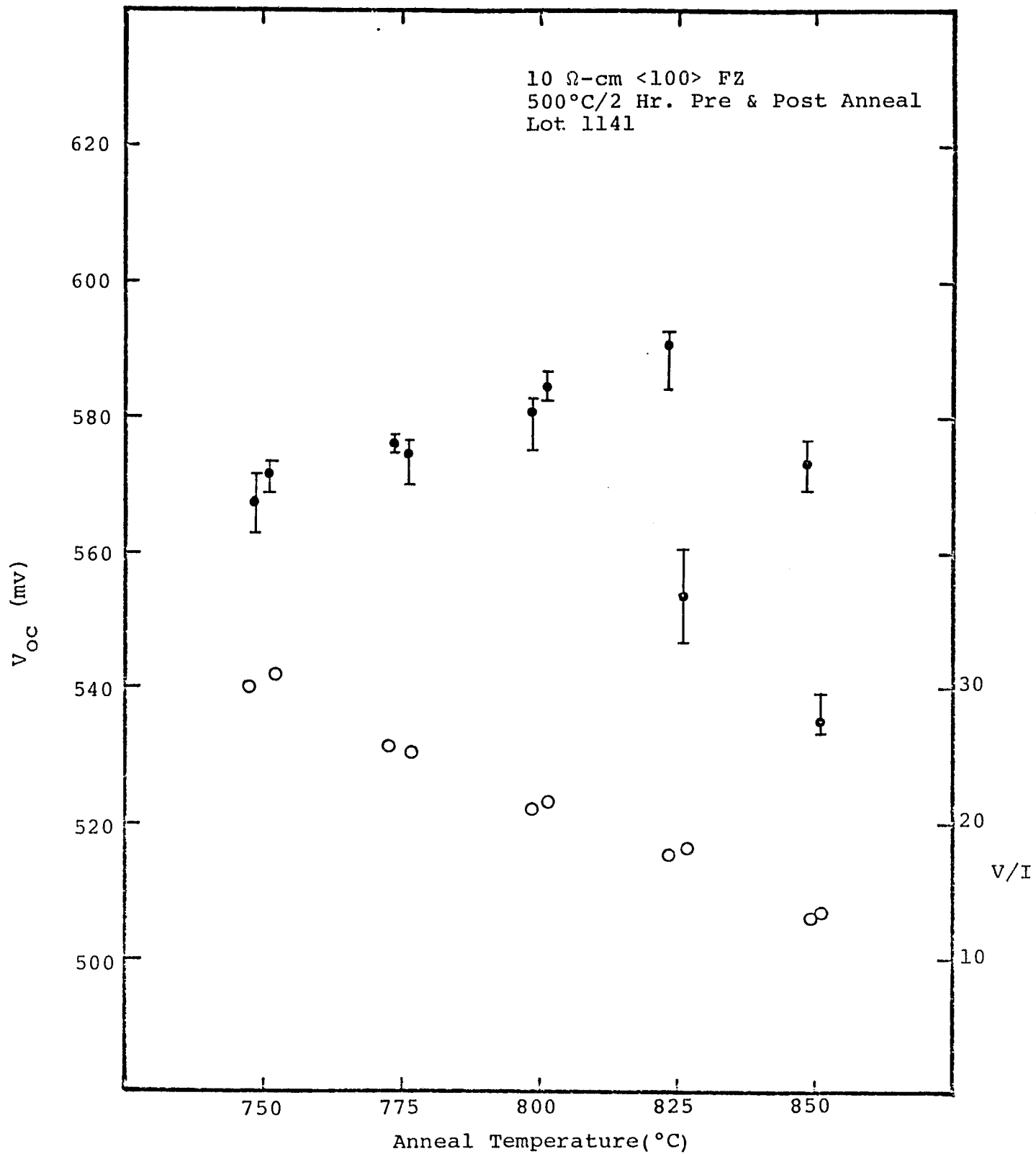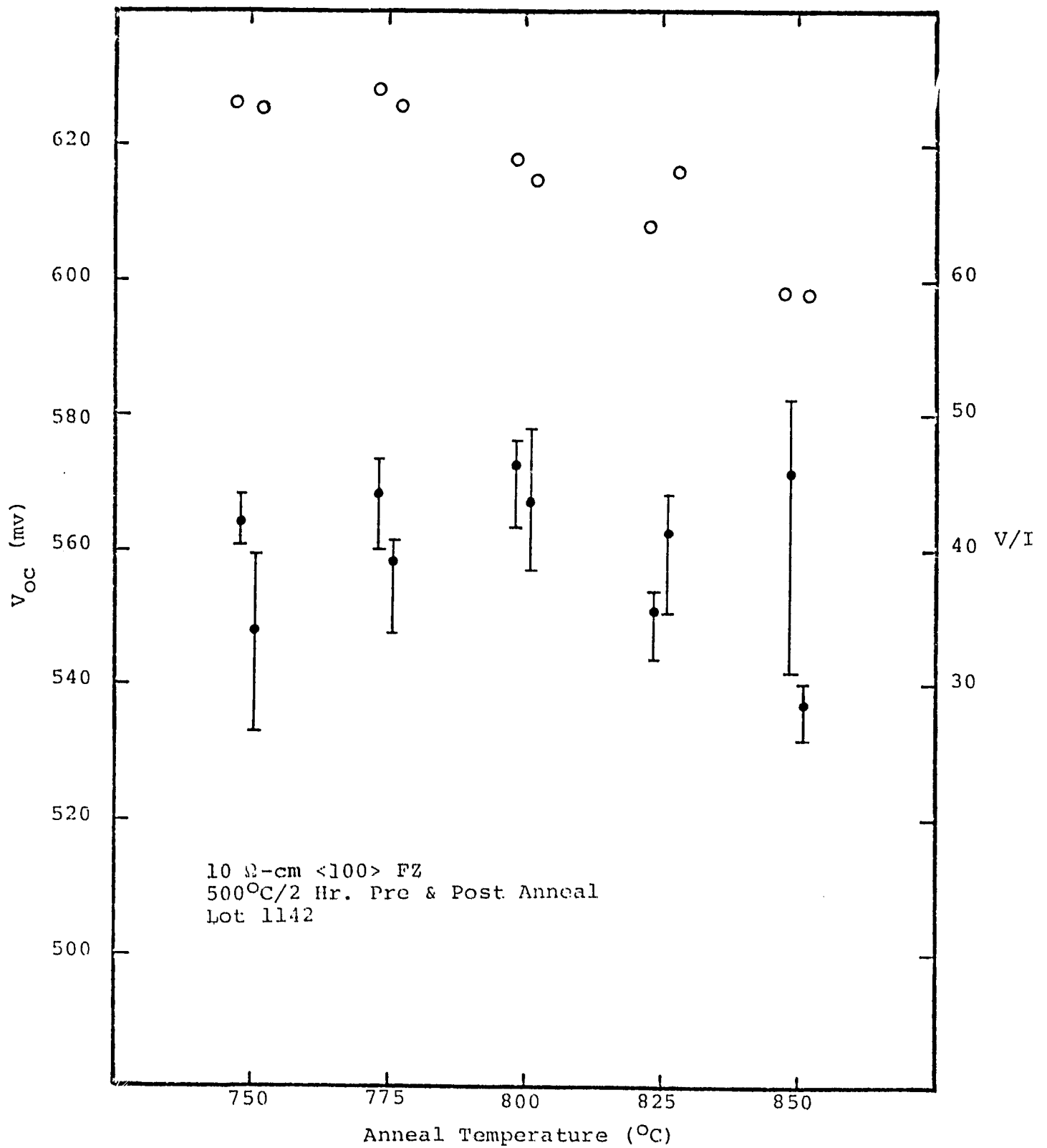0.5-ohm-cm SILICON

FIGURE A-13. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
1.0-ohm-cm SILICON

FIGURE A-14. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
1.0-ohm-cm SILICON

A-14

FIGURE A-15. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
1.0-ohm-cm SILICON

A-15

FIGURE A-16. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
1.0-ohm-cm SILICON

A-16

FIGURE A-17. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
10-ohm-cm SILICON

A-17

FIGURE A-18. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
10-ohm-cm SILICON

FIGURE A-19. ISOCHRONAL ANNEALING OF PHOSPHORUS IMPLANTED
10-ohm-cm SILICON

FIGURE A-20. ISOCHRONAL ANNEALING OF ARSENIC IMPLANTED
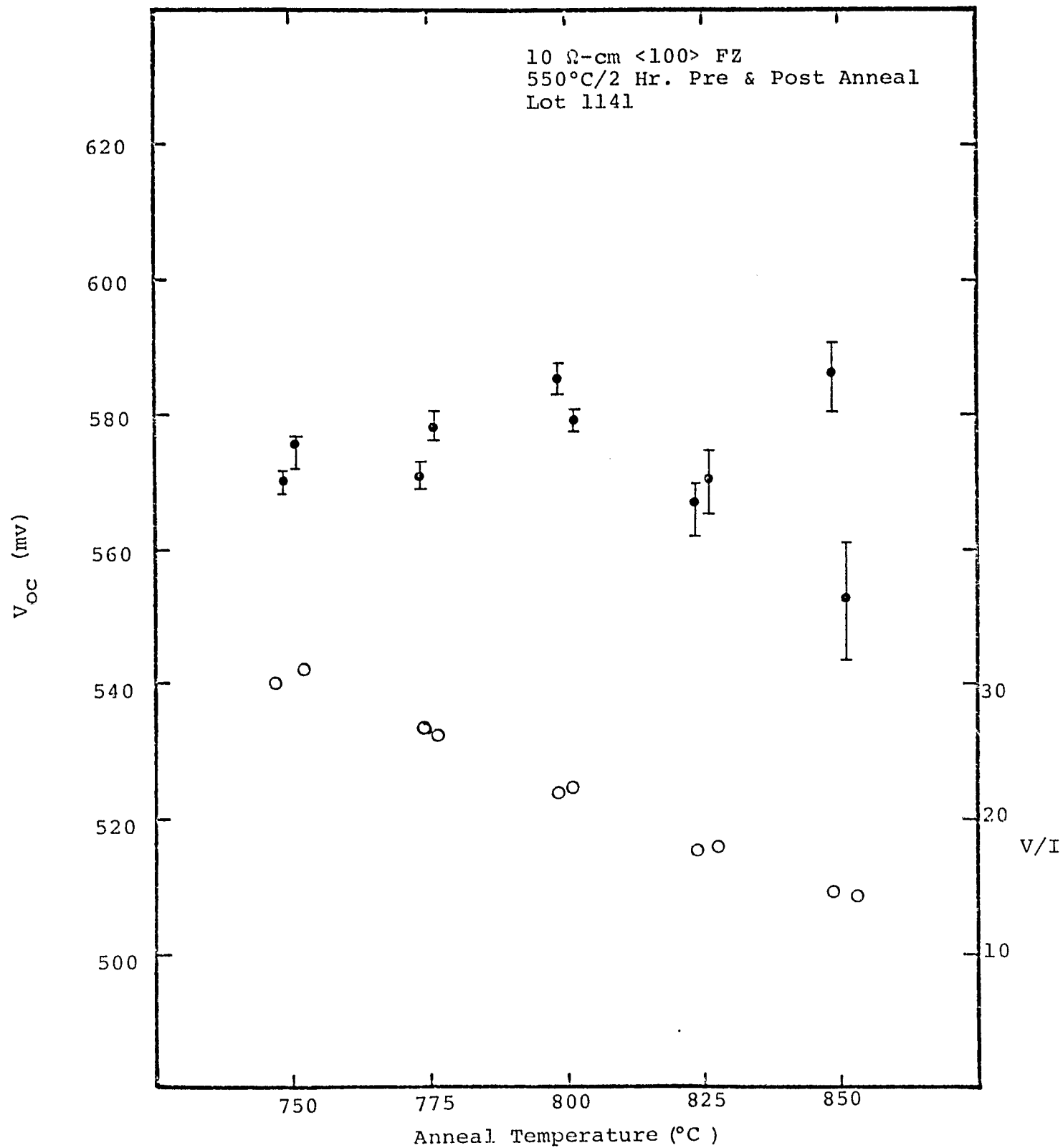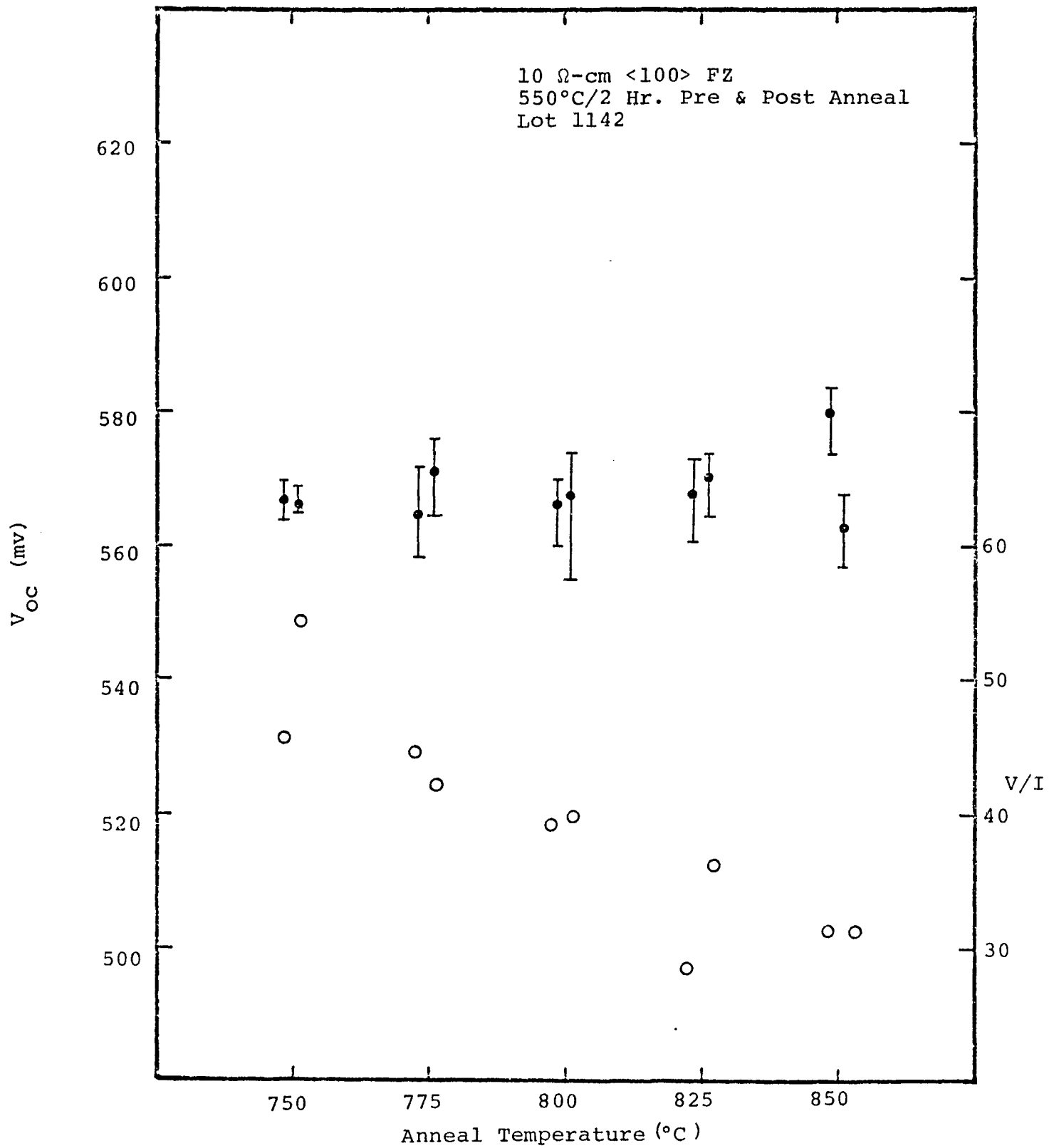10-ohm-cm SILICON