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# AUTOMATED ARRAY ASSEMBLY
# PHASE 2

Texas Instruments Report No. 03-79-58

Final Technical Progress Report
1979

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November 1979

JPL Contract No. 954881

Texas Instruments Incorporated
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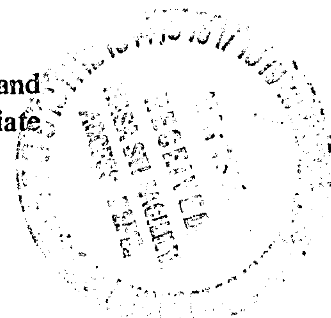

## ABSTRACT

The 1979 phase of this Automated Array Assembly, Phase 2 contract was devoted solely to the tasks of scaling up the Tandem Junction Cell (TJC) from 2 cm × 2 cm to 6.2 cm × 6.2 cm and the assembly of several modules using these large-area TJCs. The scale-up of the TJC was based on using the existing process and doing the necessary design activities to increase the cell area to an acceptably large area. The design was carried out using available device models. The design was verified and sample large-area TJCs were fabricated. Mechanical and process problems occurred causing a schedule slippage that resulted in contract expiration before enough large-area TJCs were fabricated to populate the sample Tandem Junction Modules (TJMs).

A TJM design was carried out in which the module interconnects served to augment the current collecting buses on the cell. The module was made up of a 5 × 6 TJC matrix mounted on a porcelainized steel substrate with a glass cover. The TJC matrix was series-parallel connected using copper clad Invar interconnects soldered to the TJC metallization. Sample cell matrices were assembled using dummy cells. No sample TJMs were assembled due to a shortage of large-area TJCs and contract expiration.

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# SECTION I
# INTRODUCTION

The Automated Array Assembly Task, Phase 2 of the Low-Cost Solar Array (LSA) Project is a process development task. This contract includes solar cell module process development activities in the areas of Surface Preparation, Plasma Processing, Diffusion, Cell Processing and Module Fabrication. In addition, a High-Efficiency Cell Development Activity is included. The overall goal is to advance solar cell module process technology to meet the 1986 goal of a production capacity of 500 megawatts per year at a cost of less then $500 per kilowatt. The contract activity described by this report focused on the process elements stated above and on an overall module process.

The 1978 Annual Report (DOE/JPL 954881-79-4) covered the work on process step development carried out on texture etching including the evolution of a conceptual process model for the texturing process; plasma etching; and diffusion studies that focused on doped polymer diffusion sources. Cell processing was carried out to test process steps and a simplified diode solar cell process was developed. Cell processing was also run to fabricate square cells to populate sample minimodules. Module fabrication featured the demonstration of a porcelainized steel-glass structure that should exceed the 20-year life goal of the LSA program.

Also included in the 1978 Annual Report and in a separate Final Report (DOE/JPL 954881-79-5) was a related set of studies on high-efficiency cell development carried out on the Texas Instruments developed Tandem Junction Cell (TJC) and a modification of the TJC called the Front Surface Field (FSF) cell. These cells feature planar backside contacts with no metallization of the frontside. Cell efficiencies in excess of 16% at AM1 have been attained with only modest fill factors. Photo-generated current densities as high as 44 mA/cm$^2$ at AM0 have been attained. A transistor-like model has been proposed that fits the cell performance and provides a guideline for future improvements in cell performance.

In this Final Report, the 1979 work leading toward a Tandem Junction Module (TJM) is covered. A large-area, 6.2 cm X 6.2 cm, TJC was designed, the TJC process was verified and the design was verified. Sample large-area TJCs were fabricated but due to mechanical and process problems, enough cells to populate modules could not be fabricated within the limitations of the schedule and budget. The module fabrication process was carried through the stages of defining the cell module tradeoffs, fabricating porcelainized steel substrates, fabrication of clad metal interconnects and assembly of a cell matrix using dummy TJCs. Since TJC fabrication was limited to a few sample cells, no TJMs were completed. TJM performance was calculated from performance data on sample TJCs. No cell development or process development effort was included in the 1979 portion of this contract.

## SECTION II
## TECHNICAL DISCUSSION

The technical work on this program was divided into two major areas, Large-Area TJC and Tandem Junction Module (TJM). The large-area TJC effort consisted of freezing the development of the TJC as of December 1978 and scaling up the cell size from 2 cm × 2 cm to a large-area TJC, 6.2 cm × 6.2 cm. The TJM effort consisted of adapting the porcelainized steel-glass module developed earlier to accept a TJC matrix.

A discussion of the activities in each area follows.

### A. LARGE-AREA TJC

#### 1. Cell Design

##### a. INTRODUCTION

A theoretical model has been developed which explains operation of the TJC in terms of transistor action.[1,2] This model has been applied to calculate cell performance in terms of structure.[3] Relationships for series resistance losses have also been developed.[4,5] The above models are reviewed here and have been extended to provide a quantitative design theory for the TJC.

These principles were applied to the design of a TJC structure to meet the requirements of this program. The precise relationships presented here were not available when the design was carried out; however, the principles were known and similar equations were used.

##### b. TANDEM JUNCTION CELL – STRUCTURE AND MODEL

As illustrated in the cross section of Figure 1, the TJC[6] consists of a P-type base with a thin N+ region at the front surface and interdigitated P+ and N+ regions at the back. The front N+ region is uncontacted. Current is collected at the N+ and P+ contacts at the back of the cell. The front surface is texturized. Refraction of incident light and reflection at the back surface give a long optical path so that a high percentage of the light is absorbed, even in very thin cells.

Benefits of using contacts on only the back surface include:

Elimination of metal shadowing
Potential of low series resistance
Convenience of interconnect

Additionally, high short-circuit current and open-circuit voltage have been achieved in very thin cells. An inherent limitation of back contact cells is that good performance is dependent upon high lifetime.



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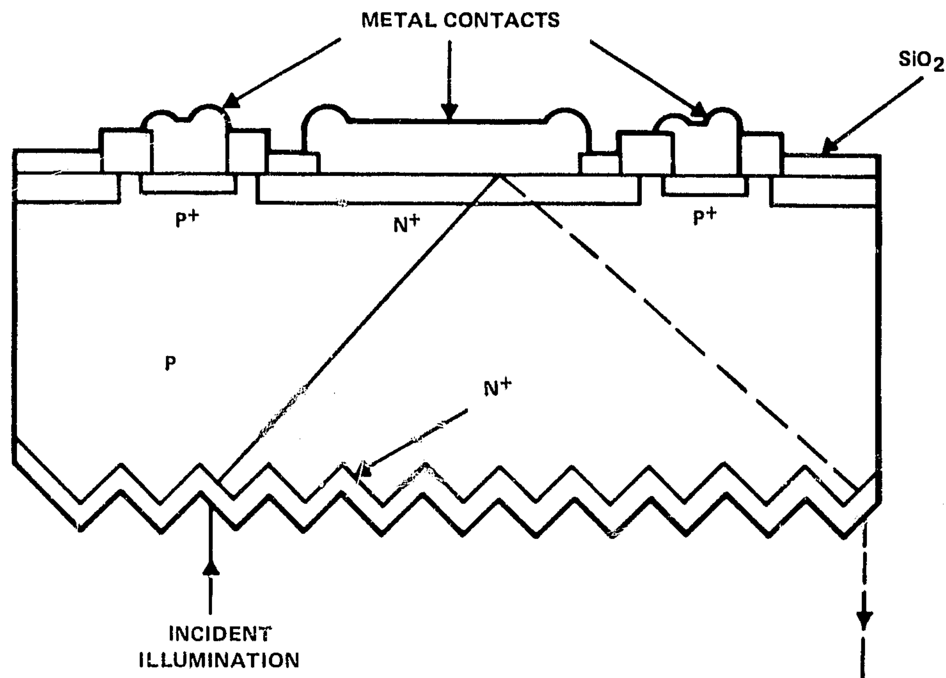


**Figure 1. Sketch of Tandem Junction Solar Cell**

Operation of the TJC is explained by the basic transistor model[1,2] shown in Figure 2. In the cross section of Figure 2(a), the front N+ region corresponds to the emitter, the P-region to the base, and the back N+ region to the collector. The current sources $I_{\lambda E}$ and $I_{\lambda C}$ in Figure 2(b) result from carrier generation in the vicinity of emitter-base and collector-base junctions, respectively.

Generation and flow of carriers is illustrated in Figure 3. When carriers are generated in the emitter, holes diffuse to the base region. For short-circuit conditions, the holes move by fields through the base to the P+ contact. To maintain charge neutrality, a potential is built up across the junction such that electrons are injected from emitter to base in approximately equal quantities. Carrier generation in the base also contributes to the emitter-base junction potential; a boundary condition for base-generated carriers is that net flow of electrons across the emitter-base junction is zero (assuming emitter injection efficiency is unity, as discussed in a later section).

From the equivalent circuit of Figure 2(b), the short-circuit current is

$$I_{SC} = \alpha_N I_{\lambda E} + I_{\lambda C} \tag{1}$$

where $\alpha_N$ is the forward (normal) current transfer ratio. Most of the current is generated very close to the surface. As a first-order approximation, the total photon-generated current $I_\lambda$ is at the emitter junction so that

$$I_{SC} \cong \alpha_N I_\lambda . \tag{2}$$

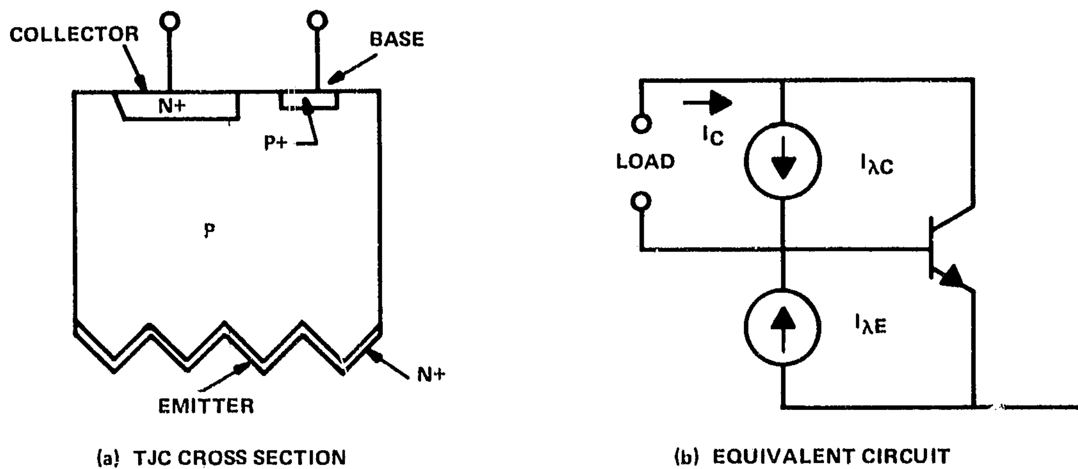


Figure 2. Representation of TJC as Transistor Structure

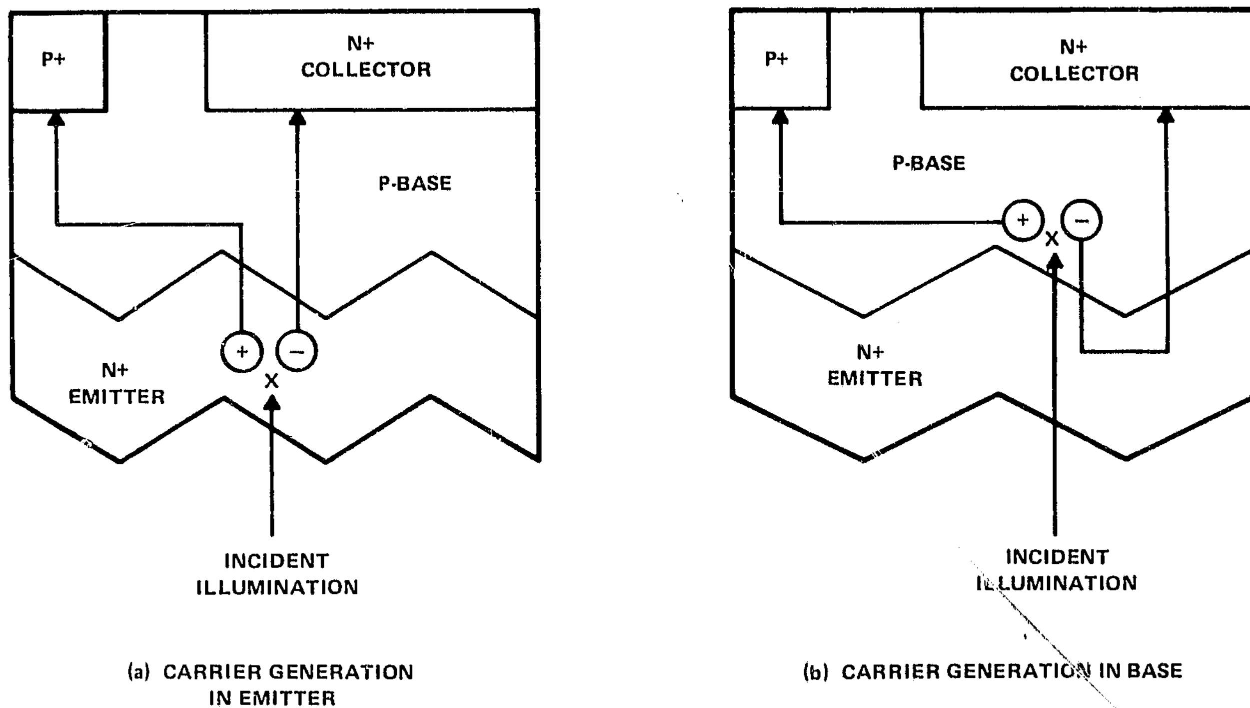


Figure 3. Schematic Representation of Carrier Flow in Tandem Junction Cell

Open-circuit voltage determined from the Ebers-Moll relationship is

$$V_{OC} = \frac{kT}{q} \ln \frac{I_{SC}}{I_{CS}\,(1 - \alpha_N\,\alpha_I)} \tag{3}$$

where $I_{CS}$ is the saturation current of the collector-base junction. In principle, $V_{OC}$ can be made quite high if forward and inverse current transfer ratios, $\alpha_N$ and $\alpha_I$, approach unity.

High measured values of short-circuit current, open-circuit voltage, and good response at short wavelength are consistent with the transistor model.

The transistor model provides a familiar frame of reference[3] for optimizing the TJC structure and estimating performance. Short-circuit current, in Equation (2), is related to physical parameters of the cell by expressing current transfer ratio as

$$\alpha_N = \gamma_E \frac{1}{\cosh \frac{W}{L}} \tag{4}$$

where W is base width, L is diffusion length for minority carriers in the base, and $\gamma_E$ is injection efficiency for the emitter-base junction. Values of $\gamma_E$ near unity can be obtained using heavily doped emitters.

From Equations (2) and (4), short-circuit current is approximated as

$$I_{SC} = I_\lambda \frac{1}{\cosh \frac{W}{L}} \tag{5}$$

## c. DESIGN RELATIONSHIPS

### *1. Short-Circuit Current Density*

Short-circuit current and open-circuit voltage for the TJC follow from the transistor model. Short-circuit current is approximated from Equation (5).

A more accurate calculation (5) has been carried out using the carrier continuity equation

$$qD\frac{d^2N}{dX^2} - \frac{q}{\tau} N + G(X) = 0 \tag{6}$$

The carrier generation function, G(X), has been adapted to the TJC by including the effects of refraction and reflection. The continuity equation is solved by a computer routine to obtain short-circuit current due to carriers generated in the base. Boundary conditions are

$$N'(X_E) = 0 \qquad (\text{assuming } \gamma_E = 1.0)$$

$$N(X_E + W) = 0$$

where $X_E$ is emitter junction depth and W is base width. Current due to generation in the emitter is obtained from the transistor model.

Short-circuit current density is plotted in Figure 4 as a function of base width for several constant values of diffusion length. The solid lines are results from the computer solution; the transistor approximation from Equation (5) is shown by the dotted lines. For small values of W/L the two are essentially coincident. The transistor model deviates for large values of W/L but still gives a useful engineering estimate. Measured values for several cells are shown in Figure 4. These follow predicted trends and are within limits of lifetime measurement.

Dependence of open-circuit voltage on cell parameters can be calculated from Equation (3), using values of short-circuit current density obtained from Figure 4 with the relationship

$$I_{CS} = \frac{A\,qD\,n_i^2}{W\,N_A} \tag{7}$$

where

$A$ = area

$q$ = electronic charge

$D$ = diffusion coefficient for minority carriers

$n_i$ = intrinsic carrier concentration

$W$ = base width

$N_A$ = acceptor doping concentration

It is assumed that emitter and collector injection efficiencies are unity so that

$$\alpha_N \approx \alpha_I \approx \frac{I}{\cosh \frac{W}{L}} \tag{8}$$

where

$$L = \sqrt{D\tau}$$

and $\tau$ is minority carrier lifetime.

### 2. *Open Circuit Voltage*

Open-circuit voltage calculated from this model is plotted in Figure 5 as a function of base lifetime, $\tau$, for constant values of base resistivity (related to $N_A$). Values of resistivity below 1.0 ohm-cm were not considered here. Injection efficiency for the corresponding base doping concentration could become significantly less than unity for low resistivity bases so that benefits of the TJC are not realized.

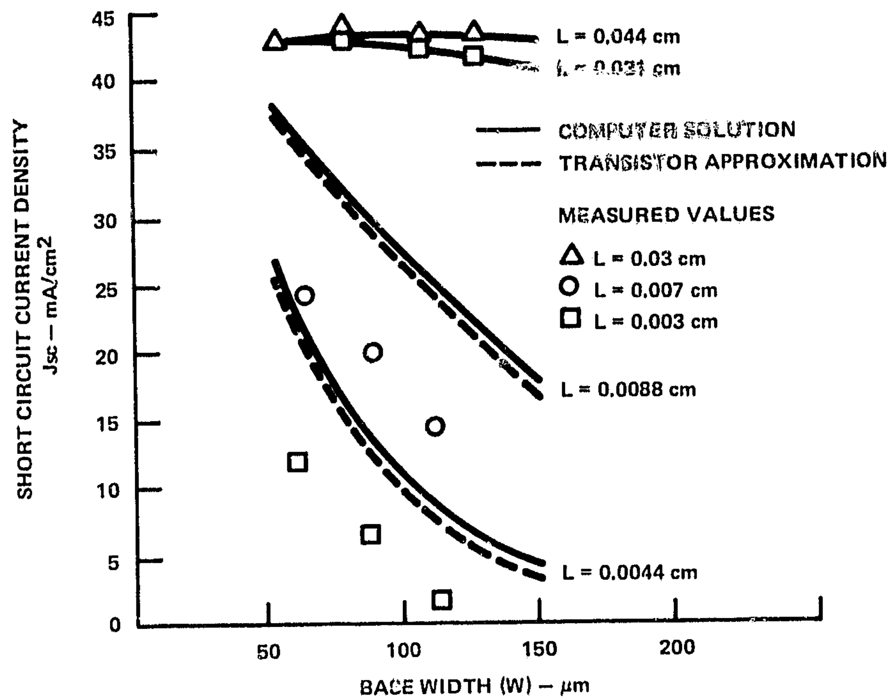


**Figure 4. Short-Circuit Current Density (AMO) for the TJC as a Function of Base Width for Constant Values of Minority Carrier Diffusion Length**

## 3. *Series Resistance Losses*

Resistivity power losses from a cell or cell segment are evaluated using fractional loss components.[4,5] The fractional loss component due to a series resistance effect is defined as

$$F = \frac{P_R}{P_{MA}}$$

where $P_R$ is the resistive loss component and $P_{MA}$ is the maximum power available.

Current paths for photon-generated hole electron pairs are illustrated in Figure 6. Resistive losses are due to the majority carrier components, i.e., holes in the P-base region and electrons in the N+ collector region. Hole current flows transversely through the base to the P+ contact; electron current flows across the N+ collector region to the metal contact.

The fractional loss $F_B$ due to the base current is approximately

$$F_B = \frac{K_I^2 J_{SC} \rho_S S^2}{12 V_{OC} CF} \tag{9}$$

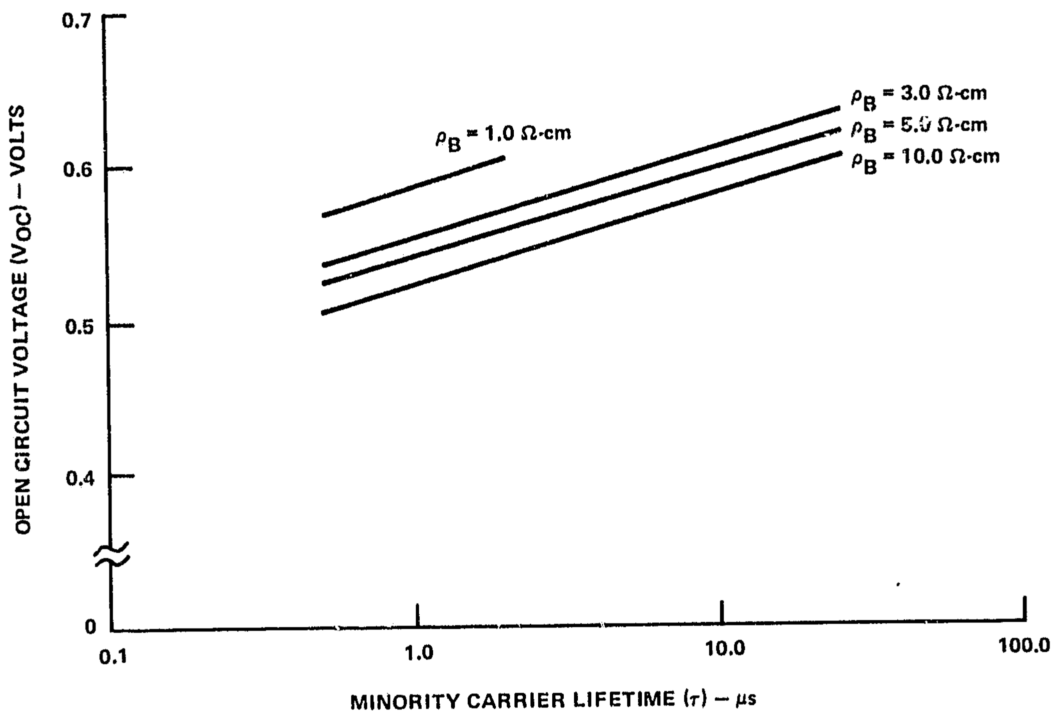


Figure 5. Calculated Values of Open-Circuit Voltage of TJC as a Function of Minority Lifetime in the Base with Base Resistivity as a Parameter

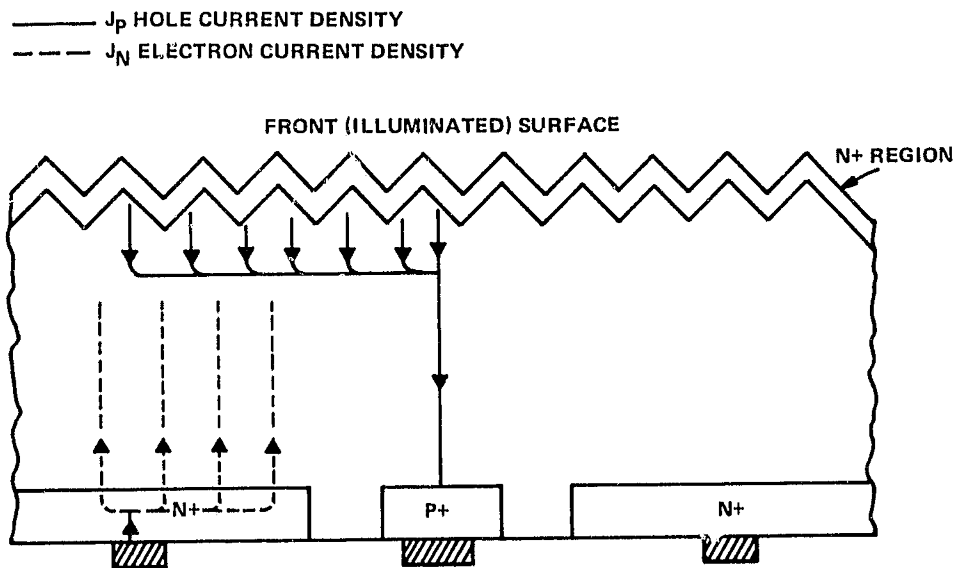


Figure 6. Current Paths in TJC

where S is spacing between adjacent P+ fingers, $\rho_S$ is sheet resistance of the base, $J_{SC}$ is short-circuit current density. This expression is based on ideal junction characteristics for which the curve factor, CF and

$$K_I = \frac{J_M}{J_{SC}}$$

are uniquely determined by $V_{OC}$. (In the above expression, $J_M$ is current density at the maximum power point.) For a wide range of $V_{OC}$

$$\frac{K_I^2}{CF} \approx 1.1$$

For a tandem junction cell, the base sheet resistance is

$$\rho_S = \frac{\rho_B}{W}$$

where $\rho_B$ is base resistivity and W is base width.

The fractional loss $F_N$ due to the $N^+$ resistance is approximately

$$F_N = \frac{K_I^2 J_{SC} \rho_N S^2}{12 V_{OC} CF} \tag{10}$$

where $\rho_N$ is the sheet resistance of the $N^+$ region.

For metal contact fingers of constant width, T, length, L, and metal sheet resistance, $\rho_M$, the resistive loss factor is approximately

$$F_M = \frac{K_I^2 J_{SC} \rho_M L^2 S}{3 V_{OC} CF\, T} \tag{11}$$

The resistive loss factor for contact resistance is

$$F_C = \frac{K_I^2 J_{SC} \rho_C S}{V_{OC} CF\, T_C} \tag{12}$$

where $\rho_C$ is the specific contact resistance and $T_C$ is the width of the contact.

The total resistive loss is

$$F_T = F_B + F_N + F_{M(P+)} + F_{M(N+)} + F_{C(P+)} + F_{C(N+)} \tag{13}$$

where the loss factors are as defined above. Metal finger losses $F_{M(P+)}$ and $F_{M(N+)}$ are for the $P^+$ and $N^+$ fingers respectively. $F_{C(P+)}$ and $F_{C(N+)}$ are contact resistances for $P^+$ and $N^+$ contacts.

### 4. *Conversion Efficiency*

The models described above were used to calculate cell parameters $J_{SC}$, $V_{OC}$ and $F_B$ and conversion efficiency (at AM0)

$$\eta = \frac{J_{SC}\, V_{OC}\, CF\, F_T}{0.135\ W/cm^2} \qquad (14)$$

for the Tandem Junction Cell. Physical parameters used for this calculation are

$$W = 0.005\ cm$$

$$S = 0.08\ cm$$

Cell parameters were calculated for base resistivity values of 1.0, 3.0, 6.0 and 10 ohm-cm and values of lifetime from 0.5 to 25.0 $\mu$s. Conversion efficiency for the TJC is plotted in Figure 7 as a function of minority carrier lifetime with base resistivity as a parameter.

## d. RATIONALE

There are additional loss components, less clearly defined, which affect the open-circuit voltage, $V_{OC}$, and the short-circuit current density, $J_{SC}$, in Equation (14). Quantitative relationships are not available; however, these factors affect conversion efficiency and provide design guidelines, as discussed below.

1) Surface recombination in the P-area (fingers and bond pad) contributes to dark current and is a sink for photon-generated current. This loss is reduced by use of a boron implant; however, the P-area should be as small as possible.
2) The $P^+$ contacts are an area of infinite surface recombination velocity. This loss is reduced by increasing the active P-impurity concentration in the $P^+$-area (e.g., high temperature aluminum alloy) and by using the smallest area compatible with contact resistance.
3) Metal contacts to the $N^+$-area are regions of infinite surface recombination velocity and very low reflection. These contact areas should be minimized.

A design was carried out based on the design relationship considerations described above with several additional constraints:

1) Dimensions are a 6.2 × 6.2 cm truncated square
2) One each $N^+$ and $P^+$ bond pad on opposite edges of the cell
3) Minimum widths or spacings on the cell are 26 $\mu$m
4) Minimum spacing between adjacent metal fingers is 250 $\mu$m.

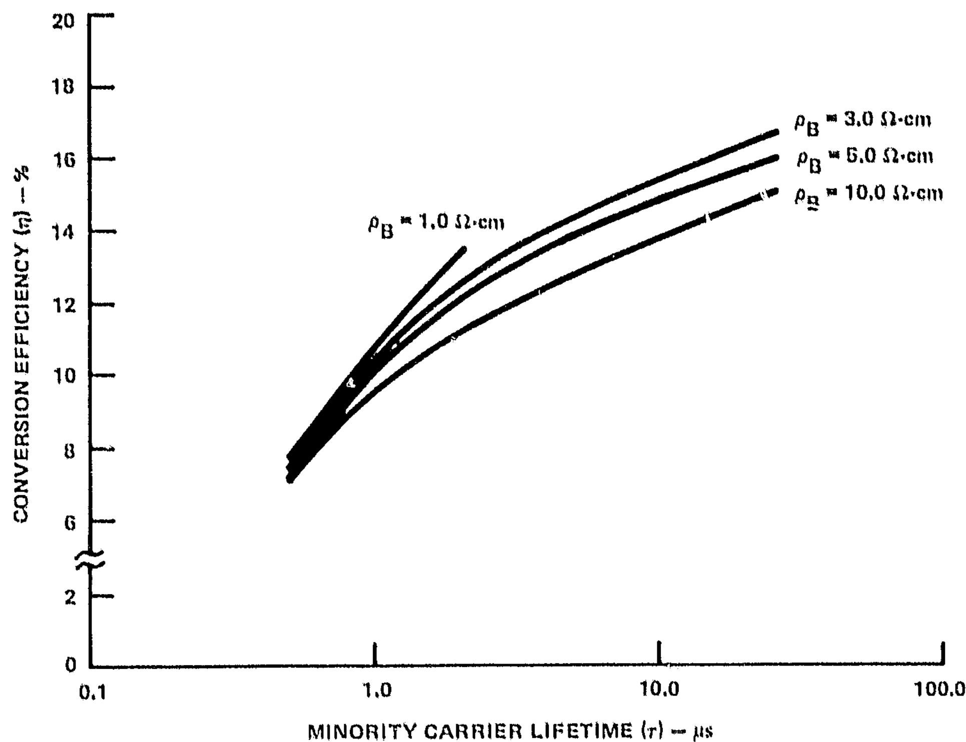


**Figure 7. Calculated Values of Conversion Efficiency as a Function of Minority Carrier Lifetime in the Base with Base Resistivity as a Parameter**

The metal pattern for the mask configuration selected is shown in Figure 8. The rationale used in designing the mask layout is discussed below:

1. Maximum center-to-center spacing is determined from series resistance. For the cross section used here, the sheet resistance of the P-base is much larger than that of the N+ collector so that Equation (9) applies. The smallest finger density consistent with resistance loss is used since the percent of P-area increases with finger density.

2. Resistive loss in metal is limited by total area; interdigitated fingers extending across the entire slice gives the most efficient use of area. Stepped metal fingers are used with the widest part connected to the bond pad. Tapered fingers might be more efficient but would add complexity to masks. Resistive loss in the bond pads (trunk) would be significant; these losses are essentially eliminated by soldering connecting bus bars across the full width of the entire metallized pad in the module assembly scheme.

3. $N^+$ contact width is limited to 50 $\mu$m. This minimizes dark current (higher $V_{OC}$) and absorption of light at the back surface. Metal fingers are expanded over the oxide to reduce series resistance of metal fingers.

4. $P^+$ contacts are slightly wider (75 $\mu$m) since $P^+$-contact resistivity is high and erratic.

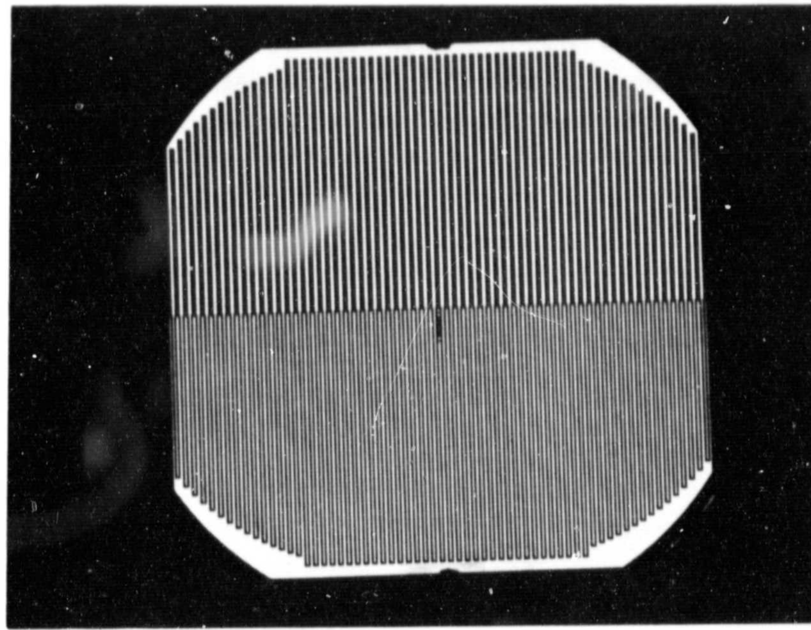

Figure 8. Metal Pattern for 6.2 × 6.2 cm Truncated Square TJC

## 2. Process Verification

Process verification test lots were run on 2 × 2 cm TJCs. Probe testing was done before sawing into squares by using backside illumination (the light shines between the metal contacts). Only preliminary conclusions can be drawn regarding photoresponse from these probe tests.

Two Czochralski (Cz) grown crystals were used to check minority carrier lifetime after a steam oxidation and again after a $POCl_3$ diffusion at 850°C. Two slices from each crystal were oxidized in steam at 850°C, the oxide was stripped and the lifetime was measured using the surface photovoltage (SPV) technique. The slices were then coated on one side with a low-temperature plasma-deposited silicon oxide and the other side was phosphorous-diffused at 850°C for 60 minutes. The oxide was removed and the SPV lifetime measurement was repeated. Two fresh slices from each Cz crystal were coated on one side with plasma-deposited silicon oxide and subjected to the same phosphorous diffusion conditions. The oxide was removed and the SPV lifetime measurement was made. The results are listed in Table I.

Table I. Process Lifetime Measurements

| Crystal | Lifetime After Steam Oxidation ($\mu$s) | Lifetime After $POCl_3$ Diffusion ($\mu$s) |
|---|---|---|
| 548 | 6 - 8.5 | 24 - 27 |
| 548 | No Oxidation | 28 |
| 549 | 7.5 - 16 | 33 - 42 |
| 549 | No Oxidation | 45 - 50 |

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The data suggests that while a steam oxidation degrades minority carrier lifetime in Cz grown crystals, a subsequent phosphorous diffusion provides a gettering effect that substantially recovers the lifetime. The conclusion from this data is that any process sequence that uses a steam oxidation step must follow the steam oxidation with a phosphorous diffusion step to retain minority carrier lifetime for solar cell operation.

Contact resistivity on the $P^+$ regions was measured after alloying Al at 650°C and 850°C. The concentric ring pattern described in earlier reports on this contract was used. Contact resistivity between the evaporated Ti-Pd-Ag contact metallization and the alloyed Al $P^+$ layer is shown below. In all cases, 4000Å of evaporated Al was used.

| **Alloy Conditions** | **650°C/30 min** | **850°C/30 min** |
|---|---|---|
| $\rho_c$ ($\Omega$-cm$^2$) | $2 - 4 \times 10^{-3}$ | $0.4 - 2 \times 10^{-3}$ |

Further sintering of the evaporated Ti-Pd-Ag contacts at 450°C did not appreciably change $\rho_c$. The $\rho_c$ obtained with the 850°C alloyed Al region is acceptable for cell fabrication.

Alloying Al $P^+$ contacts at 650°C or 850°C gives virtually identical results at backside probe. Both temperatures are effective.

Frontside illumination tests on cells where the $P^+$ region was created by alloying evaporated Al at 850°C and 650°C showed that the 850°C alloy condition gave slightly better results with $V_{OC}$ rising to 0.595 V from 0.587 V and $J_{SC}$ increasing to 38 mA/cm$^2$ from 36 mA/cm$^2$ at AM1. The 850°C alloy step was included in the baseline process.

During the process verification, it was noticed that $V_{OC}$ values after mounting for test were lower than anticipated, see Table II. A careful evaluation of the "tail end" mounting process sequence, strip frontside process oxide, deposit AR coating, saw, gold tab bond, showed that the gold tab mounting process was causing a degradation in the cell photoresponse. The saw and gold tab bonding process are carried out in a separate facility as a service to this program. Careful checking of recent history showed that a change had been made in the routine gold bonding procedure several months earlier. The bonding pressure had been increased significantly to improve bond strength on IC's. One wafer containing two 2 X 2 cm cells was carefully monitored through the process to verify that the increased bonding pressure was the culprit. The front oxide strip, AR deposition steps were replaced by a thinning of the front oxide to eliminate the possibility of photoresponse degradation, increased surface recombination, while the front surface was bare. Data on the 150-$\mu$m thick wafer from lot AAAP-II-116 is shown in Table III. Prior to gold tab bonding all measurements are made with backside illumination under an AM1 source (ELH lamp). (It is not convenient to make frontside illumination measurements on a TJC without bond tabs.)

The drop in $I_{SC}$ after saw caused by the elimination of lateral collection from areas external to the cell was expected. After bond, both $V_{OC}$ and $I_{SC}$ show significant degradation. This degradation is attributed to damage generated in the diffused region under the bond. This effect is of no concern in the proposed module assembly scheme since reflow solder bonding will be used to assemble the modules. Reverse leakage across the collector-base junction at 1 volt did not change during the assembly for test process.

**Table II. Process Variation Photoresponse**

| Lot No. | Thickness (μm) | $V_{OC}$ (V) | $J_{SC}$ (mA/cm$^2$) |
|---|---|---|---|
| AAAP-II-107 | 100 | 0.575 | 26 |
| | 150 | 0.575 | 27 |
| AAAP-II-108 | 100 | 0.577 | 31 |
| | 150 | 0.52 | 10 |
| AAAP-II-109 | 100 | 0.50 | ≈10 |
| | 150 | 0.50 | ≈10 |

**Table III. Photoresponse During Assembly for Test**

| Assembly Process Step | Illumination Side | 12 Finger TJC | | 16 Finger TJC | |
|---|---|---|---|---|---|
| | | $V_{OC}$ (mV) | $I_{SC}$ (mA) | $V_{OC}$ (mV) | $I_{SC}$ (mA) |
| Before saw | Back | 589 | 94 | 588 | 87 |
| After saw | Back | 587 | 86 | 585 | 79 |
| After bond | Back | 576 | 80 | 576 | 74 |
| After bond | Front | 586 | 130 | 589 | 128 |

TJCs from lots AAAP-II-113 and -116 were assembled using a low-pressure gold tab bonding process. Photoresponse was measured under an AM1 source (ELH lamp) using front illumination. The data on three cells from each lot is shown in Table IV. The increase in $V_{OC}$ and $I_{SC}$ for lot AAAP-II-116 is evident (compare to bottom line of Table III).

Individual process steps were varied to establish process limits. These variations were run in groups, with each group containing a baseline lot that was used as the process control.

The backside boron implant was varied along with the phosphorous diffusion temperature. The diffusion step was used to anneal the implant. A baseline group ($1 \times 10^{14}$ atom/cm$^2$ B implant, 850°C $POCl_3$ diffusion), lot AAAP-II-107; a reduced implant group ($5 \times 10^{13}$ atom/cm$^2$ B implant, 850°C $POCl_3$ diffusion), lot AAAP-II-108; and a high-temperature phosphorous diffusion group ($1 \times 10^{14}$ atom/cm$^2$ B implant, 1000°C $POCl_3$ diffusion), lot AAAP-II-109. Each group contained 100-μm and 150-μm thick wafers. The 2 X 2-cm cells were attached to gold ribbon tabs and measured at AM1. The results are shown in Table II. The baseline process lot AAAP-II-107 results were typical for this modest lifetime crystal. The equivalent results for both thicknesses were encouraging. The reduced implant process, lot AAAP-II-108, is also encouraging at 100-μm thickness. The optimum implant dose has a fairly broad range, $5 \times 10^{13}$ to $1 \times 10^{14}$ atom/cm$^2$. The high-temperature phosphorous diffusion process, lot AAAP-II-109, is not acceptable and apparently the high temperature causes lifetime degradation. These cell measurements probably include some degradation due to gold tab bonding (see above).

**Table IV. Photoresponse with Corrected Gold Tab Bond Process**

| Lot No. | Al Alloy Temp (°C) | $V_{OC}$ (V) | $I_{SC}$ (mA) | $J_{SC}$ (mA/cm$^2$) |
|---|---|---|---|---|
| AAAP-II-113 | 650 | 0.590 | 136 | 34 |
| AAAP-II-116 | 850 | 0.599 | 142 | 36 |

Backside boron implant doses above $1 \times 10^{14}$ atom/cm$^2$ cause degradation of the base-emitter junction and are not acceptable. For example, at an implant dose of $8 \times 10^{13}$ atom/cm$^2$ in 10 Ω-cm P-type substrate, the base-emitter reverse breakdown voltage is 6.2 V, at a dose of $5 \times 10^{14}$ atom/cm$^2$ in the same substrate, the base-emitter reverse breakdown voltage is $< 1$ V.

Five process variation test lots were completed through backside illumination testing. These process variations and backside photoresponse measurements are summarized in Table V. Several useful correlations can be made from this and earlier data.

Lot AAAP-II-113: The deep front $N^+$ diffusion, $\approx 0.5$ to 0.6 μm, does not severely impact current collection during back illumination. This effect was checked using front illumination (Table IV) confirming the transistor model proposed earlier for the TJC.

Lots AAAP-II-113A, -114 and -115: Variations in the first oxidation process step, have only second-order effects on photoresponse. In particular, the 1000°C dry $O_2$ oxidation does not exhibit any marked reduction in lifetime when followed by an 850°C phosphorous diffusion. The low temperature, 450°C, silane deposition does not offer any marked advantage.

Lot AAAP-II-116: The increase in the Al alloy process step from 650°C to 850°C appears to offer a significant improvement in the baseline process.

The process variation data reported above coupled with earlier reported process variation data gives the outline for an updated baseline process relative to each of the high-temperature operations. The optimal conditions for each critical process step are outlined below.

1. Backside boron implant dose — $5 \times 10^{13}$ to $1 \times 10^{14}$ atom/cm$^2$ at 35 KeV
2. First oxidation — 850°C steam oxidation will be retained but the upper temperature limit could be raised if it offered a processing advantage so long as the oxidation is followed by a phosphorous diffusion.
3. Phosphorous diffusion — 850°C appears to be near optimum, 950°C causes a marked loss in collection efficiency. The depth of the front $N^+$ diffusion up to $\approx 0.6$ μm does not appear to have a significant effect.
4. Al alloy — An 850°C alloy process step appears to offer significantly better response than a 650°C alloy. This effect is probably due to improved electrical activation of the alloyed Al atoms.

Table V. Process Variation Test Runs

| Lot Number | Crystal No. | Crystal Type (in) | Res (Ω–cm) | Thickness (μm) | Back Illumination | | Process Variation |
|---|---|---|---|---|---|---|---|
| | | | | | $V_{OC}$ (V) | $I_{SC}$ (mA) | |
| AAAP-II-113 | 452 | 2 Cz | 6 | 100,150 | 0.588* | 89* | Deep Front N+ |
| AAAP-II-113A | 348 | 3 Fz | 10 | 150 | 0.573–.579† | 105–120† | Baseline |
| AAAP-II-114 | 348 | 3 Fz | 10 | 150 | 0.578–.581† | 96–107† | 1000°C Oxidation |
| AAAP-II-115 | 348 | 3 Fz | 10 | 150 | 0.571–.576† | 104–116† | Silane Oxide |
| AAAP-II-116 | 348 | 3 Fz | 10 | 100,125,150 | 0.595–.599† | 107–115† | 850°C Al Alloy |

* AM1 Illumination
† W-lamp

Lots AAAP-II-113A, -114, -115 and -116 were all run using 2 cm X 2 cm cells on 3-inch (7.62 cm) wafers. No particular handling or breakage problems have been observed. The 150-μm thick wafers are somewhat less fragile than the 100-μm thick wafers.

From these process verification tests, a baseline process was evolved for fabrication of large-area, 6.2 X 6.2 cm, TJCs. The process outline is given in Table VI.

### 3. Design Verification

The large-area TJC design described in II.A was verified by calculating $I^2R$ power loss in the key loss areas, the masks were checked for overlay accuracy and the final verification was checked by device fabrication. An outline of each verification process is given below.

$I^2R$ power losses were calculated using Equations (15) and (9) to calculate the fractional loss in the P+ fingers and in the base, respectively. Equation (15) represents the metallization loss, as derived in Eq. (11), for the case of a metal pattern with steps in width, i.e., $T_1$ and $T_2$.

$$F_F = \frac{K_I^2 J_{SC} S \rho_m L^2}{3 V_{OC} T_1 CF} + \frac{K_I^2 J_{SC} S \rho_m L^2}{24 V_{OC} T_2 CF} \qquad (15)$$

and

$$F_B = \frac{K_I^2 J_{SC} S^2}{12 V_{OC} CF} \rho_s \text{ (base)} \qquad (16)$$

where

$J_{SC}$ = short-circuit current density = 0.035 A/cm$^2$

S = center-to-center finger spacing = 0.102 cm

$\rho_m$ = metallization resistivity (Ω/□) = 0.005 Ω/□

L = finger length = 6 cm

$T_1$ = finger width narrow section = 0.0076 cm

$T_2$ = finger width wide section = 0.0254 cm

$V_{OC}$ = open circuit voltage = 0.6 V

$\rho_S$ = base sheet resistivity (Ω/□) = 533 Ω/□

$K_I = J_M/J_{SC}$ where $J_M$ is current density for maximum power

CF = curve factor

The fractional power loss in the fingers, $F_F$ is ≈ 1.7% and in the high-resistivity base region is ≈2.6% for this design. Other design options using internal plated metal bus bars would give larger fractional power losses.

**Table VI. Baseline Tadem Junction Call Process**

**Frontside textured, thin (150 μm) wafer**
**7.62 cm dia, P-type, 6-10 Ω-cm**

Boron inplant, 8 X $10^{13}$ atom/cm$^2$ @ 35 KeV (back)
Steam oxidation, 850°C, 80 minutes
Define $N^+$ region (back)
Phosphorous diffusion, 850°C, $POCl_3$, 60 minutes
Remove front oxide
Phosphorous diffusion, 850°C, $POCl_3$, 15 minutes
Deposit oxide (front and back)
Define $P^+$ region (back)
Evaporate Al
Pattern
Alloy Al, 850°C, 15 minutes
Define $N^+$ and $P^+$ contacts (back)
Evaporate Ti-Pd-Ag
Define contacts
Backside probe (optional)
Plate Ag
Laser scribe squares
Test

The photomasks were checked for pattern registration using an overlay technique. Each mask level was compared to every other mask level by photolithographic comparison. On the first pass, it was discovered that mask level 1 was slightly oversized. This was corrected by refabricating this level. Before cell fabrication began, pattern registration was verified on all levels.

Finally, the design was verified by fabrication of test TJCs. Large-area cells, 6.2 X 6.2 cm, from lot AAAP-II-120 were fabricated using the baseline process shown in Table VI. Backside probe measurements gave $I_{SC}$ = 0.55 – 0.60 A, $V_{OC}$ ≈0.55 V. Since over 50% of the back is covered by the metallization pattern, the expected $I_{SC}$ for front illumination was > 1 A.

This completed the design verification.

## 4. Cell Fabrication

Four lots of large area TJCs were started. The lead lot, AAAP-II-121A, containing 14 cells was completed through metal plating and laser scribe. During the final process steps and testing operations, six of the 150-$\mu$m thick cells were broken. The remaining cells were examined and tested.

The frontside illumination test is conducted by holding the cell against a ceramic, alumina, fixture using a vacuum hold down. The ceramic fixture has metal tabs that correspond to the bus areas of the cell metallization. The ceramic fixture metallization is connected to the test equipment, either a Tektronix curve tracer or a digital multimeter, using probes. The frontside of the cell is illuminated at AM1 using an ELH lamp system. The cell test setup is adequate for measuring $V_{OC}$ and $I_{SC}$ but there is too much internal test fixture resistance to allow fill factor measurements. The main element of resistance external to the cell is in the pressure contacts to the cell metallization.

During examination, it was noted that the silicon dioxide layer on the front of the cells, this layer functions as an AR coat, was very thin and on some cells had been virtually removed during processing. The thickness of this deposited oxide layer was increased on the subsequent lots to eliminate this problem.

The remaining eight large-area TJCs were checked for photoresponse at AM1. The data is shown in Table VII.

**Table VII. AM1 Photoresponse for Lot AAAP-II-121A**

| Cell Number | $V_{OC}$ (mV) | $I_{SC}$ (A) |
|---|---|---|
| 1 | 579 | 1.16 |
| 2 | 533 | 0.84 |
| 3 | 584 | 1.21 |
| 4 | 585 | 1.19 |
| 5 | 542 | 0.64 |
| 6 | 535 | 0.86 |
| 7 | 577 | 0.95 |
| 8 | 530 | 0.93 |

The cells with low $V_{OC}$ and $I_{SC}$ all exhibit frontside areas where the front oxide layer was completely removed during processing. The best cells, numbers 1, 3 and 4, all appear to have continuous oxide on the frontside. All cells exhibit a lowered $V_{OC}$ due to heating from the AM1 source. The ceramic fixture thermally insulates the cell from the controlled temperature mount. The decrease in $V_{OC}$ is estimated to be approximately 10-15 mV (4-7°C).

The decrease in $V_{OC}$ and $I_{SC}$ for cells with part of the front oxide removed is much greater than would be expected from reflection of light alone. It is assumed that the bare areas on the front surface allow areas of very high surface recombination to exist and these areas act as current sinks. This problem was eliminated on later process lots by increasing the front oxide thickness so that oxide thinning during processing did not remove the front oxide layer.

As an experiment using cells 7 and 8, the frontside $SiO_2$ layer was stripped and redeposited using a low-temperature plasma desposition. After the plasma oxide deposition, photoresponse at AM1 was $V_{OC}$ = 0.579 V and $I_{SC}$ = 1.17 A, equivalent to cells 1, 3 and 4. Due to the possibility of surface contamination during the strip and redeposition, this technique is not recommended as a standard process on completed cells.

Three following lots, AAAP-II-121B, -122A and -122B, containing a total of 100 potential cells, were processed through backside probe. All three lots showed no photoresponse. Failure analysis indicated that there was no $N^+/P$ junction in these devices. Initial problem tracing pointed to a mechanical failure in the phosphorous diffusion system, either a leak or a solenoid failure. All three lots were scrapped. This mechanical failure was corrected by replumbing the phosphorous diffusion furnace and recalibrating the system. This mechanical breakdown caused a serious delay in the program schedule that jeopardized program completion within the allotted budget.

Three more lots, AAAP-II-123, -124 and -125, containing a total of 225 potential cells, were started on a rush basis to try to recover some of the lost time. A process-related problem, oxide undercut, occurred on lot AAAP-II-123 during the second photoresist-etch operation, $P^+$ oxide removal (O.R.). The interposed $N^+$ and $P^+$ regions on the backside of the TJC are separated by a design spacing of $2.5 \times 10^{-3}$ cm (0.001 inch). When an oxide undercut occurs, the alloyed Al spreads into the undercut region. As a consequence of the oxide undercut, the $P^+$ Al alloy process step resulted in $P^+$ to $N^+$ leakage or shorting. This leakage or shorting degrades device performance to unacceptable levels. Lot AAAP-II-123 was scrapped.

Cells from lots AAAP-II-124 and -125 were used for process testing on the photoresist and etching steps relevant to the second O.R., $P^+$ oxide removal. Changes in the photoresist bake temperature, from 110°C to 165°C, and in the oxide etch composition, increase the ratio of $NH_4F$ to HF, solved the oxide undercut. The undercut was not observed at the first O.R., $N^+$ oxide removal or at the third O.R., contact oxide removal. It was deduced that this oxide undercut was related to a change in the adhesion of the photoresist to the oxide surface. The cause of the oxide undercut at second O.R. was not identified. Although the source of this process problem is technically interesting and relevant, the program schedule and budget were exhausted.

The process test experiments did eliminate a number of possible sources of the oxide undercut problem. The deposited oxide layer had the same refractive index, 1.50; thickness, 2000Å; and etch rate, 1000Å/minute at 25°C in Bell 2 etch, that had been maintained for many months. No other program using this same oxide deposition system observed an undercut problem. The use of commercial adhesion promoters did not help. The use of a fresh supply of photoresist or processing the photoresist in a different facility showed no improvement. Removal of the phosphorous glaze prior to the oxide deposition and/or densifying the deposited oxide in $O_2$ at 850°C for 15 minutes did not eliminate the undercut. Nonpatterned etch removal of the top 200 to 400 Å of the deposited oxide prior to photoresist application did not eliminate the undercut. Vacuum baking of the wafers at 250°C prior to photoresist application did not eliminate undercut. The relative humidity and temperature of the photoresist facility remained within normal operating limits.

Using the empirical parameter changes, increased photoresist bake temperature and a more buffered etch solution, five wafers from lot AAAP-II-125 were processed to completion. At backside probe using backside AM1 illumination, all five cells exhibited $V_{OC}$ of 0.56 V ±0.02 V and $I_{SC}$ = 0.60 A ±0.05 A. Prior to laser scribe, frontside AM1 illumination gave $V_{OC}$ = 0.58 V ±0.01V and $I_S$ = 1.15 A ±0.05 A. During laser scribe, three of the five cells were broken by an inexperienced operator. The two remaining 6.2 × 6.2-cm cells at AM1 exhibit $V_{OC}$ of 0.579 V and 0.581 V and $I_{SC}$ of 1.19 A and 1.20 A, equivalent to the good cells in the first lot of large-area TJCs.

From the measured short-circuit current, a short-circuit current density, 1.20 A ÷ (6.2 cm × 6.2 cm) = 0.0312 A/$cm^2$ at AM1 can be derived for these 150-$\mu$m thick large-area TJCs. Although slightly better current density has been observed on 2 cm × 2 cm TJCs, this is a satisfactory result for the first generation of large-area devices. Improvements in the frontside AR coating, higher refractive index materials, e.g., silicon nitride, would be expected to yield ≈5% increases in short-circuit current density.

Fill factor was not measured on these individual cells due to series resistance in the vacuum hold-down jig. The cell design was based on a FF of 0.75–0.78. Using a FF value of 0.75, the calculated cell power at AM1 would be

$$\text{Cell power} = 0.58\ \text{V} \times 1.2\ \text{A} \times 0.75 = 0.522\ \text{W}$$

and the cell power density at AM1 would be

$$\text{Power Density} = \frac{0.522\ \text{W}}{37.05\ \text{cm}^2} = 14.1\ \text{mW/cm}^2$$

This large-area TJC module program was initiated on a schedule that did not allow for any significant slippage and a budget that did not comprehend any unplanned consumption of resources. The mechanical failure of the phosphorous diffusion system coupled with the oxide undercut process problem caused a program slippage of approximately eight weeks and consumed labor and resources over this period. A request for a schedule extension and additional funds was denied. Consequently, the cell fabrication activity was not completed.

Although process simplification was not a specified part of this project, some thought was given to a more cost-effective, simpler process flow. The guiding theme behind this concept of process simplification was that all process steps should be additive, i.e., anything that is added to the silicon wafer should appear in the final product. Guided by this theme, the conceptual process sequence shown in Figure 9 is proposed. In the figure, the wafer is always shown with the topside (sunside) up. This process has not been tried in the labroatory, but most of the individual process steps have been demonstrated in the semiconductor industry. A brief discussion of each process step is given below.

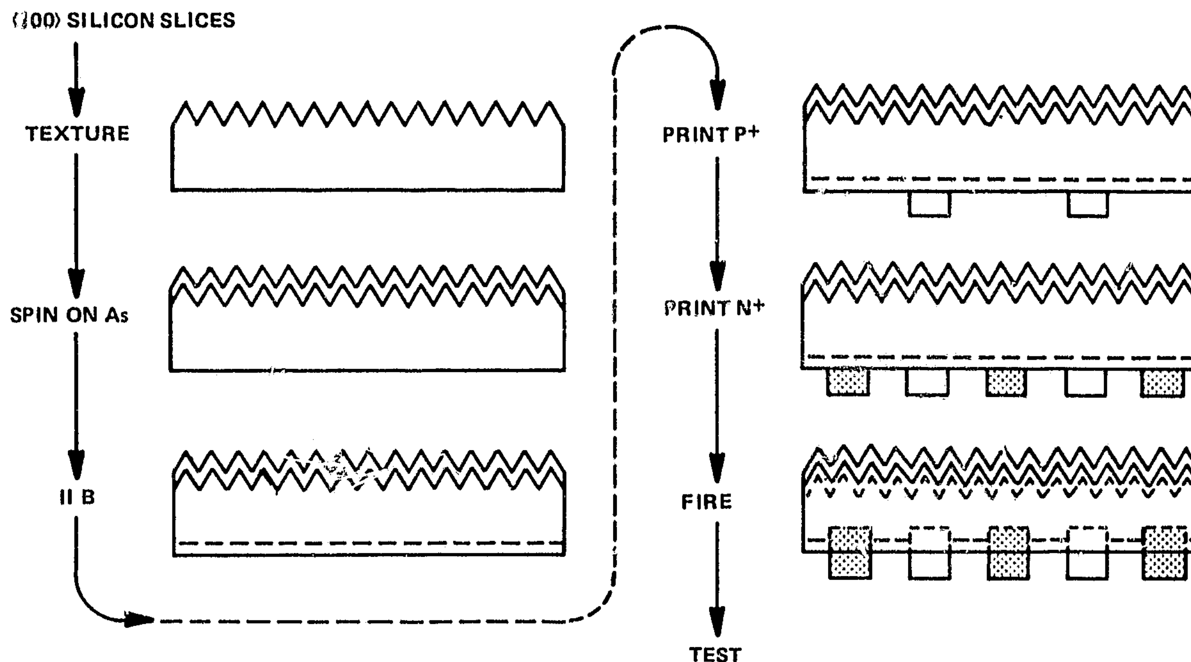



**Figure 9. Conceptual Process Sequence for Tandem Junction Cell Fabrication**

**Step 1 – Texture.** This is a standard dilute sodium hydroxide texture etch process to reduce surface reflection and refract light in the thin substrate.

**Step 2 – Spin-on As.** This step provides the source for the topside $N^+$ layer. This step would use spin-on polymer dopants, spray techniques or ion implantation. The choice of a spin or spray polymer dopant is based on using the residual silicon oxide film as the AR coating. The choice of As as the dopant is based on the slower diffusion rate for As, however P or Sb may work as well or better, depending on the final firing cycle.

**Step 3 – Ion Implant B.** This step provides the pseudo back surface field used in the TJC. A dose of 5-10 $\times$ $10^{13}$ atom/cm$^2$ would be recommended (as discussed on pages 15, 16).

**Step 4 – Print $P^+$.** In this operation, the $P^+$ metallization and the source for the $P^+$ diffusion under the printed metal contacts are applied at one time as a printed ink. As an example, Al doped Ag can be applied to P-type silicon to form an ohmic contact after firing. Any of the group III dopants, B, Al or Ga, could be used as the source of the $P^+$ layer. This process has been demonstrated to fabricate a diode solar cell using a phosphorous containing polymer dopant and an Al-Ag ink[8] followed by a single firing-diffusion step.

**Step 5 – Print $N^+$.** In this operation the $N^+$ metallization and the source for the $N^+$ diffusion are applied at one time as a printed ink. This process step has not been tried. The $N^+$ ink should contain an $N^+$ dopant that will diffuse ahead of the alloyed contact metallization to form the $N^+/P$ junction. This operation is similar to the old alloy junction technique used in the 1950s to fabricate diodes and transistors.

**Step 6 – Fire.** This one high-temperature operation is planned to diffuse the front $N^+$ layer, convert the polymer dopant film to a silicon oxide film, anneal the boron ion implant, diffuse the $P^+$ dopant and sinter the $P^+$ metallization, and diffuse the $N^+$ dopant and sinter the $N^+$ metallization. All of these operations can be carried out in the vicinity of 850°C under a suitable atmosphere. Mixtures of nitrogen and oxygen, possibly clean air, should be ideal. This step will require careful development to get a proper balance of time and temperature such that all thermal operations are reasonably optimized.

While this conceptual process sequence has not been demonstrated, it does show that a simple, potential low-cost TJC process is possible. Future work in this area of process development should be pursued as part of the LSA Program.

## B. TANDEM JUNCTION MODULE

### 1. Define Cell-Module

A properly designed photovoltaic module requires a coordination between the design of the cell and the design of the module. In particular, cell bond pads and the module interconnect system must be compatible and should be complementary. In this vein, a design review was held before the cell design was finalized. Critical geometries on the cell and on the module components were compared and tradeoffs were established. The module was designed as a parallel (5)-series (6) array of 30 cells. The external cell dimension, a nominal 6.2 cm, is shown in Figure 8.

The cell would have a single $N^+$ bond pad and a single $P^+$ bond pad. These bond pads would be located on opposite sides of the square cell. The bond pad width would be 0.127 cm with a 0.025 cm separation from the opposite conductivity metal finger. This bond pad width, 0.127 cm, would not be sufficient to collect the current generated by the cell without serious $I^2R$ losses. In the module assembly, however, the interconnect bus would be attached along the entire flat width, ≈ 4 cm, of the bond pad and would provide the necessary low conductivity current collection. In this fashion, one of the module components, the interconnect bus bar, augments the current collecting bond pads on the cell.

The clad metal interconnect bus bar will span from the $P^+$ bond pad on one cell to the $N^+$ bond pad on the next (series) cell. At the same time, the interconnect bus bars will connect adjacent cells in a redundant parallel fashion, see paragraph B.7 in this section. The interconnect bus bars were designed to fall 0.025 cm from the inside dimension of the bond pad to allow for the solder fillet. The solder attachment can be made using condensation or infrared soldering.

### 2. Modify Tooling

An analysis of the minimodule size indicated that embossing is not necessary to assure substrate rigidity. On larger substrates, 1.2 × 0.6 m, embossing would be recommended. The embossed groove also provides a recess for the backside interconnects. In the series-parallel configuration chosen for this work, the interconnect thickness is only 0.002 inch (0.0051 cm) and recessing is unnecessary. Therefore, tooling modification was not necessary and was eliminated.

Sheet steel was cut, Figure 10, and formed to shape. Twenty substrates were formed using 20-gauge (0.0359 inch, 0.0912 cm) cold rolled steel and 20 substrates were formed using 22-gauge (0.0299 inch, 0.0759 cm) cold rolled steel. Top and front views of the formed cold rolled steel for the substrate are shown in Figure 11.

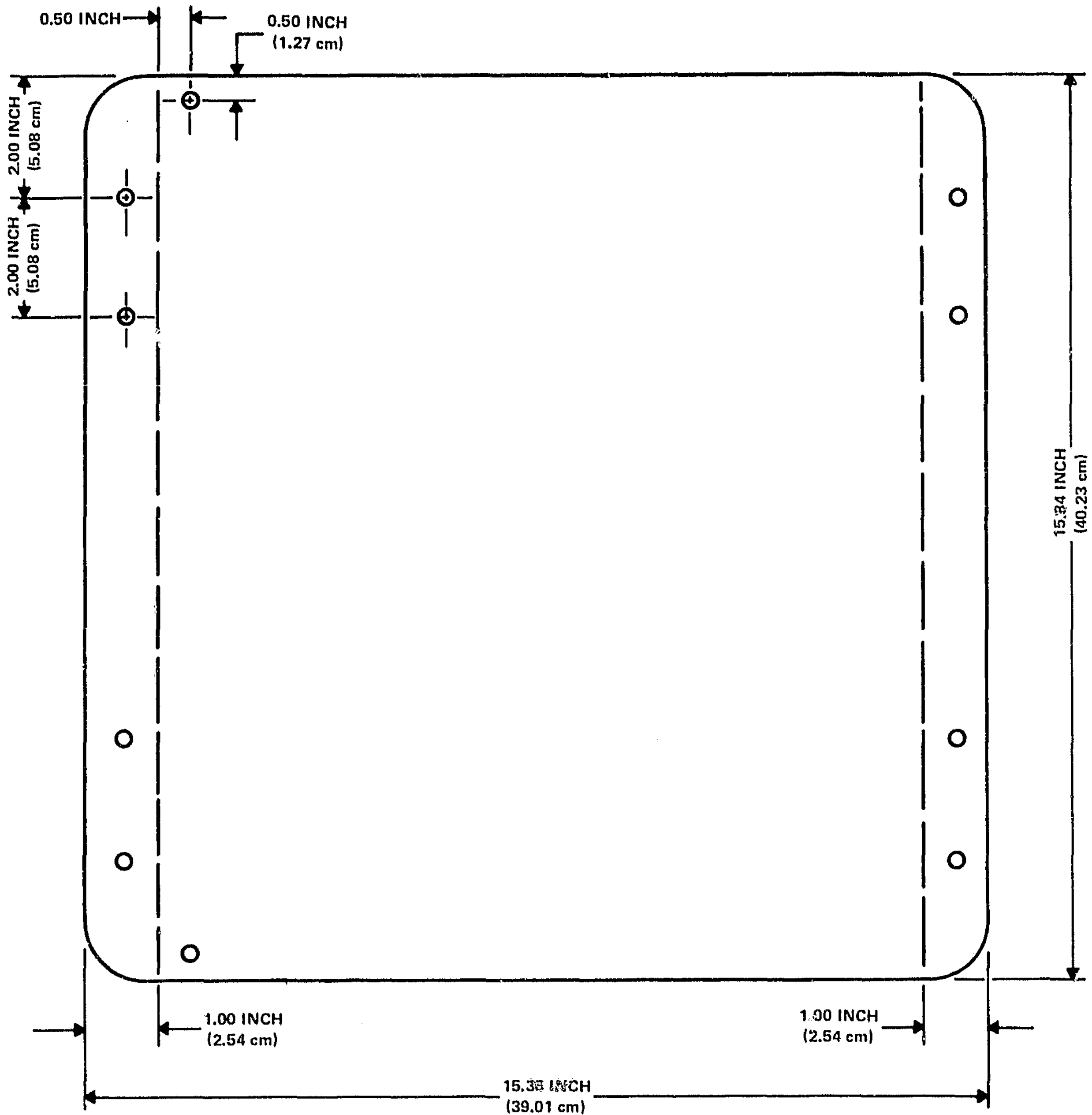



Figure 10. Top View of Substrate Blank

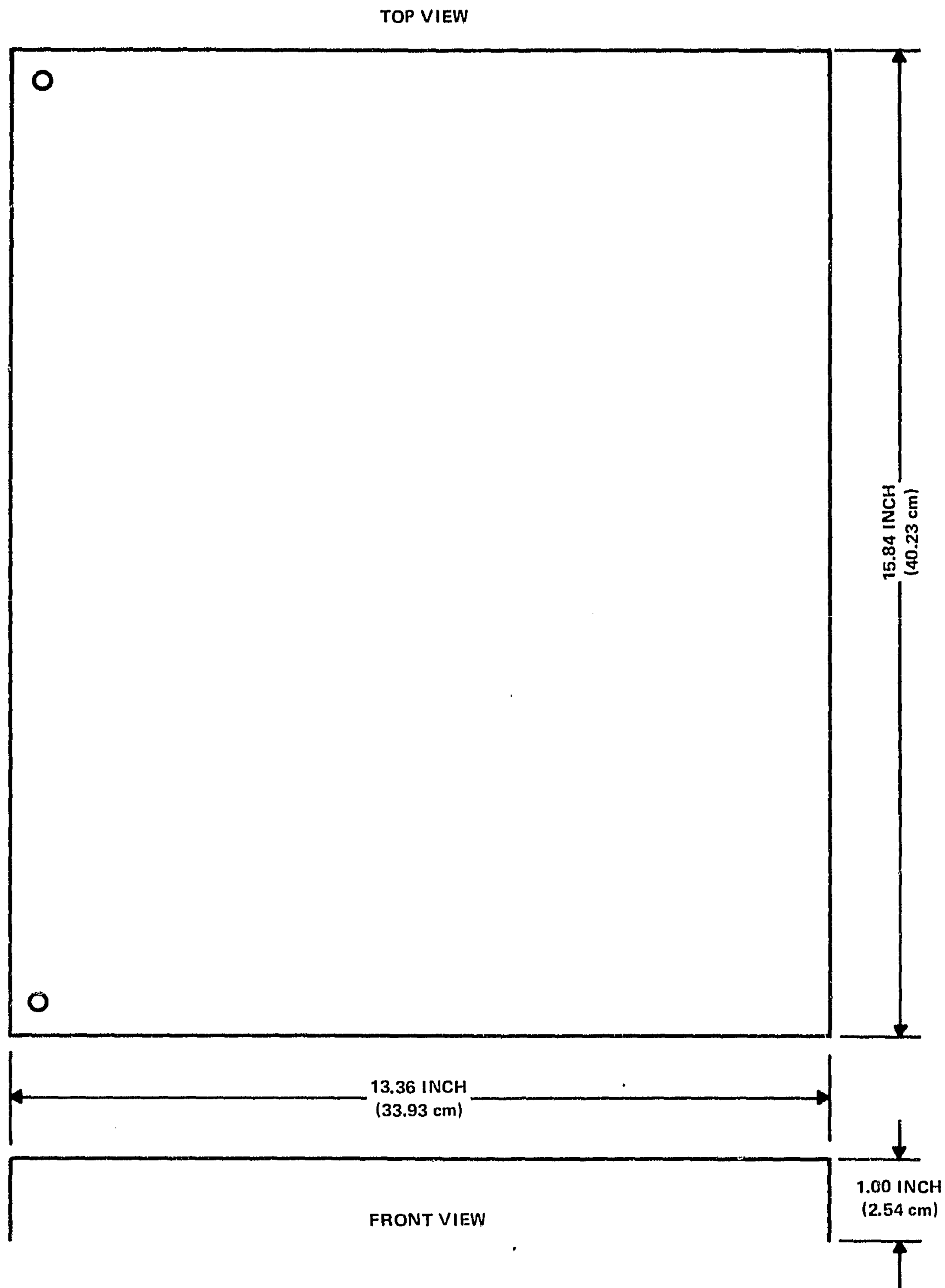



Figure 11. Formed Substrate

### 3. Define Heat Treatment

Previous work on the combination of steel forming and subsequent porcelainizing indicated a problem in that improper stress-relief prior to porcelainizing results in an "oil can," twist, or bow of the substrate during porcelainizing. Consequently, a small program was established to evaluate stress-relieving of the substrates prior to and after porcelainizing.

Ten formed substrates of each gauge cold rolled steel were stress relieved at 600°F (316°C) for one hour in air. Ten formed substrates at each of the two gauges (0.091 cm and 0.076 cm) that were heat treated and 10 formed substrates from each gauge that were not heat treated were shipped to Ervite Corporation, Erie, Pennsylvania, for porcelainizing. After procelainizing, the substrates were measured for bow. The measurements are given in Table VIII. Heat treatment at 600°F has no significant effect on bowing of the formed substrates during the procelainizing operation. Thickness or gauge of the formed substrate does not appear to be a significant factor.

**Table VIII. Heat Treatment Results**

| Substrate Number | Heat Treat | Gauge (cm) | Convex Bow | |
|---|---|---|---|---|
| | | | Avg. (cm) | Range-Min-Max (cm) |
| 1–10 | No | 0.091 | 0.181 | 0.152–0.889 |
| 11–20 | Yes | 0.091 | 0.150 | 0.127–1.09 |
| 51–60 | No | 0.076 | 0.141 | 0.127–0.686 |
| 61–70 | Yes | 0.076 | 0.163 | 0.064–0.828 |

### 4. Porcelainized Substrates

As reported above, all substrates exhibited some bow. A fixture was built to attempt a straightening operation after porcelainizing. See Figures 12 and 13. Preliminary tests indicate that a low temperature-time heat treat reduces the bow.

Although very flat substrates were not achieved in this attempt, flat porcelainized steel ware is common in industrial and consumer businesses, e.g., refrigerators, stoves and fluorescent light fixtures. The substrates fabricated in this one-shot trial are acceptable. Better flatness could be achieved with a reasonable amount of effort.

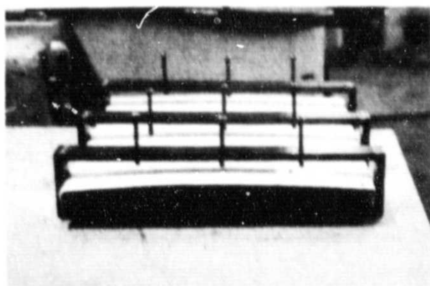


Figure 12. Substrate in Fixture Before Reversing the Bow

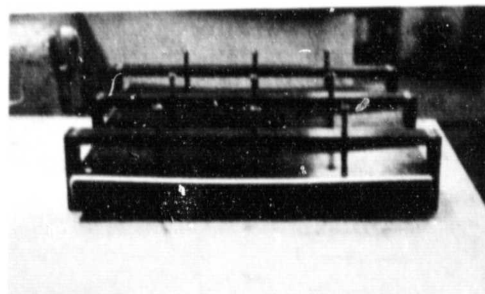


Figure 13. Substrate with Bow Reversed Prior to Heat Treating

## 5. Design and Form Bus Bars

As demonstrated earlier in this contract, copper/Invar/copper laminates can be fabricated to more closely match the thermal expansion coefficient of silicon. The tandem junction module interconnect scheme will use thin ribbons of this clad metal material. Copper/Ivar/copper was bonded with a 12.5/75/12.5 ratio, and rolled to a thickness of 0.0102 cm. The bus bar material was subsequently rolled to a final thickness of 0.0051 cm.

The minimum allowable bus bar thickness can be calculated by defining the minimum allowable power loss in the bus bar. If we allow a 1% $I^2R$ power loss and assume a cell output of 1.0 A at 0.5 V, then minimum bus bar thickness is calculated as follows:

$$\Delta P = I^2 R_C \tag{17}$$

where

$\Delta P$ = allowable loss = 0.01 × 1.0 × 0.5 = 0.005 W

$I$ = cell output

$R_c$ = resistance of clad bus bar

then

$$0.005 \text{ W} = (1.0)^2 R_c$$

$$R_c = 0.005\ \Omega$$

The resistance of the composite clad metal conductor can be calculated as a set of parallel layers

$$\frac{1}{R_c} = \frac{1}{R_1} + \frac{1}{R_2} \cdots \frac{1}{R_n}$$

where $R_1, R_2 \cdots R_n$ are the respective resistances of the clad metal layers.

By combining the top and bottom copper layers into one term, we obtain:

$$\frac{1}{R_c} = \frac{1}{R_{Cu}} + \frac{1}{R_{Invar}} \tag{18}$$

or

$$\frac{1}{R_c} = \frac{W \times t_{Cu}}{\rho_{Cu} \times L} + \frac{W \times t_{Invar}}{\rho_{Invar} \times L} \tag{19}$$

where

$W$ = width of bus bar = 4 cm

$L$ = length of bus bars = 0.2 cm

$t_{Cu}$ = total copper thickness = 0.25 $T_B$

$t_{Invar}$ = Invar thickness = 0.75 $T_B$

$\rho_{Cu}$ = resistivity of copper = $1.7 \times 10^{-6}\ \Omega$-cm

$\rho_{Invar}$ = resistivity of Invar = $5.0 \times 10^{-5}\ \Omega$-cm

$T_B$ = thickness of bus bar

Solving for $T_B$ we obtain

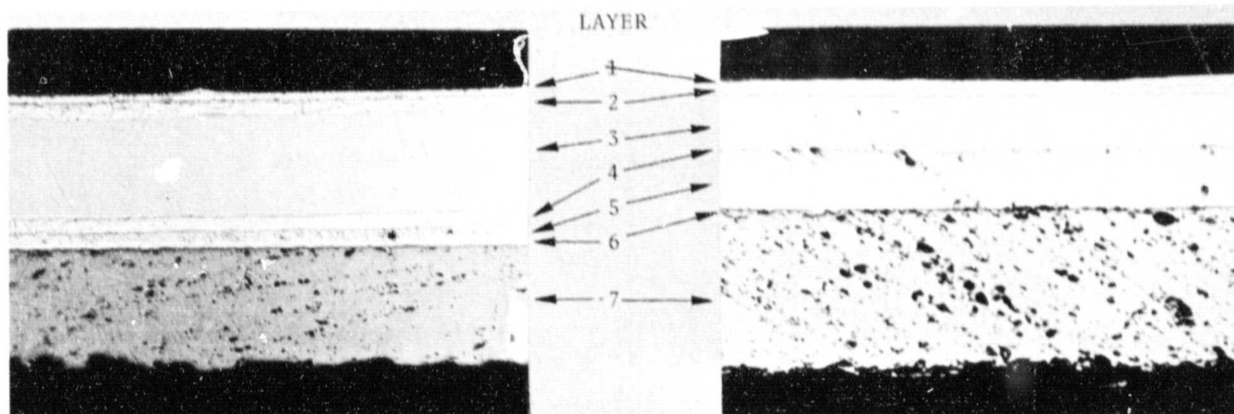
$$T_B = 6.2 \times 10^{-5} \text{ cm}$$

Therefore the actual loss in the bus bar interconnects of $5.1 \times 10^{-3}$ cm thickness would be significantly less than 0.1% of the power available at the cell bond pads. The use of wide, short clad interconnect bus bars results in a deliverable power saving while maintaining a stress-free cell-to-cell interconnect system.

### 6. Solder Fixture

Soldering evaluations were conducted with bus bar thickness of 0.025 cm, 0.0102 cm, and 0.0051 cm using 2 × 2 cm TJCs. Cross sections of the soldered interconnects are shown in Figure 14. No problems were encountered nor were expected with the bond integrity at the bus bar – plated Ag interface. The thin, 0.0051 cm, clad metal interconnects perform as expected.

A soldering fixture was built which could accommodate up to a 5 × 6 matrix. The fixture is basically a vacuum chuck on which the cells are positioned. The vacuum chuck is supported by a hot plate which preheats the chuck to minimize heat sinking prior to infrared soldering, see Figures 15 and 16.




0.0102 cm BUS @ ~ 146X

0.0051 cm BUS @ ~ 146X

LAYER 1 – SOLDER
2 – COPPER
3 – INVAR
4 – COPPER
5 – SOLDER
6 – CELL METALLIZATION
7 – CELL

Figure 14. Cross Sections of Clad Metal Interconnects Soldered to TJCs



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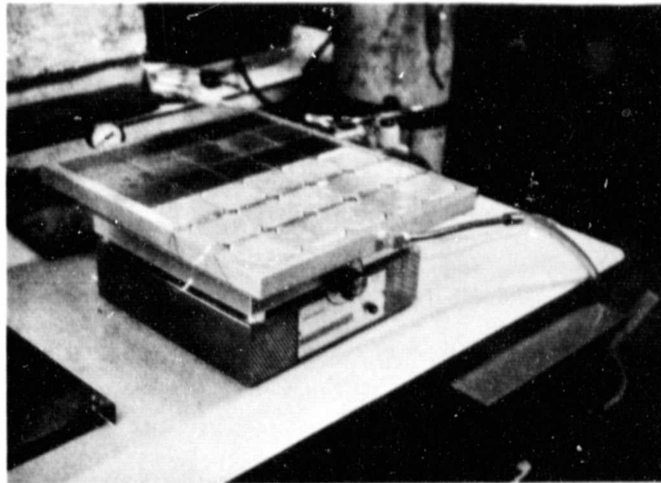

**Figure 15. Vacuum Chuck with 3 × 5 Cell Matrix (Front View)**

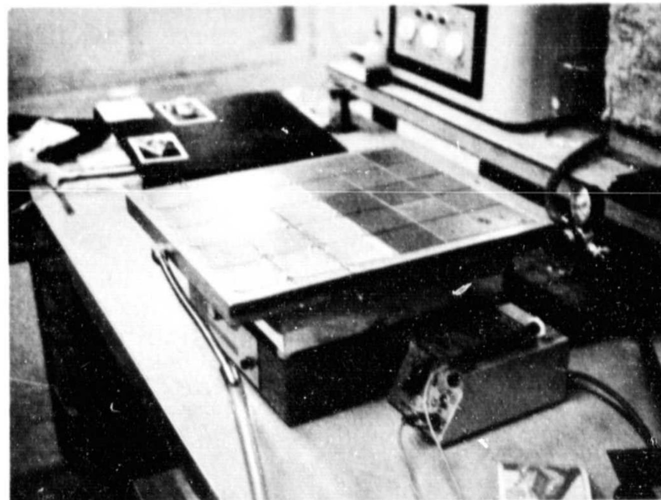

**Figure 16. Vacuum Chuck with 3 × 5 Cell Matrix (Side View)**

7. **Assemble Cell Matrix**

Infrared soldering was first successfully demonstrated on a one-cell and two-cell string of dummy cells. The dummy cells contain the correct metallization pattern but are not electrically active.

Using dummy cells, a 3 × 5 cell matrix and 5 × 5 cell matrix were assembled to check out the assembly technique. The two parallel-series cell matrices are shown in Figures 17 and 18. The excellent cell nesting efficiency is evident in these photographs. The cells are series connected horizontally, left to right, and parallel connected vertically, top to bottom.

Since enough TJCs to fabricate modules were not available from task I.4, no photovoltaic TJC matrices were assembled. The assembly technique was demonstrated to be effective.

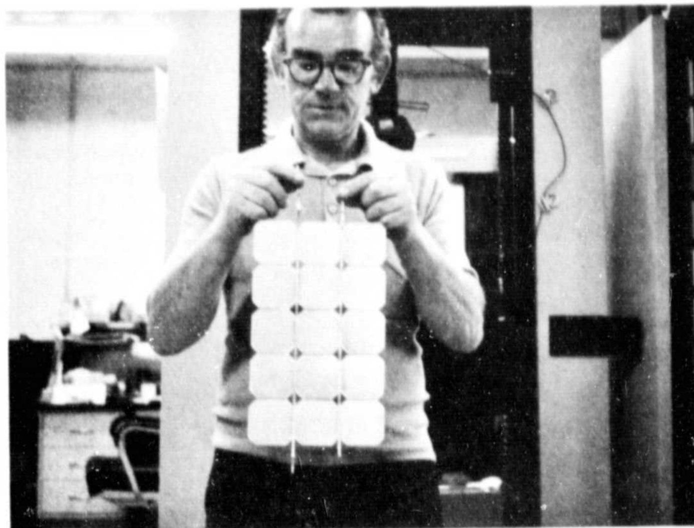

Figure 17. 3 × 5 Cell Matrix

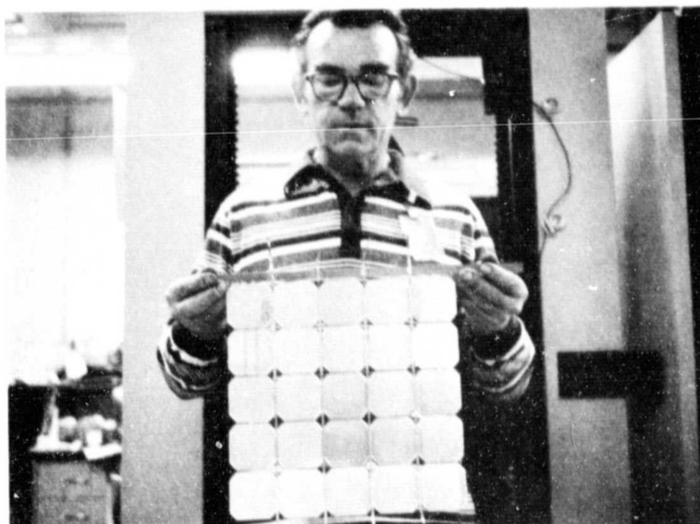

Figure 18. 5 × 5 Cell Matrix

## 8. Assemble Module

Due to mechanical and process problems (section II.4), large-area TJC fabrication was not completed. The module assembly procedure can be described as follows.

1. Assemble 5 × 6 TJC matrix.
2. A small drop of RTV-615 is placed on the backside of each cell in the 6 × 5 cell matrix. The cell matrix is then positioned on the porcelainized steel substrate and connected electrically with the feedthroughs.

3. A small RTV-1284 bead is laid around the periphery of the glass 0.95 cm in from the edge. After curing, the glass is positioned on the substrate with the RTV gasket in contact with the substrate. The purpose of this gasket is to act as a dam for the polysulfide seal (EC801). The seal is applied using an automatic dispensing unit and it filled the cavity from the RTV gasket out to the edge of the module, see Figure 19. The polysulfide is cured at 120°F for 24 hours.

   (Liquid filling was chosen instead of a gel as a pottant for a number of reasons. Gels inherently are associated with delamination at cell interfaces, interconnect areas, or along module borders. Gels are more difficult to work with. The major disadvantage of a liquid results when the seal integrity is violated or the glass cover breaks. The liquid chosen was a Union Carbide Silicone Fluid (L-45). L-45 has excellent mechanical properties, resist breakdown by shear, is compressible, and highly efficient at dampening vibrations. It is available in high purity, for electrical use, has high resistance to breakdown by voltage, exceptional insulation quality and resistivity, and very low electrical losses. Union Carbide L-45 silicone dielectrics are used in ac and dc circuitry.)

4. Liquid filling is accomplished using the automatic dispensing unit. The seal on the module was punctured with a needle from the dispensing unit and then filled. Another approach is also to leave a section of seal uncompleted, fill the module cavity using an ordinary oil can dispenser, and then finish the seal.

5. After liquid-filling, the gating seal is cured.

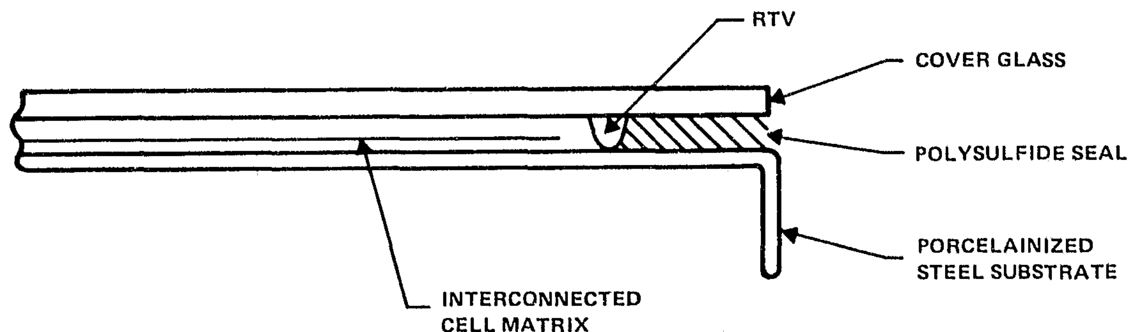


Figure 19. Schematic of Module Edge Seal

## 9. Test and Ship

No TJC modules were completed when this program terminated. Therefore no test data was taken and no modules were shipped. However, one can calculate the expected performance of a 5 X 6 array of TJCs in a glass-covered module as follows.

From the measured AM1 characteristic of 6.2 cm X 6.2 cm TJCs, the single cell $V_{OC}$ is 0.58 V and $I_{SC}$ is 1.2 A for a bare cell. Encapsulation loss would be ≈ 4%, primarily because of topside reflection from the glass cover (one side reflection from a glass-air interface). Power loss in the array due to interconnects would amount to less than 0.1 %. No losses in generated cell power need to be accounted for due to interconnect shadowing or module bus lines. The voltage, current, power and power density are summarized in Table IX for the bare TJC, encapsulated TJC, 30 cell TJC matrix encapsulated and the 30-cell TJC module, assuming a fill factor of 0.75.

The total cell area in a 30-cell matrix is 1111.38 $cm^2$. The total module area (external dimension) is 1365 $cm^2$. If a 1.0-cm border around the exterior edge of the module is dedicated to sealing the glass cover to the porcelainized substrate, the interior area of the module is 1220.68 $cm^2$. The ratio of cell area to total module area is 0.814 and the ratio of cell area to internal module area is 0.91.

**Table IX. Calculated Photoresponse**

| | $V_{OC}$ (V) | $I_{SC}$ (A) | Power (W) | Power Density $mW/cm^2$ |
|---|---|---|---|---|
| Bare TJC | 0.58 | 1.2 | 0.522 | 14.09 |
| Encapsulated TJC | 0.58 | 1.152 | 0.501 | 13.52 |
| 5 (parallel) X 6 (series) TJC matrix (encapsulated) | 3.48 | 5.76 | 15.03 | 13.52 |
| TJC Module | 3.48 | 5.76 | 15.03 | 11.01 |

If full square were used for the TJC instead of the truncated squares used in this study, the ratio of cell area to total module area would rise to 0.844 and the ratio of total cell area to interior module area would rise to 0.944. As total module size is increased, the 1.0-cm perimeter dedicated to sealing the glass cover to the procelainized steel substrate would remain fixed and the ratio of the interior module area to the total module area would increase from the 0.894 on this module to 0.960 on a 1.00 m X 1.00 m module and the cell area, using full squares, to total module area ratio would rise to 0.906. This demonstrates the high nesting efficiency that can be achieved using square cells with all backside interconnects. The incorporation of clad metal interconnect buses whose thermal expansion coefficient matches silicon over the temperature range of interest eliminates the need for expansion or stress relief loops without sacrificing reliability.

## SECTION III
## CONCLUSIONS AND RECOMMENDATIONS

The transistor module for the TJC has proved to be very useful in increasing the cell size from 2 cm X 2 cm to 6.2 cm X 6.2 cm. Further improvements in cell efficiency should be obtainable by improving the existing model and applying the module to structure and process optimizations.

Scale up of the TJC from 2 cm X 2 cm to 6.2 cm X 6.2 cm was successful. Bare cell efficiencies of 14% at AM1 were achieved.

Process limits for the key process steps were established. All process limits are within readily controllable ranges.

Cell design must be coordinated with module matrix design to achieve optimum packing density. Module components, such as interconnects, can be designed to supplement cell components for overall module performance.

Future development efforts on the TJC should emphasize improved device modeling and use of device models to guide structure and process optimization. AM1 efficiency of 20% should be achievable.

A simplified, all additive TJC process has been proposed. This process concept will require development effort to bring the proposed process to a factory process.

## SECTION IV
## NEW TECHNOLOGY

No areas of new technology were identified in 1979.

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## SECTION V
## PROGRAM SUMMARY

Figure 20 shows the final work plan status. Activity I.4, Cell Fabrication, was not completed. Activities II.7, II.8 and II.9, Assemble Cell Matrix, Assemble Module and Test and Ship could not be completed. All other activities were completed.

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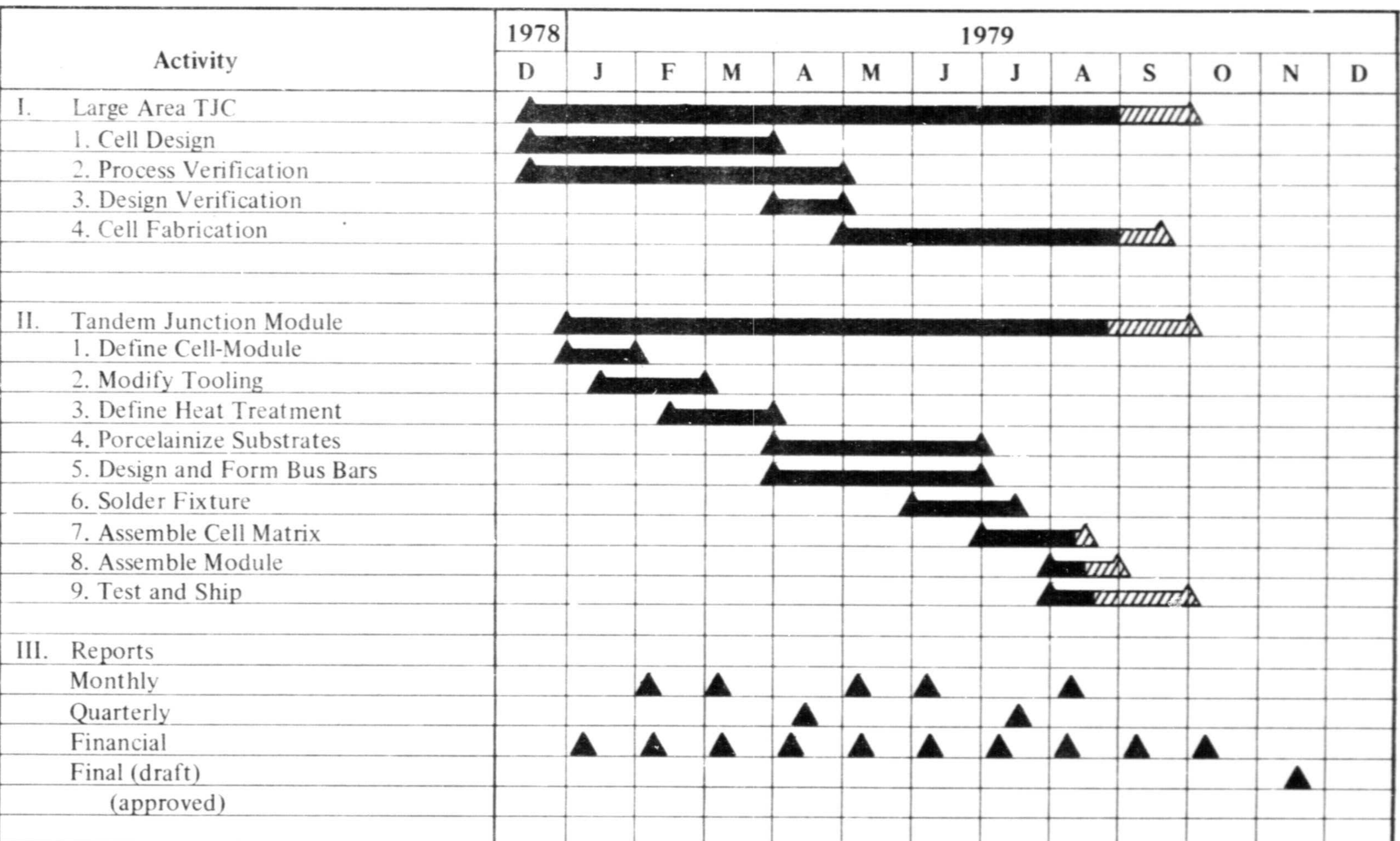


Figure 20. Work Plan Status



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## SECTION VI
## REFERENCES

1. W. T. Matzen, S. Y. Chiang, and B. G. Carbajal, "A Device Model for the Tandem Junction Solar Cell," *IEDM* (Late News), Washington, D.C. (December 1978).

2. W. T. Matzen, S. Y. Chiang, and B. G. Carbajal, "A Device Model for the Tandem Junction Solar Cell," *IEEE Trans in Electron Devices,* Vol ED-26, No. 9, 1365 (September 1979).

3. W. T. Matzen, B. G. Carbajal and R. W. Hardy, "Design Considerations for the Tandem Junction Solar Cell," Conference on Solar Cell High Efficiency and Radiation Damage, NASA Lewis (June 1979).

4. W. T. Matzen, S. Y. Chiang and B. G. Carbajal, "Optimized Metallization Patterns for Large-Area Silicon Solar Cells," Twelfth IEEE Photovoltaic Specialists Conference, Baton Rouge, Louisiana (1976).

5. W. T. Matzen, "A Physical Model for Series Resistance Losses in Solar Cells," to be published.

6. S. Y. Chiang, B. G. Carbajal and G. F. Wakefield, "Improved Performance Thin Solar Cell," *IEDM,* Washington, D.C. (1977).

7. S. Y. Chiang, W. T. Matzen, B. G. Carbajal, G. F. Wakefield, "The Back Surface Field Effect on Tandem Junction Solar Cell," Electrochemical Society Meeting, May 1979.

8. B. G. Carbajal, *Automated Array Assembly, Phase 2,* Annual Technical Progress Report 1978, DOE/JPL 954881-79-4, 23-24 (February 1979).