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Executive Summary
First Year Report:
On-Board Processing Concepts for Future Satellite Communications Systems

Edited by:

William T. Brandon, Project Leader

Dr. Brian E. White

MAY 1980

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BEDFORD, MASSACHUSETTS

ABSTRACT

This report is an executive summary of the first year's study which provides initial definition of on-board processing for an advanced satellite communications system to service domestic markets in the 1990's. An exemplar system with both RF on-board switching and demodulation/remodulation baseband processing is used to identify important issues related to system implementation, cost, and technology development. Analyses of spectrum-efficient modulations, coding, and system control techniques are summarized. Implementations for an RF switch and baseband processor are described. Major conclusions of the first year's study are listed in the final section.

FOREWORD

The report was prepared by editing the previously published final report and incorporating some newly prepared text. Contributions of the authors of the original final report text and new draft materials are acknowledged as follows:

SYSTEM CONTEXT (from section 6 of final report)	Dr. John M. Ruddy
SIGNAL DESIGN, PROCESSING, AND SYSTEM CONTROL	
Waveform Analysis (from sections 3.2, 3.3 of final report)	Dr. Brian E. White
Regenerative Processing (from section 3.4)	Dr. Joseph Katz
System Control (from section 3.1 and new text)	S. L. Kota
LARGE SCALE BROADBAND MICROWAVE SWITCH (from section 5 and new text)	Murray Hoffman
BASEBAND PROCESSOR (from section 4)	Dr. David P. White

The specific selection of material from the final report and the modification of the report structure are the responsibility of the editors.

We were assisted in editing the report by Ruth W. Wales.
Joan Johnson prepared the text for reproduction.
Charles Provencher, Jr., NASA Lewis Research Center, expedited a review of the draft providing useful comments. Their assistance is acknowledged with thanks.

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EXECUTIVE SUMMARY

INTRODUCTION

The anticipated growth in demand for telecommunications services will accelerate with the introduction or elaboration of new services (such as video conferencing and high speed computer networks). Even without these new services, the continuing growth in private line, video broadcast networks, and other familar services leads to the conclusion that United States domestic satellite capacity achievable in the 4/6 and 12/14 GHz bands will not be sufficient in the 1990 time period. Since satellite communications has proven cost-effective for domestic telecommunications, expansion of the satellite capability into the 1990's appears essential. Accordingly, National Aeronautics and Space Administration (NASA) Lewis Research Center is conducting a program of studies leading toward development and demonstration of technology which can form the basis for a 1990's satellite system which can expand the communications capacity available from the geostationary arc.

The NASA Lewis program has focused on the development of a new frequency band (30/20 GHz) with frequency reuse as a central feature. This approach will provide technology for greatly extending the utility of U.S. domestic satellite communications in the 1990's and beyond. System concepts devised to provide frequency reuse and high capacity incorporate multiple beam uplink and downlink antennas interconnected by either radio frequency (RF) switching (in which the signals are not demodulated) or demodulate/remodulate processing (in which the signals are demodulated to data bits and reformatted for downlink transmission). Neither concept is strictly new, but for the applications envisioned, considerable extension of the state-of-the-art is implied.

MITRE is conducting a two-year study of on-board processing for NASA Lewis Research Center as an integral part of the 30/20 GHz program. This volume is an abbreviated executive summary of an extensive final report on the first year's study effort. The complete report contains more detailed treatments of the topics discussed herein, and also contains discussions of a number of topics not included in this volume. In addition to the main study report, a second volume summarizes the results of a thorough literature survey of on-board processing in an annotated bibliography of 272 papers and reports.

SYSTEM CONTEXT

A preliminary system level cost/performance tradeoff was undertaken to identify critical technologies required to support wideband trunking and thin route (or customer premises) services in the 30/20 GHz satellite communications band. In particular, the tradeoff focuses on the relationship between on-board signal processing and terminal size, complexity, and cost.

To define relationships between system elements, technology needs, and costs, it is necessary to investigate relationships in a system context. The exemplar system context developed for this purpose is illustrated in figure 1.

Trunking terminals handle wideband high data rate traffic and are located in major metropolitan areas. Traffic is concentrated by the terrestrial system and consists of multiple T3 (44.736 Mb/s) and/or T4 (276.176 Mb/s) trunks. In the United States there are 36 metropolitan areas with populations greater than one million persons. Therefore, approximately 40 trunking centers (each with dual diversity) are potential high data rate users. We believe this notion provides adequate rationale for 40 fixed high gain antennna beams using satellite switched time division multiple access (TDMA) for beam interconnection. The number of beams is a primary system parameter and must ultimately be closely related to the terrestrial telephone plant.

Customer premises terminals, which are associated with T1 (1.544 Mb/s) and T2 (6.312 Mb/s) data rates, are greater in number. The total population could be in the tens of thousands, depending upon the cost of the service provided. In the preliminary analysis presented in this report, the population of T1/T2 terminals is 5000.

An examination of the implications of international regulations on power flux density (pfd) limits and conservation of geostationary arc estimated an upper bound (-11.5 dBW/Hz)* on satellite effective isotropic radiated power (EIRP) and a lower bound (1/2 m diameter, 36.9 dB at 18.6 GHz) on terminal antenna size.

The uplink and downlink transmitter powers are related and should not be specified independently since no advantage accrues in link performance by over-specifying either. Analysis of satellite

*This upper limit results from a terminal elevation angle of less than 5° to a geostationary satellite using the International Telecommunications Union 1971 pfd limit of -115 dBW/m² in any 1 MHz at the earth's surface.

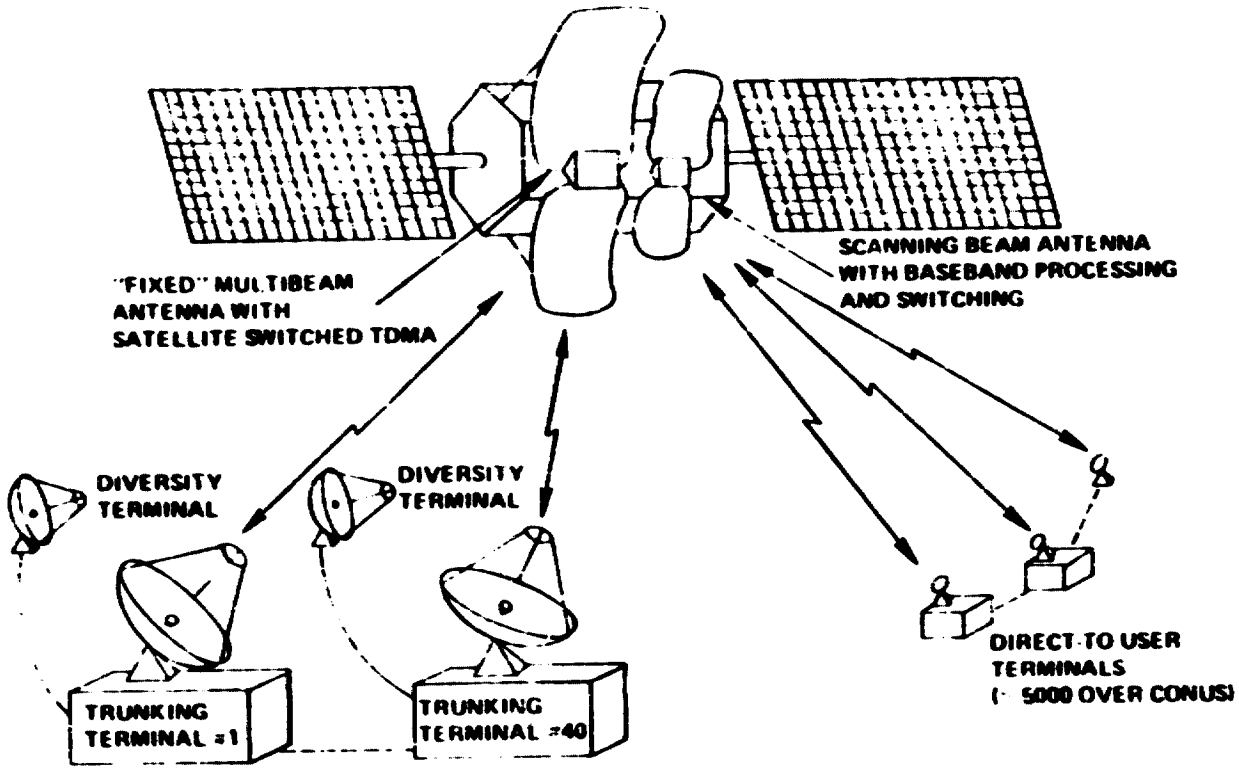

Figure 1. Exemplar 30/20 GHz System Concept

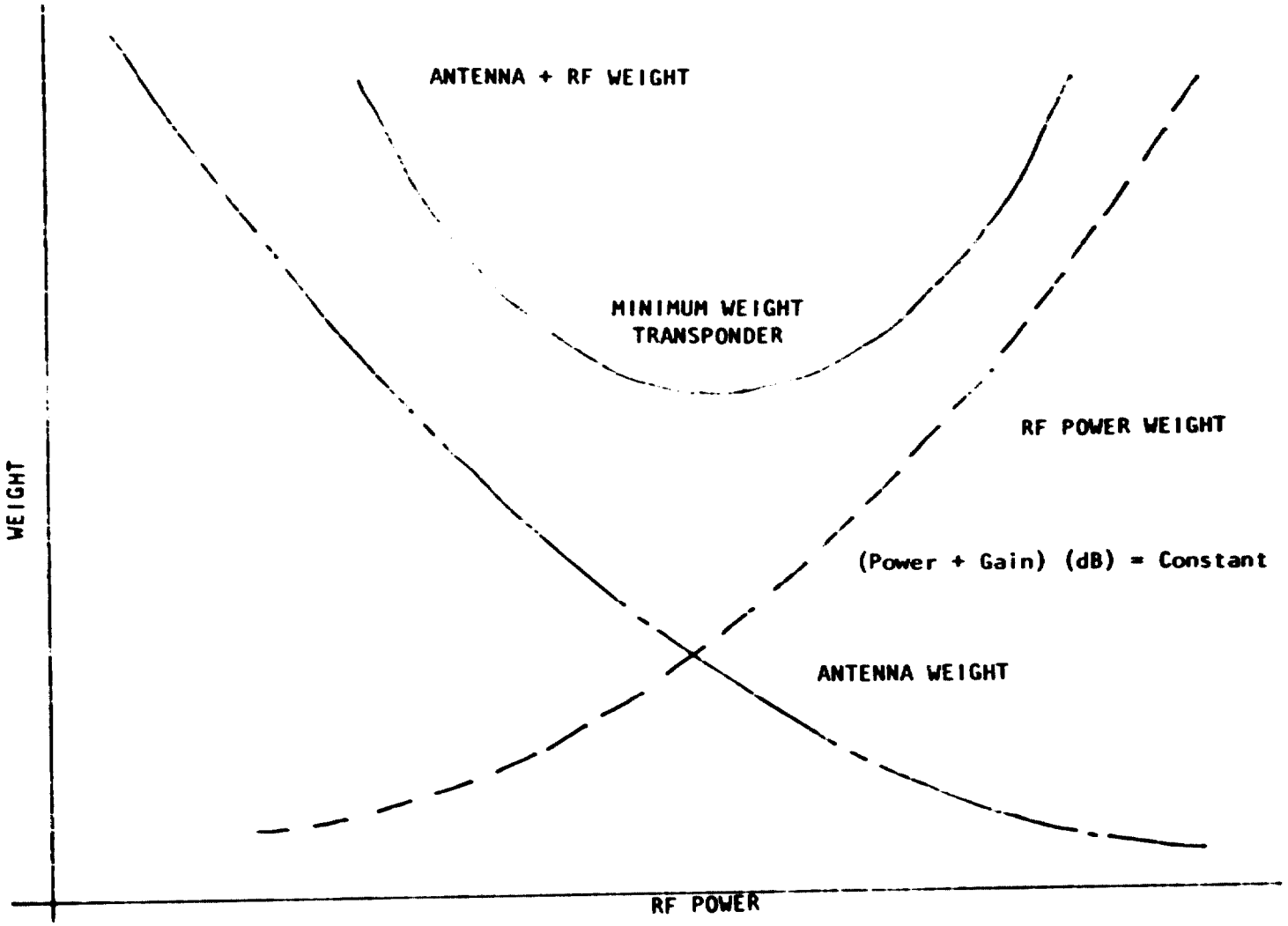

Figure 2. Weight of Transmitter and Antenna for Constant Satellite ERP

Technology Implications

The cost/performance analysis found in the main report* has led to the following preliminary conclusions. In order to minimize on-orbit weight and space segment cost, there is a definite trend toward using large satellite multibeam antennas with small RF power amplifiers. These antennas will be for fixed beam and scanning beam service. The lower power transmitters should provide reliability and life advantages as well as weight reduction.

There is a need for a large RF switch matrix for the wideband trunking channel. The switch size must exceed 40 x 40, but the final size requires further analysis, including studies of switch structures.** On-board processing is required for transmultiplexing of FDMA channels (i.e., converting frequency division multiple access (FDMA) uplink to time division multiplex (TDM) downlink with demod/remod) for rates on the order of 15 Mb/s per beam for the thin route channel Consequently, satellite technology development should emphasize large antenna structures with multiple fixed and scanning beam capabilities; RF switching for trunking channels; and demodulation, baseband processing and switching, remodulation of customer premises channels (with associated developments in high speed memory and logic), and low power solid state 20 GHz power amplifiers (5 W).

Terminal technology development should emphasize low cost, low power (10 W) and moderate power (50 W) 30 GHz transmitters; low cost GaAs field effect transistor (FET) low noise amplifiers (LNAs); low cost FDMA/TDM modems for the thin route terminals; low cost dual frequency antenna hardware; and high rate (800 Mb/s) modems for the trunking terminals.

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* "Final Report, Application of Advanced On-Board Processing Concepts to Future Satellite Communications Systems," MTR-3787, Volume 1, June 1979, Section 6.
**Ibid., Section 5.

Table 2

Some Characteristics of a Minimum Cost System Design

Item	Trunking Channel	Customer Premises Channel
No. Sat. Beams	40 fixed	2 scanning
Modulation	DQPSK (up/down)	DQPSK/CQPSK
Access(Up/Downlink)	TDMA/TDM	FDMA/TDM
Bandwidth/Beam	2400 MHz	100 MHz
Data Rate/Beam	3300 Mb/s	150 Mb/s
Sat. Ant. Dia. (ft)	(20/30)16.8/11	7.5/4.8
Sat. Ant. Dia. (m)	(5.1/3.4)	(2.3/115)
Terminal Ant. Dia. (ft)	24	3.3
Terminal Ant. Dia. (m)	(7.3m)	(1m)
Terminal RF Power	30 W	6 W
No. of Terminals	80	5000
Terminal Cost	$87M	$505M
Satellite Weight	5200 lb (2363 kgm)	
Satellite Power	2630 W	
Non-Recurring Engineering Cost	$300M	
Unit Production Cost	$89M	
Total Cost	$981M	

SIGNAL DESIGN, PROCESSING, AND SYSTEM CONTROL

This section summarizes several background studies of modulation, the use of coding, and the interrelationships of these system design techniques with regenerative and non-regenerative satellite repeaters. The results indicate the performance improvements which can be obtained through waveform and repeater design, coding, and transmitter operating points. Also included is a discussion of system control.

Waveform Analysis

In a system designed for spectrum conservation, choice of waveforms is extremely important. Signals with efficient spectrum occupancy exhibit higher values of b/s per Hz. Studies have identified and compared various waveforms in terms of several parameters, including how closely they can be spaced (close packing) in the frequency domain for a given bit error rate of detection (errors caused by interference of the adjacent signal spectrum). Some generalizations of continuous (frequency) shift keying (CSK) have excellent bandwidth efficiency compared with quadrature phase shift keying (QPSK) modulations. With unsynchronized signals which vary in received power by as much as 10 to 15 dB, a weak signal can still be reliably demodulated with roughly five to ten times as many CSK signals per unit bandwidth compared to QPSK.

Stated another way, a typical center frequency separation for CSK signals is 3/2 to 2 times the burst rate. This can be improved upon by forming a weighted sum of adjacent data bits to produce very smooth phase transitions. With this so-called tamed frequency modulation (FM) signaling, separations of only about 3/4 the burst rate may be feasible. Tamed FM requires only about a 1 dB larger E/N_o* than CSK for a given bit error probability in additive white Gaussian noise (AWGN). In band-limited situations, however, such a small increase in the energy contrast ratio (E/N_o) may be well worth the increased packing density required.

The salient parameter is the number of bits/cycle or b/s per Hz, which for FDMA is defined as the channel burst rate B normalized by the center frequency separation Δf, i.e., $\beta = B/\Delta f$. It is possible to state with assurance that low crosstalk digital modulations exist with $\beta > 2/3$, e.g., phase comparison sinusoidal

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*E denotes received signal energy per data symbol and N_o is the single-sided noise power spectral density at the receiver.

8

frequency shift keying (PCSFSK) and tamed FM, which perform within 1 dB of the ideal even when the received FDMA signals are mutually unsynchronized and vary in power by up to 10 or 15 dB. Equivalent performance with β as large as 2 may eventually be shown to be feasible. For now it may be conservatively assumed that $\beta = 2/3$ for the digital modulation employed in FDMA.

The close packing property is important not only to conserve the spectral resource but also to reduce digital sampling rates required to perform the demodulation of groups of FDMA signals. As an illustrative example, suppose the maximum feasible clocking rate is 300 MHz. (This is consistent with the discussion in the multiple access/multiplexing section related to a maximum QPSK burst rate of 600 Mb/s.) For digital quadrature carrier modulations like QPSK and CSK, this implies a maximum complex sampling rate of 300 MHz at a satellite demodulator, i.e., the bandwidth of the composite received signal to be demodulated must not exceed W = 300 MHz. For a packing factor of $\beta = 2/3$, the maximum product of burst rate B and number of FDMA carriers N is $BN = \beta W = 200$ Mb/s. Suppose the burst to data ratio for the T1 and T2 users is $r = B/R = 20$. Then, at most N = 200 Mb/s/20R, or about six T1 carriers or two T2 carriers per beam are possible. (A set of design curves is provided in figure 3. The required number of demodulators is obtained by multiplying by the number of beams for each user class.) If the packing factor were smaller by a factor of 5, as it might be for unsynchronized QPSK, TDMA operation would be infeasible for an equivalent level of crosstalk performance. On the other hand, if β could be increased to 2, 19 T1 carriers and five T2 carriers per beam can be processed.

Regenerative (Baseband) Processing

Regeneration is defined to include demodulation, manipulation of data (such as decoding, signal routing or baseband switching, and reformatting), and remodulation for downlink transmission. While the need for a large RF switch follows immediately from the concept of a multiple beam satellite with frequency reuse and TDMA operation of T3 and T4 trunks, the utility of regenerative baseband processing requires additional insight into applications and system design.

Regeneration decouples the uplink from the downlink, improving performance in digital satellite communication systems. The principal reason for the improvement is that uplink signal detection avoids the direct transfer of noise on the uplink to the downlink. The combination of detection and remodulation isolates uplink and downlink and hence permits individual tailoring of the waveforms such as FDMA uplink and TDM downlink.

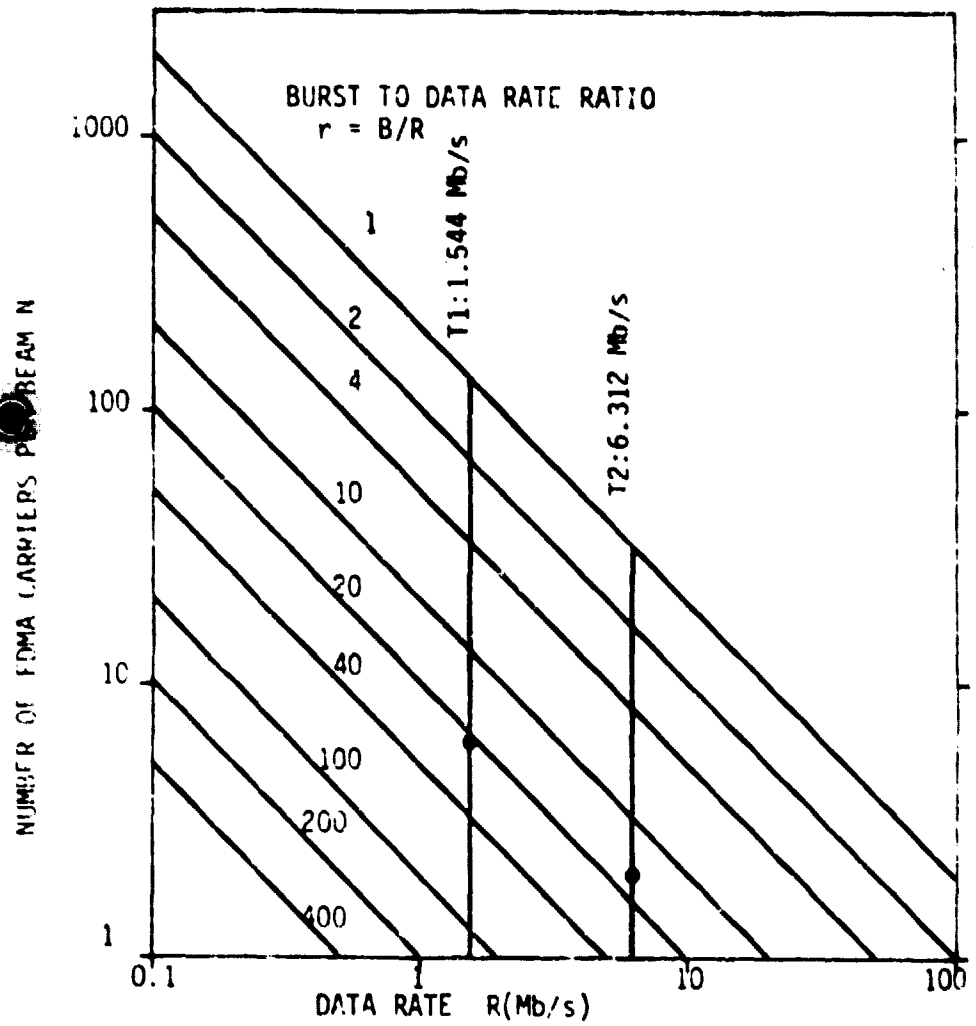

Figure 3. Number of Regenerators per Beam for Signal Bandwidth W = 300 MHz and Carrier Packing Factor β = 2/3 (βW = 200 Mb/s)

Regeneration may be relevant to all applications; however, it appears particularly useful for efficient operation and spectrum utilization for applications involving terminals at customer premises. In the present study, we have assumed T1 (1.544 Mb/s) and T2 (6.3 Mb/s) data rates for such users, although applications have been envisioned for even lower data rates.

Multiple Beams

A parametric analysis was conducted with the objective of identifying and exercising multiple beam satellite system tradeoffs for mixed classes of users operating at the transmit (TX) carrier data rates. This work will serve as a foundation for creating and evaluating specific system designs responsive to future domestic satellite communications markets.

A fundamental assumption of this 30/20 GHz study was that multiple beams are attractive for providing frequency reuse and higher satellite antenna gain. In order to insure the offloading of the terrestrial network in the heavier traffic areas and to provide a significant advance in the satellite state-of-the-art, at least 40 fixed spot beams covering the major US metropolitan centers are suggested. Large terminals operating in a TDMA mode at QPSK burst rates up to about 600 Mb/s through an RF switched satellite are appropriate for this fixed beam, wideband trunking service. Throughputs of several tens of Gb/s are attainable.

Customer Premises service in cities and remote areas as well, is best accomplished with scanning spot beams, controlled on a demand assignment basis, using minimum shift keying (MSK)-type uplink modulation at lower burst rates with FDMA/TDM through regenerative satellite channels. Reasonable on-board digital processing speeds limit the throughput of these smaller terminals to several hundred Mb/s. Accordingly, most of the 2.5 GHz allocated bandwidth is employed by the fixed beams.

Analysis shows that throughput is maximized by devoting the entire bandwidth and all the beams to the channels with the largest b/s per hertz efficiency. However, this solution precludes the stated objective of providing satellite capacity to more than one class of user. For balanced service to different user classes which employ disjoint bands for non-interference in overlapping beam areas, the number of beams devoted to each class of service should be inversely proportional to the spectral efficiency of the terminal modulation employed. Example throughputs and numbers of users were obtained for 100 coverage areas, 24 beams and 2.5 GHz, with only 100 MHz allocated for customer premises service. The bandwidth

efficiency of the FDMA modulation and the corresponding number of scanning beams are taken as the independent variables.

The FDMA modulation choice is important because MSK permits as many as 5 or 10 times more carriers in a given sampling bandwidth for an acceptable crosstalk level at the satellite compared with QPSK or staggered QPSK, for example. This is especially relevant for networks of many smaller terminals where symbol synchronization, frequency correction, and power control at the transmitters could be prohibitively expensive. On the other hand, single channel QPSK is a very bandwidth and power efficient modulation for the TDMA mode, as shown by figure 4.

Although on-board digital switching requirements do not dominate spacecraft technology, the square of the switch size implied by each realization is an important indication of processing complexity. Conditions for minimum complexity have been derived for both the digital and RF switches.

Use of Coding

Regeneration allows use of coding for uplink (and/or downlink) performance improvement with digital transmission. Since decoding and re-encoding would represent additional logic tasks for a processing regenerative repeater, extensive investigation of the improvement which might be provided through coding was accomplished. The analysis identified improvements ranging from 2.4 dB to 5.9 dB which are considered significant.

Measurements performed by COMSAT Laboratories have estimated the amount of degradation experienced in a satellite link for various backoff conditions of the ground station high-power amplifier (HPA) and low-power traveling wave tube amplifier (TWTA) in the satellite. Results for a bit error rate (BER) of 10^{-4} are given in table 3. The link degradation is measured as an increase in the required E/N_0 to achieve a given bit error rate. E/N_0 increases significantly as the amount of backoff decreases. This degradation is caused in part by amplitude modulation (AM) (induced by the action of band-limiting filters on the digitally modulated carrier) with the AM to phase modulation (PM) conversion of the amplifiers. Such PM degrades the performance of the coherent demodulation process and also interferes with carrier and bit timing recovery, resulting in significant degradation relative to the back-to-back (perfect channel) modem performance.

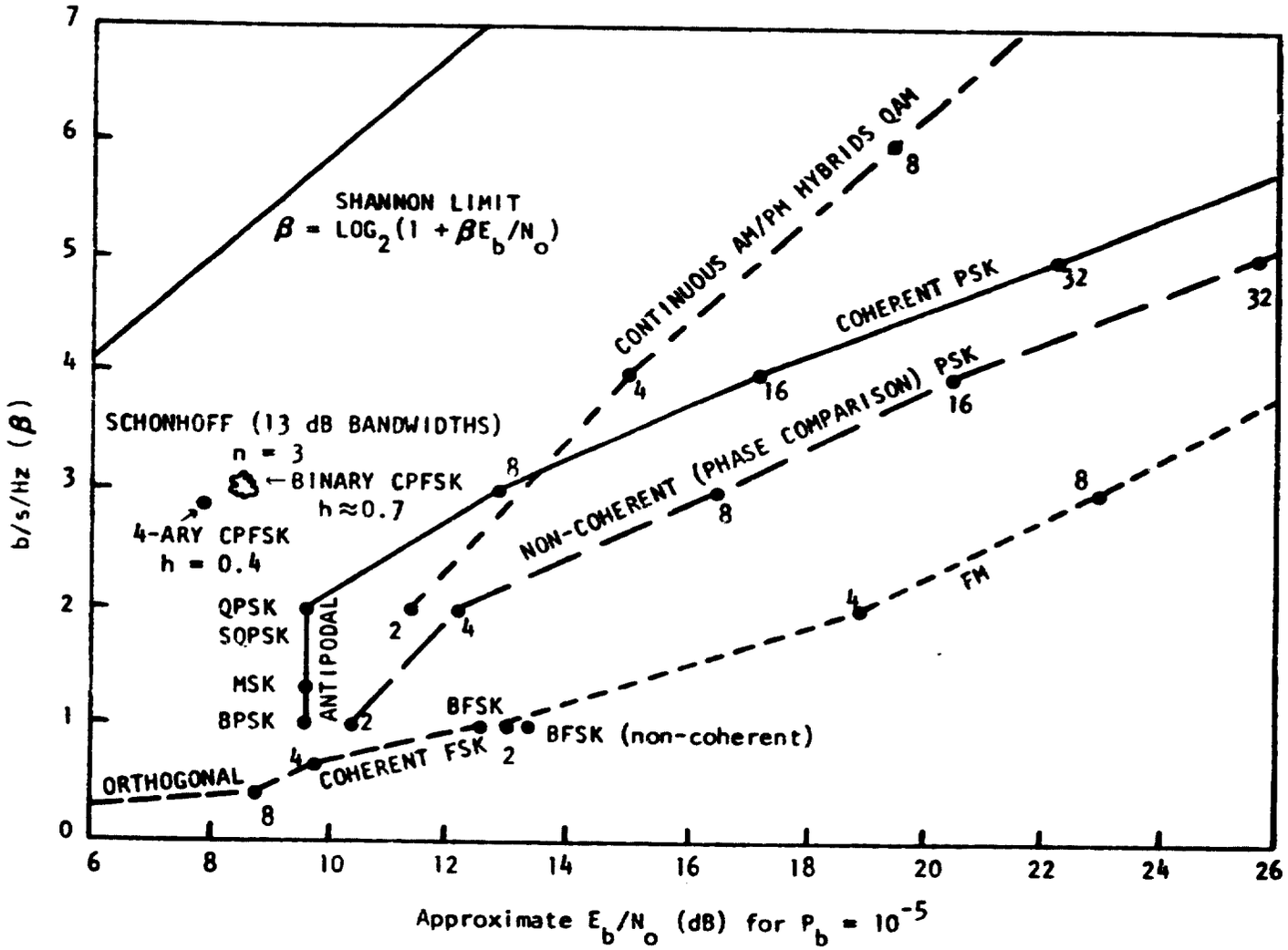

Figure 4. Single Channel Bandwidth-Power Tradeoffs for Various Modulation Schemes

Both hard decision processing (HDP) and decode encode processing (DEP), representing fundamentally different concepts, were studied. Plots of R_o* versus downlink energy-to-noise ratio E/N_o (ENR) for various TWTA backoff conditions are presented in the report. The interesting uplink versus downlink ENR curves for non-regenerative HDP and DEP repeaters were developed and are exemplified by figure 5.

Results of this type were used to develop the new results of table 4, which quantify the link improvement realizable through processing.

Table 3**

Link E/N_o Degradation Due to Terminal Transmitter HPA and Satellite TWTA Nonlinearities for Uncoded Links With a Conventional Repeater (BER = 10^{-4})

HPA Output Backoff (dB)	Satellite TWTA Backoff (dB)	Overall Degradation (dB)	HPA Degradation (dB)	Satellite TWTA Degradation (dB)
6	4	2.8	1	1.8
6	0	3.2	1	2.2
0	0	5.2	3	2.2

* R_o is a measure of channel capacity in bits/channel symbol and corresponds to a practical, reliable channel capacity achievable with an optimum coding scheme, assuming a particular modulation format, in this case M-ary orthogonal waveforms.
**S. J. Campanella, COMSAT Laboratories, analyzed digital regeneration techniques for single-carrier per channel, link performance due to ground station HPA and satellite TWTA; results presented with the author's permission.

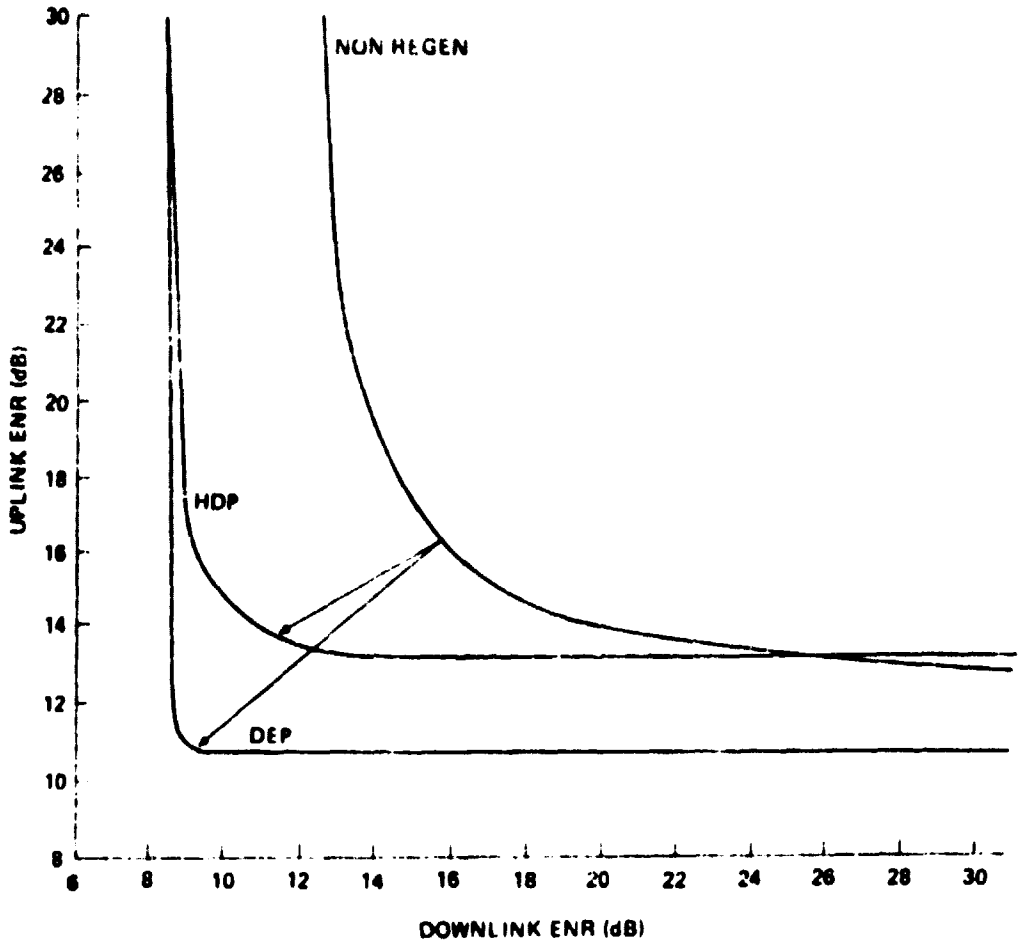

Figure 5. Performance Curves for Constant R_o of 1.4 Bits/Channel Symbol with HPA Backoff = 0 dB, TWTA Backoff = 0 dB

Table 4

Difference in Link E/N_0 Between Regenerative and Conventional Frequency Translating Repeaters (Uplinks and Downlinks)

HPA Output Backoff (dB)	Satellite TWTA Backoff (dB)	Uplink Difference HDP (dB)	Uplink Difference DEP (dB)	Downlink Difference HDP (dB)	Downlink Difference DEP (dB)
0	0	3.0	4.0	6.5	5.5
6	0	2.75	3.0	5.9	4.9
6	4	2.4	3.0	2.4	4.0

For all backoff cases examined, the operating points for a given performance level are significantly better for the regenerative repeater case than for the conventional repeater case. That is, the regenerative repeater results in either a greater fade margin or a reduced power requirement on both uplinks and downlinks. It should also be noted that the improvement is greatest for the 0/0 dB backoff case in which the HPA/TWTA degradations are also the greatest (from table 4). The regenerative repeater accomplishes its greatest improvement when the degradation encountered for the conventional case is the greatest.

System Control

Demand assigned multiple access (DAMA) schemes vary according to switching technique (circuit, message, and packet), and method of control dispersal (central, distributed, or hybrid). Figure 6 represents the universe of all possible DAMA schemes and indicates the character of the known existing and planned DAMA systems, both commercial and military. All possible systems have not been realized as indicated by the voids on the chart.

Two alternatives for system control are suggested for the wideband satellite communications system of this study. The first is a conservative call establishment protocol which is based upon circuit switching and centralized control. The second alternative is a more advanced destination variable demand assignment technique based on non-store and forward message/packet switching and hybrid or decentralized control. At present, there are no DAMA systems of this nature, as indicated by figure 6. NASA may wish to pursue the

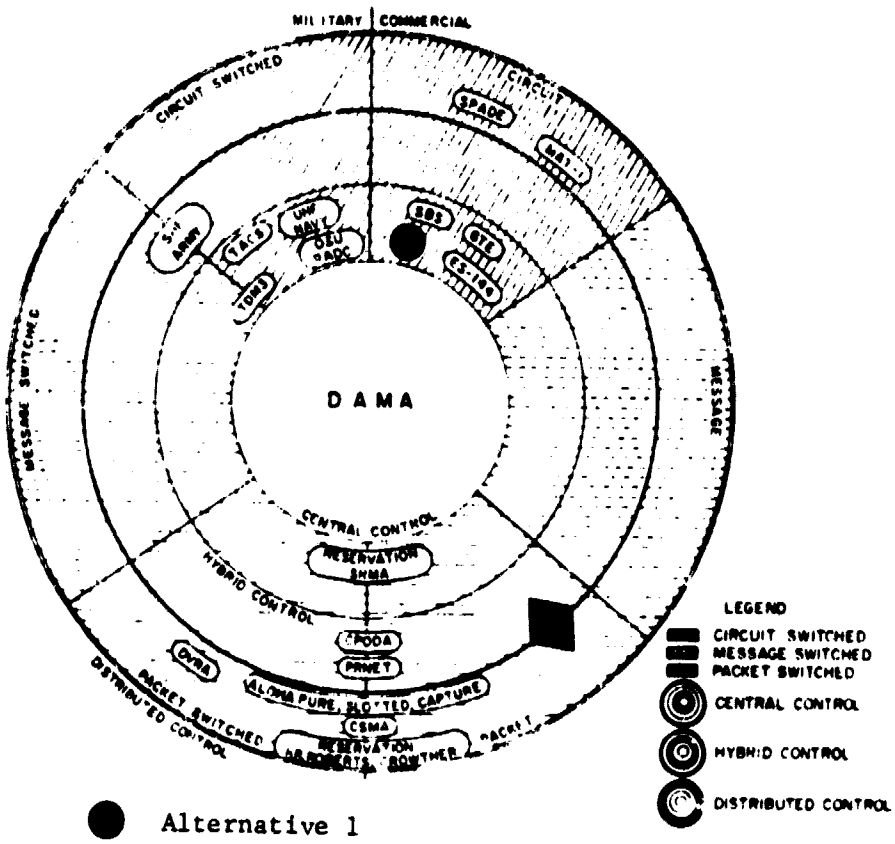

Figure 6. DAMA System/Application

second alternative if it proves to offer more efficient use of the satellite channel and improved control flexibility.

This destination variable assignment scheme involves the immediate retransmission of a message/packet where the header is stored and recognized, provided that a free outgoing channel is available. Message/packet buffering is required only if all outgoing channels are busy. Although an end-to-end system delay model has been defined, further analysis would be worthwhile.

The performance of the first alternative, for blocked calls cleared and delayed models, has been analyzed to a greater extent in terms of the number of circuits vs. utilization for a given blocking probability. Figure 7 shows the results for the blocked calls cleared model. Here utilization means load carried per circuit and blocking probability is equivalent to grade of service. The dashed lines show typical values for a 1% grade of service.

LARGE SCALE BROADBAND SATELLITE MICROWAVE SWITCH

For high capacity through frequency reuse, a satellite having time division multiple accesses switched among spot beams has been suggested. A study was performed of a large scale (100 x 100) broadband, crossbar function, microwave switch to be used on a satellite operating at 30/20 GHz.

First the implications of switch operation in a multibeam, frequency reuse, TDMA repeater satellite were studied to determine a specification for the switch. For the purpose of exploring design issues, a size on the order of 100 x 100 was justified by observing the existence of 73 metropolitan areas in the United States with populations over half a million.

The operation of a TDMA frame and slot timing scheme fitted to the changing traffic demand set several operating switch parameters, including a switching time no greater than 50 nanoseconds. A preliminary switch specification was determined and is presented in table 5. The rationale for some of the parameters is summarized below.

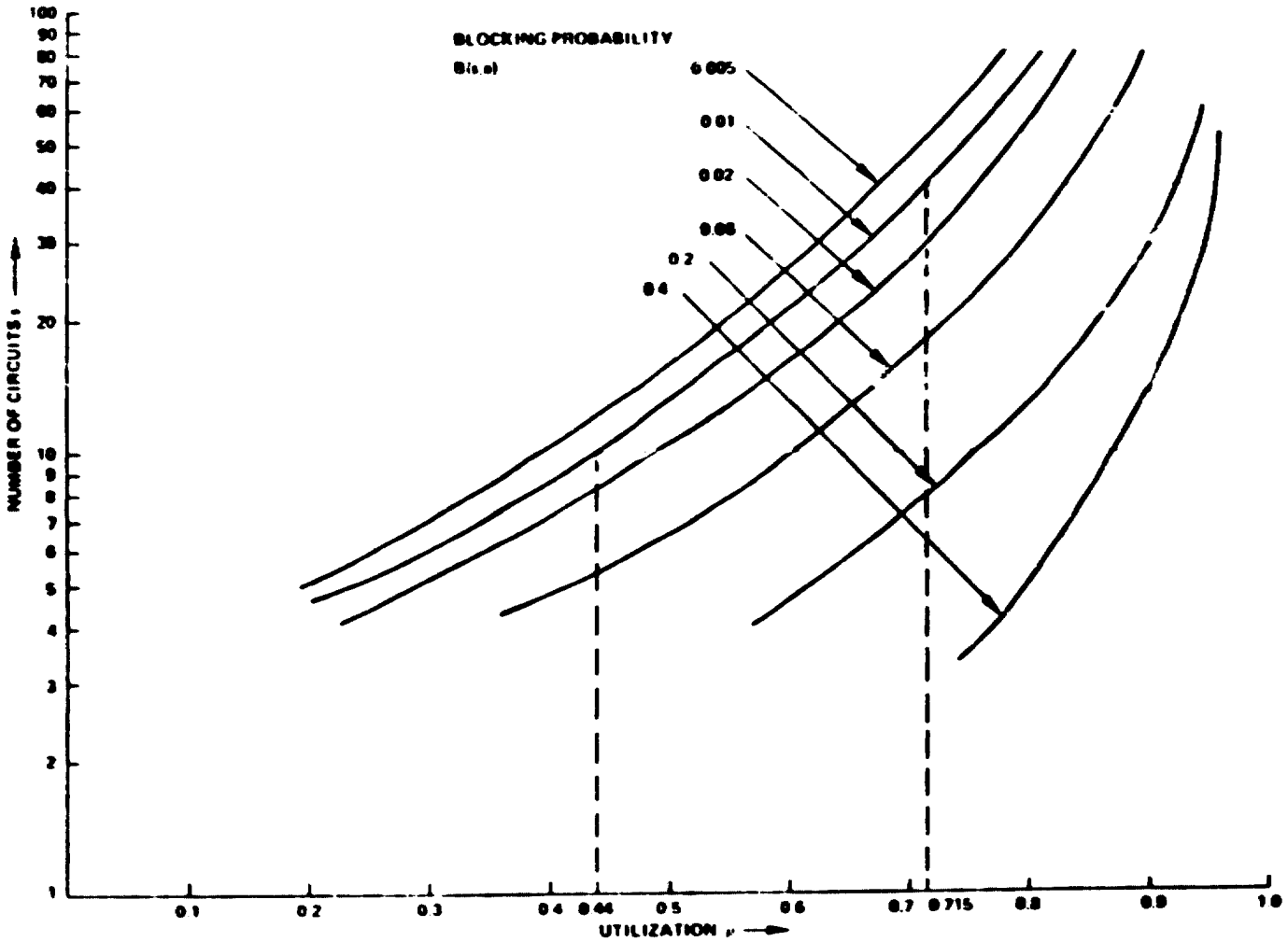

Figure 7. Blocked Calls Cleared Model Performance

Table 5

Tentative Satellite RF Switch Specifications

Size, n, (input/outputs)	100 x 100
Bandwidth (channels, connections)	2.5 GHz
Switching Time	50 ns maximum
Mode of Operation	TDMA
Frame Duration	125 μs
Slot Durations	Proportional to traffic, unequal
Frame/Slot Schedules	reconfigurable
Slot Size	2 μs minimum
Slot Communications Efficiency	85 percent
Switching Occurrence	independent times
Accessibility	to any unoccupied output
Interruption of Estab. Conn.	none due to switching
Signal Flow, at Unmade Cross Point	input, output signals bypass it
Input Power Level	1.0 mW per channel
Switch Isolation Coefficient, A (closed/open)	S/C** + n (in dB)
Attenuation Var. (f) (WB)	±1.0 dB/2.5 GHz maximum
Attenuation Var. (f) (NB)	±0.5 dB/10 MHz maximum
Insertion Loss Absolute	50.0 dB maximum
Insertion Loss Variation	6 dB port to port maximum
Group Delay Var. (f) (WB)	±1 ns/2.5 GHz
One Port to Many Connectivity	provided
Redundancy	sufficient to overcome failure rate
Prob. of Success*	99.99 percent, 7 years

* Probability of success is probability that any input port can be connected to any output port, even with some crosspoint failures.
**S/C is a signal-to-crosstalk or coupling ratio.

Switch architecture was explored in detail. Fan-out, rearrangeable, phased array, and crossbar architectures were considered. Rearrangeable architecture was found unsuitable for TDMA, and fan-outs were found to be too large and heavy. Phased arrays were shown to require multiple duplication of the entire array except for radiators when used for switching, and to require components not realizable as passive elements for frequency reuse.

Crossbar RF switch architecture, before thought difficult to achieve in microwave construction, was found to be smaller, lighter, and the most reliable. A new method of constructing a microwave crossbar* is presented in figure 8. Signal inputs enter the switch via microstrip lines from the left. These are printed on an upper layer. Signals which have been connected by switches leave in an upward direction via microstrip lines printed on a lower layer. The switches are at the mid-points of directional couplers which sample signals from input lines and couple them to output lines if the switch makes the connection. Half the coupler is in the upper layer and half in the lower. The two halves are connected by a feed-through with a switch in series. If the switches take the form of amplifier devices, failure of an amplifier at a cross point will not seriously degrade the signal-to-crosstalk ratio of other output signals; thus, only a single cross point will become inoperative. Due to the typical requirement for seven-year life for a spacecraft component, 13 failures are estimated since there are 10,000 (i.e., 100 x 100) cross points. Inability to make a connection from any input port to any output port might represent a stringent definition of switch failure.

To prevent the failure of one switching device from causing a failure of the overall RF switch, two features are provided. First, a few extra ports at input and output can be used and substituted for failed paths. Second, a feedback or wraparound technique allows a signal to pass from an input to an operative output port and back through the RF switch a second time through another input port which is connected to the desired output port. Thus, a backup is provided for expected device failures by means of wraparound techniques so that connection can be made despite the anticipated small number of cross point failures.

*Patent Applied For.

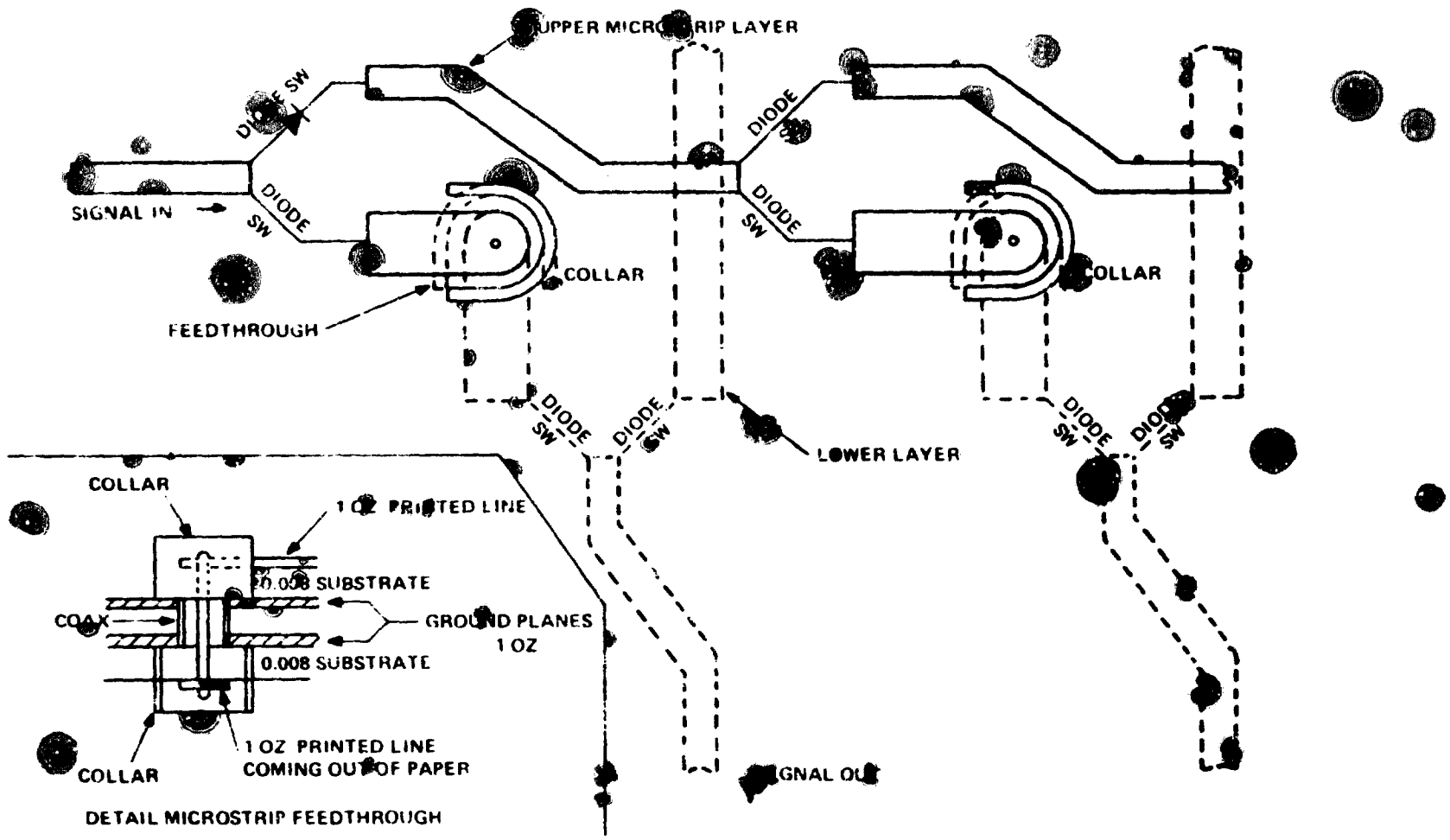

Figure 8. Physical Cross Bar and Feed Throughs

A recommended input signal level to the switch ports of 1 milliwatt was determined. It was found that the total switch insertion loss could be as high as 60 dB but the isolation, I, at any switch cross point must be given in dB as:

I = desired signal-to-crosstalk ratio + number of input switch ports (all terms expressed in dB).

For a 30 dB desired signal-to-crosstalk ratio and a 100 port switch, the isolation specification is 50 dB.

An investigation of device switching technology covered diodes, ferrites, optical switches, and MESFETs. Diodes and MESFETs were found to be the most applicable with MESFETs offering a greater return in reduced weight, power requirements, and component numbers. Their speed and reliability were also superior. MESFETs require further research and development (R&D) for optimization, whereas PIN diodes are mature. But, MESFETs offer so many advantages over PINS that R&D should be undertaken to secure the benefits which MESFETs promise.

The investigations conducted brought RF switching to focus, deduced preliminary requirements, provided an architecture and switch organization, and a summary switch specification. Switching device technologies, provision of system broadcast capability, switch control, and reliability were also studied and conclusions provided.

The RF switch study reached the following specific conclusions:

- A crossbar architecture is superior and should be used.
- A coupler crossbar realized in microstrip is the lightest weight and most reliable design identified and should be given in-depth study.
- A MESFET should be used as the switching element.

It was recommended that an analytical study of RF circuit performance be made in conjunction with a switch layout and construction; and that MESFETs should be optimized for switching.

BASEBAND PROCESSOR IMPLEMENTATION AND TECHNOLOGY

The rapidly advancing art of microprocessors should make feasible a microprocessor-based regenerative on-board processor for a future system serving smaller users and having rates less than T1. Consequently, we have emphasized this approach (as opposed to hardware demodulators and remodulators). The conceptual baseband processor design is illustrated in figure 9. It consists of demodulators and functional processors arranged on a bus architecture, and downlink demodulators. These units are described below.

Demodulation Processor Module

The pre-processed FDMA signals from each beam serve as the input to the demodulation processor module. This module contains M demodulators; one for each FDMA channel. The data demodulators are conceived as essentially all-digital programmable units whose input intermediate frequency (IF) signal is switch-selectable from a subset of individual FDMA channel downconverters by the master controller. All uplink demodulators have identical capabilities and are interchangeable. Bit timing acquisition time goals of 1 to 2-bit intervals are assumed to minimize overhead.

Other inputs are:

- o Operating rate control: at T1, K x T1, T2, or K x T2, rates are minimum where K is the scanning beam frame period/dwell time ratio.

- o Frame sync and burst sync word inputs, for synchronizing the start of actual data reception, are loaded once per frame and stored in holding registers. High-speed multi-bit digital comparators are used to perform detection tasks.

Outputs include:

- o A start-of-data or data valid flag signal marking the data portion of each burst, which enables clocking of the data into the input serial-to-parallel register.

- o Bursts of synchronous clock and data are coincident with the above flag. Rates are T1, K x T1, T2, or K x T2 b/s.

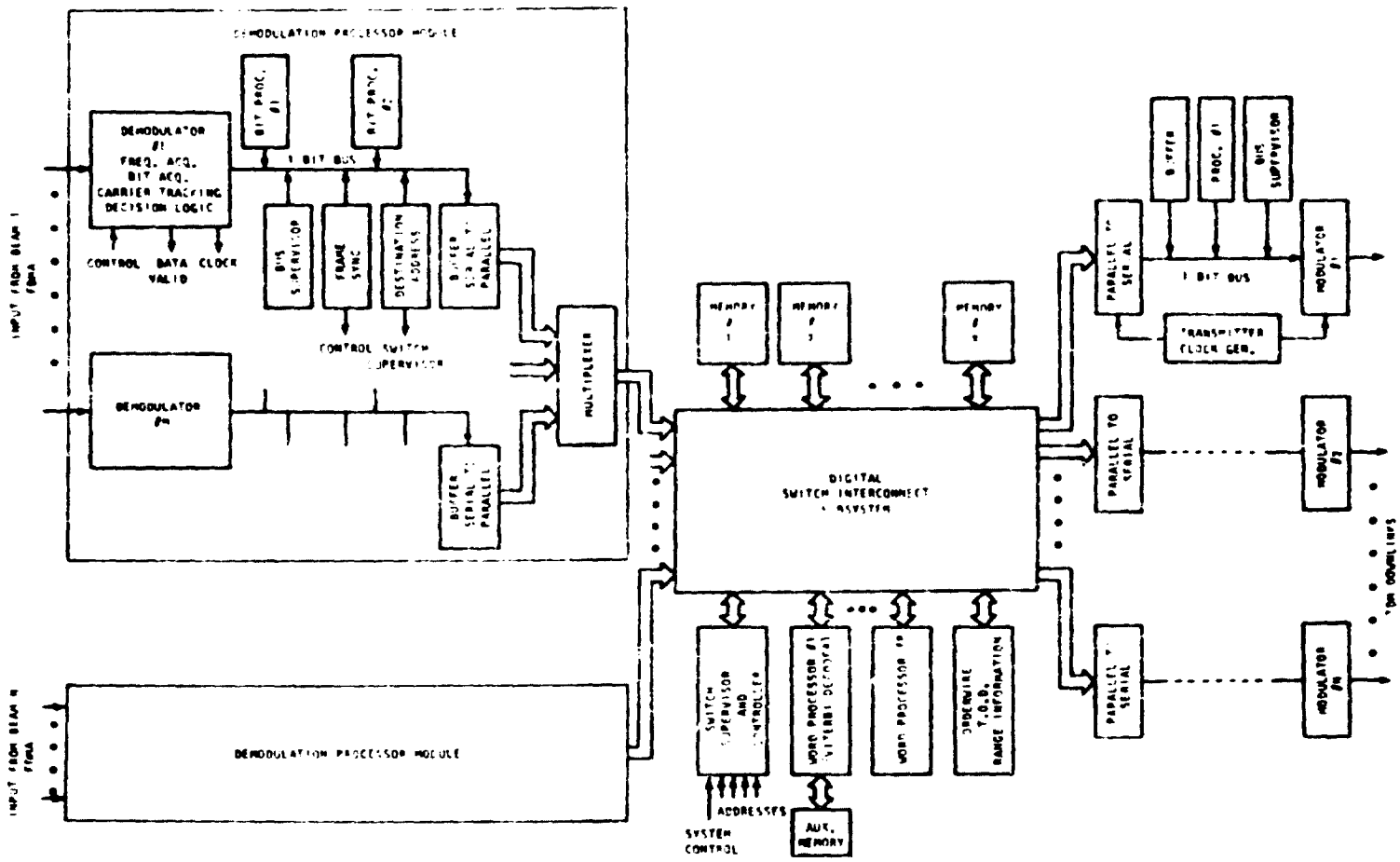

Figure 9. Baseband Processing System

The output of the demodulators feeds a one-bit bus on which hang additional bit and function processors. Bit processors are programmable and perform specific operations such as de-interleaving of the bit stream. Other special functions required by a specific link can be provided as required. The serial bit stream is buffered and converted to a parallel stream of information words. The buffer, which is a part of each demodulator unit, consists of three components:

- o Serial input to parallel output (SIPO) register, b bits in length (b_n = (sL)/n where (sL) is the number of bits/burst and n is an integer).

- o A b_n bit clock counter which transfers the contents of the SIPO register to a b_n bit wide parallel holding register at the end of each clock interval.

Clocking rates range from T1 to K x T2; if K = 10 is assumed as an example, clocking would occur at 63.12 Mb/s (10 x 6.312 Mb/s). Shift registers and counters capable of operating at this speed are readily available using Schottky or emitter-coupled logic (ECL) families. Because of the lower clocking/transfer rate, the b_n bit holding register can be made from regular transistor-to-transistor logic (TTL) devices.

Microprocessors attached to the switch handle the data transfer between demodulators and modulators and the memory which is partitioned for each link. The connectivity algorithm used to drive these microprocessors is obtained from a central processor which receives assignment information from the ground control station via the command and control link.

Processing speeds for T1 and T2 scanned-input (uplink) data handling are considered low to moderate. Processing rates are reduced by serial-to-parallel (S/P) conversion circuitry, since it would be prohibitive to handle all uplink data bits on a bit-by-bit basis. Multi-bit word transfers to memory can be accomplished in 50 ns or less using currently available bipolar random access memory.

Downlink Modulators

Data destined for a specific downlink are passed from memory to the respective modulator through the switch as a series of information words. A parallel-to-serial (P/S) shift register converts the words in serial bit stream. Data are passed along a one-bit bus to the modulator. Here, as with the uplink, one-bit

processors are available to perform specific functions required by the link.

TDM downlink processing speeds are high. In a typical case, the translation from N uplink beams, each with M FDMA channels to N downlink beams using TDM, causes the downlink channel rate to be at least M times the uplink rate. If a downlink is scanned, the rate goes up by the ratio of scan frame time to user dwell time, K. For values of 10 for M and 100 for K, the downlink rate for T2 carrier approaches 1000 times the uplink rate (~6 Gb/s) which may be feasible in the future.

P/S circuitry aids assembly of data words unloaded from the user address in the common memory for downlink transmission. Word transfer takes place at a very high rate, which can only be accomplished by the use of wide words in the memory organization of the processor. Wide-word memory organization reduces output processing data transfer rates to small values.

Memory Requirements and Technology

A large high-speed memory is required in the processor section. The quantity is dependent on the total uplink capacity received per master system timing frame and the amount of delay incurred in the satellite before beam connectivity is established.

As an example, assume a beam, composed of 10 FDMA channels each with T1 data, scanning 100 uplink beam coverage areas during a frame of 10 msec; storage required for a whole frame is at least 15.44M bits (100 areas x 10 channels/beam x 1.544 Mb/s (T1) x 0.01 s).* For a double buffer arrangement, the bulk memory would be twice this value or 30.88M bits. This amount of memory is moderate but the 15.44M bits must be transferred in 0.01 seconds which is a 1.544 Gb/s link transfer rate.

For one T1 channel per user, 15,440 (1.544 Mb/s x 0.01 seconds) user bits (not including overhead) are received during each master frame. The basic buffer portion of the bulk memory for this user would probably have to be at least twice the calculated size because

*The bit sizes and transfer rates would be reduced by an order of magnitude with the currently favored 1 ms frame period.

of processing delay. The uplink is received continuously and must store a frame of data before sending it down as a high-speed TDM burst. A basic user memory storage allocation is therefore 30,880 bits. The bulk memory would then be organized into 1000 blocks.

The output from all demodulator buses is multiplexed into a single stream of information words and passed to the digital switch interconnect subsystem.

Digital Switch Interconnection

The switch interconnection subsystem, which is the core of the processor, performs the function of interconnecting the various elements of the processing system. The switch is assumed to operate in a time division mode with interconnection between devices determined by the switch supervisor. Address information is obtained from the demodulation processor module and from the switching algorithm provided by the ground control station.

Memories 1 to R are used to organize the uplink data according to their destination. While data are in the memory, further operation can be performed on them by the word processors attached to the switch. Functions such as decoding, re-encoding, automatic request (ARQ) strategies, and one-to-many type transmission can be handled by the word processors.

Maximum obtainable density in memories is directly related to the memory circuit (one, two, or three transistors per bit) and power dissipation ratings of the package. Very high density (64K) NMOS memories which require periodic refreshing of the data every one or two milliseconds have been designed using one transistor per bit. Static memories (not needing refreshing) are usually less densely packed (two or three transistors per bit) and are available in a 4K configuration. Current packaging designs are limited in overall power dissipation capabilities. Typically, common integrated circuit packages are rated at 1 W dissipation or less. Larger package designs, containing multiple chips or a larger high-density die, are being investigated by several manufacturers. Gigabit memories suitable for spacecraft application are described in a brief article presented at the 1978 International Telemetry Conference.

Logic Speed Requirements

The power-speed product is an important figure of merit for logic devices or arrays made from the various gate technologies (TTL, ECL, NMOS SOS, I^2L, GaAs FET). The power-speed product is usually expressed in picojoules and is formulated by the product of the power dissipation of the simplest gate function developed for the technology involved and the propagation delay from input to output through the gate. Power-speed products as a function of gate delay for various current logic families are presented in figure 10. Logic devices will have to be manufactured as arrays to minimize capacitance effects and reduce switching speeds below 1 ns.

SELECTED CONCLUSIONS

- High gain satellite antennas capable of handling tens of simultaneous beams for the efficient reuse of the 2.5 GHz wide 30/20 frequency band are necessary; several scanning beams are recommended in addition to fixed beams.

- Low power solid state 20 GHz GaAs FET power amplifiers in the 5W range should be developed.

- An RF switch with in the order of 100 input/output ports for 500 to 600 MHz wide trunking channels is suggested to advance the state-of-the-art.

- On-board transmultiplexing of frequency division multiple access (FDMA) uplink and time division multiplex (TDM) downlink customer premises channels consuming a few hundred MHz of bandwidth and with data rates in the order of 15 mb/s per beam is suggested.

- A general-purpose digital baseband processor with gigahertz logic speeds and megabits of memory is recommended.

- Commensurate RF trunking and customer premises terminal technologies are recommended. The minimum satellite weight and lower terminal transmitter power obtained by optimum system design imply an estimated $300M system cost savings with 5000 customer premises terminals.

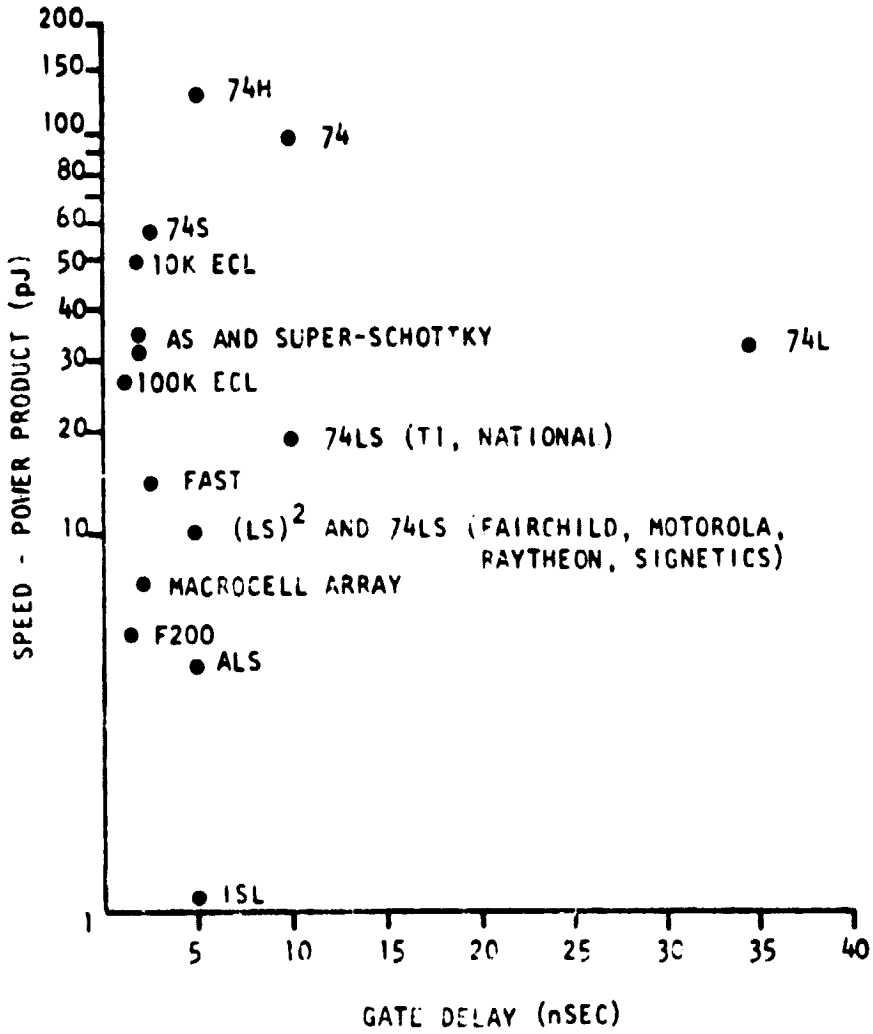

Figure 10. Speed-Power Product for Various Logic Families [Ranada, 1979]