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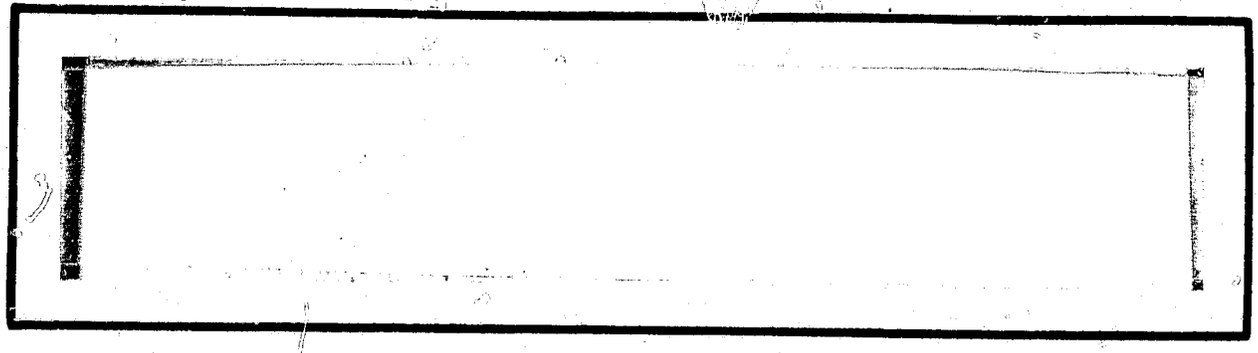

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(NASA-CR-160661) CRITIQUE OF THE HUGHES AIRCRAFT SHUTTLE Ku BAND LEADING EDGE BIT SYNCHRONIZER Interim Report (Axiomatix, Los Angeles, Calif.) 17 p HC A02/MF A01 CSCL 17B G3/32

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CRITIQUE OF THE HUGHES AIRCRAFT SHUTTLE KU-BAND LEADING EDGE BIT SYNCHRONIZER

Contract No. NAS 9-15795B

Interim Report

Prepared for

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Houston, Texas 77058

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Axiomatix Report No. R8005-2
May 5, 1980

1.0 SUMMARY AND CONCLUSIONS

A bit synchronizer proposed by Hughes Aircraft (Culver City) is analyzed via timing diagrams in a noise-free environment. This synchronizer is, in part, a substantial revision of the bit synchronizer proposed by P. H. Conway [1] of Hughes Aircraft Company (HAC).

Based on a review of a HAC note [2] and the timing diagrams of Figures 2 through 9, it is believed that this new bit synchronizer will track the rising edge of the data bits with 25% asymmetry and up to a 90° phase shift between the received clock and data bit timing. In addition, the data bits will be demodulated correctly.

It is not true that phase shifts larger than 90° will necessarily be corrected by this bit synchronizer, as evidenced by Figures 8 and 9. However, the specifications currently require the loop to operate over only a ±75° phase shift between the received data stream leading edges and the bit synchronizer leading edges; consequently, there should be no problem.

2.0 INTRODUCTION AND DESCRIPTION OF THE LEADING EDGE BIT SYNCHRONIZER

The purpose of the bit synchronizer, shown in Figure 1, is to track the leading edge of the incoming bit stream with the aid of the received clock and, from this, to regenerate a symmetric bit stream to be processed by the convolutional encoder. In addition, the synchronizer provides a clock at the data rate as well as twice the data rate.

In Figure 1, two additional subsystems are shown; the first is an adaptive threshold device that attempts to restore symmetry to the bit stream, and the second is a false frequency lock detector. Since the asymmetry corrector will be the subject of another report, we will now discuss the false frequency lock detector.

The purpose of the false frequency lock detector is to ascertain whether the bit synchronizer is in true lock or false frequency lock. This is accomplished by counting both the received clock and the synchronizer-generated clock in two separate 8-bit counters. After either one counts to its maximum count of 256, the other counter is inhibited from further counting. At this point, the count of the unfilled counter is compared to 256. If the error is small enough, true lock is accepted;

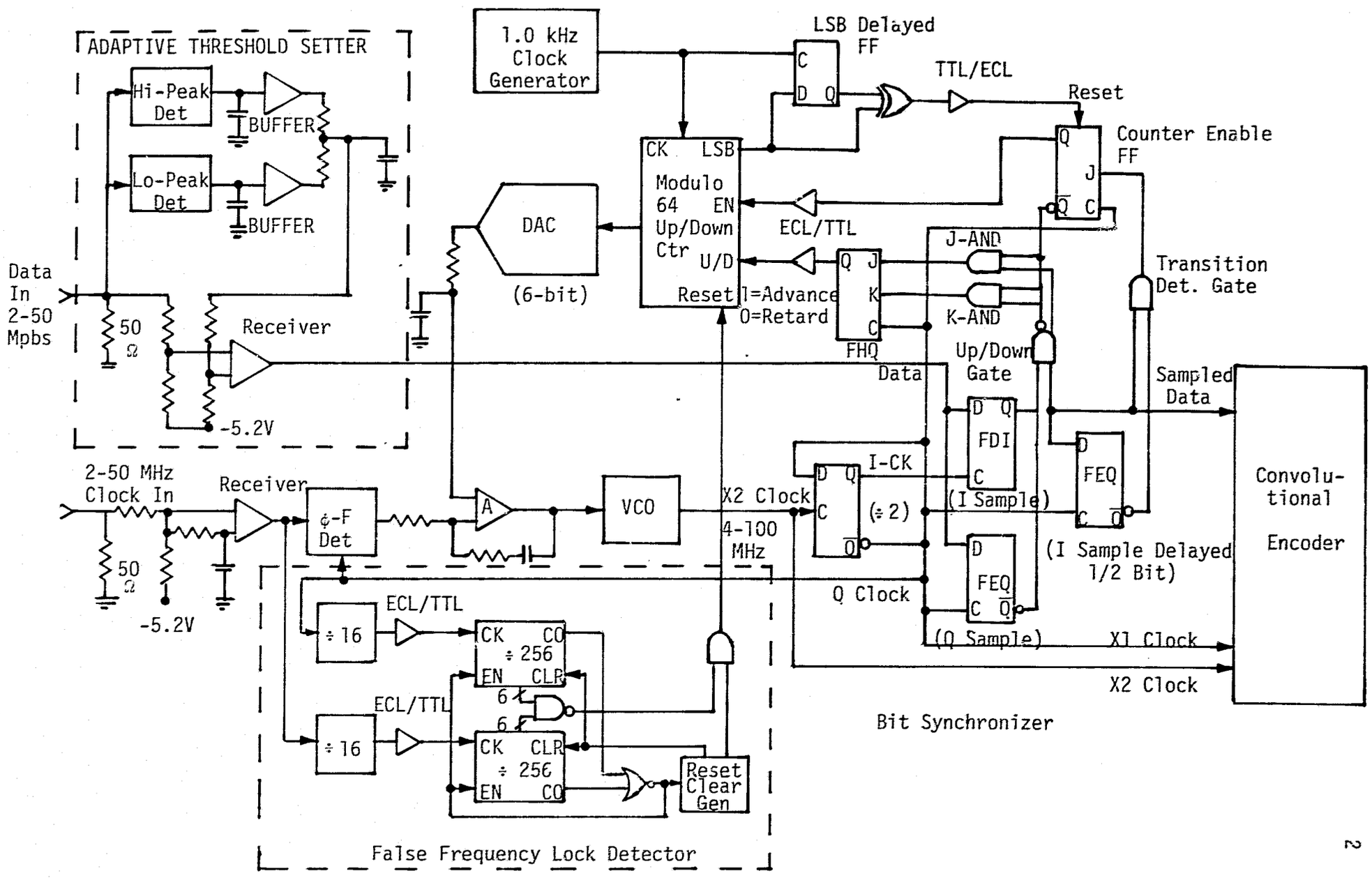

Figure 1. Hughes Culver City Ku-Band Bit Synchronizer Block Diagram

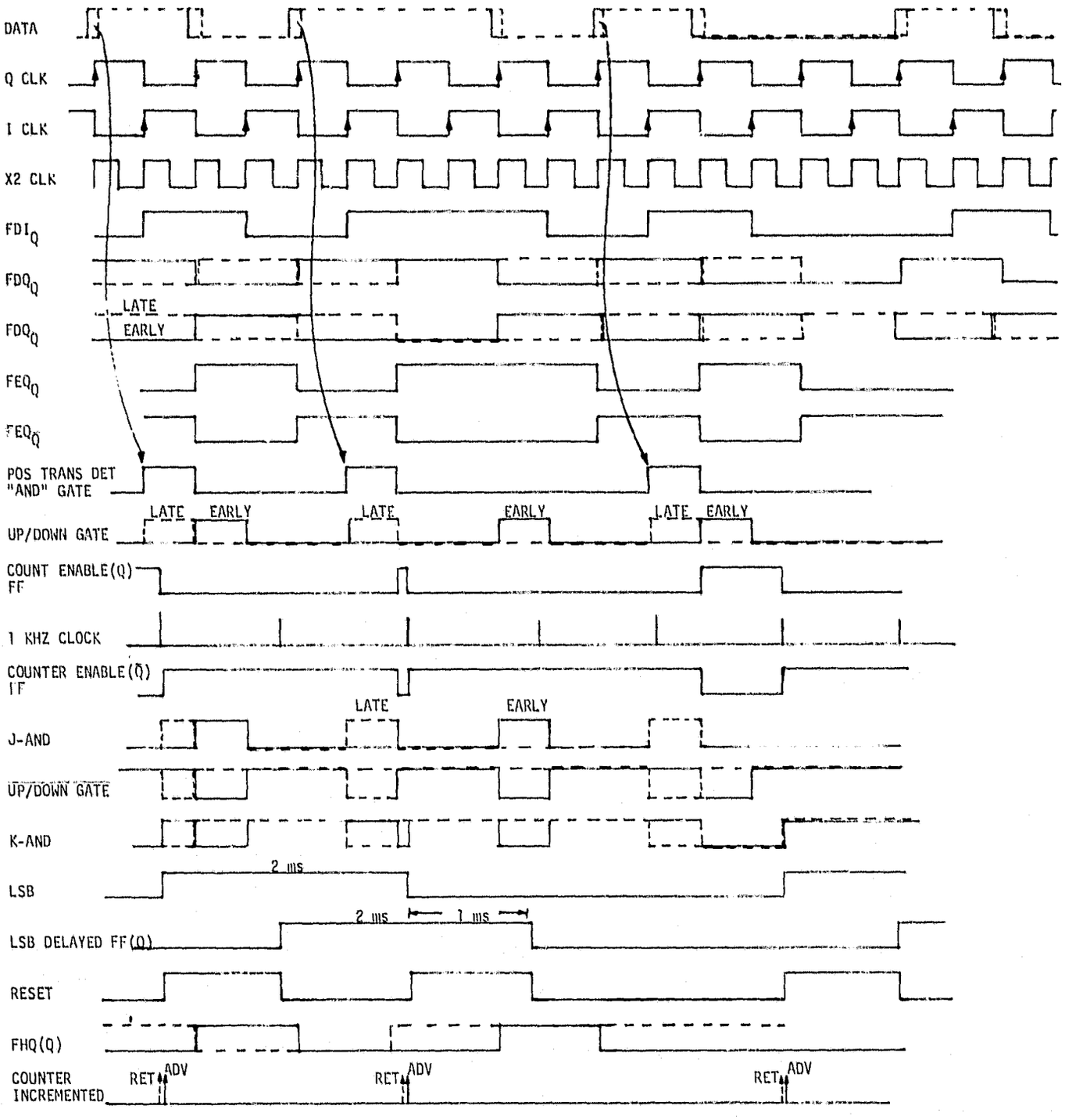

Figure 2. Timing Diagram of the Bit Synchronizer Illustrating An Early and Late Bit Sequence For the Culver City Ku-Band Bit Synchronizer

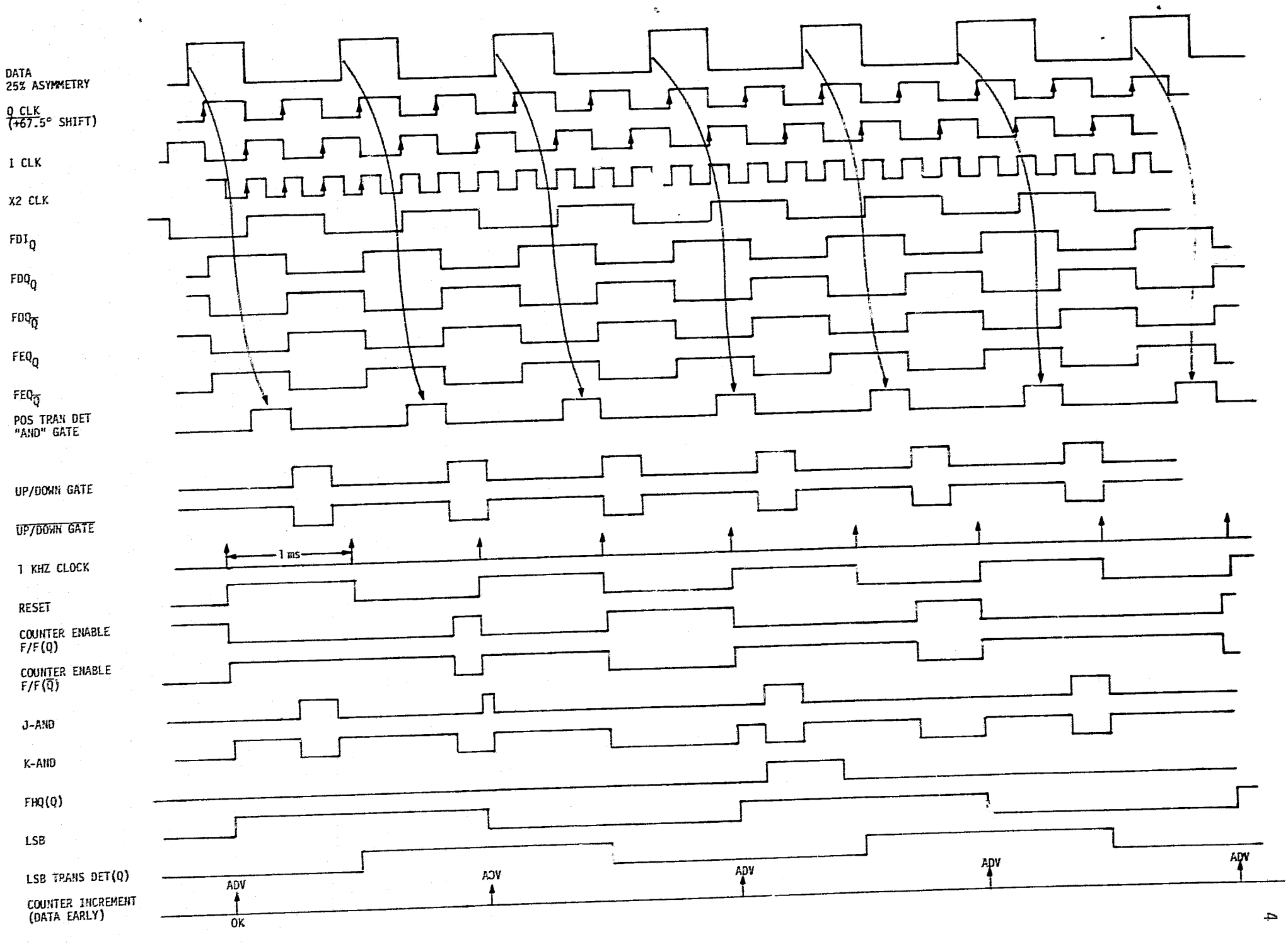

Figure 3. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Leading the Q-Sampler by 67.5° (Results Hold Up To 99°)

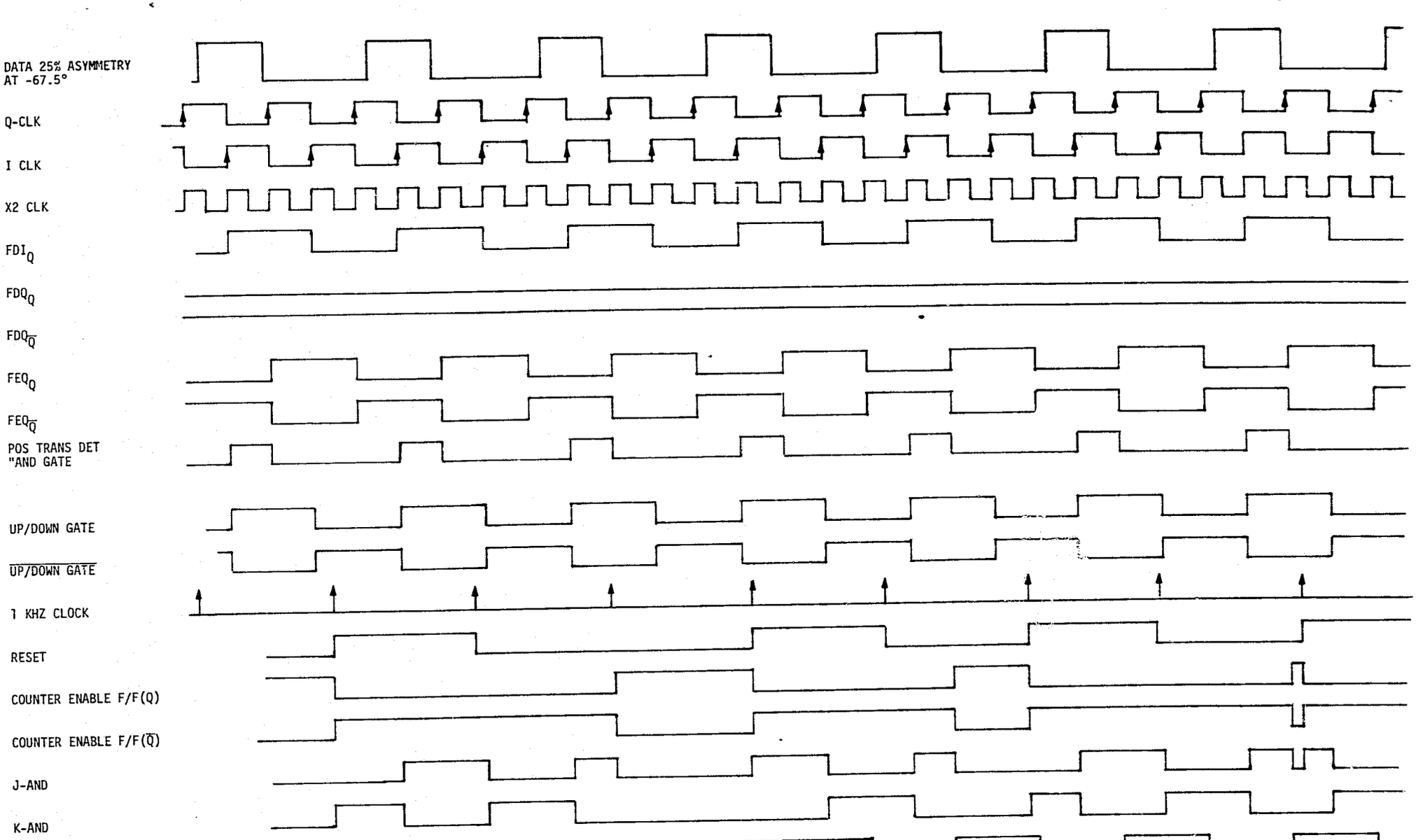

Figure 4. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Lagging the Q-Samples by 67.5° (Results Hold Up to 90°)

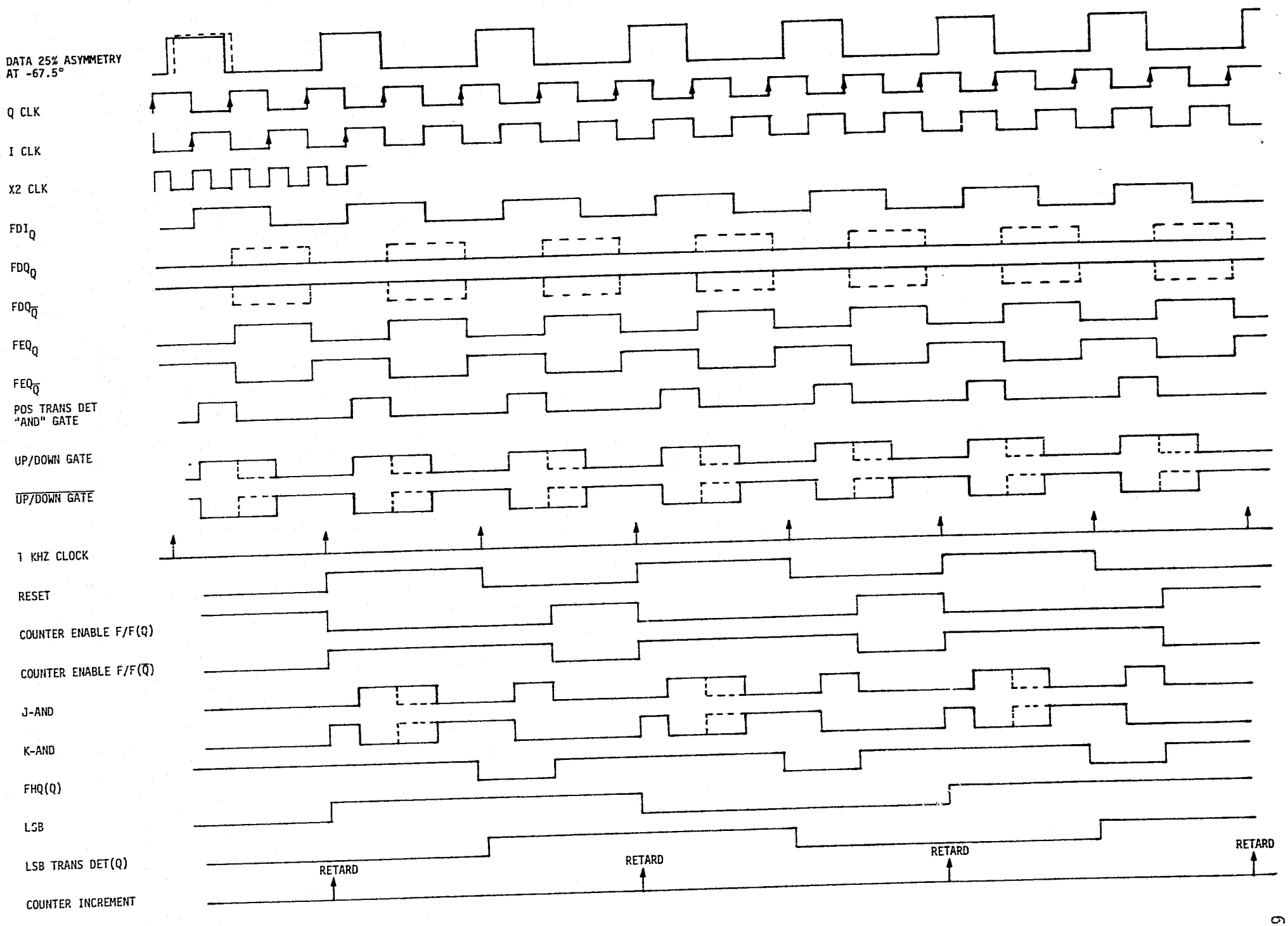

Figure 5. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Lagging the Q-Samples by 67.5° (Different 1 kHz Clock Phase Than That of Figure 4)

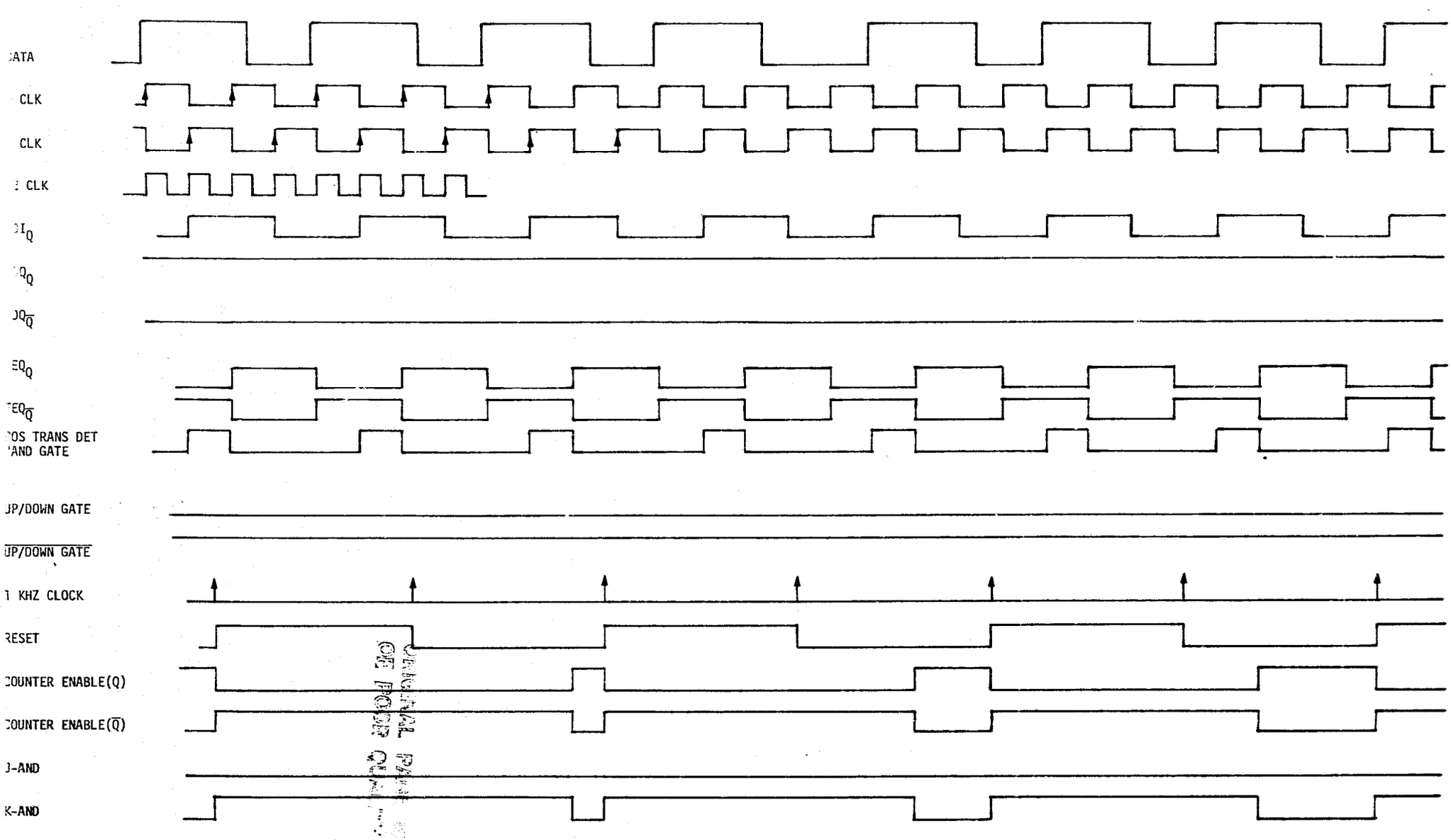

Figure 6. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Leading the Q-Samples by 22.5°

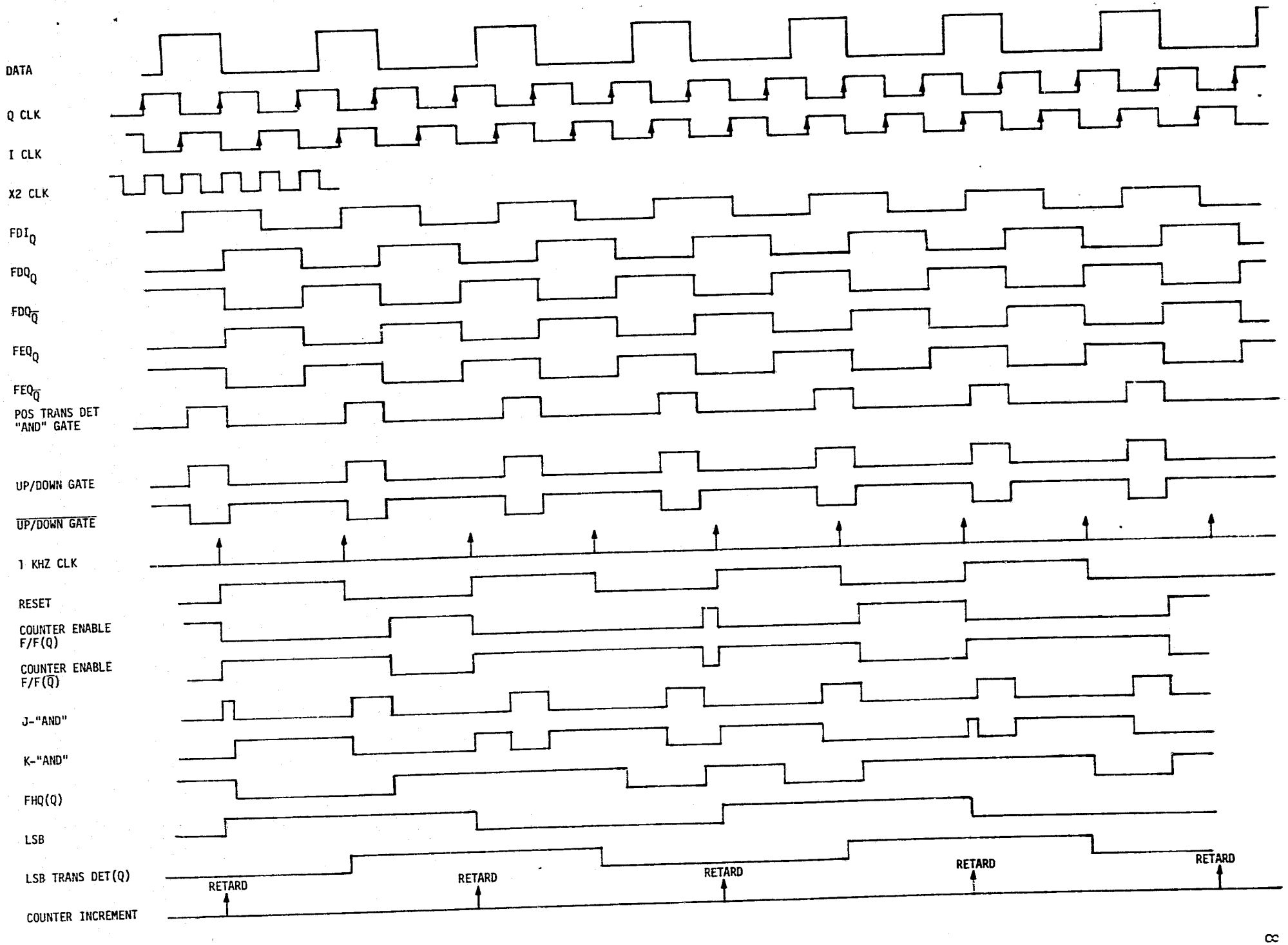

Figure 7. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Lagging the Q-Samples by 100°

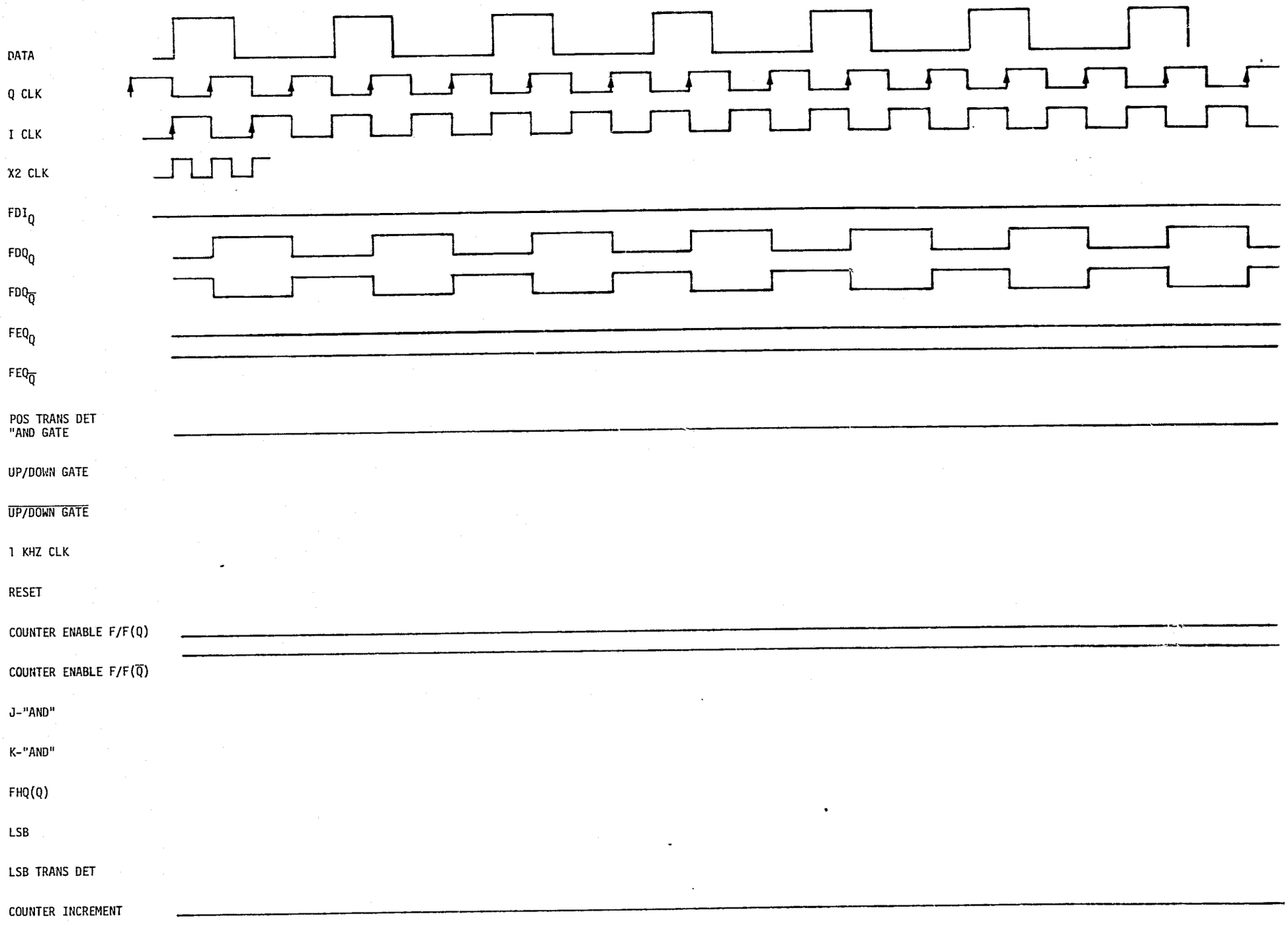

Figure 8. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry with the Data Lagging the Q-Samples by 190°

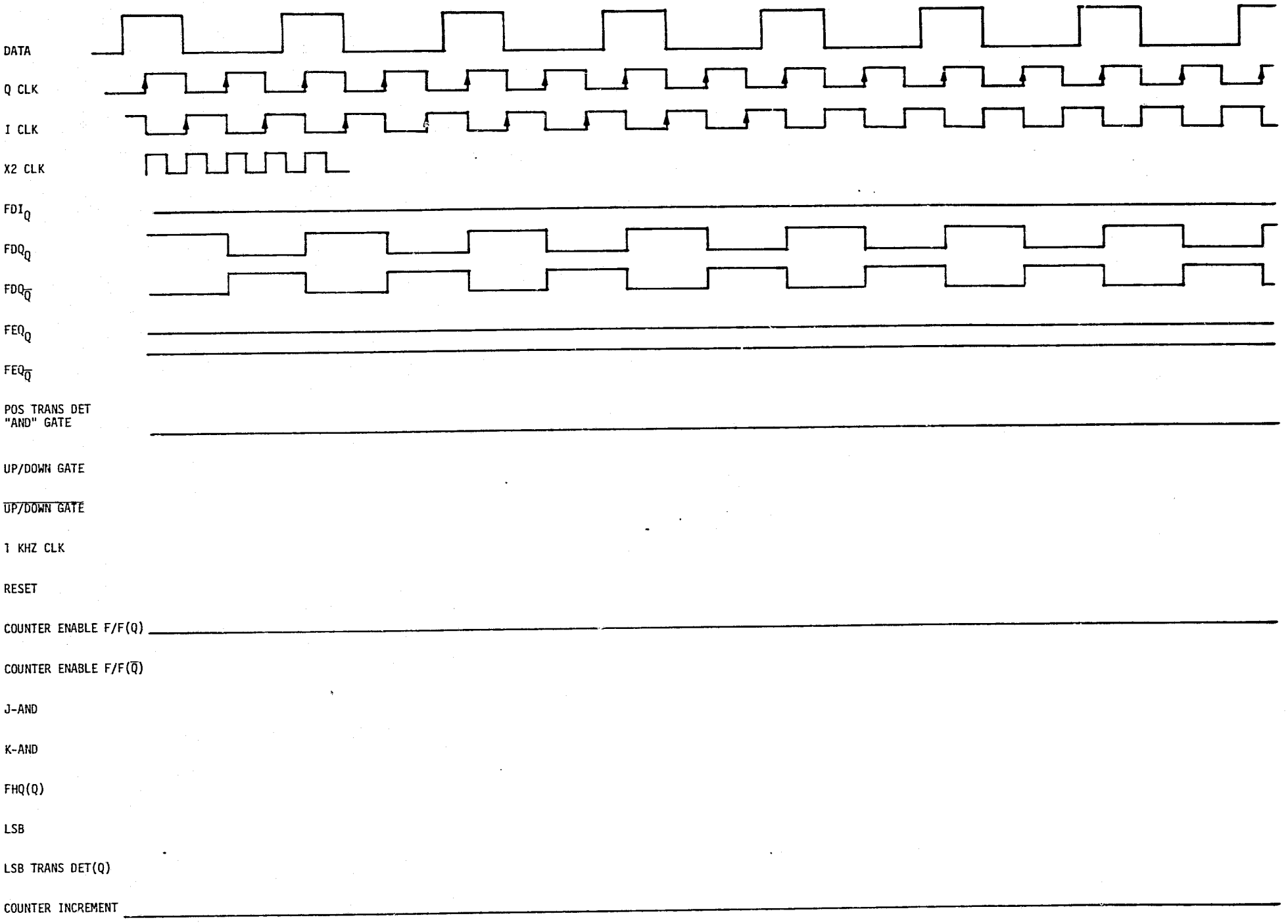

Figure 9. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Leading the Q-Clock Leading Edge by 100°

otherwise, false lock is assumed. If false lock is detected, the digital-to-analog converter (DAC) voltage is set to provide 0 DC bias into the loop filter, which allows the loop to reacquire in true lock.

The bit synchronizer loop is composed of a Motorola high-frequency phase-frequency detector (ϕ-F) [3-4] which is capable of detecting both phase and frequency errors and is used to track the received clock, as well as a bit timing detector, based on positive data transitions.

The phase-frequency detector has been discussed in some detail in [1] and will not be discussed here except to say that its function is to act as a discriminator in a frequency lock loop during frequency acquisition and as a phase detector during tracking.

In effect, the ϕ-F detector removes the frequency error between the VCO and the received clock, then removes the phase error. The function of the flip-flops, least significant bit detector, and counter-DAC unit is to position the clock-generated bit timing so that the Q-clock straddles the leading edge of each bit.

The VCO is run at 4-100 MHz and divided by 2 by the D flip-flop (F/F) following the VCO. From the $\overline{Q}$ output, the Q-clock is generated and, from the Q output, the I-clock is generated. Flip-flop FDI then provides samples of the I sample (mid-bit samples) whereas FDQ outputs the Q samples (or transition samples). The function of FEQ is to delay the I sample by one-half of one bit so that the positive data detector gate will go high when a positive transition occurs. The up/down gate, along with the J-AND and K-AND gates, set the JK flip-flop so as to increase or decrease the counter count and, therefore, the DAC voltage. This voltage is subtracted in the loop filter amplifier, thereby adjusting the loop VCO phase relative to the received clock phase. Both the Q-clock and the X2 clock, plus the resynchronized data, are sent to the convolutional decoder. The function of the least significant bit transition detector is to provide a settling time of 2 ms before a new update can be processed.

Now consider Figure 2, which illustrates how the loop provides corrections so as to align the leading edge of the Q-clock with the leading edge of the bit stream. The top row illustrates an early data stream in the solid line and a late data stream in the dashed line. The next three rows illustrate the I, Q and X2 clocks.

In the 5th row, the FDI D-type flip-flop samples the data stream at the rising edge of the I-clock (CLK), whereas FDQ_Q outputs the Q-CLK sample of the data in row 6. The 7th row indicates that the $FDQ_{\overline{Q}}$ output is simply the complement of FDQ_Q. Notice that both FDQ_Q and $FDQ_{\overline{Q}}$ are dependent on the data timing relative to the Q-CLK timing.

Row 8 illustrates the output of FEQ_Q which is a one-half-bit delay of the I samples. $FEQ_{\overline{Q}}$ is the complement of FEQ_Q. In the 10th row, the positive transition detector output AND-gate is shown. Notice that a pulse occurs one-half a bit after the occurrence of the leading edge of each bit.

The 11th row illustrates the up/down gate output for both late and early data streams. In the 12th row, the count enable flip-flip is indicated. In order for the count enable to be high, the reset input must be at the 0 state and the transition detector must be high when the Q-clock arrives. When the Q-output is high, the up/down counter is free to accept a unit change in its count.

In the 13th row, the 1 kHz clock tick marks are shown, for convenience, at a much higher rate than 1 kHz. The counter enable ($\overline{Q}$) output of the flip-flop of row 14 is the inverse of the 12th row output.

Row 15 depicts the output of the J-AND gate, illustrating the difference for early and late data streams. In the same manner, row 17 illustrates the output of the K-AND gate. In row 16, the inverse of the up/down gate is illustrated.

Row 18 illustrates the least significant bit output of the up/down counter which feeds the LSB delayed flip-flop. This control stays high for 2 ms rather than 1 ms since the up/down counter is enabled just after the next 1 ms clock occurs, which therefore requires 2 ms to change the LSB.

In row 19, the least significant bit detector flip-flop output stays high for 2 ms, as can be seen from the sketch. The reason for the 2 ms duration is the same as for the LSB 2 ms duration. The reset control for the counter enable F/F is just the modulo 2 sum of the LSB and the LSB-delayed F/F, which is shown in row 20.

In the 21st row, the JK F/F called FHQ(Q) provides the advance or retard signal which, when clocked into the up/down counter and converted via the DAC, provides the timing error reduction. This advance or retard

is relative to the Q-clock epoch times. Finally, the last row illustrates the times when the counter is updated to correct the loop timing. Notice that the correction will be an advance of the VCO-generated clock when the leading edge of the bit stream leads the clock and a retard if the data leading edge is retarded from the clock.

3.0 TIMING DIAGRAMS UNDER IMPERFECT DATA STREAMS

In this section, timing diagrams are presented which consider data asymmetry of 25% and various timing errors. In Figure 3, the case of 25% asymmetry is illustrated via a timing diagram. Asymmetry is defined as

$$ASY = \frac{|T_1 - T_0|}{T_1 + T_0} \times 100\% \qquad (1)$$

where T_1 is the bit duration of a "one" when preceded and followed by a zero, and T_0 is the bit duration of a "zero" when preceded and followed by a one. It is currently expected that the total asymmetry due to rise time and transmitted asymmetry will be no more than 25% at 50 Mbps, and less at low bit rates.

In the last row of Figure 3, it is seem that the updating is in the correct direction; that is, the Q-clock is advancing. We conclude from Figure 3 that errors up to 90° (data leading edge of the Q-clock) are acceptable to the bit synchronizer when the data "ones" are larger than the data "zeros" with 25% asymmetry.

In Figure 4, the same case as in Figure 3 is illustrated, except that the data lags the Q samples leading edge by 67.5°. As can be seen in row 6, the Q samples are all zero; however, the last row of the timing diagram indicates that the error correction signal retards the timing, which is the proper action for the loop to take. We conclude from Figure 4 that, with errors up to 90° (data lagging the leading edge of the Q-clock) and 25% asymmetry, the bit synchronizer works properly so as to decrease the timing error.

Figure 5 illustrates the same case as Figure 4 except that the phase of the 1 kHz clock has been changed to verify that the loop operates properly, which it does.

In Figure 6, the case when the data leads the Q-clock by 22.5° is illustrated. This figure has the "ones" larger than the "zeros" but, again, the bit synchronizer provides the correct correction so as to reduce the tracking error.

Figure 7 illustrates the case where data lags the Q samples by 100° and has 25% asymmetry with the "zeros" wider than the "ones." As can be seen from the last row, the loop still corrects in the proper direction so as to reduce the timing error.

The point of Figure 8 is to illustrate the fact that the bit synchronizer has limitations as to how large a timing error can be tolerated. With the data lagging the leading edge of the Q sample by 190°, it is seen that the loop has no response; that is, no loop correction occurs since the counter enable is always at 0 or, equivalently, the counter is disabled.

Finally, Figure 9 illustrates the case when, with 25% asymmetry, and the data leading the Q-clock by 100°, the loop is incapable of providing updates to reduce the timing error.

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1. Holmes, J. K., "Critique of a Hughes Shuttle Ku-Band Data Sampler/ Bit Synchronizer," Axiomatix Report No. R8003-1, March 14, 1980.

2. "Mid-Bit Corrector," Hughes Aircraft Company (Culver City) note dated about March 1980.

3. Motorola MC4344-MC4044 Phase Frequency Detector Specifications and Operating Characteristics, Issue A, 1972.

4. Kimura, R. K., "Logic Description of the Motorola MSI Digital Phase Detectors," TRW IOC 7333.11-21, October 31, 1974.