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COPLANAR BACK CONTACTS FOR THIN SILICON SOLAR CELLS

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16. Abstract

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The development work on the dielectric included looking at three dielectrics for the wraparound application. Transene #1000, Thick Film Systems #1126RCB and an in-house formulation #61-2-2A were all tested. Both the in-house #61-2-2A and the Transene #1000 appeared to give somewhat less warpage than the TFS #1126RCB, but all were judged unsatisfactory, causing severe bowing and cracking of the thin web region. A "filler" was also introduced in order to match the thermal expansion coefficient of the dielectric a little closer to that of silicon. This was unsuccessful.

Cells with a pre-dielectric thickness of 3.0-3.5 mils using Transene #1000 as the wraparound dielectric and the procedure outlined above showed an average efficiency of 10.7 percent. Thinner cells were fabricated, but had an unacceptable yield and efficiency.

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TABLE OF CONTENTS

ABSTRACT

Development work on thin, lightweight, high efficiency, space-type, silicon solar cells was done for NASA Lewis Research Center under Contract No. NAS 3-21251. Solar cells 3.0-3.5 mils thick with an average efficiency of 10.7% that had a wraparound configuration were fabricated for the contract. Thinner cells were fabricated for the contract, but these cells had unacceptably low yield and efficiencies. The process used to fabricate the cells included a reinforced perimeter, vacuum evaporated contacts and a screen printed wraparound dielectric layer. Numerous problems have yet to be worked out that will minimize the handling and breakage that has been characteristic of the process that was used.

1.0 SUMMARY

A process for fabricating 2 to 3 mil wraparound solar cells was formulated under this contract. Sample thin wraparound cells were fabricated using this process.

The process used a reinforced perimeter construction to reduce the breakage that occurs during handling of the wafers. A retracting piston post was designed and fabricated to help minimize the breakage that occurs during the screen printing process. Two alternative methods of applying the aluminum back surface field were investigated. In addition to the standard screen printed back surface field, both spin-on and evaporated aluminum techniques were researched. Neither spin-on nor evaporated aluminum made any noticeable improvement over the screen printing technique. A fine screen mesh was chosen for the application of the aluminum paste back surface field. The optimum time and temperature for firing the aluminum turned out to be thirty seconds at 850^{o}C.

The development work on the dielectric included looking at three dielectrics for the wraparound application. Transene #1000, Thick Film Systems #1126RCB and an in-house formulation #61-2-2A were all tested. Both the in-house #61-2-2A and the Transene #1000 appeared to give somewhat less warpage than the TFS #1126RCB, but all were judged unsatisfactory, causing severe bowing and cracking of the thin web region. A "filler" was also introduced in order to match the thermal expansion coefficient of the dielectric a little closer to that of silicon. This was unsuccessful.

Cells with a pre-dielectric thickness of 3.0-3.5 mils using Transene #1000 as the wraparound dielectric and the procedure outlined above showed an average efficiency of 10.7 percent. Thinner cells were fabricated, but had an unacceptable yield and efficiency.

2.0 INTRODUCTION

2.1 Background

Future space missions requiring the use of millions of solar cells will require many refinements in present-day cell designs. The Solar Electric Propulsion System (SEPS) program[1] and the Satellite Solar Power System (SSPS) program[2] each require such huge quantities of cells that two problem areas immediately become apparent. First, the sheer weight of such large quantities of cells requires that cell designs evolve that are capable of marked improvements in the power to weight ratio. Second, the assembly of cells into solar panels must be accomplished by automated or mechanized techniques in order to keep costs within reasonable bounds, and thus cells must be designed with contact schemes that are amenable to such assembly.

Spectrolab has just completed a program that investigated extending solar cell processing techniques to very thin cells.[3] This effort was successful in producing 2 x 2 cm cells with a thickness of 0.04 mm that exhibited an AMO conversion efficiency of 13.5%, and a power to weight ratio of 2.07 watts per gram. For comparison, the best available "conventional" space type cell has a thickness of 0.20 mm, and has an efficiency of about 15.5% at AMO, which is a power to weight ratio of 0.44 watts per gram. These thin cells, aside from their dramatic improvement in power to weight, have an added advantage in that they also display a significantly better tolerance to radiation.

Additionally, Spectrolab has been engaged in developing processes and techniques for fabricating coplanar back contact solar cells since 1972 under a series of contracts sponsored by the NASA

Lewis Research Center, and by both NASA Marshall Space Flight Center and the Comsat Corporation through subcontracts with the Lockheed Missiles and Space Systems Group. The work at Spectrolab has been primarily concerned with cell designs and process sequences that make it possible to utilize wraparound metallization to provide back contact pads for both the base of the cell and the front gridline patterns. Cell designs have included both junction and dielectric isolation wraparound structures. The dielectric isolation technique was found capable of producing 2 x 4 cm cells 0.20 mm thick that had an average conversion efficiency of 14.5% under AMO illumination.[4]

2.2 Objective

The objective of this program was to achieve wraparound contacts on thin, lightweight, high efficiency, space-type, silicon solar cells. This investigation was carried out with the specific intent of developing a cell that met the following requirements:

- Weights and/or thicknesses: 45 to 70 milligrams and/or 0.05 to 0.075 mm (2 to 3 mils). Although a uniform thickness was preferred, structures of nonuniform thickness, e.g. reinforced perimeters were permitted.
- Efficiency: goal 14% AMO at 28°C; minimum 13% AMO at 28°C
- Base Resistivity: 1 to 10 ohm-cm
- Junction depth: shallow with approximately 100 ohm/square sheet resistance
- Texturized front surface with AR coatings
- Design which incorporates a back surface field
- Design which maximizes cell active area
- Design which minimizes rear contact loss
- Cell flatness equivalent to a minimum 7 cm radius or edge to center deflection of less than one mm for a 2 x 2 cm cell at 28° C.

3.0 TECHNICAL DISCUSSION

3.1 Thin Cell Fabrication

Cell thickness has become an important design consideration in modern solar cell technology, not only because of its effect on cell performance, but also because of the direct effect on solar panel weight requirements. During the last fifteen years there has been a gradual increase in the amount of power delivered as a function of solar panel weight, partially because of improvements in cell efficiencies, and partially because of reductions in average cell thickness. It has been the program's goal to produce cells with weights of 45 to 70 milligrams and thicknesses of .05 to .075 mm (2 to 3 mils). Although cells with uniform thickness were made, the fabrication process used a reinforced perimeter wafer.

The advantages of reinforced perimeter structures are impressive. Handling fractures are nearly eliminated, and cells as thin as 0.01 mm can be fabricated. The warpage caused by heavy back contact metallization is reduced to acceptable limits. The texturized front surface, which is recessed, is protected from fractures of the tetrahedra, and welded contacts to the cell (more difficult on texturized surfaces) can be made on the polished perimeter to give yield strengths up to 1200 grams, compared to about 500 grams on a texturized surface.

In order to make cells that are this thin, this program used chemical etching. A titanium-silver layer was evaporated over one face of a 51 mm (2 inch) diameter silicon wafer that had a 29 mm (1.14 inch) diameter circular region masked in the center. A titanium-silver layer was also evaporated on the back side. The wafer was chemically thinned until the round region in the center was at the desired thickness. The metal layers were etched away, leaving a depression in the center

having the dimensions (roughly) and thickness of the final cell. Later on in the cell process sequence, the thinned section was cut out of the parent wafer by a dicing step. By using this technique the thin "web" was supported during much of the cell fabrication process, providing ease in handling and minimizing breakage. The process results in a final cell of uniform thickness.

It was found that relatively tight tolerances on the planarity and parallelism of the wafer faces must be maintained in order to obtain thinned down regions that have uniform thickness. Saw marks and taper must be removed by lapping both sides of the starting wafers, since the chemical etching tends to accent irregulatities.

A series of etching and thinning runs were made in order to determine the quality of starting wafer that could suffice with regard to the allowable taper and any saw marks that might be present. Since nearly all wafers are sliced to a taper tolerance of 0.5 mil (0.0127 mm) maximum for a 51 mm diameter wafer, taper has not been a serious problem. If taper exists in the starting wafer, it will usually be found in the thinned section after etching. Saw marks, on the other hand, can create difficulties, since the surface irregularities are maintained through the etching, and if the deviations from flatness are appreciable, they can be a sizable fraction of the final cell thickness. The term "sawmarks", as used here, are steps in the silicon surface caused by the saw blade during slicing. These are not necessarily an indication of saw damage, which is lattice damage that is usually propagated several mils into the silicon.

Etch thinning of wafers cut on reciprocating saws (which generates less saw damage but more saw marks) was found to be difficult, with etch-through points appearing very often before the desired

thickness could be attained. The supplier had previously indicated that wafers cut on wire saws had damage extending only about 0.7 mil into the silicon, which may prove to be useful in maintaining good carrier diffusion lengths without the necessity of etching away relatively thick surface layers. This effect, however, could not be utilized due to the etch-through problem. Wafers cut on ID saws (with comparatively smooth surfaces) and little taper gave webs that were uniform and etch-through was minimal. In order to evaluate planar and parallel surface wafers, a group of 100 wafers was sent out for planetary lapping. Generally, it was found that 51 mm wafers could be etched to provide a web region that was 0.05 mm thick without undue difficulty. These could also be texturized using the 1% NaOH/alcohol process with few problems, however, texturized webs exhibited a higher degree of fragility than smooth ones.

3.2 Back Surface Field Formation

Normally, with relatively thick cells, the P^+ back surface field structure has been produced by screen printing fritless aluminum paste on the back surface of a wafer, drying the paste, and then subjecting the wafer to a short "spike" thermal cycle to alloy the aluminum with the back surface of the wafer. This results occasionally, in regions where the aluminum alloys excessively, resulting in a deeper penetration of the alloy in such areas and the production of an irregular lumpy surface. When this occurs with very thin silicon, the alloy penetration may well be sufficiently deep to punch through the silicon wafer. Some experiments were performed to attempt to make the alloying process more uniform. Spin-on and evaporated aluminum were tested as possible procedures that would give an even distribution of the aluminum on the back surface.

In order to test the spin-on procedure, aluminum paste was thinned to a relatively low viscosity using butyl carbitol. This paste was applied to diffused silicon wafers using conventional spin-on techniques. After drying and alloying, it was found that the amount of aluminum applied did not appear to be sufficient to provide a continuous alloy-regrowth layer. The values of V_{oc} obtained appeared to be comparable to that obtained from an evaporated layer of aluminum. Thicker pastes were difficult to spin on uniformly. By repeated spin-on and dry cycles this might be an alternate method for applying aluminum paste, however, such a technique would have a decided disadvantage in terms of time and labor inputs.

The addition of one percent by weight of 5 - 10 micron aluminum oxide powder to the aluminum paste has previously been found to aid in producing uniform alloying, probably by inhibiting lateral aluminum particle transport. Also, it has been found that performing the alloying in artificial air helped uniformity. It was also thought that by evaporating a thin layer of aluminum on a freshly etched wafer back, prior to printing on the aluminum paste, additional uniformity might be obtained. Several previously diffused wafers were back etched and approximately 200 angstroms of aluminum evaporated onto the back surface. These, along with a similar number of nonevaporated wafers were then screen printed with aluminum paste and alloyed as usual. Open circuit voltages were then checked by probing the wafers under a solar simulator. It was found that the wafers without the evaporated aluminum had an average V_{oc} (probe) of 613 mV, while the wafers with the evaporated aluminum layer had probe V_{oc}'s averaging 586 mV. This investigation was therefore not carried any further. The evaporated aluminum seemingly inhibits the alloying and penetration of the aluminum paste.

Since exploration of spin-on and evaporated aluminum back surface field formation techniques did not produce adequate results, attention was focused on optimizing the screen printed aluminum paste back surface field. The process initially reported in the NASA-Lewis Research Center final report, "Automated Fabrication of Back Surface Field Silicon Solar Cells with Screen Printed Wraparound Contacts", was tried.[5] This requires screen printing a fritless aluminum paste on the back surface (without the depression) of the wafer. This step has been characterized by excessive mechanical breakage losses caused by fracturing the web during the printing operation. Printing the wafers with the recess up gave excessive aluminum in some regions around the periphery of the web. A printing post was designed with a retractable piston in the center to provide support for the web during screen printing in order to rectify this problem. A sketch of this printing post is shown in Figure 3.1. Since the piston on which the thinned web rests during printing is round, an appropriate size punch was obtained and modified to make 0.006" thick discs with a diameter of 1.140". These discs are used for masking the evaporated metal from the center of the silicon wafer prior to etch thinning to produce the 0.05 mm thick web.

When the printing operation began, it was found that sufficient vacuum leakage occurred between the wafer surface and the teflon top plate of the printing post to cause marked deformation of the periphery of the webbed region. Thus, once the piston was adjusted to the proper height and was clamped into place, prints were made by manually lowering the platen into position, lowering the squeegee and operating the print stroke control. All of this was done without the use of vacuum hold-down. Vacuum was then applied, the screen was manually released from

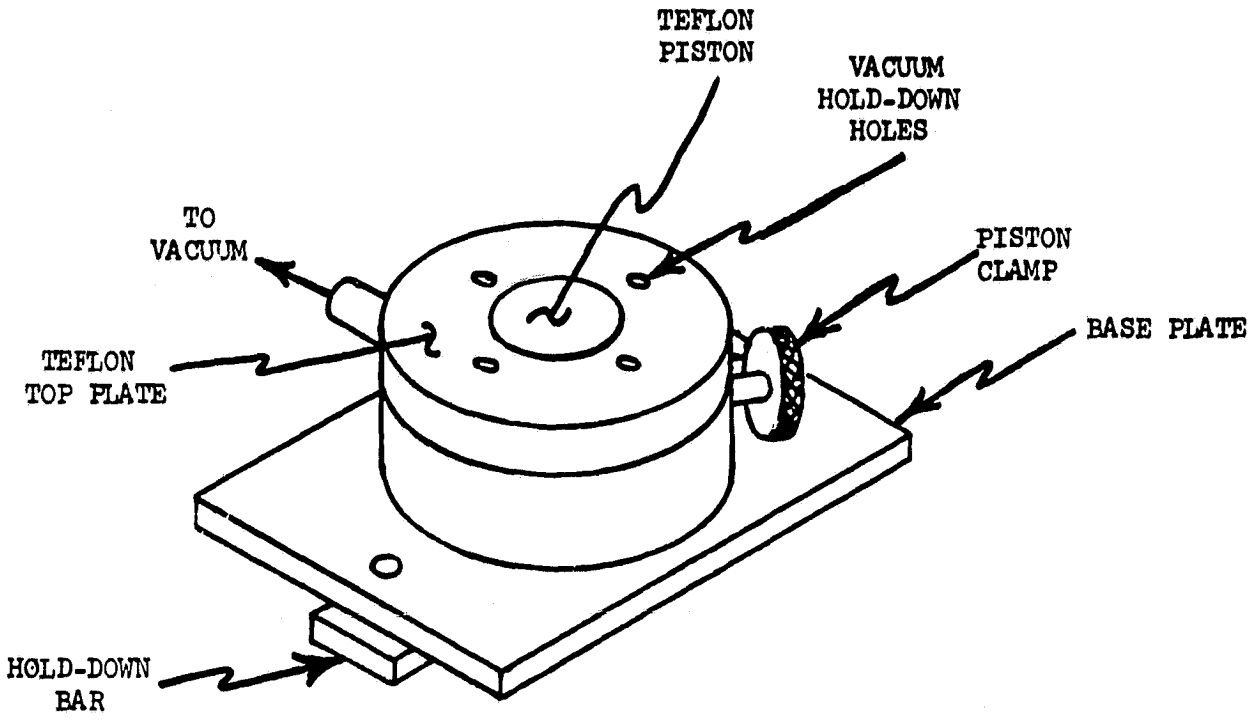


Figure 3.1

Thin Cell Printing Post

the wafer and the platen was raised. Satisfactory prints were made like this without fracturing the thin web section of the wafers. Initial prints of aluminum paste were judged uniform and of good quality. Once the aluminum paste was dried and alloyed, the excess was removed by etching in hot hydrochloric acid. The resulting dendritic regrowth silicon was essentially the same as thicker wafers, however, probe open circuit voltages were not as high as anticipated.

Further experimentation was conducted to optimize both the thickness of the aluminum paste and the alloying time so that both the open circuit voltage and the short circuit current were maximized.

The standard in-house aluminum paste (70% Alcoa #1401 powder, 28% Terpineol, and 2% Ethyl Cellulose) which has 2% aluminum oxide powder added was printed on 0.05 mm thick web wafers using the retracting piston printing post. It was immediately found that a 200-mesh screen deposited excessive paste and resulted in the alloy penetrating completely through the web in spots. By using a 325 mesh screen for the print step, the alloying could be accomplished without any serious problems and without excessive penetrations.

In order to optimize the alloying time, web wafers, diffused to sheet resistances of 80 to 100 ohms per square, were processed using a matrix of firing temperatures and times. Since alloying times and firing temperatures are interrelated, and since probably some gettering of substrate impurities occurs for the longer firing times, this series of tests was more in the nature of an empirical establishment of the proper time/temperature cycle for the specific web thickness being used and for the specific substrate material than a universal process. The data from these trials are shown in Table 3.1.

Table 3.1

V_{oc} Probe Readings (mV)

Firing Temperature	Firing Time 10 Sec	20 Sec	30 Sec	40 Sec
750°C	562	560	562	553
800°C	596	601	602	600
850°C	615	618	612	611

The optimum firing time and temperature have been shown (see Final Report for JPL Contract No. 954600) to peak first for enhancement of the short circuit current for a given temperature as the times are increased, and then for the open circuit voltage.[3] It should be emphasized that the optimum firing time will be affected by the thermal system used (i.e., the thermal mass of the wafers and boat), as well as the withdrawal rate from the furnace.[6]

3.3 Application of Dielectric Wraparound

The work completed on the application of the dielectric wraparound during this contract covered verification of the mechanical printing process, investigation of various mesh sizes, testing various kinds of pastes, testing various kinds of filler for the pastes and various methods of putting the pastes on the cells.

Wraparound dielectric layers of Thick Film Systems #1126RCB were printed on 0.05 mm thick metal (stainless steel) blanks in order to investigate any problems that might be encountered in the printing operation itself. It was found that uniform layers could be produced with only a minimal bead along the edge. Isolation was very good (greater than 10,000 ohms), but warpage was marked. This was not a test for silicon wraparound structures, since in this case, the glass was under compression after firing and thus was virtually crack-free. It did indicate, however, that the printing step would not encounter mechanical problems. This experiment cleared the way for wraparound printing on thin silicon specimens.

A series of 2 x 2 cm cells having a thickness of 0.05 mm, texturized front surfaces with N^+ diffused junctions (sheet resistances of about 80 ohms/sq.), P^+ back surface field junctions, and a back surface metallized with Cr-Pd-Ag were started into the wraparound dielectric screen printing operation. The cells were placed on a flat printing post and positioned accurately with stops attached to the post. Vacuum hold-down was used until the printer platen was lowered and then turned off to avoid deforming the cell during printing.

Thick Film Systems #1126RCB dielectric paste was printed on wafers using a 200-mesh screen. This screen gave a fired dielectric layer thickness of approximately 0.03 mm. The result was excessive warpage of the silicon wafer accompanied by the generation of a large number of cracks in the wafer. Successive printings of this paste using finer mesh screens gave increasingly less and less deformation, with no visible cracks in the silicon. Isolation checks appeared satisfactory, but warpage was still evident. Dielectric thickness in the thinnest layers was roughly 0.008 mm. When Transene #1000 dielectric paste was used as the wraparound isolation, a 325-mesh screen worked out the best. A 400-mesh screen was also used to limit the thickness of the paste layer. This caused a problem in printing, since the screen was found to plug repeatedly, requiring cleaning after nearly every other print. The deposited layers were also too thin to give isolation, even after printing and firing double layers. The 325-mesh screen therefore appeared to give the best compromise between adequate isolation and silicon deformation after firing. An in-house formulated paste#61-2-2A was also tried as a possible isolation material. Both the in-house paste and the Transene #1000 appear to give somewhat less warpage than the TFS #1126RCB,

but all are unsatisfactory, causing severe bowing and cracking of the thin web region.

Powdered silica and silicon were obtained to attempt to "fill" the dielectric paste to reduce the effective linear expansion coefficient, and therefore reduce the bowing. The silicon powder was oxidized prior to mixing with the paste to provide a silica layer around each silicon particle in order to prevent formation of conductive paths through the layer. Initial printings indicate that Transene #1000 filled with oxidized silicon powder deformed 0.05 mm thick silicon sections only slightly. Single layers printed with a 325-mesh screen have an as-fired thickness of approximately 0.025 mm. Layers made on the initial runs appear to isolate electrically when tested with an ohmmeter and salt water droplets. This, however, was only a preliminary check. The quality of the isolation must be established with evaporated metallization.

Cell warpage was reduced by use of oxidized silicon powder and powdered silica as fillers in the dielectric paste. However, these fillers also caused screen plugging, since the powders were relatively coarse and no equipment was immediately available to obtain finer ground materials. This practice had to be abandoned in order to minimize pinholes in the layers.

In order to avoid the mechanical stresses and less than adequate material deposited along and around the edges of 0.05 mm thick cells, it became necessary to apply the dielectric to the wraparound edge by dipping the edge into a freshly screen printed layer on a glass substrate. The size of the bead along the isolation edge can be controlled to some extent by the mesh size of the screen used to print the dielectric on the glass. Several groups of cells were processed through this point with minimal difficulty and acceptable losses due to mechanical breakage.

3.4 Contact Metallization

The front gridline Cr-Pd-Ag metallizations were applied using shadow mask tooling which had been originally made for use on 2 x 4 cm cells that had 4 cm long gridlines. By placing the 2 x 2 cm cells at the extreme end of the mask, the gridlines left a 0.03 cm gap at one edge of the cells and extended over the dielectric bead at the wraparound edge. By evaporating the metal with the mask holder held at a 45° angle to the impinging metal, the grid lines could be made to wrap more than halfway around the dielectric bead. The long fingers of the gridline masks would break the thin cells when a magnet was used to hold the mask tightly against the silicon. Placing 1 x 2 cm silicon spacers in the fixture minimized this breakage. The size of the bead had to be kept minimal, since this held the mask away from the silicon surface near the isolated edge, thus giving some overspray and widening out the gridlines.

The back gridline contact pad was evaporated using Cr-Pd-Ag. The normal back contact mask for this tooling was used, and resulted in acceptable spacing between the contacts and the edges of the cells. Aluminum foil was positioned to limit the pad size. Again, by positioning the fixture at a 45° angle, the pad could be deposited more than halfway around the dielectric bead, thus making contact to the gridlines.

Several groups of cells were completed through metallization, and checked for electrical behavior prior to applying an AR coating. Copper clad plastic sheet was used as a test fixture to make contact to the thin cells. The copper was etched into a pattern matching the pads on the backs of the cells. A hole was punched in the plastic so that vacuum hold-down could be used to press

the cells against the copper contacts and also hold the cells tightly against the temperature controlled base block. The plastic layer was slightly more than 0.025 mm thick after removal of the copper cladding. Removal of the copper caused the polyimide film to develop a marked bow. Even when the film was held in place with tape, sufficient movement occurred when the vacuum was applied to occasionally break the cells.

3.5 Process Sequence Used for Wraparound Cells

The process sequence shown in Table 3.2 has been developed during this contract. During the course of this program, it was decided to evaporate titanium and silver on both the front and the back when etch thinning the cells. This offered better uniformity of the finished wafer, because the surface imperfections were only being accentuated on one side of the silicon wafer. Transene #1000 was selected as the appropriate dielectric although none of the dielectrics that were tested during the program were judged satisfactory. The wraparound configuration is shown in Figure 3.2.

3.6 Test Results for Both Wraparound and Non-Wraparound Cell Configurations

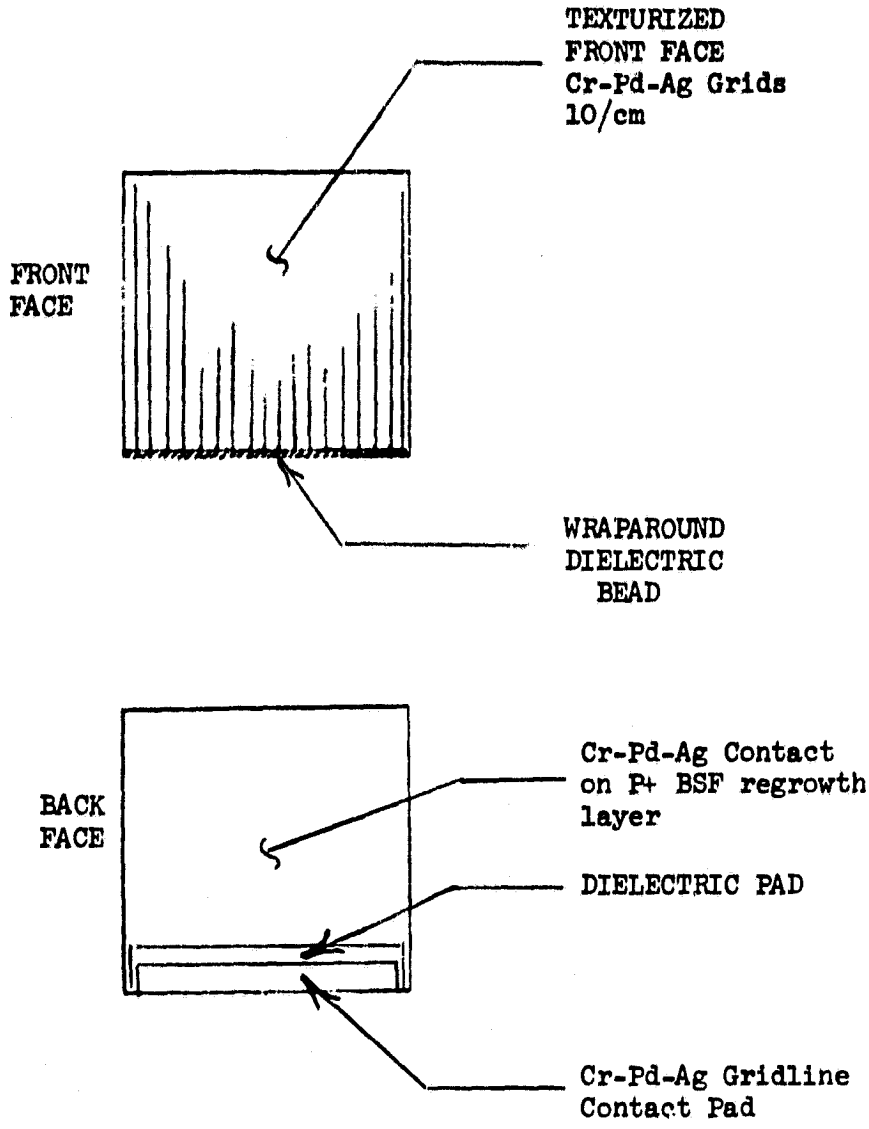
During the course of the contract one lot of wafers was processed through the entire non-wraparound process sequence and two lots of wafers were processed through the entire wraparound process sequence. One lot of wafers was completed through all wraparound process steps, but the antireflective coating step. The test data from a lot of non-wraparound control wafers are shown in Table 3.3. A representative cell was chosen from this group. This cell's I-V characteristic is displayed in Figure 3.3.

Table 3.2

COPLANAR CONTACTS FOR THIN SILICON SOLAR CELLS

PROCESS SEQUENCE

1. Evaporate titanium-silver mask on front
2. Evaporate titanium-silver on entire back
3. 30% NaOH etch (damage removal and thinning)
4. 2% NaOH etch (texturize to final thickness)
5. Etch off titanium-silver (NH_4OH + H_2O_2 then dil. HNO_3)
6. Diffuse (phosphene gas)
7. 10% HF etch
8. Screen print aluminum paste (flat side)
9. Dry aluminum paste
10. Alloy aluminum paste
11. Remove aluminum layer (boiling HCl)
12. Evaporate back (flat) side with chromium-palladium-silver
13. Wax mount on dummy wafer (depression up)
14. Cut to 2 X 2 cm size (dicing saw)
15. Demount from dummy wafer
16. Clean to remove all wax
17. Print Transene #1000 dielectric (to edge but not over)
18. Dry dielectric paste
19. Repeat Step 17
20. Repeat Step 18
21. Dip edge in freshly printed Transene #1000 on glass (200X1.6-mesh)
22. Repeat Step 18
23. Fire dielectric paste (550°C - 10 min. - air)
24. Mount in evap. tooling
25. Evap. chromium-palladium-silver wraparound grid lines
26. Reverse tooling fixture
27. Evap. chromium-palladium-silver gridline contact pad
28. Remove from tooling and inspect
29. Deposit Ta_2O_5 AR coating
30. Bake at 375°C for 1 min.
31. Test



2 X 2 CM. WRAPAROUND CELL CONFIGURATION

Figure 3.2

Table 3.3

Data for Baseline 2 x 2 cm Non-Wraparound 2 mil Cells

Cell No.	V_{oc} (mV)	I_{sc} (mA)	V_{mp} (mV)	I_{mp} (mA)	P_{max} (mW)	M.P.D. (mW/cm^2)	Calc. Eff.(%)	Calc. CFF	Cell Wt.(mg)
1	600	157	485	144	69.7	17.5	12.9	.74	58.3
2	605	154	502	142	71.5	17.9	13.2	.77	47.8
3	605	157	500	146	73.2	18.3	13.5	.77	63.0
4	600	153	488	142	69.4	17.3	12.8	.76	65.3
5	604	151	490	136	66.6	16.7	12.3	.73	49.0
Av.	603	154	493	142	70.0	17.5	12.9	.75	56.7

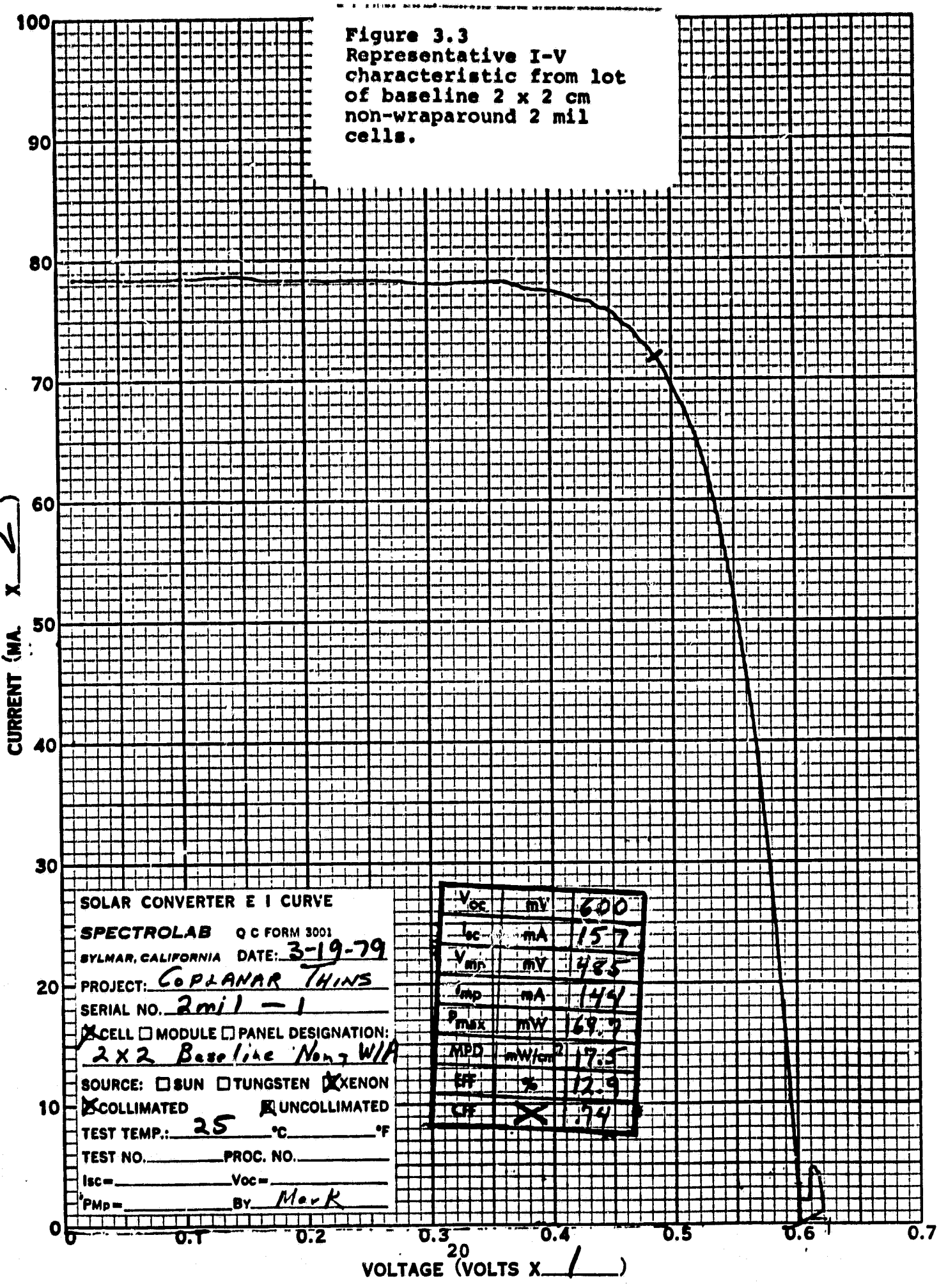


Figure 3.3
Representative I-V characteristic from lot of baseline 2 x 2 cm non-wraparound 2 mil cells.

Two lots of wraparound cells were also fabricated. The test data for these cells are shown in Table 3.4. The I-V characteristic of the only cell that could be tested from Group 19 is shown in Figure 3.4. The cells made in this group had an unacceptable yield. These cells were made at the target weight requirements. The I-V characteristic of a representative cell from Group 20 is shown in Figure 3.5. The average efficiency of the cells in Group 20 was about 10.7%. Group 20 had a pre-dielectric thickness of 3.0-3.5 mils. This thickness was above the design goals of the contract. A discussion of possible recommendations in order to improve the overall performance of the cells is presented in the section on Further Technological Development. The data for cells that were not processed through the entire process sequence are shown in Table 3.5. The contract required that all cells have a texturized front surface with multiple antireflection coatings. All of the cells processed in the unfinished group of cells did not have multiple antireflection coatings, and some did not have a texturized front surface. Representative I-V characteristics for this group of cells are shown in Figures 3.6 and 3.7.

Table 3.4

Group 20 (11 starts) - Pre-dielectric Thickness 3.0-3.5 mils
2 X 2 cm Dielectric Wraparound Cells

Cell No.	V_{oc} (mV)	I_{sc} (mA)	V_{mp} (mV)	I_{mp} (mA)	P_{max} (mW)	M.P.D. (mW/cm^2)	Calc. Eff.(%)	Calc. CFF	Cell Wt.(mg)
1	595	167	395	138	54.5	13.6	10.1	.55	90.3
2	593	165	412	146	60.0	15.0	11.1	.61	87.9
3	598	166	445	149	66.3	16.6	12.3	.67	81.6
4	593	167	385	140	53.9	13.5	10.0	.54	87.0
5	595	167	365	137	50.0	12.5	9.2	.50	94.0
6	591	167	420	148	62.3	15.5	11.5	.63	84.0
7	590	162	410	141	57.8	14.5	10.7	.60	86.7
Av.	594	166	405	143	57.9	14.5	10.7	.59	87.2

Group 19 (5 starts) - Pre-dielectric Thickness 1.9-2.2 mils
2 X 2 cm Dielectric Wraparound Cells

Three cells remaining - mechanical samples - excessive warpage. Cell "A" had V_{oc} = 581 mV, I_{sc} = 146 mA, Calc. Eff. = 9.4%. Average weight = 56.6 mg.
Calc. CFF = .60

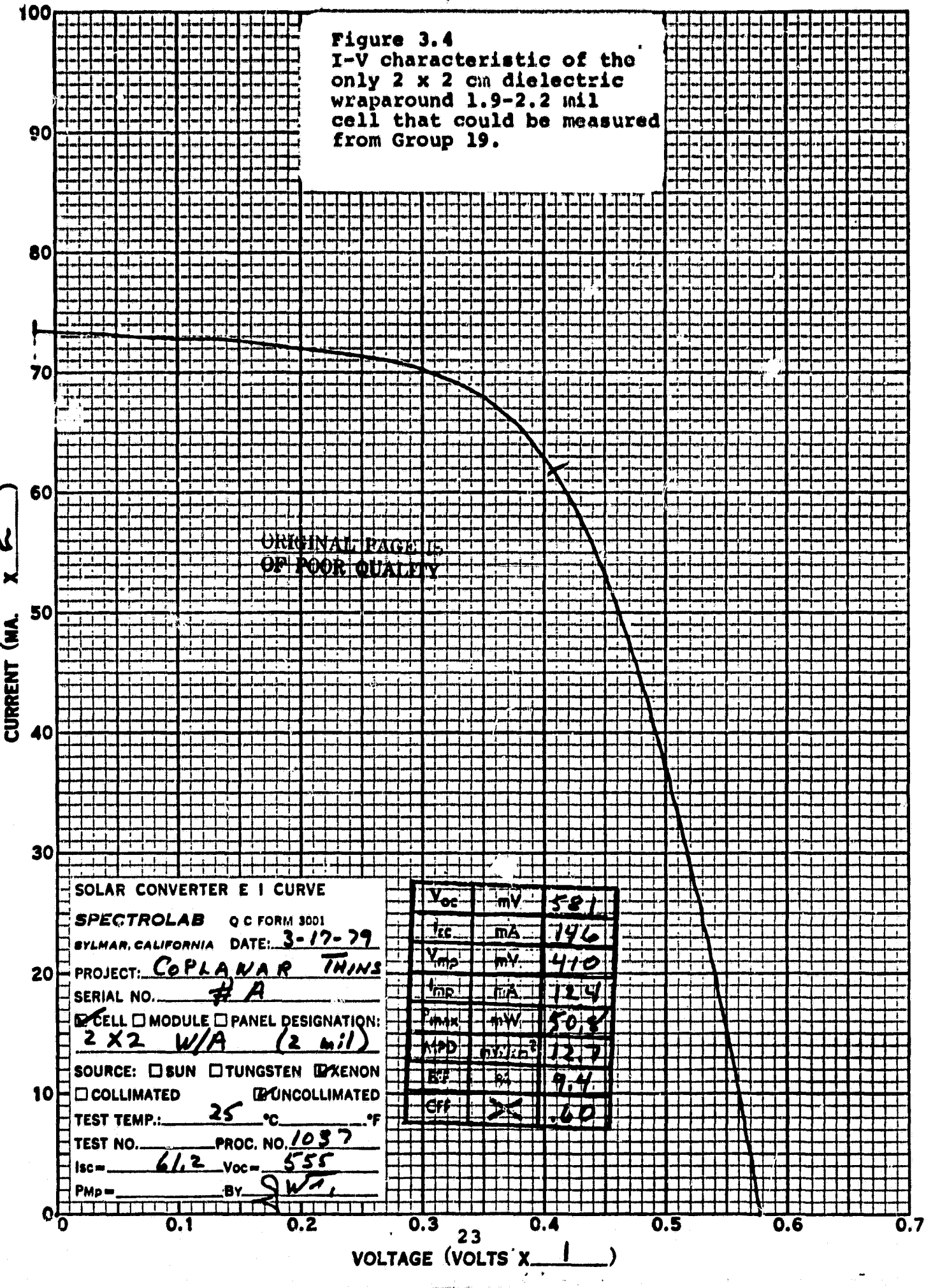


Figure 3.4
I-V characteristic of the only 2 x 2 cm dielectric wraparound 1.9-2.2 mil cell that could be measured from Group 19.
ORIGINAL PAGE IS
OF POOR QUALITY
CURRENT (MA. X 2)
VOLTAGE (VOLTS X 1)
100
90
80
70
60
50
40
30
20
10
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
SOLAR CONVERTER E I CURVE
SPECTROLAB Q C FORM 3001
SYLMAR, CALIFORNIA DATE: 3-17-79
PROJECT: COPLANAR THINS
SERIAL NO. # A
☑ CELL ☐ MODULE ☐ PANEL DESIGNATION:
2 X 2 W/A (2 mil)
SOURCE: ☐ SUN ☐ TUNGSTEN ☑ XENON
☐ COLLIMATED ☑ UNCOLLIMATED
TEST TEMP.: 25 °C °F
TEST NO. PROC. NO. 1037
Isc = 61.2 Voc = 555
Pmp = BY
Voc mV 581
Isc mA 146
Vmp mV 410
Imp mA 124
Pmax mW 50.8
MPD mW/cm² 12.7
Eff % 9.4
Cff % .60

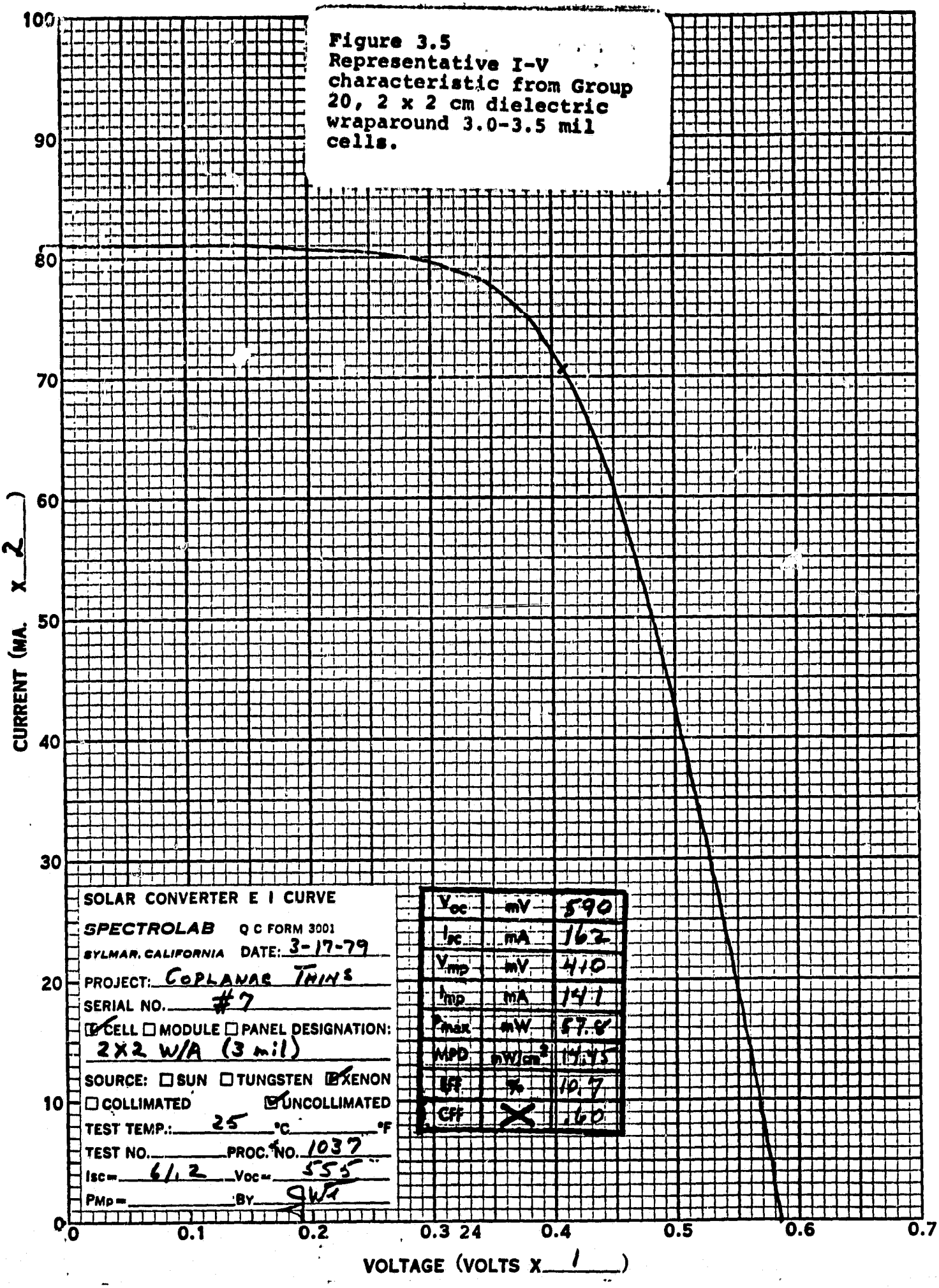


Figure 3.5
Representative I-V characteristic from Group 20, 2 x 2 cm dielectric wraparound 3.0-3.5 mil cells.

Table 3.5

Data on Unfinished Group of Wraparound Cells (Before AR Coating)

Cell No.	V_{oc} (mV)	I_{sc} (mA)	V_{mp} (mV)	I_{mp} (mA)	P_{max} (mW)	M.P.D. (mW/cm^2)	Calc. Eff.(%)	Calc. CFF	Cell Wt.(mg)
S-A	587	112	470	102	47.9	12.0	8.9	.73	95.2
S-B	585	113	455	101	46.0	11.5	8.5	.70	84.8
T-A	583	154	445	138	61.4	15.4	11.3	.68	90.3
T-B	583	153	462	134	62.1	15.5	11.5	.70	86.5
T-C	586	153	465	138	64.2	16.0	11.9	.72	86.8

NOTE: "S" cells are non-texturized, but are NOT chemical polished.
"T" cells are texturized.

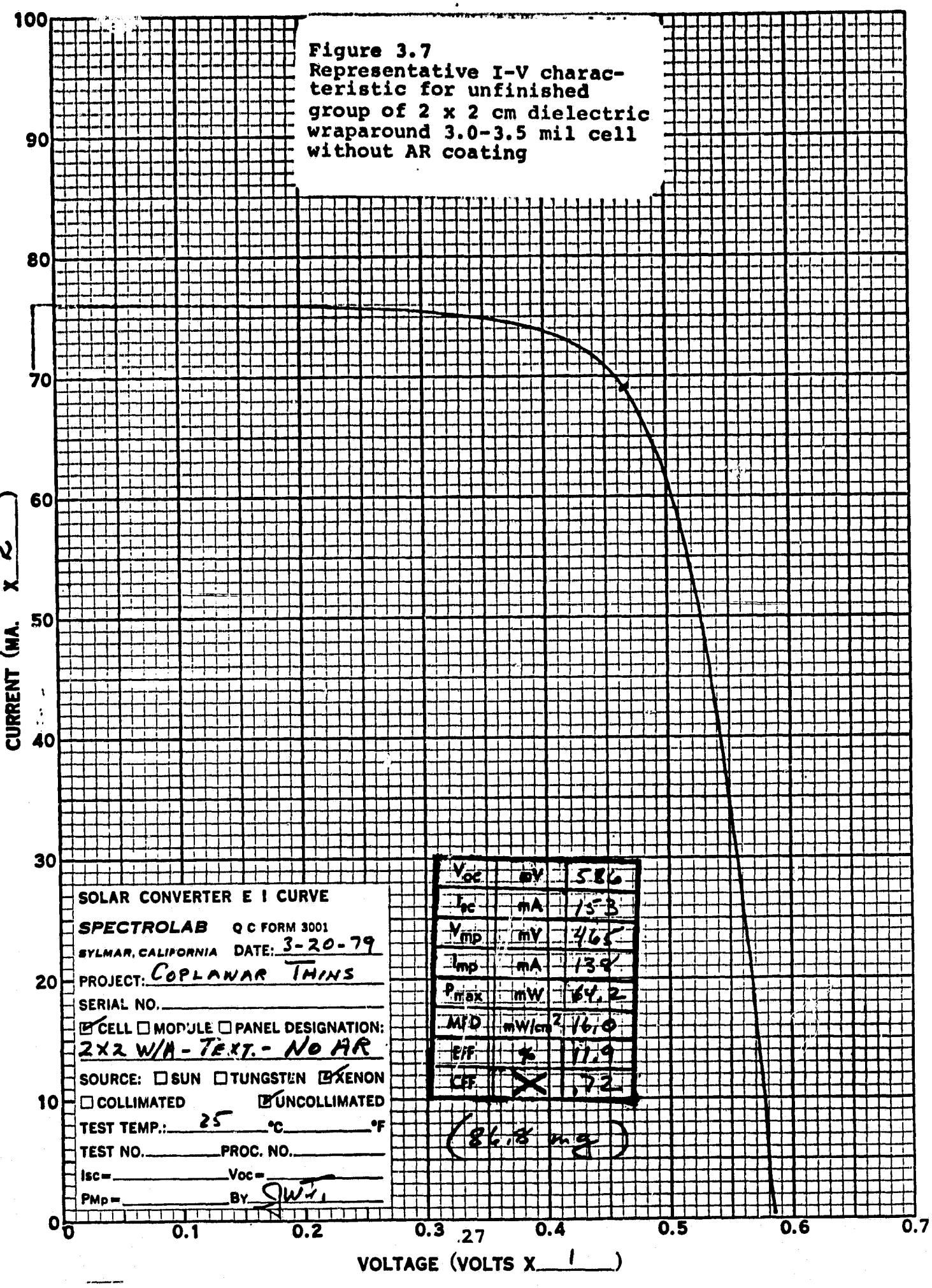


Figure 3.7
Representative I-V characteristic for unfinished group of 2 x 2 cm dielectric wraparound 3.0-3.5 mil cell without AR coating
CURRENT (MA. X 2)
VOLTAGE (VOLTS X 1)
100
90
80
70
60
50
40
30
20
10
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
.27
SOLAR CONVERTER E I CURVE
SPECTROLAB Q C FORM 3001
SYLMAR, CALIFORNIA DATE: 3-20-79
PROJECT: COPLANAR THINS
SERIAL NO.
☑ CELL ☐ MODULE ☐ PANEL DESIGNATION:
2x2 W/A - TEXT. - NO AR
SOURCE: ☐ SUN ☐ TUNGSTEN ☑ XENON
☐ COLLIMATED ☑ UNCOLLIMATED
TEST TEMP.: 25 °C °F
TEST NO. PROC. NO.
Isc = Voc =
PMp = BY JWH
Voc mV 586
Isc mA 15.3
Vmp mV 465
Imp mA 13.8
Pmax mW 64.2
MFD mW/cm² 16.0
EFF % 11.9
CEF X .72
(86.8 mg)

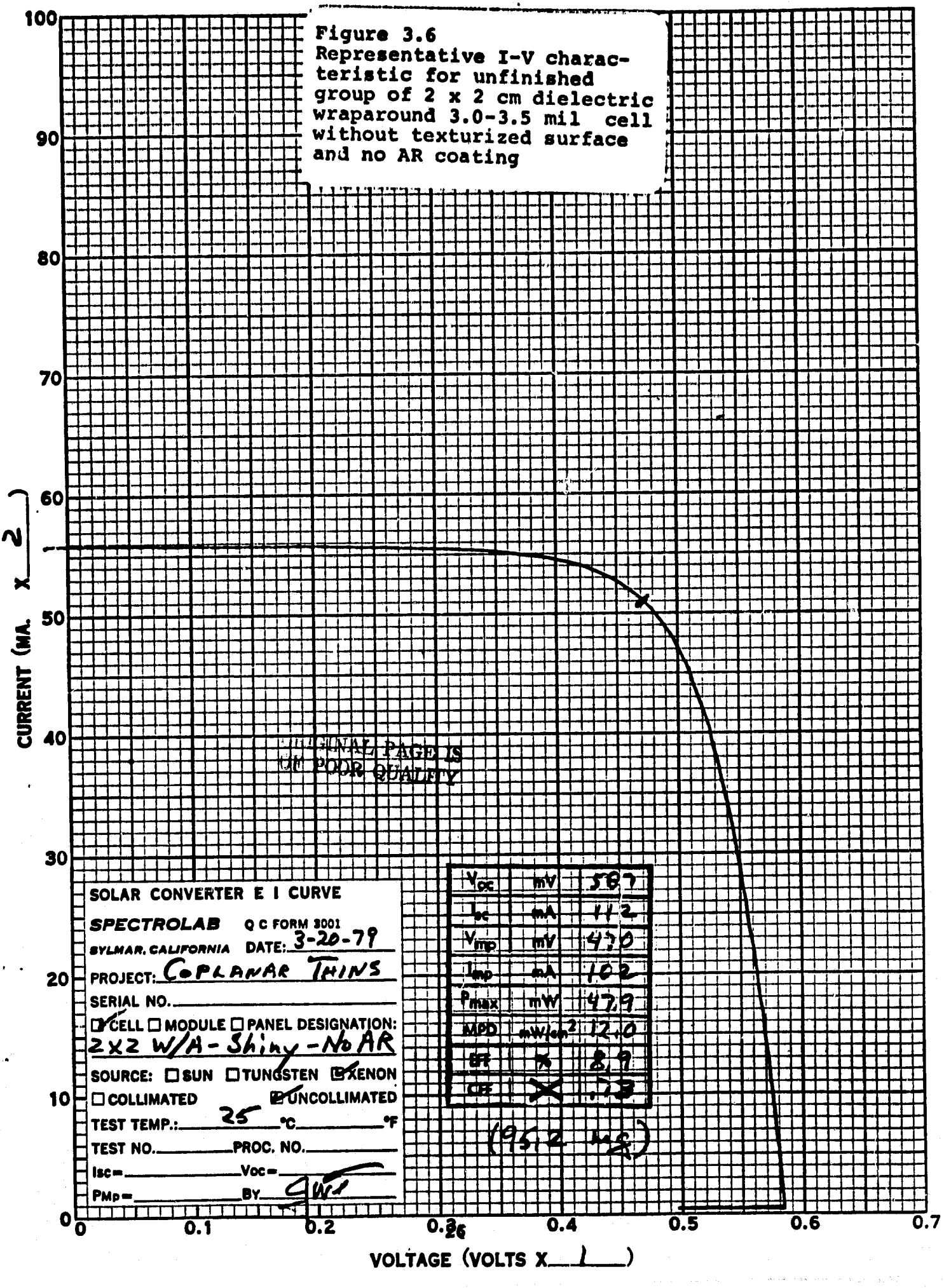


Figure 3.6
Representative I-V characteristic for unfinished group of 2 x 2 cm dielectric wraparound 3.0-3.5 mil cell without texturized surface and no AR coating

4.0 FURTHER TECHNOLOGICAL DEVELOPMENT

4.1 Screen Printing Problems and Considerations

Most of the major screen printing problems were associated with the mismatch between the thermal expansion coefficient of silicon and that of the dielectric paste. A warped wafer was produced after firing. The warped wafer could not be screen printed without breaking. Neither the mechanical support piston nor the inaction of the vacuum hold-down was able to alleviate this problem. The warped wafers were also not compatible with the boat used during firing. The boat had a high thermal mass so that the wafers cooled slowly after firing. However, because some of the cells were warped and made poor thermal contact with the boat, slow cooling was not always achieved.

The dielectric paste thickness was also a consideration. The thicker the dielectric paste, the more effect the thermal mismatch can have on the final cell shape. The dielectric paste was kept thin by the size of the screen mesh. A fine screen mesh ruled out using oxidized silicon powder as fillers because these powders are relatively course.

Another problem with the screen printing process was the dielectric overprinting which resulted in a ragged bead along the wraparound edge. The ragged bead also kept the wafer from making good thermal contact with the firing boat. A dip application of the dielectric wraparound had to be made. This process resulted in considerable individual handling of the cells.

Aluminum conglomerates or lumps also appeared on the backs of the cells and resulted in excessive aluminum penetration. This happened because the web cooled faster than the rim of the wafer.

4.2 Dielectric Considerations

Regardless of which dielectric is selected for use with the wraparound cell, thickness of the dielectric chosen is one of the most important considerations. If the dielectric is too thick, the wafer warps due to the mismatch in thermal expansion coefficients. If the dielectric is too thin the cell is not adequately isolated. The dielectric is in general much stronger than the silicon wafer, especially if the wafer is thin. This condition results in frequent breakage of the wafers when the vacuum hold-down is engaged. The break occurs right along the seam between the dielectric and the thin silicon wafer. The height difference at this seam causes destructive stress to build up and crack the wafer. The problem might be eliminated by going to a thicker cell or by eliminating the height difference on the back of the cell.

Clearly, a better match in the thermal expansion coefficient between silicon and the dielectric would improve the breakage problem. Dielectrics with a high firing temperature have a much better thermal expansion coefficient match. At these high temperatures, however, damage to the minority carrier diffusion length may result. Dielectrics that are fired at low temperatures should also be investigated, even though there is more of a thermal expansion coefficient difference. "Filling" the dielectric with a material with a thermal expansion coefficient closer to that of silicon shows merit and has been considered in the work done for this program. The "filler" that is added, however, must not plug the screen. Other dielectrics that should

be considered include conventional passivation glass that is used for power transistors (ZBSG). ZBSG consists of 2% PbO, 25% B_2O_3, 60% ZnO, 10% SiO_2, and 3% CeO_2. The fusion temperature of the glass is 700°C and the thermal expansion coefficient is 4.5 x 10^{-6}/°C. The glass adheres well to bare silicon. The only potential problem with (ZBSG) is that it contains boron oxide, which could contaminate the cell at its fusion temperature. Another technique that would make the use of the dielectric more effective is electrophoretic deposition of Al_2O_3. This substance seals the imperfections in the dielectric isolation layer.

There are other techniques to apply the dielectric which would minimize the breakage and isolation problems that were encountered with the methods used in this contract. Among these techniques, anodic oxidation and sputtering stand out as the most promising. The dielectric isolation for anodic oxidation is provided by a layer of silicon dioxide that is grown at room temperature by anodization techniques. The electrolyte for the constant current anodization is a bath containing N-methylacetamide and 0.04 N potassium nitrate. The anodization operates at 300 volts. The anodization cell would have to be designed to maximize the growth on the edge and back of the wafer, and would require development. Sputtered dielectrics are also possible, but transistor usage has indicated device degradation during depositions.

Of all possible methods of depositing the dielectrics on the cells, screen printing still appears to be the most economical method if the proper dielectric material can be found. Screen printing is also compatible with mechanization.

5.0 CONCLUSIONS

Based on the cells fabricated during this contract, it was clear that there was a marked improvement in both efficiency and yield as the wafers were made thicker. The initial intent of this contract was to make a thirteen percent efficient cell that was two to three mils thick. However, after making a two mil cell that had an efficiency of less than ten percent and a yield less than thirty percent, it was clear that this goal could not be achieved with the technology that was used during the contract. The current technology should be used with thicker cells. A thicker cell would solve most of the problems that were encountered under this contract. A thicker cell (greater than or equal to 3 mils) would allow the use of the vacuum hold-down in both the testing and fabrication of the cell. A vacuum hold-down is necessary to stabilize the temperature of the cell during testing and it insures a uniform product during fabrication. A piston post would not be necessary to support the web during processing. A good match between the thermal expansion coefficients of silicon and the dielectric would no longer be critical. No "fillers" would have to be used in the dielectric in order to match the thermal expansion coefficients. A thicker cell would also not need a reinforced perimeter wafer during processing, thereby allowing the wafer to heat and cool uniformly.

Thin cells (2 to 3 mils) could be made with technology not explored under this contract. Such technology could include chemical vapor deposition (CVD), sputtering, or evaporation. These techniques would allow deposition of a dielectric layer that had a matching thermal expansion coefficient on the silicon wafer. These techniques would not create a step on the back side of the wafer that would result in cracking when a vacuum is applied.

6.0 REFERENCES

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6) Thornhill, J.W., "Screen Printing Technology Applied to Silicon Solar Cell Fabrication", Final Report, NASA Lewis Research Center, Contract NAS3-20826, NASA CR-159789, April, 1980.