# AN IMAGING INFRARED (IIR) SEEKER USING A MICROPROGRAMMED PROCESSOR

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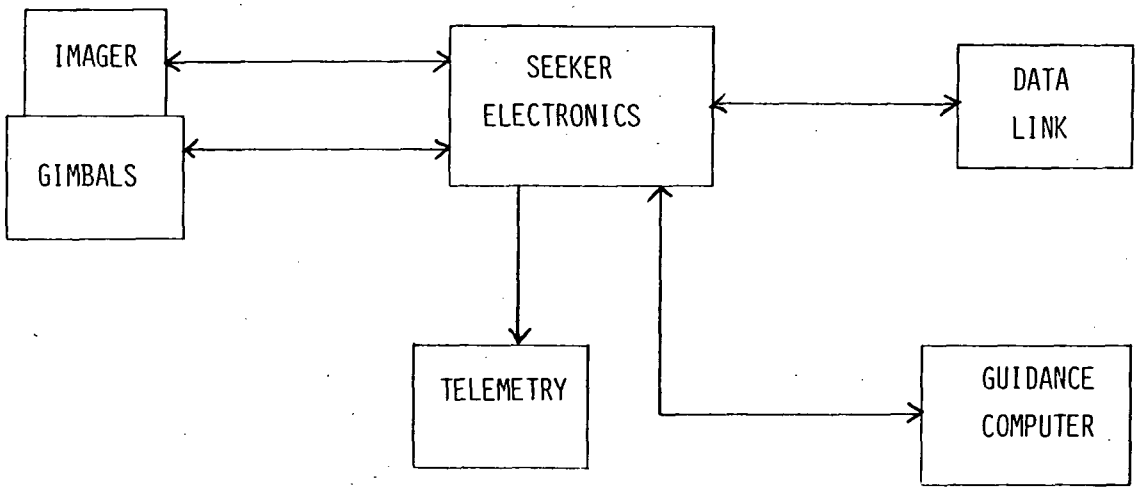
A recently developed IIR seeker uses a microprogrammed processor to perform gimbal servo control and system interface via a MIL-STD 1553 port while performing the seeker functions of automatic target detection, acquisition and tracking. Although the acquisition and centroid tracking are relatively low computation load seeker modes, the automatic detection mode requires up to 80% of the available capability of a high performance 2900 based microprogrammed processor. With the high speed processing capability available it is possible to implement a digital servo in the same processor using only 5% of the computation capacity. This digital servo includes six modes of gimbal control at the basic processor 60 Hz computation loop plus a 200 Hz rate loop, the latter being transparent to the main seeker functions. These two asynchronous timing loops plus a 50 Hz system interface loop driven from the 1553 port are implemented in the one processor. The fast response required by the rate loop for the rate sensor demodulator inputs also requires an interrupt driven analog data acquisition system. A 4K microcode program driven by eight interrupts implements these functions as well as the other operator and system interfaces.

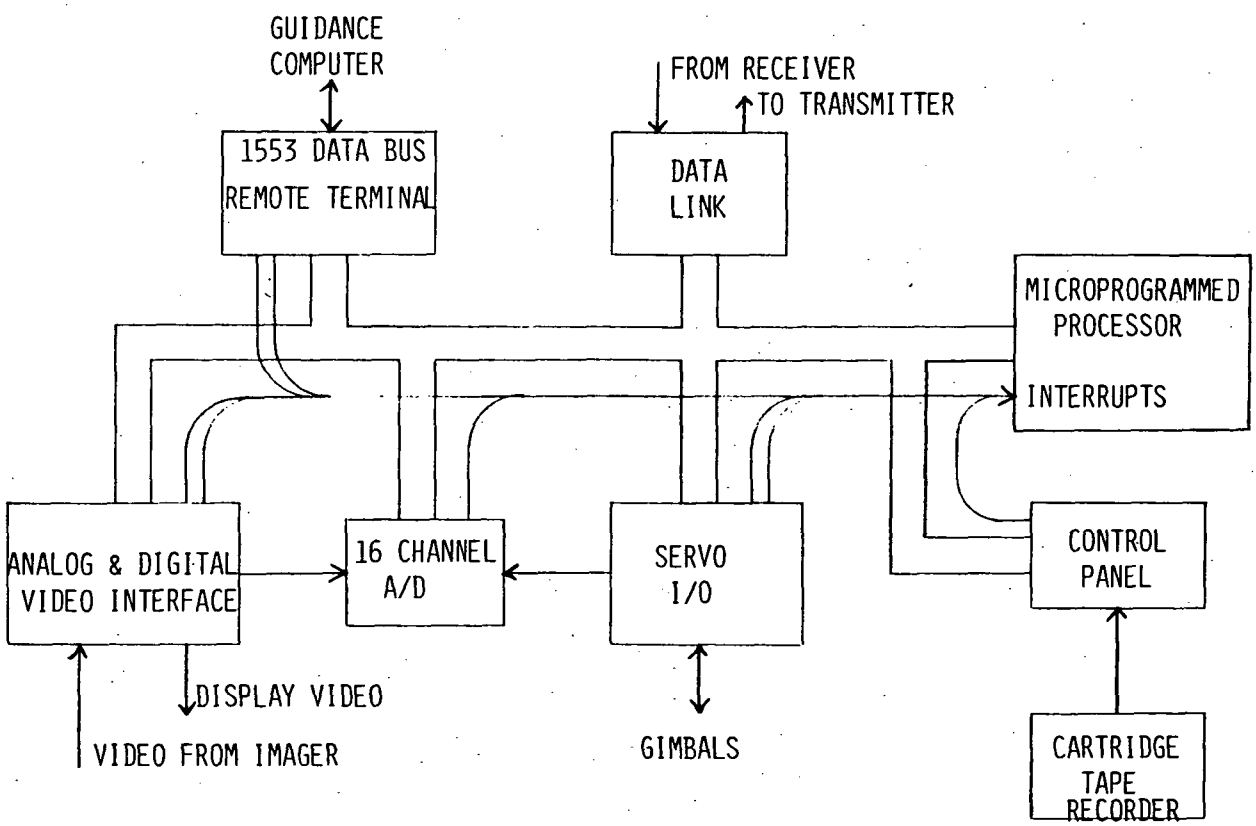
The eighth interrupt is used to force the processor into special "front panel" code which suspends all other interrupt processing and saves the state of the processor to allow the programmer to view the contents of all registers and memory as well as enter new values and resume normal processor execution at the interrupted location or any other selected location. This programmer debug aid in the hardware coupled with a set of support software including a symbolic cross assembler and a software simulation of the 2900 based processor allow efficient program development and checkout.

This system developed around the microcoded processor required by one of the system tasks has been designed, checked out and flown successfully. Although system complexity was increased significantly by adding the additional functions this approach can be cost effective when the basic computation capacity is already available.

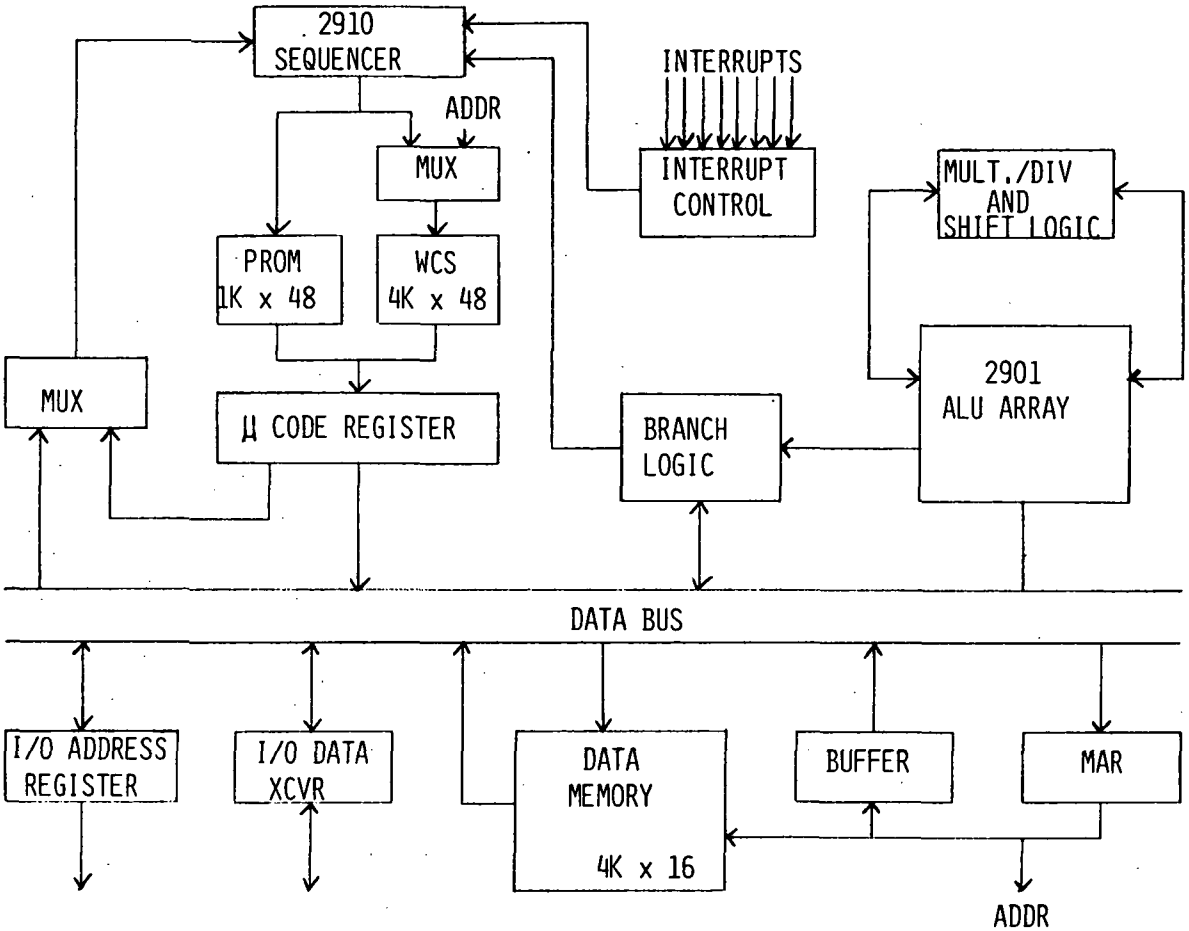
IIR SEEKER MISSILE INTERFACES



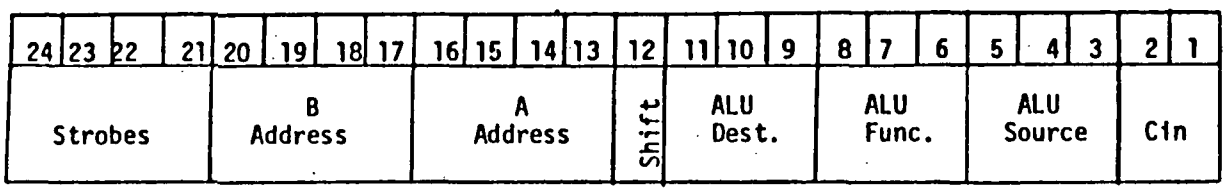

SEEKER BLOCK DIAGRAM

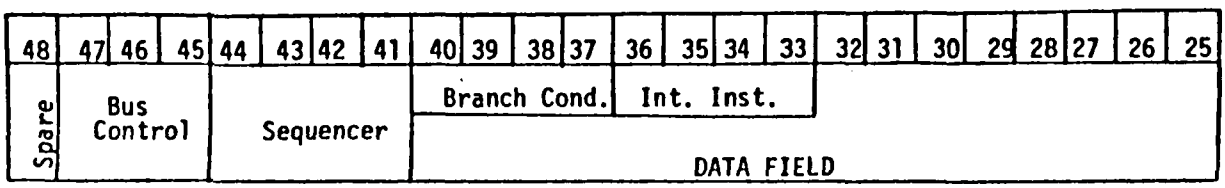


CPU BLOCK DIAGRAM




MICROCODE WORD



## CPU PERFORMANCE/REQUIREMENTS

- 2900 BIT SLICE MICROPROGRAMMED PROCESSOR
- 48 BIT WIDE MICROCODE WORD
- 267 NANOSECOND CYCLE TIME
- 4K PROGRAM MEMORY
- 2K SCRATCH PAD MEMORY
- 8 INTERRUPTS

## SEEKER INTERRUPTS

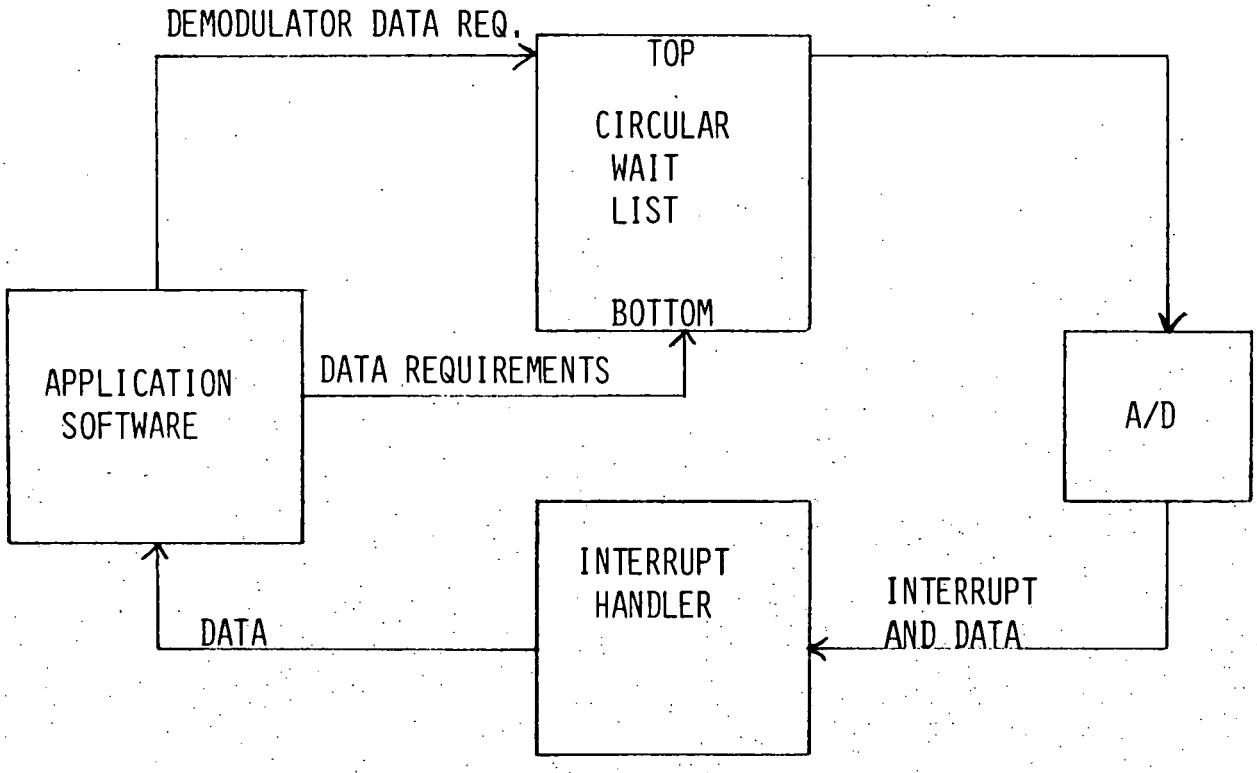
SYSTEM INTERRUPTS
- CONTROL PANEL
- A/D COMPLETION

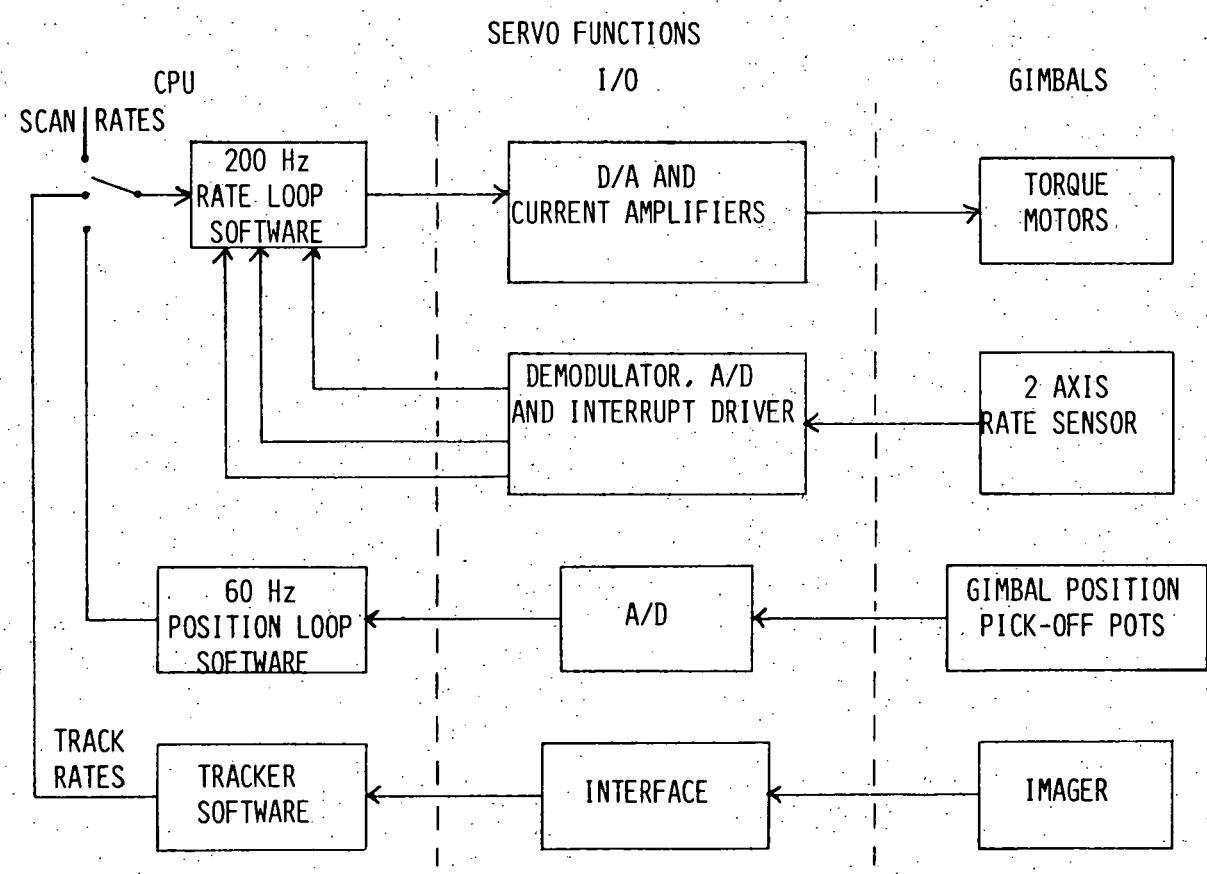
60 Hz MAIN LOOP
- END OF GATE
- END OF FIELD

200 Hz SERVO RATE LOOP
- SAMPLE AZIMUTH DEMODULATOR
- SAMPLE ELEVATION DEMODULATOR

50 Hz GUIDANCE COMPUTER TIMING LOOP
- 1553 INPUT DATA READY
- 1553 OUTPUT DATA READY

## ANALOG DATA ACQUISITION



## FRONT PANEL FUNCTIONS

- READ/LOAD DATA MEMORY
- READ/LOAD REGISTERS
  - CPU
  - I/O ADDRESS
  - MEMORY ADDRESS
  - CONDITION CODE
- READ/LOAD INTERRUPT STATUS
- EXIT/RETURN TO PROGRAM

## SOFTWARE SUPPORT