THE ROLE OF THE MICROPROCESSOR IN ONBOARD
IMAGE PROCESSING FOR THE INFORMATION ADAPTIVE SYSTEM

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The Information Adaptive System (IAS) is an element of the NASA End-to-End Data System program and is focused toward high speed onboard data processing for NASA missions in the 1980's. Particular emphasis is placed on multispectral-image data processing since the speed and quantity of that variety of data places the greatest burden on the current NASA data system. Some of the image processing functions planned for the IAS include sensor nonuniformity correction, geometric correction, data editing, formatting, packetization and adaptive system control.

The design of the IAS is intended to apply to a variety of future missions; therefore, architectural flexibility is a key design feature. The programmability of the microprocessor lends this required flexibility to the system, allowing it to accommdate new processing functions and interface with a variety of sensor configurations. The high throughput rate required for multispectral image data processing prohibits the use of conventional computer software approaches without significant increases in the speed of the central processing unit. Hence, a combination of high speed special purpose hardware and microprocessors for control and computational support, appears to offer the best technical approach for the near term. In addition, a sophisticated microprocessor will serve as the overall system supervisor interfacing with commands from the spacecraft and the ground.

This paper presents the preliminary design of the Information Adaptive System and discusses the role of the microprocessor in the implementation of the individual processing elements.

THE CURRENT NASA DATA SYSTEM PROBLEM

- EVER INCREASING DEMAND MET WITH PROBLEM BY PROBLEM SOLUTIONS.

- CURRENT DATA LOAD – 10" bits/day.

- DATA PROCESSING DELAYS ARE EXCESSIVE.

- DATA PROCESSING COSTS ARE TOO HIGH.

- FORTHCOMING PROJECTS WILL INCREASE DATA LOAD BY AN ORDER OF MAGNITUDE.

- SHUTTLE CAPABILITY WILL BOOST LAUNCH RATE BY FACTOR OF 6.

NEEDS $II-INFORMATION ADAPTIVE SYSTEM

GOAL: DESIGN, DEVELOP AND DEMONSTRATE IN EARLY 1983 A SYSTEM ARCHITECTURE THAT UTILIZES ADVANCED TECHNOLOGY FOR HIGH-SPEED MULTISPECTRAL IMAGE DATA PROCESSING.
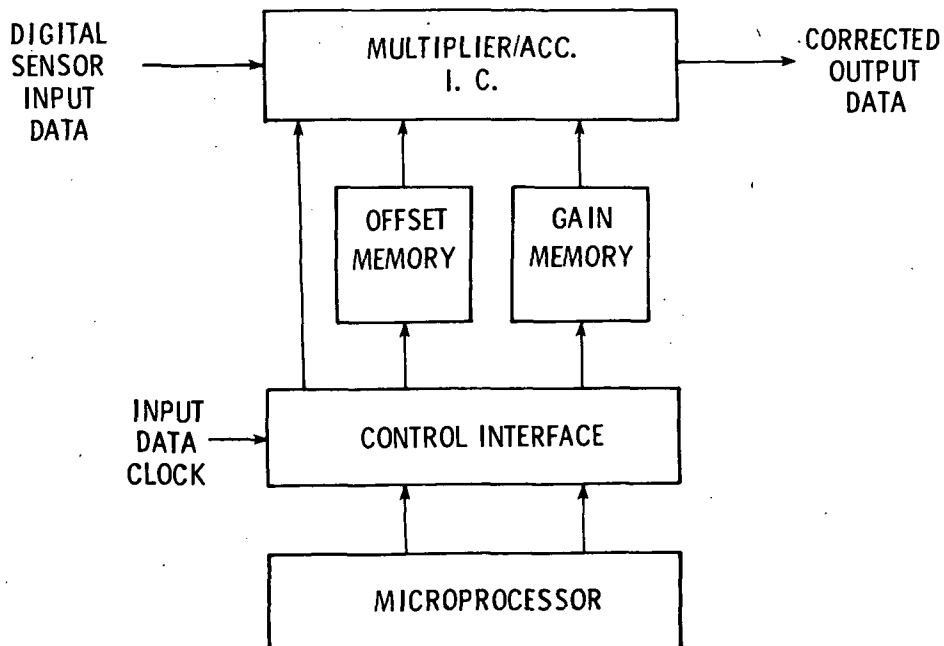
DESIGN
FEATURES:
- HIGH DATA THROUGHPUT RATE
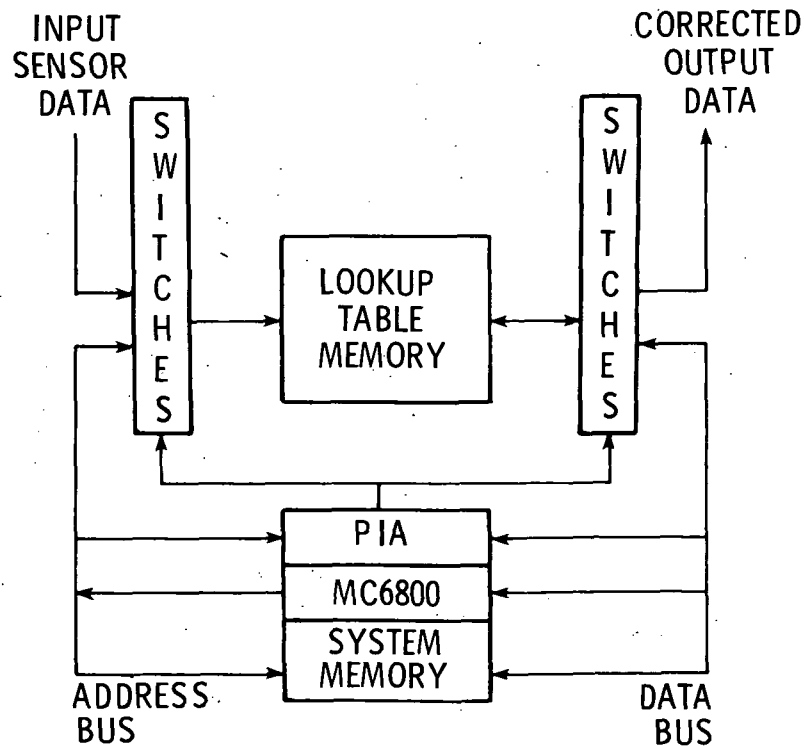- PROGRAMMABILITY
- FLEXIBLE ARCHITECTURE
- ADAPTABILITY

IAS DEMONSTRATION SYSTEM BLOCK DIAGRAM
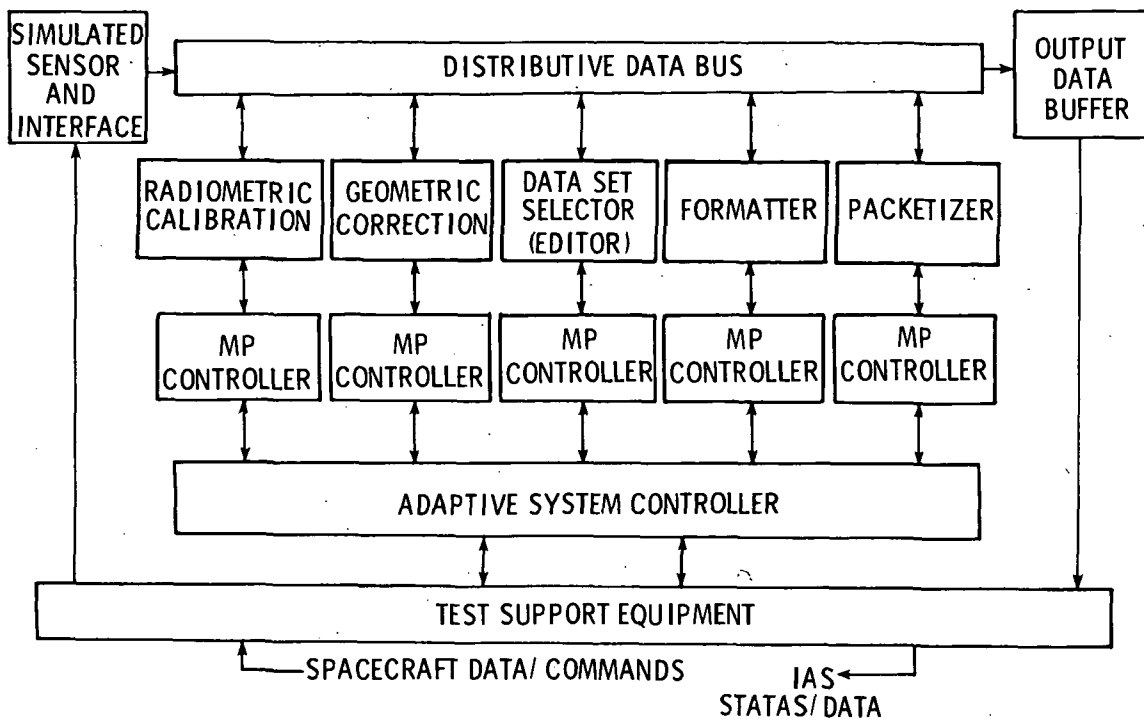
RADIOMETRIC CORRECTION - LINEAR CURVE FIT APPROACH

LOOKUP TABLE DESIGN FOR RADIOMETRIC CALIBRATION

SOURCES OF DISTORTION IN IMAGE DATA AND THEIR

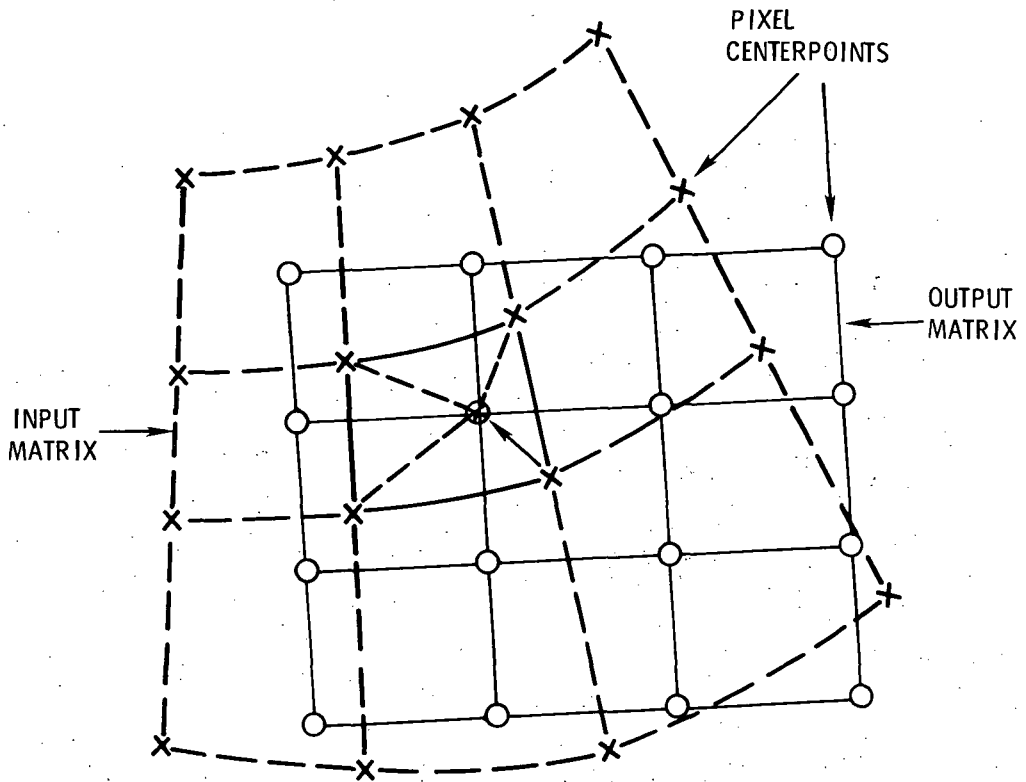# CORRESPONDING ERROR MEASUREMENT TECHNIQUES

EPHEMERIS VARIATIONS ⟶ GLOBAL POSITIONING SYSTEM (GPS)
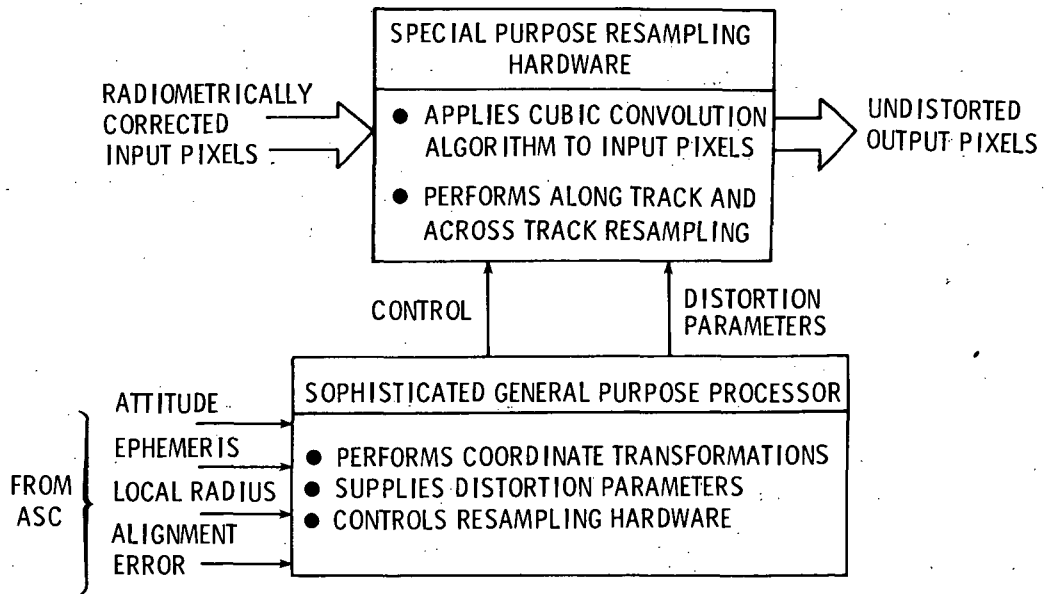
SPACECRAFT ATTITUDE ⟶ ADVANCED STAR TRACKER
VARIATIONS

SENSOR MISALIGNMENT ⟶ PERIODIC GROUND CALIBRATION

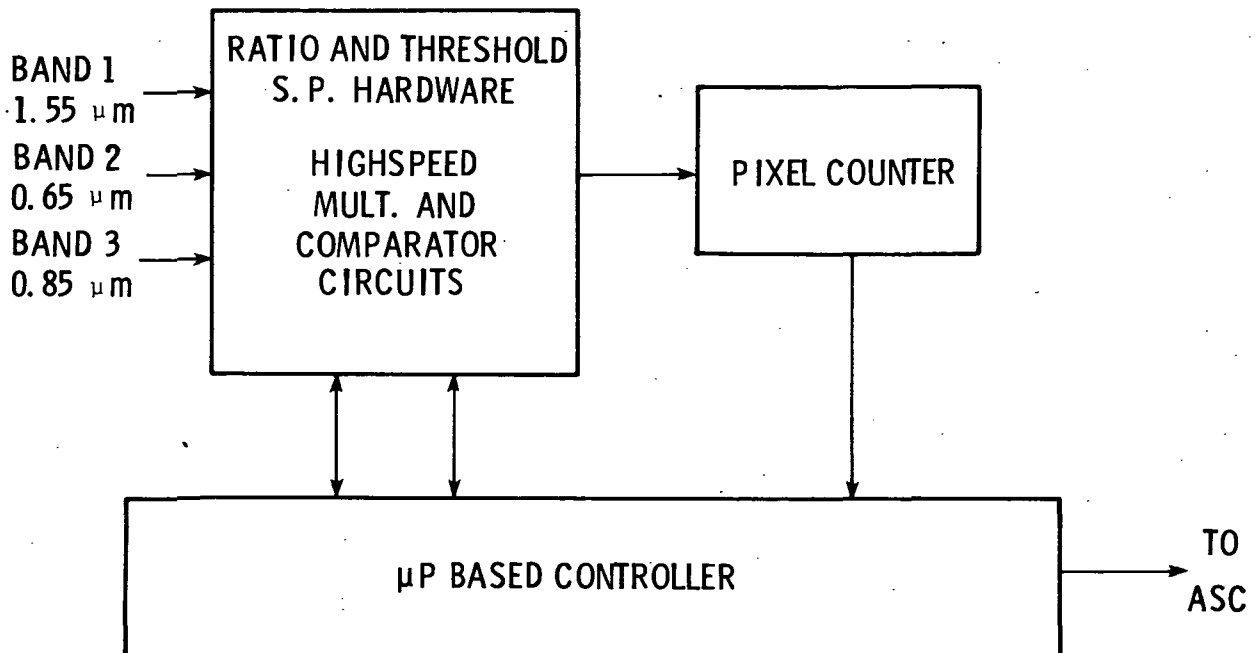EARTH CURVATURE ⟶ GPS WITH LOCAL EARTH RADIUS
INFORMATION

GEOMETRIC CORRECTION

PIXEL CENTERPOINTS

OUTPUT MATRIX

INPUT MATRIX

GEOMETRIC CORRECTION PROCESSING

RADIOMETRICALLY
CORRECTED
INPUT PIXELS

SPECIAL PURPOSE RESAMPLING HARDWARE

● APPLIES CUBIC CONVOLUTION ALGORITHM TO INPUT PIXELS

● PERFORMS ALONG TRACK AND ACROSS TRACK RESAMPLING

UNDISTORTED
OUTPUT PIXELS

CONTROL

DISTORTION PARAMETERS

FROM ASC

ATTITUDE
EPHEMERIS
LOCAL RADIUS
ALIGNMENT ERROR

SOPHISTICATED GENERAL PURPOSE PROCESSOR

● PERFORMS COORDINATE TRANSFORMATIONS
● SUPPLIES DISTORTION PARAMETERS
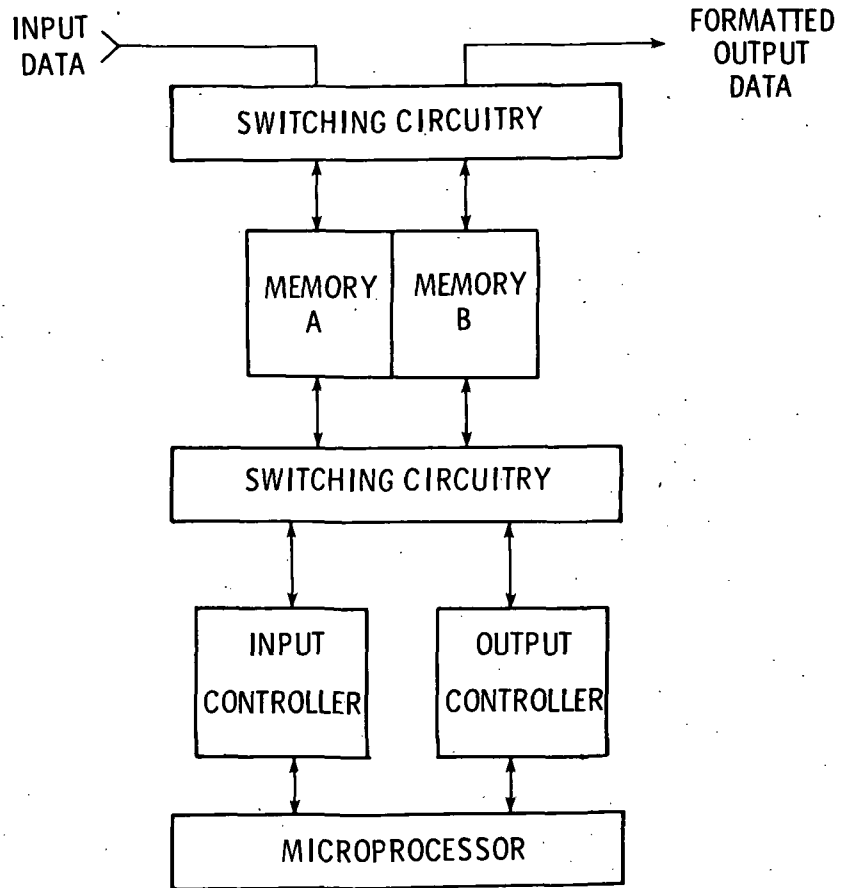● CONTROLS RESAMPLING HARDWARE

EDITING CRITERIA UNDER INVESTIGATION
FOR THE IAS

- TIME

- SPACECRAFT POSITION

- INFORMATION FROM OTHER EXPERIMENTS

- CLOUD COVER

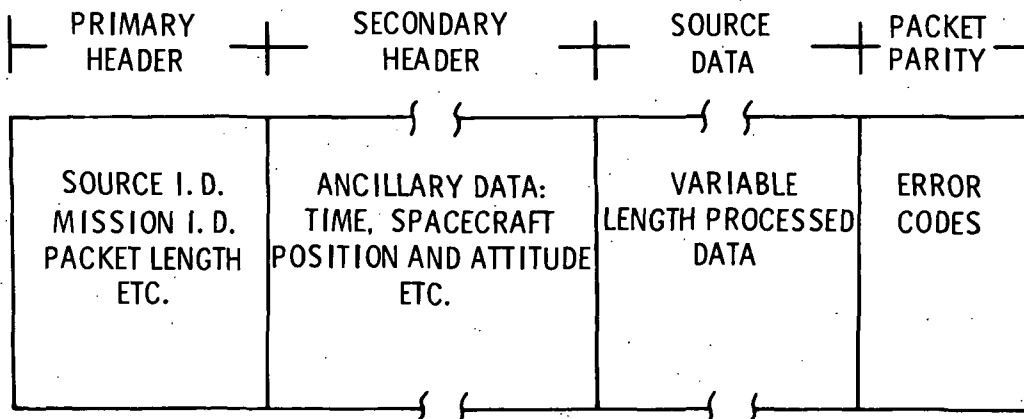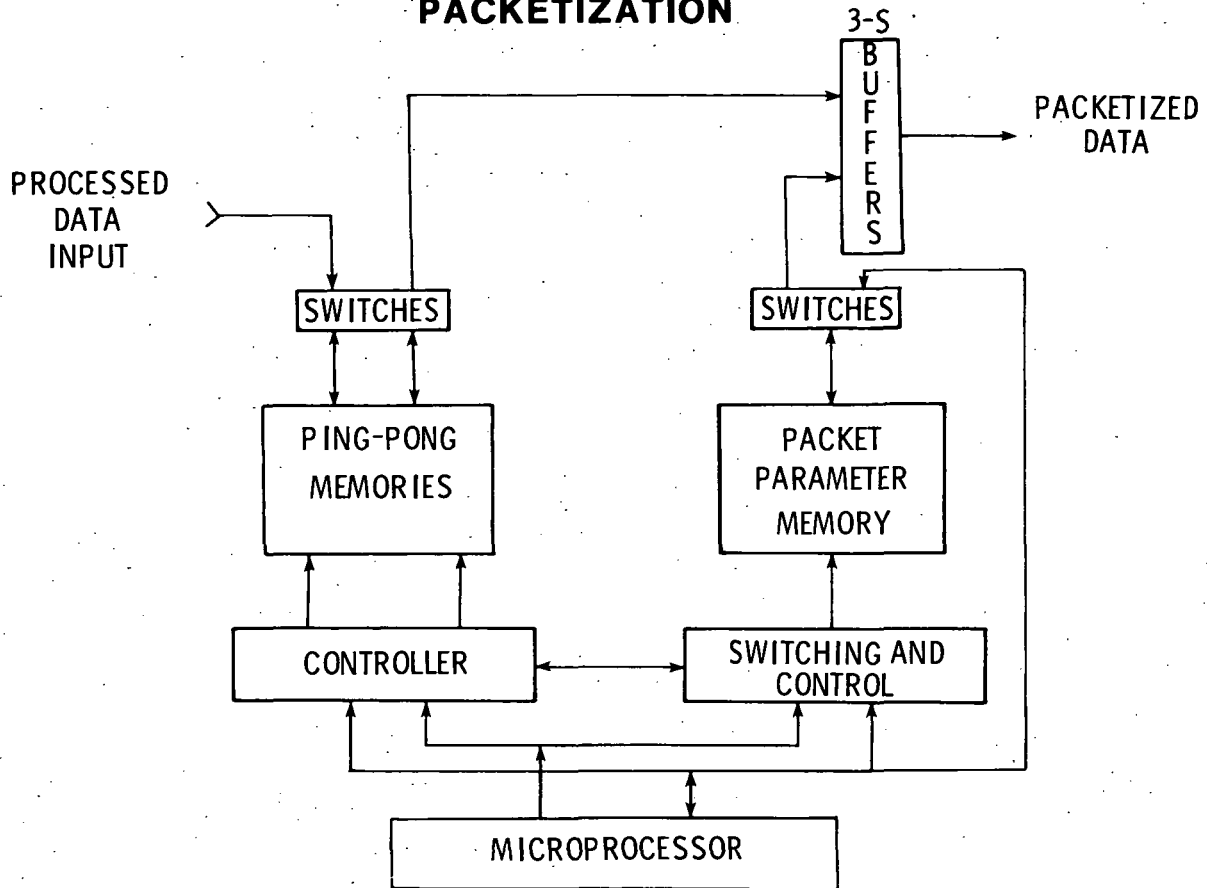## IMPLEMENTATION OF CLOUD DETECTION ALGORITHM

BAND 1
1.55 μm

BAND 2
0.65 μm

BAND 3
0.85 μm

RATIO AND THRESHOLD
S. P. HARDWARE

HIGHSPEED
MULT. AND
COMPARATOR
CIRCUITS

PIXEL COUNTER

μP BASED CONTROLLER

TO
ASC

BUFFER MEMORY SYSTEM FOR DATA FORMATTING

INPUT DATA

FORMATTED OUTPUT DATA

SWITCHING CIRCUITRY

| MEMORY A | MEMORY B |

SWITCHING CIRCUITRY

INPUT CONTROLLER

OUTPUT CONTROLLER

MICROPROCESSOR

NASA DATA PACKET FORMAT

PRIMARY HEADER	SECONDARY HEADER	SOURCE DATA	PACKET PARITY
SOURCE I. D. MISSION I. D. PACKET LENGTH ETC.	ANCILLARY DATA: TIME, SPACECRAFT POSITION AND ATTITUDE ETC.	VARIABLE LENGTH PROCESSED DATA	ERROR CODES

HIGH SPEED PING-PONG MEMORY APPROACH TO DATA PACKETIZATION

ADAPTIVE SYSTEM CONTROLLER TASKS

- INITIALIZE INDIVIDUAL CONTROLLERS

- ASSIST CONTROLLERS IN INITIALIZATION OF IAS COMPONENTS

- ESTABLISH AND MAINTAIN OPERATING MODE

- MONITOR STATUS OF ALL IAS COMPONENTS

- FORMULATE ERROR MESSAGES

- MAINTAIN COMMUNICATION WITH SPACECRAFT AND GROUND

- PROVIDE COMPUTATIONAL SUPPORT TO IAS MODULES

ADAPTIVE SYSTEM CONTROLLER DESIGN FEATURES

- SOPHISTICATED MICROPROCESSOR ARCHITECTURE

- ADAPTABLE

- EXPANDABLE

- COMPATABLE WITH HIGH ORDER LANGUAGE