DISTRIBUTED MICROPROCESSORS IN A TACTICAL UNIVERSAL MODEM

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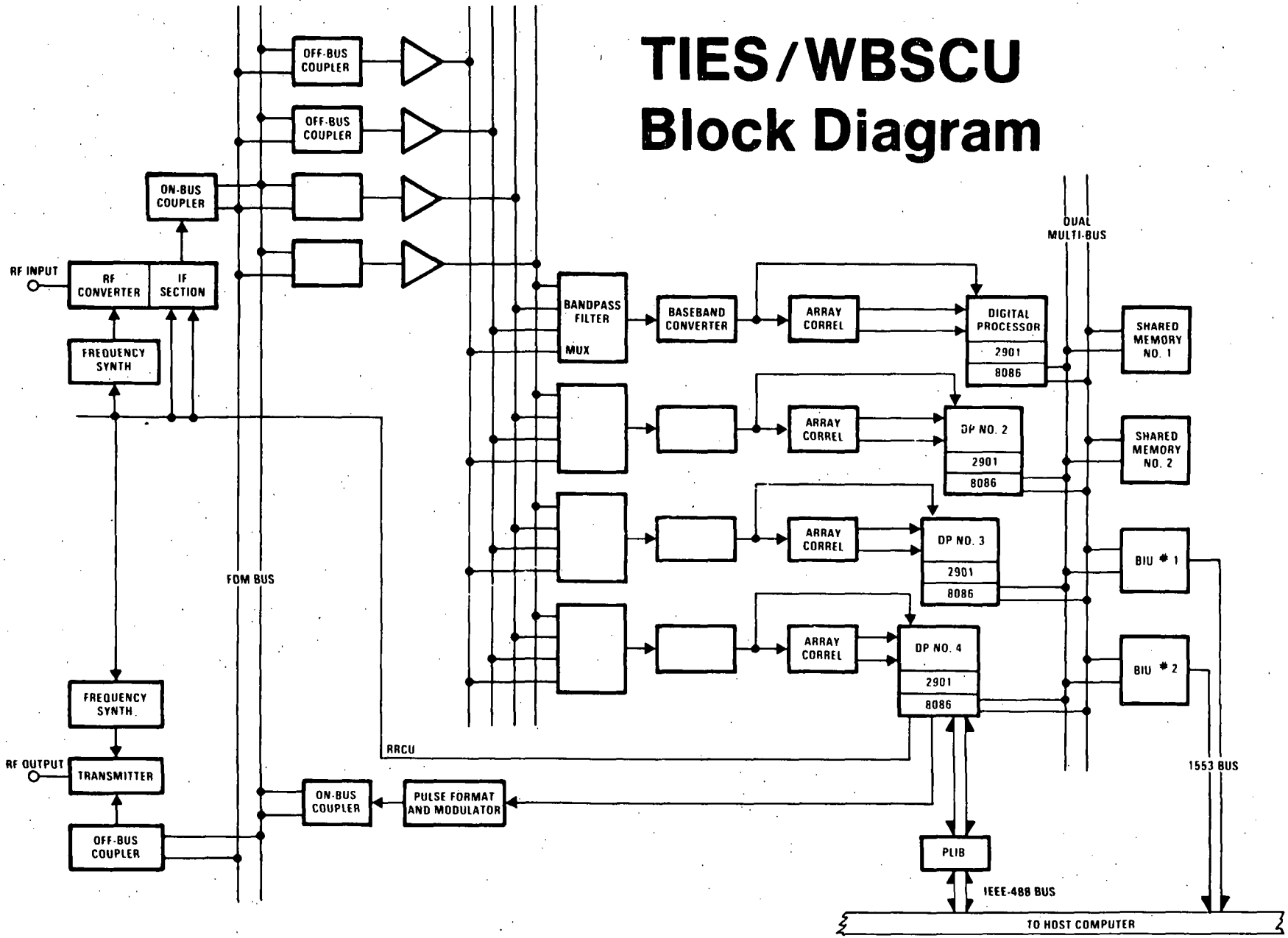
The Wideband Signal Conversion Unit (WBSCU) for the Tactical Information Exchange System (TIES) is a four-channel software reprogrammable modem. System goals are high resource availability, growth potential, reliability, and graceful degradation. The WBSCU processes JTIDS, GPS, IFF/DABS, and TACAN waveforms simultaneously under direction of a host computer. For both complex spread spectrum and pulse-based waveforms, the WBSCU provides matched filtering, signal processing, error detection/correction and encoding/decoding, and data communication via IEEE 488 and MIL-1553 buses.

Multiple embedded 8086 and 2901 microprocessors, supported by dedicated hardware modules, perform the required real-time operations for both transmit and receive functions. Commands from a host computer determine the configuration of the WBSCU via the IEEE 488 bus. Each of the four WBSCU channels is assigned to process a specified IF waveform; each channel configures its own resources and, in some cases, borrows resources from other channels. The processed waveform data is communicated from individual channels to redundant global memories. Data flow between the user community and global memories occurs via redundant 1553 buses through intelligent Bus Interface Units.

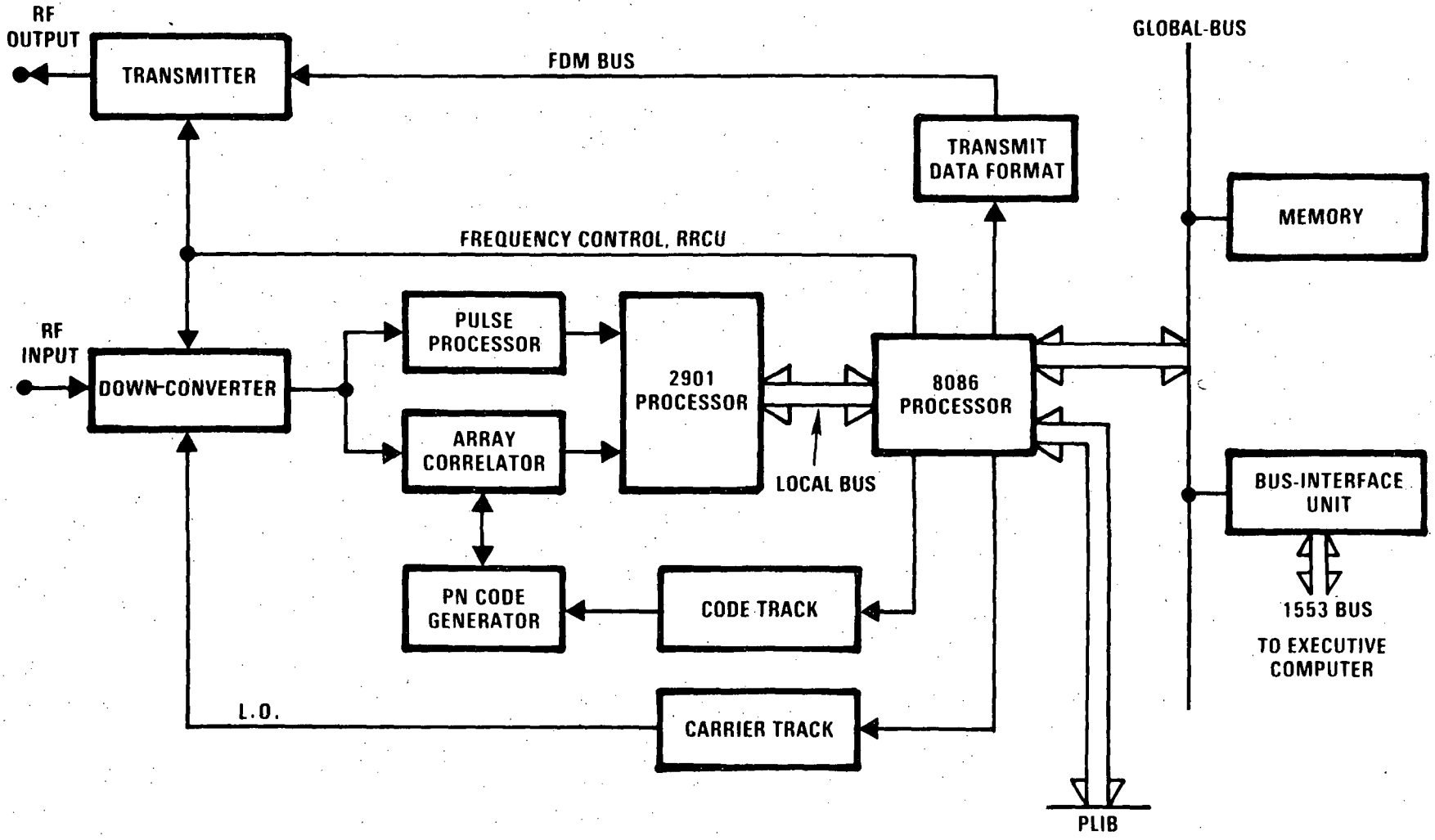
Each WBSCU channel contains one 2901 bit-slice machine and one 8086 microprocessor. The 2901 provides high-speed processing capability for the most time-critical operations. Features include a 16-bit word size, 64-bit microcoded instruction, and 10 MHz instruction throughput. The 8086 is used for lower speed processing tasks where its high level language capability can be better exploited. Each 8086 has a global bus for wideband interprocessor communication, and a local bus for 8086/2901, master/slave communication. Software architecture consists of a control and communications structure governing mode-dependent signal processing tasks.

In GPS data acquisition, the 2901 processes array correlator outputs and generates code and carrier error signals. The 8086 implements the loop filters required to achieve code lock and carrier synchronization, performs error detection and extracts message bits at a 50 b/s data rate. This data is output via the global memory. During JTIDS signal processing, the 2901 controls hardware modules to generate the acquisition strobe and time refine signals, readying the system to receive the data message. The 8086 performs message level data processing for both transmit and receive functions, data routing, and interchannel communications.

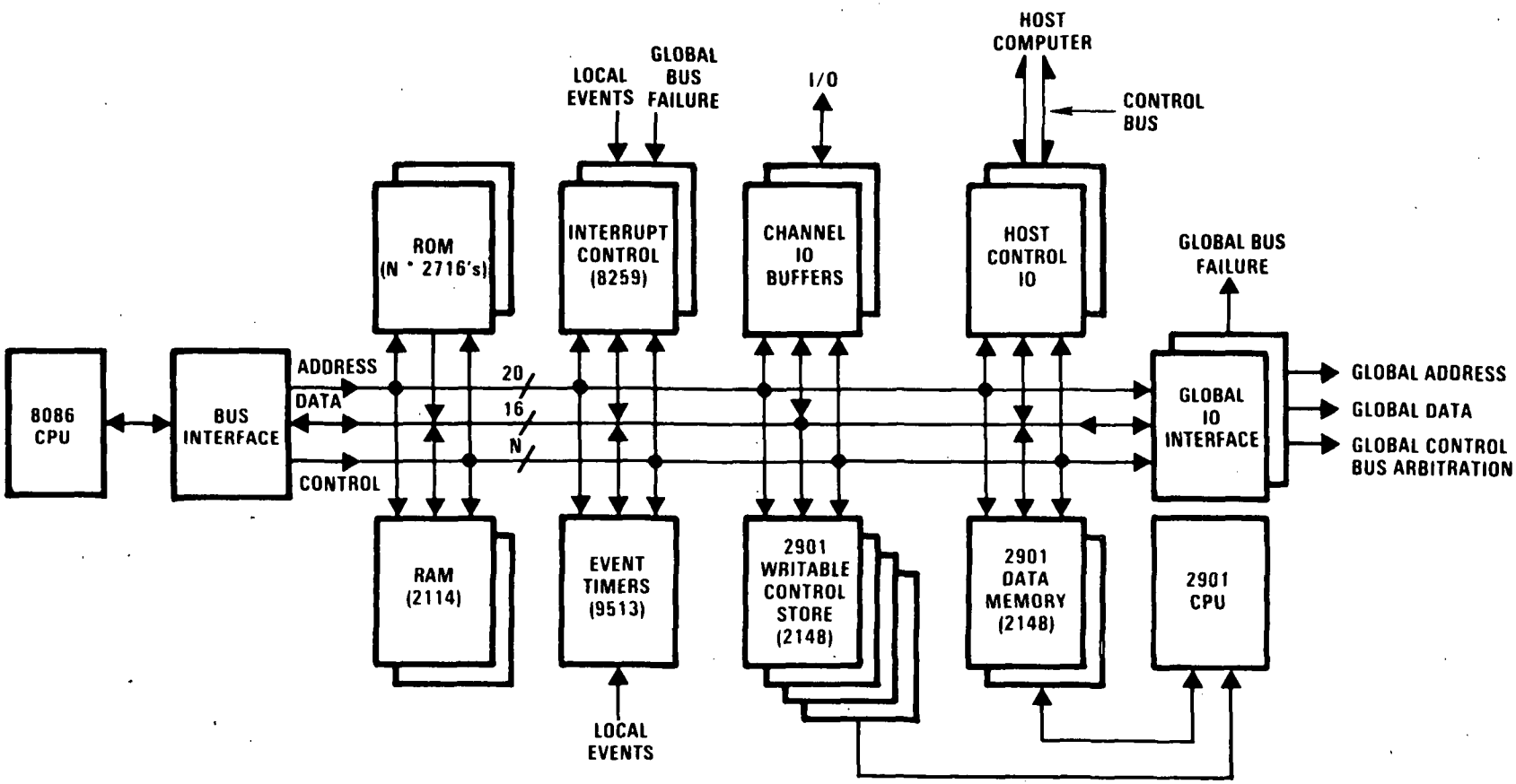
TIES/WBSCU Block Diagram



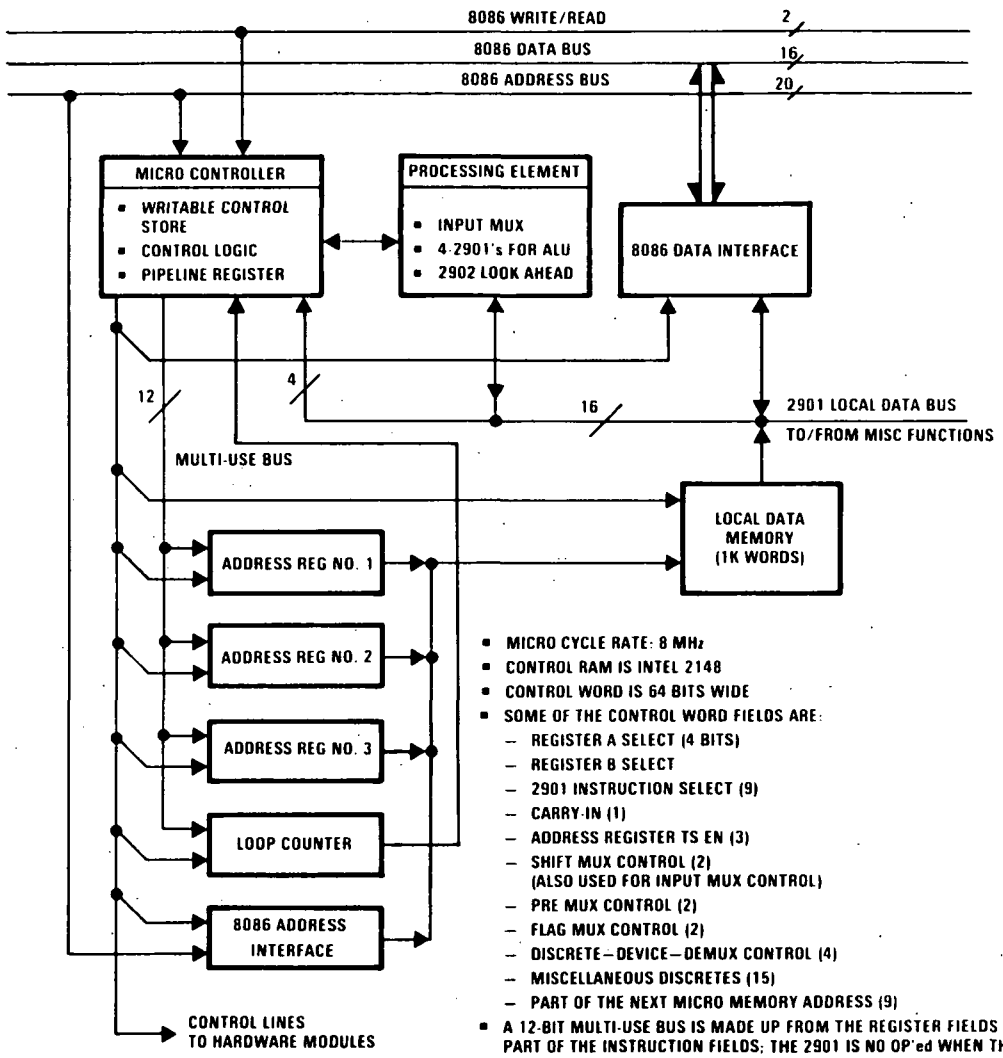
Single Channel WBSCU Configuration



Local 8086 Architecture

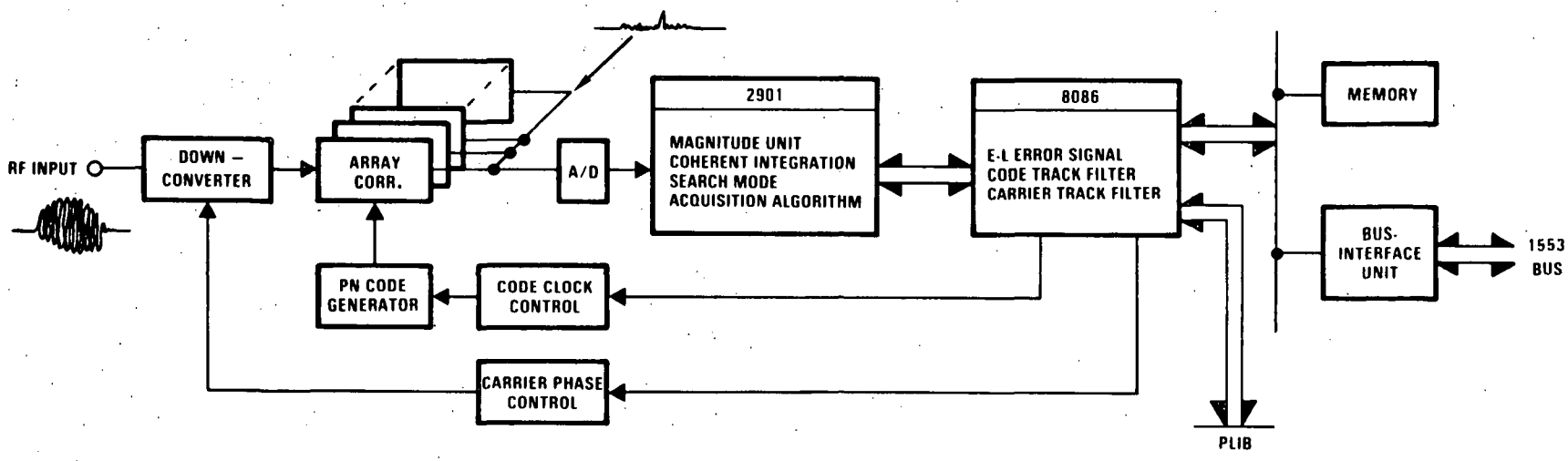


2901 Bit-Slice Microprocessor

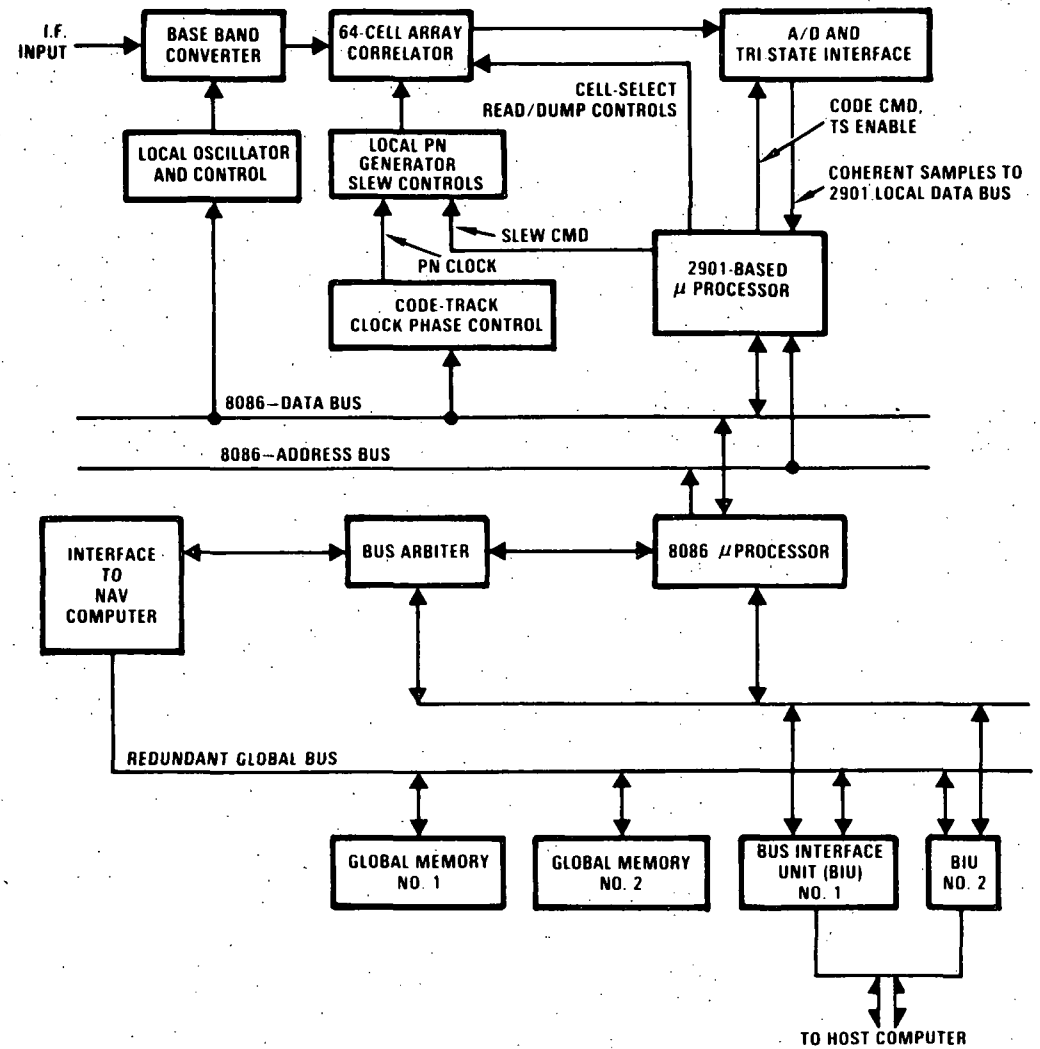


- MICRO CYCLE RATE: 8 MHz
- CONTROL RAM IS INTEL 2148
- CONTROL WORD IS 64 BITS WIDE
- SOME OF THE CONTROL WORD FIELDS ARE:
  - REGISTER A SELECT (4 BITS)
  - REGISTER B SELECT
  - 2901 INSTRUCTION SELECT (9)
  - CARRY-IN (1)
  - ADDRESS REGISTER TS EN (3)
  - SHIFT MUX CONTROL (2) (ALSO USED FOR INPUT MUX CONTROL)
  - PRE MUX CONTROL (2)
  - FLAG MUX CONTROL (2)
  - DISCRETE–DEVICE–DEMUX CONTROL (4)
  - MISCELLANEOUS DISCRETES (15)
  - PART OF THE NEXT MICRO MEMORY ADDRESS (9)
- A 12-BIT MULTI-USE BUS IS MADE UP FROM THE REGISTER FIELDS AND PART OF THE INSTRUCTION FIELDS; THE 2901 IS NO OP'ed WHEN THE MULTI-USE FIELD IS USED

Single Channel GPS Configuration



GPS SYSTEM USES 2901 AND 8086 MICROPROCESSORS



- 8086 TASKS
  - LOAD 2901 WRITABLE CONTROL STORE
  - LOAD CONSTANTS IN 2901 LOCAL DATA RAM
  - SERVICE 2901 INTERRUPTS
  - USE INTEGRATED DATA FROM ON-TIME CELL TO LOCATE GPS DATA BIT BOUNDARIES
  - FILTER INTEGRATED DATA FROM EARLY AND LATE CELLS TO CONTROL CODE-TRACK CIRCUIT
  - FILTER INTEGRATED DATA FROM ON-TIME CELL TO CONTROL LOCAL OSCILLATOR CIRCUIT
  - PASS GPS DATA AND WBSCU CHANNEL STATUS TO GLOBAL MEMORIES
- 2901 TASKS
  - COHERENT INTEGRATION OF CORRELATOR SAMPLES; THIS EXTENDS 64-CELL ARRAY INTEGRATION TIME
  - NON COHERENT INTEGRATION OR VECTOR SUMATION OF SAMPLES PREVIOUSLY INTEGRATED COHERENTLY
  - THRESHOLD DETECTION AND ACQUISITION—TO-TRACK DECISION-MAKING
  - COHERENT INTEGRATION OF DATA SAMPLES FROM THE ON-TIME CELL
  - COHERENT INTEGRATION OF DATA SAMPLES FROM THE EARLY AND LATE CELLS

Single Channel JTIDS Configuration