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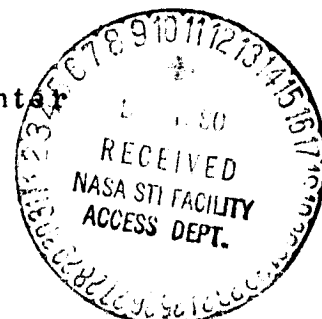REPORT

NASA CR-150783

HIGH SPEED CMOS/SOS STANDARD CELL NOTEBOOK

By RCA
Advanced Technology Laboratories
Government and Commercial Systems
Camden, New Jersey 08102

September 1978

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This work was done under the technical supervision of Mr. Teddy M. Edge, George C. Marshall Space Flight Center, Alabama.

16. ABSTRACT

This report describes the NASA/MSFC high speed CMOS/SOS standard cell family. The cells were designed to be compatible with the PR2D (Place, Route in 2-Dimensions) Automatic Layout Program. Included are cell descriptions and the standard cell data sheets for each cell. Each cell sheet includes the logic diagram, the schematic, the truth table, and propagation delays for each logic cell.

17. KEY WORDS

19. SECURITY CLASSIF. (of this report) Unclassified	20. SECURI Unc

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LIST OF CMOS/SOS STANDARD CELL DATA SHEETS

LIST OF CMOS/SOS STANDARD CELL DATA SHEETS (Concluded)

I. INTRODUCTION

This report describes the NASA-MSFC high speed CMOS/SOS standard cell family, which was developed on (1) NASA programs NAS12-2233 and NAS8-29072 under the direction of John Gould, NASA Technical Program Director, MSFC, Huntsville, Alabama, and (2) internal Independent Research and Development programs.

The circuits were designed to be compatible with and maximize the performance of the Automatic Placement and Routing Program PR2D which was also originally developed under NASA program NAS12-2233 directed by John Gould and improved on other Government programs as well as on several Independent Research and Development programs. Together the program and circuits provide the capability of generating high speed, high performance, random logic custom LSI arrays with quick turnaround, high density, and low static and dynamic power.

The basic technology with which circuits are designed is the self-aligned, silicongate CMOS/SOS process.

These cells are used in the generation of design automated custom LSI arrays in virtually the same manner as other RCA-designed standard cell families. Briefly this requires user-generated input data to the computer program which consists of the net or connectivity list of circuit cells as well as the cell or pattern identification number which is available from the data sheets. With essentially this information, the computer placement and routing program will provide an automatically generated layout and interconnection in a data format consistent and compatible with an automatic precision mask artwork pattern generator.

This report contains standard cell data sheets for each of the cells. It contains a description of the general information and data that are contained on all data sheets. It also contains additional information and descriptions where appropriate. For example, additional information is provided as to how the dynamic performance curves shown on the data sheets were generated, the validation process, and the means by which their accuracy will be updated. A user's guide is planned, which will complement the data contained here, to provide the design information necessary for complete user utilization.

II. HIGH SPEED CMOS/SOS STANDARD CELL FAMILY

A. CELL DESCRIPTIONS

The table lists the cells that currently make up the CMOS/SOS standard cell family. Data sheets are contained for these cells in the Appendix. Where necessary, the accompanying table contains information additional to that on the data sheets to describe cell operation.

Each data sheet contains the following information:

- Cell family technology.

- Descriptive name of the cell indicating its function.

- Cell identification or pattern number. This number identifies the cell in the input data to the automatic placement and routing program.

- Supply voltage for which the given propagation delay and transition times are applicable.

- Width of the cell in mils.

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- Circuit schematic of the logic configuration including the numbering of each input and output connection. These numbers provide the means by which the chip interconnection or net list is generated.

- Capacitance at each input and output connection. This capacitance is computed on the basis of the geometry, topology, and materials associated with the capacitor. The Miller effect is not included in value. It is automatically included when the device is analyzed by computer simulation techniques.

- Logic symbol plus the Boolean equation describing the cell function.

- Truth table.

- Dynamic performance data.

Dynamic performance data at $V_{DD} = 10$ V is provided for each logic cell. These data may be presented in several ways. These include propagation delay on a per stage basis, transition time, clock rate, minimum or maximum pulse width, delay measured with respect to the clock, or combinations of these. In all cases the dynamic data are given as a function of load capacitance.

For logic cells like the 1120, 1130, 1140, 1220, 1230, 1240, 1310, 1520 and the 1620, the delay is given in the form of curves showing stage delay and transition times as a function of capacitive loading. The stage delay is the average of the propagation delay as measured at the 50 percent signal swing level for positive and negative going input signals. Similarly, the transition time is measured over the 10 to 90 percent rise and fall times. The input signal to these circuits during the generation of these data is the output of an inverter stage which acts as a buffer against the programmed input pulse. The principal objective of this buffer is to minimize the effect of the transition time of the input on the dynamic data. The dependency, nevertheless, exists and should be considered.

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In contrast to this, the dynamic data for those circuits which contain storage devices are given in terms of the minimum pulse width to transfer new data into the master and slave storage elements as well as propagation delay data. In the latter case, the delay is specified from the 50 percent level of the negative transition of the clock to the 50 percent level of the output of the slave.

As new cells are added to the CMOS/SOS family, they will be dynamically characterized in a manner that will optimize the cell's usefulness to the system designer.

B. PROCEDURE FOR GENERATING DYNAMIC DATA

The dynamic data shown on the data sheets are based on computer simulation techniques using a RCA-developed computer circuit analysis and simulation program. Primarily developed for integrated circuit application, the program contains specially developed device models with parameters expressed in process parameters as well as circuit parameters. To characterize a particular process, the parameters of the device models are provided values that correspond directly to the process being used.

A detailed description of how the dynamic data were generated can be found in the final report.[1]

Briefly, however, each cell was simulated as follows: all transistors were simulated by a device model that included its mask geometries; electrical characteristics like threshold voltages; intrinsic capacitances, process parameters values for mobility, gate oxide, field oxide thickness, and permitivity;

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1. P. Ramondetta, A. Feller, R. Noto and T. Lombardi, "CMOS Array Design Automation Techniques," Final Report on Contract NAS12-2233 Mods 6 and 11, RCA Advanced Technology Laboratories, Camden, New Jersey, May 1975.

effect of lateral diffusions expressed in terms of modified channel length; and resistance associated with the polysilicon gate and intracell connections. Each cell was analyzed with a load that consists of a series resistor and capacitive load. The series resistor represents the anticipated average resistance that a typical cell will be driving as a result of polysilicon interconnections. In addition, the cell being analyzed is driven by an inverter circuit which is designed to provide a signal that simulates the input signal which it normally encounters in a CMOS/SOS LSI array environment.

A key to the accuracy and reliability of the results produced by the analysis and simulation techniques lies in the accuracy and validity of the values used to define the parameters of the device models. To date RCA has produced more than 50 CMOS/SOS LSI arrays including at least four test chips. Although all of the test chips, including the one described in the reference NASA final report, were designed for different purposes, each one had special circuits designed to characterize the process and generate device model parameter values. Then, as the various functional CMOS/SOS arrays were fabricated and tested, the values of the parameters were improved and updated. In this way, the accuracy and validity of the model are established with a corresponding increase in the accuracy and validity of the performance predicted by the simulation techniques. As additional CMOS/SOS LSI arrays are produced using the CMOS/SOS standard cell family, the model and its parameter values will continue to be improved and updated.

Although the stage propagation delays and transition times given in the data sheets are specifically for a 10-V V_{DD}, they can be used to a first-order approximation to provide corresponding cell information at supply voltages other than 10 V. For example, at 5-V V_{DD} and assuming a threshold voltage for P and N at 1.5 V, the delay will be reduced as compared to the 10-V data as follows:

Reduction in stage delay at 5 V = $\left[\dfrac{(10 - 1.5)^2}{(5 - 1.5)^2} \right] \cdot \left(\dfrac{5}{10} \right) \cdot (0.8) = 2.4$

The 0.8 factor in the equation is an empirical figure that is considered reasonably conservative.

C. ADDITIONAL CELL DATA

1. D-Type, Master/Slave Flip-Flop (Cell No. 2820)

This cell is a true master-slave flip-flop designed for various register applications. With the addition of an external inverter, such as the 1310 or 1520 cell, it may be used for counter and toggle applications. Information is stored by means of tristate type devices, ensuring a data input characteristic that is purely capacitive. Data present at the "D" input are transferred to the "Q" output during the negative-going transition of the clock pulse. Loading the master flip-flop is initiated on the positive-going edge of the clock pulse.

Operating Characteristics

● Clock should remain in the high state for a minimum of 22 ns to insure a proper transfer of the data information into the master flip-flop.

● The clock should remain in the low state for a minimum of 20 ns to insure a proper transfer of the master data to the slave flip-flop.

● The clock transition (10-90 percent) edge time should be kept below 60 ns.

● For output loading on "Q" greater than 0.4 pF, allow a minimum of 26 ns to transfer the data to slave and latch it in.

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The cell is implemented with a combination of functional, transmission gate, and tristate logic. The transmission devices are used to connect (and disconnect) the master and slave storage devices from the "D" input and master rank, respectively. Each storage element is implemented with a single inverter and a low conductance feedback tristate device. Information is held by means of the smaller, high impedance tristate inverter. The outputs of these tristate inverters are disconnected while their particular flip-flop is being loaded. Latch-up occurs during the transition time of the clock signal, during the falling edge for the master flip-flop, and during the rising edge for the slave flip-flop. At this time, the transmission devices are disconnecting. When the clock signal is high, the logical level at the "D" input is propagated through the first transmission device and loaded into the inverter of the master flip-flop. When the clock signal goes from a high to a low (1 to 0) state, two simultaneous events occur. The master's tristate begins to maintain and define the logical level at the input to the master rank, and the input transmission device begins to isolate the master rank from the "D" input. Concurrent with these events, the second transmission device begins to connect the slave to the master. Opposition from the slave's feedback tristate is eliminated by disconnecting the output from this node.

2. Off-Chip Inverting Buffer Pad (Cells No. 9060 and 9070)

These cells are designed for driving large off-chip capacitive loads. To increase the gate density of the arrays using the drivers, the cells have been incorporated into an output pad design. Consequently, they are placed in the pad area. The two cells differ only in their ground and power bus connection.

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TABLE. HIGH SPEED CMOS/SOS STANDARD CELL LIBRARY

Cell Number	Cell Function	Description/Comments
1120	Two-Input NOR	Logical NOR
1130	Three-Input NOR	Logical NOR
1140	Four-Input NOR	Logical NOR
1220	Two-Input NAND	Logical NAND
1230	Three-Input NAND	Logical NAND
1240	Four-Input NAND	Logical NAND
1310	Buffer Inverter	On-chip operation with loads up to 4 pF
1340	Inverting 2×1 Multiplexer	When the control is in the high state (10 V), the output is $\bar{A}$. When the control is low, the output is $\bar{B}$.
1370	Low Z Transmission Gate	Electronic equivalent of a single pole, single throw switch. When the control is in the low state, the input and output are effectively disconnected and the other node either floats or is defined by other circuit elements. In the high state, the transmission gate is in the "ON" state with the output connected to the input with a series resistance of approximately 2000 ohms.
1510	Non-Inverting Buffer	Primarily designed for "on-chip" use, this cell can be used to reduce delays when the load capacitance exceeds 2 pF.

TABLE (Continued)

Cell Number	Cell Function	Description/Comments
1520	Double Buffer Inverter	For capacitance loads in excess of 4 pF
1570	On-Chip Tristate	This cell is a tristate device designed for on-chip use. A control is available to determine the operation mode of this cell. With the control high, the cell operates as an inverter buffer capable of driving heavy on-chip loads. With the control low, the cell is in the "OFF" state, with an extremely high output impedance — on the order of 0.1 pF. This permits the use of bidirectional busses on the chip.
1620	Two-Input AND	Logical AND through two functional stages
1630	Three-Input AND	Logical AND through two functional stages
1640	Four-Input AND	Logical AND through two functional stages
1720	Two-Input OR	Logical OR through two functional stages
1730	Three-Input OR	Logical OR through two functional stages
1740	Four-Input OR	Logical OR through two functional stages
1870	Two, Two and-Two NOR	This cell performs the function $Z = \overline{AB+CD}$. Drive capability and performance are similar to the 1120 type cell.

TABLE (Continued)

Cell Number	Cell Function	Description/Comments
1890	Two, Two, Two And-Three NOR	This cell performs the function $Z = \overline{AB+CD+EF}$. Drive capability and performance are similar to the 1130 type cell.
2000	J/K Flip Flop with Set/Reset	This cell is one of the more complex of the standard cells. Both the set and reset are unconditional except that the two positive pulses must not be applied simultaneously. The truth table, shown below, was extracted from the data sheet.

$$
\begin{array}{cccccl}
C & J & K & S & R & Q \\
\text{↘} & 0 & 0 & 0 & 0 & Q_{n-1} \\
\text{↘} & 1 & 0 & 0 & 0 & 1 \\
\text{↘} & 0 & 1 & 0 & 0 & 0 \\
\text{↘} & 1 & 1 & 0 & 0 & Q_{n-1} \\
\text{↗} & * & * & 0 & 0 & Q_{n-1} \\
* & * & * & 1 & 0 & 1 \\
* & * & * & 0 & 1 & 0 \\
* & * & * & 1 & 1 & \text{Prohibited}
\end{array}
$$

Note: Q_{n-1} is state of flip-flop before last clock transition

* Don t care condition

Cell Number	Cell Function	Description/Comments
2020	D-Type, M/S, S/R Flip-Flop	This is another of the more complex of the standard cells. Both the set and reset are unconditional except that the two positive pulses must not be applied simultaneously. The truth table, shown below, was extracted from the data sheet.

Cell Number	Cell Function	Description/Comments
		C_{lock} D R S Q $\overline{Q}$ ⬂ 0 0 0 0 1 ⬂ 1 0 0 1 0 * * 1 0 0 1 * * 0 1 1 0 * * 1 1 ■ ■ * — Don't Care Case ■ — Undefined Output Case
2310	Exclusive OR	Exclusive OR through a unique combination of four transistors.
2570	Off-Chip Tristate Pad	A special off-chip tristate device with 5 times the drive power of the 9020/9050 cell.
2810	D Flip-Flop with Inverter Output	This cell is one of three latches in the cell family. This cell provides all the functions of the 2830 cell except that it provides an output in which the polarity of the data is inverted.
2820	D Type Master-Slave Flip-Flop	See Section II C 1.
2830	D Flip-Flop with Open Feed-Back Loop	This cell performs the function $Q = D\overline{C} + Q_{n-1} C$ where D is the data input, C is the clock or control element, Q is the output of the latch and Q_{n-1} is the state of the latch prior to application of the negative clock. This cell can be used as an input or output register element, for buffering, for temporary storage, and as a control flip-flop.

TABLE (Continued)

Cell Number	Cell Function	Description/Comments
2840	D Flip-Flop with Reset	This cell is the third of the latch type cells in the CMOS/SOS cell family.
7000	PLA Input Decoder	This cell, together with the 7010, provides a PLA function. This cell provides a full three-input decoded output with an inhibit control that permits expandability. Functionally the cell consists of eight 4-input gates with each providing the full 3 data input decoding.
7010	PLA Output Function String	This cell provides the programmable part of the PLA through mask programming. It essentially provides the "OR" function and may be cascaded serially to provide more complex logic functions.
9020/ 9050	Off-Chip Tristate Pad	These cells are tristate high current drivers designed to drive high capacitance "off-chip" loads. The state of these cells are determined by a control input. When the control is high the cells are low Z, non-inverting buffers. when control is low, devices become high impedance devices that may be common bussed or phantom ORed. The two cell types are distinguished by their location and orientation in the street area.
9030/ 9040	Input Inverter Buffer Pad	An input pad that provides waveform shaping buffering and signal inversion.

TABLE (Concluded)

Cell Number	Cell Function	Description/Comments
9060/ 9070	Off-Chip Inverting Buffer Pad	See Section II C. 2.
9130/ 9140	Buffered Non-Inverting Input Pad	An Input pad that provides waveform shaping and buffering with no signal inversion.

APPENDIX

CMOS/SOS STANDARD CELL DATA SHEETS

TWO–INPUT NOR

SOS STANDARD
CELL NO. 1120

4 DEVICES

3 PADS **CELL WIDTH = 3 MILS** V_{DD} = 10 V

SCHEMATIC

PIN	CAPACITANCE (pF)
2	0.030
3	0.265
4	0.265

LOGIC SYMBOL

$X = \overline{A + B}$
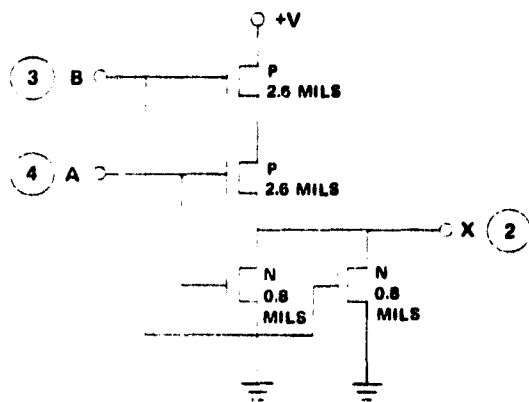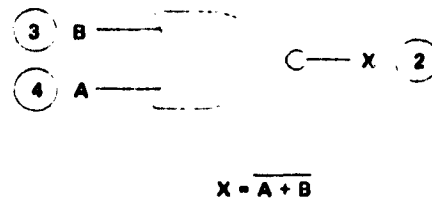
TRUTH TABLE

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0
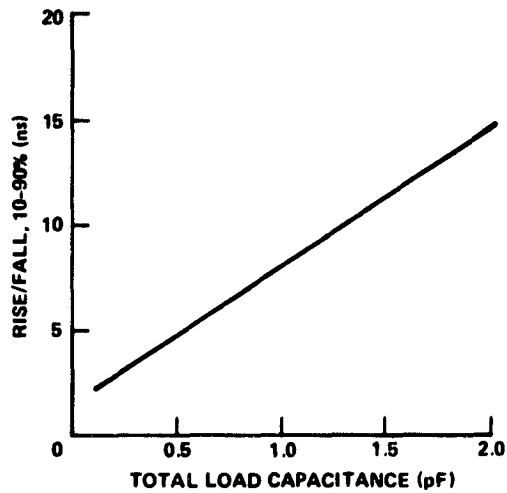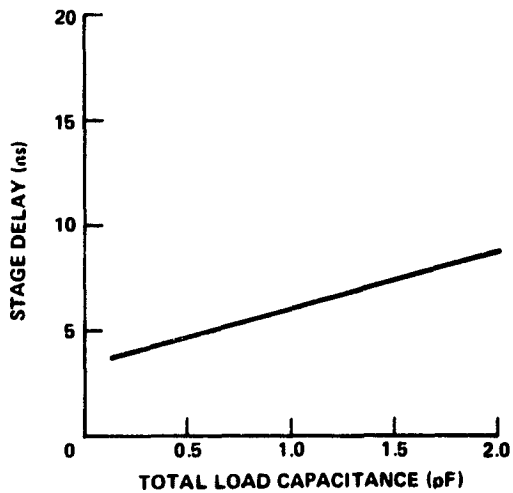
THREE—INPUT NOR

SOS STANDARD
CELL NO. 1130

6 DEVICES

4 PADS   **CELL WIDTH = 4 MILS**

$V_{DD} = 10$ V

SCHEMATIC

LOGIC SYMBOL

$$X = \overline{A + B + C}$$
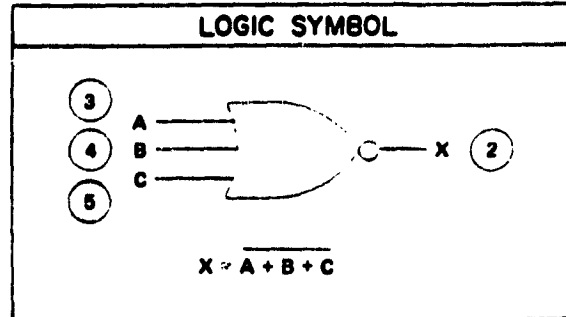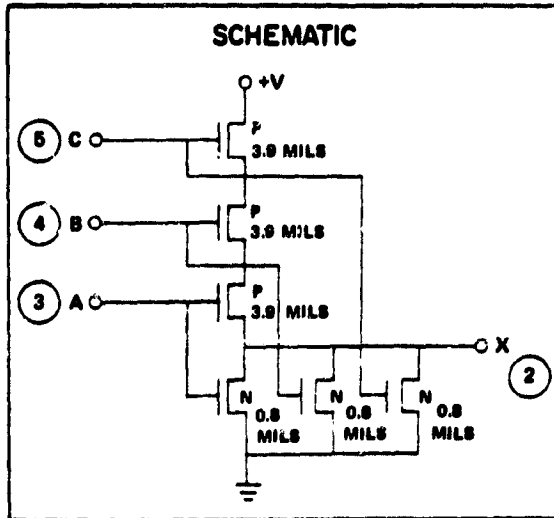
PIN	CAPACITANCE (pF)
2	0.060
3	0.375
4	0.375
5	0.375

TRUTH TABLE

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0
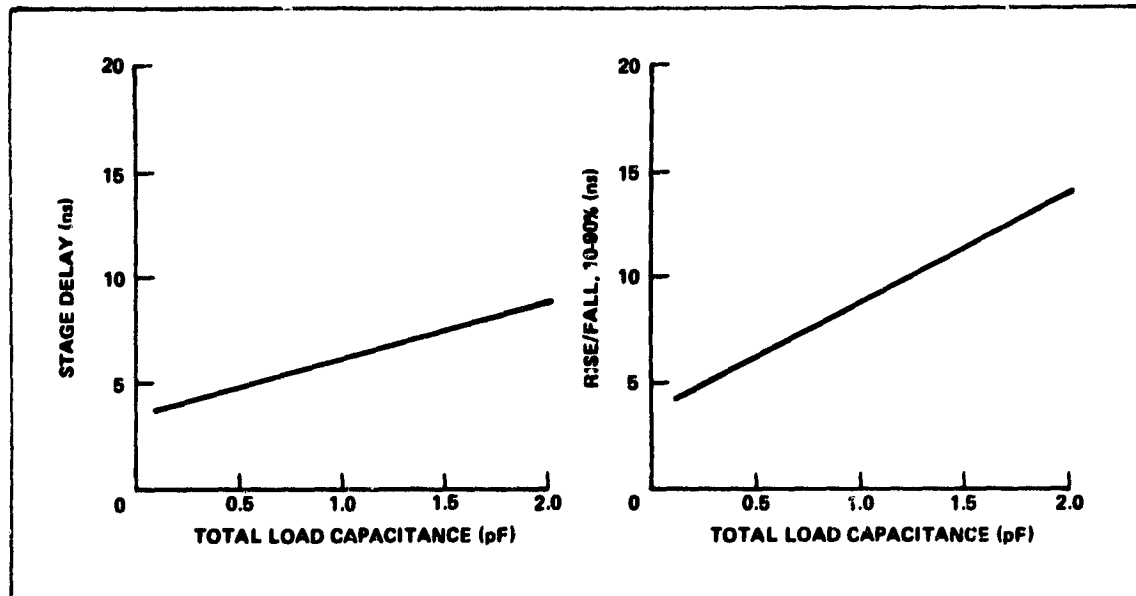
FOUR—INPUT NOR

SOS STANDARD
CELL NO. 1140

8 DEVICES

5 PADS   **CELL WIDTH= 5 MILS**

$V_{DD} = 10$ V

SCHEMATIC

(6) D — P 5 MILS
(5) C — P 5 MILS
(4) B — P 5 MILS
(3) A — P 5 MILS

X (2)

N 0.8 MILS | N 0.8 MILS | N 0.8 MILS | N 0.8 MILS

LOGIC SYMBOL

(3)
(4) A B C D
(5)
(6)

X (2)

$$X = \overline{A + B + C + D}$$
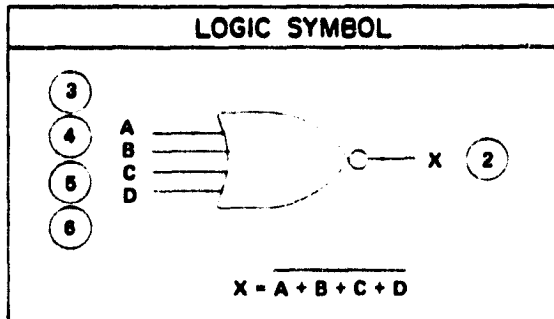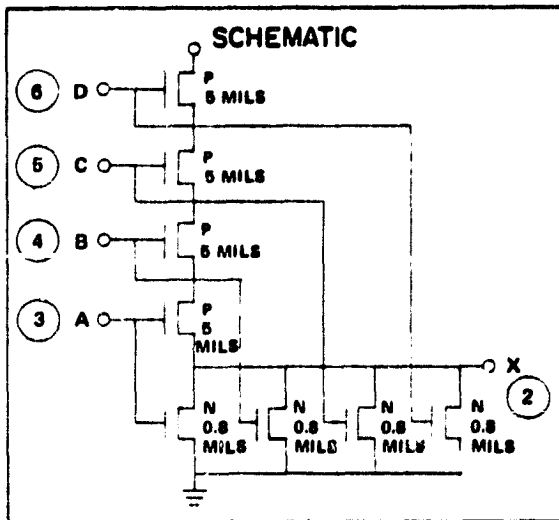
TRUTH TABLE

A	B	C	D	X
0	0	0	0	1
ALL OTHER INPUT COMBINATIONS				0

PIN	CAPACITANCE (pF)
2	0.070
3	0.450
4	0.450
5	0.450
6	0.450

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)
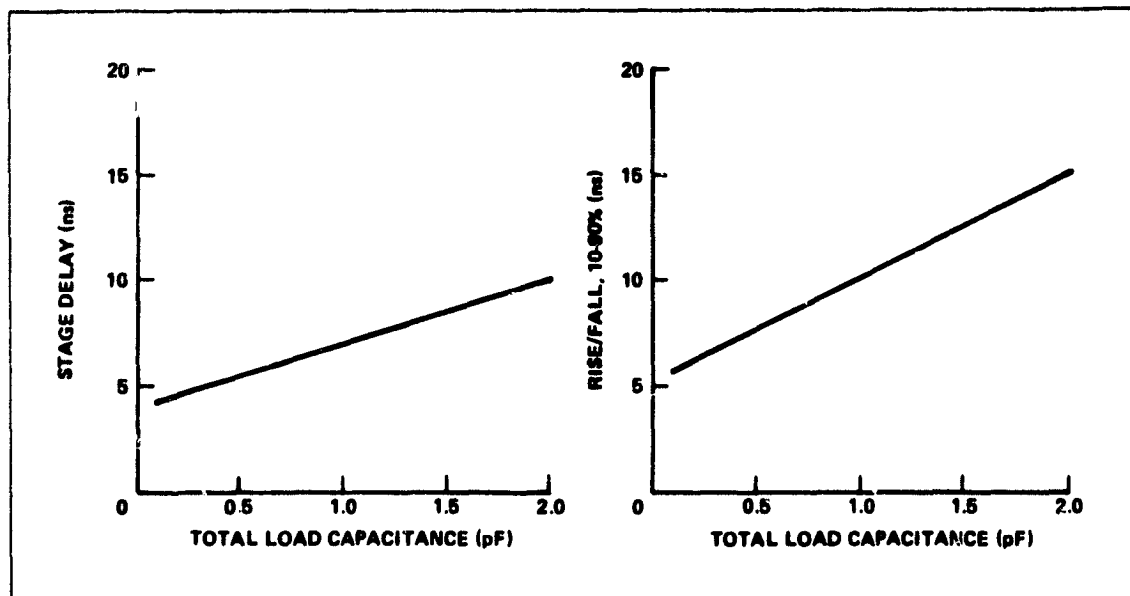
TWO—INPUT NAND

SOS STANDARD
CELL NO. 1220

4 DEVICES

3 PADS   CELL WIDTH= 3 MILS

V_{DD} = 10 V

SCHEMATIC

+V

P 1.3 MILS
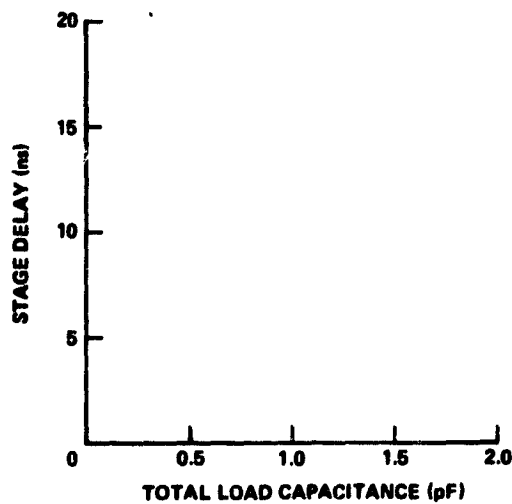P 1.3 MILS

X ④

③ B

N 1.4 MILS

② A

N 1.4 MILS

LOGIC SYMBOL

② A

③ B

X ④

$X = \overline{A \cdot B}$

PIN	CAPACITANCE (pF)
2	0.201
3	0.201
4	0.043
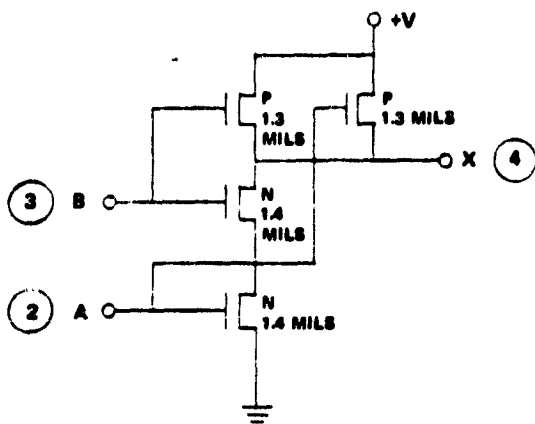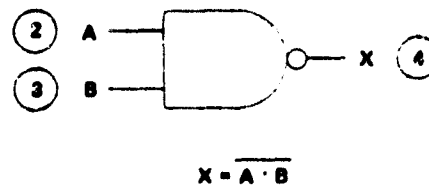
TRUTH TABLE

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

STAGE DELAY (ns)

0   0.5   1.0   1.5   2.0

TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns)

0   0.5   1.0   1.5   2.0

TOTAL LOAD CAPACITANCE (pF)

19
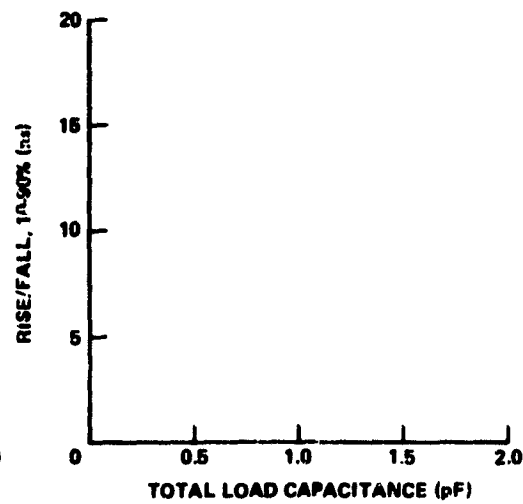
THREE-INPUT NAND

SOS STANDARD
CELL NO. 1230

6 DEVICES

4 PADS   CELL WIDTH= 4 MILS

V_{DD} = 10 V

SCHEMATIC

LOGIC SYMBOL

$$X = \overline{A \cdot B \cdot C}$$
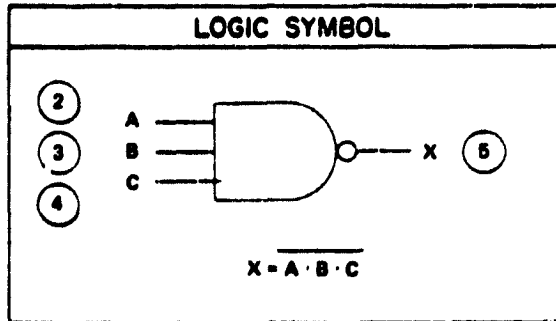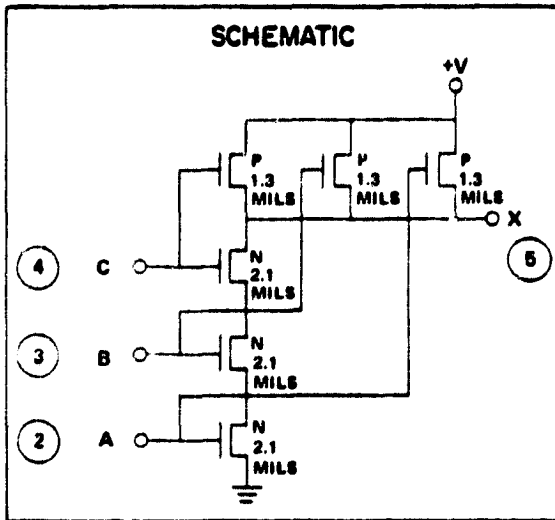
PIN	CAPACITANCE (pF)
2	0.266
3	0.266
4	0.266
5	0.076

TRUTH TABLE

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0
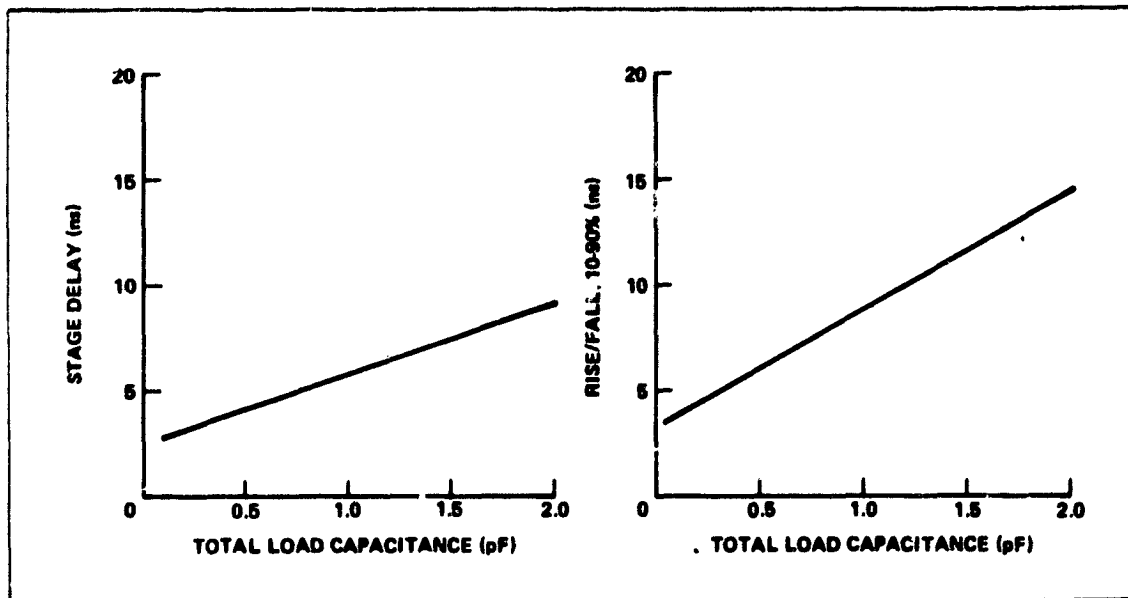
FOUR—INPUT NAND

SOS STANDARD
CELL NO. 1240

8 DEVICES

5 PADS   CELL WIDTH= 5 MILS

$V_{DD} = 10$ V

SCHEMATIC

LOGIC SYMBOL

$X = \overline{A \cdot B \cdot C \cdot D}$
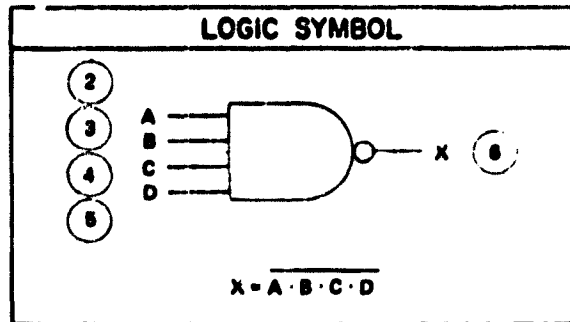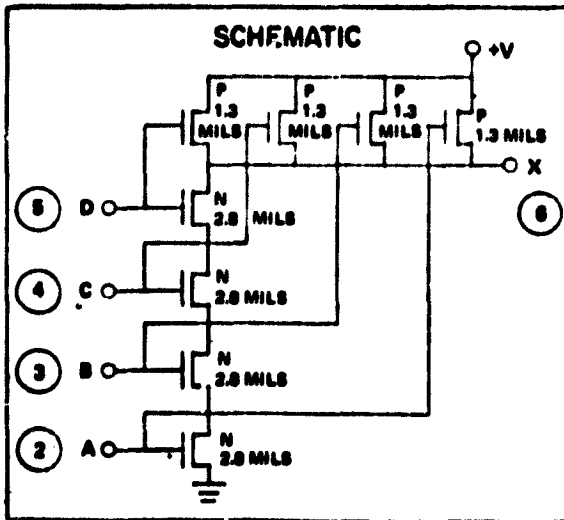
TRUTH TABLE

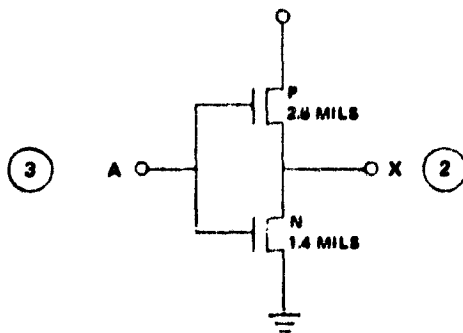| A	B	C	D	X
1	1	1	1	0
ALL OTHER INPUT COMBINATIONS				1

PIN	CAPACITANCE (pF)
2	0.319
3	0.319
4	0.319
5	0.319
6	0.142
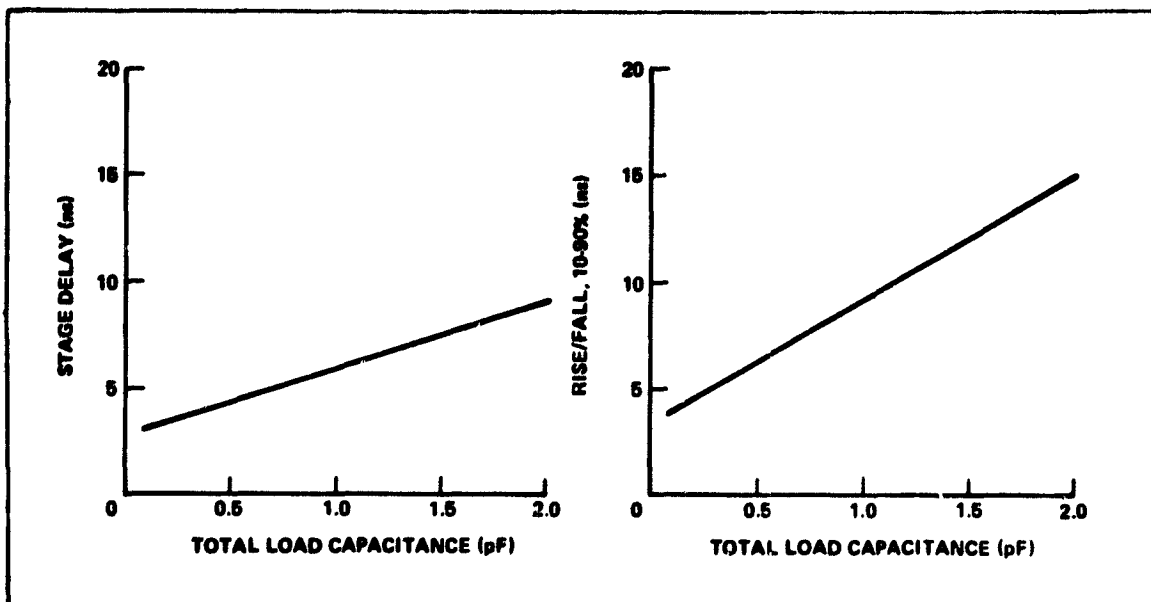
BUFFER INVERTER

SOS STANDARD
CELL NO. 1310

2 DEVICES

2 PADS   CELL WIDTH = 2 MILS V_{DD} = 10 V

SCHEMATIC

P
2.8 MILS

③ A

X ②

N
1.4 MILS

LOGIC SYMBOL

③   A ----▷○---- X   ②

$X = \overline{A}$
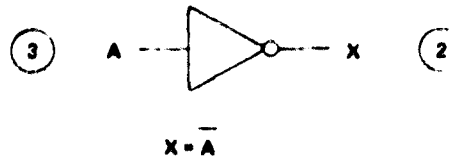
TRUTH TABLE

A	X
0	1
1	0

PIN	CAPACITANCE (pF)
2	0.010
3	0.311

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)
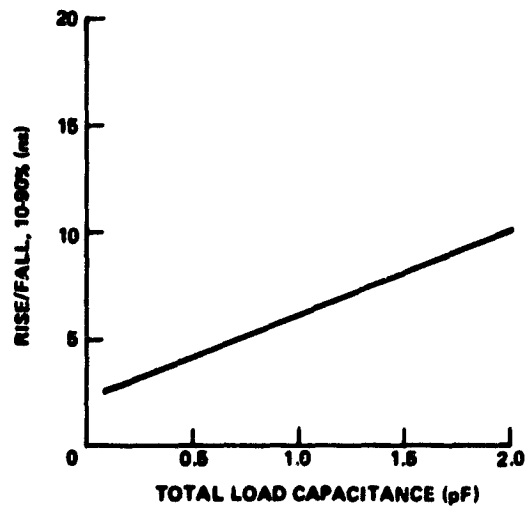
INVERTING 2X1 MULTIPLEXER	SOS STANDARD CELL NO. 1340
10 DEVICES	
4 PADS CELL WIDTH = 5.0 MILS	V_{DD} = 10 V

SCHEMATIC

+V

4,B
2,A

P 2.8   P 2.9
P 2.7   P 2.5
N 1.7   N 1.6
P 1.2
5,C
N 1.6   N 1.8
N 0.8

3,Z

LOGIC SYMBOL

4, B
2, A
5, C
3, Z

$$C\bar{A} + \bar{C}\bar{B} = Z$$

TRUTH TABLE

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0
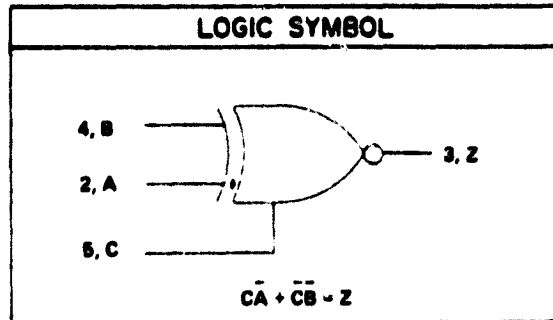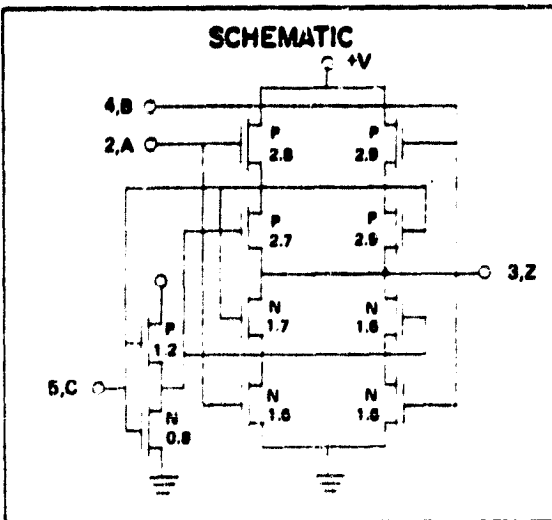
PIN	CAPACITANCE (pF)
2	0.38
3	0.01
4	0.41
5	0.69

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

A, B, OR C INPUT

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)
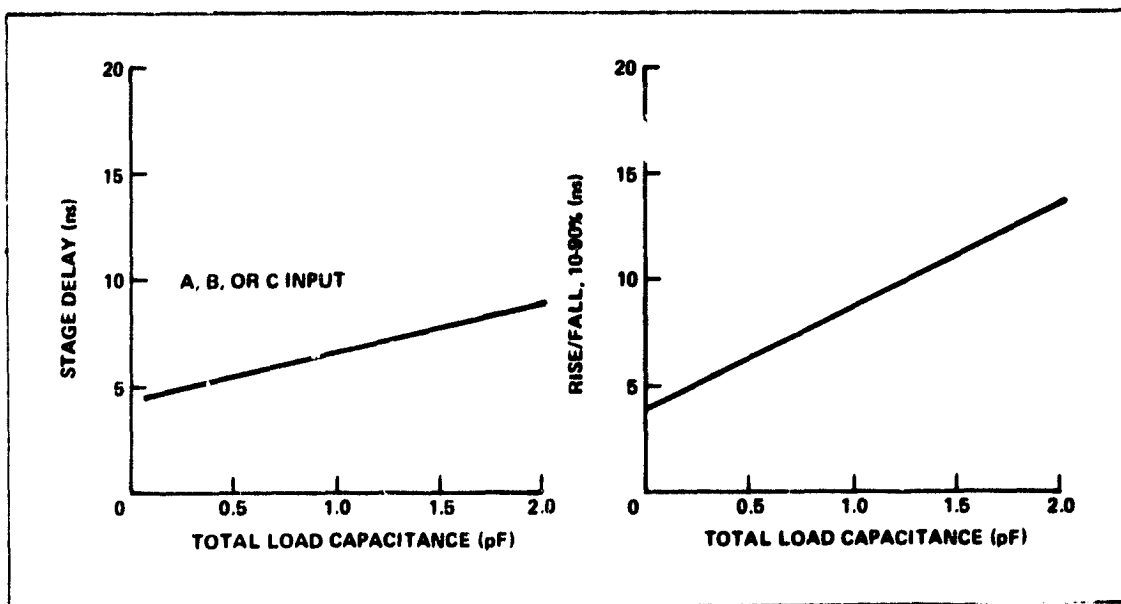
TRANSMISSION GATE

SOS STANDARD CELL NO. 1370

4 DEVICES

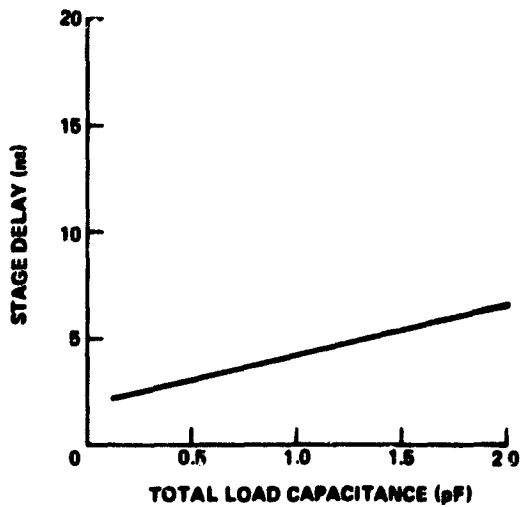3 PADS   CELL WIDTH = 4 MILS

V_{DD} = 10V

SCHEMATIC

P
1.6 MILS

N
1.0 MILS

P
6.1
N
2.7

2 D ——— C X 3

4 C

LOGIC SYMBOL

4 C

2 D ——— X   3
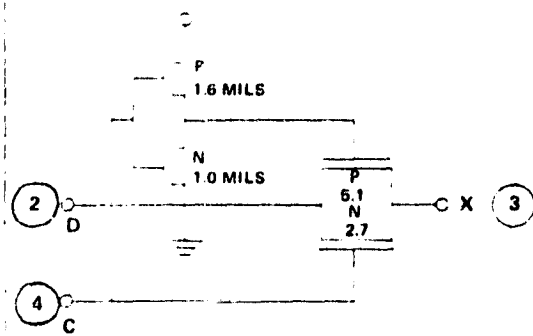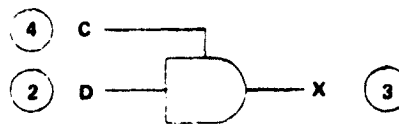
X = DC

TRUTH TABLE

D	C	X
0	0	*
0	1	0
1	0	*
1	1	1

* OUTPUT IS UNDEFINED, HI Z STATE

PIN	CAPACITANCE (pF)
2	0.255
3	0.078
4	0.335

C INPUT HI Z DRIVER

C IN LOW Z

D IN

STAGE DELAY (ns)

TOTAL LOAD CAPACITANCE (pF)

HIGH Z DRIVER

LOW Z DRIVER

RISE/FALL, 10-90% (ns)

TOTAL LOAD CAPACITANCE (pF)
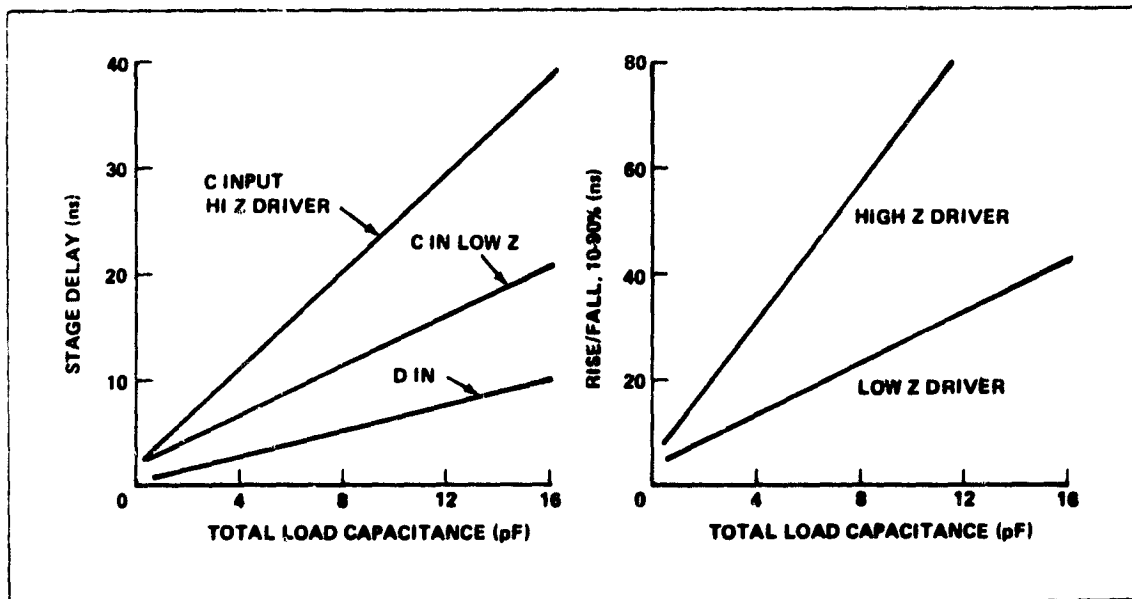
NON—INVERTING BUFFER	SOS STANDARD CELL NO. 1510

4 DEVICES

2 PADS CELL WIDTH= V_{DD} = 10 V

SCHEMATIC

LOGIC SYMBOL

X = A

PIN	CAPACITANCE (pF)
2	0.310
3	0.010
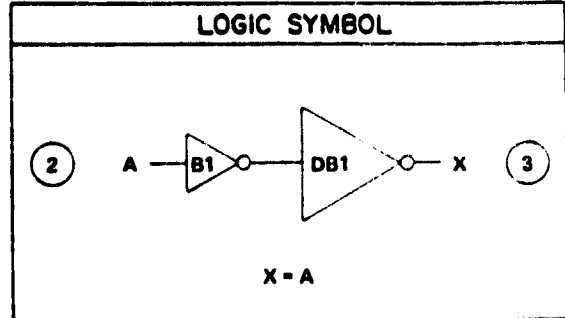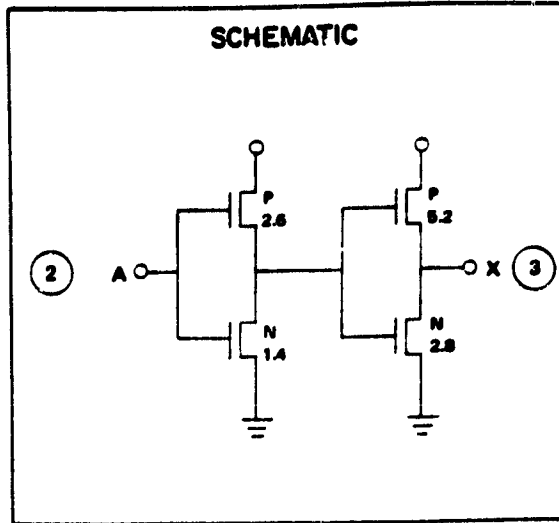
TRUTH TABLE

A	X
0	0
1	1
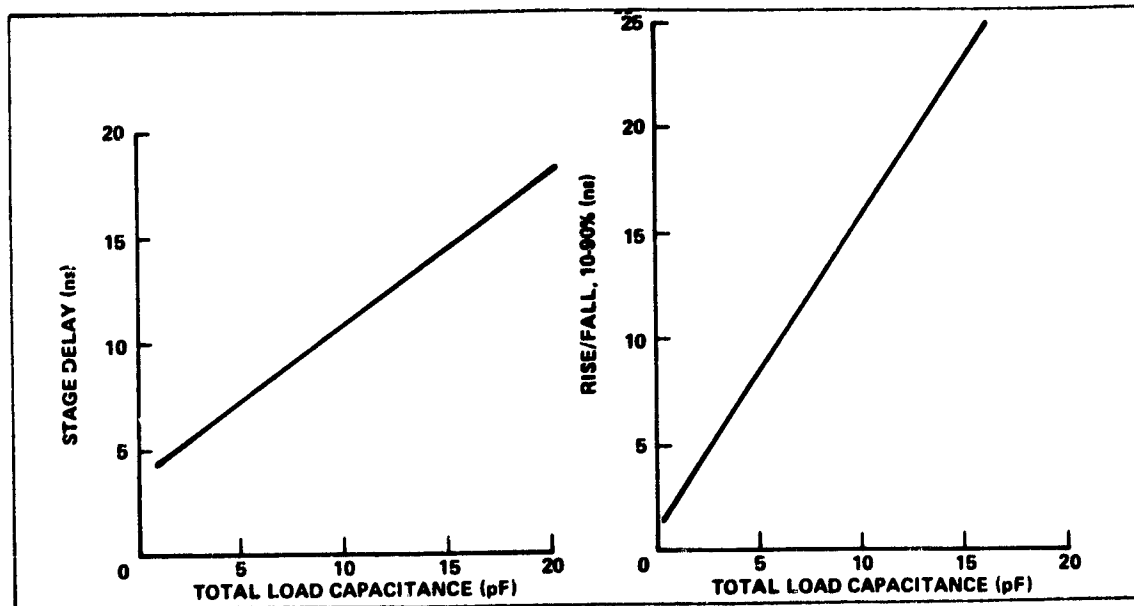
DOUBLE BUFFER INVERTER

SOS STANDARD
CELL NO. 1520

2 DEVICES

2 PADS   CELL WIDTH= 3 MILS V_{DD} = 10 V

SCHEMATIC

P
5.2 MILS

(2) A X (3)

N
2.8 MILS

LOGIC SYMBOL

(2) A X (3)

$X = \overline{A}$

PIN	CAPACITANCE (pF)
2	0.622
3	0.010

TRUTH TABLE

A	X
0	1
1	0

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)

26
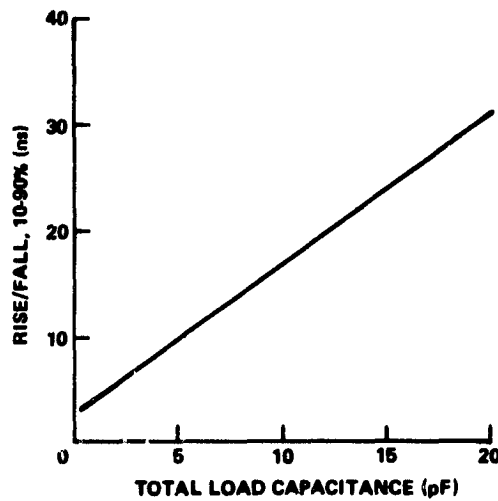
TRISTATE	SOS STANDARD CELL NO. 1570
10 DEVICES PADS 7 MIL HEIGHT	CELL WIDTH = 6.0 MILS V_{DD} = 10 V

SCHEMATIC

LOGIC SYMBOL

③ C

② D — 1570 — Q ④
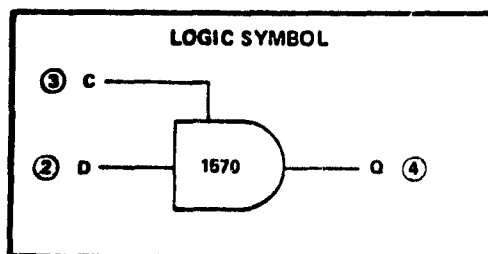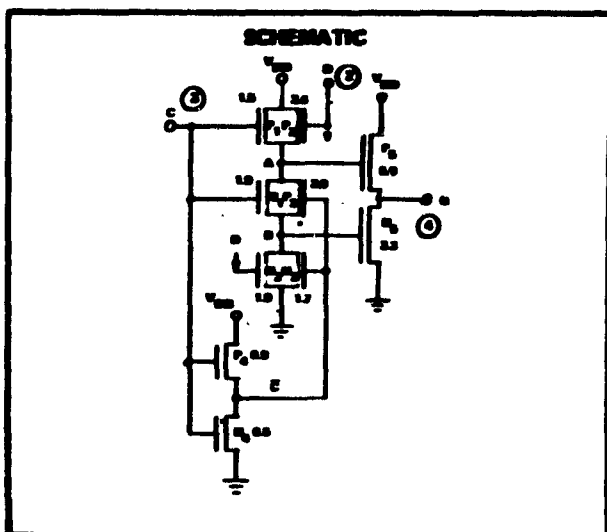
LOGIC EQUATION

$Q = D \cdot C$ for C = 1

Q = OPEN CKT. FOR C = 0

TRUTH/TABLE

C	D	Q
1	0	0
1	1	1
0	*	OPEN

* DON'T CARE

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.294
3	0.305
4	—

NOTE:
ALL DATA TAKEN
WITH ZERO IMPED-
ANCE SOURCE AT
'D'.
'C' HELD HIGH.

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)

27
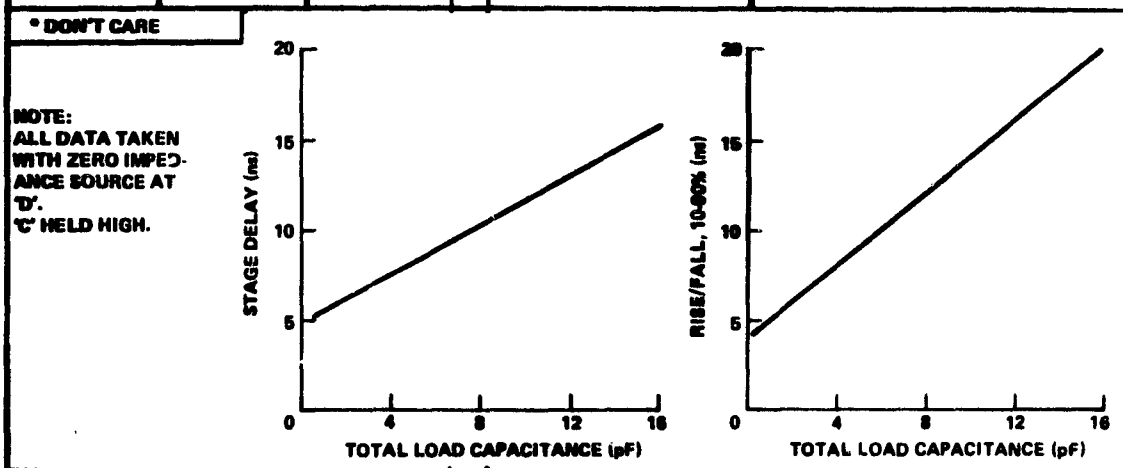
TWO—INPUT AND

SOS STANDARD
CELL NO. 1620

6 DEVICES

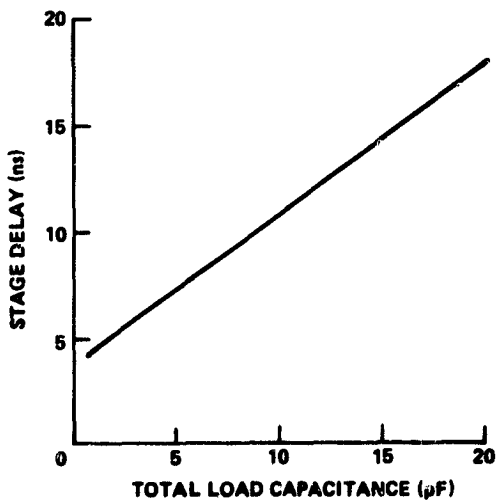3 PADS   CELL WIDTH = 4 MILS V_{DD} = 10 V

SCHEMATIC

+V

+V

P 1.5 MILS   P 1.5 MILS   P 3.0 MILS

X

4 B

N 1.6 MILS   N 2.0 MILS   2

3 A

N 1.6 MILS

LOGIC SYMBOL

3 A

4 B

X

2

X = AB
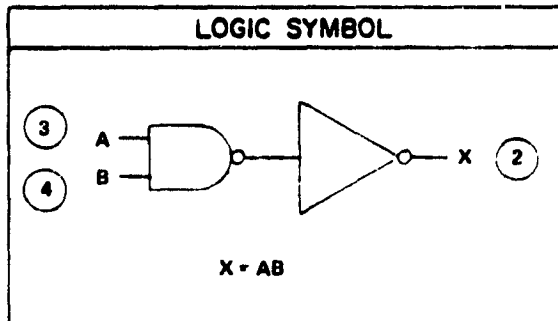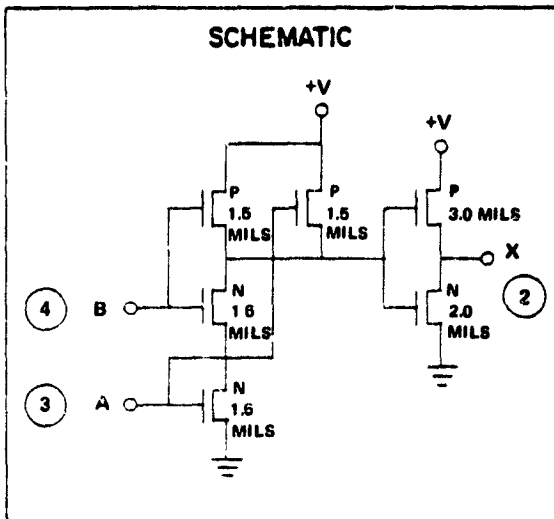
TRUTH TABLE

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

PIN	CAPACITANCE (pF)
2	0.010
3	0.243
4	0.243

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)

28

THREE–INPUT AND

SOS STANDARD
CELL NO. 1630

3 DEVICES

4 PADS   CELL WIDTH = 5 MILS

V_{DD} = 10V

SCHEMATIC

LOGIC SYMBOL

X = ABC

PIN / CAPACITANCE

PIN	CAPACITANCE (pF)
2	0.010
3	0.304
4	0.304
5	0.304

TRUTH TABLE

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1
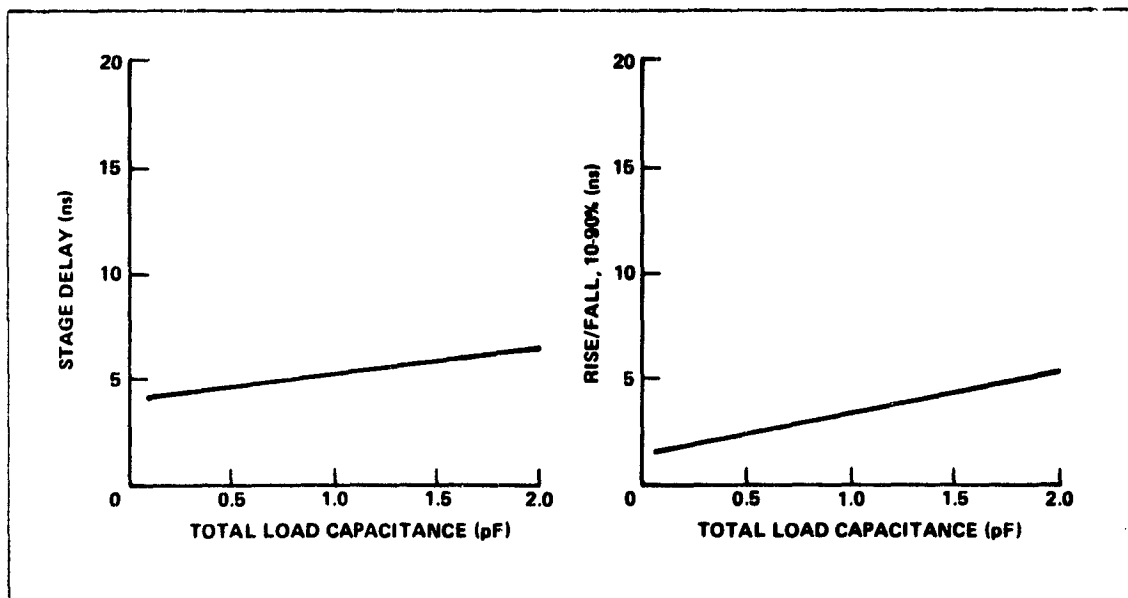
FOUR–INPUT AND

SOS STANDARD
CELL NO. 1640

10 DEVICES

5 PADS **CELL WIDTH= 6 MILS** $V_{DD} = 10\ V$

SCHEMATIC

LOGIC SYMBOL

X = ABC

PIN	CAPACITANCE (pF)
2	0.010
3	0.354
4	0.354
5	0.354
6	0.354
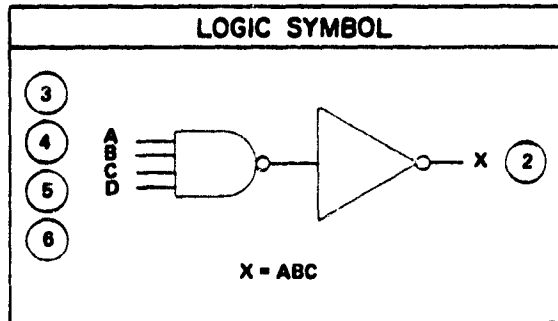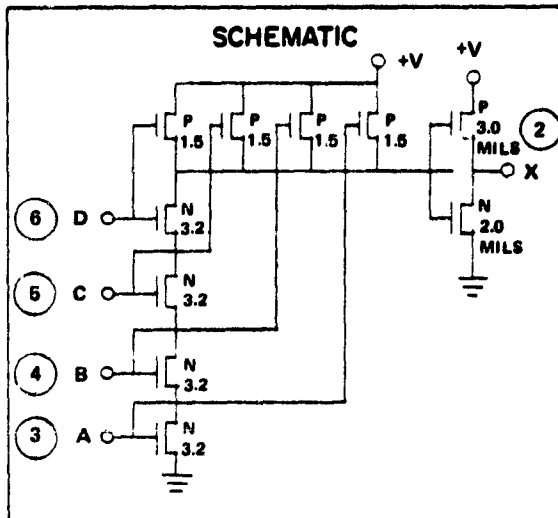
TRUTH TABLE

A	B	C	D	X
1	1	1	1	1
ALL OTHER COMBINATIONS				0
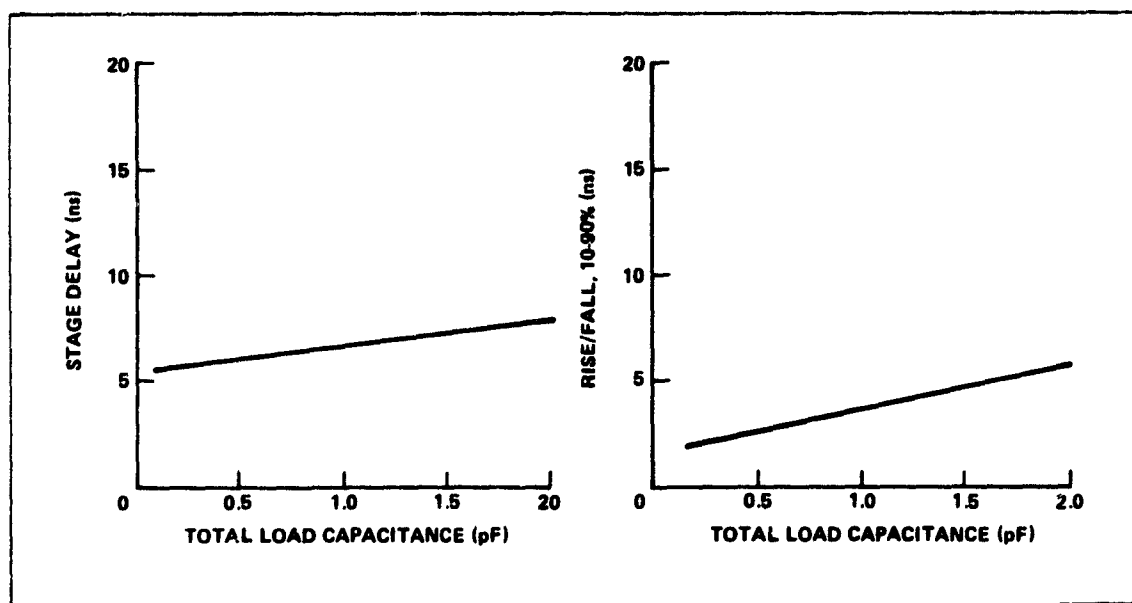
TWO–INPUT OR	SOS STANDARD CELL NO. 1720

6 DEVICES

3 PADS   CELL WIDTH = 4 MILS V_{DD} = 10 V

SCHEMATIC
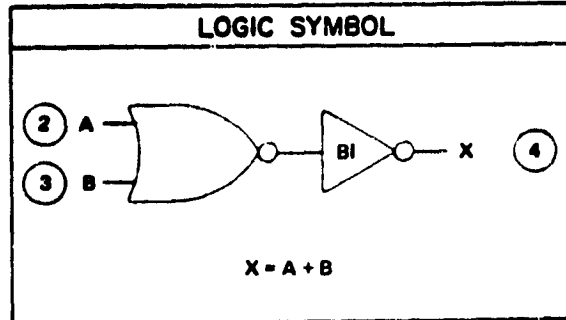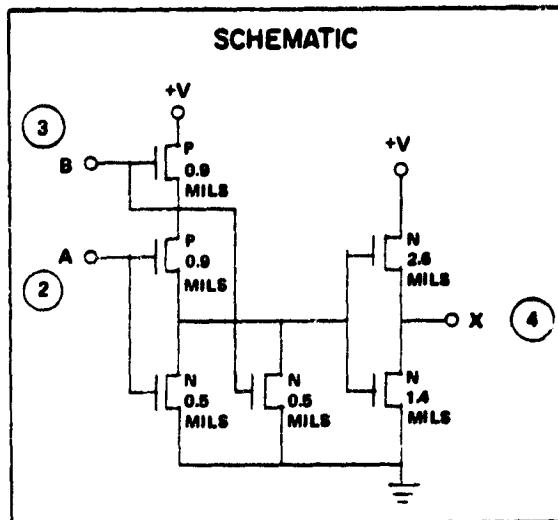
PIN	CAPACITANCE (pF)
2	0.115
3	0.115
4	0.010

LOGIC SYMBOL

$X = A + B$

TRUTH TABLE

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1
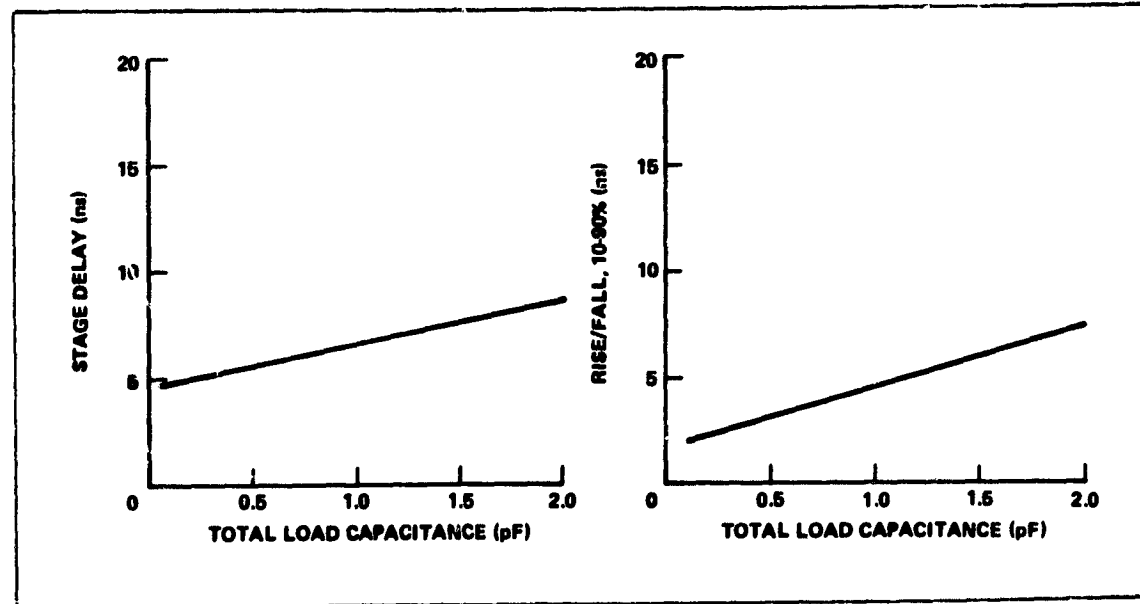
THREE—INPUT OR	SOS STANDARD CELL NO. 1730

8 DEVICES

4 PADS   CELL WIDTH = 5 MILS V_{DD} = 10 V

SCHEMATIC

+V

(4) C   P 3.5 MILS

(3) B   P 3.5 MILS   +V

(2) A   P 3.5 MILS   P 3.1 MILS

X

N 0.8 MILS   N 0.8 MILS   N 0.8 MILS   N 2.0 MILS   (5)

LOGIC SYMBOL

(2) A
(3) B
(4) C

X (5)

X = A + B + C

PIN	CAPACITANCE (pF)
2	0.225
3	0.225
4	0.225
5	0.010
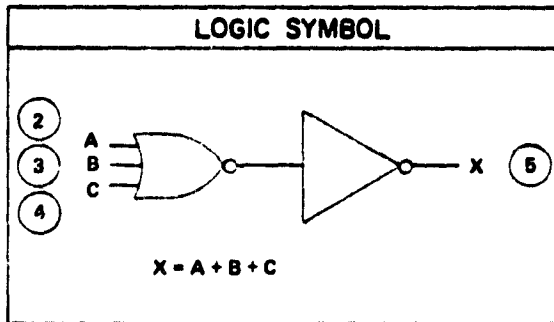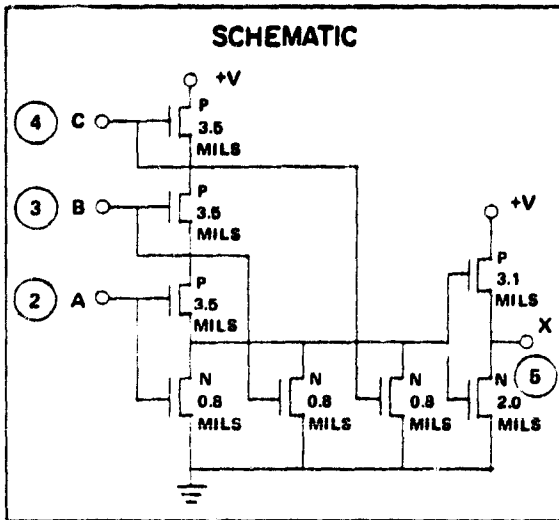
TRUTH TABLE

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)
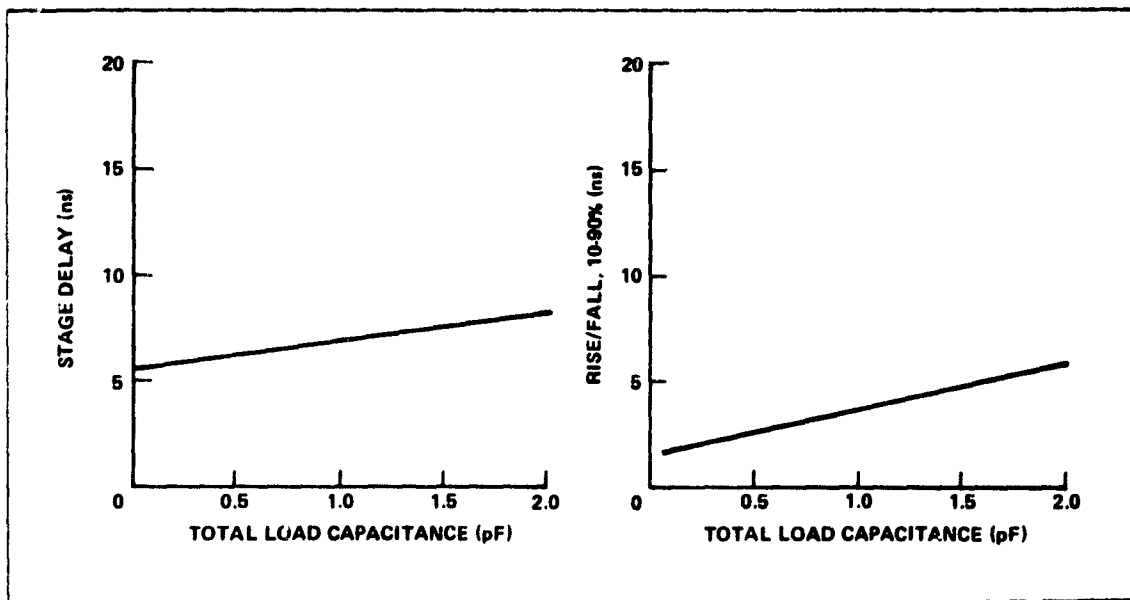
FOUR—INPUT OR

SOS STANDARD
CELL NO. 1740

10 DEVICES

5 PADS   **CELL WIDTH = 6 MILS**

$V_{DD} = 10$ V

SCHEMATIC

+V

5 D — P 4.4 MILS

4 C — P 4.4 MILS

3 B — P 4.4 MILS

2 A — P 4.4 MILS

+V

P 3.0 MILS

X

6

N 0.8 N 0.8 N 0.8 N 0.8 N 2.0 MILS

LOGIC SYMBOL

A
B
C
D

6 — X

$X = A + B + C + D$

TRUTH TABLE

A	B	C	D	X
0	0	0	0	0
ALL OTHER INPUT COMBINATIONS				1

PIN	CAPACITANCE (pF)
2	0.400
3	0.400
4	0.400
5	0.400
6	0.010
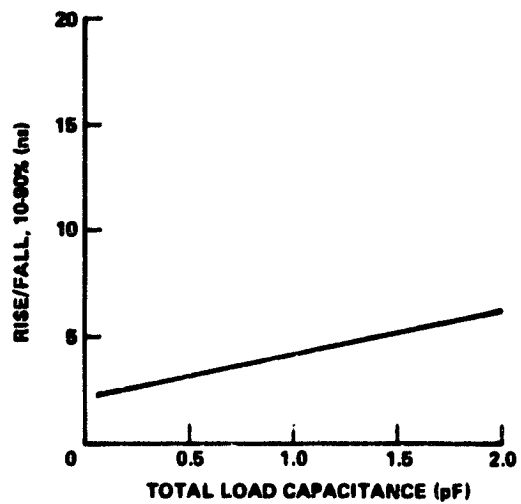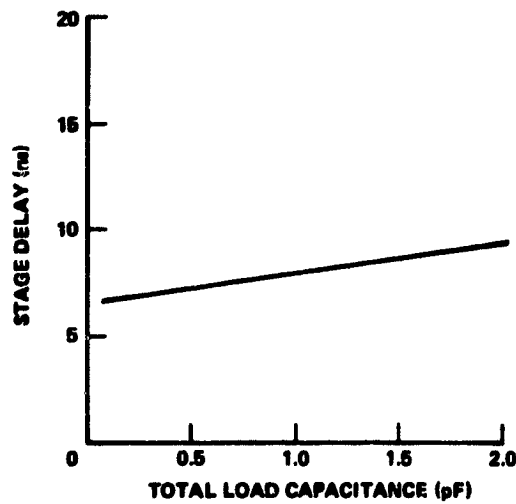
2,2 AND–2 NOR

8 DEVICES
5 PADS

CELL WIDTH = 5.0 MILS

SOS STANDARD
CELL NO. 1870

CELL HEIGHT 7

V_{DD} – 10

SCHEMATIC

LOGIC SYMBOL
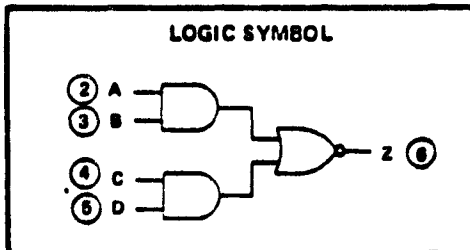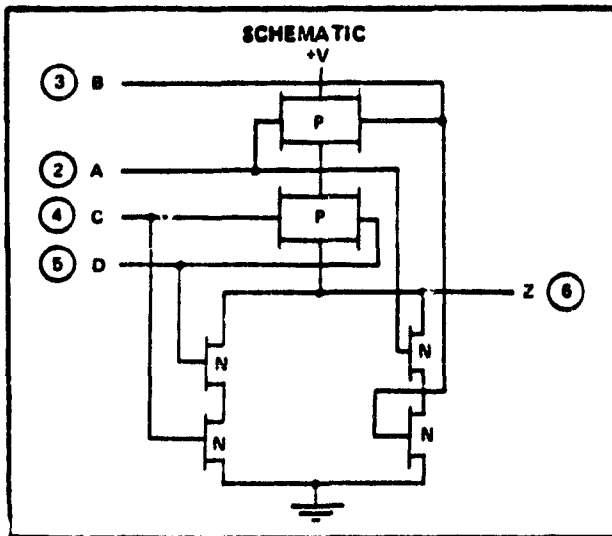
LOGIC EQUATION

$$Z = \overline{AB + CD}$$

TRUTH/TABLE

A	B	C	D	Z
1	1	*	*	0
*	*	1	1	0

ALL OTHER INPUT
COMBINATIONS — 1

* DON'T CARE

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.45
3	0.45
4	0.45
5	0.45
6	0.03

34
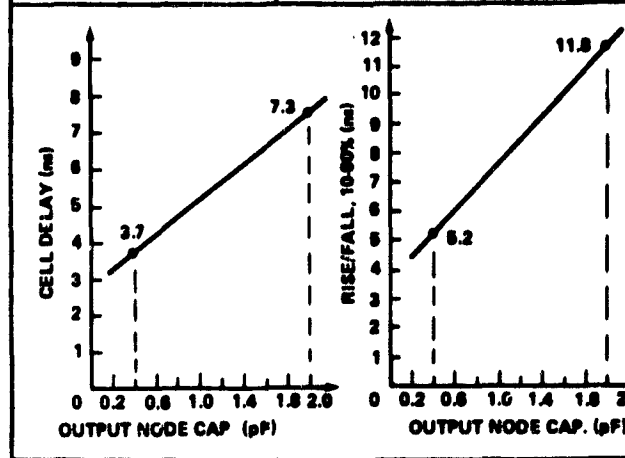
12 DEVICES
7 PADS

CELL HEIGHT 7.0 MILS

CELL WIDTH = 7.0 MILS

SOS STANDARD
CELL NO. 1890

$V_{DD}-10$

SCHEMATIC

LOGIC SYMBOL

LOGIC EQUATION
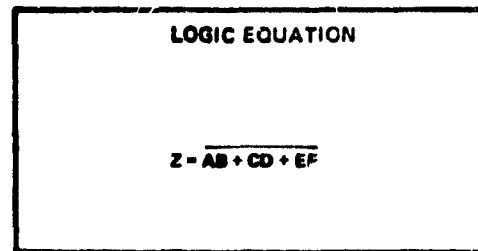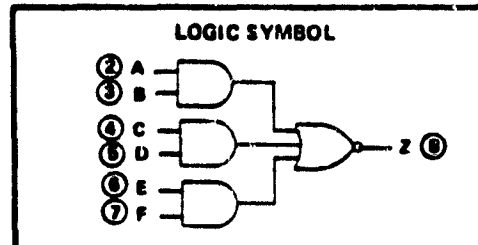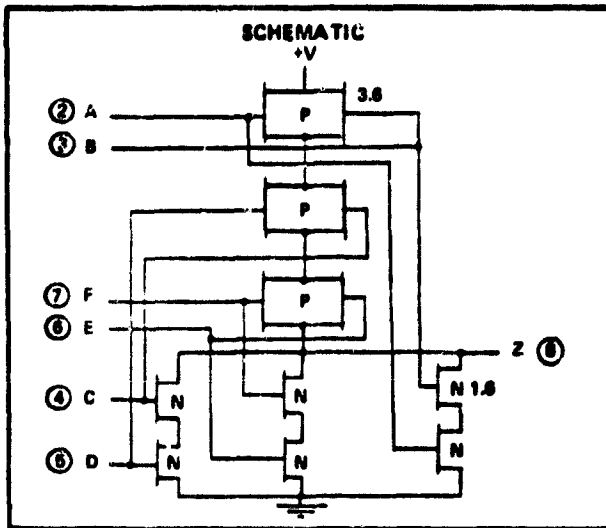
$$Z = \overline{AB + CD + EF}$$

TRUTH/TABLE

A	B	C	D	E	F	Z
1	1	•	•	•	•	0
•	•	1	1	•	•	0
•	•	•	•	1	1	0
ALL OTHER INPUT COMBINATIONS						1

• DON'T CARE

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.44
3	0.44
4	0.43
6	0.44
6	0.44
7	0.44
8	0.63

35

SOS STANDARD CELL NO. 2000

28 DEVICES
8 PADS

CELL WIDTH - 17 MILS

7 MIL FAMILY @ 10 V

SCHEMATIC

LOGIC SYMBOL
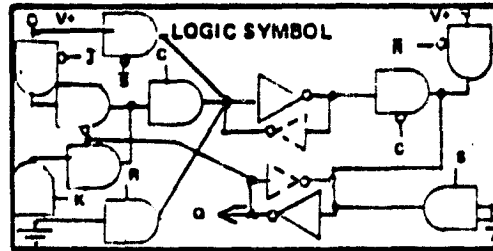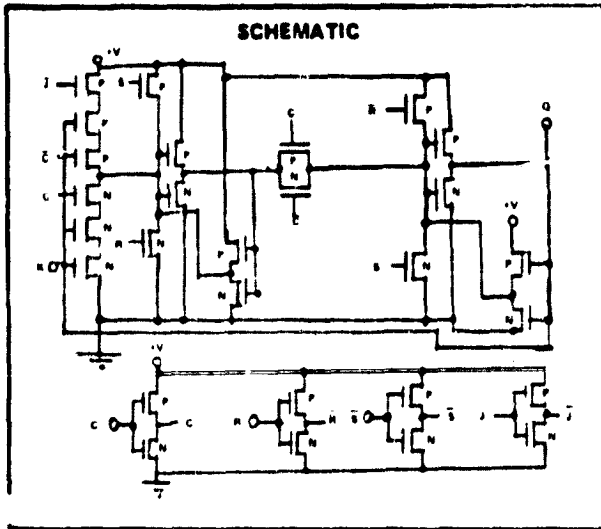
LOGIC EQUATION

$$Q_n = C \cdot \bar{R} \cdot Q_{n-1} + \bar{C} \cdot J_{n-1} \cdot \bar{K}_{n-1} \cdot \bar{R}$$
$$+ S \cdot \bar{R} + J_{n-1} \cdot K_{n-1} \cdot \overline{Q_{n-1}} \cdot \bar{R}$$

Note: J_{n-1}, K_{n-1}, and Q_{n-1} ARE THE VALUES OF J, K AND Q BEFORE THE CLOCK CHANGES STATE.

TRUTH/TABLE

C	J	K	S	R	Q
⌐⌐	0	0	0	0	Q_{n-1}
⌐⌐	1	0	0	0	1
⌐⌐	0	1	0	0	0
⌐⌐	1	1	0	0	$\overline{Q_{n-1}}$
⌐	*	*	0	0	Q_{n-1}
*	*	*	1	0	1
*	*	*	0	1	0
*	*	*	1	1	PROHIBITED

NOTES: Q_{n-1} IS THE STATE OF THE OUTPUT BEFORE THE LAST CLOCK TRANSITION

* DON:T CARE

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2,J	0.12
3,Q	0.90
4,K	0.12
5,C	0.37
6,S	0.16
7,R	0.16

10 V OPERATION

STAGE DELAY

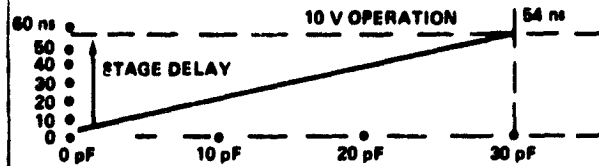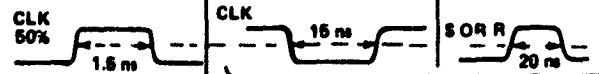| MIN CLK TO LOAD MASTER	MIN CLK TO LOAD SLAVE	MIN SET OR RESET TO LATCH
CLK 50% ... 1.5 ns	CLK ... 15 ns	S OR R ... 20 ns

EXTERNAL LOAD ON Q < 3 pF

36

D--TYPE, M/S, S/R FLIP FLOP

26 DEVICES
6 PADS

CELL WIDTH - 4 MILS

SOS STANDARD
CELL NO. 2020

7 MIL FAMILY @ 10 V

SCHEMATIC
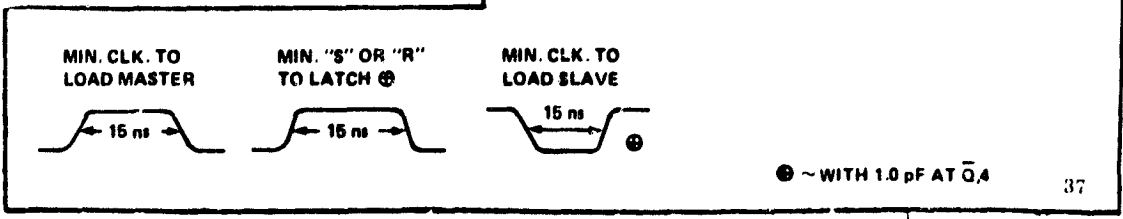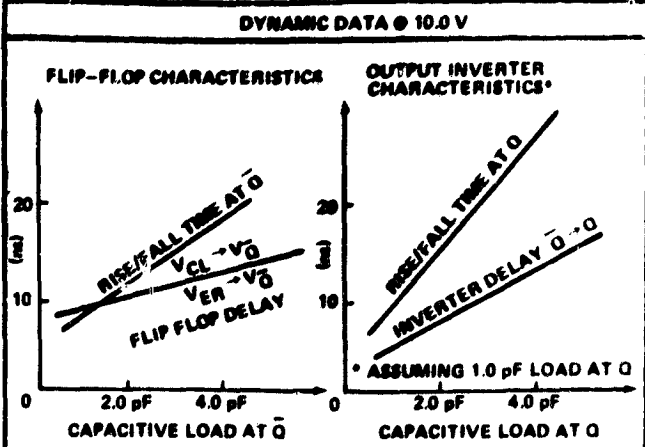

LOGIC SYMBOL
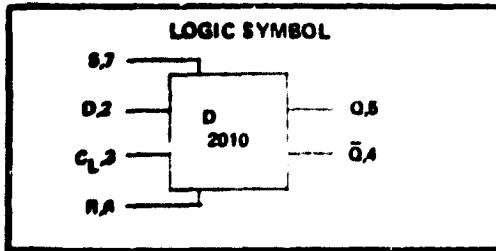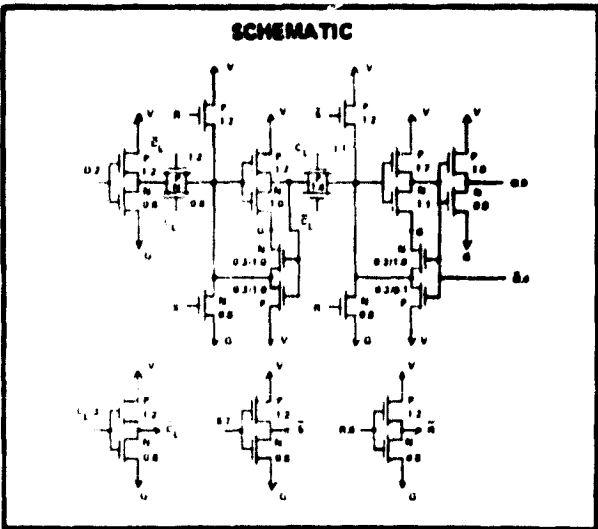
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.20
3	0.42
4	–
5	0.10
6	0.20
7	0.20

TRUTH/TABLE

C_L	D	R	S	Q	$\bar{Q}$
⌐	0	0	0	0	1
⌐	1	0	0	1	0
•	•	1	0	0	1
•	•	0	1	1	0
•	•	1	1	☆	☆

• DON'T CARE

☆ UNDEFINED OUTPUTS

DYNAMIC DATA @ 10.0 V

FLIP-FLOP CHARACTERISTICS

OUTPUT INVERTER CHARACTERISTICS*

* ASSUMING 1.0 pF LOAD AT Q

CAPACITIVE LOAD AT $\bar{Q}$

CAPACITIVE LOAD AT Q

MIN. CLK. TO LOAD MASTER

MIN. "S" OR "R" TO LATCH ⊕

MIN. CLK. TO LOAD SLAVE

15 ns

15 ns

15 ns

⊕ ~ WITH 1.0 pF AT $\bar{Q}$,4

37

SOS STANDARD
CELL NO. 2310

8 DEVICES
3 PADS   CELL WIDTH = 6 MILS V_{DD} = 10 V

SCHEMATIC

+V   +V

P   P   P   P
2.1   1.3   3.0   2.1

○ X
④

N   N   N   N
1.0   1.0   1.8   1.2

A   B

②   ③

LOGIC SYMBOL

② A

③ B

X   ④

X = A + B
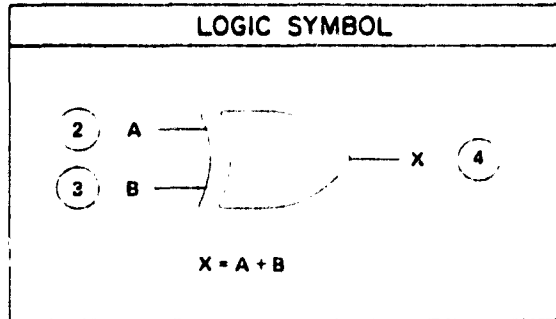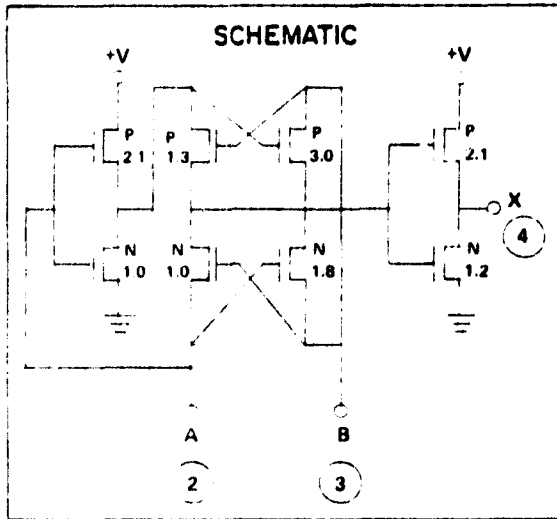
TRUTH TABLE

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

PIN	CAPACITANCE (pF)
2	0.365
3	0.362
4	

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

RISE/FALL, 10-90% (ns) vs TOTAL LOAD CAPACITANCE (pF)
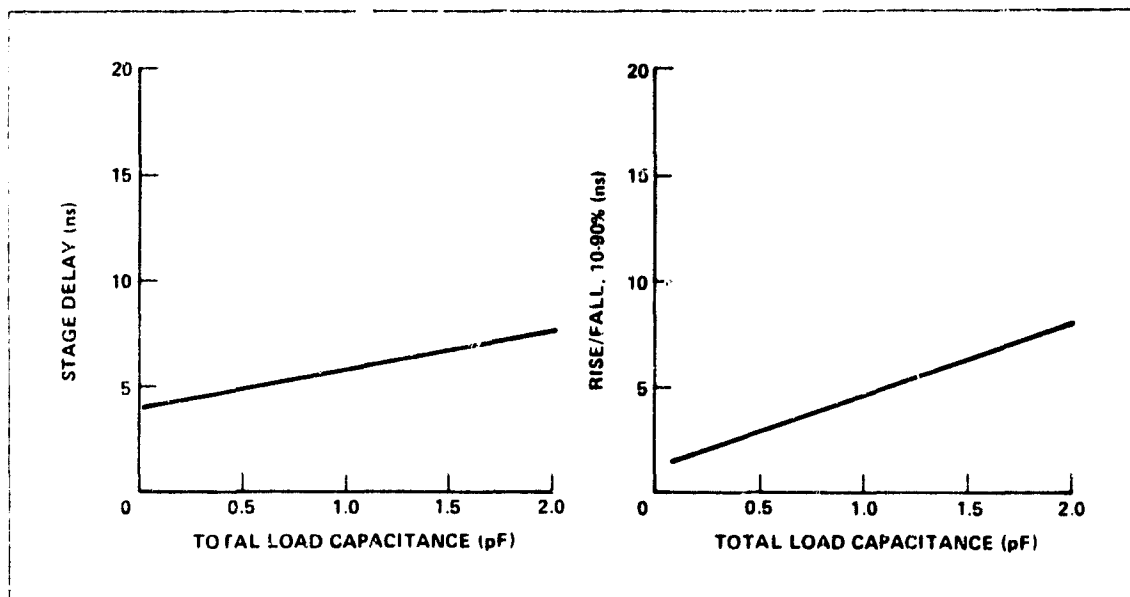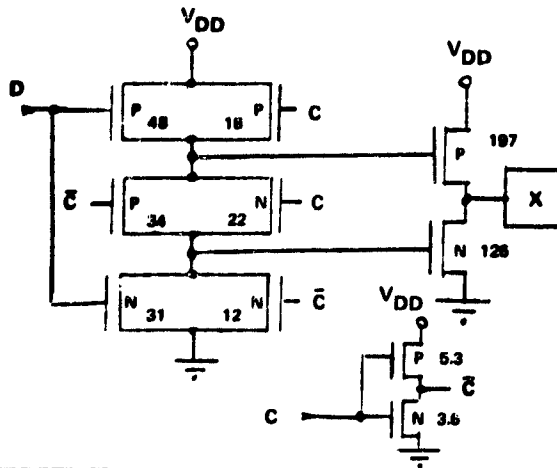
SOS STANDARD CELL NO. 2570

10 DEVICES

2 PADS

(OUTPUT PAD)
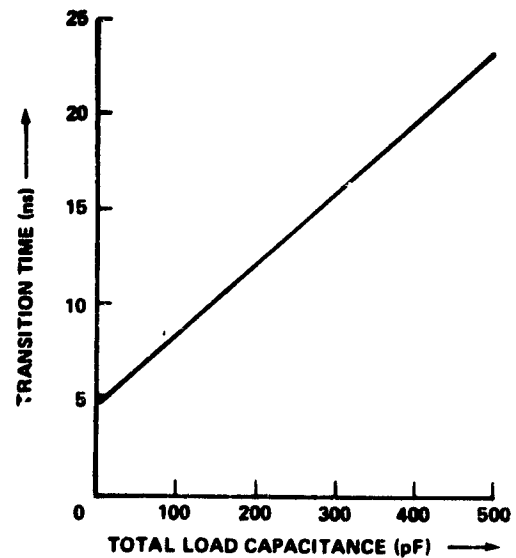
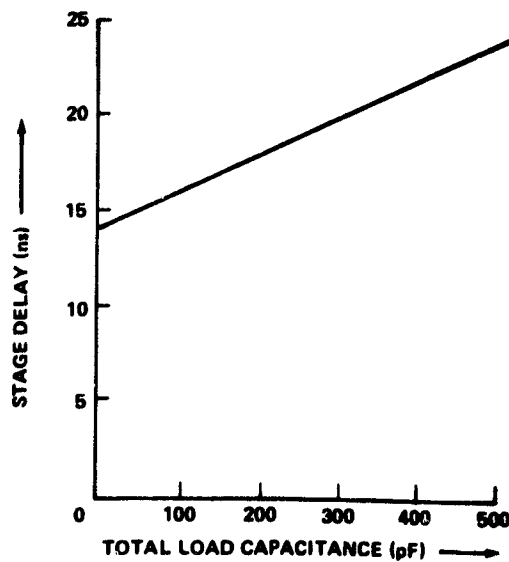CELL WIDTH = 24 MILS   CELL HEIGHT = 42 MILS

SCHEMATIC

LOGIC SYMBOL

PIN	CAPACITANCE (pF)
1	4.4
2	2.8
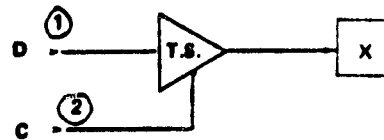
TRUTH TABLE

D	C	X
1	1	1
0	1	0
1 or 0	0	HIGH IMPED.

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

TRANSITION TIME (ns) vs TOTAL LOAD CAPACITANCE (pF)

10 DEVICES

3 PADS   CELL WIDTH = **5 MILS** V_{DD} = 10 V

SCHEMATIC

PIN	CAPACITANCE (pF)
2	0.23
3	0.15
4	0.05

LOGIC SYMBOL
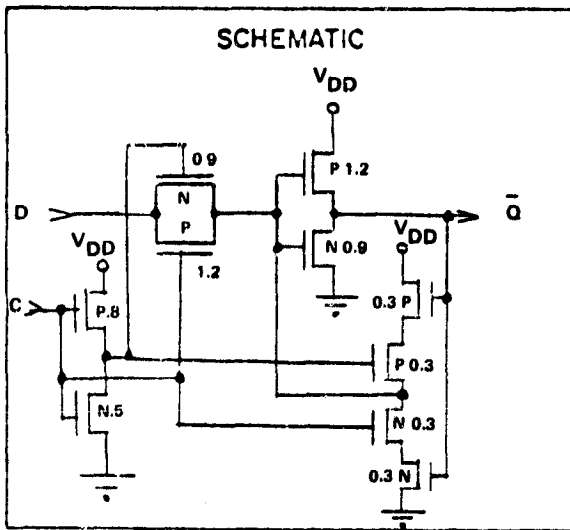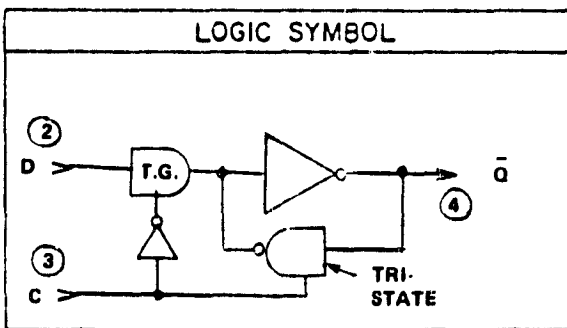
TRUTH TABLE

C	D	$\bar{Q}$
0	1	0
0	0	1
1	1	$\bar{Q}_{n-1}$

$\bar{Q}_{n-1}$ IS OUTPUT BEFORE CLOCK GOES HIGH

MIN. CLOCK PULSE
WIDTH TO TRANSMIT
INPUT, D TO OUTPUT
$\bar{Q}$.
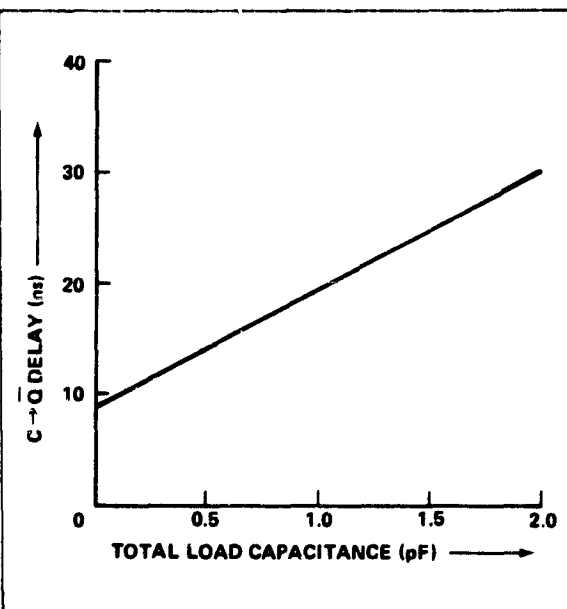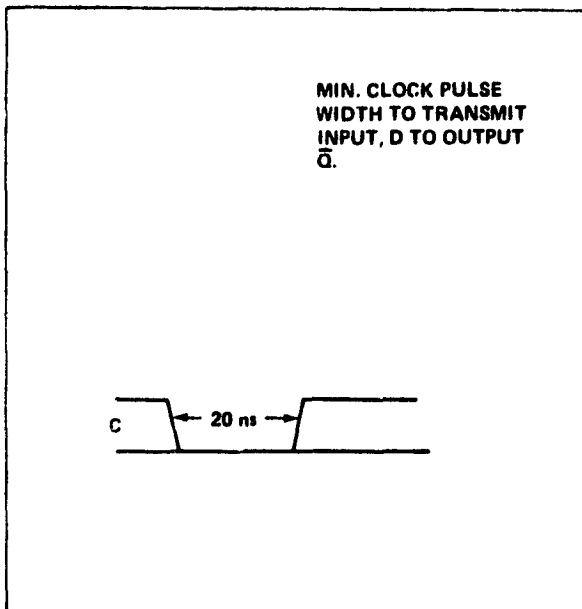
D—TYPE, MASTER/SLAVE FLIP FLOP

SOS STANDARD
CELL NO. 2820

18 DEVICES
3 PADS

CELL WIDTH = 10.0 MILS

7 MIL FAMILY
$V_{DD} = 10 V$
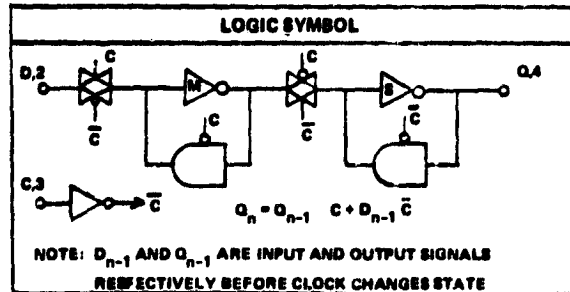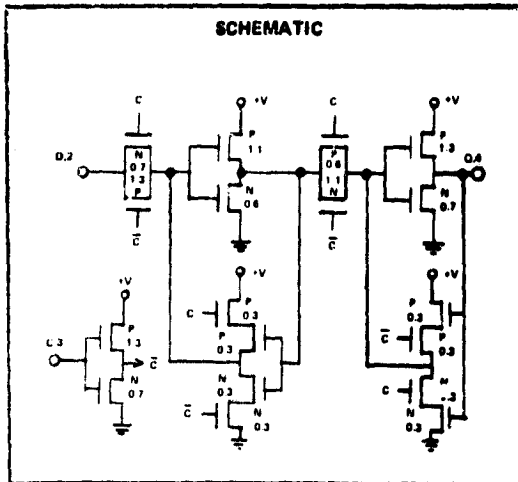
SCHEMATIC

PIN	CAPACITANCE (pF)
2	0.255
3	0.229
4	0.040

LOGIC SYMBOL

$$Q_n = Q_{n-1} \quad C + D_{n-1} \bar{C}$$

NOTE: D_{n-1} AND Q_{n-1} ARE INPUT AND OUTPUT SIGNALS RESPECTIVELY BEFORE CLOCK CHANGES STATE

TRUTH TABLE

C	D	Q_n
�	1	1
	0	0
	1	Q_{n-1}
	0	Q_{n-1}

Q_{n-1} IS OUTPUT BEFORE CLOCK GOES HIGH

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

10.0 V OPERATION

MIN. CLOCK PULSE WIDTH REQUIRED TO LOAD MASTER

22 ns

MIN. CLOCK PULSE WIDTHS REQUIRED TO TRANSFER INFORMATION FROM MASTER TO OUTPUT $C_L = 0.4$ pF; $T_C = 19$ ns

$C_L = 3.0$ pF; $T_C = 75$ ns

CONDITIONS:
ALL DELAY INFORMATION BASED ON AN ASSUMED 15 ns 10-90 RISE OR FALL TIME FOR CLOCK SIGNALS

50% CLK   50% OUTPUT Q

41
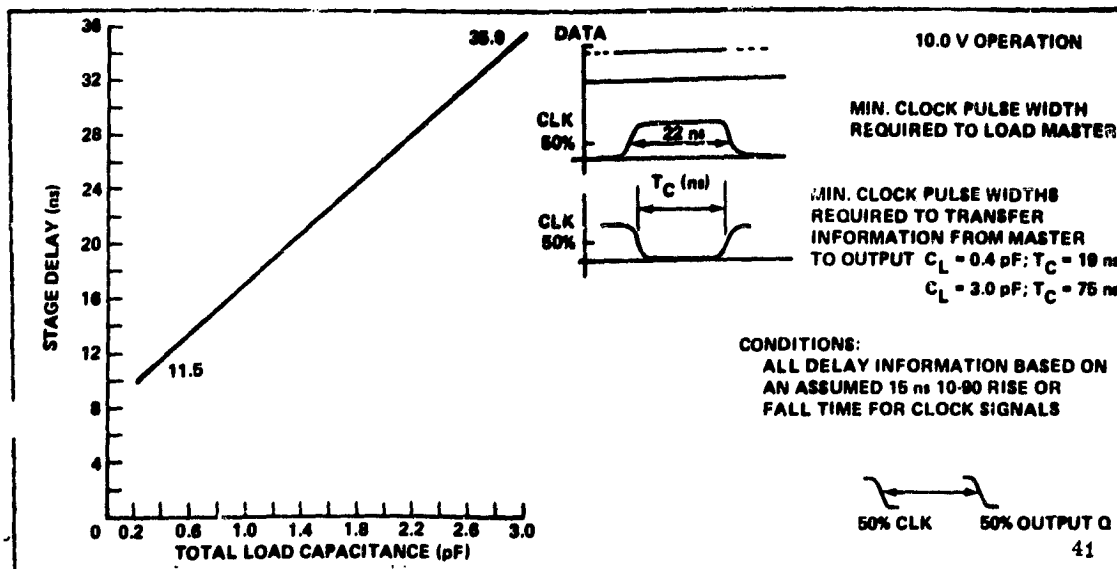
12 DEVICES
3 PADS

CELL HEIGHT = 7.0   **CELL WIDTH = 6 MILS** $V_{DD} = 10 V$

SCHEMATIC

LOGIC SYMBOL
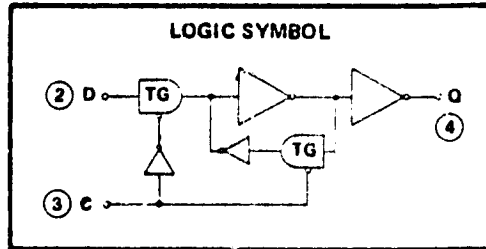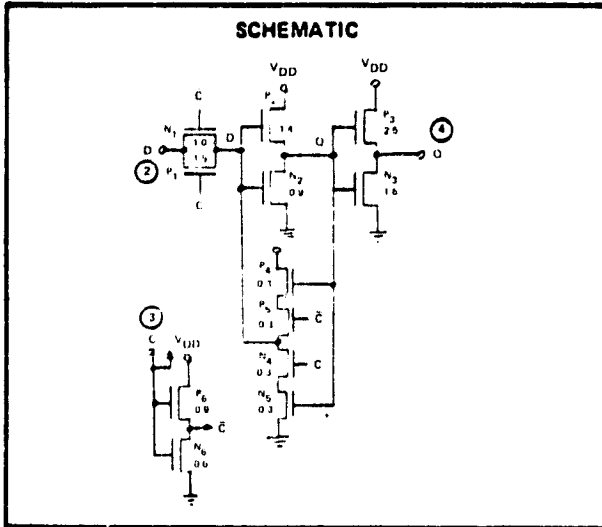
LOGIC EQUATION

TRUTH/TABLE

C	D	Q
⟋	1	1
⟋	0	0
⟍	1	Q_{n-1}
⟍	0	Q_{n-1}

Q_{n-1} IS OUTPUT BEFORE CLOCK GOES HIGH

DATA

20 ns   MIN. CLOCK PULSE WIDTH TO TRANS. INPUT 'D' TO OUTPUT 'Q'

CLOCK
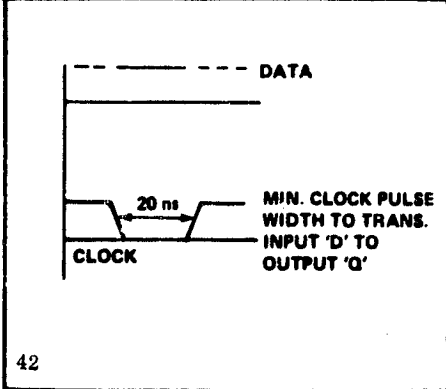
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.069
3	0.123
4	—

STAGE DELAY (ns) vs TOTAL LOAD CAPACITANCE (pF)

42
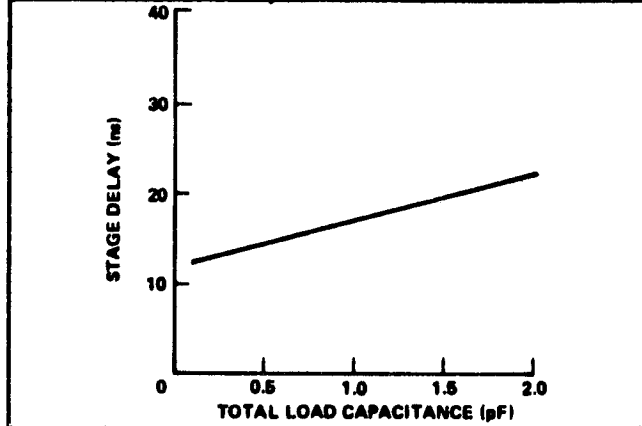
SOS STANDARD CELL NO. 2840

11 DEVICES

4 PADS

CELL WIDTH = 8 MILS

SCHEMATIC
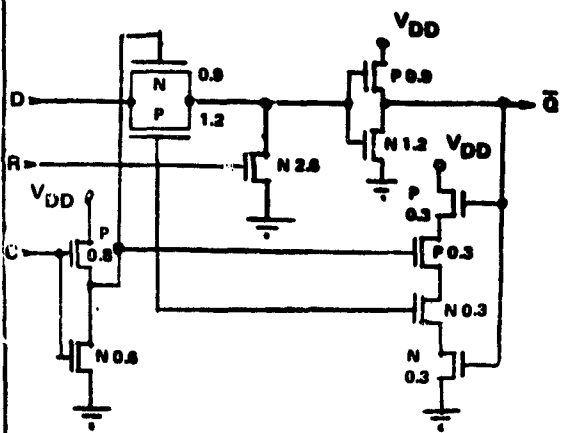
LOGIC SYMBOL
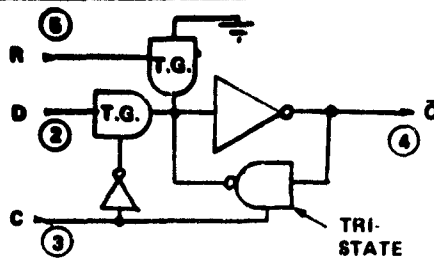
TRUTH TABLE

C	R	D	$\bar{Q}$
0	0	1	0
0	0	0	1
1	0	1	$\bar{Q}_{n-1}$
1	1	0	1
0	1	1	NOT DETERMINED

$\bar{Q}_{n-1}$ IS OUTPUT BEFORE CLOCK GOES HIGH

PIN .	CAPACITANCE (pF)
2	0.23
3	0.15
4	0.05
5	0.15

MIN. CLOCK PULSE WIDTH TO TRANSMIT INPUT 'D' TO OUTPUT 'Q'.
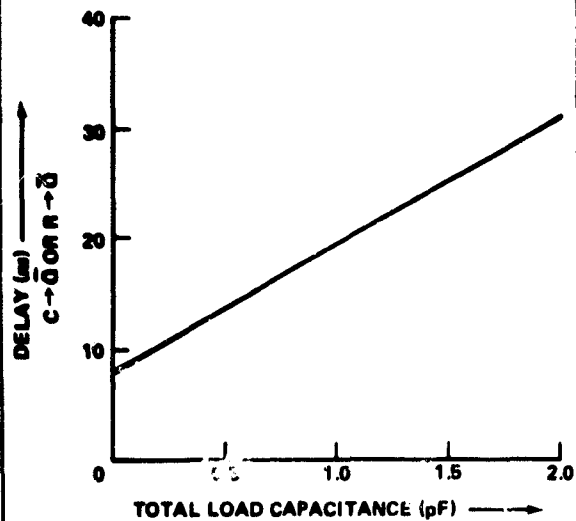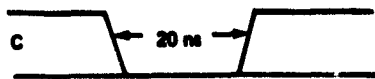
PLA INPUT DECODER

54 DEVICES
5 PADS
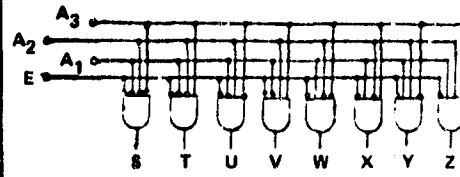**8 SIDE CONTACTS**

CELL HEIGHT: 14 MILS
CELL WIDTH: 13 MILS

SOS STANDARD
CELL NO. 7000

$V_{DD} = 10$

SCHEMATIC
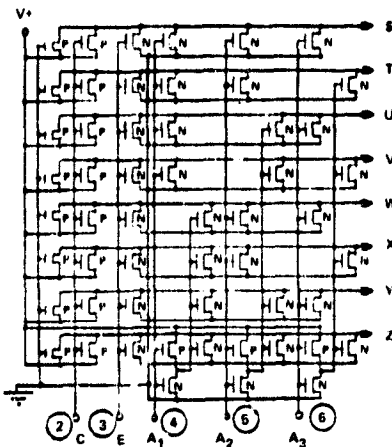
LOGIC SYMBOL

LOGIC EQUATION

$S = \bar{A}_1 \cdot \bar{A}_2 \cdot \bar{A}_3 \cdot \bar{E}$ $W = A_1 \cdot A_2 \cdot \bar{A}_3 \cdot \bar{E}$

$T = \bar{A}_1 \cdot \bar{A}_2 \cdot A_3 \cdot \bar{E}$ $X = A_1 \cdot \bar{A}_2 \cdot A_3 \cdot \bar{E}$

$U = \bar{A}_1 \cdot A_2 \cdot \bar{A}_3 \cdot \bar{E}$ $Y = A_1 \cdot A_2 \cdot \bar{A}_3 \cdot \bar{E}$

$V = \bar{A}_1 \cdot A_2 \cdot A_3 \cdot \bar{E}$ $Z = A_1 \cdot A_2 \cdot A_3 \cdot \bar{E}$

NOTE: C NORMALLY HIGH. A 25 ns NEGATIVE PULSE ON C FOLLOWING THE SETTLING OF OTHER INPUTS SPEEDS OUTPUT.

TRUTH/TABLE

| E	A_1	A_2	A_3	S	T	U	V	W	X	Y	Z
0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	0	1	0
0	1	1	1	0	0	0	0	0	0	0	1
1	*	*	*	0	0	0	0	0	0	0	0

NOTES:
1. * MEANS "DON'T CARE"
2. WHEN C IS LOW, ALL OUTPUTS ARE UNDEFINED. C IS ASSUMED HIGH FOR THE ENTIRE TRUTH TABLE.
3. THE CIRCUITRY IN THIS CELL IS NOT TRUE CMOS. ABOUT 1 mA STANDBY CURRENT IS DRAWN

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2,C	0.7
3,E	0.45
4,A_1	0.3
5,A_2	0.3
6,A_3	0.3
S, T, U, V, W. X, Y, Z	0.6 EACH

10 VOLT OPERATION
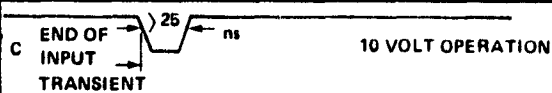
DELAY OF S, T, U, V, W, X, Y, Z (FROM TRAILING EDGE OF C) VERSUS CAPACITIVE LOADS ON S → Z
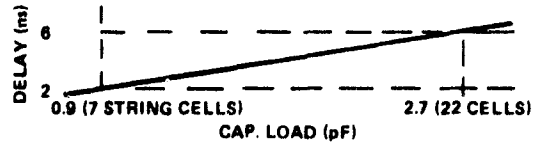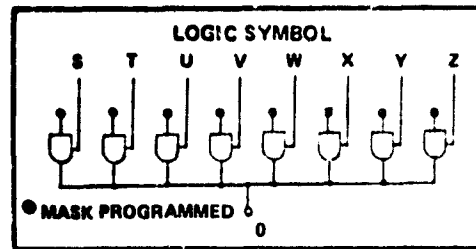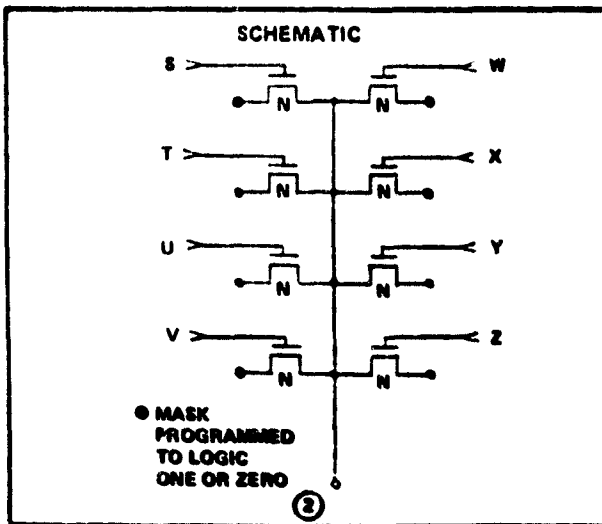
PLA OUTPUT FUNCTION STRING

8 DEVICES
1 PAD
8 THROUGH SIDE CONTACTS

CELL HEIGHT: 14 MILS
CELL WIDTH: 3 MILS

**SOS STANDARD
CELL NO. 7XX0**

$V_{DD} = 10$

SCHEMATIC

● MASK
PROGRAMMED
TO LOGIC
ONE OR ZERO

②

LOGIC SYMBOL

● MASK PROGRAMMED 0

LOGIC EQUATION

$O = S + T + U + V + W + X + Y + Z$

NOTE: ANY OF THESE TERMS FOR WHICH
THE MASK IS PROGRAMMED TO A LOGIC
ZERO DROPS OUT OF THE EQUATION.

TRUTH TABLE

S	T	U	V	W	X	Y	Z	O
1	0	0	0	0	0	0	0	X_1
0	1	0	0	0	0	0	0	X_2
0	0	1	0	0	0	0	0	X_3
0	0	0	1	0	0	0	0	X_4
0	0	0	0	1	0	0	0	X_5
0	0	0	0	0	1	0	0	X_6
0	0	0	0	0	0	1	0	X_7
0	0	0	0	0	0	0	1	X_8
0	0	0	0	0	0	0	0	FLOATING

NOTES:
1. $X_1 \rightarrow X_8$ VALUES ARE DETERMINED BY
   PROGRAMMING AT THE CONTACT MASK
   LEVEL.
2. COMBINATIONS NOT SHOWN IN TABLE
   ARE NOT ALLOWED BY THE INPUT
   DECODER CELL WHICH DRIVES S, T, U, V,
   W, X, Y, AND Z.
3. EXPANDABILITY ACHIEVED BY
   PHANTOM OR "ING" OUTPUTS.

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)	
S, T, U, V, W, X, Y, Z	0.12	EACH
O	0.24	

10 V OPERATION

DELAY FROM S, T, U, V, W, X, Y OR Z TO 0
VERSUS CAPACITIVE LOAD ON 0
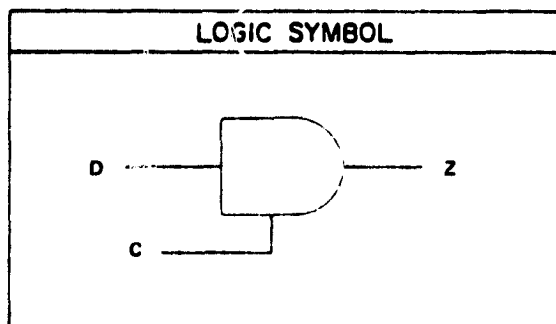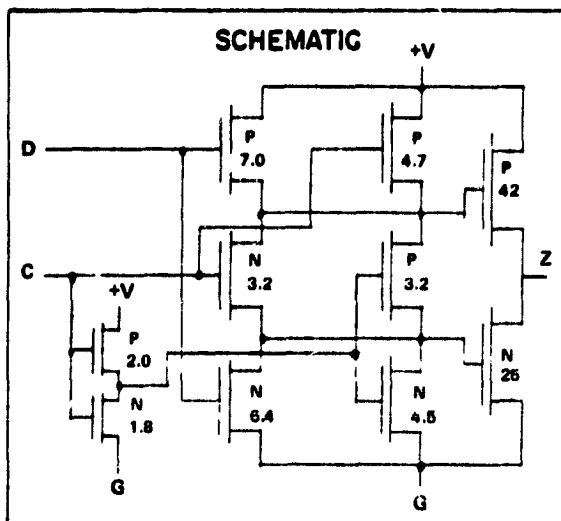

45
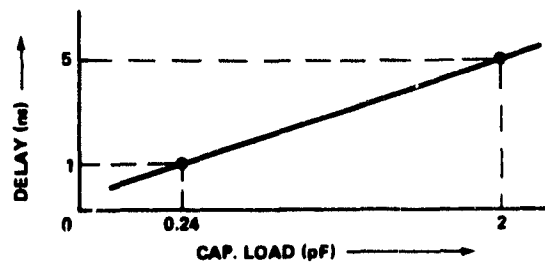
SOS STANDARD
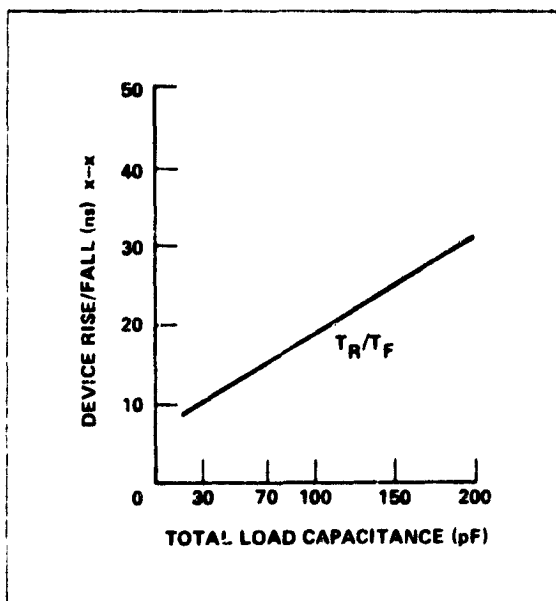## CELL NO. 9020 & 9050

10 DEVICES

3 PADS **CELL WIDTH = 18** **CELL HEIGHT = 7 MILS** $V_{DD} = 10$

SCHEMATIC

+V

D

P 7.0

P 4.7

P 42

C

N 3.2

P 3.2

Z

+V

P 2.0

N 25

N 1.8

N 6.4

N 4.5

G

G

LOGIC SYMBOL

D

C

Z

PIN	CAPACITANCE (pF)
2	1.2
3	1.0

TRUTH TABLE

C	D	Z
1	0	0
1	1	1
0	*	HIGH IMP.

STAGE DELAY (ns)

T_D

TOTAL LOAD CAPACITANCE (pF)

DEVICE RISE/FALL (ns) x—x

T_R/T_F

TOTAL LOAD CAPACITANCE (pF)
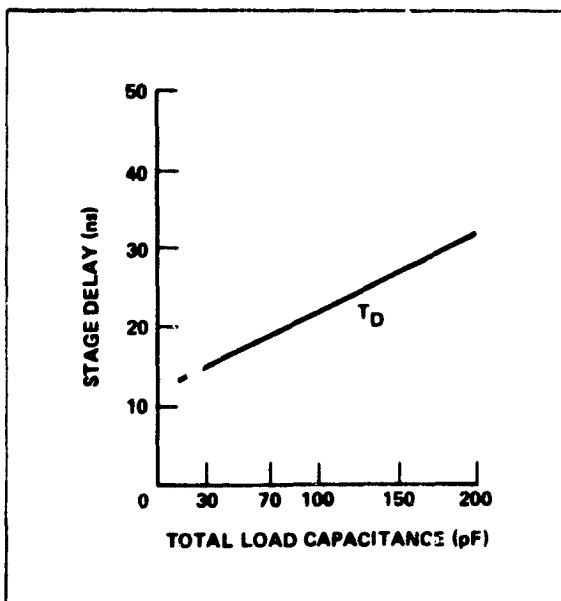
INVERTING BUFFER INPUT PAD	SOS STANDARD CELL NO. 9030 & 9040

DEVICES 2

PADS   CELL WIDTH = 8 MILS   7 MIL FAMILY @ 10 V

SCHEMATIC

+V

16.0

A   Z

10.4

G

LOGIC SYMBOL

A   2,2
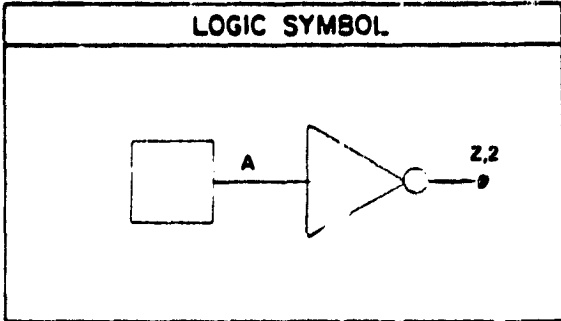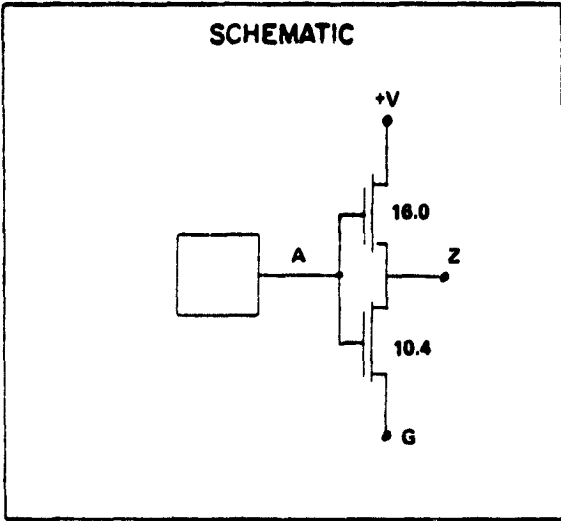
TRUTH TABLE

A	Z
0	1
1	0

PIN	CAPACITANCE (pF)
A	2.5
2	0.1

CELL DELAY (ns) vs OUTPUT CAP. AT Z (pF)

CELL DELAY (ns) vs OUTPUT CAP. AT Z (pF)

47
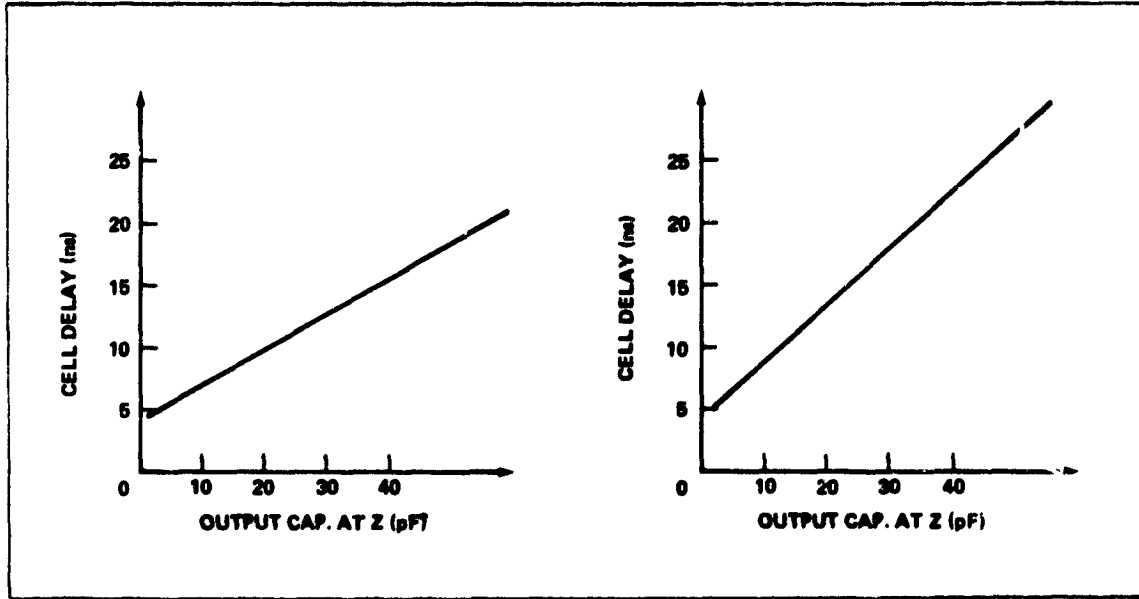
OUTPUT CELL WIDTH - 8 MILS

SCHEMATIC

+V

P-17 mils

② A

N-11.5 mils

LOGIC SYMBOL

② A   X
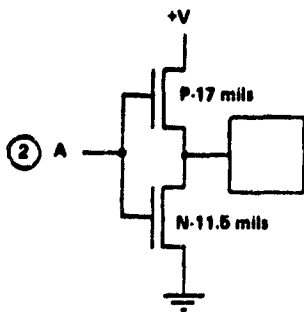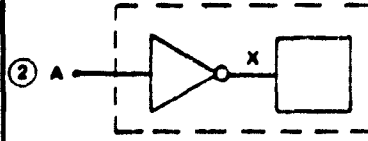
LOGIC EQUATION

$$X = \bar{A}$$

TRUTH/TABLE

A	X
0	1
1	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	2.5
X-COUT	0.03

CELL DELAY (ns)

17.0

5.1

OUTPUT NODE CAP. (pF)

OUTPUT EDGE, 10-90% (ns)

25.2

6.2

OUTPUT NODE CAP. (pF)

48
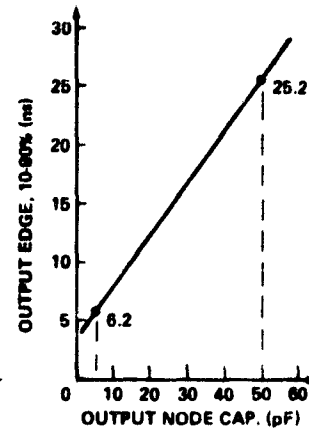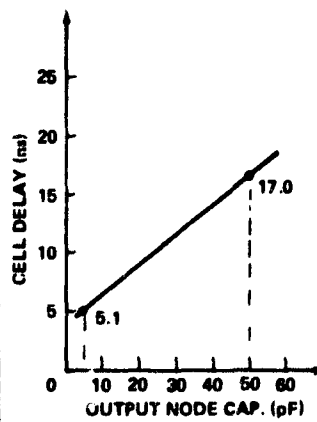
SOS STANDARD
CELL NO. 9130/9140

4 DEVICES

1 PADS **CELL WIDTH = 8 mils**

SCHEMATIC

V_{DD} V_{DD}

P 1.7 P 16.5

A   X

N 1.0

N 10.5

LOGIC SYMBOL

A   X   2

PIN	CAPACITANCE (pF)
2	0.08

TRUTH TABLE

A	X
1	1
0	0

DELAY (ns) vs TOTAL LOAD CAP. (pF)

RISE/FALL TIME (ns) vs TOTAL LOAD CAP. (pF)

49