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DIGITAL DATA RECORDING SYSTEM (DDRS) OPERATING AND MAINTENANCE MANUAL

Final Technical Manual under Contract NAS9-15217, Sub Task 4

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I. BACKGROUND

When the NASA/JSC B-57 synthetic aperture radar (SAR) development testbed program was planned, an existing side-looking radar, the APQ-102, was selected for remote sensing study programs. This radar is a purely analog system, employing photographic processing and azimuth correlation using analog film processing into a SAR map. When the investigation was expanded to include parametric variation for digital SAR, a system had to be acquired to digitize the video data produced by the APQ-102 and to record it on a wideband tape recorder aboard the aircraft.

The system designed and built by ARL:UT is called the digital data recording system, or DDRS. In addition to digitizing the raw (pulse compressed) video signals from the radar, the system provides for recording various parameters from the radar operating environment, such as the inertial platform signals and aircraft operating parameters. These parameters are necessary in the reconstitution of the radar video into a synthetic aperture high resolution radar map.

The purpose of the DDRS is to supplement the analog radar system with a digital SAR system which will permit the study and analysis of various radar parameters, leading to the effective design of an orbiting SAR for remote sensing applications.

II. SYSTEM DESCRIPTION

The DDRS is mounted on a pallet carried in the pressurized and temperature controlled electronic equipment bay of a testbed aircraft, an RB-57.

A. Aircraft and Radar

1. B-57 Flight Testbed

The aircraft testbed is a light twin-engine jet designed for high altitude operation, up to 65,000 ft. At this height the synthetic aperture radar (SAR) has the capability of simulating, in the geometry of ground mapping, the look-down angles (complement of nadir angle), associated with a SAR on an orbital platform. There are usually two flight modes at 60,000 ft: a start map nadir angle of 15°, or of 45°. The 15° nadir angle gives a swath coverage for the SAR map of 2.5-12.5 nmi (called Mode 1), and the 45° nadir angle gives coverage of 10-20 nmi--a 10 nmi swath (Mode 2). See Figs. 1 and 2. Two antennas (and receivers) are used to obtain both horizontal and vertical polarized radar data.

The B-57 is equipped with the LTN-51 inertial platform, with clutter lock for velocity update. This platform provides antenna stabalizing signals to the radar antennas, and provides velocity information required for the synthetic aperture radar system.

The aircraft normally operates at a ground speed of about 400 kt, and this is important since the radar pulse repetition frequency (prf) is set at twice the ground speed in feet per second; in this case, 2 × 675, or 1350 pps.

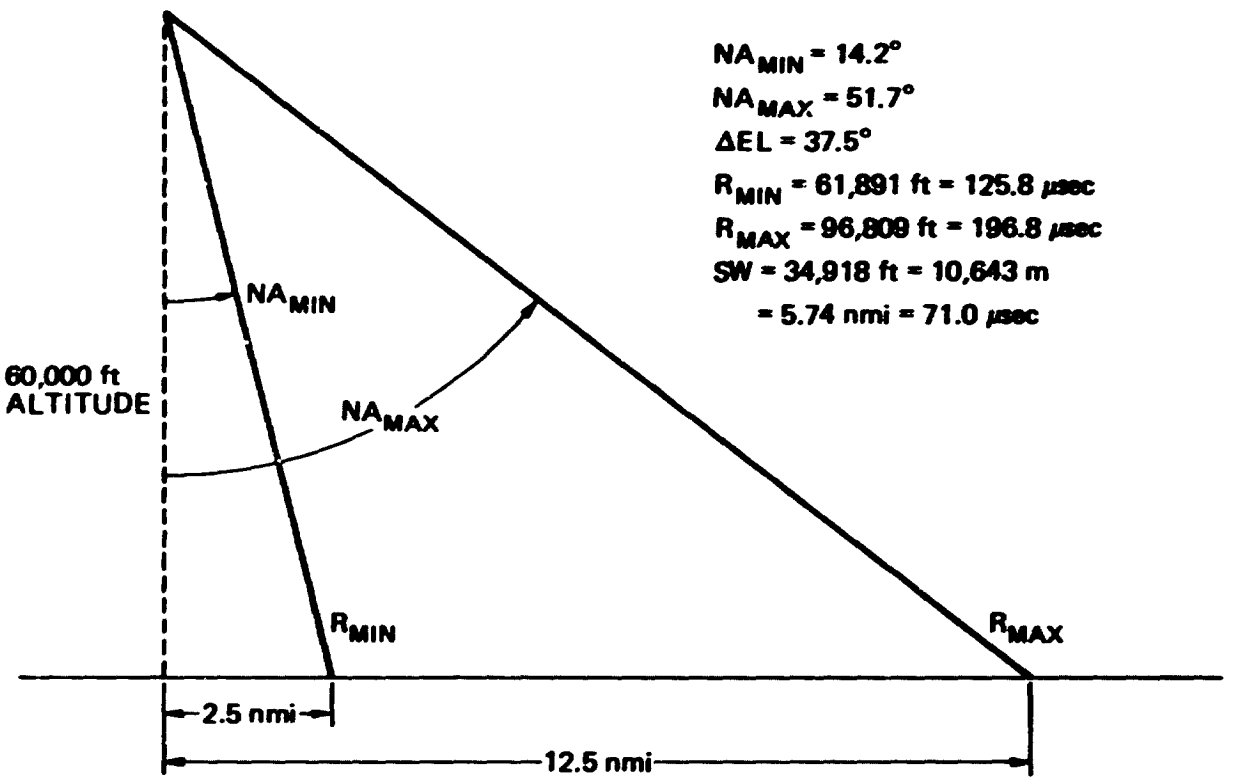


FIGURE 1
MODE 1 GEOMETRY

ARL:UT
AE-80-01
CRG-GA
9-11-80

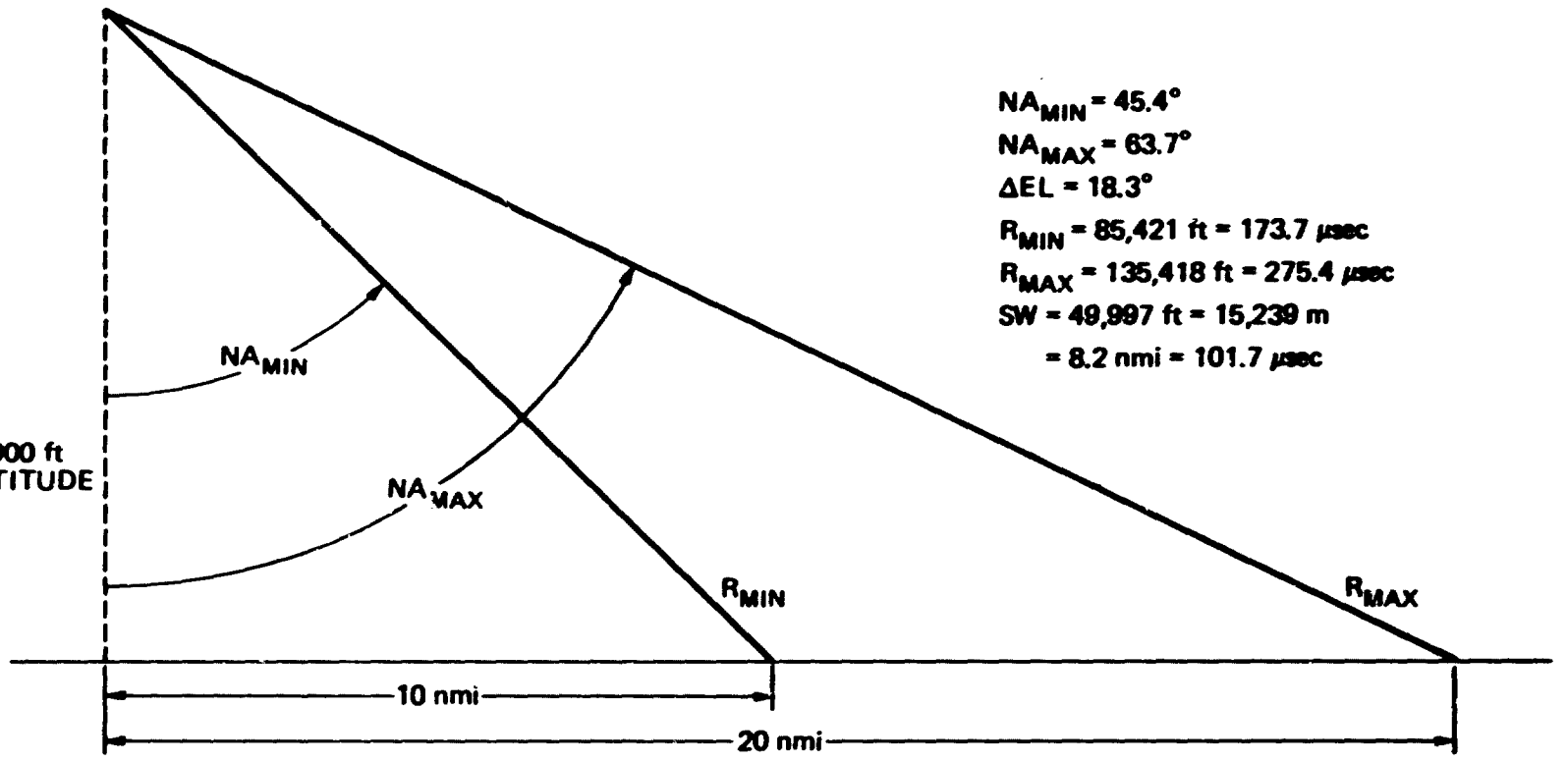


FIGURE 2
MODE 2 GEOMETRY

ARL:UT
AE-80-92
CRG-GA
9-11-80

The APQ-102 uses linear FM pulse compression and the pulse compressed, noncoherent video signals from the two receiver channels are provided to the DDRS for high speed conversion to digital format.

The radar uses sensitivity time control (STC) and it is the STC trigger which starts the DDRS data recording function.

Figure 3 indicates the various equipment locations in the testbed aircraft. A DDRS control panel in the cockpit permits the crew to digitize and record the SAR map data. The wideband (MINCOM) recorder is located in the pressurized section of the aircraft, and the right and left looking antennas are in the nose of the RB-57.

2. APQ-102 Radar

The radar is a standard Air Force procured item with some significant modifications. The original radar had a single polarized antenna; the modified system has both vertical and horizontal polarized receiver channels, both of which are recorded. The antenna has a cosecant squared pattern in elevation.

Another important modification is in the photographic film used for video recording. A 5 in. wide film is exposed with a 2 in. width utilized for each video channel, horizontal and vertical. This film is used in the azimuth correlation process, the usual analog processing which develops the SAR map.

The two channels of 15 MHz video are already motion compensated and pulse compressed when they are digitized by the DDRS. The antenna gimbals receive stabilizing signals from the LTN-51 inertial platform, and these motion compensating servo signals are recorded along with other dynamical parameters of the system.

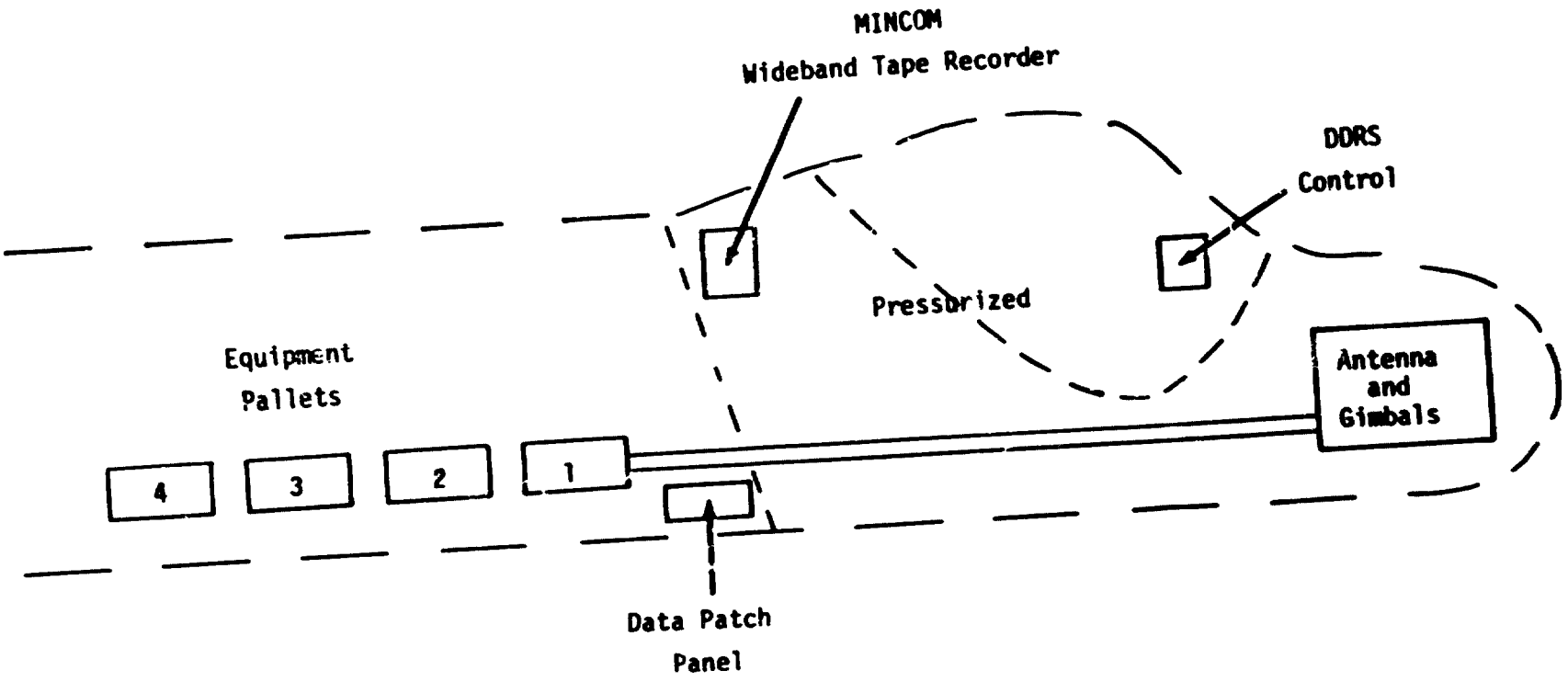


FIGURE 3
AIRCRAFT EQUIPMENT LOCATIONS

The radar operates at an X-band frequency with variable prf, as indicated previously, such that two samples per foot of the synthetic aperture are obtained.

In addition to the two channels of video data, which the DDRS records, various radar parameter environment (RPE) signals are recorded. Figure 4 shows the sources of these. Some are obtained from the universal programmable parameter stripper (UPPS), designed and built by Lockheed for NASA, and the data are from the NASA Earth Resources Data Acquisition System (NERDAS). The data are recorded on a wideband MINCOM tape recorder, carried in the pressurized section of the RB-57, after processing through the DDRS.

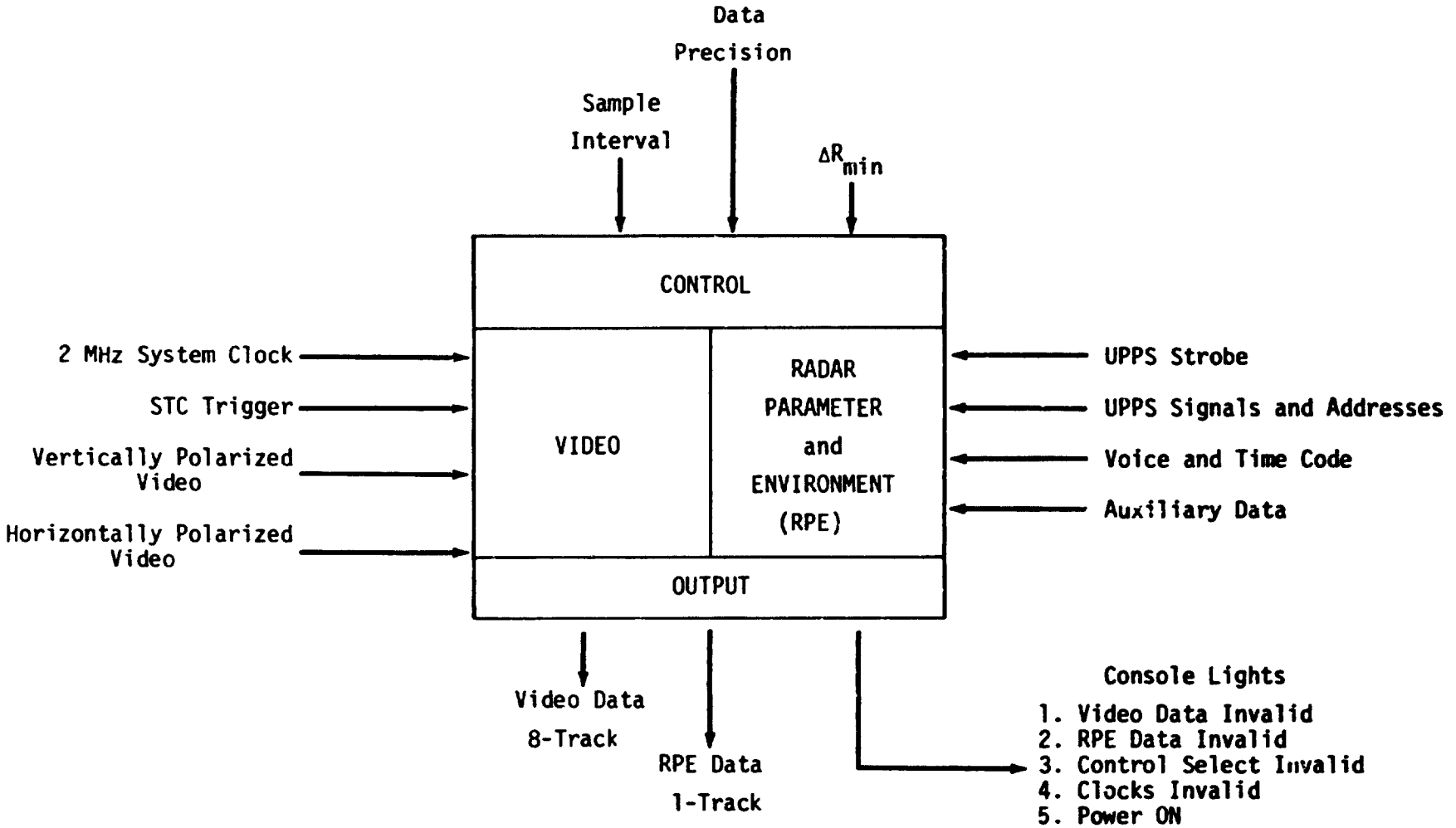


FIGURE 4
DIGITAL DATA RECORDING SYSTEM
OVERVIEW

III. DDRS DESCRIPTION

The unit is designed to digitize the radar data and format it and the RPE data into a format compatible with the Hughes Aircraft digital recording interface equipment (DRIE). The DRIE is used at the ARL:UT SAR playback facility to both play back wideband tapes and reformat them onto computer-compatible tapes (CCT) on a 9-track standard tape recorder. Figure 5 is a block diagram of the system.

A MINCOM wideband tape recorder on board the aircraft produces 14 tracks of RPE and video data, which can be played back at the ARL:UT facility, since the data are properly formatted by the DDRS to be compatible with the DRIE playback equipment. The Doppler analysis software, called the ground signal processor (GSP), will produce digital SAR images on a high resolution display from the filter outputs.

A. Functions of the DDRS

The principal function of the DDRS is to digitize the two channels (called H and V) of raw video developed by the APQ-102 from the 70 MHz IF. In addition, it provides a single record track of RPE data corresponding to the video data. Figure 4 illustrates the sources of the data on which the DDRS operates, and the controls used by the operator to obtain the desired outputs to the wideband tape recorder.

The timing of the system is critical; it is controlled by the radar (APQ-102) timing. This comes from a 2.07065 MHz clock which controls a coherent oscillator in the DDRS. The start of a range sweep is controlled by the sensitivity time control trigger. The two video channels are picked off from the optical recorder of the radar system.

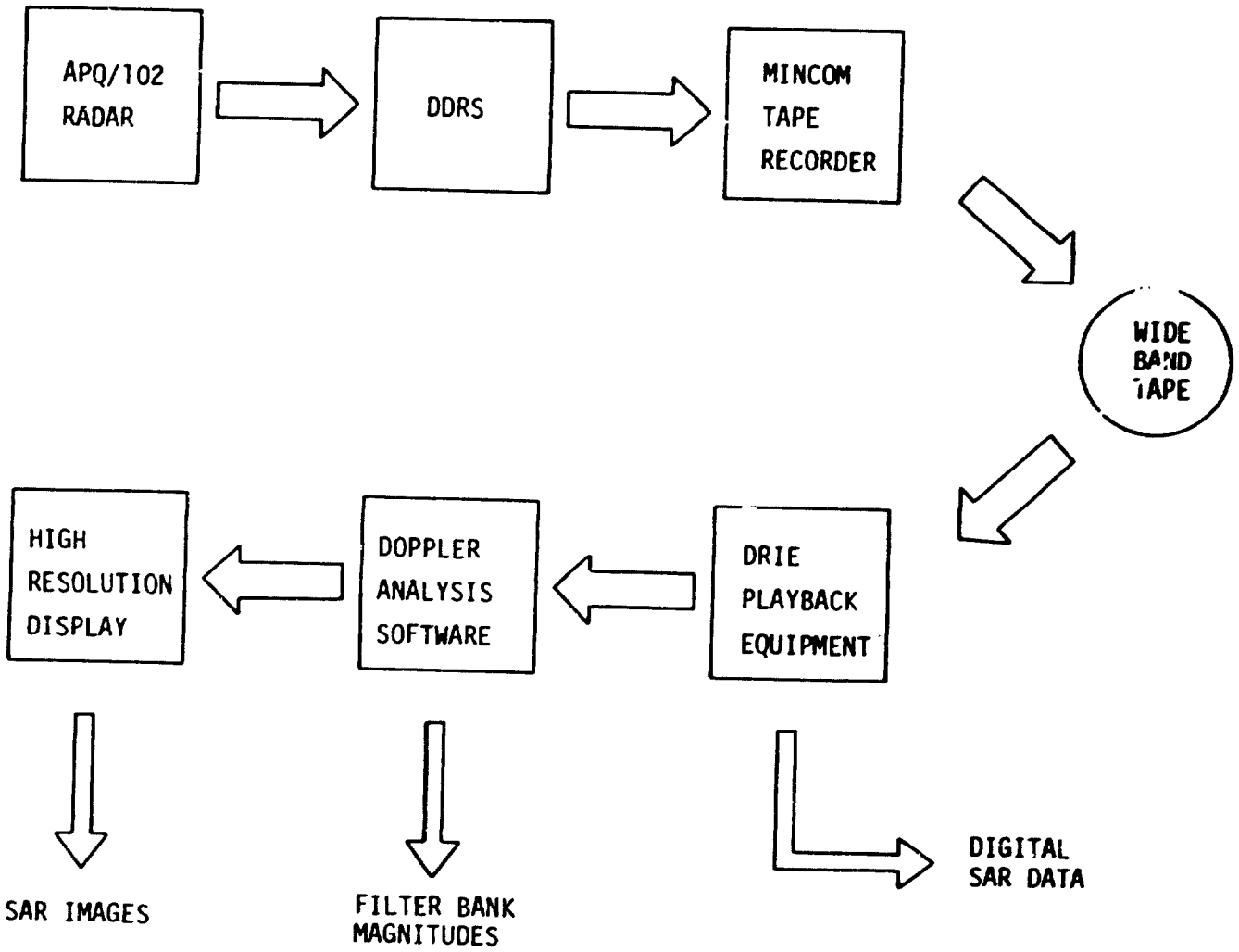


FIGURE 5

SAR DATA FLOW

The universal programmable parameter stripper (UPPS) is a device which permits digitally coded radar system parameters to be input to the DDRS in a compatible format. Voice and time code data are also input for recording on the wideband tape.

The cockpit-mounted control panel permits an operator to enter a delay time from the start of the STC trigger to set the starting range for the radar map--a value called ΔR_{min}. The sampling rate may also be set by selecting the value of the sample interval. Finally, the operator may select from 7-, 4-, 2-, or 1-bit data precision.

1. Digitizing

The DDRS digitizes analog video in video A/D board 6. Two channels of video are digitized at a sample rate set by the operator (a crew member) setting switches which select the sample interval (SI) and the start of sampling (DRMIN), which is a selected delay from the STC trigger. The latter is routed through the AGC/STC processor, which is a Lockheed-built special device for the APQ-102 radar. See Fig. 6.

Besides the video, certain monitored environmental signals in the DDRS, temperature and pressure and operating voltages, are digitized externally in the auxiliary data board, located in the AGC/STC processor. Analog signals are shipped out to the auxiliary data board, converted to digital, and transferred back out to the DDRS, where they are formatted in the same manner as the UPPS data.

2. Recording

Figure 7, the DDRS block diagram, indicates those signals recorded on the wideband MINCOM tape recorder. One track of the recorder is used for the RPE data, made up from the UPPS output and the auxiliary data coming from the auxiliary data board. These digital data are transferred through the auxiliary data bus. Eight tracks of the recorder are used for the digitized video. All the digitized data are routed through

Lockheed-built AGC/STC Processor

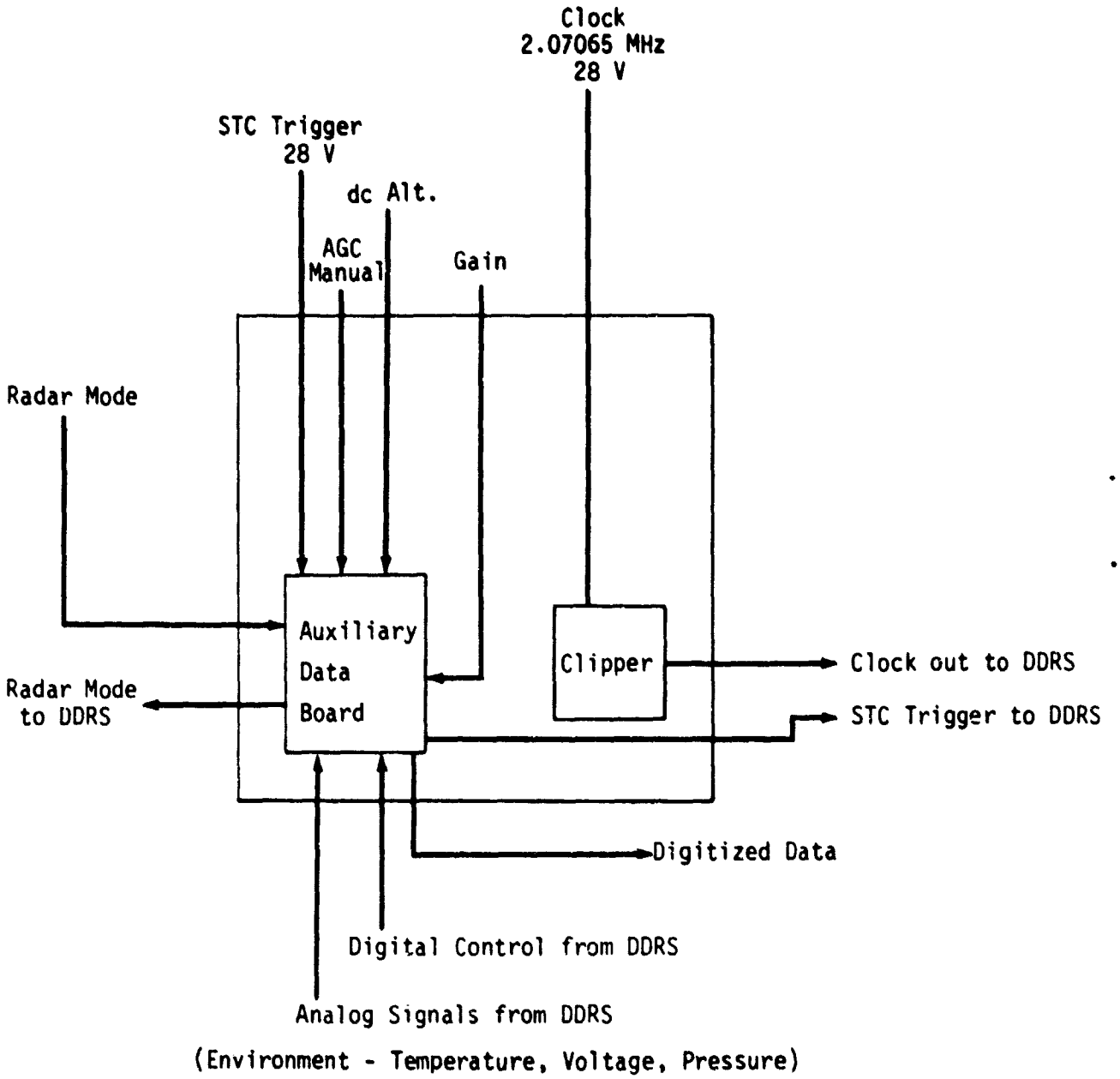


FIGURE 6

AGC/STC PROCESSOR WITH AUXILIARY DATA BOARD

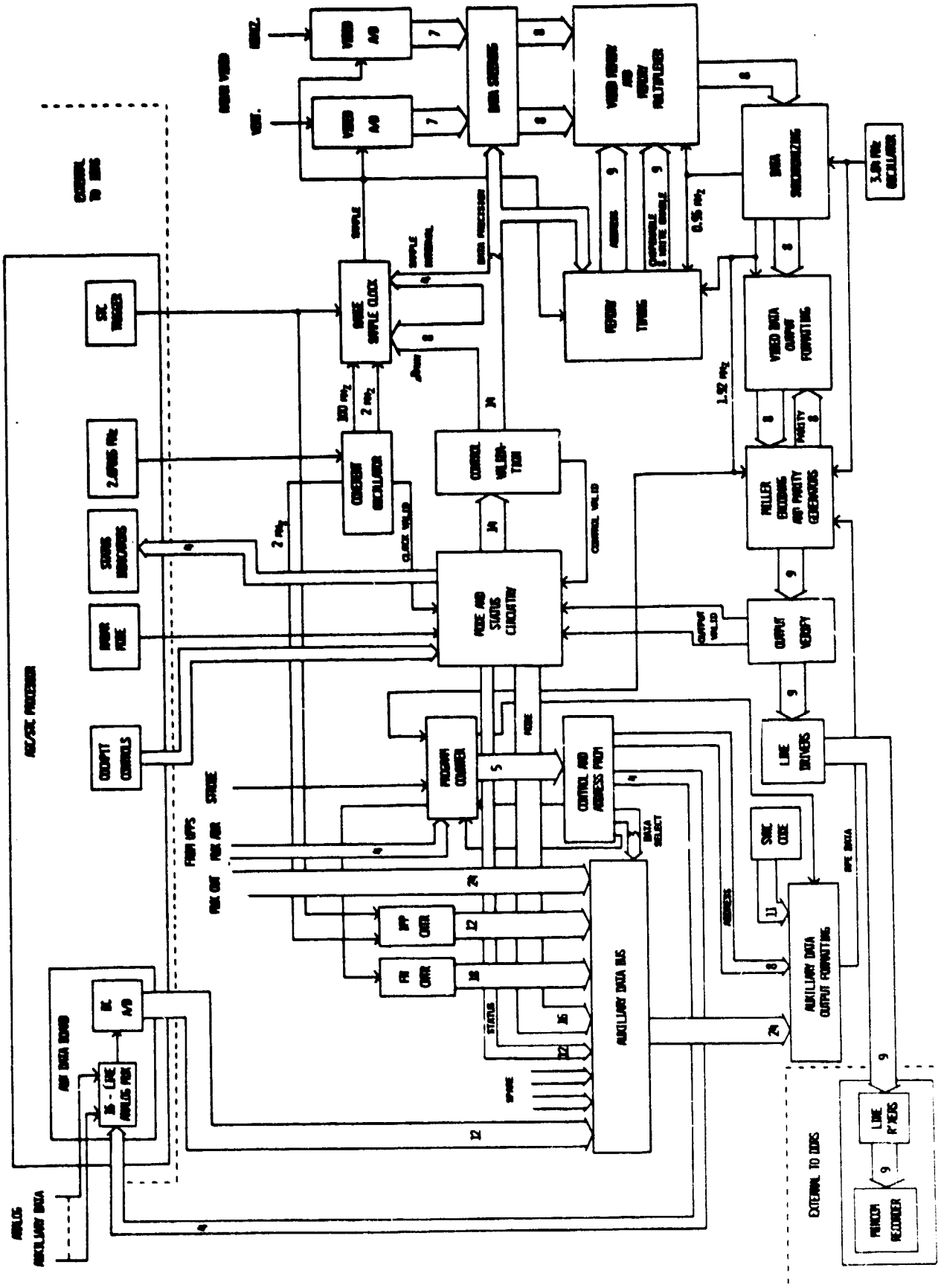


FIGURE 7
DDRS BLOCK DIAGRAM

Miller encoders and a parity bit generator. The LSB of the video tape data is used for parity check (only in the 7-bit mode).

In addition to the outputs of the DDRS recorded in the MINCOM recorder, the voice from the crew and ground stations and time code signals from the IRIG time code generator are frequency modulation coded, and recorded on two more tracks of the MINCOM tape recorder. This is, of course, independent of the DDRS.

B. Interfaces

The principal interfaces of the DDRS are with the radar system, to obtain the video data, with the NERDAS outputs via the Lockheed-built UPPS, with the auxiliary data board in the STC/AGC processor (built by Lockheed), the cockpit-mounted control box, and the DRIE by way of the wideband recorder. These will be described in turn.

1. Radar

Refer to Table I. The horizontal and vertical channel video signals, pulse compressed bipolar (±0.5 V) analog signals are supplied to the DDRS from the optical recorder subsystem of the APQ-102. A test signal is generated as a reference on the video A/D board, variable from zero to negative full scale for the analog input. This signal is furnished on a connector for use in testing and adjusting the video inputs.

2. UPPS/NERDAS

Four address lines and a strobe signal are supplied from the Lockheed-built universal programmable parameter stripper. In addition, on a separate connector (J-101), 24 data lines are available from the UPPS. These are differential, TTL signals.

TABLE I

LIST OF FRONT PANEL CONNECTOR SIGNALS FOR THE DDRS

J101:	MUX_0 - MUX_{23}; differential signal inputs from the UPPS, TTL.
J102:	ADD_0 - ADD_3, and STRB; differential signal inputs from the UPPS, TTL.
J103:	REF; analo voltage reference output to patch into video inputs for test, 0 to -1 Vdc, adjustable on Board 6. TRIGRPE, TRIGVID: scope trigger output for the RPE and video channels, respectively; TTL. $VIDNRZ_0$ - $VIDNRZ_7$; video data outputs, unencoded for scope viewing, TTL. RPENRZ; RPE data output, unencoded, TTL. PARCHK; parity error pulse output, for connection to an event counter, TTL. $\overline{\text{RPETEST}}$; input, when grounded puts the RPE subsystem into the test mode. AUX/UPPS; input, when $\overline{\text{RPETEST}}$ is grounded, determines either auxiliary or UPPS data to be displayed, UPPS when grounded.
J104:	VIDMIL: differential outputs, Miller encoded video data, to recorder, TTL.
J105:	SI_0 - SI_3; ±5 V inputs, binary coded sample interval control. $DRMIN_0$ - $DRMIN_7$; ±5 V inputs, 9's complement BCD delta RMIN control. DP_0 - DP_1; ±5 V inputs, data precision control. RPEINVAL, VIDINVAL, CNTINVAL, ORALT, CLKINVAL: TTL outputs, TRUE (+2 V, 20 mA) indicates, respectively, poor RPE data, poor video data, invalid control setting, video overrange, clock out of sync. PWR ON; +2 V, 20 mA output whenever power is applied.

TABLE I (Cont'd)

LIST OF FRONT PANEL CONNECTOR SIGNALS FOR THE DDRS

	N5.7; - 5.7 V "false" voltage reference to control switches, limited by 100 Ω.
J106:	AUX ADD_0 - $AUXADD_3$, AUXCLK, AUXST: differential outputs to the auxiliary data board in the AGC/STC processor, TTL. RADMODE: AUXDATA, AUXSTRB, STCTRIG, differential inputs from the auxiliary data board, TTL. N2, P5, N5.7, TEMP1, TEMP2, PRES; analog dc voltage outputs to auxiliary data board, TTL. P15, +15 V at 20 mA, resistor limited, from the auxiliary data board. SYSCLK: 2.07065 MHz, TTL system clock signal input from the auxiliary data board.
J107:	+28 V with return at 4 A max, fused; 200 V, 400 Hz, 3-phase, at 300 mA max
J108:	50 Ω vertical polarization video input from the optical recorder. Level is adjustable from ±0.5 V pp to ±1.0 V pp. The input is dc coupled.
J109:	50 Ω horizontal polarization input, at the same level as J108.

3. Auxiliary Data Board

Because of inadequate processing space in the DDRS, certain analog signals are shipped out to the AGC/STC processor for conversion to digital signals on the auxiliary data board. These are pressures, temperatures, and voltages, which are monitored in the DDRS and recorded on the wideband recorder. Clock strobe outputs and inputs control the operation of the auxiliary data board. Other outputs from the AGC/STC processor that involve the auxiliary data board are the STC trigger, which initiates a digitizing cycle in the DDRS, a dc altitude signal which is digitized and sent back to the DDRS for formatting, a signal conditioned 2.07065 MHz clock pulse, and a digitized radar mode signal.

4. Controls

The cockpit-mounted control panel permits an operator to send control signals in digital form to the DDRS. The operator can select the sample interval (SI), data precision or number of bits (DP), and the start sampling range (DRMIN). Power ON and logic voltages are also supplied. Signals sent to the control panel are invalid signals for the clock, video, and RPE data, to inform the operator of a problem in the DDSP. A control invalid (CNT INVAL) signal informs the operator that an invalid set of switch settings has been selected. An over-range alert (OR ALT) signal alerts the operator to video signals which are exceeding the range of the A/D converters.

5. Recorder

Eight tracks of formatted video (in FLAMR format) are sent to the wideband tape recorder in Miller code, and one track, similarly formatted and coded, of RPE data. A clock output signal is furnished to the same connector (J-104); however, it is not recorded.

6. Power

The DDRS uses +5 V for TTL operations, and -5.75/-2.0 V for MECL operations. These are supplied from two integral dc power supplies, which are driven from the aircraft 28 Vdc bus. A cooling fan is driven by 400 Hz ac power.

7. System Test

Video and RPE data encoded in NRZ format are supplied on connector J-103 for other uses, such as checking the performance of the DDRS in real time. A RPE test signal and a signal to select between UPPS and the auxiliary data board are input to the DDRS. A RPE trigger and parity check signal are supplied on the same connector, as is a video trigger.

C. Performance Specifications

1. Controllable Parameters

Number of Range Samples Recorded:

7-bit data: 512 per polarization channel
4-bit data: 1024 per polarization channel
2-bit data: 2048 per polarization channel
1-bit data: 4096 per polarization channel

Allowable Slant-Range Sample Intervals: 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150 nsec

Recorded Slant Range and Ground Range Swath Widths:

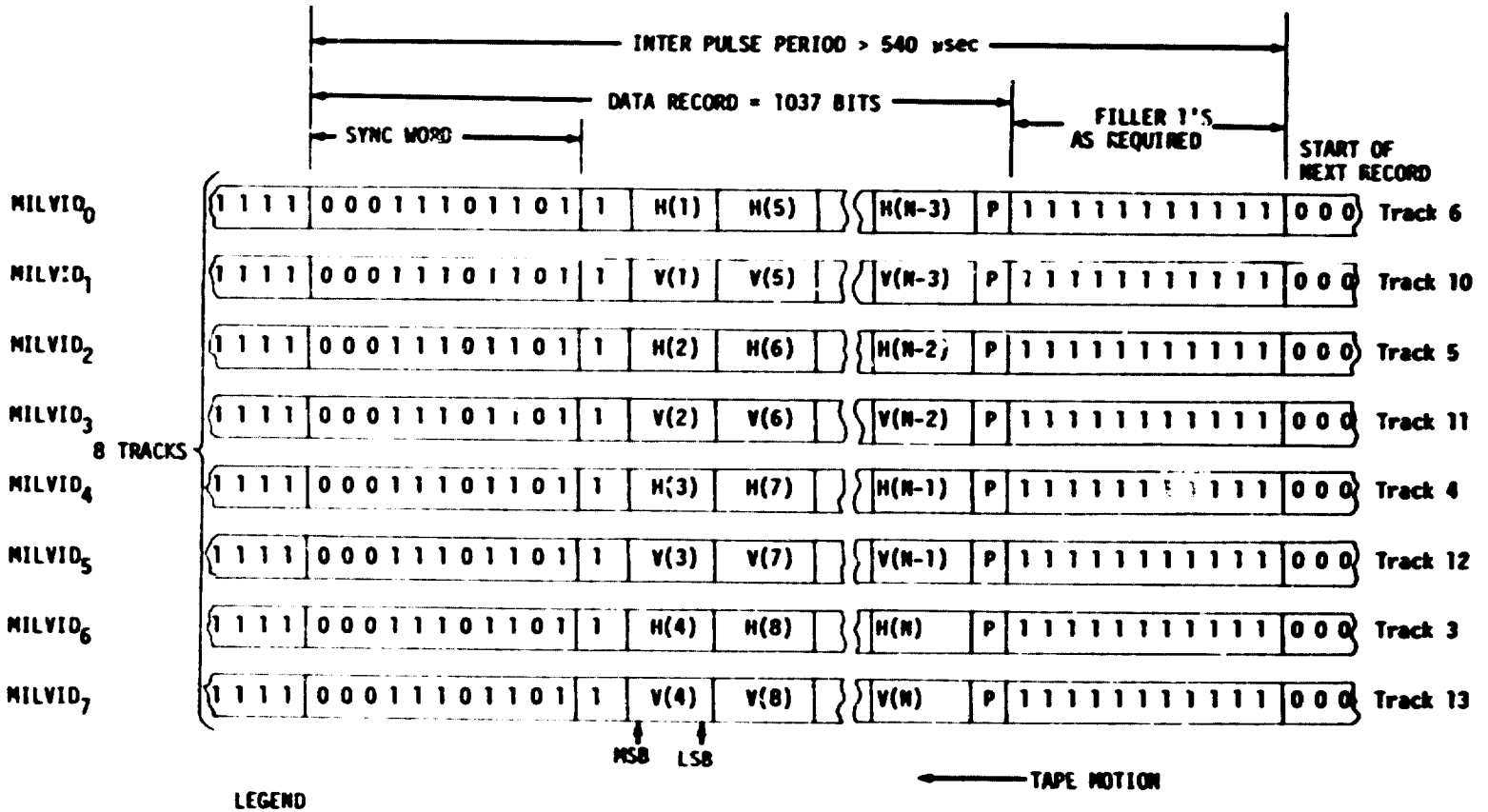
Slant Range Sample Interval (nsec)	Data Precision (bits)	Slant Range Swath Width (km)	Mode 1 G-R Swath (nmi)	Mode 2 G-R Swath (nmi)
40 (6.0 m)	7	3.1 (1.66 nmi)	2.5 - 6.5	10 - 12.2
"	4	6.1 (3.31 nmi)	2.5 - 9.2	10 - 14.3
"	2	12.3 (6.62 nmi)	2.5 - 13.6	10 - 18.2
"	1	24.6 (13.2 nmi)	2.5 - 21.2	10 - 25.4
50 (7.5 m)	7	3.8 (2.07 nmi)	2.5 - 7.3	10 - 12.7
"	4	7.6 (4.14 nmi)	2.5 - 10.4	10 - 15.3
"	2	15.2 (8.28 nmi)	2.5 - 15.6	10 - 20.0
"	1	30.4 (16.6 nmi)	2.5 - 24.9	10 - 29.0
60 (9.0 m)	7	4.6 (2.48 nmi)	2.5 - 7.9	10 - 13.3
"	4	9.2 (4.97 nmi)	2.5 - 11.5	10 - 16.3
"	2	18.4 (9.94 nmi)	2.5 - 17.5	10 - 21.9
"	1	36.8 (19.9 nmi)	2.5 - 28.4	10 - 32.5
100 (15.0 m)	7	7.6 (4.14 nmi)	2.5 - 10.4	10 - 15.3
"	4	15.2 (8.28 nmi)	2.5 - 15.6	10 - 20.0
"	2	30.4 (16.6 nmi)	2.5 - 24.9	10 - 29.0
"	1	60.8 (33.2 nmi)	2.5 - 42.2	10 - 46.2

Available Delays from STC Trigger to Start of Sampling:

2-99 μsec in 1 μsec intervals

2. Video Characteristics (each polarization channel)

Video Input Impedance	75 Ω
Video 3 dB Bandwidth	>20 MHz
Maximum Video Level (adjustable)	±1.0 V
Maximum Video Sampling Rate	25 MHz
Conversion Accuracy	<30 mV
rms Sampling Jitter	1 nsec
Digital Code after Conversion	2's complement
Minimum IPP (worst case)	700 μsec
Data Record Format to Tape	Fig. 8
Tape Track Encoding	Miller Code
Tape Track Assignment	Table II



LEGEND

H(2) = H DATA FOR RB NO. 2
V(2) = V DATA FOR RB NO. 2
P = PARITY BIT

FIGURE 8

VIDEO DATA RECORD FORMAT

TABLE II

MINCOM RECORDER OPERATING PARAMETERS

Record Electronics Required:	11 Channels IRIG Wideband Direct Record
Record Speed:	120 ips
Tape Used:	Scotch Type 888-1-9200-IRH, (1"x9200'), Stock No. 84-9800-3637-4, or equivalent
Tape Reels Used:	14 in. metal precision
Record Time:	920 sec (15.3 min)

Recorder Track Assignments:

Track	Signal
1	IRIG Time Code
2	Open
3	Video Data Channel 6 (1.92 Mbs Miller Code)
4	Video Data Channel 4 "
5	Video Data Channel 2 "
6	Video Data Channel 0 "
7	RPE Data (1.92 Mbs Miller Code)
8	Open (FLAMR PPD Track)
9	Open (FLAMR FB Track)
10	Video Data Channel 1 (1.92 Mbs Miller Code)
11	Video Data Channel 3 "
12	Video Data Channel 5 "
13	Video Data Channel 7 "
14	Voice Direct

3. RPE Characteristics

Data Sampling Frequency (established by NERDAS)	100 Hz
Data Types and Formats	Table III
Data Record Format to Tape	Fig. 9

4. Power Requirements

+28 Vdc at 4 A max

200 Vac, 400 Hz, 3 Phase at 0.4 A max

5. Physical Characteristics

Weight	25 lb
Dimensions	13 1/4 in. L x 8 1/2 in. W x 9 3/8 in. H

D. Hardware Description

1. Mechanical Overview and Interconnection Scheme

The circuitry of the DDRS, other than the auxiliary data board, is contained in a custom fabricated enclosure designed for mounting in the RB-57 electronic pallet (Dwg. No. 1). On the back panel of this enclosure are mounted all input and output cylindrical connectors (J-101-J-109). Inside the enclosure are mounted two power supplies, a cooling fan, and a card cage with eleven numbered card slots, six of which (slots 2, 4, 6, 8, 9, and 11) contain circuit boards and one of which (slot 1) contains a cable connecting board.

Drawings No. 2 and 3 show the wiring scheme inside the enclosure. The six circuit boards plug into the backplane connectors (J2, J4, J6, J8, J9, J11) through the board-mounted plug connectors (P2, P4, P6, P8, P9, P11). The backplane connectors are wired to one another by wirewrap connections according to the backplane wiring diagram, Dwg. No. 2. Also, the circuit board plugged into J2 (in card cage slot 2) is connected to

TABLE III

RPE DATA FORMAT

	Data Bit Numbers (MSB 23 20 16 12 4 0 LSB)						
1. TIME	10xH	1xH	10xMIN	1xMIN	10xSEC	1xSEC	BCD
2. DATE	10xYR	1xYR	10xMO	1xMO	10xDAY	1xDAY	BCD
3. LATITUDE	SIGN	10xDEG	1xDEG	10xMIN	1xMIN	.1xMIN	BCD
4. LONGITUDE	SIGN	100xDEG	10xDEG	1xDEG	10xMIN	1xMIN	BCD
5. RADAR ALT	xxxx	10kxFT	1kxFT	100xFT	10xFT	1xFT	BCD
6. HEADING	xxxx	xxxx	100xDEG	10xDEG	1xDEG	.1xDEG	BCD
7. DRIFT	xxxx	xxxx	SIGN	10xDEG	1xDEG	.1xDEG	BCD
8. ROLL	SAME AS DRIFT						
9. PITCH	SAME AS DRIFT						
10. GND SPD	xxxx	xxxx	xxxx	100xkt	10xkt	1xkt	BCD
11. VERT ACC	xxxx	xxxx	SIGN	1xG	.1xG	.01xG	BCD
12. IPP	xxxxxxxxxxxxxxxxxxxxxx			IPP_{11} ... IPP_0			BIN
				LSB = 482.94 nsec			
13. FRAME NO.	xxxxxxxxxxxx		FN_{18} ... FN_0				BIN
			incremented every 80 msec				

TABLE III (Cont'd)

RPE DATA FORMAT

14. STATUS WORD

SW_0: VIDVAL (1=video data valid)

SW_1: RPEVAL (1=RPE data valid)

SW_2: CLKVAL (1=clock in sync)

SW_3 SW_7: OR_0-OR_4 (count of video overranges in 100 msec)

LSB=8 for 7-bit precision data
LSB=16 for 4-bit precision data

LSB=32 for data precision=2-bit
LSB=64 for data precision=1-bit

SW_8 SW_{11}: $PARERR_0$ - $PARERR_3$ (count of buffer memory parity errors in 10 msec - active only in 7-bit data precision mode)

LSB=1 error

SW_{12} SW_{23}: undetermined

15. MODE WORD

MD_0 - MD_7: undetermined

MD_8 - MD_{15}: $DRMIN_0$ - $DRMIN_7$ - coded into 2 digits of 9's complement of BCD

(delta RMIN)

LSB=965.880 nsec

MD_{16} - MD_{19}: SI_0 - SI_3 (sample interval)

LSB=10.0613 nsec (inverted binary)

MD_{20} - MD_{21}: DP_0 - DP_1 (data precision)

DP_0	DP_1	Data Precision
0	0	1-bit
0	1	2-bit
1	0	4-bit
1	1	7-bit

MD_{22}: RADMODE (Radar Mode: 0=Mode 1, 1=Mode 2)

MD_{23}: CNTLVAL (1=Mode Control Settings Valid)

NOTE: FOR NERDAS DATA, THE SIGN CODE IS: + : 1110

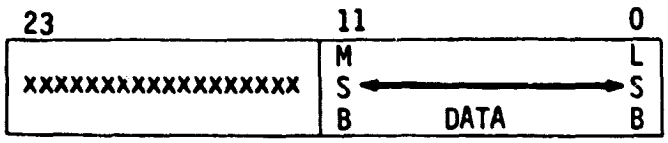
- : 1100

TABLE III (Cont'd)

RPE DATA FORMAT

RPE ADDRESS 201 - 220 (AUXILIARY DATA)

DATA FORMAT



Binary bits 0-11 define a whole number integer (N) between 0 and 4095. To translate N into its corresponding voltage for each parameter, use the following equations:

AUXILIARY DATA	EQUATION
0. UNDEFINED	Voltage = $(2.443 \times 10^{-3})N$
1. TEMP1	TEMP, °C = (0.0304) (N-1309)
2. TEMP2	"
3. TEMP3 (not connected)	"
4. TEMP4	"
5. -5.7 V DDRS	Voltage = $-(2.397 \times 10^{-3})N$
6. +5 V DDRS	Voltage = $(2.443 \times 10^{-3})N$
7. -2 V DDRS	Voltage = $-(2.397 \times 10^{-3})N$
8. +5 V AUX	Voltage = $(2.443 \times 10^{-3})N$
9. -15 V AUX	Voltage = $-(4.986 \times 10^{-3})N$
10. REF (+10 V)	Voltage = $(4.888 \times 10^{-3})N$
11. dc ALT	Voltage = $(2.443 \times 10^{-3})N$
12. AGC/MAN	Voltage = $(7.473 \times 10^{-3})N$
13. GAIN	Voltage = $(2.443 \times 10^{-3})N$
14. +15 V AUX	Voltage = $(4.893 \times 10^{-3})N$
15. PRESSURE	PSIA = $[(4.618 \times 10^{-3})N] - 3.75$

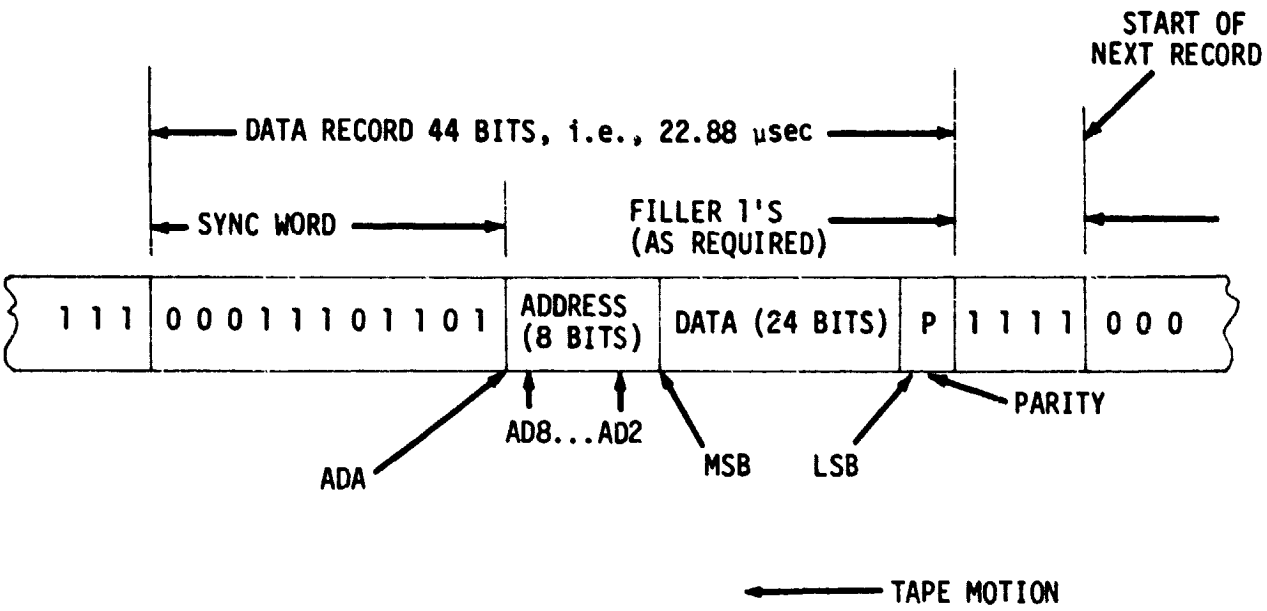
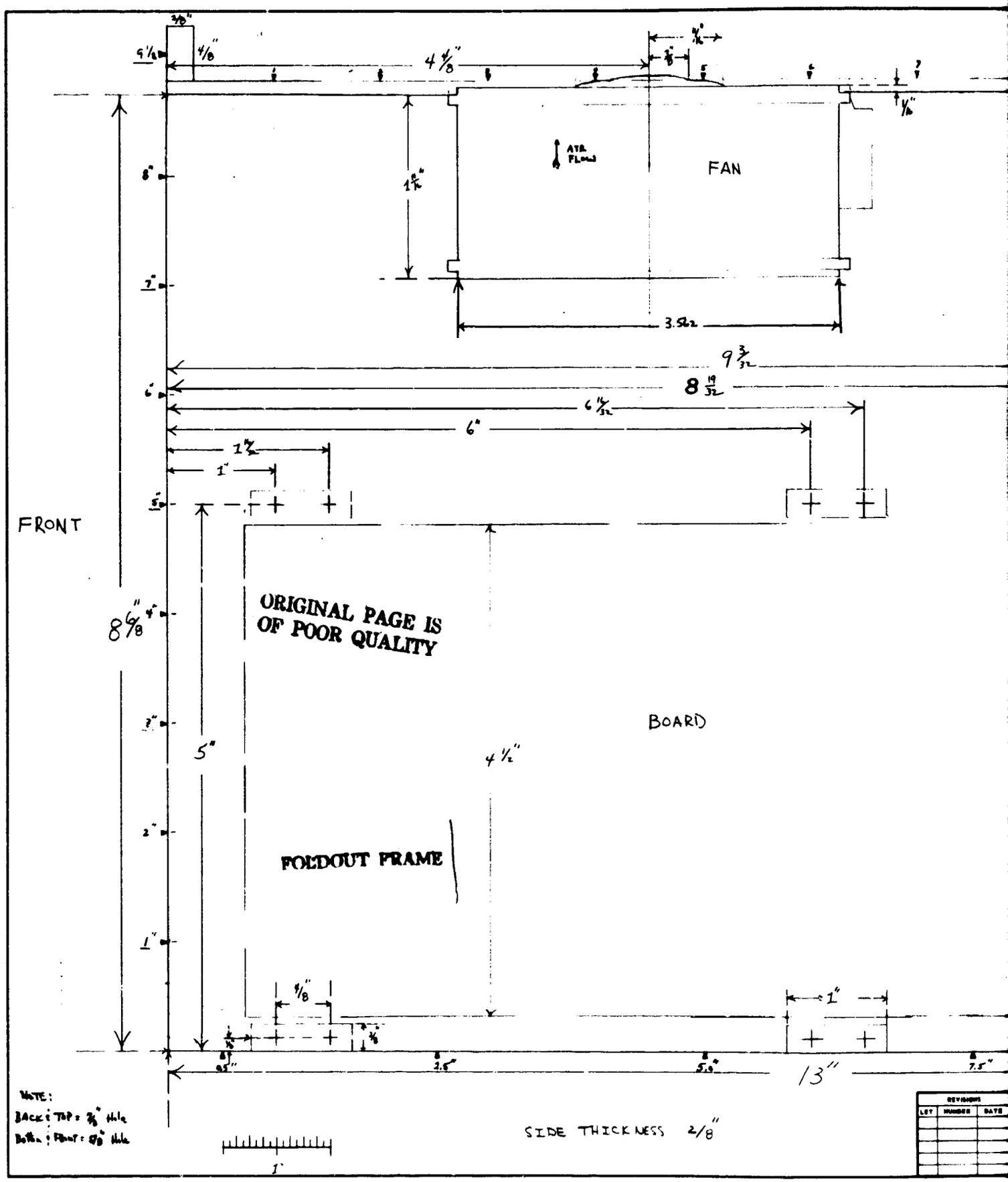
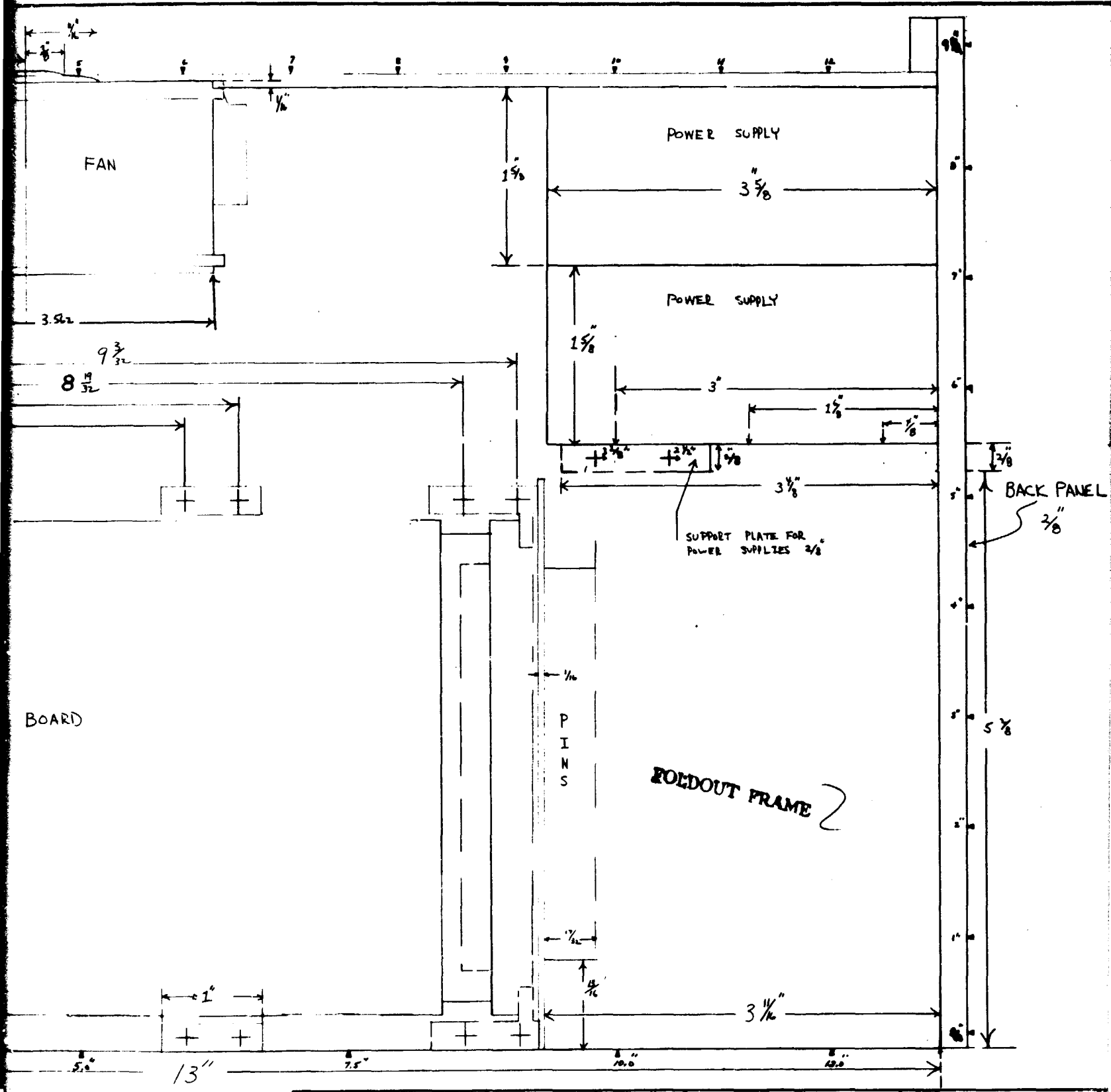


FIGURE 9

MAGNETIC TAPE FORMAT - RPE DATA RECORD


FAN
AIR FLOW
FRONT
BOARD
FOLDOUT FRAME
ORIGINAL PAGE IS
OF POOR QUALITY
4 4/8"
1 7/8"
9 3/32
8 19/32
6 1/32
6"
1 1/2
1"
8 6/8"
5"
4 1/2"
13"
SIDE THICKNESS 2/8"
NOTE:
BACK : TOP = 3/8" thick
Bottom : Front = 1/8" thick



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DECIMAL ±
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FULL VIEW
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DDRS

MATERIAL NAS9-15017-4

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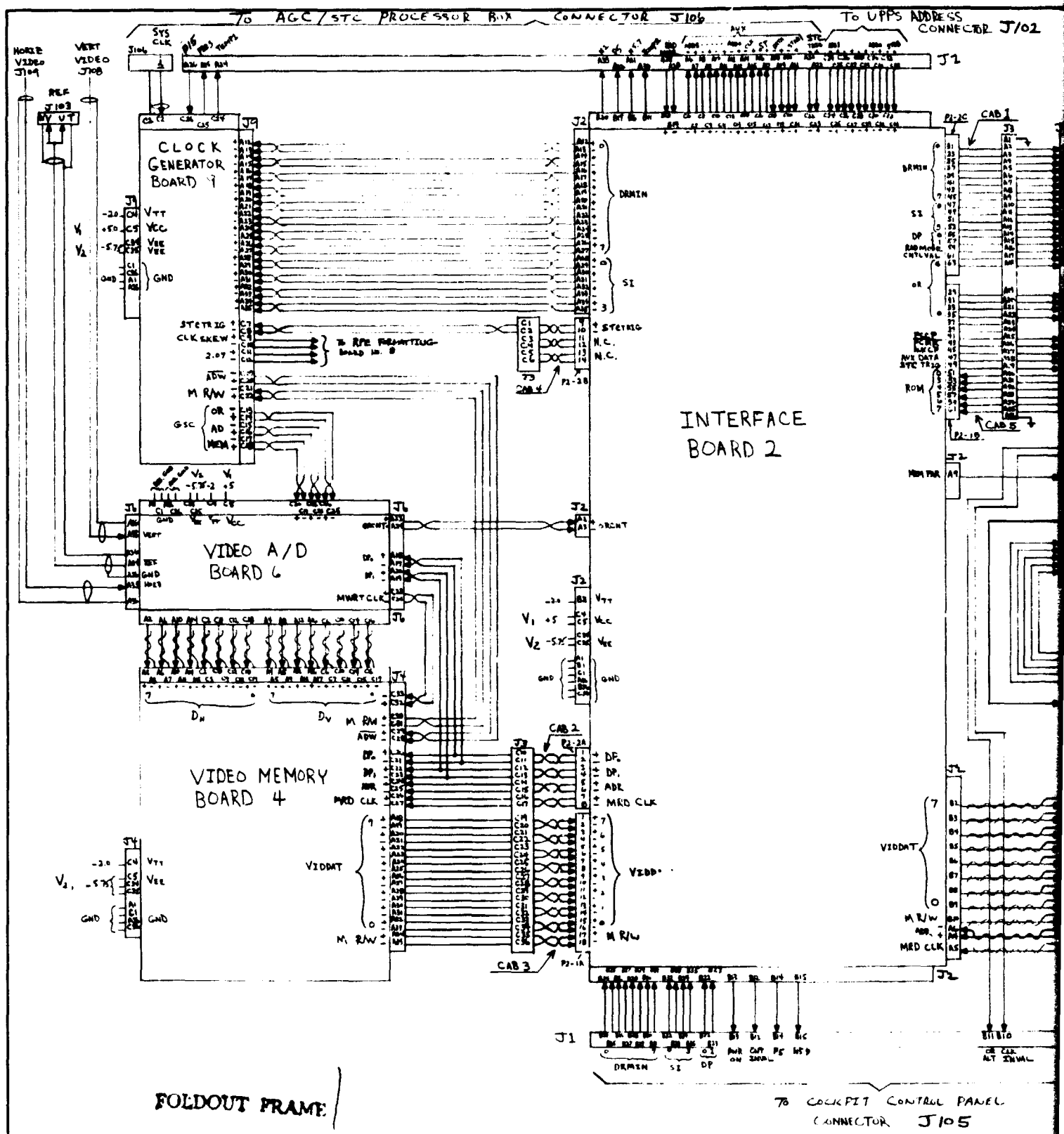
D Drawing No. 1

NESS 2/8"



FOLDOUT FRAME

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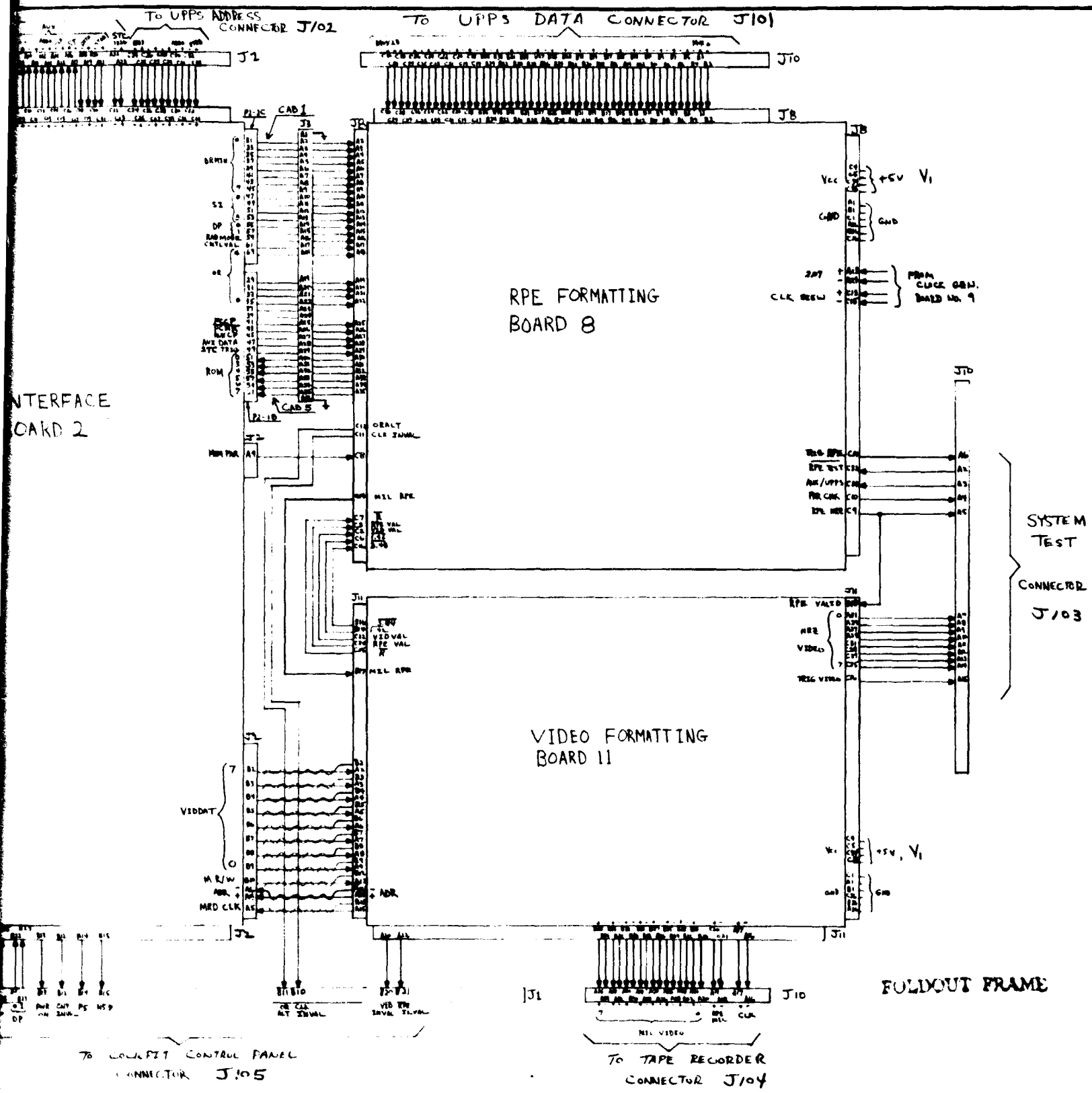

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DDRS SYSTEM PACK ASSEMBLY SIGNAL WIRING DIAGRAM

MATERIAL NA:9 15217-4

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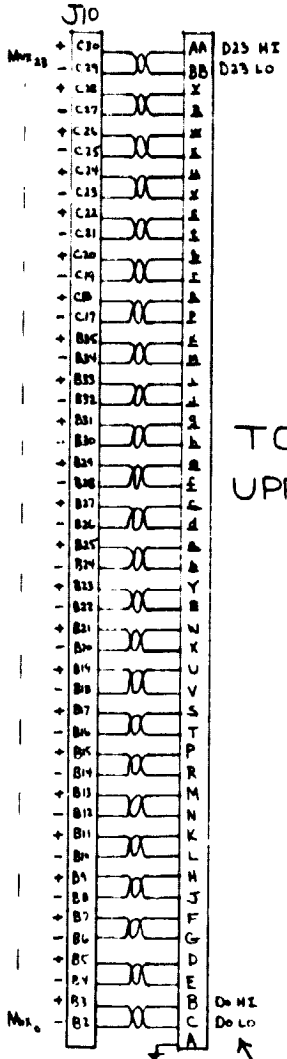
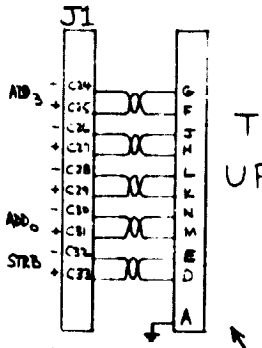
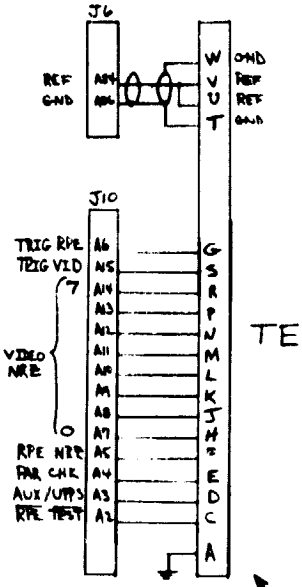
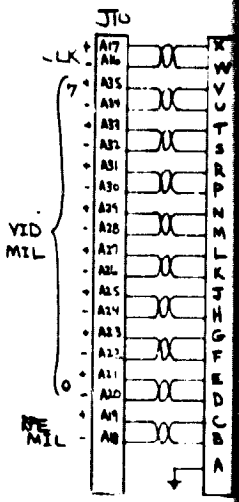
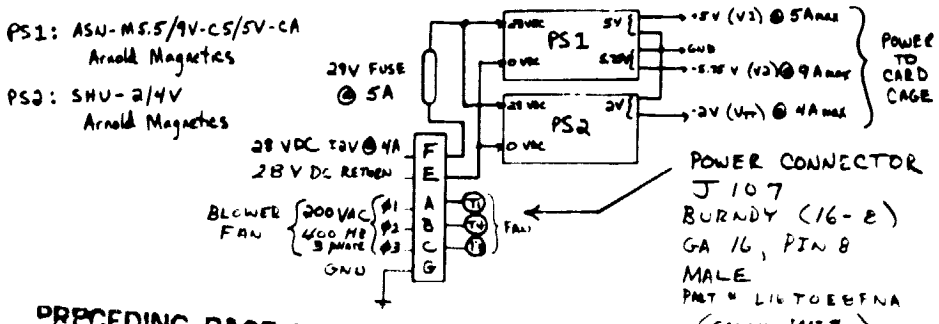
D Drawing No. 2

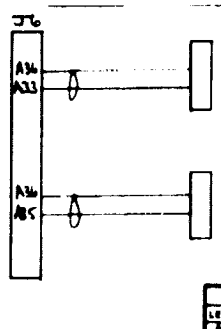












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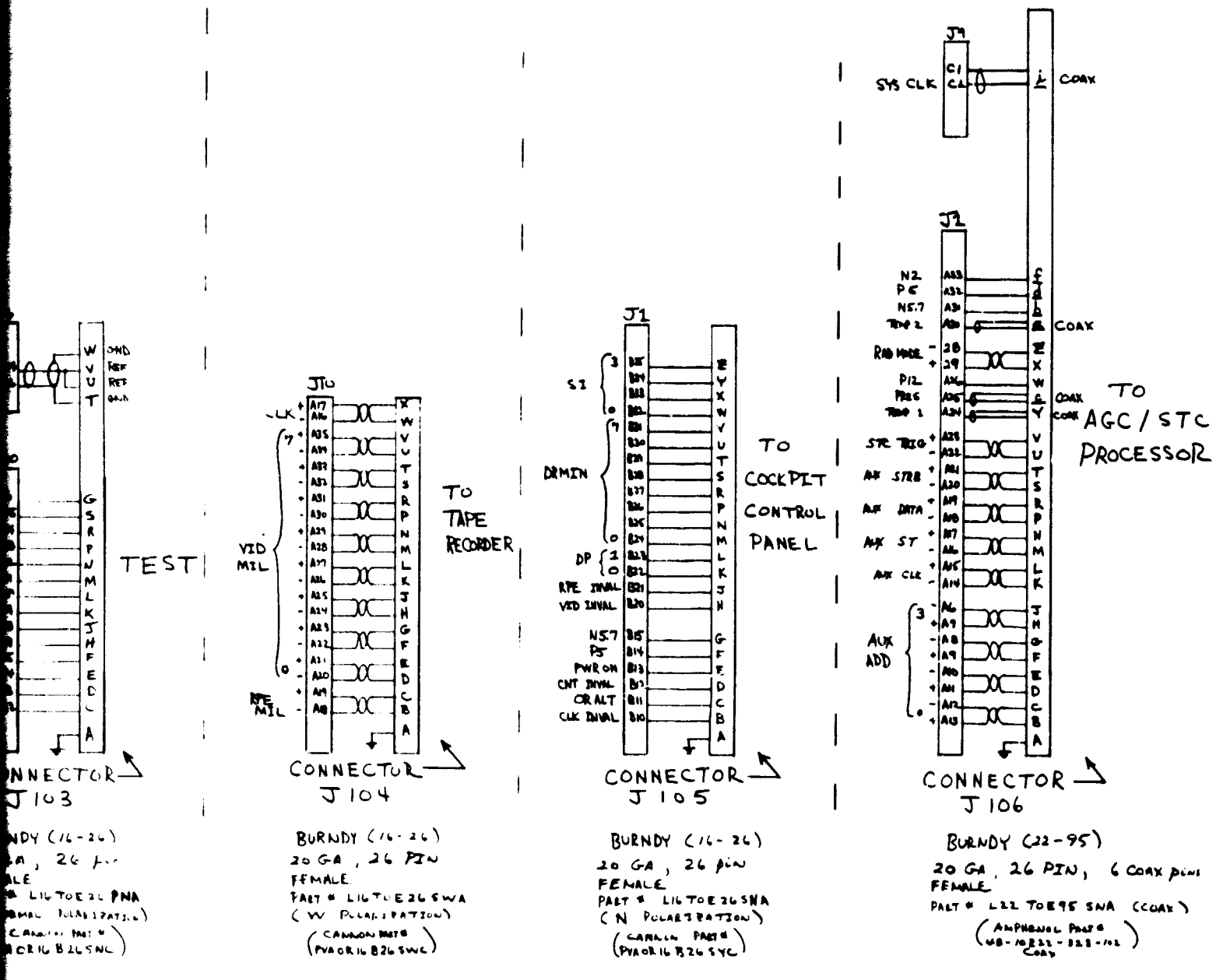

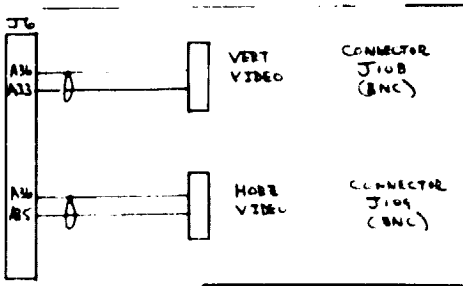

NOTE : DDRS CONNECTORS
TYPE – MINITURE CIRCULAR CONNECTORS
SHELL STYLE – (NARROW) SQUARE FLANGE
COUPLING – THREE LOCK BAYONET
CLASS & TERMINATION – CONDUCTIVE FINISH WITH ENVIRONMENT RESISTANT GROMMET WIRE SEAL
PINS – CRIMP TYPE

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DDRS SYSTEM BACK PANEL CONNECTORS

MATERIAL NAS9-15217-4

SIZE D
SCALE

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Drawing No 3

ROUGH FRAME 2

J3 in the backplane through the five ribbon cables (CAB 1 - CAB 5) and the plug connector (P3) which are mounted on the cable board (in slot 3).

Interconnections between the card cage and the enclosure back panel are made by ribbon cables (for digital signals) and by coaxial cable (for analog signals) as specified in Dwg. No. 3. Digital signals leave the card cage backplane from connectors J1 and J10, which are mounted in slots 1 and 10. Unlike the other backplane connectors, J1 and J10 have no circuit boards plugged into them, but serve merely to connect the ribbon cables from the cylindrical I/O connectors on the enclosure to the backplane wiring on the card cage.

2. Circuitry Description and Theory of Operation

a. Overview

The DDRS circuitry is partitioned into seven circuit boards, six of which are contained inside the main enclosure and one of which is in the AGC/STC processor unit. An effort was made to assign each circuit board a unique function, rather than randomly distribute the required system components among an arbitrary number of boards. Furthermore, the circuitry is composed of a very high speed section employing emitter coupled logic (ECL) and a medium speed section of transistor-transistor logic (TTL), each having very different requirements in terms of supply voltages and circuit layout. Finally, there simply was not enough room in the space allotted for the DDRS in the equipment pallet to fit in all the required circuitry and power supplies. So a seventh board (the auxiliary data board), containing all the components requiring ±15 V supplies, was fabricated to go in the AGC/STC processor unit, where ±15 V was already available.

The seven circuit boards perform the following functions:

Clock Generator Board (4-layer printed circuit - slot 9): Generates "clock" pulses which cause the radar video signals to be sampled

and digitized at a programmable frequency and with a programmable delay with respect to the STC trigger.

Phase locks the sample pulses to the 2.07065 MHz radar timing clock.

Provides detection of an out-of-lock condition in the phase lock loop.

Contains temperature and pressure sensors.

Video A/D board (4-layer printed circuit - slot 6): Converts the instantaneous horizontal and vertical video voltages into two digital data words, upon receipt of a sample pulse from the clock generator board.

Truncates the data words to a programmable number of bits (1, 2, 4, or 7) and steers the retained bits into the video memory to allow for packing of data words less than 8 bits long into 8-bit wide storage.

Adds an even parity bit to 7-bit data words.

Tests for overrange (clipping) of the video signals at the sampling times.

Provides a reference dc output to the test connector for testing purposes.

Video memory board (4-layer printed circuit - slot 4): Stores the video data words at the high sampling rates and reads them back out at the lower recording range.

Packs 4-, 2-, and 1-bit data into 8-bit words.

Multiplexes horizontal and vertical data words onto eight lines as they are read out of the memory.

Video formatting board (wirewrap - slot 11): Demultiplexes and formats the horizontal and vertical video data words from the video memory into eight channels of FLAMR-formatted serial data.

Miller-encodes the eight video channels and outputs them through differential line drivers to the wideband tape recorder.

Sets the 1.92 MHz recording clock rate.

Tests for activity on the video and RPE outputs to the tape recorder and alerts the operator in the case of an inoperative channel.

Radar parameters and environment (RPE) formatting board (wirewrap - slot 8): Commutates and formats data words from the UPPS, the auxiliary data board, and the cockpit control panel switches, as well as data words generated on the RPE formatting board, into a single FLAMR-formatted serial data stream.

Measures the interpulse period (IPP).

Generates frame numbers.

Tests the phaselock of the clock generator board and alerts the operator of loss of lock.

Counts the video memory parity errors.

Miller-encodes the RPE output data stream.

Interface board (wirewrap - slot 2): Converts ECL-level logic signals to TTL-level, and vice versa.

Receives differential TTL signals and ±5 V signals and converts them to single ended TTL.

Checks the cockpit control switch settings against a programmed set of valid settings and alerts the pilot if his settings are invalid.

Checks the parity of the video data as they are read out of the video memory.

Counts the number of A/D samples that were clipped.

Auxiliary data conversion board (wirewrap - inside the AGC/STC processor unit): Converts 16 channels of auxiliary analog information (temperatures, pressure, voltages, radar parameter signals) into 12-bit digital words.

Outputs the 12-bit words to the RPE formatting board to be formatted into the RPE data tape track.

Measures the temperature inside the AGC/STC processor unit.

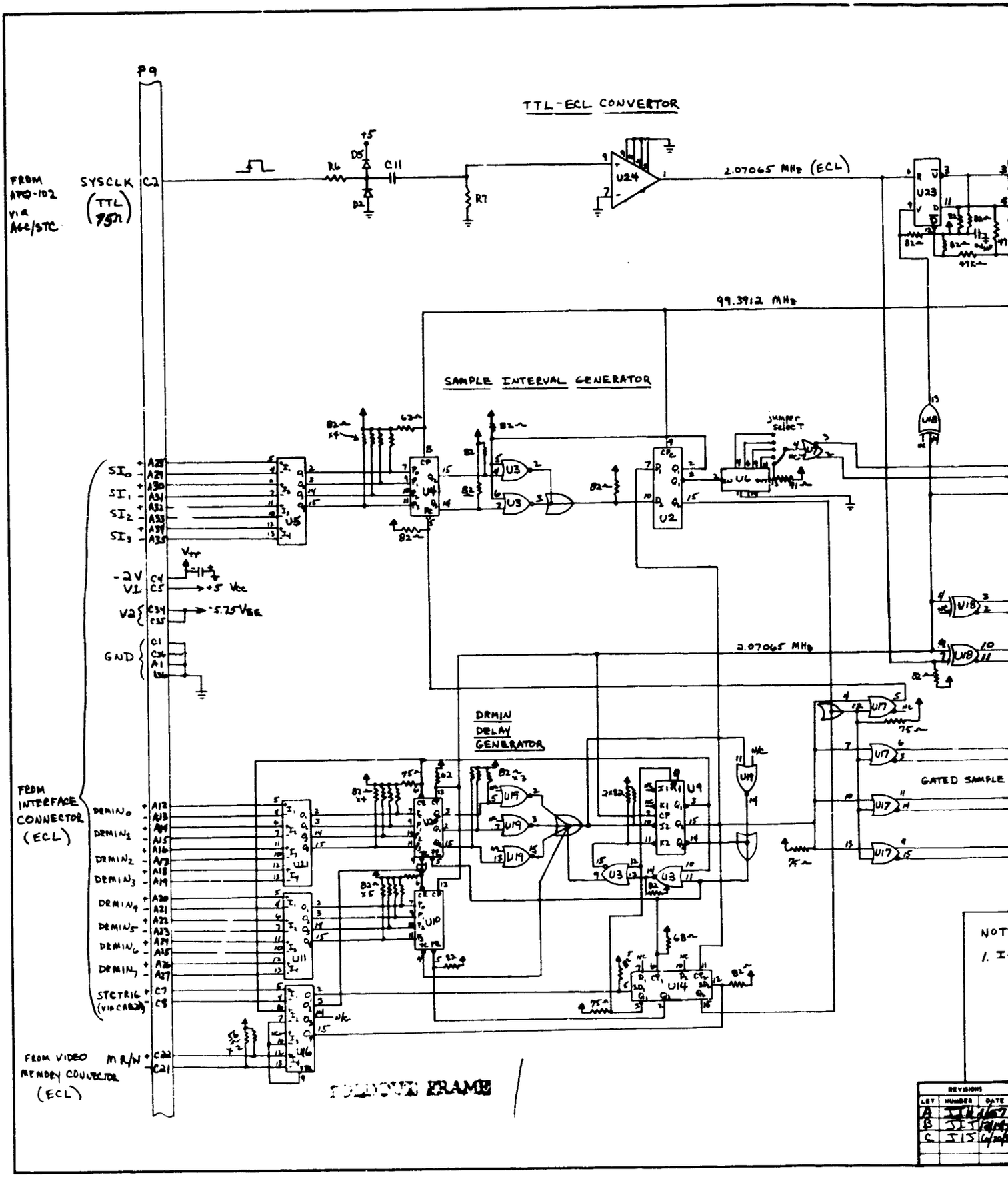
Buffers the STC trigger and radar mode output signals from the AGC/STC processor unit to the DDRS.

b. Detailed Board-by-Board Description

(1) Clock Generator Board (Dwg. No. 4)

The primary input to the clock generator board is the SYSCLK clock signal at 2.07065 MHz. This signal is clipped at +5 V and ground, and then converted to ECL levels by U24. ECL logic signals are described in Appendix D, Section 1.

The primary output of the circuit is the gated sample clock, the three identical copies of which are called GSCOR, GSCAD, and GSCMEM. Since this clock must be phase coherent with SYSCLK but at a much higher frequency, a coherent oscillator at 99.3912 MHz is employed which is phase locked to the 2.07065 MHz SYSCLK. U12 is an ECL oscillator; its


P9
TTL-ECL CONVERTOR
FROM APQ-102 VIA A6C/STC
SYSCLK (TTL 75Ω)
C2
D5
D2
C11
R6
R7
U24
2.07065 MHz (ECL)
U23
99.3912 MHz
SAMPLE INTERVAL GENERATOR
SI0 A28
SI1 A30
SI2 A32
SI3 A34
U5
U4
U3
U2
U6
JUMPER SELECT
-2V C4
V1 C5
+5 Vcc
V2 C34
C35
-5.75 VEE
GND C1 C36 A1 L36
2.07065 MHz
U8
U17
GATED SAMPLE
DRMIN DELAY GENERATOR
FROM INTERFACE CONNECTOR (ECL)
DRMIN0 A12
DRMIN1 A13
DRMIN2 A15
DRMIN3 A16
DRMIN4 A18
DRMIN5 A19
DRMIN6 A21
DRMIN7 A22
STCTRIG (VIDCARD) C7 C8
U10
U11
U12
U9
U14
U19
FROM VIDEO MEMORY CONNECTOR (ECL)
M R/W C22 C21
TIMING FRAME
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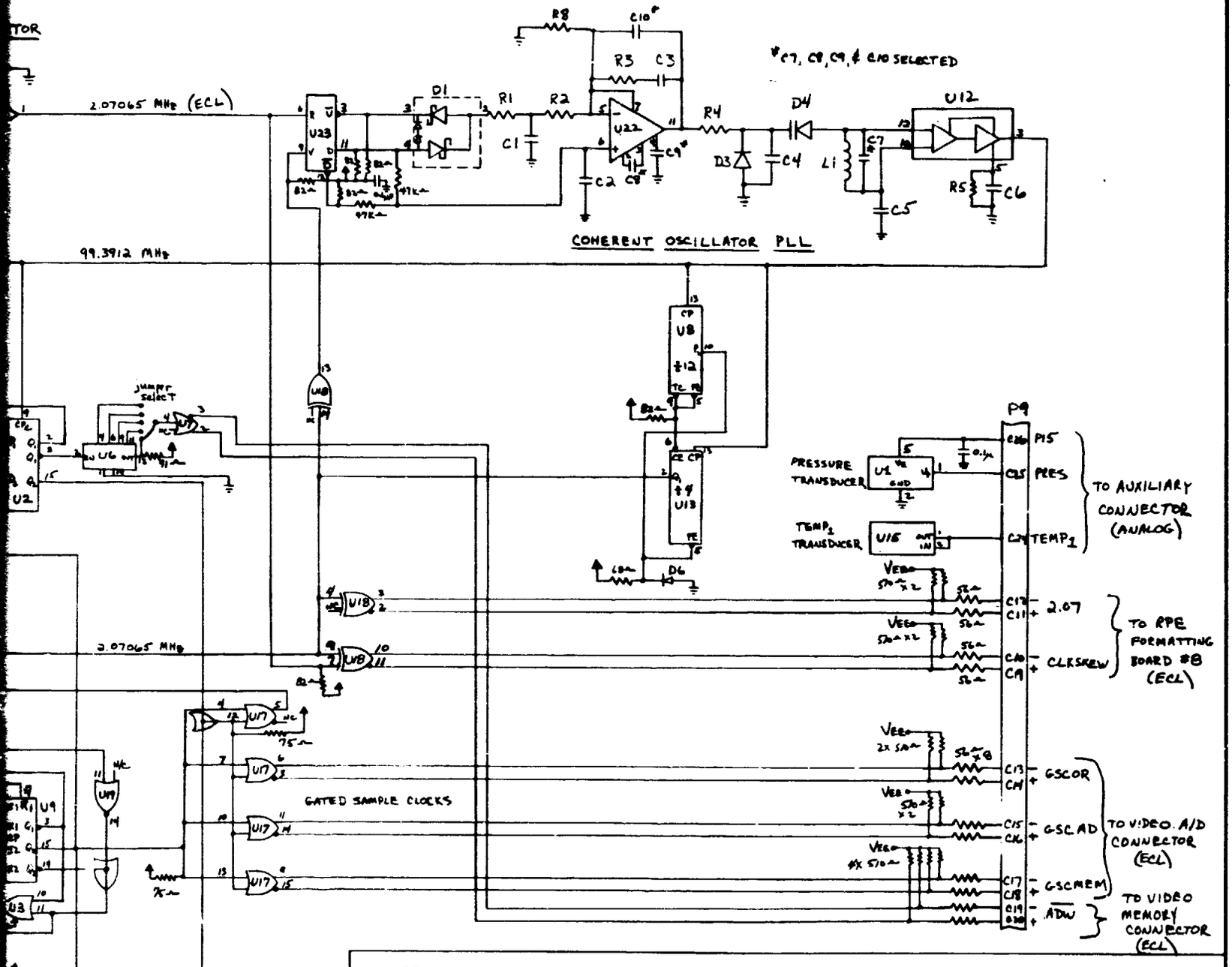

NOTES:

1. IC POWER PIN ASSIGNMENTS:

DIP NO.	+5V PIN	GND PIN	-5.2 PIN
U16	—	3	4
U23	—	1, 14	7
U12	—	1, 14	7, 8
U22	12	—	10
U24	11	3, 14	6
U2	—	2	—
U6	—	1, 16	—
ALL OTHERS	—	1, 16	8

2. POWER SUPPLY BYPASS CAPACITORS NOT SHOWN
3. CIRCUIT IS CONTAINED ON 7.5" X 9.5" PC BOARD
4. CONNECTOR P9 IS MURAC #3612056-01 72-PIN RIGHT ANGLE PLUG WITH SOLDER CONNECTORS.
5. CIRCUIT BOARD PLUGGED INTO SLOT 9 OF SYSTEM RACK AND CONNECTED TO J9 (#3612251-01 72-PIN RECEPTACLE) IN THE BACKPLANE.

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HEAT TREATMENT
NO REQD

CLOCK GENERATOR BOARD 9
MATERIAL NAS9-15217-4

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SCALE
D Drawing No 4

SCHEMATIC PLANE 2

frequency is established by the resonance frequency of L1 in parallel with C7 and the reverse junction capacitance of varactor diode D4. The output of U12 is a phase coherent 99.3912 MHz timing signal used to synthesize the sampling frequency. It is divided by 48 in U8 and U13 to produce a 2.07065 MHz square wave coherent in phase and frequency to SYSCLK. Phase comparator U23 compares the phase of the SYSCLK signal to that of the synthesized 2.07065 MHz square wave; any phase difference results in correction pulses at pins 3 and 11 of U23. These pulses either sink or source current through Schottky diode bridge D1 to the integrating circuit built around the high speed operational amplifier U22. The integrated correction pulses at the output of U22 are connected to the cathode of the varactor D4 in order to correct the output frequency by changing the capacitance of D4. This closes the loop and ensures phase coherence.

The phase lock loop natural frequency and damping factor are set by R1, R2, R3, and C3. Loop stability is improved by C1 and C4. C8, C9, and C10 frequency compensate the operational amplifier. R6 injects a small dc current into the integrator, which results in a small constant phase offset in the VCO output. It was found when integrating the DDRS with the noisy radar equipment in the pallet that external noise rejection was improved by this phase offset.

The sampling frequency is synthesized by the circuit composed of U2, U3, and U4. The output of U2 at pin 15 is a series of 20 nsec pulses, which is gated (by a wire OR connection) with U14, pin 15. The repetition frequency of these pulses is determined by the programmable counter U4, which divides the 99.3912 MHz coherent clock frequency by any integer from 4-15. The actual divisor integer is set by the logic levels on the programming inputs of the counter; these levels are in turn set by the position of the cockpit "sample interval" switch. The resulting sampling intervals available range from approximately 40 nsec (divide by 4, actually 40.2 nsec) through 150 nsec (divide by 15, actually 150.9 nsec) in 10 n sec intervals.

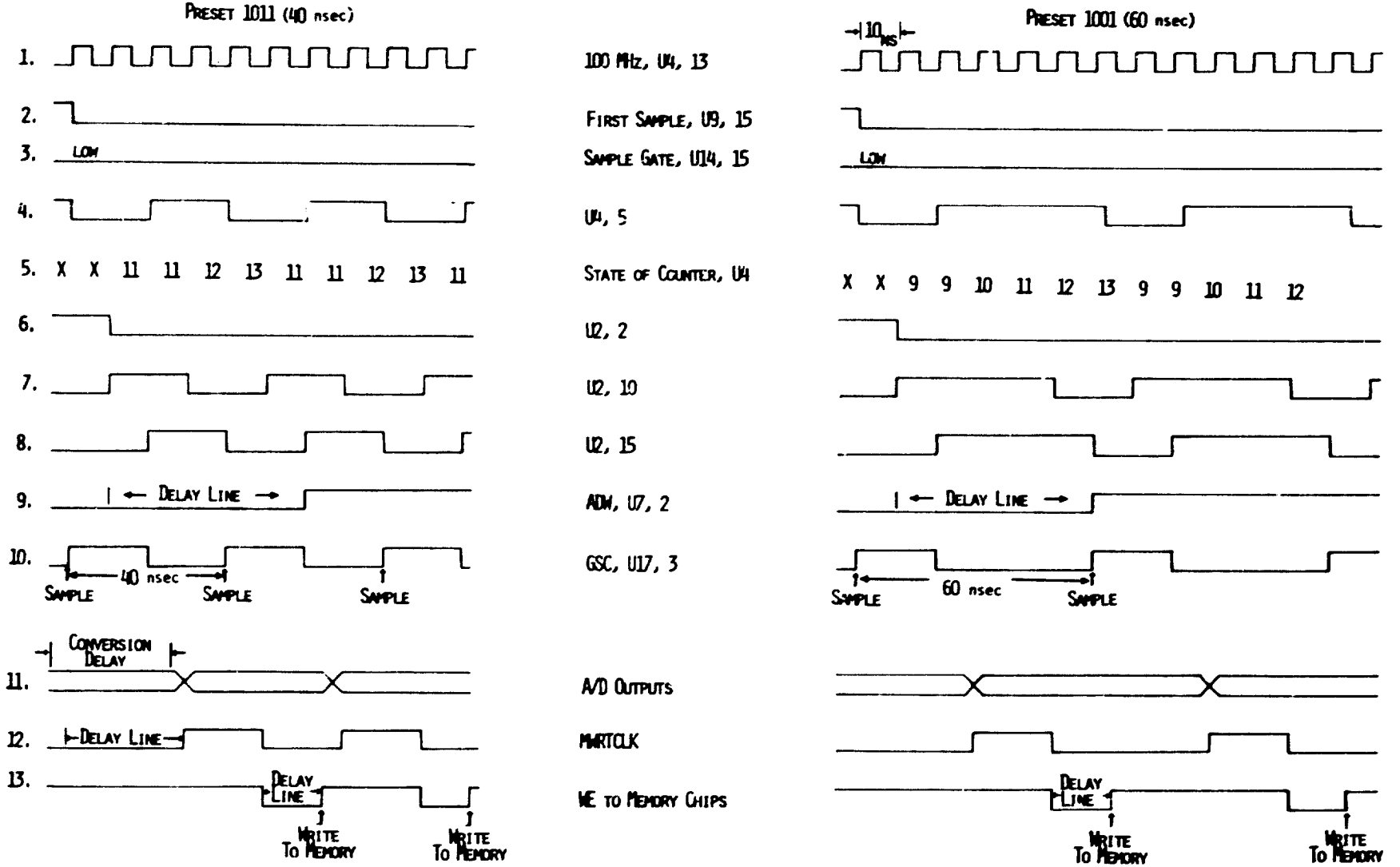
The circuit composed of U3, U9, U10, U14, U19, and U20 gates the output of the sampling frequency synthesizer. This circuit

is triggered out of its quiescent state by the STC trigger pulse (STCTRIG), which sets the left side of dual flip-flop U14. This enables the decimal counters U10 and U20 to begin counting up from their pre-set values, which are set by the cockpit DRMIN control switches. The clock input to these counters is the phase locked 2.07065 MHz clock, and their enable input is a 1.035325 MHz signal from U9, pin 3; therefore, the counters increment once every microsecond (actually once every 0.966 μsec). The pre-set values from the DRMIN cockpit control switches determine the number of counts (1 μsec per count) that the counters must increment before gating "on" the sampling interval generator. After the programmed DRMIN delay has passed since the STC trigger, pin 15 of U9 and pin 15 of U14 have gone false and the sampling clock pulses from pin 15 of U2 are gated through U17 to the video A/D board.

Once the sampling pulses are gated on, they continue until the buffer memory has been filled with one IPP's worth of digitized data. At this time, the video memory board sets the memory read/write (MR/W) line high. This signal sets the right half of flip-flop U14 on the clock generator board, which in turn gates off the sampling clock. At this time, the DRMIN delay circuit has returned to its quiescent state, and awaits the return of MR/W to a low state and the occurrence of the next STC trigger. The net effect of the circuit is to deliver sample pulses to the A/D board in each IPP from the time the DRMIN delay times out after the STC trigger, until the buffer memory is full.

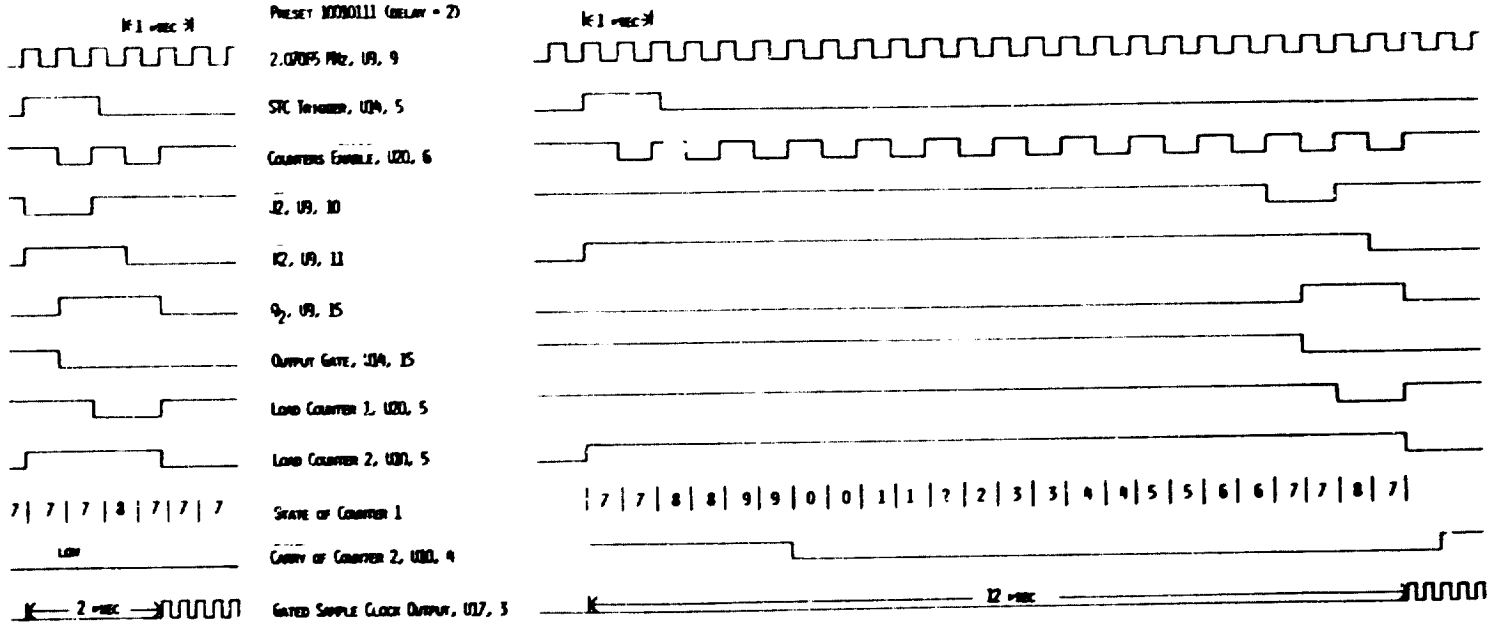
A detailed timing diagram of the sampling interval generator and DRMIN delay generator circuits is found in Figs. 10 and 11 which fully describe the operation of these circuits.

Included on the clock generator board are a pressure transducer and one of the three temperature transducers (TEMP 1) included in the DDRS. The transducer output is connected to the auxiliary data conversion board in the AGC/STC processor unit.



NOTE: WIRE-OR CONNECTIONS MAY ALTER THE APPEARANCE OF SOME OF THESE SIGNALS ON AN OSCILLOSCOPE. THIS IS A LOGICAL TIMING DIAGRAM, NOT AN ELECTRICAL ONE.

FIGURE 10
SAMPLE CLOCK TIMING



NOTE: WIRE OR CONNECTIONS MAY ALTER THE APPEARANCE OF SOME OF THESE SIGNALS ON AN OSCILLOSCOPE. THIS IS A LOGICAL TIMING DIAGRAM, NOT AN ELECTRICAL ONE.

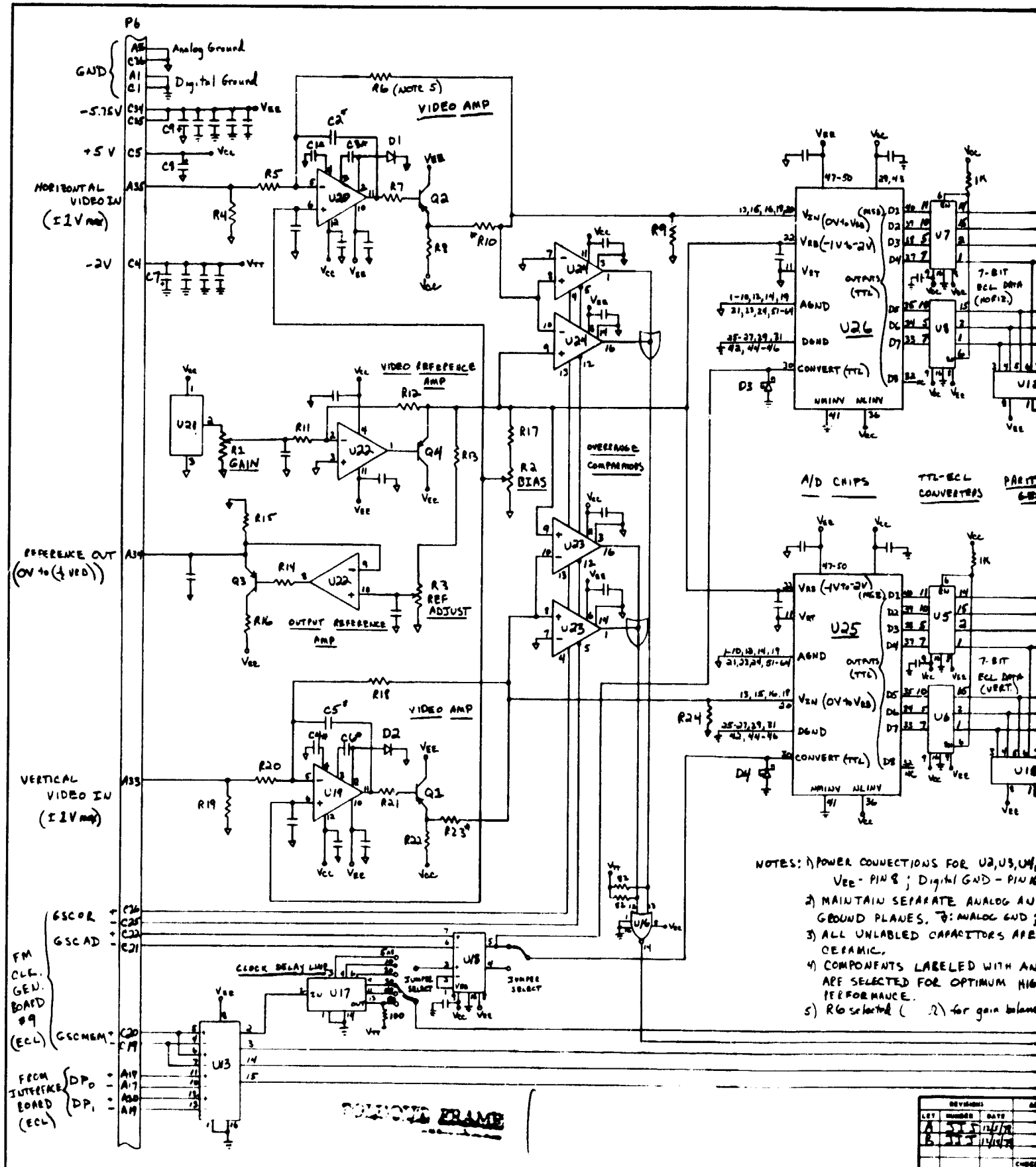
FIGURE 11
DRMIN TIMING
(CLOCK GENERATOR BOARD 9)

(2) Video A/D Board (Dwg. No. 5)

The primary inputs to the video A/D board are the two video channels and the three (identical) sampling clocks. The outputs are two channels of quantized video data, a memory write signal, and an overrange count signal.

The heart of the A/D board is the TRW 1007 8-bit, 33 MHz A/D converter integrated circuit (U25 and U26). The limits on the input voltage the chip can quantize are the potential at pin 11 (V RT) on the positive end and the potential at pin 22 (V RB) on the negative end. This voltage range is divided into 256 discrete subranges, to which the chip assigns consecutive 8-bit digital numbers. The most positive voltage (V RT) must be set to ground potential; the most negative voltage (V RB) may be set to between -1 V and -2 V. The A/D conversion is triggered by a TTL level pulse at pin 30 (CONVERT). The output words are TTL level, and one of four different digital encoding schemes may be selected by appropriate TTL levels on pins 36 (NL/NV) and 41 (NM/NV).

The horizontal and vertical video inputs to the video A/D board are bipolar signals of approximately 1 V pp, i.e., ±0.5 V. Video amplifiers U19 and U20 invert the video signals (voltage gain = -1) and offset them by an adjustable voltage (currently set at -0.5 V). The outputs of the video amplifiers have a voltage range of 0 to -1 V with a ±5 V input and feed into the analog inputs of the two TRW 1007 chips (one chip for horizontal video and one for vertical). The negative full-scale voltage level at pins 22 of the chips is set by the gain adjustment potentiometer R1, which in conjunction with 2.5 V reference source U21 and voltage inverter U22A, effectively sets the A/D gain of the DDRS. If the video signals turn out to actually be, e.g., 2 V pp, R1 may be adjusted to set negative full scale at -2 V (as measured at the A/D chip, not at the video input; full scale at the input would in this case be ±1 V). The bias (offset) of the video amplifier outputs is adjusted by R2, which varies the voltage at the noninverting inputs of the amplifiers from 0 to one-half the reference voltage. It is normally set at one-fourth the



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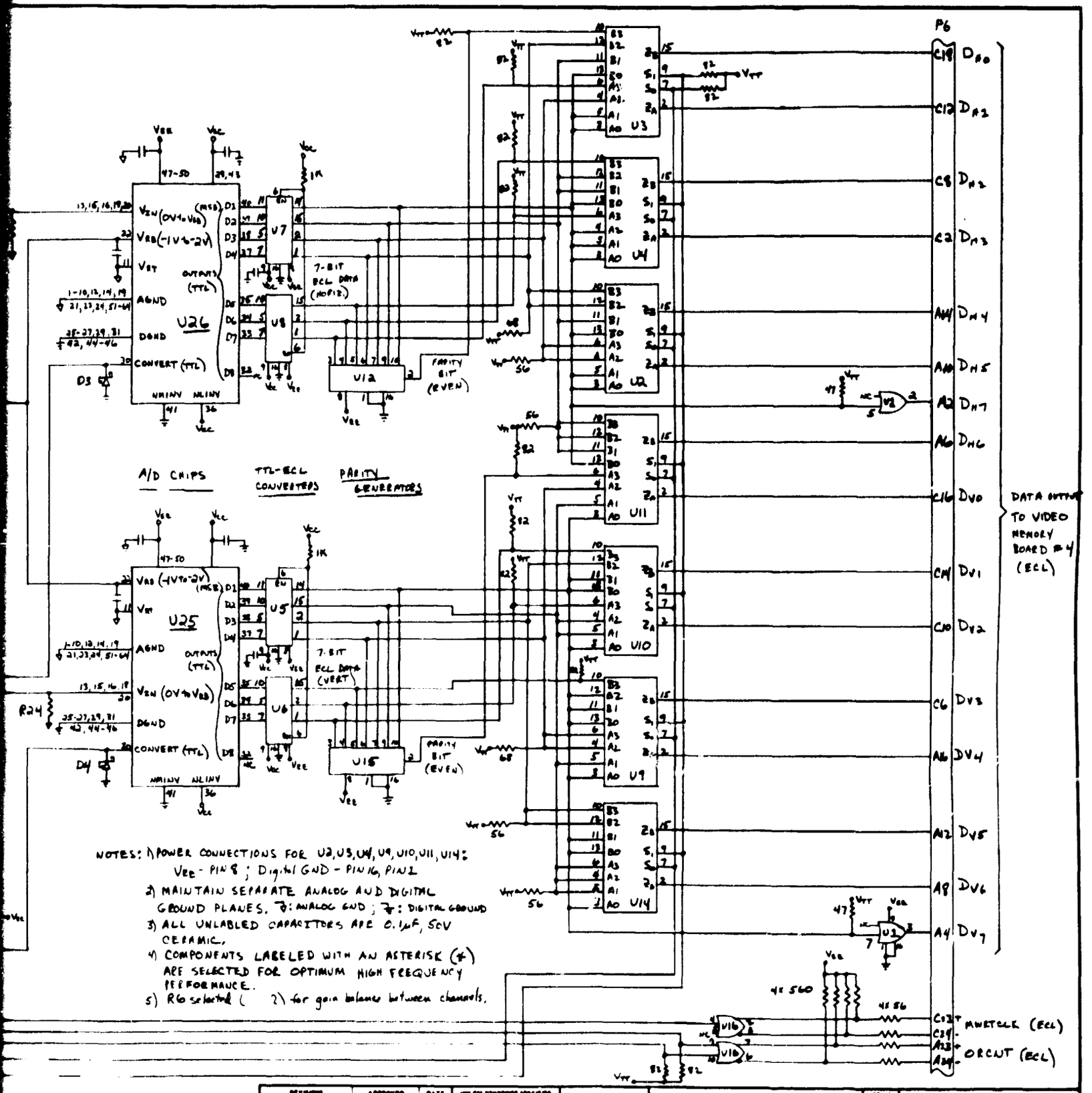

A/D CHIPS
TTL-ECL CONVERTERS
PARITY GENERATORS
U26
U25
U7
U8
U5
U6
U12
U15
U3
U4
U2
U11
U10
U9
U14
7-BIT ECL DATA (HORIZ)
7-BIT ECL DATA (VERT)
PARITY BIT (EVEN)
P6
DATA OUTPUT TO VIDEO MEMORY BOARD #4 (ECL)
NOTES: 1) POWER CONNECTIONS FOR U2, U3, U4, U9, U10, U11, U14: Vee - PIN 8 ; Digital GND - PIN 16, PIN 1
2) MAINTAIN SEPARATE ANALOG AND DIGITAL GROUND PLANES. ⏚: ANALOG GND ; ⏚: DIGITAL GROUND
3) ALL UNLABLED CAPACITORS ARE 0.1μF, 50V CERAMIC.
4) COMPONENTS LABELED WITH AN ASTERISK (*) ARE SELECTED FOR OPTIMUM HIGH FREQUENCY PERFORMANCE.
5) R6 selected ( ) for gain balance between channels.
VIDEO A/D BOARD #6
MATERIAL NAS9-15017-4
APPLIED RESEARCH LABORATORIES
D Drawing No 5

reference voltage; as a result, a grounded video input translates into a one-half full scale voltage at the analog input of the TRW chip. This results in a digital "zero" on the TRW output. In case of an unwanted dc offset in the video signals, this potentiometer may be adjusted to compensate. Since the bias voltage tracks the reference voltage, adjustment of the gain control will not alter the effective bias setting.

Overrange voltage comparator IC's U23 and U24 produce a positive ECL level when the video inputs to the TRW chips exceed the positive or negative full scale levels. These levels are latched by the sampling clock (GSCOR) inside the comparators and are gated with the sampling clock (GSCMEM) to create a sample signal of one pulse per overrange (ORCNT).

A clock delay line, U17, is included to allow timing adjustments of the sampling clock. Provision is made for two jumper selectable delays: one allows the memory write clock (MWRTCLK) to be delayed in order to compensate for propagation delay from the rising edge of the sample clock to the presentation of data to the memory board; the other allows the sample clock to U25 to be delayed with respect to the sample clock to U26, to compensate for different propagation delays through the two TRW chips. The setting of these timing adjustments will be discussed in Sec. IV.

All logic signals to the TRW A/D chips are TTL level. U5, U6, U7, U8, and U18 perform ECL to TTL and TTL to ECL conversions. Separate ground planes are maintained on the board; the analog ground plane is ground for all analog components, while the digital ground plane is ground for all digital components. The two grounds are connected on the backplane where the video A/D board plugs in.

The output code selected by the NMINV and NLINV lines on the TRW chips is positive-true 2's complement:

DDRS VIDEO INPUT	A/D CHIP DIGITAL CODE
	MSB LSB
+ full-scale:	01111111
+ one-step:	00000001
zero:	00000000
- one-step:	11111111
- full-scale:	10000000

The least significant bit (LSB) of this code is dropped by U12 and U15 and replaced by an even parity bit.

According to the data precision selected, each data word from the A/D's and parity generators is truncated and has its individual bits steered to the proper buffer memory chip by multiplexers U2, U3, U4, U11, and U9, U10, U11, U14. The following data patterns are output to the video memory board on lines D_{V0}-D_{V7} (and D_{H0}-D_{H7}):

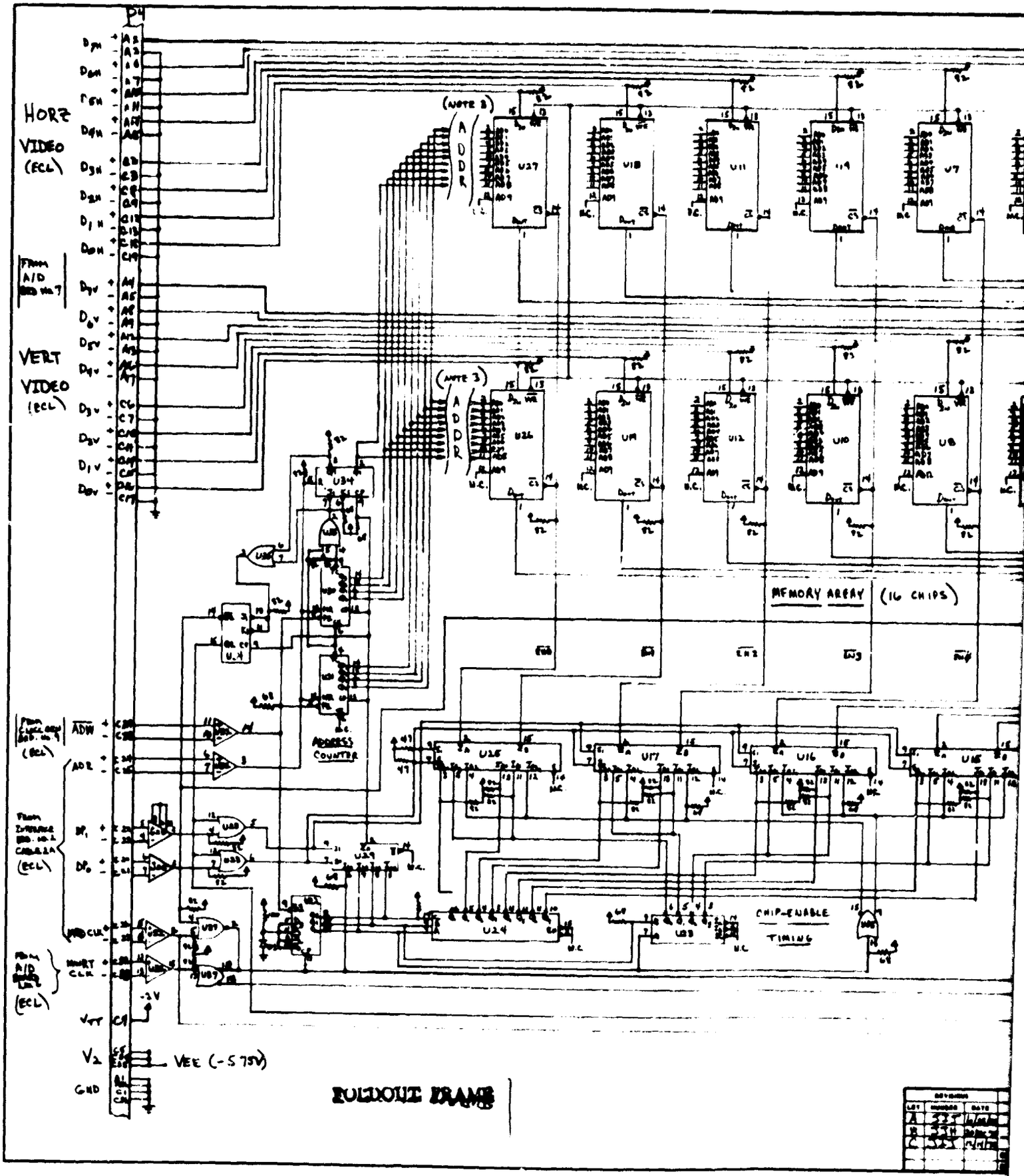
Data Precision	D_{V7}	D_{V6}	D_{V5}	D_{V4}	D_{V3}	D_{V2}	D_{V1}	D_{V0}
7 bit	D_1	D_2	D_3	D_4	D_5	D_6	D_7	P
4 bit	D_1	D_2	D_3	D_4	D_1	D_2	D_3	D_4
2 bit	D_1	D_2	D_1	D_2	D_1	D_2	D_1	D_2
1 bit	D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1

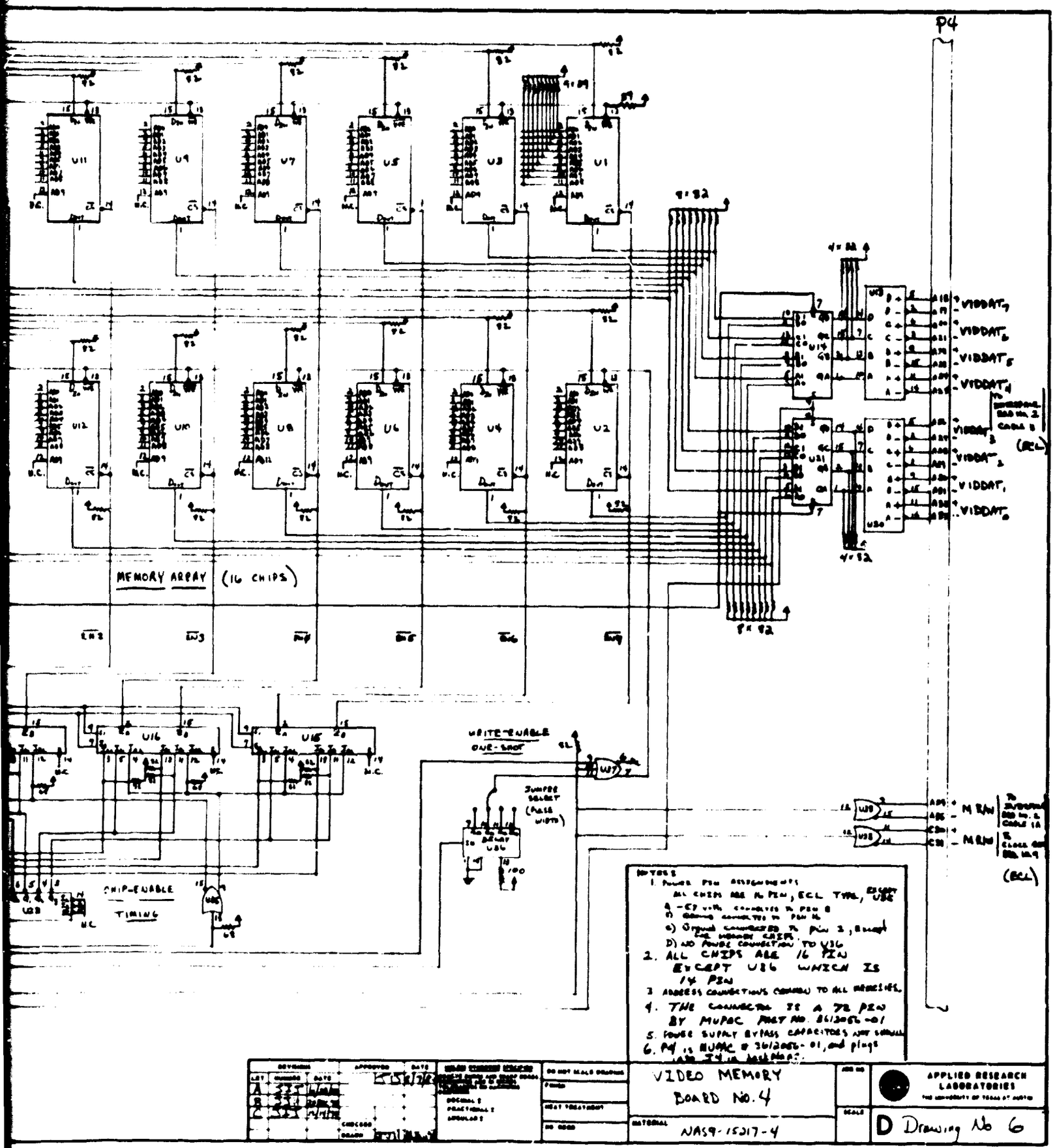
Notes: D_1(MSB)-D_7 refer to outputs from the TRW A/D chip.
P is the parity bit.

As shown above, only 7-bit data words contain a parity bit.

(3) Video Memory Board (Dwg. No. 6)

The data patterns from the video A/D board are temporarily stored in 1024 by 1-bit random access memory (RAM) IC's on the video memory board. Separate write clock and read clock inputs are provided on the board so that the data in the memories may be read out at a slower rate than they are written in. The board produces a key


HORZ VIDEO (ECL)
VERT VIDEO (ECL)
MEMORY ARRAY (16 CHIPS)
ADDRESS COUNTER
CHIP-ENABLE TIMING
VEE (-5.75V)
FOLDOUT FRAME



51

FULLOUT FRAME

control signal, MR/W, which sets the DDRS in either the acquire-data state or the record-data state.

When DRMIN times out after the STC trigger, the clock generator board begins sending sampling pulses to the A/D board. These pulses are delayed on the A/D board (to allow the digitized video samples to propagate through the A/D board) and sent to the video memory board as a memory write clock (MWRTCLK). The pulses are 20 nsec wide and positive going. The rising edge of each pulse is used to clock the address counter composed of U30, U31, and U34; the falling edge triggers the write-enable one-shot composed of U36 and U37. The address counter increments from 0 to 511 and drives the address lines of the RAM; note that only the first 512 (out of 1024 total) locations in the RAM chips are used. The write-enable one-shot generates a negative going pulse to the write-enable input of each RAM chip when triggered. The width of this pulse is set by tapped delay line U36 and can be set to 12, 14, 16, or 18 nsec. The 20 nsec between the rising and falling edges of the write clock pulse allows the address lines to the RAM chips to settle at least 5 nsec before the write-enable pulse arrives, as specified by the RAM data sheet (Fairchild 10415A).

Each RAM chip has an enable input which must be brought low for data to be written or read. This input is used to control the number of parallel data bits that are written for each A/D sample, which depends on the data precision requested. For 7-bit data plus parity, eight parallel bits are required and all enable lines ($\overline{EN}_7$ - $\overline{EN}_0$) to each 8-bit wide memory bank are brought low. For 4-bit data, first $\overline{EN}_7$ - $\overline{EN}_4$ are brought low, then $\overline{EN}_3$ - $\overline{EN}_0$ are brought low, and then the address lines are incremented for the next two 4-bit data words. Similarly, for 1-bit data, each enable line is sequentially pulsed low, beginning with $\overline{EN}_7$ and ending with $\overline{EN}_0$, and after all eight enables have been pulsed, the address lines increment for the next round of eight samples. Changes on the enable lines are triggered by the rising edge of MWRTCLK, and all enable lines are stable by the time the write-enable pulse occurs. The chip-enable logic consists of U15, U16, U17, U22, U23, U24, and U25.

Since the address lines must change after every video sample in the 7-bit mode but only after every two, four, or eight samples in the 4-, 2-, and 1-bit modes, respectively, the clock frequency to the address counter must be changed with changes in the data precision. Multiplexer U29 selects the full frequency MWRTCLK or else divided-down frequencies, depending on the state of the data precision (DP_0, DP_1) lines, and outputs the clock signal to the address counter. The data precision lines are coded as follows:

DP_0	DP_1	Data Precision
0	0	1 bit
1	0	2 bit
0	1	4 bit
1	1	7 bit with parity

After the address counter has reached a count of 511, the next rising edge of the clock signal resets the counter to zero and toggles flip-flop U34 at pins 14 and 15. The state of this flip-flop determines whether the memory is in the read or the write mode. U34, pin 15, is the memory read write (MR/W) signal: true means read; false means write. A transition from read to write sets the clock generator board into a quiescent state, waiting for an STC trigger. A transition from write to read starts the video formatting board to immediately begin reading data from the memory.

When the memory is in the read mode, the data precision signals (DP_0 and DP_1) are gated true (at U33, pins 5 and 6) so that the memory reads out eight bits at a time. The memory read clock (MRDCLK)) is gated on, and the write-enable one-shot (U37, pin 7) is gated off (true). The memory write clock (MWRTCLK) is gated off on the clock generator board. The net result is that the stored memory words are read out by MRDCLK. During this time, the 8-bit output of each memory bank is multiplexed by U14 and U21 onto eight lines ($VIDDAT_0$-$VIDDAT_7$) to the video formatting board. The multiplexers are controlled by MRDCLK: when MRDCLK is low, the horizontal video memory data appear on the VIDDAT lines;

when MRDCLK is high, the vertical video memory data appear. Figure 12 illustrates the memory read timing.

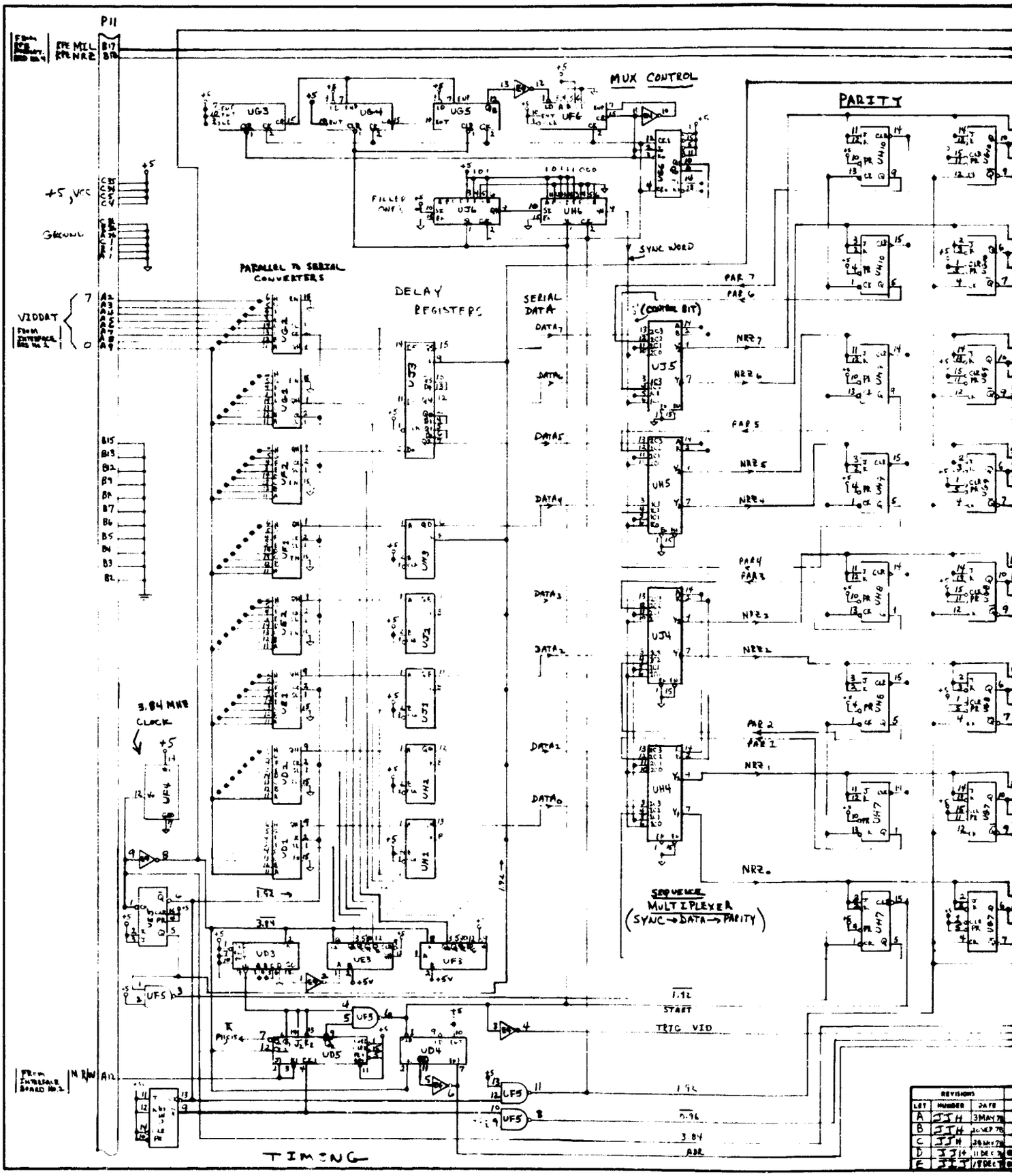
(4) Video Formatting Board (Dwg. No. 7)

The detailed timing and operation of the video formatting board is fully described in Fig. 12. A general summary of the board's functions will be given here.

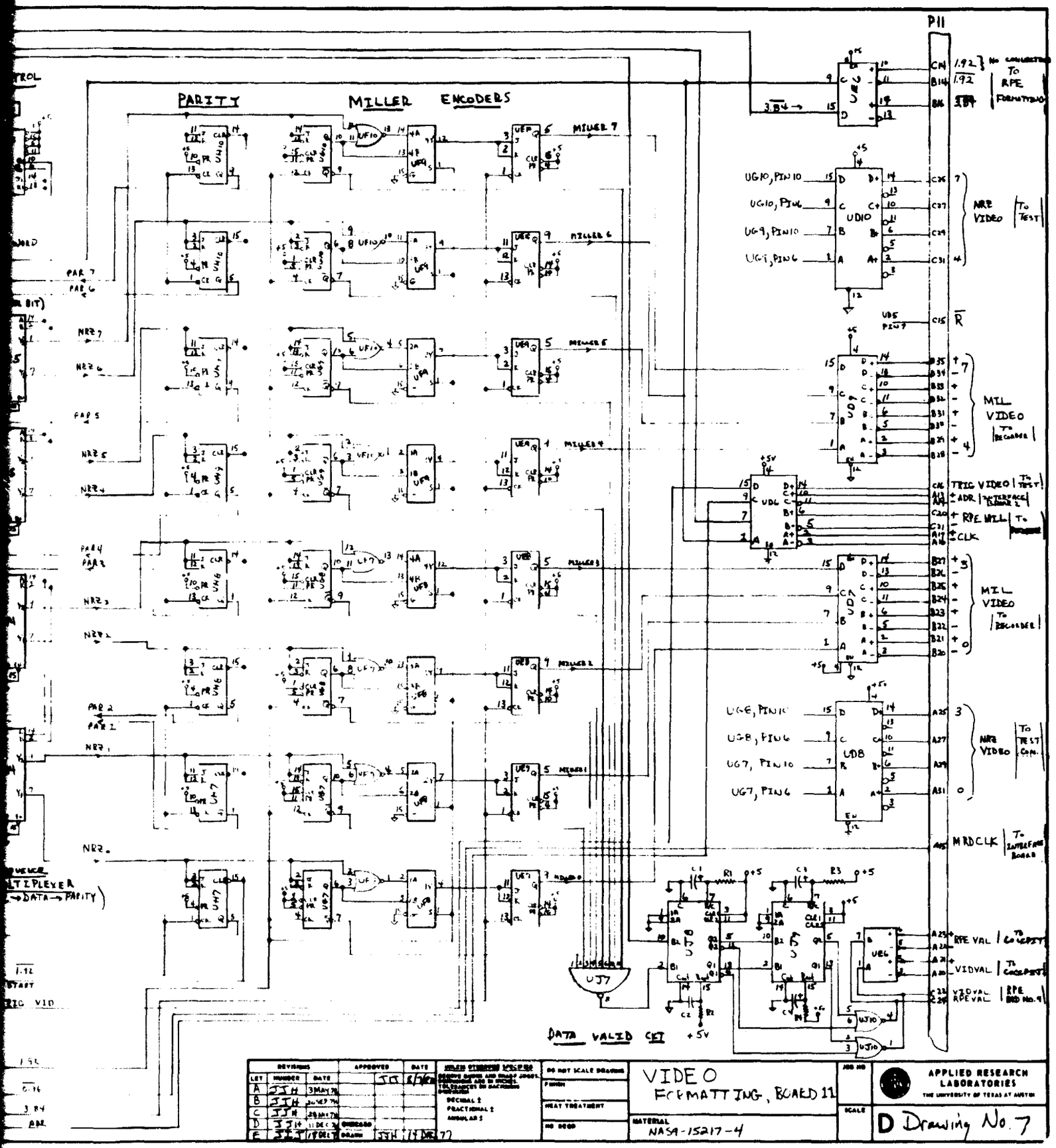
The rising edge of MR/W, signifying that the buffer memory is full and ready to be read, triggers the video formatting circuitry from its quiescent state. This rising edge is synchronous with the sampling clock and, therefore, asynchronous with the 3.84 MHz timing clock in the video formatting board. Flip-flop VD5 synchronizes the rising edge of MR/W, loads the sync word into shift register UH5, and starts it clocking out the sequence multiplexers (UH4, UH5, UJ4, UJ5) to the Miller encoders at 1.92 MHz. Meanwhile, signal ADR clears the address counters in the video memory board for two MRDCLK cycles. Then the parallel-to-serial converting shift registers (VD1, VD2, UE1, UE2, UF1, UF2, UG1, UG2) begin loading data from the memory board. UD1 loads first; its first data word is the first sample of the horizontal video. UG2 loads last; its first data word is the fourth sample of the vertical video.

The outputs of the parallel-to-serial converters are differentially delayed by registers UH1, UH2, UH3, UJ1, UJ2, and UJ3. This ensures that the serial data lines ($DATA_0$-$DATA_7$) are bit parallel, i.e., the first bit of each data word emerges from the delay registers at the same time. Note that the parallel-to-serial converters are loaded such that the most significant bit ($VIDDAT_7$) of a memory data word is shifted out first.

After the sync word has passed through the sequence multiplexers, the multiplexer control lines change state and gate the FLAMR format control bit through the multiplexers. This bit is wired true. One bit time later, the controls again change state and gate the



EQUINOX FRAME



FOLDOUT FRAME 2 FOLDOUT 5.4

INTENTIONALLY BLANK

data lines from the delay registers through to the Miller encoders. At this time, the first bit of each of the first eight data words has appeared at the delay register outputs. 128 words (1024 bits) of data are clocked through the multiplexers at 1.92 Mbs and are counted by the MUX control circuitry (UG3, UG4, UG5), after which the control lines to the multiplexers again change state. Now the outputs of the parity accumulator flip-flops (UH7, UH8, UH9, UH10) are allowed through to the Miller encoders for 1-bit time. After this 1-bit time, the sync word shift register is again gated through the multiplexer; the output of this register (UH6, pin 9) remains true until the sync word is loaded on the next rising edge of MR/W. Thus, the interrecord gap on the wideband tape contains a series of filler ones.

Included on the video formatting board is a data validation circuit (UJ7, UJ8, UJ9, UJ10). This circuit tests for activity on the video and RPE output data lines before Miller encoding. Retriggerable one-shot UJ8 will normally remain constantly triggered. If, however, there is no activity on either the video data lines for approximately 6.6 msec or on the RPE data lines for 81 msec, then the one-shot outputs will go false, and the respective signals VIDINVAL or RPEINVAL to the cockpit will go true. One-shot UJ9 is included to catch short dropouts from UJ8 and stretch them into 1 sec pulses to the cockpit.

(5) RPE Formatting Board (Dwg. No. 8)

Operation of the RPE formatting board is controlled by the program counter (UF9, UF10) in conjunction with the control PROM (UE10). The program counter counts from 0 to 31; accordingly, there are 32 possible RPE data sources. Currently, only 30 of these possible sources are recorded; these are shown in line 9 in the timing diagram, Fig. 13. Timing for the entire board is described in this figure.

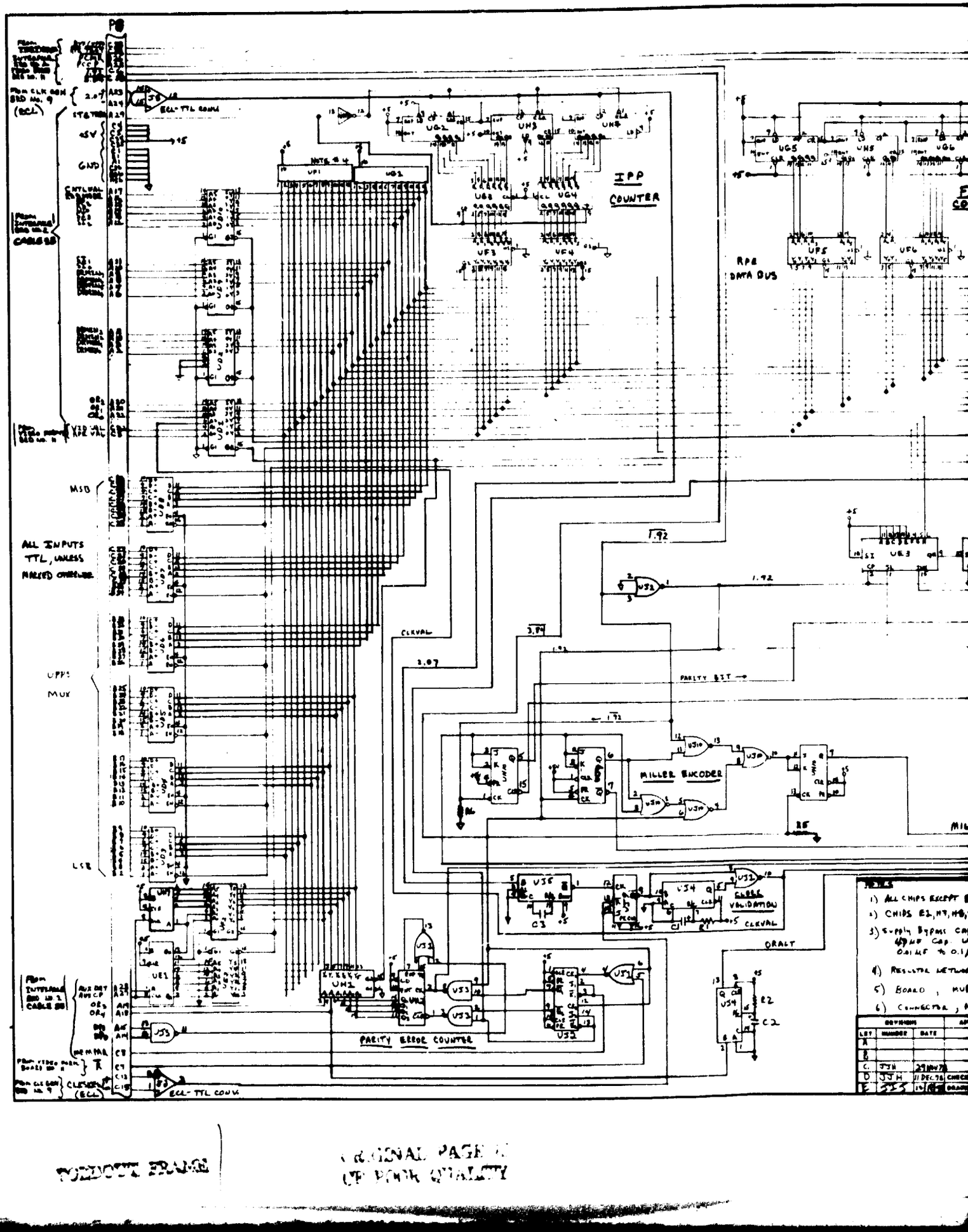
The primary control signals to the board are PCMR and PCCP (lines 2 and 3 of Fig. 13). PCMR, which is the (inverted) strobe signal from the UPPS corresponding to time-of-day, resets the counter to

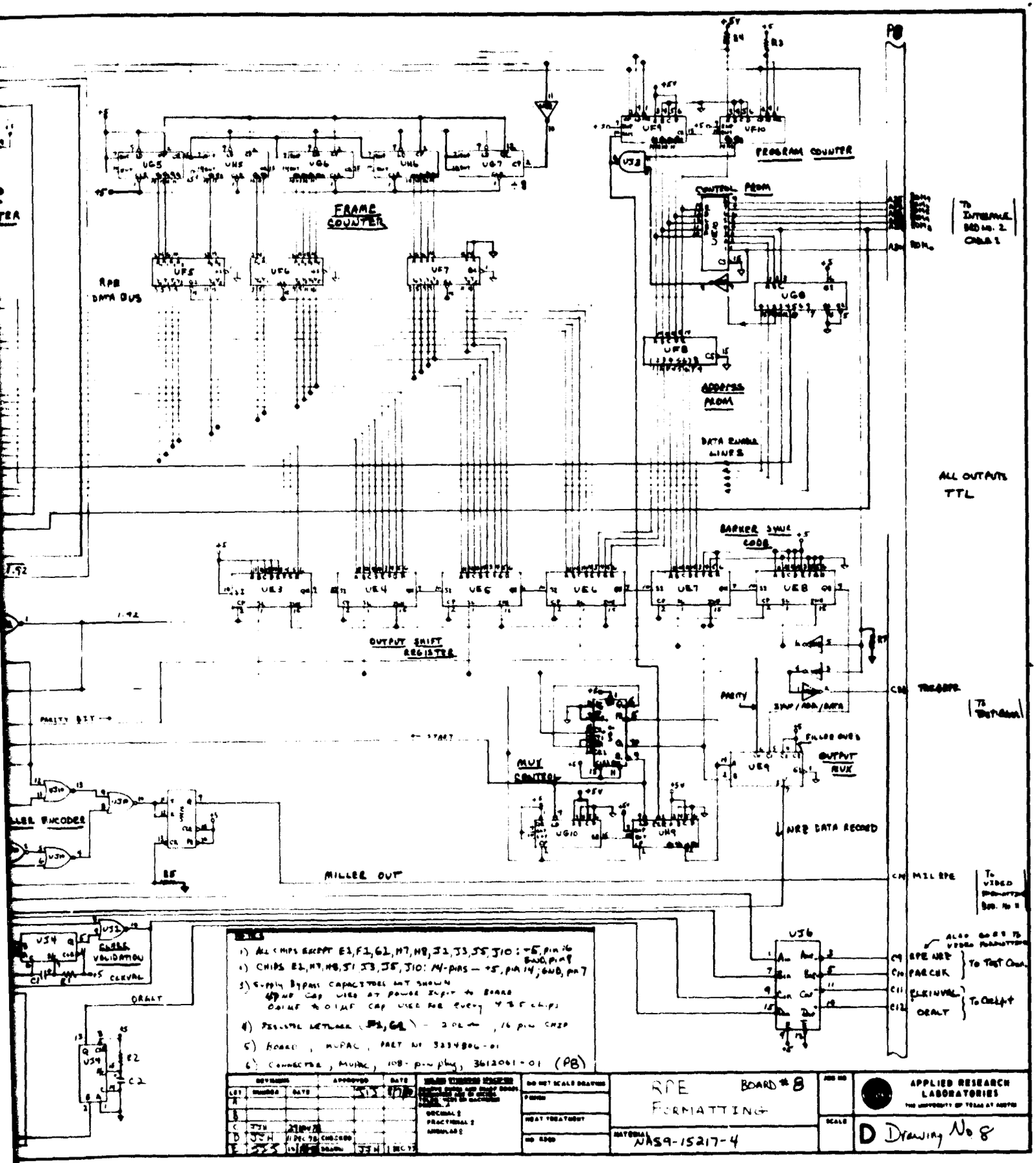
zero, which initiates the RPE output cycle and accesses the first memory location in the control PROM. The control PROM is programmed as shown in Table IV. Bits 2, 3, and 4 of the PROM output determine the source of the data on the RPE data bus. For the first eleven locations, these bits are all zeroes which, when decoded by UG8, select the UPPS data bus driver (UD3, UD4, UD5, UD6, UD7, UD8). Thus, the first eleven RPE records after a PCMR pulse contain NERDAS data.

Bit 0 of the control PROM output selects either the UPPS strobe or a DDRS internal 15 kHz clock as source of the program counter clock, PCCP. The first eleven PCCP pulses are from the UPPS strobe. While the rising edge of PCCP increments the program counter, the falling edge initiates the output of an RPE data record by enabling the output shift register (UE3, UE4, UE5, UE6, UE7, UE8) to begin shifting the record out. The PCCP rising edge also resets both halves of flip-flop UG9, which commands the output multiplexer (UE9) to gate the data record through to the Miller encoder (UJ9, UJ10, UH11). After 43 bits (11 bits sync, 8 bits address, 24 bits data) have been shifted out of the output shift register, pin 12 of counter UH9 goes false, which causes the record parity bit (even parity) to be gated through the output multiplexer for 1-bit time. At this time, flip-flop UG9 is set, which gates a high level through the multiplexer (interrecord filler one's) until the next rising edge of PCCP.

The contents of each data record are latched into the parallel inputs of the output shift register on the rising edge of PCCP. The first eleven bits are hard-wired as the sync code 00011101101. The next eight bits are the output of the address PROM (UF8). This PROM is programmed as shown in Table IV. The addresses are chosen according to the following criteria:

(a) Parameters most useful during playback and CCT conversion are given the addresses of data which are displayed on the DRIE (at ARL:UT). These parameters are:




FRAME COUNTER
PROGRAM COUNTER
CONTROL PROM
ADDRESS PROM
RPB DATA BUS
DATA ENABLE LINES
ALL OUTPUTS TTL
BARKER 3 VALUE CODE
OUTPUT SHIFT REGISTER
PARITY
MUX CONTROL
OUTPUT MUX
NRZ DATA RECORD
MILLER OUT
MILLER ENCODER
CLOCK VALIDATION
To INTERFACE BD NO. 2 CABLE 1
To TEST CABLE
To VIDEO FORMATTER BD. NO. 11
To CLOCK
RPE FORMATTING
BOARD # 8
MATERIAL NAS9-15217-4
APPLIED RESEARCH LABORATORIES
D Drawing No 8

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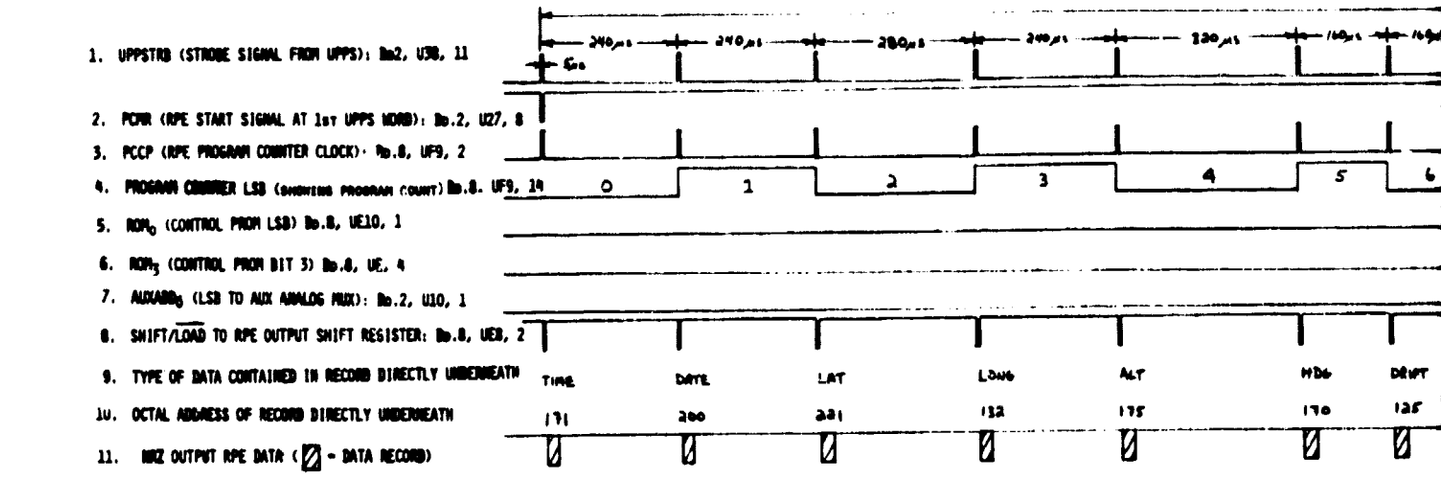
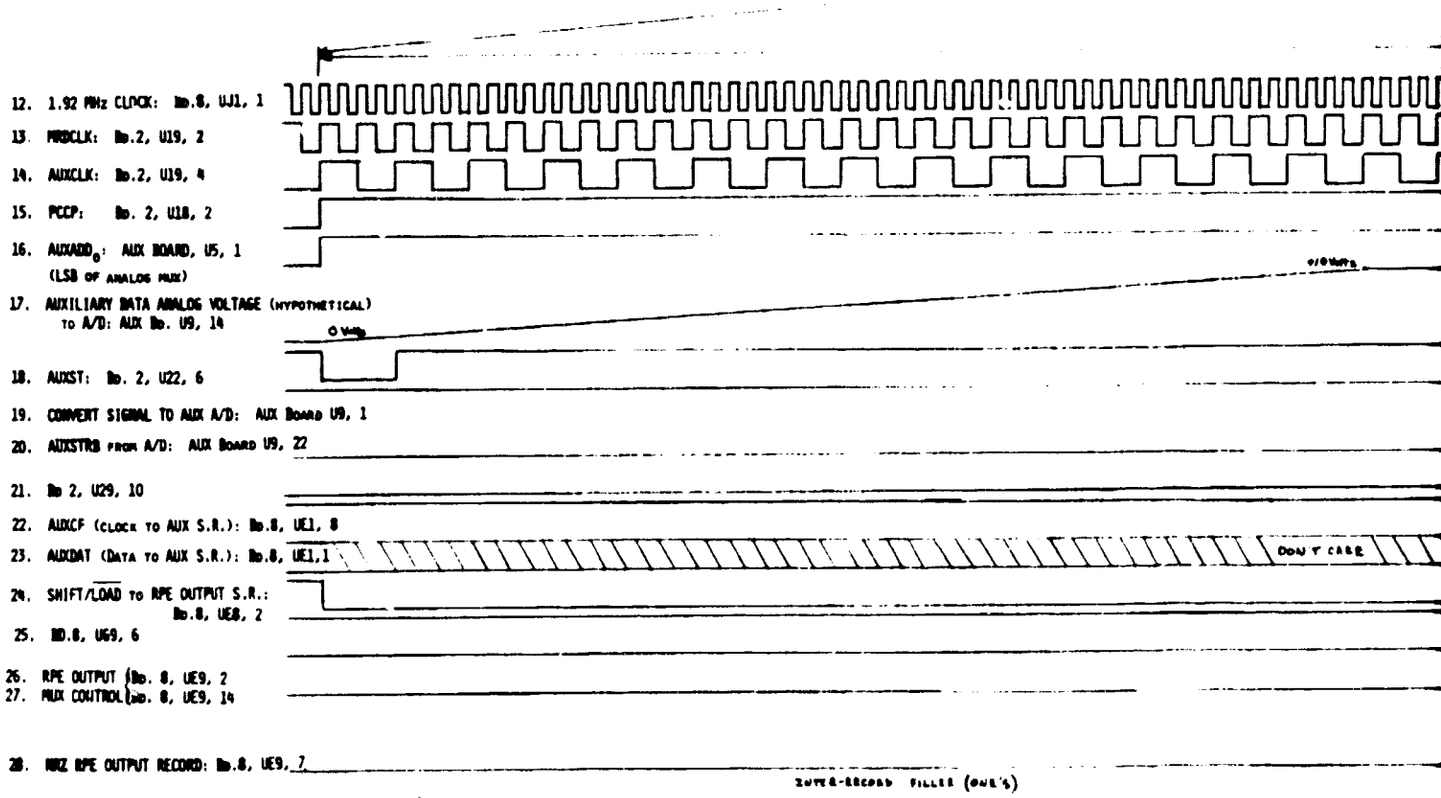




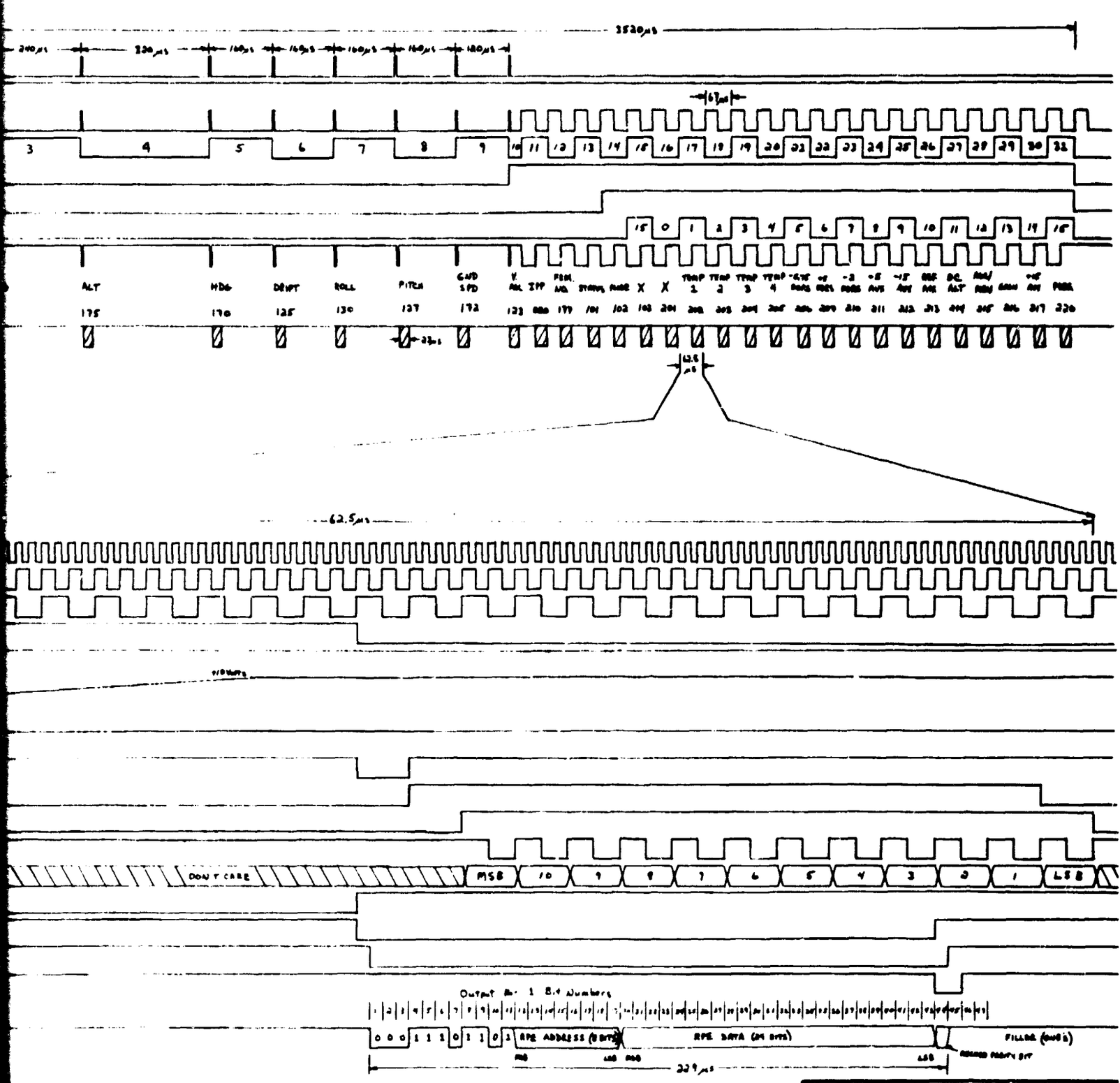


FIGURE 13
RPE TIMING DIAGRAM

BE-80-102

TABLE IV

RPE CONTROL PROM AND ADDRESS PROM BIT PATTERNS

PROGRAM COUNTER ADDRESS		CONTROL PROM OUTPUTS (UE10)					RPE ADDRESS PROM OUTPUTS (UF8)						
DECIMAL	HEX	BINARY 8766	432	1	OCTAL	HEX	BINARY 87	654	321	OCTAL	HEX	DATA CORRESPONDING TO RPE ADDRESS	
0	0	0000	000	0	000	00	01	111	001	171	79	TIME	NERDAS
1	1	0000	000	0	000	00	10	000	000	200	80	DATE	
2	2	0000	000	0	000	00	10	010	001	221	91	LATITUDE	
3	3	0000	000	0	000	00	01	011	010	132	5A	LONGITUDE	
4	4	0000	000	0	000	00	01	111	101	175	7D	ALTITUDE	
5	5	0000	000	0	000	00	01	111	000	170	78	HEADING	
6	6	0000	000	0	000	00	01	010	101	125	55	DRIFT	
7	7	0000	000	0	000	00	01	011	000	130	58	ROLL	
8	8	0000	000	0	000	00	01	010	111	127	57	PITCH	
9	9	0000	000	0	000	00	01	111	010	172	7A	GROUND SPEED	
10	A	0000	000	1	001	01	01	010	011	123	53	VERTICAL ACCELERATION	
11	B	0000	001	1	003	03	00	010	000	020	10	INTER-PULSE PERIOD	DDRS
12	C	0000	010	1	005	05	01	111	111	177	7F	FRAME NUMBER	
13	D	0000	011	1	007	07	01	000	001	101	41	STATUS	
14	E	0000	100	1	011	09	01	000	010	102	42	MODE	
15	F	1111	101	1	373	FB	01	000	011	103	43	UNDEFINED	
16	10	0000	111	1	017	0F	10	000	001	201	81	UNDEFINED	AUXILIARY DATA CONVERSION BOARD
17	11	0001	111	1	037	1F	10	000	010	202	82	TEMP 1 (DDRS BOARD 9)	
18	12	0010	111	1	057	2F	10	000	011	203	83	TEMP 2 (DDRS BOARD 2)	
19	13	0011	111	1	077	3F	10	000	100	204	84	TEMP 3 (NOT CONNECTED)	
20	14	0100	111	1	117	4F	10	000	101	205	85	TEMP 4 (AGC/STC)	
21	15	0101	111	1	137	5F	10	000	110	206	86	-5.75 V POWER (DDRS)	
22	16	0110	111	1	157	6F	10	000	111	207	87	+5 V POWER (DDRS)	
23	17	0111	111	1	177	7F	10	001	000	210	88	-2 V POWER (DDRS)	
24	18	1000	111	1	217	8F	10	001	001	211	89	+5 V POWER (AGC/STC)	
25	19	1001	111	1	237	9F	10	001	010	212	8A	-15 V POWER (AGC/STC)	
26	1A	1010	111	1	257	AF	10	001	011	213	8B	+10 V REFERENCE	
27	1B	1011	111	1	277	BF	10	001	100	214	8C	dc ALTITUDE	
28	1C	1100	111	1	317	CF	10	001	101	215	8D	AGC/MANUAL GAIN	
29	1D	1101	111	1	337	DF	10	001	110	216	8E	GAIN	
30	1E	1110	111	1	357	EF	10	001	111	217	8F	+15 V POWER (AGC/STC)	
31	1F	1111	111	1	377	FF	10	010	000	220	90	AMBIENT PRESSURE (DDRS)	

ANALOG MUX ADDRESS

RPE DATA BUS ENABLE SELECT

SELECTS UPPS STROBE INTERNAL CLOCK

RECORDED ON TAPE AS RPE ADDRESS

RPE Parameter	Address (Octal)	DRIE Display Label
Time	171	LONGITUDE
Heading	170	LATITUDE
Ground Speed	172	HEADING
Frame Number	177	FRAME NUMBER
Altitude	175	RMIN

(b) The other parameters are assigned arbitrary addresses convenient for the ARL:UT software which reads and processes the RPE data.

The 24 bits following the eight address bits are latched from the RPE data bus. There are six sets of bus drivers, only one of which is enabled (by UG8, according to bits 2, 3, and 4 of the control PROM) at a time. The bus driver for UPPS data has been mentioned. The others are (1) the IPP counter driver (UF3, UF4), (2) the frame counter driver (UF5, UF6, UF7), (3) the mode driver (UD2, UD9, UD10), (4) the status driver (UD1, UH1), and (5) the auxiliary data driver (UE2, UF2).

The IPP counter (UG2, UG3, UG4, UH2, UH3, UH4) counts the number of cycles of the 2.07065 MHz radar clock that have occurred between STC triggers. This number is latched on the rising edge of each STC trigger pulse, about once every 750 μsec. However, the IPP counter number, like all RPE data values, is only recorded on the wideband tape once every RPE output cycle, every 10 msec. Since the STC trigger is asynchronous with the RPE timing, occasionally the IPP number will change while being latched into the output shift register, resulting in faulty IPP reading. However, such an error should not occur more than once every 2.7 min, or about six times during an entire wideband tape.

A frame number is recorded on the RPE track which is used by the DRIE and the ARL:UT data reduction software to block off the

video data into manageable segments. The frame counter (UG5, UG6, UG7, UH5, UH6) on the PPE board increments with every eighth cycle of UPPS/ NERDAS data. This amounts to once every 80 msec, or approximately once every 107 video data records (or once every 107 IPP's). The actual frame number is arbitrary. The playback operator will not use the frame number to identify the data; he will only use it to manage the data. Data identification and correlation with the optical recorder data may be accomplished using NERDAS time-of-day.

The mode data are the 15 bits of the operator control settings along with the control valid bit, which are recorded as one contiguous data word. The status data consist of a 5-bit count of video overranges (from the interface board), the video valid and RPE valid bits (from the video formatting board), the clock valid bit, and a 4-bit count of word-by-word parity errors, all composed into one 12-bit data word. The parity error counter is on the RPE board (UJ1, UJ2, UJ3, UH2). When the DDRS is in the 7-bit data precision mode, the circuit counts the number of parity errors (in the 7 bit plus even parity video data words) during each data record. The count accumulates for 10 msec up to a maximum of 15 errors, at which count it holds until output to the wideband tape. The clock validation circuit (UJ4, UJ5, UJ9, UJ1) tests for an out-of-lock condition on the clock generator board. The clock skew (CLKSKEW) signal from the clock generator board is an exclusive-NOR of the two inputs to the phase comparator. A false level on this line occurs during the time when the reference 2.07065 MHz signal and the synthesized phase locked 2.07065 MHz are out of phase. The rising edge of the clock to flip-flop UJ9, pin 12, occurs approximately 75 nsec after the rising edge 2.07065 MHz synthesized clock. If at this point, in each 2.07065 MHz clock cycle, CLKSKEW is false, then the CLKVAL line goes false and CLKINVAL to the cockpit goes true. One shot UJ4, pin 5, stretches momentary losses of lock into 1 sec pulses on CLKINVAL.

The auxiliary data comes from the auxiliary data conversion board as a serial data stream. The interface board generates a signal (AUXCP) to clock the serial data into the auxiliary data shift

register (UE1, UH7). The parallel outputs of this shift register constitute the 12-bit auxiliary data word. Fifteen different analog parameters are digitized, shifted into the auxiliary data shift register, and output through the output shift register during each 10 msec RPE cycle. The RPE timing diagram (Fig. 13) shows the order in which the auxiliary data are output. The order shown is determined by bits 5, 6, 7, and 8 of the control PROM (UE10). Data formats for all types of RPE data are shown in Table III.

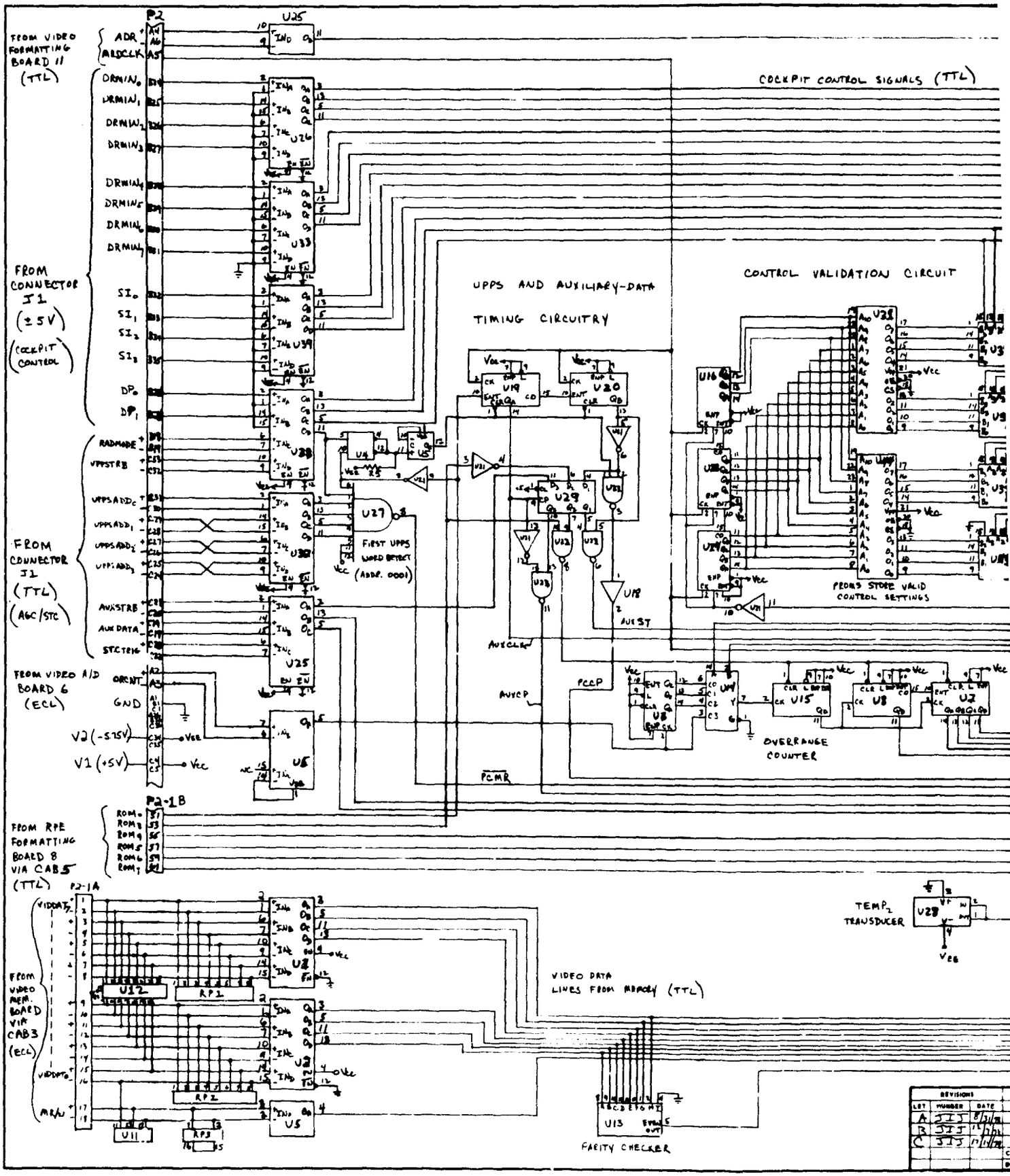
Included on the RPE formatting board is the overrange alert one-shot (UJ4), which outputs a 1 sec ORALT pulse to the cockpit when the MSB of the overrange counter (OR_4) goes true. This condition will occur when about 30% of the video samples are in saturation.

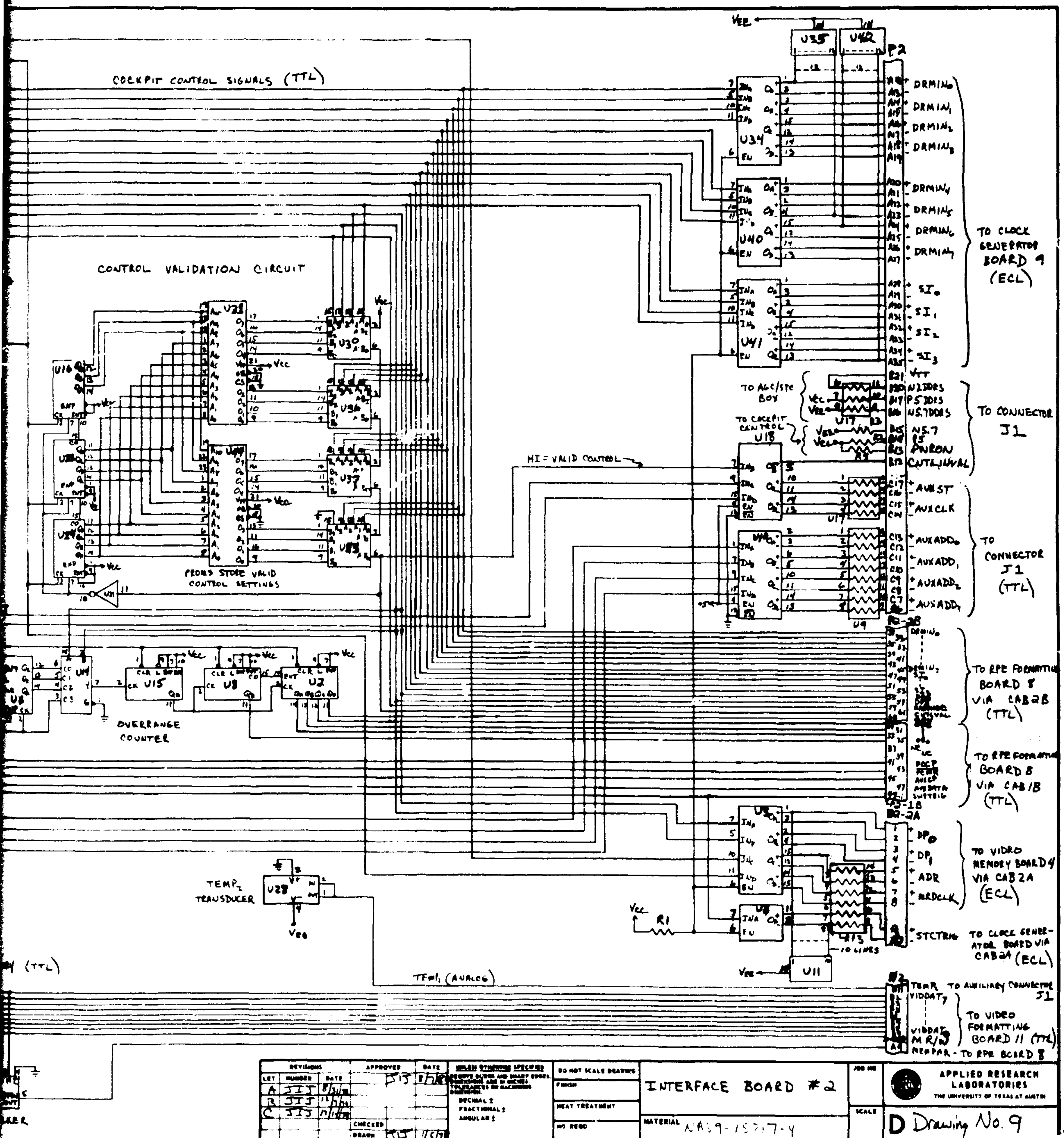
(6) Interface Board (Dwg. No. 9)

Most of the circuitry on the interface board is involved with logic level conversion, line receiving, and line driving. Most ECL-TTL and TTL-ECL signal conversions in the DDRS take place on the interface board. The ±5 V logic signals from the cockpit control panel are converted to TTL and ECL levels here. Since Dwg. No. 9 clearly shows the signal conversion circuitry, no further discussion of it is necessary here.

However, there are a few control circuits included on the interface board. These are (1) UPPS and auxiliary data timing, (2) control validation, (3) overrange counting, and (4) parity checking.

The UPPS and auxiliary data timing circuit (U19, U20, U21, U22, U27, U29) synthesizes the PCMR and PCCP signals required by the RPE formatting board, as well as control and timing signals for the auxiliary data conversion board. U27 outputs the PCMR pulse when the first strobe (time-of-day) of a data cycle from the UPPS occurs. The UPPS address line receiver (U32) is currently wired to recognize an address of 0001 for the time-of-day strobe, but for future requirements, these may


FROM VIDEO FORMATTING BOARD 11 (TTL)
ADR
BLOCLK
DRMIN0
DRMIN1
DRMIN2
DRMIN3
DRMIN4
DRMIN5
DRMIN6
DRMIN7
FROM CONNECTOR J1 (±5V) (COCKPIT CONTROL)
SI0
SI1
SI2
SI3
DP0
DP1
RADMODE
VPPSTRB
VPPSADD0
VPPSADD1
VPPSADD2
VPPSADD3
FROM CONNECTOR J1 (TTL) (AGC/STC)
AUXSTRB
AUX DATA
STCTRIG
FROM VIDEO A/D BOARD 6 (ECL)
ORCNT
GND
V2 (-5.75V)
V1 (+5V)
P2
P2-1B
FROM RPE FORMATTING BOARD 8 VIA CAB5 (TTL)
ROM0
ROM1
ROM2
ROM3
ROM4
ROM5
ROM6
ROM7
P2-1A
FROM VIDEO MEM. BOARD VIA CAB3 (ECL)
VIDDAT7
VIDDAT0
MR/W
COCKPIT CONTROL SIGNALS (TTL)
UPPS AND AUXILIARY-DATA TIMING CIRCUITRY
CONTROL VALIDATION CIRCUIT
FIRST UPPS WORD DETECT
(ADDR. 0001)
AUXST
AUXCLK
AUXCP
PCCP
PCMR
PROMS STORE VALID CONTROL SETTINGS
OVERRANGE COUNTER
TEMP. TRANSDUCER
VIDEO DATA LINES FROM MEMORY (TTL)
PARITY CHECKER
REVISIONS
LET
NUMBER
DATE
A
B
C


COCKPIT CONTROL SIGNALS (TTL)
CONTROL VALIDATION CIRCUIT
PROMS STORE VALID CONTROL SETTINGS
HI = VALID CONTROL
OVERRANGE COUNTER
TEMP2 TRANSDUCER
TEMP2 (ANALOG)
TO CLOCK GENERATOR BOARD 9 (ECL)
TO AGC/STC BOX
TO COCKPIT CONTROL
TO CONNECTOR J1
TO CONNECTOR J1 (TTL)
TO RPE FORMATTING BOARD 8 VIA CAB 2B (TTL)
TO RPE FORMATTING BOARD 8 VIA CAB 1B (TTL)
TO VIDEO MEMORY BOARD 4 VIA CAB 2A (ECL)
TO CLOCK GENERATOR BOARD VIA CAB 2A (ECL)
TO AUXILIARY CONNECTOR J1
TO VIDEO FORMATTING BOARD 11 (TTL)
TO RPE BOARD 8
DO NOT SCALE DRAWING
INTERFACE BOARD #2
MATERIAL NAS9-15717-4
APPLIED RESEARCH LABORATORIES
THE UNIVERSITY OF TEXAS AT AUSTIN
D Drawing No. 9

be changed to recognize any time-of-day address by reversing the inverting and noninverting inputs as required.

The PCCP signal has for its source either the UPPS strobe or a 15 kHz square wave from U20, pin 13. Signal ROM_0 from the RPE formatting board (the LSB of the control PROM on that board) determines the source: a false level selects the strobe by disabling counters U19 and U20, while a true level selects the square wave by enabling the counters and gating off the strobe at U4, pin 10. (An ECL inverter with a wire OR connection followed by a ECL-TTL translator is used here because of lack of space for another TTL NAND gate on the board.)

The AUXST signal commands the A/D converter in the auxiliary data conversion board to start a conversion. It is a 2 μsec negative going pulse generated on the rising edge of the 15 kHz square wave from U20, pin 13. The AUXCLK is the 0.96 MHz clock signal to the A/D converter chip on the auxiliary data board. The timing of these signals is shown in Fig. 13.

The control validation circuit (U16, U23, U24, U30, U31, U36, U37, U43, U44) compares the four cockpit settings (delta RMIN, sample interval, data precision, and radar mode) with preprogrammed valid control setting in the PROM's U31 and U34. Appendix C, Sec. 1, outlines the valid control settings as currently programmed, and Appendix C, Sec. 2, is a printout of the actual numbers (in base 16) stored in the PROM chips. Address counters U16, U23, and U24 count through the 2048 address location in the PROM's until one of the address locations is reached which contains data that match the control switch setting. At this time, the "equals" output of the 16-bit magnitude comparator (U30, U36, U37, U43) at pin 6, U43, goes true. This stops the address counters and turns off the CONTROL INVALID light in the cockpit.

The overrange counter circuit (U6, U7, U8, U14, U15) counts the number of video samples during a 10 msec period for which either the horizontal or the vertical video input circuitry was in saturation.

It was found during the FLAMR program that an optimum video level resulted in about 10% of the video samples being in saturation. The overrange counter circuit counts up to a maximum 60% saturation (at an IPP of 740 μsec); the MSB goes high at 30% saturation and causes the overrange alert (ORALT) light to turn on in the cockpit. The lower the data precision is, the more video samples are produced in a 10 msec interval, and multiplexer U14 and counter U6 compensate to allow the overrange count to accumulate to a greater number for the lower data precisions.

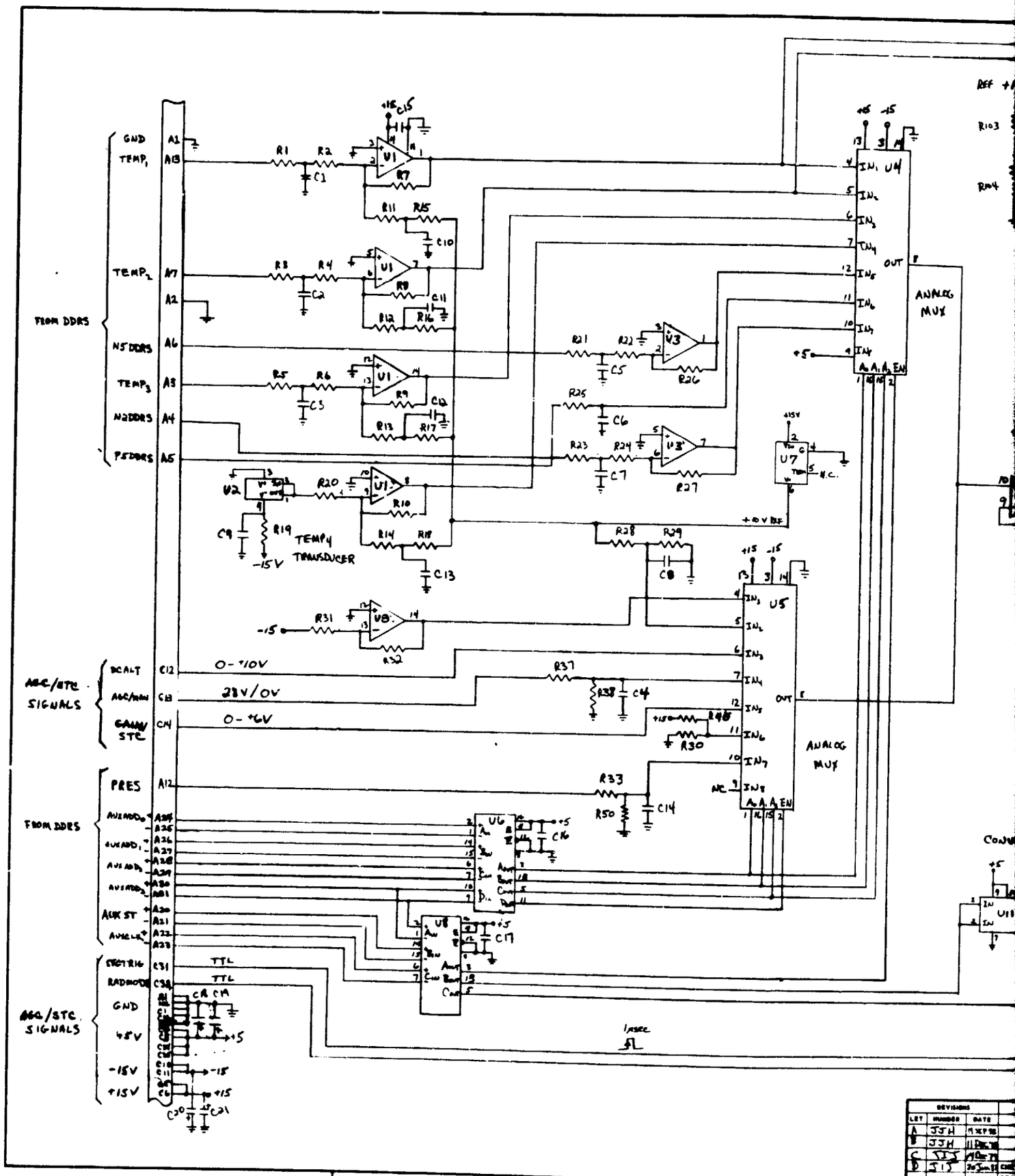
Finally, as the video data are read from the memory, U13 outputs a true level at pin 5 whenever the eight bits of the data words do not have even parity. This signal (MEMPAR) is sent to the RPE formatting board which, when the system is in the 7-bit mode, counts the number of memory words which do not have even parity when read, as indicated by MEMPAR.

(7) Auxiliary Data Conversion Board (Dwg. No. 10)

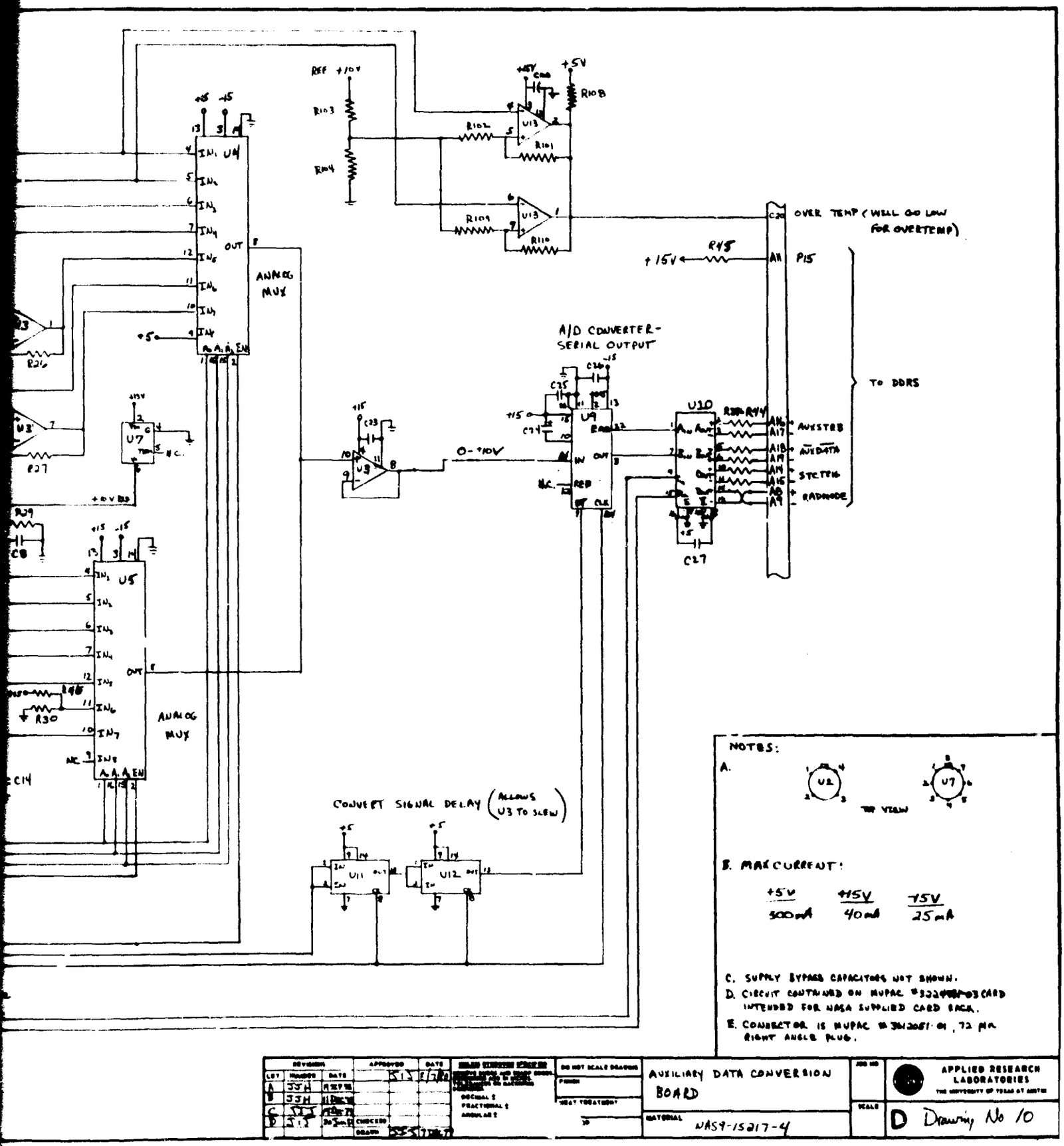
The main purpose of the auxiliary data conversion board is to digitize dc voltages corresponding to radar and environmental parameters. It also interfaces the STC trigger and the radar mode signals from the AGC/STC processor with the DDRS.

Temperature transducer outputs from the DDRS and the TEMP 4 transducer output on board the auxiliary data board are amplified by quad operational amplifier U1. Since the auxiliary A/D converter (U9) operates on an analog voltage range of 0 to +10 V, the negative polarity of the temperature transducer outputs and the negative supply voltages are inverted by U1 and U3.

Sixteen analog voltages (one of which is not currently connected) are multiplexed through the analog multiplexers U4 and U5. Each of the 16 voltages are sequentially selected by the control PROM on the RPE formatting board through the auxiliary address lines ($AUXADD_0$-



FULLDOUT FRAME



FOLDOUT FRAME 2

$AUXADD_3$). The output of the multiplexers is buffered by part of U3 and connected to the analog input of the A/D.

The interface board of the DDRS synthesizes the start convert (AUXST) and the conversion clock (AUXCLK) signals to the auxiliary A/D, as required by the A/D data sheet (Micro Networks MN5216). The start conversion signal is delayed 33 μsec by shift registers U11 and U12 to allow the multiplexer output buffer to slew between successive data voltages. Control timing for the auxiliary A/D is shown in the RPE timing diagram, Fig. 13.

Overtemperature comparator U13 senses the outputs of the DDRS temperature transducers (TEMP 1 and TEMP 2). The comparator output will go to a TTL low level when either of the transducers indicate 60°C or greater. This output (OVERTEMP) should be used to disconnect power to the DDRS. The relay to remove DDRS power should be latching; i.e., once triggered to remove power, it should have to be manually reset. This is necessary because as soon as the DDRS is turned off, the OVERTEMP signal will immediately go high again. If, at this time, the relay is not latched off, power will be reconnected to the DDRS and OVERTEMP will again go low, disconnecting power again, ad infinitum.

IV. OPERATION AND MAINTENANCE

A. Preflight Checkout Procedure

1. Test Equipment Required

oscilloscope, event counter

2. Video System Checkout

a. Connections required to test connector J103:

(1) VIDEO NRZ track 7 to the oscilloscope vertical input
(2) TRIGVID to the oscilloscope
(3) PARCHK to the event counter
(4) REF to the video inputs J108 and J109

b. Connect all other DDRS I/O connectors to their respective pallet cables.

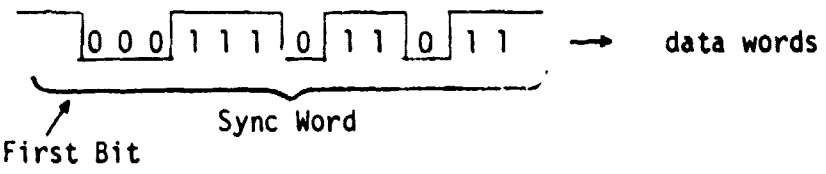
c. Double check connections and apply power.

d. From the control panel, switch the DDRS into the 4-bit data precision mode and adjust the event counter sensitivity to show a rapid count on the event counter.

e. From the control panel, switch the DDRS into the 7-bit mode. The count rate should decrease to zero. If the count rate is still high, decrease the counter sensitivity just until the counting stops and switch

back to the 4-bit mode. The count rate should always be very high in the 4-bit mode. Now switch back to the 7-bit mode for further tests and reset the event counter to zero.

f. Set the horizontal sweep rate on the oscilloscope to 1 μsec/div, and adjust the trigger sensitivity to display a stable digital waveform on the CRT. This waveform is the first part of the video data record. The bit duration is 0.51 μsec, or about 2 bits per horizontal division. The first bit begins where the waveform first falls from a high level to a low level. The first twelve bits in the record compose the sync word and should always be 000111011011:



The rest of the record is composed of 128, 8-bit, serial 2's complement data words, MSB (sign) first and parity bit last. The same word should be repeated all 128 times. The value of this word depends on the reference voltage level connected to the video inputs from the test connector, and is adjustable internally on board 6 of the DDRS. Note that the seventh bit of this word may toggle (on noise along with the eighth parity bit). Check all eight tracks of video NRZ data for the same characteristic waveform. This test may be more easily done in the 4-bit mode, if the toggling of the LSB and parity bits becomes too distracting.

g. Disconnect video inputs J108 and J109 and repeat step 6. The value of the data word should be within 1 or 2 LSB's of all zeroes.

h. Check the event counter for zero parity errors for as long as the system was in the 7-bit mode.

i. Check the eight Miller-encoded video data lines to the

wideband tape recorder with an oscilloscope for a phase encoded square wave on each.

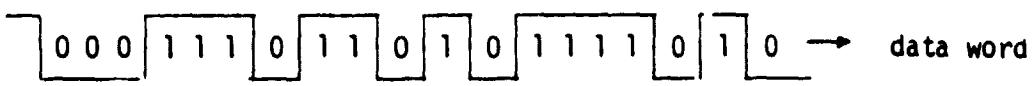
3. RPE System Checkout

a. Connections required to test connector J103:

(1) RPE NRZ to the oscilloscope vertical input
(2) TRIGRPE to the oscilloscope trigger input
(3) RPE TEST to ground
(4) AUX/UPPS to ground

b. Input a constant 24-bit word (DOD-23) from the UPPS MUX output to the DDRS with a periodic strobe pulse from the UPPS STRB output. (Repetition rate of the STRB pulse not to exceed 25 kHz.)

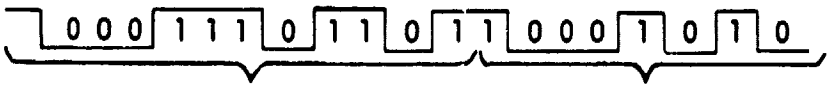
c. Set the horizontal sweep rate of the oscilloscope to 1.0 μsec/div and adjust the trigger sensitivity to obtain a stable waveform on the CRT. Observe the waveform. The first eleven bits are the sync words, 00011101101, and the next eight bits are the "test" address bits, 01111010:



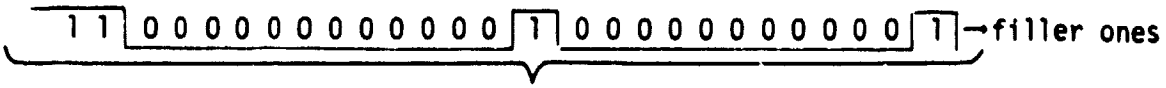
sync word address

The following 24-bit data word (MSB first) should be identical to the 24-bit word input from the UPPS. After the 24th bit of the data word will be the record parity bit followed by filler ones.

d. Now disconnect the AUX/UPPS input on J103 from ground. Observe the scope waveform. The sync word should now be f llowed by a different 8-bit address, 10001010:



The 24-bit data word should be nominally
000000000000 1 0000000:



The data word may vary several bits from its nominal value.

e. Check the Miller-encoded RPE data line to the wideband tape recorder for a phase encoded square wave.

4. Disconnect J103 and reconnect the video lines from the optical recorder. The DDRS is now ready for flight.

B. System Operation

After a successful preflight checkout, the system is ready for in-flight operation. With the unit cabled up and installed in the pallet, the operator has only to set the required sample interval, data precision, and delta RMIN from the control panel. Once the pallet is powered up, and the DDRS receives UPPS data and clock and STC signals, all the control panel lights except "POWER ON" should go out. After this time, merely connect voice and time code to the wideband recorder and start the recorder when desired.

C. Adjustments

There are few internal adjustments in the DDRS. Those most often requiring attention are the trimmer potentiometers on the A/D board. Other

adjustments rarely requiring attention are timing adjustments by jumper wires on the clock generator board, the video A/D board, and the video memory board.

The gain and bias potentiometer adjustments on the video A/D board are explained in Sec. III.D. The gain adjustment should be set so that the overrange alert (ORALT) light rarely, if ever, lights up. Otherwise, adjust the gain for optimum image quality, which past experience has shown to be about 10% overrange. The bias adjustment should be used to compensate for an unwanted dc offset in the video signals. There is also an output reference potentiometer which may be adjusted to set a desirable test voltage for preflight checkout of the video A/D subsystem (Sec. IV.A). The best reference voltage is that which, after being digitized, produces an easily recognized digital waveform on the video data recorder tracks.

The other internal adjustments are timing adjustments and involve changing jumper wires. These jumpers select one of several taps on tapped lumped-constant delay lines. There are four of these jumpers: one on the clock generator board 9 (Dwg. No. 4) to delay the reset memory address for write ($\overline{ADW}$); one on the video A/D board 6 (Dwg. No. 5) to delay the sample pulse to the vertical channel A/D with respect to the sample pulse to the horizontal channel A/D; and finally, one on the video memory board 4 (Dwg. No. 6) to set the width of the write-enable pulse ($\overline{WE}$) to the memory chips. The current positions of these jumpers are shown in the drawings. They should not have to be repositioned except when a TRW A/D chip is replaced, or perhaps as the TRW chips age and their propagation delay characteristics change.

The object in setting the jumpers is to meet the memory chip (Fairchild 10415A) requirements for write pulse width (14 nsec) and for stable A/D data at the memory chip inputs throughout the time the $\overline{WE}$ signal is low. To check timing, use a high speed oscilloscope (Tek 7834 or 485 recommended) preferably with a fast FET input active probe (Tek P6201 or P6202). Observe the data input (pin 15) and the $\overline{WE}$ input (pin 13) on a 10415A memory chip. With the system in the 7-bit mode and while digitizing

a video signal (a sine wave is good), A/D transitions at the D_{in} pin should be visible. Ensure that these transitions occur only when $\overline{WE}$ is high. It is important to check every 10415A this way since propagation delays to each chip are slightly different. Check the timing at 40 nsec sampling intervals and also at 60 nsec sampling intervals. (Refer to Fig. 10.)

If data transitions occur during a $\overline{WE}$ pulse, the timing of the $\overline{WE}$ pulse must be changed. It can be advanced by decreasing the delay of the MWRTCLK on the video A/D board (currently set to 30 nsec) and it may be retarded by increasing the same delay. Line 12 of Fig. 10 illustrates this delay. If the data timing from one A/D channel is good, but the timing of the other A/D channel is off, the vertical A/D may be delayed with respect to the horizontal A/D by using the other jumper on the A/D board. This requires the faster A/D to be in socket U25 with the slower in U26, and the TRW chips may need to be reversed.

It is not recommended that the $\overline{WE}$ pulse width be changed (by changing the jumper on the video memory board). This width is currently set to 14 nsec (as shown in line 13 of Fig. 10).

The other timing adjustment involves the delay of the $\overline{ADW}$ signal on the clock generator board. This will not require adjustment unless the MWRTCLK delay is decreased. Refer to Fig. 10, line 9. The $\overline{ADW}$ signal (available on the memory board at U31, pin 5) must rise after the first pulse of MWRTCLK (on memory board at U32, pin 15) in an IPP, but before the second one. The delay is currently set at 50 nsec.

D. Maintenance

Symptoms and Causes - Corrective Action

1. RPE-INVALID lights up
   Probable cause - no UPPS strobe or address

2. VIDEO-INVALID lights up
   Probable causes - no STC trigger
   - no 2.07065 MHz clock

3. CLOCK-INVALID lights up
   Probable causes - no 2.07065 MHz clock
   - noisy clock signal

4. CONTROL-INVALID lights up
   Probable cause - invalid control setting (will not disable DDRS)

5. OVERRANGE-ALERT lights up
   Probable cause - video A/D gain not properly adjusted

6. High parity error count (in 7-bit mode only)
   Probable causes - MWRTCLK timing needs adjustment (Sec. IV.C)
   - bad memory chip

The above symptoms will probably be most common and are fairly simple to correct. If more serious problems develop, a complete understanding of the DDRS circuitry and timing will be required, and the drawings and timing diagrams of this document will have to be studied thoroughly. It is recommended that before any major surgery is performed, all connector pins and sockets be checked (both on front panel I/O connectors and on internal card cage connectors) and all power supply outputs be checked. The DDRS circuitry is made up of reliable components; however, those most likely to be the first to fail will be the more complex components: the TRW A/D chips, the memory chips, and the power supplies.

It must be stressed that the key to reliability in the DDRS is in maintaining as low an operating temperature as possible. The cooling fan inside the unit will help in this regard, but even with the fan, the interior DDRS temperature runs 10°C hotter than outside ambient temperature at sea level. It is important that the power to the unit be disconnected when the OVERTEMP line on the auxiliary data board goes low, and it is

also recommended that close attention be given to the recorded values for TEMP 1, TEMP 2, and TEMP 4 on the first data tapes.

APPENDIX A

CRITICAL SPARES AND PARTS LIST WITH COMPONENT PLACEMENT DRAWINGS

CRITICAL SPARES LIST

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS	1A. Contract No.	2. Code (Army)	3. PL	4. Revision: Ltr. Date
5. List Title: SPARE PARTS FOR DDRS		6. Authentication:		7. Rev Auth No.	8. Sheet 1 of 3 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description	
1	1	pkg.		1301422-01	Mupac wire-wrap socket terminal	@$13.20
2	1	pkg.		1301402-01	Mupac wire-wrap slotted terminal	@ 12.10
3	1	pkg.		1311517-01	Mupac mini terminal receptacle	@ 15.40
4	1	unit		SIRU-2V/4A	Arnold Magnetics 2 V power supply	@353.00
5	1	unit		ASN-MS.5/9V -CS/5V-CA	Arnold Magnetics ±5 V power supply	@791.00
6	1	unit		387JH	Rotron Propimax 3B fan	@ 99.20
7	1	"		TDC 1007J	TRW Video A/D Converter Chip	@745.00
8	3	"		54LS365	Integrated Circuit	@ 0.92
9	3	"		54LS165	Integrated Circuit	@ 2.09
10	2	"		54S28R	Integrated Circuit	@ 4.37
11	1	"		54LS138	Integrated Circuit	@ 1.44
12	2	"		54LS04	Integrated Circuit	@ 0.61
13	1	"		54LS00	Integrated Circuit	@ 0.61
14	2	"		54LS109A	Integrated Circuit	@ 0.72
15	1	"		54LS123	Integrated Circuit	@ 1.79
16	1	"		54121	Integrated Circuit	@ 1.38
17	3	"		54LS112	Integrated Circuit	@ 0.73
18	2	"		54LS02	Integrated Circuit	@ 0.58
19	1	"		54LS30	Integrated Circuit	@ 0.58
20	1	"		54LS37	Integrated Circuit	@ 0.68
21	1	"		54LS85	Integrated Circuit	@ 2.03
22	1	"		54LS280	Integrated Circuit	@ 2.39
23	2	"		2N5583	Transistor	@ 3.85
24	2	"		2N4403	Transistor	@ 0.46

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No.	2. Code Ident.	3. PL	4. Revision Ltr. Date
5. List Title: SPARE PARTS FOR DDRS		6. Authentication:		7. Rev Auth No.	8. Sheet 2 of 3 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description	
25	2	unit		MC12040L	Motorola Integrated Circuit	@ 7.09
26	2	"		MC1648L	Motorola Integrated Circuit	@ 3.90
27	2	"		LH0032G	National Integrated Circuit	@ 50.90
28	1	"		LX5600AH	National Integrated Circuit	@ 6.50
29	1	"		LX1602A	National Integrated Circuit	@ 85.00
30	1	"		LM139D	National Integrated Circuit	@ 12.00
31	1	"		UA124DM	Fairchild Integrated Circuit	@ 6.75
32	3	"		10115	Fairchild Integrated Circuit	@ 0.60
33	2	"		10125	Fairchild Integrated Circuit	@ 1.50
34	2	"		10105	Fairchild Integrated Circuit	@ 0.50
35	3	"		10124	Fairchild Integrated Circuit	@ 1.50
36	2	"		10160	Fairchild Integrated Circuit	@ 3.20
37	4	"		10174	Fairchild Integrated Circuit	@ 2.70
38	2	"		10103	Fairchild Integrated Circuit	@ 0.47
39	3	"		10016	Fairchild Integrated Circuit	@ 4.25
40	2	"		10010	Fairchild Integrated Circuit	@ 4.25
41	2	"		10131	Fairchild Integrated Circuit	@ 1.80
42	2	"		10135	Fairchild Integrated Circuit	@ 1.60
43	2	"		10102	Fairchild Integrated Circuit	@ 0.47
44	2	"		10107	Fairchild Integrated Circuit	@ 0.50
45	2	"		10101	Fairchild Integrated Circuit	@ 0.47
46	5	"		10415A	Fairchild Integrated Circuit	@ 18.20
47	2	"		10173	Fairchild Integrated Circuit	@ 2.70
48	2	"		10171	Fairchild Integrated Circuit	@ 2.40

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No.	2. Code Ident.	3. PL	4. Revision Ltr. Date
5. List Title: SPARE PARTS FOR DDRS		6. Authentication:		7. Rev Auth No.	8. Sheet 3 of 3 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description	
49	2	unit		10161	Fairchild Integrated Circuit	@ 2.40
50	2	"		10136	Fairchild Integrated Circuit	@ 6.50
51	2	"		AM 687	Advanced Micro Devices IC	@ 42.00
52	2	"		25LS 153	Advanced Micro Devices IC	@ 1.60
53	4	"		25LS 161	Advanced Micro Devices IC	@ 2.01
54	2	"		25 LS 174	Advanced Micro Devices IC	@ 1.80
55	3	"		25LS 164	Advanced Micro Devices IC	@ 2.90
56	5	"		25LS 32	Advanced Micro Devices IC	@ 11.85
57	6	"		25S 31	Advanced Micro Devices IC	@ 13.65
58	2	"		25LS 157	Advanced Micro Devices IC	@ 1.60
59	1	"		PE 9824	Pulse Engineering, Inc., Delay Line	@ 21.25
60	1	"		PE 21171	Pulse Engineering, Inc., Delay Line	@ 21.40
61	2	"		AD580SH	Analog Devices, Inc., Voltage Ref.	@ 11.75
62	2	"		HI-0508A-2	Harris Analog Multiplexer	@ 39.00
63	1	"		REF-01J	Precision Monolithics Voltage Ref.	@ 15.75
64	1	"		MN5216M	Micro Networks Corp. 12-bit ADC	@330.00
65	1	"		L [illegible]3E	Conner-Winfield Corp. 3.84 MHz Oscillator	@ 63.00
66	2	"		4116R-002-202	Bourns Resistor Network	@ 1.25
67	2	"		4308R-101-121	Bourns Resistor Network	@ 0.50
68	2	"		899-1-R560	Beckman Resistor Network	@ 1.43
69	2	"		316B560	Allen-Bradley Resistor Network	@ 1.43
70	2	"		316A561	Allen-Bradley Resistor Network	@ 1.43
					Total Cost for Spare Parts	$3301.78

PARTS LIST WITH COMPONENT PLACEMENT DRAWINGS

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217	2. Code	3. PL	4. Revision Ltr. Date
5. List Title: AUXILIARY DATA CONVERSION BOARD		6. Authentication:		7. Rev Auth No.	8. Sheet 1 of 3 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
U1, U3	2	ea		UA124DM	Quad Operational Amplifier, Fairchild
U2	1	ea		LX5600A	Temperature Transducer, National Semiconductor
U4, U5	2	ea		HI1-0508A-2	8-Channel Analog Multiplexer, Harris
U6, U8	2	ea		AM26LS32DC	Quad Line Receiver, Advanced Micro Devices
U7	1	ea		REF-01J	+10 V Precision Voltage Reference, Precision Monolithics
U9	1	ea		MN5216M	12-Bit A/D Converter, Micro Networks Corp.
U10	1	ea		AM26LS31DC	Quad Line Driver, Advanced Micro Devices
U11, U12	2	ea		AM25LS164DC	8-Bit Serial-In, Parallel-out Shift Register, Advanced Micro Devices
U13	1	ea		LM339N	Quad Comparator, National
C18, C19 C20, C21	4	ea		CSR13G226KM	Capacitor, 22 µF, Tantalum
C24	1	ea		CSR13G225KM	Capacitor, 2.2 µF, Tantalum
C	10	ea		1802-Z5U050A104M	Capacitor, 0.1 µF, Green Goddess, Varadyne
R1, R2, R3, R4, R5, R6, R21, R22 R23, R24 R32	11	ea		RN60D4991	Resistors, 4.99 kΩ, 1%, 1/4 W
R7, R8, R9, R10	4	ea		RN60D8062	Resistors, 80.6 kΩ, 1% 1/4 W
R15, R16 R17, R18	4	ea		RN60D4222	Resistors, 42.2 kΩ, 1%, 1/4 W

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217	2. Code Ident.	3. PL	4. Revision Ltr. Date
5. List Title: AUXILIARY DATA CONVERSION BOARD		6. Authentication:		7. Rev Auth No.	8. Sheet 2 of 3 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
R11, R12 R13, R14 R20, [illegible]	4	ea		RN60D6340	Resistor, 634 Ω, 1%, 1/4 W
R27, [illegible] R28, R29	4	ea		RN60D1022	Resistor, 10.2 kΩ, 1%, 1/4 W
R30, R46	4	ea		RN60D1001	Resistor, 1.00 kΩ, 1%, 1/4 W
R37	1	ea		RN60D2001	Resistor, 2.0 kΩ, 1%, 1/4 W
R33	1	ea		RN60D1051	Resistor, 1.05 kΩ, 1%, 1/4 W
R50	1	ea		RN60D4021	Resistor, 4.02 kΩ, 1%, 1/4 W
R38	1	ea		RN60D9790	Resistor, 979 Ω, 1%, 1/4 W
R103	1	ea		RN60D2371	Resistor, 2.37 kΩ, 1%, 1/4 W
R104	1	ea		RN60D1542	Resistor, 15.4 kΩ, 1%, 1/4 W
R102 R109 R101	2	ea		RN60D4751	Resistor, 4.75 kΩ, 1%, 1/4 W
R110	2	ea		RN60D4752	Resistor, 47.5 kΩ, 1%, 1/4 W
R25	1	ea		RCR07-102	Resistor, 1 kΩ, 5%, 1/4 W
R39 - R44	6	ea		RCR07-560	Resistor, 56 Ω, 5%, 1/4 W
R45	1	ea		RCR07-270	Resistor, 27 Ω, 5%, 1/4 W
R19	1	ea		RCR07-822	Resistor, 8.2 kΩ, 5%, 1/4 W
R108	1	ea		RCR07-302	Resistor, 3.0 kΩ, 5%, 1/4 W
Aux Board	1	ea		3223081-01	322-type universal panel w/o sockets, MUPAC Corp.
Aux Connector	1	ea		3612061-01	108-contact right-angle connector, MUPAC Corp.

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217	2. Code (Agency)	3. PL	4. Revision Ltr. Date
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9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
N/A	174	ea		1301402-01	Wire-wrap slotted terminals, MUPAC Corp.
N/A	174	ea		1301422-01	Wire-wrap socket terminals, MUPAC Corp.
--	--	--		----------	30 ga. wire-wrap as needed.

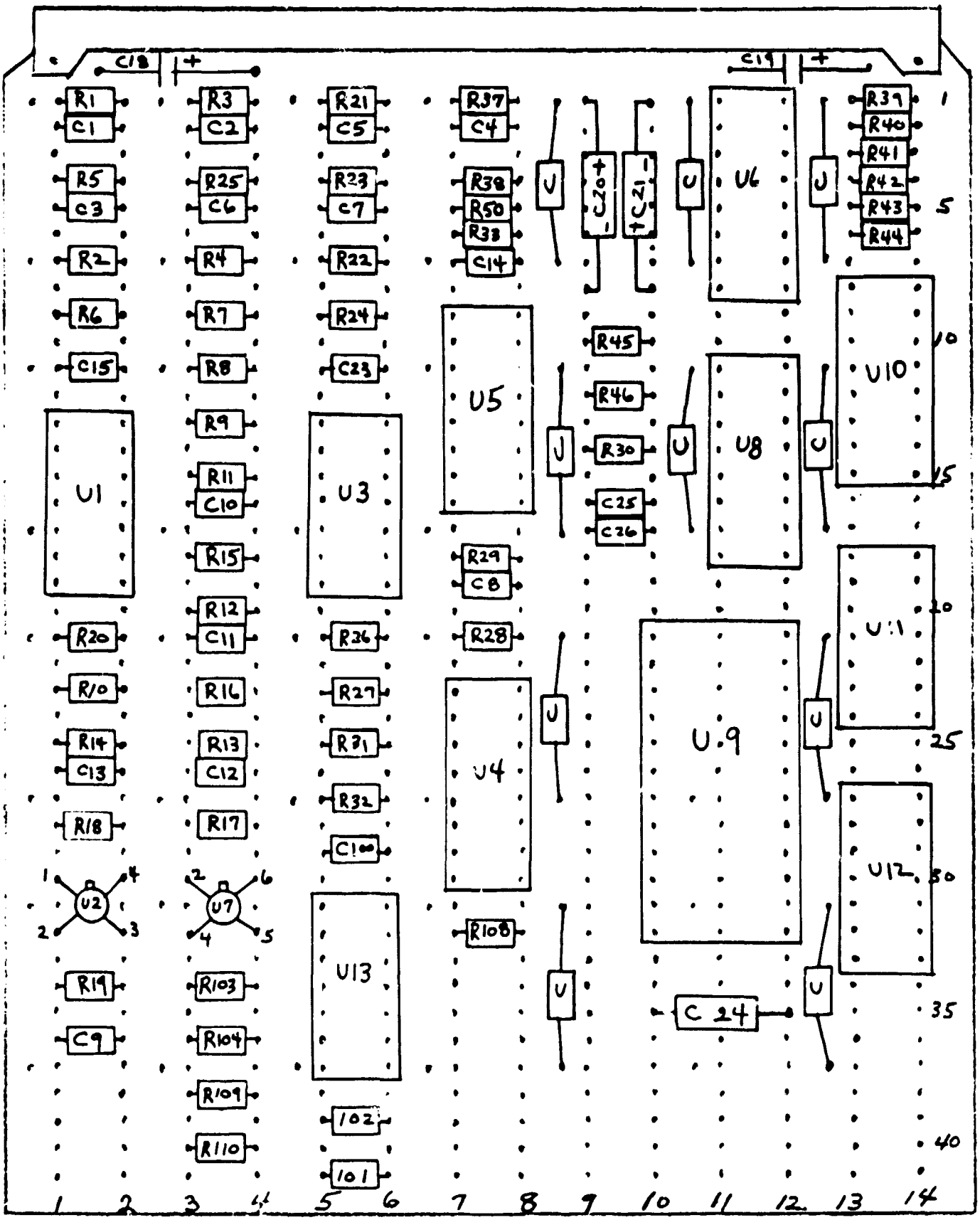

FIGURE A-1
AUXILIARY DATA CONVERSION BOARD

11 Oct 78 JJH
REV 11 Dec 78 JJH

AE-80-103

PARTS LIST

1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS

1A. Contract No. NAS9-15217-3

2. Code Ident.

3. PL

4. Revision Ltr. Date

5. Item Title: DDRS System Hardware

6. Authentication:

7. Dev Auth No.

8. Sheet No. 1 of 1 Sheets

9. Item or Find Number	10. Qty Req'd	11. Unit of Measure	12. Reference (Specification or Document Number)	13. Part or Identifying Number	14. Nomenclature or Description
P2, P4, P11	3	ea.		3612061-01	108-pin Right Angle Plug
J2, J4 J11, J3 J10	5	ea.		3612261-01	108-pin Receptacle
P5, P7 P9	3	ea.		3612056-01	72-pin Right Angle Plug with Solder Connectors
J5, J7, J9	3	ea.		3612251-01	72-pin Receptacle
CAB1	1	ea.		3552015	36-conductor Flat Cable
CAB2, CAB4	2	ea.		3552035	8-conductor Twisted-Pair Cable
CAB3	1	ea.		3552045	18-conductor Twisted-Pair Cable
P2-1, P2-2A P2-2B P2-2C					Part of In--face Board
BOARD4 BOARD11	2	ea.		3234806-01	323 DIP Wirewrap Panel
BOARD2	1	ea.		3234890-01	323 Universal Wirewrap Panel
BOARD5 BOARD7 BOARD9	3	ea.			Multilayer PC Board, ARL Custom
	1	ea.		3312045-01	6-position Half-Rack Assembly
					All hardware manufactured by MUPAC, Inc., with exception of PC boards.

PARTS LIST	1. Assembly (Contractor Identification) APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-)5217-4	2. Code Ident.	3. PL	4. Revision Ltr. Date
5. List Title INTERFACE BOARD (BOARD NO. 2)		6. Authentication:		7. Rev Auth No.	8. Sheet 1 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
U5	1	ea		10125 DC	Quad ECL-to-TTL Translator, FAIRCHILD
U3, U4, U34, U40 U41	5	ea		10124 DC	Quad TTL-to-ECL Translator, FAIRCHILD
U6,U7,U8 U15, U16 U19, U20 U23, U24	9	ea		AM25LS161 DM	Hexadecimal Counter, ADVANCED MICRO DEVICES
U10, U18	2	ea		AM26LS3[illegible] DM	Quad Differential Line Drivers, ADVANCED MICRO DEVICES
U1, U2 U25, U26 U32, U33 U39, U39	8	ea		AM26LS32 DC	Quad Differential Line Receivers, ADVANCED MICRO DEVICES
U14	1	ea		AM25LS153 DM	Dual Four-Input Multiplexer, ADVANCED MICRO DEVICES
U29	1	ea		AM25LS174 DM	Hex D Flip-Flop, ADVANCED MICRO DEVICES
U30, U36 U37, U43	4	ea		SN54LS85J	4-Bit Magnitude Comparators, TEXAS INSTRUMENTS
U13	1	ea		SN54LS280J	9-Bit Parity Generator/Checker, TEXAS INSTRUMENTS
U22	1	ea		SN54LS37J	Quad NAND Gate, TEXAS INSTRUMENTS
U21	1	ea		SN54LS04J	Hex Inverter, TEXAS INSTRUMENTS
U27	1	ea		SN54LS30J	Eight-Input NAND Gate, TEXAS INSTRUMENTS
U28	1	ea		LX5600A	Temperature Transducer, National
U17,U35 U42	3	ea		899-1-R560	Resistor Network, 56 Ω, 13 Resistor, Pin 14 common, BECKMAN

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code	3. PL	4. Revision Ltr. Date
5. List Title: INTERFACE BOARD (BOARD NO. 2)		6. Authentication:	7. Rev Auth No.		8. Sheet 2 of 2 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
U9, U17 RP3	3	ea		316B 560	Resistor Network, 56 Ω, 8 resistors, ALLEN-BRADLEY
U12	1	ea		316A561	Resistor Network, 560 Ω, Pin 16 common, ALLEN-BRADLEY 15 resistors
RP1, RP2	2	ea		4308R-101-121	Resistor SIP, 120 Ω, 8 pin, BOURNS
R1	1	ea		RCR07-102	Resistor, 1 kΩ , 5%, 1/4 W
R2, R3, R4	3	ea		RCR07-101	Resistor, 100 Ω , 5%, 1/4 W
R5	1	ea		RCR07-561	Resistor, 560 Ω, 5%, 1/4 W
BYPASS CAP.	30	ea		1802-Z5U050A104M	Capacitor, 0.1 μF, GREEN GODDESS, VARADYNE
BYPASS CAP.	2	ea		CSR13G226KM	Capacitor, 22 μF, Tantalum
BOARD NO 2	1	ea		3234890-01	Universal 323-type wire-wrap panel, MUPAC
CONNECTOR No. 2	1	ea		3612061-01	Connector, 108-pin, right angle, MUPAC

2-1

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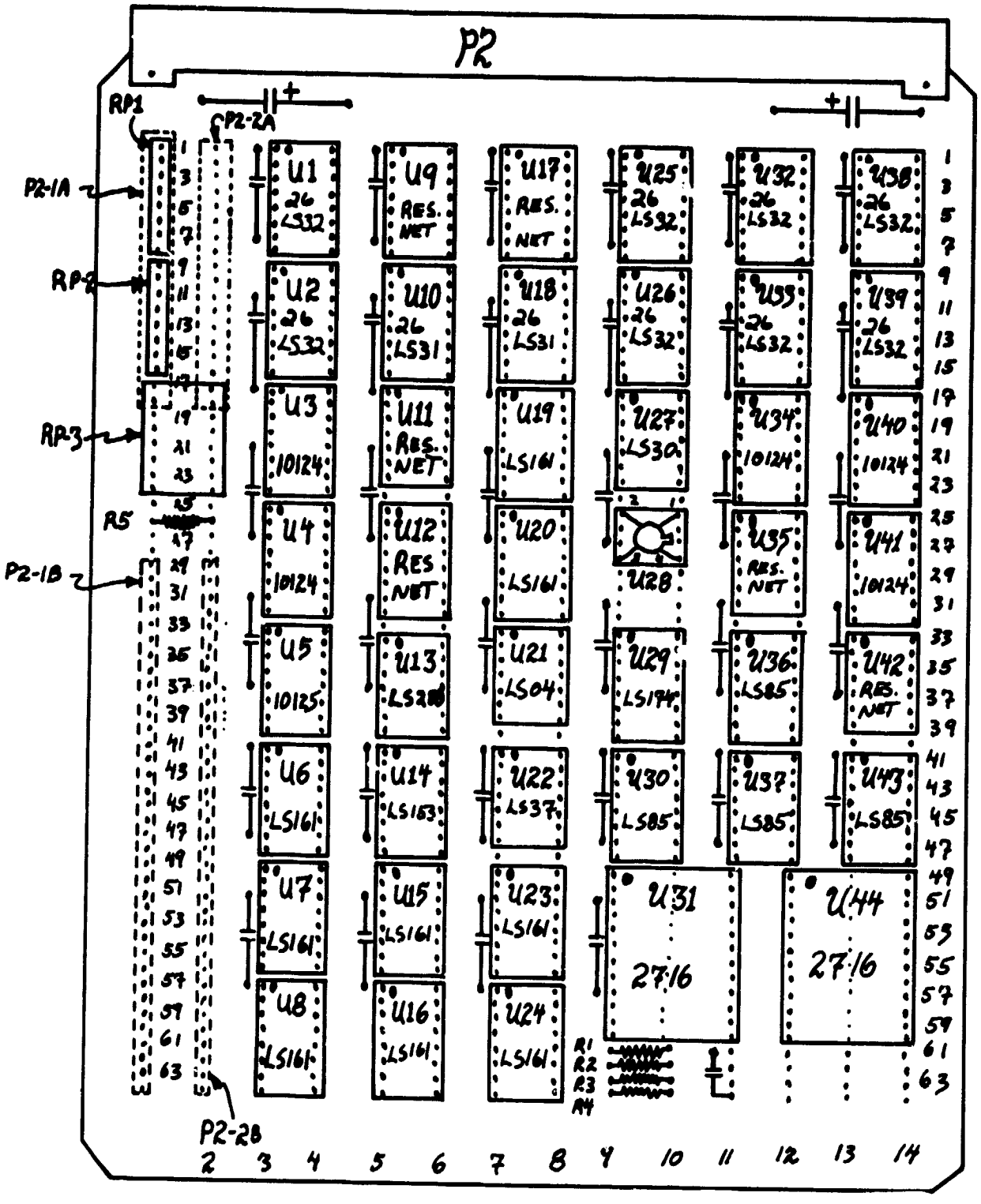
COMPONENT SIDE



MUPAC # 3234890-01

FIGURE A-2
INTERFACE BOARD NO. 2

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code	3. PL	4. Revision Ltr. Date
5. List Title: VIDEO MEMORY (BOARD NO. 4)		6. Authentication:		7. Rev Auth No.	8. Sheet 1 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
U1, U2 U3, U4 U5, U6 U7, U8 U9, U10 U11, U12 U18, U19 U26, U27	16	ea.		10415ADC	1024 x 1-bit RAM, Fairchild
U15, U16 U17, U25 U29	5	ea.		10174DC	Dual Multiplexer, Fairchild
U13, U20 U33	3	ea.		10101 DC	Quad OR/NOR Gate with Common Enable, Fairchild
U32, U28	2	ea.		10115 DC	Quad Line Receiver, Fairchild
U21, U14	2	ea.		10173 DC	Quad Multiplexer/Latch, Fairchild
U30, U31	2	ea.		10016 DC	4-bit Binary Counter, Fairchild
U34	1	ea.		10135 DC	Dual J-K Master-Slave Flip-Flop, FAIRCHILD
U22	1	ea.		10136 DC	4-bit Up-Down Counter, Fairchild
U23	1	ea.		10171 DC	Dual J-K Master-Slave Flip-Flop, Fairchild
U37	1	ea.		10105 DC	Triple 2-3-2 Input OR/NOR Gate, Fairchild
U36	1	ea.		PE 21171	20 nsec Delay Line, Pulse Engineering, Inc.

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS5-15217-4	2. Code 1	3. PL	4. Revision Ltr. Date
5. List Title: VIDEO MEMORY (BOARD NO. 4)		6. Authentication:		7. Rev Auth No.	8. Sheet 2 of 2 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
—	75	ea.		RCR07-820	Resistor, 82 Ω, 1/4 W, 5%
—	10	ea.		RCR07-390	Resistor, 39 Ω, 1/4 W, 5%
—	7	ea.		RCR07-680	Resistor, 68 Ω, 1/4 W, 5%
—	2	ea.		RCR07-470	Resistor, 47 Ω, 1/4 W, 5%
D1	1	ea.		1N840	DIODE,
—	14	ea.		2120-Z5V050R104M	Capacitor, Radial Lead, 0.1 μF, 50 V, Epoxy Dipped Ceramic Cap., VARADYNE
-	2	ea.			Tantalum/Capacitor, 33 μF, 25 V
P4	1	ea.		3612056-01	72-pin Right-Angle Plug, MUPAC
	1	ea.			4.5 x 7.5, 4-layer Printed Circuit Board, ARL:UT

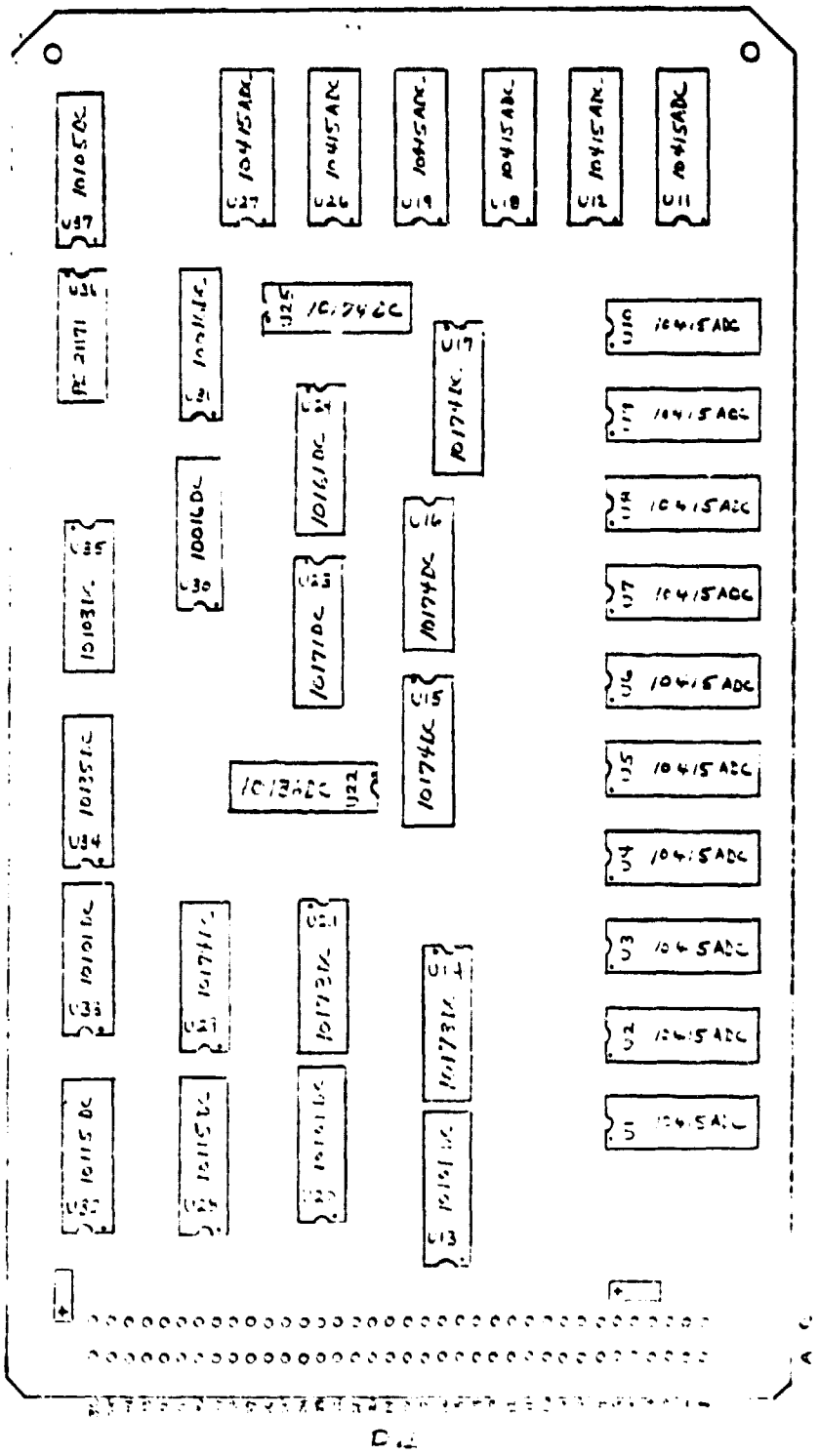


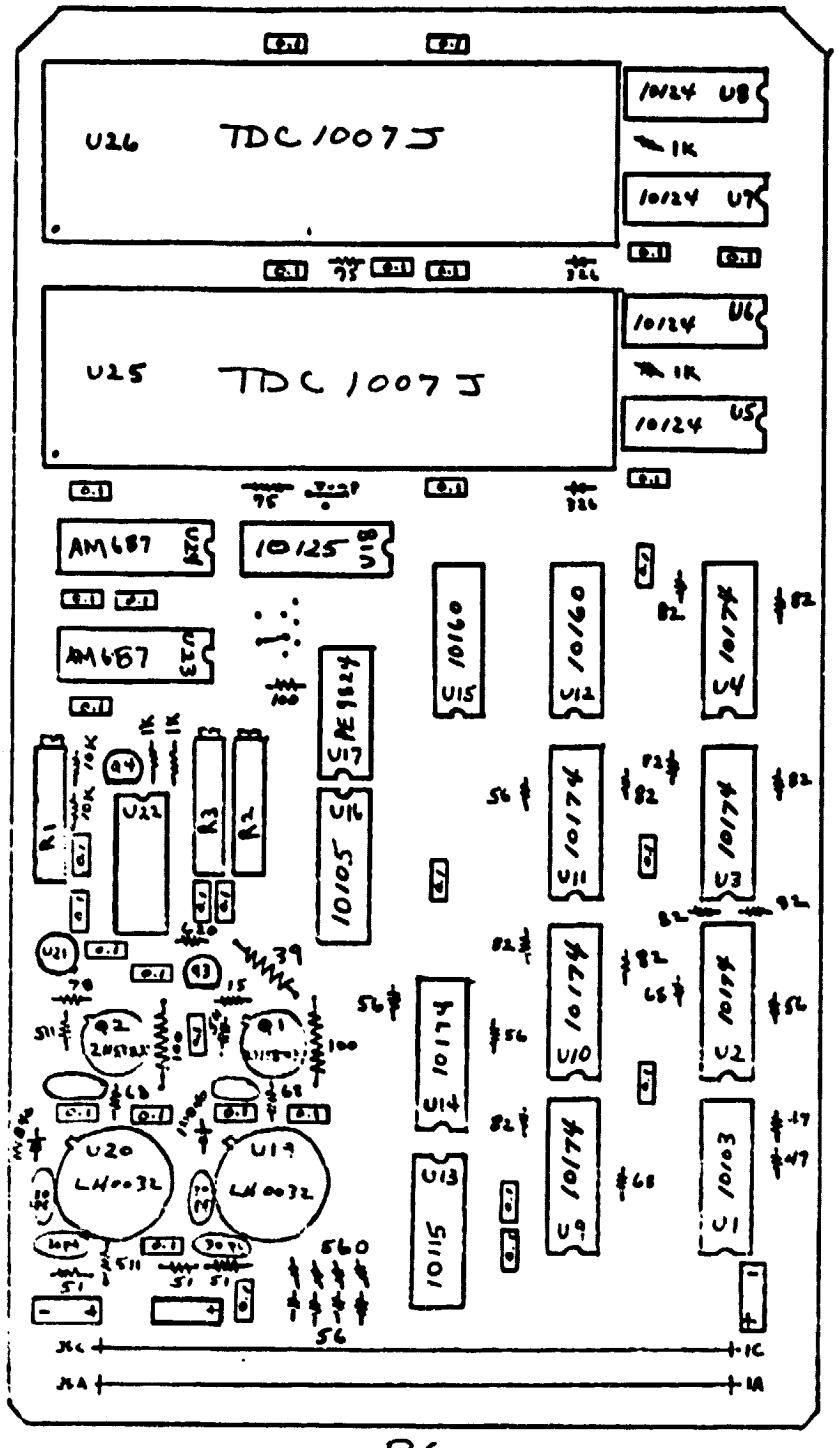
FIGURE A-3
VIDEO MEMORY BOARD NO. 4

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. N00039-15217-4	2. Code (Agency)	3. PL	4. Revision Ltr. Date
5. List Title: Video A/D Board #6		6. Authentication:		7. Dev Auth No.	8. Sheet 1 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
U26, U25	2	ea.		TDC1007J	8-bit Monolithic Video A/D COnverter, TRW LSI Products
U20, U19	2	ea.		LH0032G	Ultra-Fast FET Operational Amplifier, National
U22	1	ea.		LM 124D	Quad Operational Amplifier, Fairchild
U13	1	ea.		10115D	Quad ECL Line Receiver, Fairchild
U17	1	ea.		9824	50 nsec Delay Line, 5 nsec taps, Pulse Engineering, Inc.
U18	1	ea.		10125D	Quad ECL-to-TTL Translator, Fairchild
U24, U23	2	ea.		AM687D	Dual ECL Voltage Comparator, Advanced Micro Devices
U16	1	ea.		10105D	Triple OR/NOR Gate, Fairchild
U5, U6, U7, U8	4	ea.		10124D	Quad TTL-to-ECL Translator, Fairchild
U12, U15	2	ea.		10160D	12-bit ECL Parity Generator, Fairchild
U2,U3,U4, U9,U10, U11,U14	7	ea.		10174D	Dual 4-to-1 Multiplexer, Fairchild
U1	1	ea.		10103D	Quad ECL OR Gate, Fairchild
U21	1	ea.		AD580SH	Three-terminal 2.5 V Reference, Analog Devices
Q1, Q2	2	ea.		2N5583	RF PNP Transistor, Motorola
Q3, Q4	2	ea.		2N4403	PNP Transistor, Motorola
C1, C2 C3, C4					
C5, C6	6	ea.			Selected Silver Mica Capacitor
C7,C8,C9	3	ea.			33 μF, 25 V Tantalum Capacitor
R1,R2,R3	3	ea.			1 kΩ Cermet Trimpot, Dale Series #784
none					0.1 μF, 50 V, Radial Leads, Ceramic Capacitor

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code (Agency)	3. PL	4. Revision Ltr. Date
5. List Title: Video A/D Board #6		6. Authentication:		7. Rev Auth No.	8. Sheet 2 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Identif. Number	14. Nomenclature or Description
R4, R19	2	ea.			51 Ω, 1/4 W, 5% resistor
R5, R 6					
R20, R18	4	ea.			511 Ω, 1/4 W, 1% resistor (see note 5)
R7, R21	2	ea.			6.8 Ω, 1/4 W, 5% resistor
R8, R22	2	ea.			100 Ω, 1/2 W, 5% resistor
R10, R23	2	ea.			Selected 1/4 W, 5% resistor
R13, R17					
R15	3	ea.			1 kΩ, 1/4 W, 5% resistor
R11, R12	2	ea.			10 kΩ, 1/4 W, 5% resistor
R9, R24	2	ea.			75 Ω, 1/4 W, 5% resistor
R14	1	ea			560 Ω, 1/4 W, 5% resistor
R16	1	ea			39 Ω, 1/2 W, 5% resistor
D1, D2					
D3, D4	4	ea.			5082-2800, Schottky Diode, Hewlett-Packard
none					assorted 47 Ω - 560 Ω, 1/4 W, 5%, as marked on schematic
P6	1	ea.		3612056-01	72-pin Right-Angle Plug, MUPAC, Inc.
	1	ea.			4.5 × 7.5, 4-layer Printed Circuit Board, ARL:UT



P6

FIGURE A-4

VIDEO A/D BOARD NO. 6

AE-80-106

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code (Agency)	3. PL	4. Revision Ltr. Date
5. List Title: RPE FORMATTING BOARD BOARD NO. 8		6. Authentication:	7. Rev Auth No.		8. Sheet 1 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
UD1, UD2 UD9, UD10 UE2, UF2 UF3, UF4 UF5, UF6 UF7, UH1	12	ea		SNC54LS365AJ	Hex Bus Buffer/Driver with 3-state outputs, Texas Instruments
UE9	1	ea		AM25LS153 DM	Dual 4-to-1 Multiplexer, Advanced Micro Devices
UF9, UF10 UG2, UG5 UG6, UG7 UG10,UH2 UH3, UH4 UH5, UH6 UH9	13	ea		AM25LS161 DM	4-Bit Synchronous Counter, Advanced Micro Devices
UG3, UG4	2	ea		AM25LS174 DM	6-Bit D Flip-Flop, Advanced Micro Devices
UF1, UG1	2	ea		4116R-002-202	Resistor Network, 2.0 kΩ, 15 resistors with one common pin, Bourns
UE3, UE4 UE5, UE6 UE7, UE8	6	ea		SN54LS165J	Parallel Load 8-Bit Shift Register, Texas Instruments
UE10,UF8	2	ea		SN54S288J	32 x 8 PROM with 3-state Output, TEXAS INSTRUMENTS
UG8	1	ea		SN54LS138J	3-to-8 Decoder, Texas Instruments
UH8	1	ea		SN54LS04J	Hex Inverter, Texas Instruments
UJ3	1	ea		SN54LS00J	Quad NAND Gate, Texas Instruments
UG9, UJ2 UJ9	3	ea		SN54LS109AJ	Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop, Texas Instruments

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. MDA9-15217-4	2. Code (Agency)	3. FSL	4. Revision Ltr. Date
5. List Title: RPE FORMATTING BOARD (BOARD NO. 8)		6. Authentication:		7. Rev Auth No.	8. Sheet 2 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
UJ4	1	ea		SN54LS123J	Dual Retriggerable One-Shot, TEXAS INSTRUMENTS
UJ5	1	ea		SN54121J	One-shot with Schmitt Trigger Input, TEXAS INSTRUMENTS
UH10	1	ea		SN54LS112J	Dual J-K Negative Edge-Triggered Flip-Flop, TEXAS INSTRUMENTS
UE1, UH7	2	ea		AM25LS1640M	8-bit Serial-in, Parallel-out Shift Register, ADVANCED MICRO DEVICES
UD3, UD4 UD5, UD6 UD7, UD8 UJ8	7	ea		AM26LS32DC	Quad Differential Line Receiver, ADVANCED MICRO DEVICES
UJ6	1	ea		AM26LS31DM	Quad Differential Line Driver, ADVANCED MICRO DEVICES
UJ10, UJ	2	ea		SN54LS02J	Quad NOR Gate, TEXAS INSTRUMENTS
R1, R2	2	ea		RCR07-184	Resistor, 180 kΩ, 5%, 1/4 W
R3, R4	2	ea		RCR07-122	Resistor, 1.2 kΩ, 5%, 1/4 W
R5, R6	2	ea		RCR07-121	Resistor, 120 Ω 5%, 1/4 W
R7	1	ea		RCR07-221	Resistor, 220 Ω, 5%, 1/4 W
C1, C2	2	ea		CSR13G226KM	Capacitor, 22 μF, Tantalum
C3	1	ea		CMFD470J0	Capacitor, 47 pF, DIP MICA, 5%
BYPASS CAPS	25	ea		1802-Z5U050A104M	Capacitor, 0.1 μF, GREEN GODDESS , VARADYNE
BYPASS CAPS	4	ea		CSR13G476KM	Capacitor, 47 μF, Tantalum
Board #8	1	ea		3234806-01	Wire-Wrap Board, MUPAC, Inc.
Connector	1	ea		3612061-01	Connector, 108 pin, MUPAC, Inc.

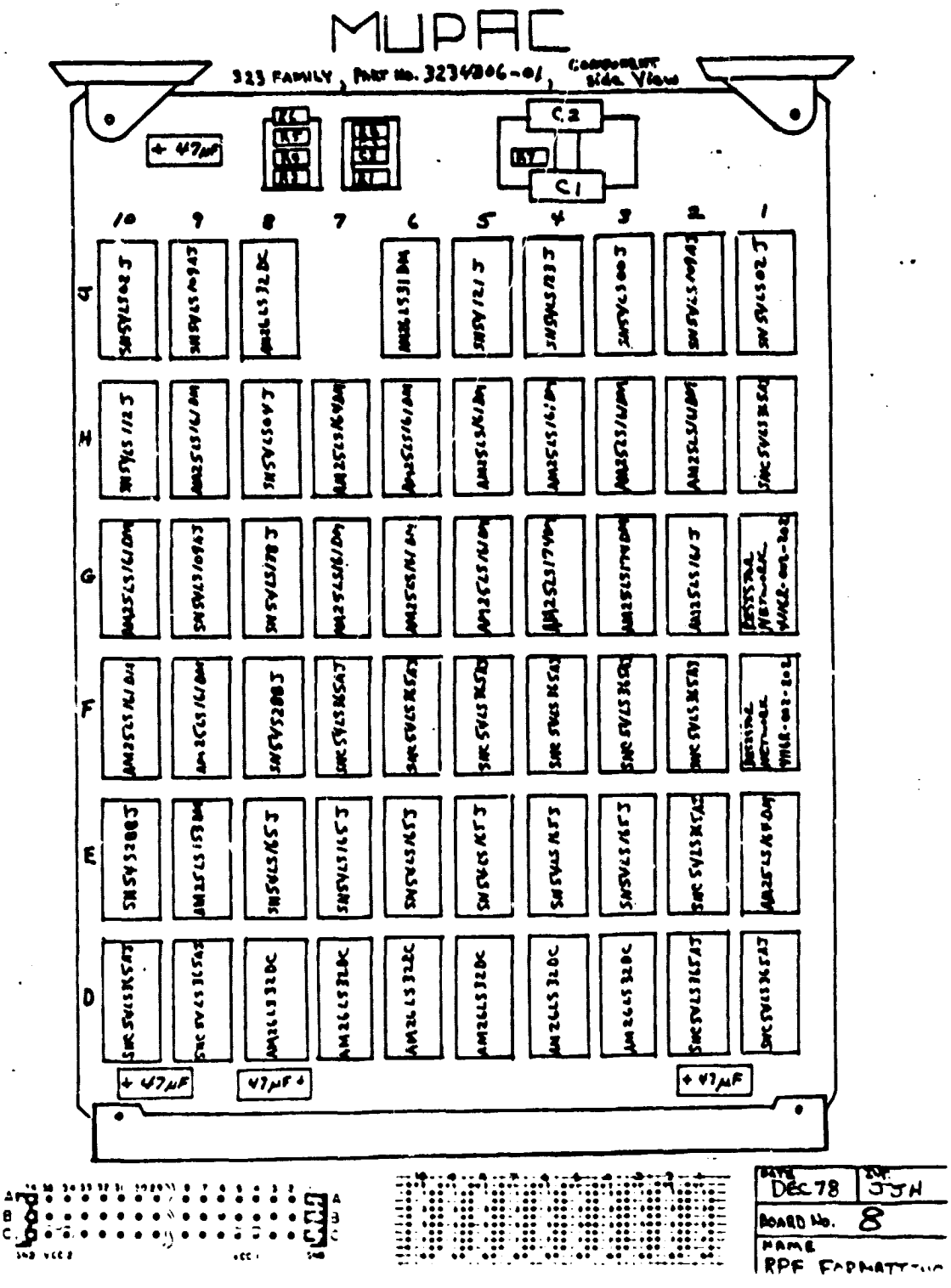


FIGURE A-5

RPE FORMATTING BOARD NO. 8

AE-80-107

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code Ident.	3. PL	4. Revision Ltr. Date
5. List Title: CLOCK GENERATOR BOARD #9		6. Authentication:		7. Rev Auth No.	8. Sheet 1 of 2 Sheets

9. Item or Find Number	10. Qty Eqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
U7	1	ea.		10105	Triple OR/NOR Gate, Fairchild
U5, U11, U16, U21	4	ea.		10115	Quad Line Receiver, Fairchild
U4,U8U13	3	ea.		10016	Hexadecimal Counter, Fairchild
U10, U20	2	ea.		10010	Decimal Counter, Fairchild
U2, U14	2	ea		10131	Dual D Flip-Flop, Fairchild
U9	1	ea		10135	Dual J-K Flip-Flop, Fairchild
U3, U19	2	ea.		10102	Quad NOR Gate, Fairchild
U18	1	ea.		10107	Triple Exclusive OR/NOR Gate, Fairchild
U17	1	ea.		10101	Quad OR/NOR Gate, Fairchild
U23	1	ea.		MC12040	Phase-Detector, Motorola
U12	1	ea.		MC1648	Voltage Controlled Oscillator, Motorola
U24	1	ea.		AM687A	Voltage Comparator, Advanced Micro Devices
U22	1	ea.		LM0032	FET-input Operational Amplifier, National
U15	1	ea.		LX560CA	Temperature Transducer, National Semiconductor
U1	1	ea.		LX1602A	Pressure Transducer, National Semiconductor
U6	1	ea.		PE-9824	Delay Line, 50 nsec, 5 nsec taps, Pulse Engineering, Inc.
	1	ea.		N/A	4.5 x 7.5 4-layer Printed Circuit Board, ARL:UT
P9	1	ea.		3612056-01	72-pin Right Angle Plug with Solder Connectors, AUPAC, Inc.
R1, R2	2	ea.			Resistor, 8.2 kΩ, 1/8 W, 5%
R3	1	ea.			Resistor, 27 kΩ , 1/8 W, 5%
R4	1	ea.			Resistor, 100Ω , 1/8 W, 5%
R5	1	ea.			Resistor, 1.0 kΩ , 1/8 W, 5%
R6, R7	2	ea.			Resistor, 27Ω , 1/4 W, 5%
None	32	ea.			Resistor, 82Ω , 1/8 W, 5%

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code (Agency)	3. PL	4. Revision Ltr. Date
5. List Title: CLOCK GENERATOR BOARD #9		6. Authentication:	7. Doc Auth No.		8. Sheet 2 of 2 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
R7	1	ea.			Resistor, 47 Ω, 1/4 W, 5%
R8	1	ea.			Resistor, 910 kΩ, 1/4 W, 5%
None	1	ea.			Resistor, 91 Ω, 1/8 W, 5%
None	6	ea.			Resistor, 68 Ω, 1/8 W, 5%
None	2	ea.			Resistor, 47 Ω, 1/8 W, 5%
None	2	ea.			Resistor, 62 Ω, 1/4 W, 5%
None	12	ea.			Resistor, 510 Ω, 1/4 W, 5%
None	12	ea.			Resistor, 56 Ω, 1/4 W, 5%
C1	1	ea.			Capacitor, 1 mF, Dipped Mica
C11, C2	2	ea.			Capacitor, 0.1 μF, Ceramic
C3	1	ea.			Capacitor, 5000 pF, Polystyrene
C4, C5					
C6	3	ea.			Capacitor, 0.01 F, Polycarbonate
C7	1	ea.			Capacitor, Selected, Dipped Mica
C8	1	ea.			Capacitor, Selected, Dipped Mica
C9	1	ea.			Capacitor, Selected, Dipped Mica
C10	1	ea.			Capacitor, Selected, Dipped Mica
None	11	ea.			Capacitor, 0.1 μF, Ceramic Bypass
None	3	ea.		CSR13G226KM	Capacitor, 22 μF, Tantalum
D1	1	ea.		HP-82-2814	Matched Quad Schottky Diode Bridge, Hewlett-Packard
D2, D3					
D4, D5	4	ea.		1N940	DIODE
D6	1	ea.		1N 5468A	Voltage-Variable Capacitance (Varactor) Diode, Motorola
L1	1	ea.			Inductor, 3 turns, 16 gauge wire

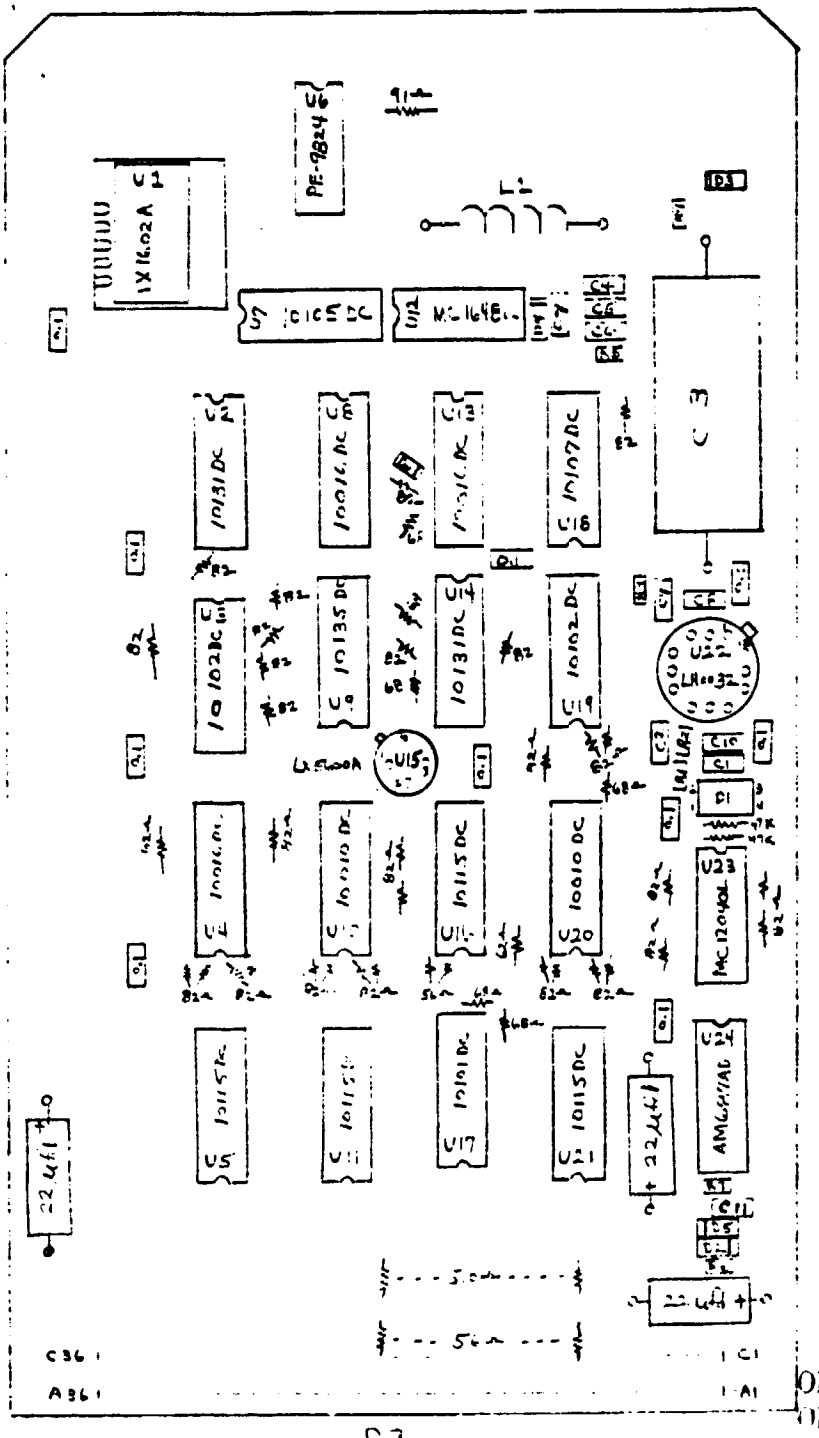


FIGURE A-6

CLOCK GENERATOR BOARD NO. 9

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code Ident.	3. PL	4. Revision Ltr. Date
5. List Title: VIDEO FORMATTING BOARD (BOARD NO. 11)		6. Authentication:		7. Rev Auth No.	8. Sheet 1 of 2 Sheets

9. Item or Find Number	10. Qty Rqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
UD5, UG6	6	ea.		SN54LS109AJ	Dual J-$\bar{K}$ Positive-Edge Triggered, Flip-Flop, Texas Instruments
UG7, UG8					
UG9, UG10					
UE5, UE7	9	ea.		SN54LS112J	Dual J-K Negative-Edge Triggered, Flip-Flop, Texas Instruments
UE8, UE9					
UE10,UH7					
UH8,UH9					
UH10					
UF8, UF9	2	ea.		AM25LS157DM	Quad 2-Input Multiplexer, ADVANCED MICRO DEVICES
UE6, UD6	6	ea.		AM26LS31DM	Quad Differential Line Driver, ADVANCED MICRO DEVICES
UD7, UD8					
UD9,UD10					
UJ7	1	ea.		SN54LS30J	8-Input Positive NAND Gate, Texas Instruments
UJ8, UJ9	2	ea.		SN54LS123J	Dual Retriggerable, Monostable Multivibrators with Clear, Texas Instruments
UE4	1	ea.		SN54LS04J	Hex Inverters, Texas Instruments
UJ3	1	ea.		AM25LS174DM	6-Bit Register with Common Clear, ADVANCED MICRO DEVICES
UD1, UD2	10	ea.		SN54LS165J	Parallel-Load, 8-Bit, Serial Shift Register, Texas Instruments
UE1, UE2					
UF1, UF2					
UG1, UG2					
UJ6, UH6					
UE3, UF3					
UH1, UH2					
UH3, UJ1 UJ2	7	ea.		AM25LS164DM	8-Bit, Serial-In, Parallel-Out Shift Register, ADVANCED MICRO DEV

PARTS LIST	1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS	1A. Contract No. NAS9-15217-4	2. Code (Army)	3. PL	4. Revision Ltr. Date
5. List Title: VIDEO FORMATTING BOARD (BOARD NO. 11)		6. Authentication:		7. Rev Auth No.	8. Sheet 2 of 2 Sheets

9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description
UH4, UH5					
UJ4, UJ5	4	ea.		AM25LS153DM	Dual 4-Input Multiplexer, ADVANCED MICRO DEVICES
UD3, UD4					
UG3, UG4					
UG5, UG6	6	ea.		AM25LS161DM	Synchronous 4-Bit Binary Counter, Asynchronous Clear, ADVANCED MICRO DEVICES
UF5	1	ea.		SN54LS37J	Quad 2-Input Positive NAND Buffers, Texas Inst.
UF7, UF10					
UJ10	3	ea.		SN54LS02J	Quad 2-Input Positive NOR Gates, Texas Inst.
UF4	1	ea.		L13E	DIP Crystal Oscillator, 3.84 MHz, Conner-Winfield Corp.
C1	1	ea.			Capacitor, 1 μF
C2	1	ea.			Capacitor, 0.082, Tantalum
C3, C4	2	ea.			Capacitor, 12 μF, Tantalum
R1, R2					
R3, R4	4	ea.		RCR07-184	Resistor, 180 kΩ, 1/4 W, 5%
Board No. 11	1	ea.		3234806-01	Panel (Wire Wrap Board) Mfg. MUPAC, Inc.
P11	1	ea.		3612061-01	108-Pin Plug, MUPAC, Inc.
BYPASS CAPS	25	ea.			Capacitor, 0.1 μF, Ceramic (Green Goddess) VARADYNE
BYPASS CAPS	2	ea.			Capacitor, 47 μF, Tantalum

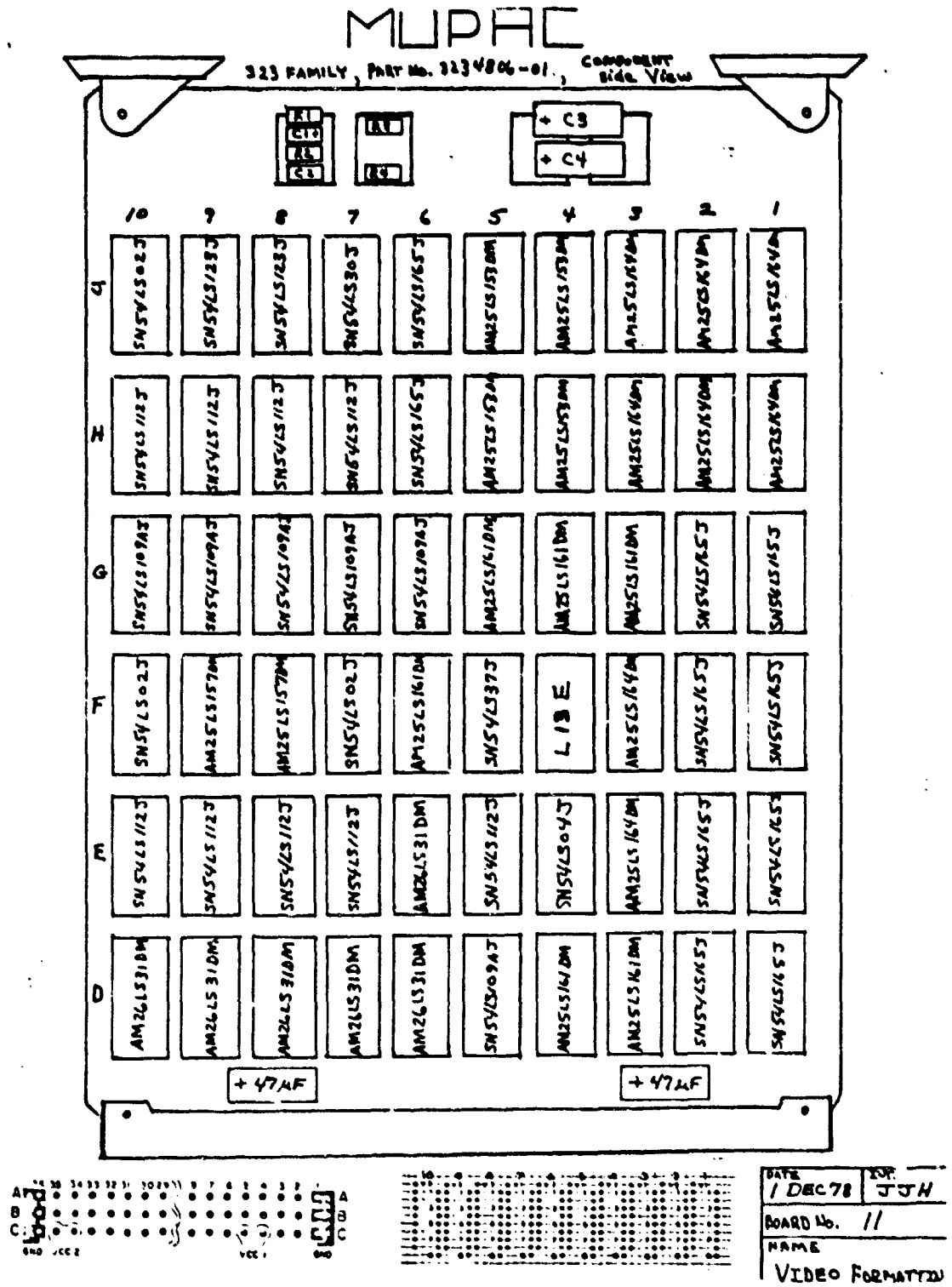


FIGURE A-7

VIDEO FORMATTING BOARD NO. 11

AE-80-109

APPENDIX B

DIGITAL DATA RECORDING SYSTEM
ACCEPTANCE PROCEDURE

DIGITAL DATA RECORDING SYSTEM
ACCEPTANCE PROCEDURE

STANDARD CONFIGURATION

1. Data precision - 7 bit
2. Sample Interval - 70 nsec
3. Range Delay - 2 μsec
4. Ramp Function - 1 V pp

1-30 ..

TEST 1. DATA PRECISION SELECTION

1. Set Standard Configuration

   a. Data Precision - 7 bit 7 BIT

   b. Sample Interval - 70 nsec 70×10^{-9} SEC

   c. Range Delay 2 μsec 2 MSEC

   d. Ramp Function (1 Vpp) - 900 KHZ

2. Set and Record Identifying word in RPE Data

   Identifier word set 000

   Identifier word observed 000

3. Record and view data for 7-, 4-, and 2-bit precision 7 BIT

4. On print out verify proper operation of the recorded signals.

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

1-30-79

L270

TEST 1. DATA PRECISION SELECTION (Cont'd)

5. Verify Proper RPE Words

Observed

Data Precision 7 BIT

Sample Interval 76.4 MSEC

Range Delay 1.93 MSEC

Heading 000

Temp 1 28.64 °C

2 27.15

3 X (NC)

4 19.24

Negative Volt 5.7 -5.75

DDRS ~~Negative~~ POSITIVE Volt 5 5.04

Negative Volt 2 -2.07

AUX Positive Volt 5 4.98

Negative Volt 15 -15.05

1-30-79

TEST 1. DATA PRECISION SELECTION

1. Set Standard Configuration

   a. Data Precision - 4 bit 4 BIT

   b. Sample Interval - 70 nsec ✓

   c. Range Delay 2 μsec ✓

   d. Ramp Function (1 Vpp) - 450 KHz

2. Set and Record Identifying word in RPE Data

   Identifier word set 001

   Identifier word observed 001

3. Record and view data for 7-, 4-, and 2-bit precision 4 BIT

4. On print out verify proper operation of the recorded signals.

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

1-30-79

270

TEST 1. DATA PRECISION SELECTION (Cont'd)

5. Verify Proper RPE Words

Observed

Data Precision 4 BIT

Sample Interval 70.4 MSEC

Range Delay 1.93 MSEC

Heading _____

Temp 1 29.03 °C

2 28.21

3 NC

4 19.58

Negative Volt 5.7 -5.75

DDRS ~~Negative~~ POSITIVE Volt 5 5.04

Negative Volt 2 -2.07

AUX Positive Volt 5 4.98

Negative Volt 15 -15.05

1-30-79

TEST 1. DATA PRECISION SELECTION

1. Set Standard Configuration

   a. Data Precision - 2 bit 2 BIT

   b. Sample Interval - 70 nsec ✓

   c. Range Delay 2 μsec ✓

   d. Ramp Function (1 Vpp) - 225 KHZ

2. Set and Record Identifying word in RPE Data

   Identifier word set 002

   Identifier word observed 002

3. Record and view data for 7-, 4-, and 2-bit precision 2 BIT

4. On print out verify proper operation of the recorded signals.

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

1-30-79

TEST 1. DATA PRECISION SELECTION (Cont'd)

HFP

5. Verify proper RPE words

Observed

Data Precision 2 BIT

Sample Interval 70.4 μSEC

Range Delay 1.93 μSEC

Heading

Temp 1 29.22 °C

2 28.61

3 NC

4 19.64

Negative Volt 5.7 -5.75

DDPS ~~Negative~~ POSITIVE Volt 5 +5.04

Negative Volt 2 -2.07

AUX Positive Volt 5 +4.98

Negative Volt 15 -15.05

1-30-79

PULSE NO. 1

⊙ - Range Bins 16-31
7-bit data Horizontal

⊡ - Range Bins 32-63
4-bit data Vertical

X - 2-bit data Vertical

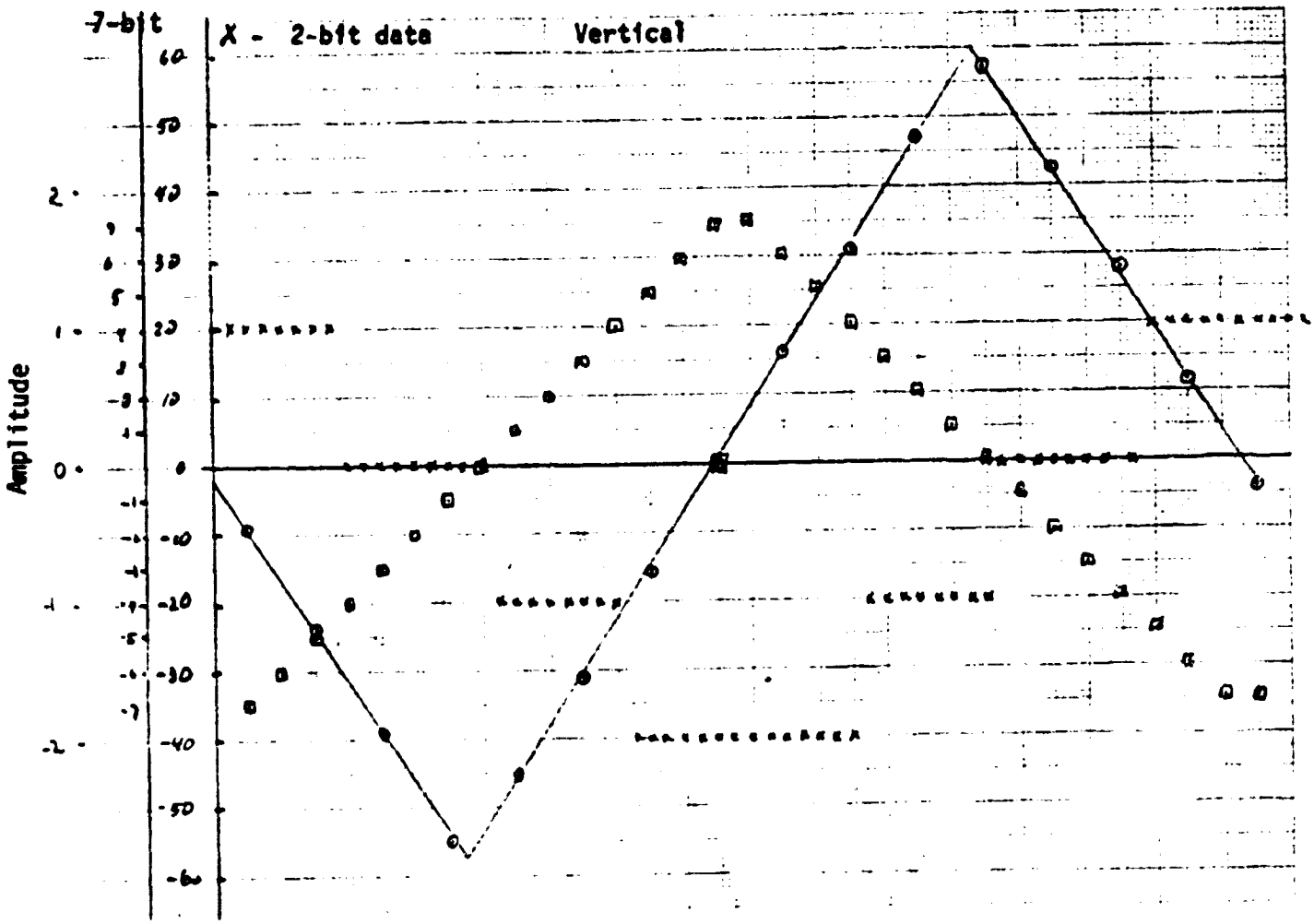


FIGURE B-1

DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVEFORM INPUT

1-30-79

Test 000

70 nsec Sample Interval

7-bit Data Precision

—⊙— Horizontal Channel

--⊡-- Vertical Channel

Pulse 1, Range Bins 16-31

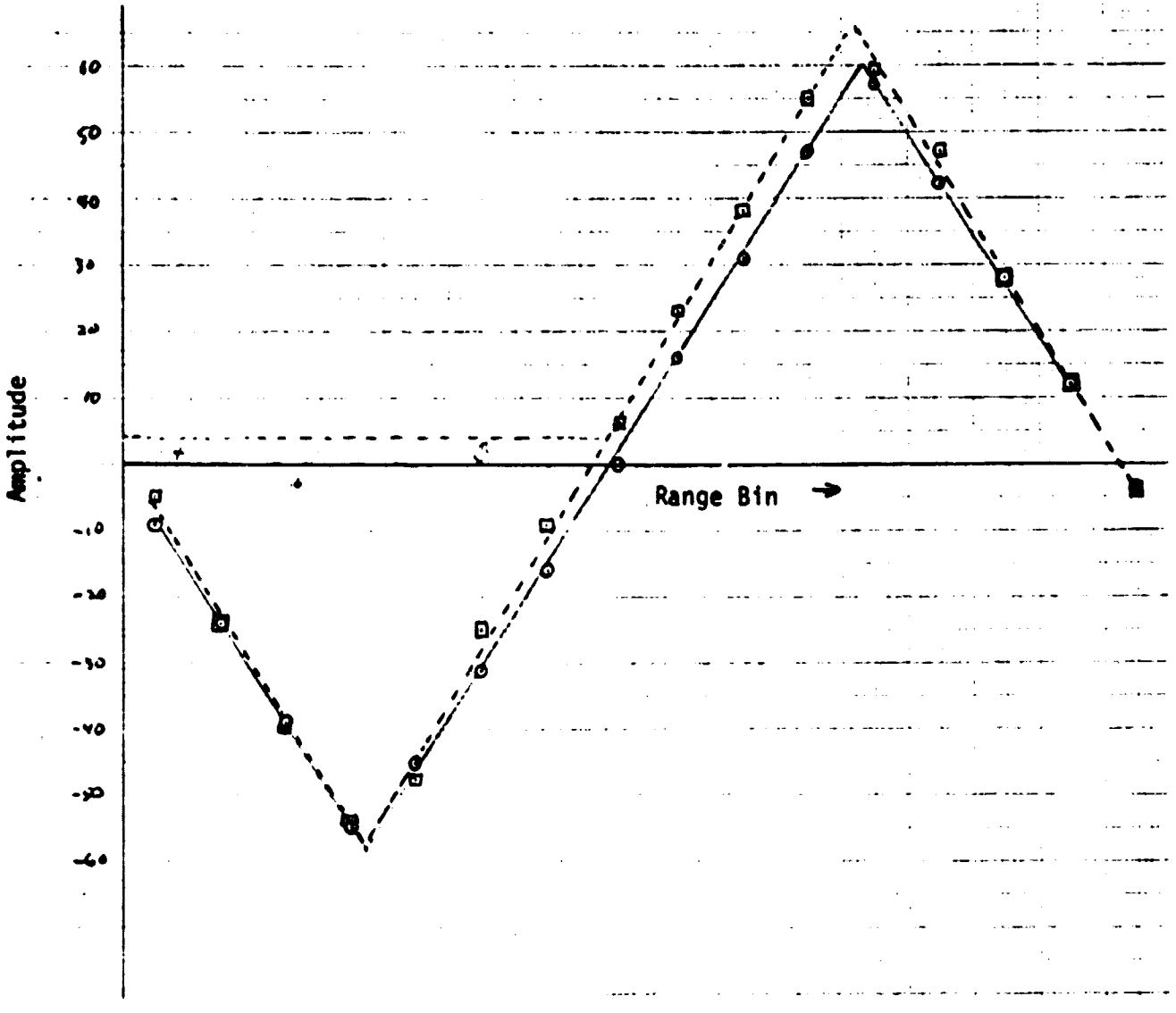


FIGURE B-2

DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVEFORM INPUT

Test 000

70 nsec

7-bit Data

Pulse 21, Range Bins 16-31

Arrows identify parity error indications

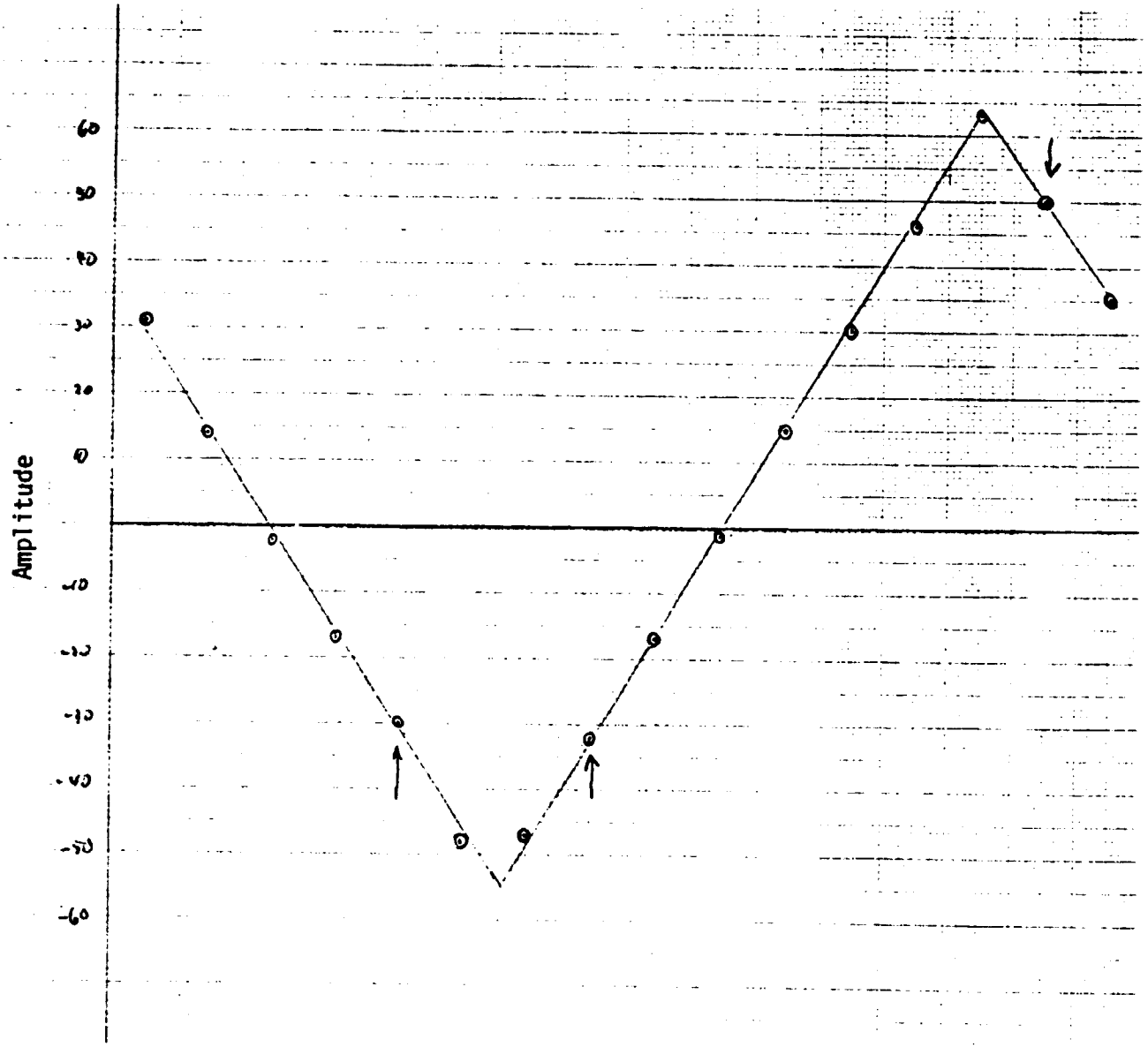


FIGURE B-3

DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVEFORM INPUT

AE-80-112

1-30-79

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7-BIT b. _____ c. 2 μSEC d. RAMP - 514 KHZ

2. Set and Record Identifying Word in RPE Data

   Identifier word set 003

   Identifier word observed 003

   LFP

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
40 μ SEC	42 μ SEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin _____	Range Bin _____	Range Bin _____

TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd)

5. Verify proper RPE words

LFP

Observed

Data Precision 7 BIT

Sample Interval 40.2 mSEC

Range Delay 1.93 μSEC

Heading _____

Temp 1 27.03 °C

2 26.51

3 NC

4 19.27

Negative Voltage 5.7 -5.75

DDRS ~~Negative~~ Positive Voltage 5 +5.04

Negative Voltage 2 -2.06

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.05

1-30-79

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7 BIT b. _____ c. 2 μSEC d. RAMP - 642 KHZ

2. Set and Record Identifying Word in RPE Data

   Identifier word set 004

   Identifier word observed 004

   IFP

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
50 μ SEC	52.5 μ SEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd) 1-30-79

5. Verify proper RPE words

Observed

Data Precision 7 BIT

Sample Interval 50.31 mSEC

Range Delay 1.93 μSEC

Heading _____

Temp 1 27.61 °C

2 27.03

3 NC

4 19.58

Negative Voltage 5.7 -5.75

DDRs ~~Negative~~ POSITIVE Voltage 5 +5.04

Negative Voltage 2 -2.07

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

1-30-79

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7 BIT b. _____ c. 2 μ SEC d. RAMP - 77 KHZ

2. Set and Record Identifying Word in RPE Data

   Identifier word set 005

   Identifier word observed 005

   LFO

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
60 n SEC	63 n SEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin _____	Range Bin _____	Range Bin _____

TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd) 1-30-79

5. Verify proper RPE words

Observed

Data Precision 7 BIT

Sample Interval 60.37 m SEC

Range Delay 1.93 μ SEC

Heading _____

Temp 1 27.85 °C

2 27.36

3 NC

4 19.67

Negative Voltage 5.7 -5.75

DDPS ~~Negative~~ POSITIVE Voltage 5 +5.04

Negative Voltage 2 -2.07

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

TEST 2. SLANT RANGE SAMPLE INTERVAL 1-30-79

1. Set Standard Configuration a. 7 BIT b. _____ c. 2 μSEC d. RAMP - 900KHz

2. Set and Record Identifying Word in RPE Data

   Identifier word set 006

   Identifier word observed 006

   I2 FP

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
70 nSEC	73.5 nSEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd)

1-30-79

5. Verify proper RPE words

LTP

Observed

Data Precision 7 BIT

Sample Interval 70.4 m SEC

Range Delay 1.93 μ SEC

Heading _____

Temp 1 27.97 °C

2 27.57

3 NC

4 19.79

Negative Voltage 5.7 -5.75

ODRS ~~Negative~~ POSITIVE Voltage 5 +5.04

Negative Voltage 2 -2.07

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

TEST 2. SLANT RANGE SAMPLE INTERVAL 1-30-79

1. Set Standard Configuration a. 7 BIT b. _____ c. 2 μSEC d. RAMP - 1028 KHz

2. Set and Record Identifying Word in RPE Data

   Identifier word set 007

   Identifier word observed 007

   1770

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
80 n SEC	84 n SEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd)

1-30-79

5. Verify proper RPE words

Observed

Data Precision 7 BIT

Sample Interval 80.49 m SEC

Range Delay 1.93 μ SEC

Heading _____

Temp 1 28.18°C

2 27.85

3 NC

4 19.88

Negative Voltage 5.7 -5.75

DDRS ~~Negative~~ POSITIVE Voltage 5 +5.04

Negative Voltage 2 -2.07

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

1-30-79

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7 BIT b. _____ c. 2 μSEC d. RAMP - 1157 KHz

2. Set and Record Identifying Word in RPE Data

   Identifier word set 008

   Identifier word observed 008

   ATP

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
90 n SEC	93 n SEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin _____	Range Bin _____	Range Bin _____

5. Verify proper RPE words

Observed

Data Precision 7 Bit

Sample Interval 90.55 μSEC

Range Delay 1.93 μ SEC

Heading _____

Temp 1 28.55 °C

2 28.49

3 NC

4 20.03

Negative Voltage 5.7 -5.75

DDRS ~~Negative~~ POSITIVE Voltage 5 +5.04

Negative Voltage 2 -2.08

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

TEST 2. SLANT RANGE SAMPLE INTERVAL 1-30-79

1. Set Standard Configuration a. 7 Bit b. _____ c. 4 μSEC d. RAMP - 1285 KHz

2. Set and Record Identifying Word in RPE Data

   Identifier word set 009

   Identifier word observed 009

   LFP

3. Verify proper sample interval using scope

Selected Sample Interval	Observed Sample Interval
100 nSEC	104 nSEC

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

   List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin

TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd) 1-30-79

5. Verify proper RPE words

Observed

Data Precision 7 BIT

Sample Interval 100.6 MSEC

Range Delay 1.93 μSEC

Heading _____

Temp 1 28.67°C

2 28.82

3 NC

4 20.07

Negative Voltage 5.7 -5.75

ODRS ~~Negative~~ POSITIVE Voltage 5 +5.04

Negative Voltage 2 -2.08

AUX Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

MTP

1-30-79

TEST 3. RANGE DELAY TEST

1. Set Standard Configuration a. 7 BIT b. 70 MSEC c. _____ d. RAMP 900-KHz

2. Set and Record Identifying word in RPE data

   Identifier word set 010

   Identifier word observed 010

   GTP

3. Verify proper range delay using scope.

Selected Range Delay	Observed Range Delay
2 μ SEC	2 μSEC

4. Record and view data for 2, 30, 60, and 90 μsec range delay
   List and Plot Amplitudes for near, mid, and far Range bins.

Range Bin	Range Bin	Range Bin

TEST 3. RANGE DELAY TEST

1-30-79

5. Verify proper RPE words.

LFP

Observed

Data Precision 7 BIT

Sample Interval 70.4 mSEC

Range Delay 1.93 μSEC

Heading _____

Temp 1 20.88 °C

2 29.52

3 NC

4 20.28

Negative Volt 5.7 -5.75

DDRS ~~Negative~~ Positive Volt 5 +5.04

Negative Volt 2 -2.09

AUX Positive Volt 5 +4.98

Negative 15 -15.06

1-30-79

TEST 3. RANGE DELAY TEST

1. Set Standard Configuration a. 7 BIT b. 70 MSEC c. _____ d. RAMP - 900KHZ

2. Set and Record Identifying word in RPE data

   Identifier word set 011

   Identifier word observed 011

   GFP

3. Verify proper range delay using scope.

Selected Range Delay	Observed Range Delay
30 μ SEC	30 μ SEC

4. Record and view data for 2, 30, 60, and 90 μsec range delay
   List and Plot Amplitudes for near, mid, and far Range bins.

Range Bin	Range Bin	Range Bin

TEST 3. RANGE DELAY TEST 1-30-79

5. Verify proper RPE words.

Observed

Data Precision 7 BIT

Sample Interval 70.4 mSEC

Range Delay 28.97 μSEC

Heading

Temp 1 28.70 °C

2 29.43

3 NC

4 20.28

Negative Volt 5.7 -5.75

DDRS ~~Negative~~ POSITIVE Volt 5 +5.04

Negative Volt 2 -2.09

AUX Positive Volt 5 +4.98

Negative 15 -15.06

1-30-79

TEST 3. RANGE DELAY TEST

1. Set Standard Configuration a. 7 BIT b. 70 MSEC c. _____ d. RAMP-900KHZ

2. Set and Record Identifying word in RPE data

   Identifier word set 012

   Identifier word observed 012

GFP

3. Verify proper range delay using scope.

Selected Range Delay	Observed Range Delay
60 μSEC	60 μSEC

4. Record and view data for 2, 30, 60, and 90 μsec range delay
   List and Plot Amplitudes for near, mid, and far Range bins.

Range Bin	Range Bin	Range Bin

TEST 3. RANGE DELAY TEST

1-30-79

GFP

5. Verify proper RPE words.

Observed

Data Precision 7 BIT

Sample Interval 70.4 m SEC

Range Delay 57.95 μ SEC

Heading _____

Temp 1 28.64°C

2 29.31

3 NC

4 20.28

Negative Volt 5.7 -5.75

DDRS ~~Negative~~ Positive Volt 5 +5.04

Negative Volt 2 -2.09

AUX Positive Volt 5 +4.98

Negative 15 -15.06

TEST 3. RANGE DELAY TEST 1-30-79

1. Set Standard Configuration a. 7BIT b. 70 MSEC c. _____ d. RAMP - 900KHZ

2. Set and Record Identifying word in RPE data

   Identifier word set [redacted] 013 270

   Identifier word observed 013

3. Verify proper range delay using scope.

Selected Range Delay	Observed Range Delay
90 [redacted] μ SEC	90 μSEC

4. Record and view data for 2, 30, 60, and 90 μsec range delay
   List and Plot Amplitudes for near, mid, and far Range bins.

Range Bin	Range Bin	Range Bin

TEST 3. RANGE DELAY TEST 1-30-79

5. Verify proper RPE words.

Observed

Data Precision 7BIT 27P

Sample Interval 70.4 m SEC

Range Delay 86.93 μSEC

Heading _____

Temp 1 28.91°C

2 29.61

3 NC

4 20.34

Negative Volt 5.7 -5.75

DDRS ~~Negative~~ Positive Volt 5 +5.04

Negative Volt 2 -2.07

AUX Positive Volt 5 +4.98

Negative 15 -15.06

TEST 4. BAND WIDTH 1-30-79

1. Standard Configuration a. 7 BIT b. 70 MSEC c. 2 MSEC d. SINE WAVE
2. Using dc input observed and record DDRS output amplitude on scope 4.3 V P-P
3. Using 7.5 MHz sine wave input observe and record DDRS output amplitude on scope 4.2 V P-P
4. Using 15 MHz sine wave input observe and record DDRS output on scope 3.8 V P-P

The dc and 15 MHz values should be within 3 dB of 7.5 MHz value.

JZFP

17 MHZ - 3.7 V P-P
12.5 MHZ - 4.0 V P-P
10 MHZ - 4.1 V P-P
5 MHZ - 4.2 V P-P
2.5 MHZ - 4.2 V P-P
1 MHZ - 4.3 V P-P
50 KHZ - 4.4 V P-P

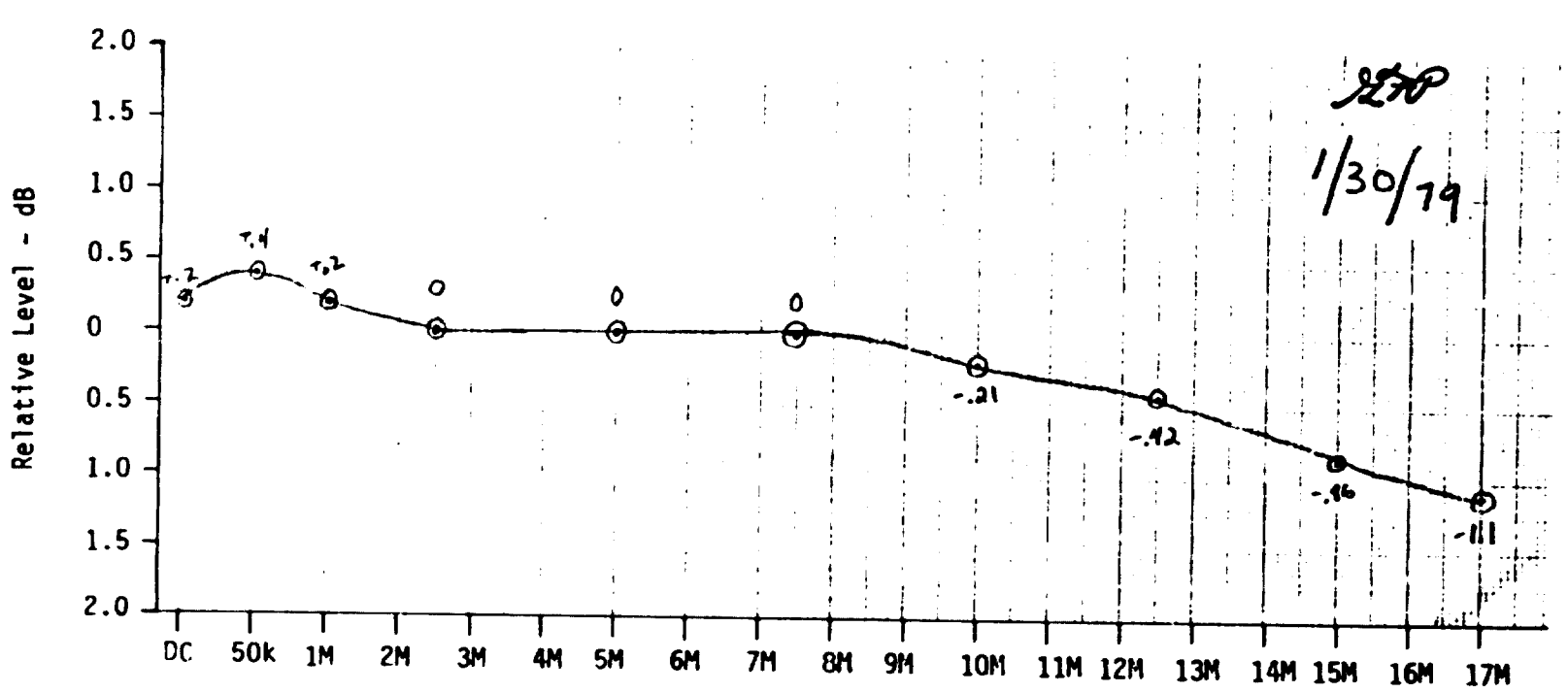


FIGURE B-4
DDRS FREQUENCY RESPONSE

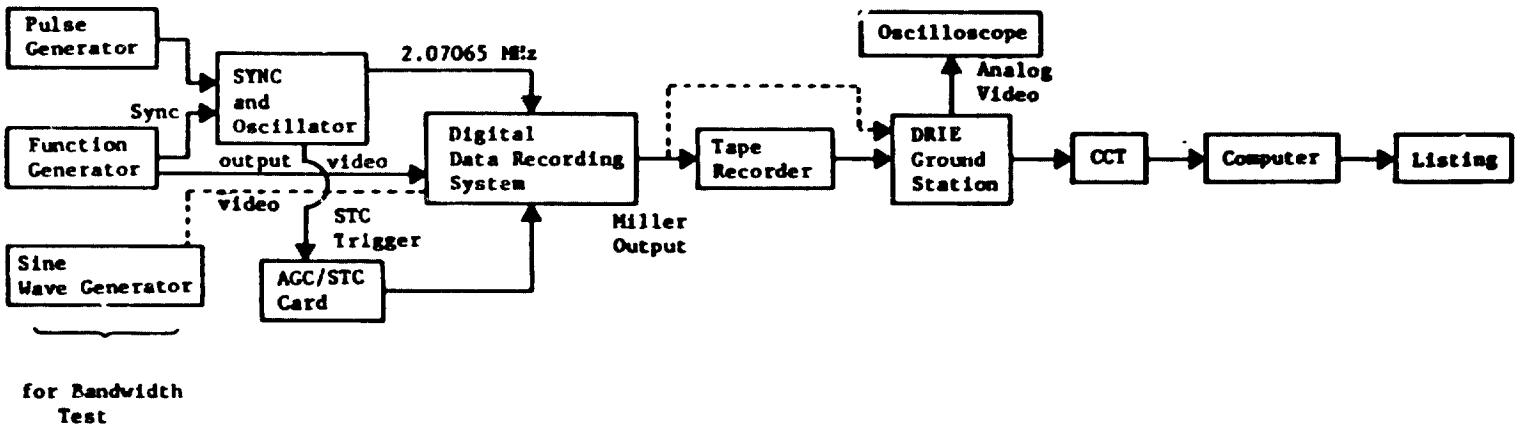


FIGURE B-5

DDRS ACCEPTANCE PROCEDURE BLOCK DIAGRAM

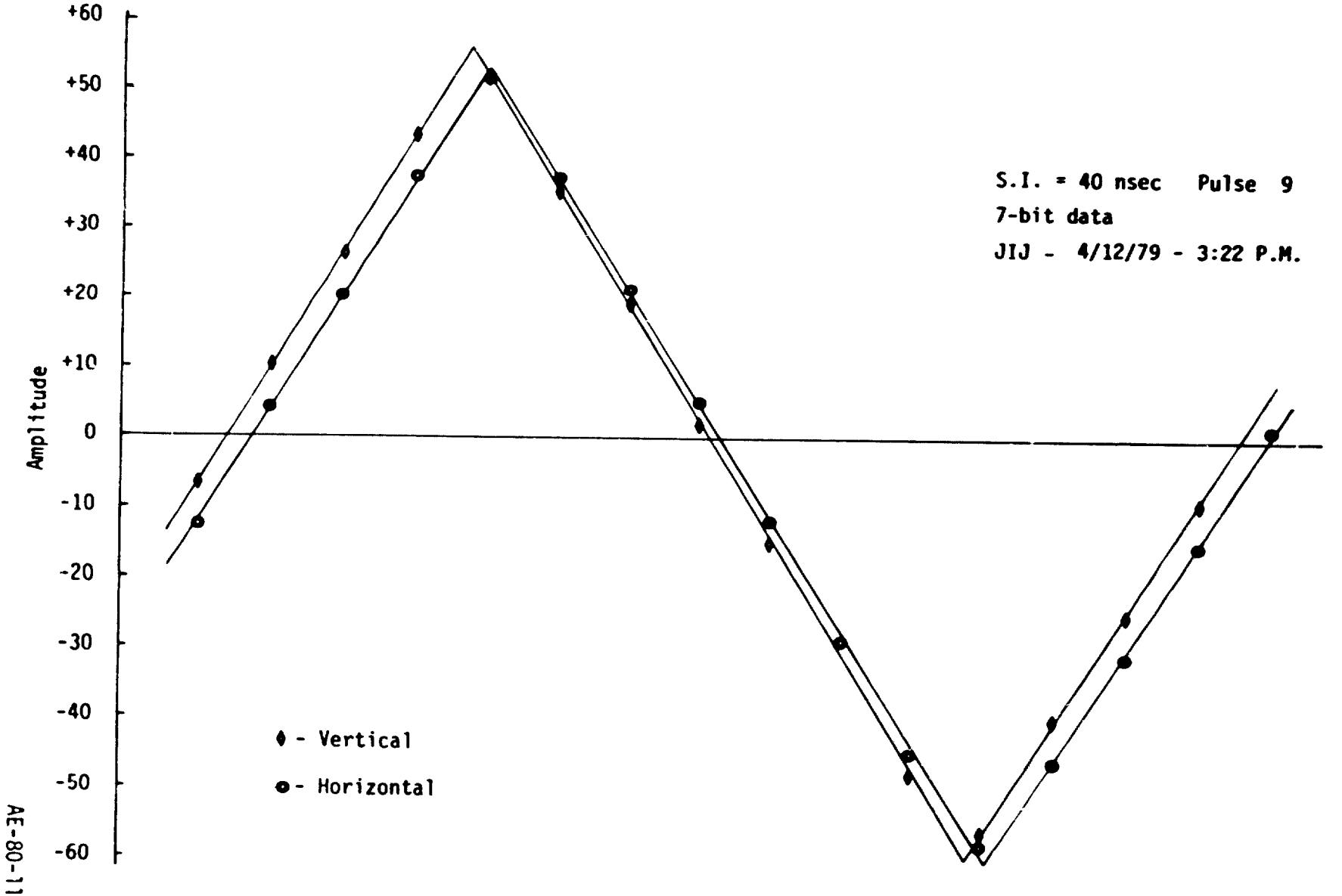


FIGURE B-6

DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVE FORM INPUT

(FINAL TEST OF DDRS)

APPENDIX C

CONTROL VALIDATION PROMS

TABLE C-1
VALID CONTROL SETTINGS

MODE	1	DELAYS 02 - 48	SI	040	DP	7
MODE	2	DELAYS 02 - 79	SI	040	DP	7
MODE	1	DELAYS 02 - 21	SI	040	DP	4
MODE	2	DELAYS 02 - 58	SI	040	DP	4
MODE	1	DELAYS 02 - 02	SI	040	DP	2
MODE	2	DELAYS 02 - 17	SI	040	DP	2
MODE	1	DELAYS 02 - 02	SI	040	DP	1
MODE	2	DELAYS 02 - 02	SI	040	DP	1
MODE	1	DELAYS 02 - 44	SI	050	DP	7
MODE	2	DELAYS 02 - 74	SI	050	DP	7
MODE	1	DELAYS 02 - 18	SI	050	DP	4
MODE	2	DELAYS 02 - 48	SI	050	DP	4
MODE	1	DELAYS 02 - 02	SI	050	DP	2
MODE	2	DELAYS 02 - 02	SI	050	DP	2
MODE	1	DELAYS 02 - 38	SI	060	DP	7
MODE	2	DELAYS 02 - 68	SI	060	DP	7
MODE	1	DELAYS 02 - 07	SI	060	DP	4
MODE	2	DELAYS 02 - 38	SI	060	DP	4
MODE	1	DELAYS 02 - 02	SI	060	DP	2
MODE	2	DELAYS 02 - 02	SI	060	DP	2
MODE	1	DELAYS 02 - 33	SI	070	DP	7
MODE	2	DELAYS 02 - 63	SI	070	DP	7
MODE	1	DELAYS 02 - 02	SI	070	DP	4
MODE	2	DELAYS 02 - 27	SI	070	DP	4
MODE	1	DELAYS 02 - 02	SI	070	DP	2
MODE	2	DELAYS 02 - 02	SI	070	DP	2
MODE	1	DELAYS 02 - 28	SI	080	DP	7
MODE	2	DELAYS 02 - 58	SI	080	DP	7
MODE	1	DELAYS 02 - 02	SI	080	DP	4
MODE	2	DELAYS 02 - 17	SI	080	DP	4
MODE	1	DELAYS 02 - 02	SI	080	DP	2
MODE	2	DELAYS 02 - 02	SI	080	DP	2
MODE	1	DELAYS 02 - 23	SI	090	DP	7
MODE	2	DELAYS 02 - 53	SI	090	DP	7
MODE	1	DELAYS 02 - 02	SI	090	DP	4
MODE	2	DELAYS 02 - 07	SI	090	DP	4
MODE	1	DELAYS 02 - 02	SI	090	DP	2
MODE	2	DELAYS 02 - 02	SI	090	DP	2
MODE	1	DELAYS 02 - 18	SI	100	DP	7
MODE	2	DELAYS 02 - 48	SI	100	DP	7
MODE	1	DELAYS 02 - 02	SI	100	DP	4
MODE	2	DELAYS 02 - 02	SI	100	DP	4
MODE	1	DELAYS 02 - 13	SI	110	DP	7
MODE	2	DELAYS 02 - 43	SI	110	DP	7
MODE	1	DELAYS 02 - 02	SI	110	DP	4
MODE	2	DELAYS 02 - 02	SI	110	DP	4
MODE	1	DELAYS 02 - 08	SI	120	DP	7
MODE	2	DELAYS 02 - 38	SI	120	DP	7
MODE	1	DELAYS 02 - 02	SI	120	DP	4
MODE	2	DELAYS 02 - 02	SI	120	DP	4
MODE	1	DELAYS 02 - 02	SI	130	DP	7
MODE	2	DELAYS 02 - 33	SI	130	DP	7
MODE	1	DELAYS 02 - 02	SI	130	DP	4
MODE	2	DELAYS 02 - 02	SI	130	DP	4
MODE	1	DELAYS 02 - 02	SI	140	DP	7
MODE	2	DELAYS 02 - 28	SI	140	DP	7
MODE	1	DELAYS 02 - 02	SI	140	DP	4
MODE	2	DELAYS 02 - 02	SI	140	DP	4
MODE	1	DELAYS 02 - 02	SI	150	DP	7
MODE	2	DELAYS 02 - 23	SI	150	DP	7
MODE	1	DELAYS 02 - 02	SI	150	DP	4
MODE	2	DELAYS 02 - 02	SI	150	DP	4
MODE						

TABLE C-2
BIT PATTERN PRINTOUT

CONTROL VALIDATION PROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	77	77	77	77	77	77	77	77	77	77	77	77	77	77	77	77
0010	77	77	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0020	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	F7
0030	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7
0040	F7	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0050	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0060	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0070	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	57	57	57
0080	57	57	57	57	57	57	57	57	57	57	57	57	57	57	57	56
0090	56	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7
00A0	D7	D7	D7	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6
00B0	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6
00C0	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	37	B7	B7	B7	B7	B7
00D0	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	17	97	75	75	75
00E0	75	75	75	75	75	75	75	75	75	75	75	75	75	75	75	74
00F0	74	74	74	74	74	74	74	74	74	74	74	74	74	74	74	74
0100	74	74	74	74	74	74	74	74	F5	F5	F5	F5	F5	F5	F5	F5
0110	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F4	F4	F4	F4	F4	F4
0120	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4
0130	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4
0140	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4
0150	F4	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0160	55	55	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5
0170	D5	D5	D5	D5	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4
0180	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4
0190	D4	35	B5	73	73	73	73	73	73	73	73	73	73	73	73	73
01A0	73	73	73	73	73	72	72	72	72	72	72	72	72	72	72	72
01B0	72	72	72	72	72	72	72	72	F3	F3	F3	F3	F3	F3	F3	F3
01C0	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F2	F2	F2	F2	F2	F2
01D0	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2
01E0	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2
01F0	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	33	53	53	53	53

TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0200	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3
0210	D3	D3	D3	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2
0220	D2	D2	D2	D2	D2	D2	33	B3	71	71	71	71	71	71	71	71
0230	71	71	71	71	71	71	71	71	71	71	70	70	70	70	70	70
0240	70	70	70	70	70	70	70	70	F1	F1	F1	F1	F1	F1	F1	F1
0250	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F0	F0	F0	F0	F0	F0
0260	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
0270	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
0280	F0	F0	F0	F0	F0	F0	51	D1	D1	D1	D1	D1	D1	D1	D1	D1
0290	D1	D1	D1	D1	D1	D1	D1	D1	D1	D0	D0	D0	D0	D0	D0	D0
02A0	D0	31	B1	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F
02B0	6F	6F	6F	6F	6F	6E	6E	6E	6E	6E	6E	6E	6E	6E	EF	EF
02C0	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF	EF
02D0	EF	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE
02E0	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE	EE
02F0	EE	EE	EE	EE	EE	EE	EE	4F	CF	CF	CF	CF	CF	CF	CF	CF
0300	CF	CF	CF	CF	CF	CF	CF	CF	2F	AF	6D	6D	6D	6D	6D	6D
0310	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6C	6C	6C	6C
0320	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED	ED
0330	ED	ED	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC
0340	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC	EC
0350	EC	EC	EC	EC	4D	CD	CD	CD	CD	CD	CD	2D	AD	6B	6B	6B
0360	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	EB	EB
0370	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB	EB
0380	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA
0390	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	4B	CB	69
03A0	69	69	69	69	69	69	69	69	69	69	69	E9	E9	E9	E9	E9
03B0	E9	E9	E9	E9	E9	E9	E9	E9	E9	E9	E9	E9	E9	E8	E8	E8
03C0	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8	E8
03D0	E8	E8	E8	E8	E8	49	C9	67	67	67	67	67	67	67	E7	E7
03E0	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7
03F0	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6	E6

TABLE C-2 CONT'D

CONTROL VALIDATION PROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0400	E6	E6	E6	47	C7	65	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5
0410	E5	E5	E5	E5	E5	E5	E5	E5	E4	E4	E4	E4	E4	E4	E4	E4
0420	E4	E4	E4	E4	E4	E4	45	C5	63	E3	E3	E3	E3	E3	E3	E3
0430	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E2	E2	E2	E2	E2
0440	E2	E2	E2	E2	43	C3	61	E1	E1	E1	E1	E1	E1	E1	E1	E1
0450	E1	E1	E1	E1	E1	E1	E1	E1	E1	E0	E0	E0	E0	41	C1	FF
0460	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0470	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0480	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0490	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0500	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0510	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0520	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0530	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0540	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0550	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0560	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0570	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0580	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0590	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION PROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0600	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0610	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0620	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0630	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0640	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0650	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0660	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0670	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0680	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0690	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0700	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0710	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0720	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0730	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0740	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0750	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0760	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0770	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0780	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0790	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION PROM #U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0600	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0610	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0620	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0630	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0640	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0650	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0660	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0670	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0680	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0690	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0700	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0710	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0720	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0730	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0740	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0750	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0760	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0770	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0780	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0790	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION FROM 4044

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0400	03	02	01	27	27	27	27	26	25	24	23	22	21	20	11	10
0410	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2
0420	E1	E0	32	00	07	06	27	27	27	27	26	25	24	23	22	21
0430	20	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5
0440	E4	E3	E2	E1	27	27	27	27	26	25	24	23	22	21	20	11
0450	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	27	27	FF
0460	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0470	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0480	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0490	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0500	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0510	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0520	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0530	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0540	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0550	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0560	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0570	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0580	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0590	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION PROM #U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0200	22	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03
0210	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7
0220	C6	C5	C4	C3	C2	C1	27	27	27	26	25	24	23	22	21	20
0230	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
0240	E3	E2	E1	E0	D1	D0	C7	C6	27	26	25	24	23	22	21	20
0250	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
0260	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0	B1	B0
0270	A7	A6	A5	A4	A3	A2	A1	A0	91	90	87	86	85	84	83	82
0280	81	80	71	70	67	66	27	27	26	25	24	23	22	21	20	11
0290	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3
02A0	E2	27	27	27	26	25	24	23	22	21	20	11	10	07	06	05
02B0	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	27	26
02C0	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00
02D0	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4
02E0	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	91	90
02F0	87	86	85	84	83	82	81	27	27	26	25	24	23	22	21	20
0300	11	10	07	06	05	04	03	02	27	27	27	26	25	24	23	22
0310	21	20	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6
0320	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03	02
0330	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6
0340	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0
0350	91	90	87	86	27	27	26	25	24	23	22	27	27	27	26	25
0360	24	23	22	21	20	11	10	07	06	05	04	03	02	01	27	26
0370	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00
0380	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4
0390	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	27	27	27
03A0	26	25	24	23	22	21	20	11	10	07	06	27	26	25	24	23
03B0	22	21	20	11	10	07	06	05	04	03	02	01	00	F1	F0	E7
03C0	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1
03D0	C0	B1	B0	A7	A6	27	27	27	26	25	24	23	22	21	27	26
03E0	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00
03F0	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4

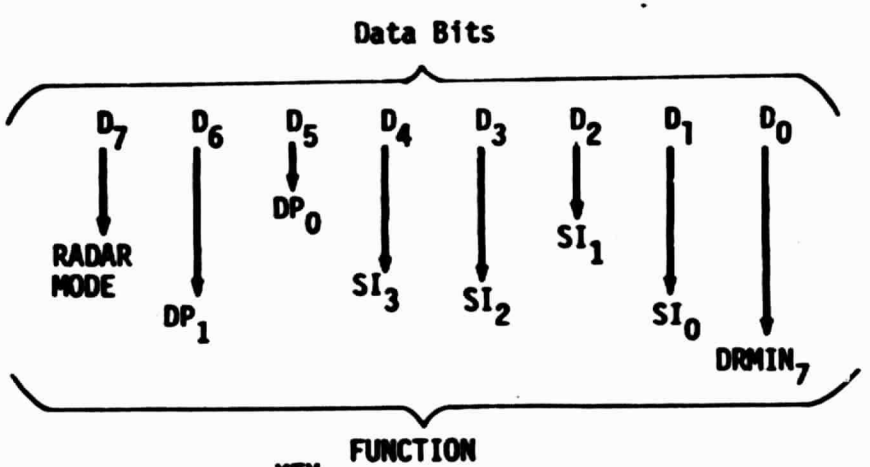
TABLE C-2 CONT'D

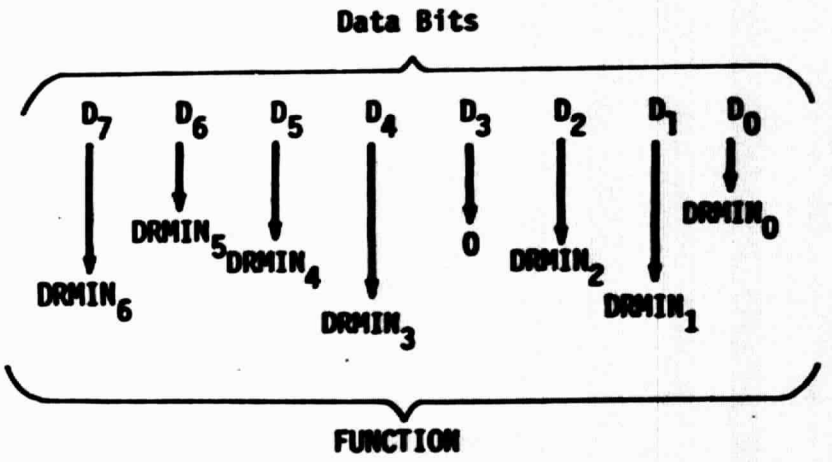
CONTROL VALIDATION FROM $U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03	02
0010	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6
0020	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	27
0030	26	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01
0040	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5
0050	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	91
0060	90	87	86	85	84	83	82	81	80	71	70	67	66	65	64	63
0070	62	61	60	51	50	47	46	45	44	43	42	41	40	27	26	25
0080	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00	F1
0090	F0	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03
00A0	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7
00B0	C6	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1
00C0	A0	91	90	87	86	85	84	83	82	81	27	27	26	25	24	23
00D0	22	21	20	11	10	07	06	05	04	03	02	27	27	27	26	25
00E0	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00	F1
00F0	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3
0100	C2	C1	C0	B1	B0	A7	A6	A5	27	26	25	24	23	22	21	20
0110	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
0120	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0	B1	B0
0130	A7	A6	A5	A4	A3	A2	A1	A0	91	90	87	86	85	84	83	82
0140	81	80	71	70	67	66	65	64	63	62	61	60	51	50	47	46
0150	45	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03
0160	02	01	27	26	25	24	23	22	21	20	11	10	07	06	05	04
0170	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0
0180	C7	C6	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2
0190	A1	27	27	27	26	25	24	23	22	21	20	11	10	07	06	05
01A0	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1
01B0	D0	C7	C6	C5	C4	C3	C2	C1	27	26	25	24	23	22	21	20
01C0	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
01D0	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0	B1	B0
01E0	A7	A6	A5	A4	A3	A2	A1	A0	91	90	87	86	85	84	83	82
01F0	81	80	71	70	67	66	65	64	63	62	61	27	26	25	24	23

TABLE C-3

CONTROL VALIDATION PROMS BIT ASSIGNMENTS





KEY

$DRMIN_7$ - $DRMIN_0$ -- 8-bit value for ΔRMIN - coded in 9's complement of BCD (2 digits)
MSB LSB
LSB = 1 μsec (e.g., 10010000 = 9 μsec)

SI_3 - SI_0 -- 4-bit value for sample interval - coded in complement binary
MSB LSB
LSB = 10 nsec (e.g., 1011 = 40 nsec)

DP_1	DP_0	
0	0	1-bit data
0	1	2-bit data
1	0	4-bit data
1	1	7-bit data

RADAR MODE - 0 = Mode 1
1 = Mode 2

APPENDIX D

MANUFACTURER'S DATA SHEETS

1. ECL COMPONENT DATA
2. TTL COMPONENT DATA
3. ANALOG AND DATA CONVERSION COMPONENT DATA

1. ECL COMPCNENT DATA

F10K VOLTAGE COMPENSATED ECL SERIES

GENERAL DESCRIPTION — Fairchild F10K Series Emitter Coupled Logic (ECL) circuits are high speed, low power logic elements intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communication systems.

F10,000 ECL is designed to be fully compatible with conventional 10,000 ECL and has the same part numbers, functions, pinouts, temperature behavior, test methods, propagation delay limits and signal voltages.

F10K circuits employ Emitter Coupled Logic to achieve typical power levels of 25 mW/gate. The nominal power supply is specified as V_{EE} equal to -5.2 V. All devices, however, may be operated over V_{EE} ranges of -4.7 to -6.2 V with negligible loss of noise immunity. Some SSI gates may be operated over a V_{EE} range of -3.5 to -6.2 V, again with a negligible loss of noise immunity, due to the built-in voltage regulator.

In accordance with standard IC practice, F10K devices are specified over 0°C to +75°C temperature range. However, limits ensure that the F10K series is fully compatible with other 10,000 devices specified over a -30°C to +85°C ambient temperature range.

High input impedance (typically 50 kΩ) and open outputs allow effective usage of series or parallel terminated line techniques and large numbers of OR-ties.

- **Very high speed . . . typically 2 ns per gate.**
- **Low power dissipation . . . typically 25 mW per gate.**
- **Voltage compensated . . . noise margin insensitive to power supply variations and transients, relaxed power supply requirements.**
- **Internal 50 kΩ (nominal) input pull down resistors . . . unused inputs may be left open.**
- **Open emitter-follower outputs drive terminated lines.**
- **Separate V_{CC} leads eliminate noise coupling.**
- **Single V_{EE} power supply . . . -4.7 to -6.2 V.**
- **Wired-OR capability.**
- **Complementary, simultaneous outputs.**
- **Fully compatible with other 10,000 series ECL.**

RECOMMENDED OPERATING AND TEST CONDITIONS — The Fairchild F10K series is designed to operate in a system whose ambient temperature is controlled by moving air or equivalent means. The ambient temperature may be any value between 0°C and +75°C, but the temperature gradient between the devices must be at a minimum to conserve noise immunity. The Fairchild F10K devices are designed to meet the specified dc characteristics when a thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

The Fairchild F10K series operates with a system power supply V_{EE} between -4.7 and -6.2 V. Detailed test specifications are for nominal V_{EE} = -5.2 V.

ABSOLUTE MAXIMUM RATINGS

(Non-operating, above which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	-8 V
Input Voltage	Gnd to V_{EE}
Output Current	-50 mA

FUNCTIONAL DESCRIPTION

F10K offers many high speed system design advantages. High speed is achieved by using small, low capacitance device geometries and operating the transistors between the active and off modes, thereby avoiding saturation. The basic ECL gate is shown in *Figure 1*.

If the input voltages are more negative than V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 LOW. If either input is more positive than V_{BB}, Q1 or Q2 will conduct and Q3 will be cut off, raising its collector voltage. Since one or more transistors are always conducting, there is a constant current drain, independent of frequency which eliminates sharp switching transients and frequency dependent power dissipation effects. The outputs of the circuit are emitter-followers, Q4 and Q5. They provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. The basic gate simultaneously performs the positive logic OR and NOR functions, providing both true and complement outputs within a single gate delay period. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor must be provided in all cases.

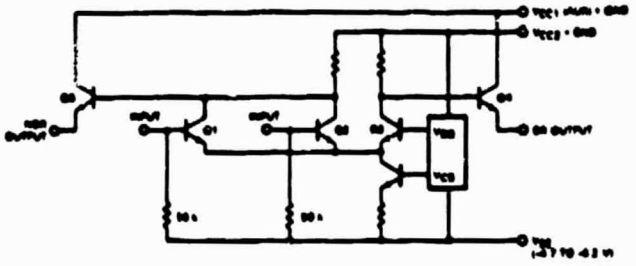


Fig. 1.

TYPICAL ECL TRANSFER CHARACTERISTICS WITH SPECIFICATION POINTS

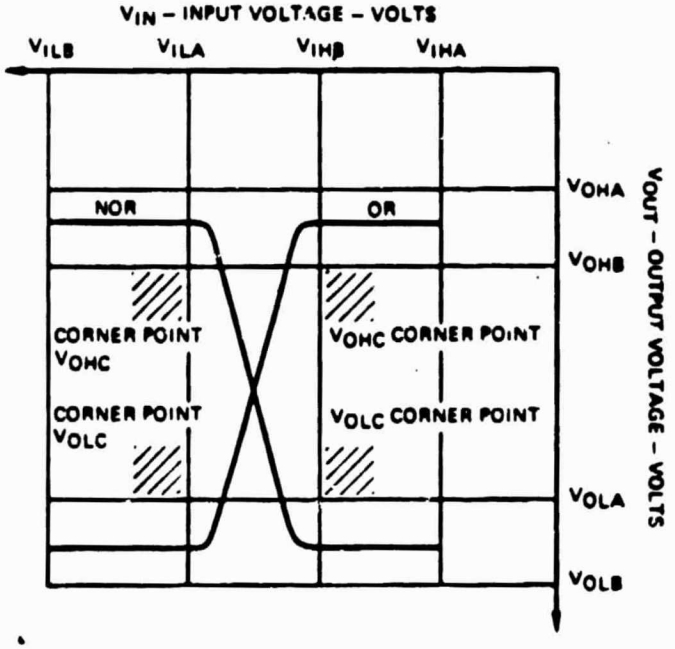
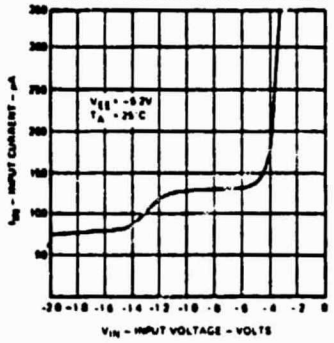


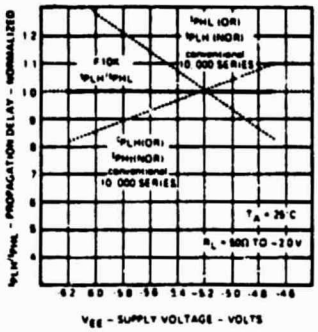
Fig. 2.

TYPICAL F10K SERIES CHARACTERISTICS

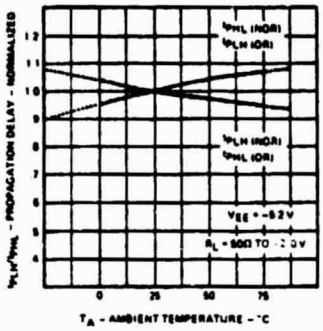
INPUT CHARACTERISTICS



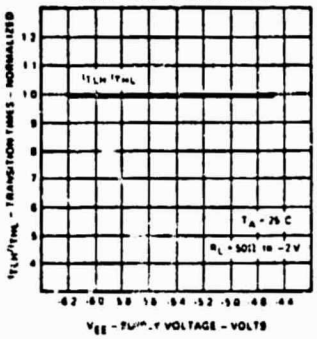
PROPAGATION DELAY VARIATION VERSUS SUPPLY VOLTAGE



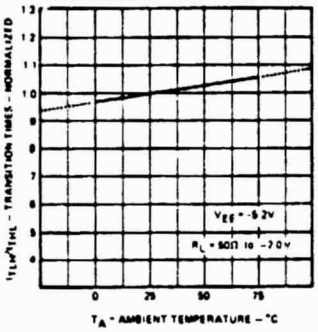
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE



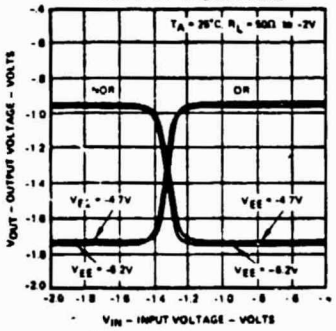
OUTPUT TRANSITION TIME VARIATION VERSUS SUPPLY VOLTAGE



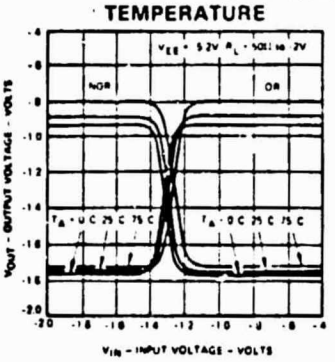
OUTPUT TRANSITION TIME VERSUS TEMPERATURE



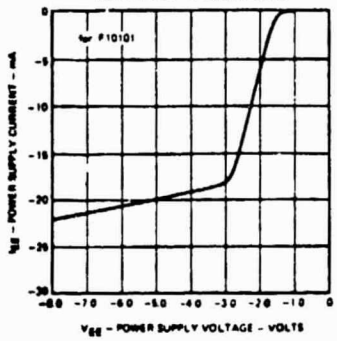
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



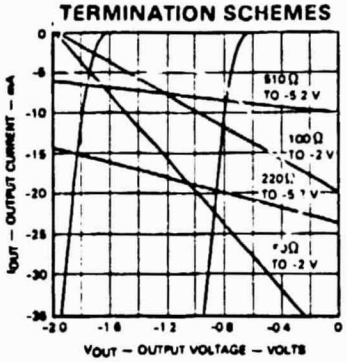
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS TEMPERATURE



CHANGE IN POWER SUPPLY CURRENT WITH RESPECT TO CHANGES IN POWER SUPPLY VOLTAGE

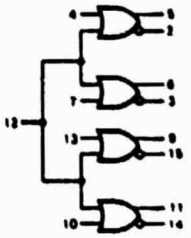


OUTPUT CHARACTERISTICS VERSUS TYPICAL OUTPUT TERMINATION SCHEMES

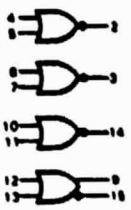


LOGIC DIAGRAMS V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

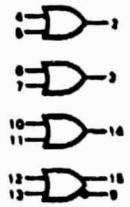
F10101



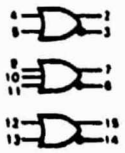
F10102



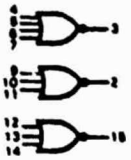
F10103



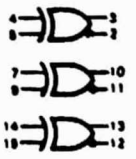
F10105



F10106



F10107

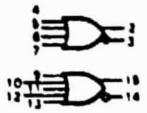


Logic Equation

$2 = 4 \cdot \overline{5} + \overline{4} \cdot 5$

$3 = 4 \cdot 5 + \overline{4} \cdot \overline{5}$

F10109



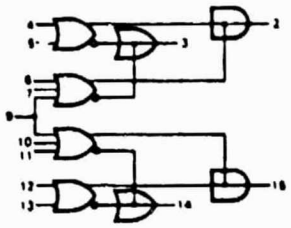
F10110

NOTE V_{CC1} = 1
V_{CC2} = 15

F10111

NOTE V_{CC1} = 1
V_{CC2} = 15

F10117

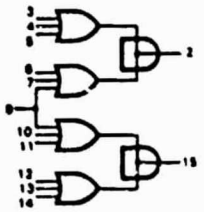


Logic Equation

$2 = (4 + 5)(6 + 7 + 9)$

$3 = \overline{(4 + 5)(6 + 7 + 9)}$

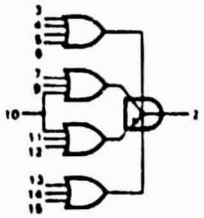
F10118



Logic Equation

$2 = (3 + 4 + 5)(6 + 7 + 9)$

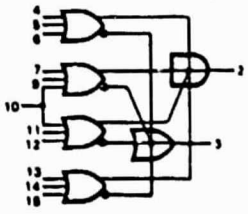
F10119



Logic Equation

$2 = (3 + 4 + 5 + 6)(7 + 9 + 10)(10 + 11 + 12)(13 + 14 + 15)$

F10121



Logic Equation

$2 = (4 + 5 + 6)(7 + 9 + 10)(10 + 11 + 12)(13 + 14 + 15)$

$3 = \overline{(4 + 5 + 6)(7 + 9 + 10)(10 + 11 + 12)(13 + 14 + 15)}$

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND F10101 • F10102 • F10103 • F10105 • F10106 F10107 • F10109 • F10110 • F10111

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Logic Function	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH F10101 Lead 12 F10107 Leads 5,7,15 F10110 All Inputs F10111 All Inputs			265 550 220 435 435	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current F10101	-26	-20		mA	25°C	Inputs and Outputs Open	
	F10102	-26	-20					
	F10103	-26	-20					
	F10105	-21	-15					
	F10106	-21	-15					
	F10107	-28	-22					
	F10109	-14	-10					
	F10110	-38	-28					
	F10111	-38	-28					

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C F10101 • F10102 • F10103 • F10105 • F10106 • F10109

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	2.0	2.9	ns	
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	2.0	2.9	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.3	ns	

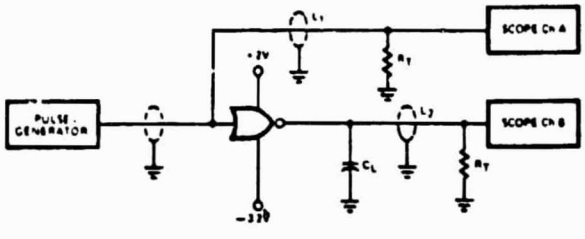
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C F10107

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.1	2.4	3.7	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.1	2.4	3.7	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.5	ns	

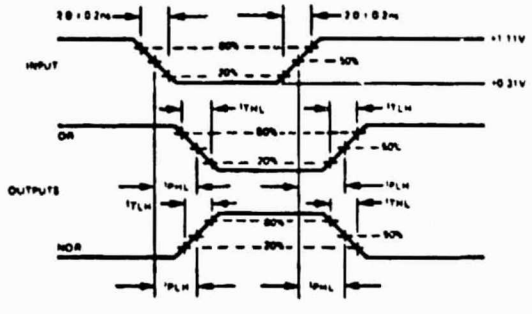
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C F10110 • F10111

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.4	2.4	3.5	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.4	2.4	3.5	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

F10010 • F10016

BCD DECADE COUNTER/4-BIT BINARY COUNTER

GENERAL DESCRIPTION — The F10010 is a high speed synchronous, presettable, cascadable BCD Decade Counter and the F10016 is a high speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 10K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

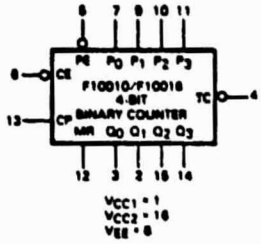
Both devices are packaged in hermetic ceramic 16-lead Dual In-Line packages and are specified for operation over the temperature range 0°C to 75°C.

- HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY
- INTERNAL COUNT ENABLE — FOR HIGHEST SPEED EXPANSION
- ASYNCHRONOUS MASTER RESET
- 50 Ω DRIVE CAPABILITY
- WIRED-OR CAPABILITY
- SEPARATE V_{CC} LEADS — ELIMINATE NOISE COUPLING
- INTERNAL 50 kΩ INPUT PULL DOWNS
- SINGLE -5.2 V POWER SUPPLY

LEAD NAMES

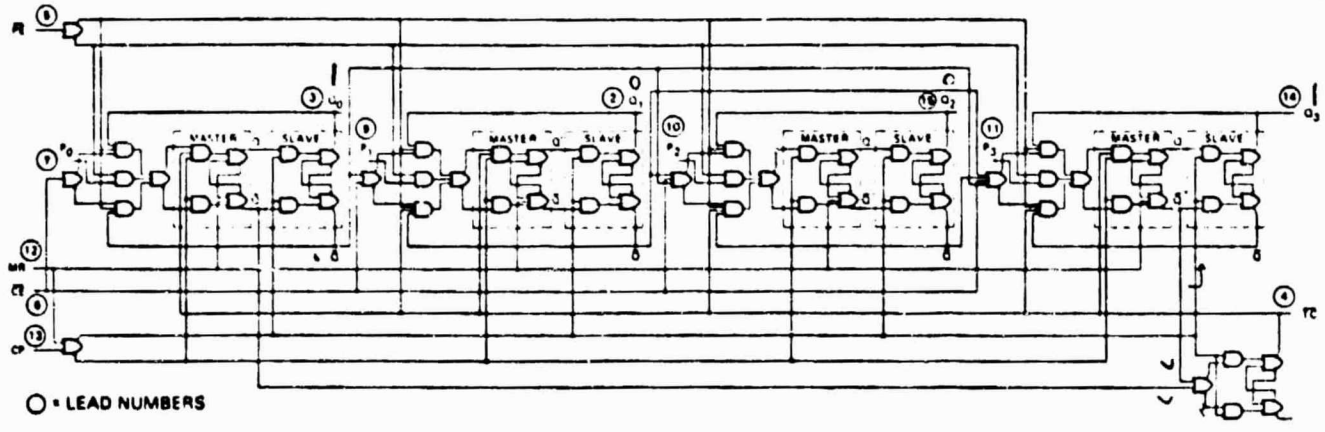
$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (10010, LOW at HLLH; 10016 LOW at HHHH)
Q_n	Counter Outputs

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)

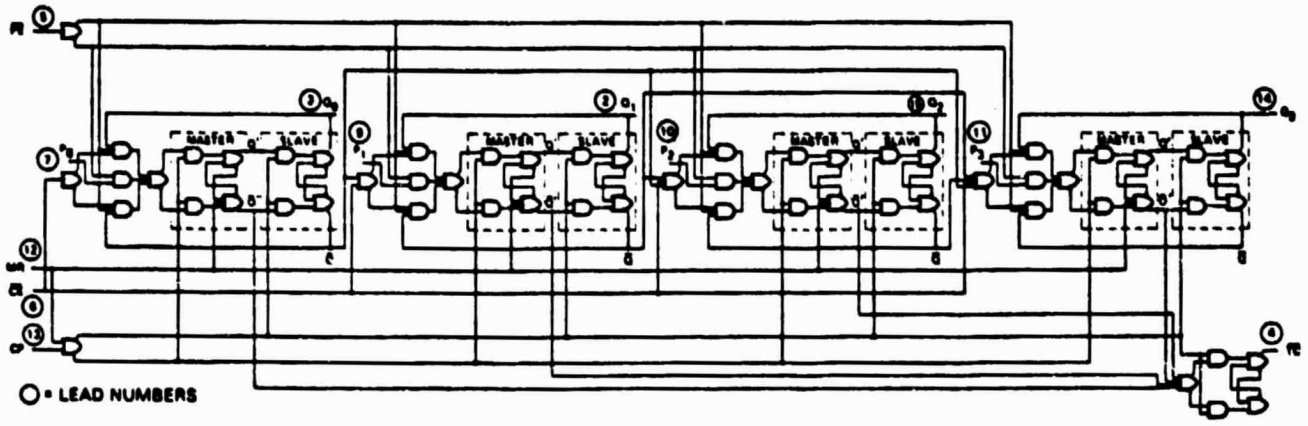
LOGIC DIAGRAM F10010



○ = LEAD NUMBERS

Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC DIAGRAM F10016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F10010 is a high speed BCD Decade Counter and the F10016 is a high speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 10010 and at count 15 (HHHH) on the 10016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table below. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

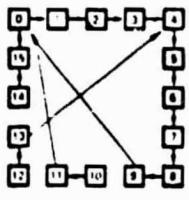
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	∫	Load Parallel (P_n to Q_n)
H	L	L	∫	Load Parallel (P_n to Q_n)
L	H	L	∫	Count
H	H	L	∫	Hold
X	X	L	⌉	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

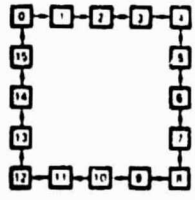
L = LOW
H = HIGH Voltage Level
X = Don't Care
∫ = Clock Pulse (LOW to HIGH)
⌉ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F10010



F10016



NOTE The 10010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses

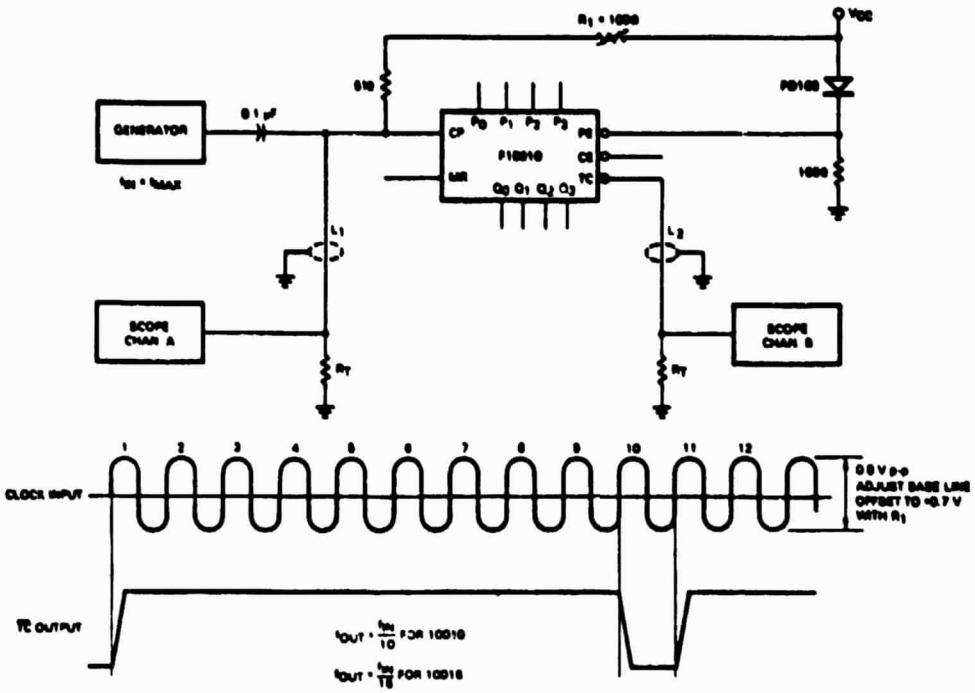
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH MR (Lead 12)			265 700	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-115	-80		mA	25°C	Outputs Open, Lead 12 Tied to V_{IH}	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_h	Hold Time After Clock P_n to CP	1.0			ns	
t_s	Set-Up Time Prior to Clock PE or CE to CP	2.5			ns	
t_h	Hold Time After Clock	0.5			ns	

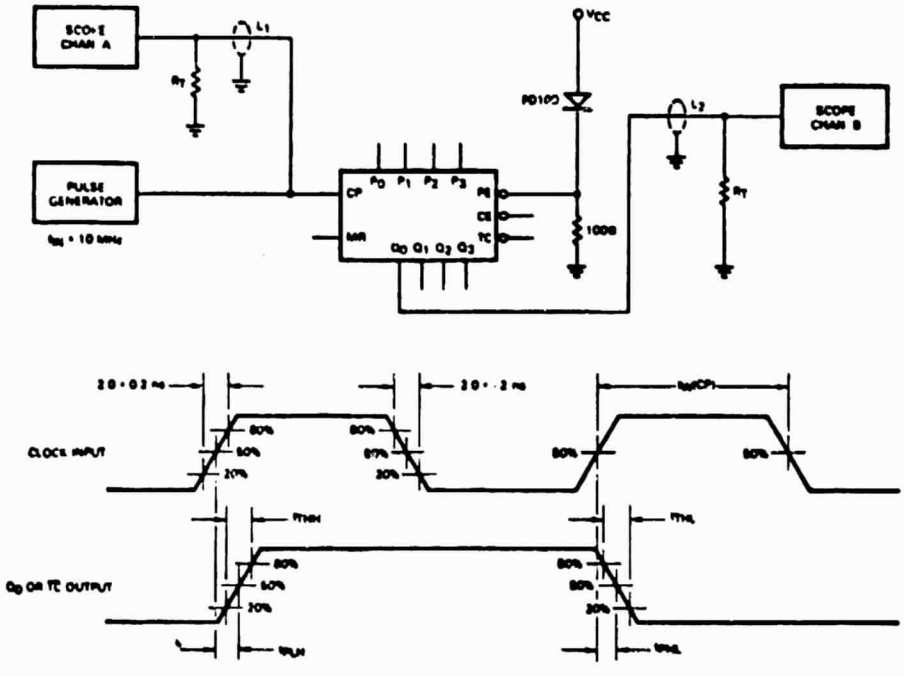
SWITCHING CIRCUITS AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency



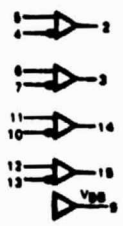
L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

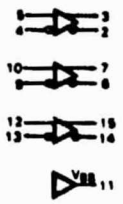
F10115 · F10116
LINE RECEIVERS

DESCRIPTION — The F10115 and F10116 are differential amplifiers with low impedance emitter-follower outputs. An internal reference supply (V_{BB}) is available for added versatility. Active current sources provide improved common mode rejection. The F10115 is a quad line receiver with single ended outputs. The F10116 is a triple line receiver with complementary outputs. The devices are voltage compensated and are fully compatible with other 10,000 series devices. The line receivers are used primarily to receive data from balanced twisted pair lines, however, with appropriate connections and feedback, they may operate as Schmitt triggers, high speed comparators, oscillators, or broadband amplifiers.

LOGIC DIAGRAM



F10115



F10116

TRUTH TABLES

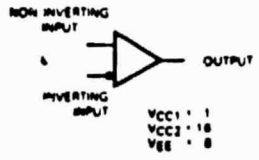
F10115 Quad Line Receiver

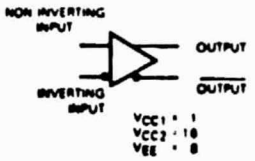
NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	H	L
V_{BB}	L	H

F10116 Triple Differential Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT	$\overline{\text{OUTPUT}}$
L	H	L	H
H	L	H	L
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	H	L	H
V_{BB}	L	H	L

FUNCTIONS





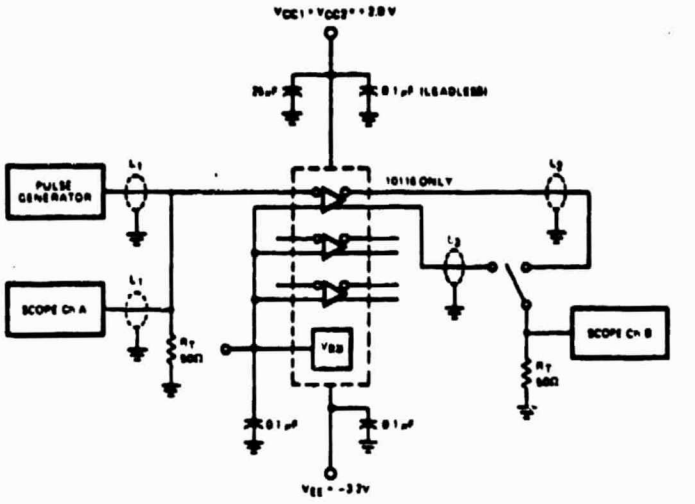
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

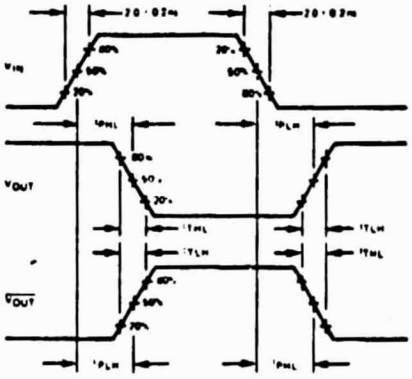
SYMBOL	CHARACTERISTIC		LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH		-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW		-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH		-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW				-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH		-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW		-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH				95	µA	25°C	V_{IN} = V_{IHA}	
I_{CBO}	Input Collector - Base Leakage Current		-1.0			µA	25°C	V_{IN} = -5.2 V	
I_{EE}	Power Supply Current	F10115	-26	-18		mA	25°C	Leads 4,7,10,13 = V_{ILB}. Leads 5,6,11,12 = V_{BB}	
		F10116	-21	-14		mA	25°C	Leads 4,9,12 = V_{ILB}. Leads 5,10,13 = V_{BB}	
V_{BB}	Reference Voltage		-1380 -1350 -1305		-1255 -1230 -1165	mV	0°C 25°C 75°C	F10115, Connect Leads 5,6,11,12 to Lead 9 F10116, Connect Leads 5,10,13 to Lead 11	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.0		2.9	ns	
t_{PHL}	Propagation Delay, HIGH to LOW	1.0		2.9	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS





Unused outputs connect to a 50Ω resistor to ground.

One input from each gate must be tied to V_{BB} during testing

L_1, L_2, and L_3 = equal length 50Ω impedance lines

R_T = 50Ω termination of scope

A line receiver is shown in *Figure 2*. The line is normally terminated in its characteristic impedance (typically 100 Ω) and output pull down resistors (typically 510 Ω) are used. The voltage across the terminating resistor V_T may be calculated as follows:

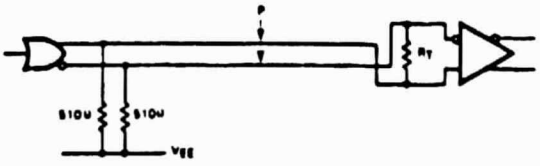
$$V_T = \frac{(V_{EE} - V_{OH})\, R_T}{R_E + R_T + R_{LINE}}$$

Where V_{OH} is the output voltage HIGH of the driving gate, R_{LINE} is the resistance and R_T is the terminating resistor. With typical values, V_T is 620 mV. The line receivers have a minimum differential input voltage gain of 7 V/V allowing very long twisted pairs to be driven. The line receivers employ active current sources which allow them to reject common mode inputs between -0.55 and -3 V.

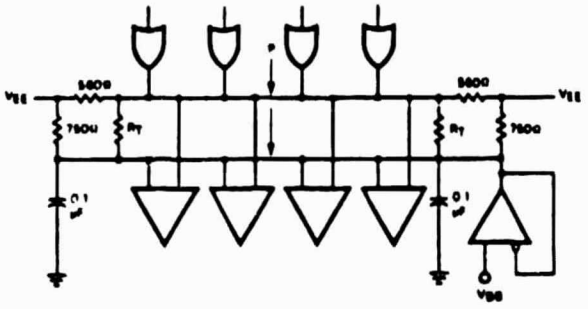
Information transfer is often organized with a data bus approach, where many sources may input and receive data on a common bus as illustrated in *Figure 3*. This configuration is a special case of wired-OR and the line receiver inputs are essentially single ended which reduces worst case voltage gain to 3.5 V/V. In practice it is possible to transmit data at rates in excess of 100 MHz over bus lengths of 10 feet, having 10 or more receivers and transmitters on the line.

Twisted pair differential lines are recommended for clock distribution since clock skew may be balanced by adjusting line lengths. Propagation time is approximately 1 ns per eight inches of line.

TWISTED-PAIR CONNECTIONS



Differential Transmission and Reception



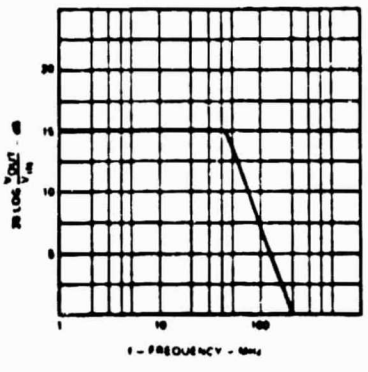
Backplane Data Bus

PARAMETERS FOR LINEAR APPLICATIONS

V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

PARAMETER	LIMITS			UNITS
	B	TYP	A	
Voltage Gain	3.5	5.0	6.0	V/V
Bandwidth		60		MHz
Input Resistance	4	6		kΩ
Input Capacitance		3		pF
Input Offset Current		2		μA
Input Bias Current		17	30	μA
Common Mode Input Voltage Range	-3.0		-0.55	V
Common Mode Rejection Ratio	50			dB
Supply Voltage Rejection Ratio		35		dB
Output Voltage Swing		0.40		Vpp
Output Source Current			50	mA
Output Resistance		9		Ω

TYPICAL LINE RECEIVER DIFFERENTIAL GAIN VERSUS INPUT FREQUENCY

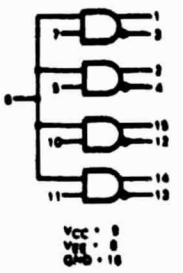


F10124
QUAD TTL TO ECL TRANSLATOR

DESCRIPTION — The F10124 is a Quad Translator, designed to convert TTL logic levels to 10K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the F10124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

LOGIC DIAGRAM



Logic Equations $2 = \overline{5 \cdot 6}$ $4 = \overline{5 \cdot 6}$

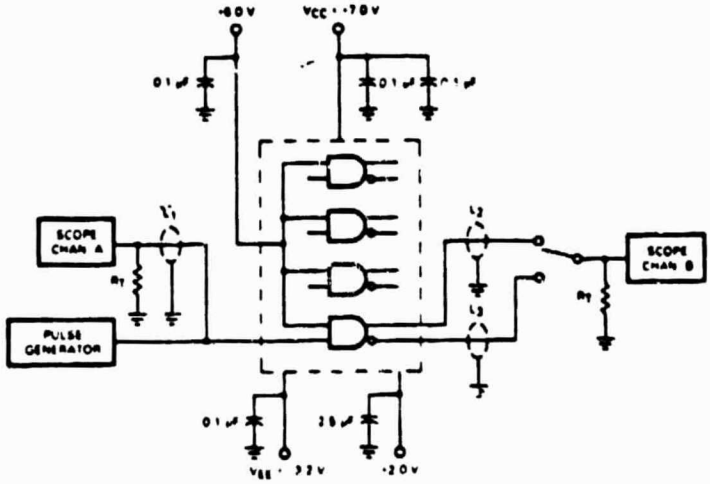
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = +5.0 V

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = +4.0 V or +0.4 V per Logic Function	—
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		Loading is 50Ω to -2.0 V
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	+1.9 +1.8 +1.8		5.0 5.0 5.0	V	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	0 0 0		+1.1 +1.1 +0.95	V	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
V_{CD}	Clamp Input Voltage	-1.5			V	25°C	I_{IN} = -10 mA	
V_{BD}	Input Breakdown Voltage	+5.5			V	25°C	I_{IN} = +1.0 mA, Other Inputs V_{IN} = GND	
I_{IH}	Input Current HIGH			50	µA	25°C	V_{IN} = +2.4 V, E_C V_{IN} = +0.4 V	
I_{IHX}	Input Current HIGH E_C			200	µA	25°C	E_C V_{IN} = +2.4 V, All Other Inputs V_{IN} = +0.4 V	
I_{ILX}	Input Current LOW E_C	-12.8			mA	25°C	E_C V_{IN} = +0.4 V, All Other Inputs V_{IN} = +4.0 V	
I_{IL}	Input Current LOW	-3.2			mA	25°C	V_{IN} = +0.4 V, E_C V_{IN} = +4.0 V	
I_{EE}	Power Supply Current	-34	-26		mA	25°C	Inputs and Outputs Open	
I_{CCH}	Power Supply Current		+13	+16	mA	25°C	All Inputs V_{IN} = +4.0 V	
I_{CCL}	Power Supply Current		+18	+25	mA	25°C	All Inputs V_{IN} = GND	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = +5.0 V, T_A = 25°C

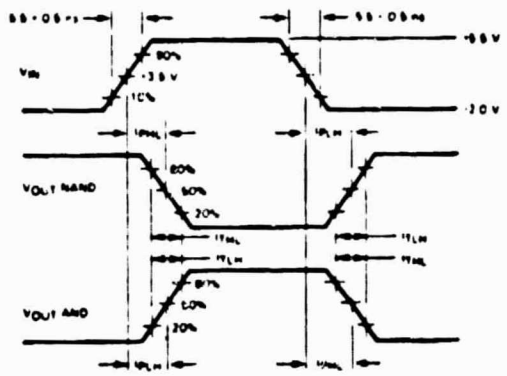
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	3.0	6.0	ns	
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	3.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.9	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.9	ns	

SWITCHING CIRCUIT AND WAVEFORMS



NOTES

Connect unused outputs through 50Ω resistor to ground
L_1, L_2 and L_3 are equal lengths of 50Ω impedance lines
R_T equals 50 Ω termination of scope



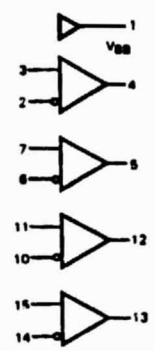
F10125

QUAD ECL TO TTL TRANSLATOR

DESCRIPTION — The F10125 is a Quad Translator for converting F10K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or as a differential line receiver. An internal reference voltage generator provides V_{BB} on lead 1 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go LOW when the inputs are left unconnected, have a fan out of 10 Schottky TTL loads.

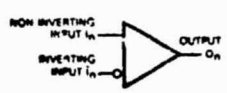
When used in the differential mode, the inputs have a common mode rejection of +1 V — making this device tolerant of ground offsets and transients between the signal source and the translator.

LOGIC DIAGRAM



V_{CC} = 9
V_{EE} = 8
GND = 16

FUNCTION



TRUTH TABLE

INPUTS		OUTPUT
Non-Inverting I_n	erting $\overline{I}_n$	O_n
L	H	L
H	L	H
L	L	*
H	H	*
OPEN	OPEN	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

*Undetermined

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

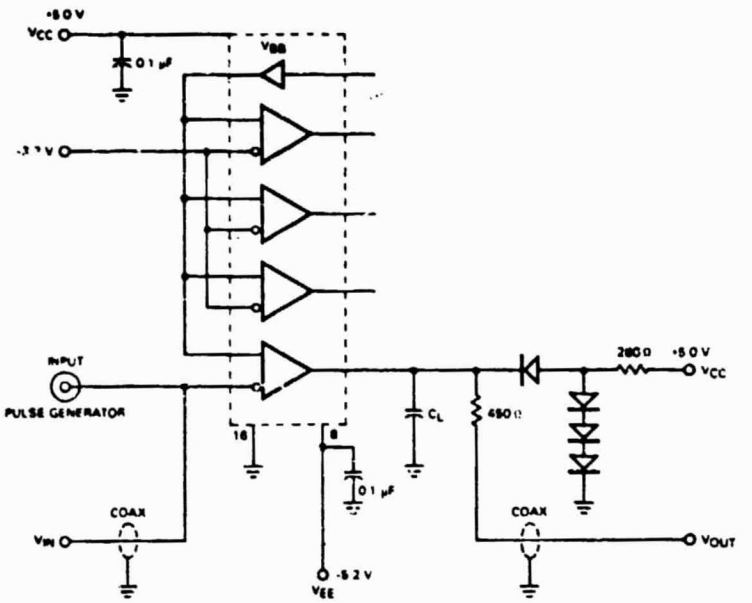
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is -2.0 mA V_{OH} +20 mA V_{OL}
V_{OL}	Output Voltage LOW			+0.5 +0.5 +0.5	V	0°C 25°C		
V_{OHC}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			+0.5 +0.5 +0.5	V	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
V_{IHH}	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.160 +0.190 +0.280	V	0°C 25°C 75°C		
V_{ILH}	Common Mode Rejection Input Voltage LOW +1.0 V	-0.870 -0.850 -0.830			V	0°C 25°C 75°C		
V_{IHL}	Common Mode Rejection Input Voltage HIGH -1.0 V			-1.840 -1.810 -1.720	V	0°C 25°C 75°C		
V_{ILL}	Common Mode Rejection Input Voltage LOW -1.0 V	-2.870 -2.850 -2.830			V	0°C 25°C 75°C		
V_{BB}	Reference Voltage	-1380 -1350 -1305		-1250 -1230 -1165	mV	0°C 25°C 75°C	V_{IN} = V_{ILB}	
I_{CBO}	Input Leakage Current	-1.0			µA	25°C	V_{IN} = V_{EE} Note 1	
I_{IH}	Input Current HIGH			115	µA	25°C	V_{IN} = V_{IHA} Note 1	
I_{OS}	Short Circuit Current	-100		-40	mA	25°C	V_{IN} = GND Note 2	
I_{EE}	Negative Power Supply	-40			mA	25°C	Inputs and Outputs Open	
I_{CCH}	Positive Power Supply			52	mA	25°C	V_{IN} = V_{IHA} Note 3	
I_{CCL}	Positive Power Supply			39	mA	25°C	V_{IN} = V_{ILB} Note 3	

NOTES
1. Complementary Input = V_{BB}
2. One Output at a Time
3. Lead 2, 6, 10, 14 = V_{IN}.
   Lead 3, 7, 11, 15 = Lead 1 (V_{BB})

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0		6.0	ns	
t_{PHL}	Propagation Delay, HIGH to LOW	1.0		6.0	ns	
t_{TLH}	Output Transition Time 1.0 V to 2.0 V			3.3	ns	
t_{THL}	Output Transition Time 2.0 V to 1.0 V			3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS

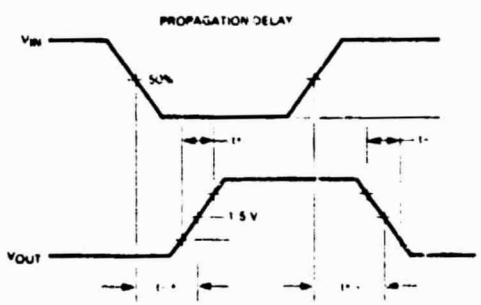


50Ω termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be <1/4 inch from TP_{IN} to input lead and TP_{OUT} to output lead

C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} (Lead 1) during testing



F10131

HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION — The F10131 contains two master/slave D-type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

LEAD NAMES

D_n	Data Input to Master
CP_n	Clock Input
CP_C	Common Clock Input
Q_n	Output
$\overline{Q}_n$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

TRUTH TABLES

SYNCHRONOUS OPERATION D TABLE

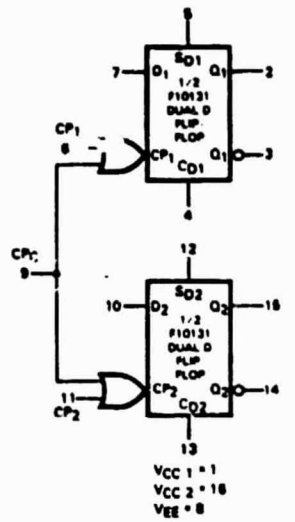
D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

(t+1) = Time after positive going clock transition

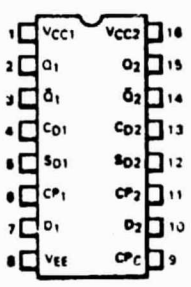
ASYNCHRONOUS OPERATION S_D C_D TABLE

C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

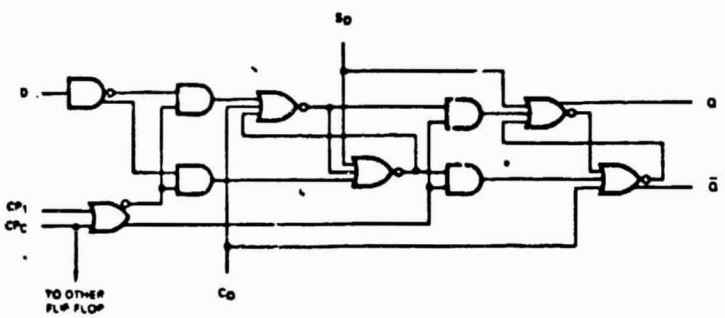
LOGIC SYMBOL



CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS		
		B	TYP	A				
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH CP C_{CP} D S_D & C_D			 220 265 245 330	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-56	-45		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

f_{count}	Toggle Frequency	125	160		MHz		
t_{PLH}	Propagation Delay Clock to Output	1.5	3.0	4.5	ns		
t_{PHL}	Propagation Delay Clock to Output	1.5	3.0	4.5	ns		
t_{PLH}	Propagation Dealy Set to Q, Clear to $\overline{Q}$	1.2	2.2	4.3	ns		
t_{PHL}	Propagation Delay Set to $\overline{Q}$, Clear to Q	1.2	2.2	4.3	ns		
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	4.5	ns		
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	4.5	ns		
t_s	Set-Up Time Data to Clock	2.5	0.5		ns		
t_h	Hold Time Data to Clock	1.5	-0.5		ns		

F10136 • F10536 • F10137 • F10537

4-STAGE UP/DOWN COUNTERS

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION – The F10136/F10536 and F10137/F10537 are 4-stage synchronous counters capable of operating at typical count rates of 250 MHz. The circuits are designed to operate in count up, count down, hold, and preset modes, as determined by signals applied to select inputs S_1 and S_2. The F10136 is a modulo-16 binary counter and the F10137 is a BCD (8421) decade counter.

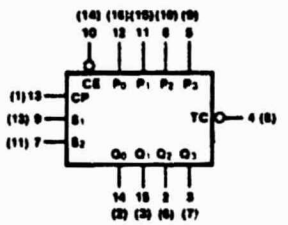
All operations are synchronous and state changes are initiated by the rising edge of the clock. Each circuit has an active LOW Count Enable ($\overline{CE}$) input and an active LOW Terminal Count ($\overline{TC}$) output which allow two or more counters to be cascaded without extra logic. The preset feature makes it possible to use the F10136 and F10137 as programmable counters in a broad variety of applications.

- HIGH SPEED . . . 250 MHz TYPICAL COUNT RATE
- FULLY SYNCHRONOUS
- RIPPLE CARRY SIMPLIFIES CASCADING
- PRESETTABLE, FOR VARIABLE MODULUS APPLICATIONS
- SELECT INPUTS CAN BE WIRED TO V_{CC}
- 50 Ω LINE DRIVING CAPABILITY
- SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING
- INTERNAL 50 kΩ INPUT PULL-DOWN RESISTORS . . . UNUSED INPUTS CAN BE LEFT OPEN

PIN NAMES

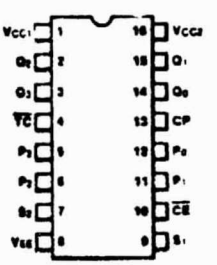
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Positive-Going Active Edge)
P_n	Preset Data Inputs
Q_n	Flip-flop Outputs
S_n	Operating Mode Select Inputs
$\overline{TC}$	Terminal Count Output (Active LOW)

LOGIC SYMBOL



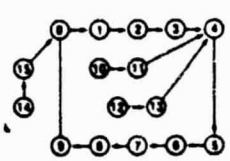
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)

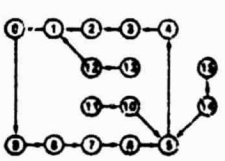


STATE DIAGRAMS

10537/10137 COUNT UP



10537/10137 COUNT DOWN



10536/10136

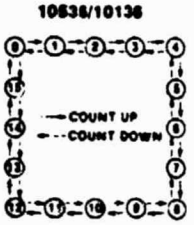
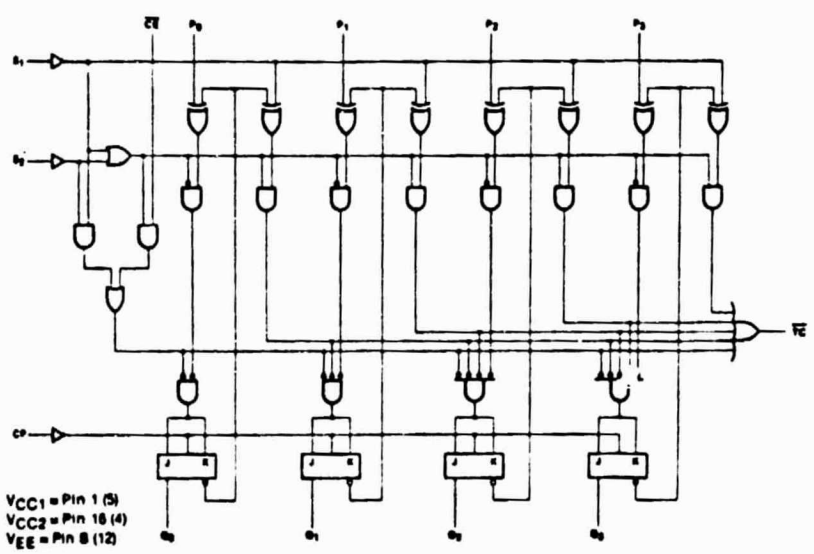


Fig. 1. Sample Operating Sequences, F10136 • F10536 Binary

INPUTS								OUTPUTS					SELECT
S_1	S_2	$\overline{CE}$	CP	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	MODE
L	L	X	∫	H	L	H	H	H	L	H	H	L	PRESET*
L	H	L	∫	X	X	X	X	H	H	L	L	H	COUNT
L	H	L	∫	X	X	X	X	H	H	L	H	H	UP
L	H	L	∫	X	X	X	X	H	H	H	L	H	
L	H	L	∫	X	X	X	X	H	H	H	H	L	(Max)
L	H	H	X	X	X	X	X	H	H	H	H	H	($\overline{CE}$ Inhibit)
L	H	L	∫	X	X	X	X	L	L	L	L	H	
L	H	L	∫	X	X	X	X	L	L	L	H	H	
H	H	X	X	X	X	X	X	L	L	L	H	H	HOLD
L	L	X	∫	L	H	L	L	L	H	L	L	L	PRESET*
H	L	L	∫	X	X	X	X	L	L	H	H	H	COUNT
H	L	L	∫	X	X	X	X	L	L	H	L	H	DOWN
H	L	L	∫	X	X	X	X	L	L	L	H	H	
H	L	L	∫	X	X	X	X	L	L	L	L	L	(Min)
H	L	L	∫	X	X	X	X	H	H	H	H	H	
H	L	L	∫	X	X	X	X	H	H	H	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
* = Starting point, arbitrary preset data

F10136/F10536 LOGIC DIAGRAM



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

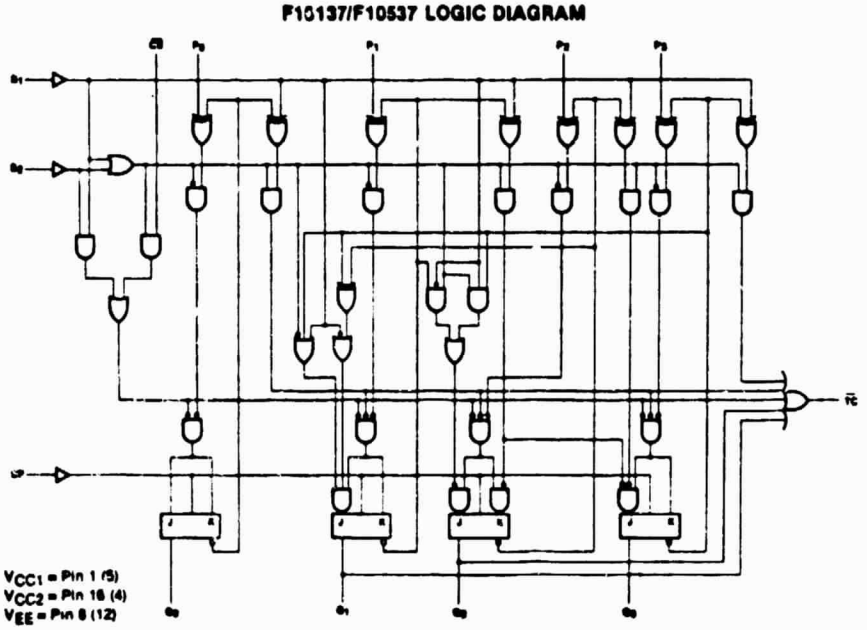
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

Fig. 2. Sample Operating Sequences, F10137 • F10537 Binary

INPUTS								OUTPUTS					SELECT
S_1	S_2	$\overline{CE}$	CP	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	MODE
L	L	X	∫	L	H	L	H	L	H	L	H	H	PRESET*
L	H	L	∫	X	X	X	X	L	H	H	L	H	COUNT
L	H	L	∫	X	X	X	X	L	H	H	H	H	UP
L	H	L	∫	X	X	X	X	H	L	L	L	H	
L	H	L	∫	X	X	X	X	H	L	L	H	L	(Max)
L	H	H	X	X	X	X	X	H	L	L	H	H	($\overline{CE}$ Inhibit)
L	H	L	∫	X	X	X	X	L	L	L	L	H	
L	H	L	∫	X	X	X	X	L	L	H	L	H	
H	H	X	X	X	X	X	X	L	L	H	L	H	HOLD
L	L	X	∫	L	H	L	L	L	H	L	L	H	PRESET*
H	L	L	∫	X	X	X	X	L	L	H	H	H	COUNT
H	L	L	∫	X	X	X	X	L	L	H	L	H	DOWN
H	L	L	∫	X	X	X	X	L	L	L	H	H	
H	L	L	∫	X	X	X	X	L	L	L	L	L	(Min)
H	L	L	∫	X	X	X	X	H	L	L	H	H	
H	L	L	∫	X	X	X	X	H	L	L	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
* = Starting point, Arbitrary data

F10137/F10537 LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

FUNCTIONAL DESCRIPTION—In the counting modes, the F10136 follows a straightforward binary sequence. The F10137 follows the 8421 BCD sequence, as indicated in the state diagrams on page 1. For either circuit type, the $\overline{CE}$ inputs must be LOW for counting to occur, as indicated in the sample sequences of *Figures 1* and *2*.

The Select inputs determine the operating mode of a circuit, as shown in the table of *Figure 3*. All operations are synchronous and state changes are initiated by the rising edge of the clock. The $\overline{CE}$ input has no effect on the preset and hold operations. Either of the Select inputs can be wired to V_{CC}; this simplifies designs in which S_1 or S_2 is required to always be HIGH.

In the counting modes the $\overline{TC}$ output is controlled by the $\overline{CE}$ input and by the state of the flip-flops, as indicated in *Figure 3*. $\overline{TC}$ is normally HIGH and goes LOW (assuming $\overline{CE}$ is LOW) when the counter reaches zero in the count down mode or when it reaches maximum (15 for the 10136, 9 for the 10137) in the count up mode. The control that the $\overline{CE}$ inputs has on the $\overline{TC}$ output makes it possible to form multi-stage counters without external logic, as shown in *Figure 4*. In order for a given stage to count, the $\overline{TC}$ outputs (and thus the $\overline{CE}$ inputs) of all the preceding stages must be LOW. The frequency capability of this arrangement is limited by the time required for a negative-going $\overline{TC}$ signal from the first stage to ripple through to the $\overline{CE}$ input of the last stage. The time between successive positive-going clock edges must not be less than the sum of the CP to $\overline{TC}$ delay of the first stage, the $\overline{CE}$ to $\overline{TC}$ delays of the intermediate stages, and the $\overline{CE}$ to CP set-up time of the last stage. The counter can be enabled/disabled at the $\overline{CE}$ input of the first stage (*Figure 4*), or by using the Select inputs.

In the preset mode, the $\overline{TC}$ output of the F10136 is forced LOW, while that of the F10137 depends on the state of Q_1 and Q_2, as indicated in *Figure 3*. For either circuit type, the $\overline{TC}$ output is forced HIGH in the hold mode. This feature can be used to simplify designs for certain types of applications. In the simple counter of *Figure 4*, for example, the second and subsequent stages can be prevented from counting by putting the first stage into the hold mode, causing a HIGH signal to ripple through to all $\overline{TC}$ outputs. Wiring simplification is possible if the counter is to operate in only one of the counting modes, plus preset and hold. For example, if the S_1 inputs of the second and subsequent stages are left open (LOW) and their S_2 inputs wired in parallel with S_2 of the first stage, then the S_2 signal selects either the count up or preset mode for these latter stages. Putting the first stage into the hold mode effectively achieves a hold for the entire counter in the manner previously described. Designers should bear in mind that a $\overline{TC}$ output is subject to decoding spikes and therefore should not be used as a clock.

The flip-flops are master/slave type with internal JK feedback. Information enters the master when the clock is LOW and transfers to the slave when the clock goes HIGH. Signals on the Preset, Select, and $\overline{CE}$ inputs must be in the intended state at least a set-up time before the clock rising edge. Hold times for these inputs are negative, however, which offers simplifications in some applications. *Figure 5* illustrates an arrangement for a programmable down counter using F10136 circuits. When the counter reaches the all-zeros state and the clock goes LOW, the $\overline{TC}$ outputs will go LOW, starting at the first stage and rippling through to make the S_1 inputs LOW. Thus with S_1 and S_2 LOW the circuits are in the preset mode and the preset data will be entered on the next rising clock edge. S_2 also goes HIGH (with the clock) but this does not interfere with presetting because of the negative hold time characteristic. The $\overline{CE}$ input of the first stage also goes HIGH with the presetting clock, causing the $\overline{TC}$ output to go HIGH and ripple through the second and third stages to make the S inputs HIGH. After this is accomplished the circuits are in the hold mode when the clock is HIGH and in the count down mode when the clock is LOW.

The outputs of these circuits have no internal pull-down resistors and the 50 kΩ input pull-down resistors of F10K elements do not provide sufficient current to perform the pull-down function at electronic speeds. External pull-down current is an integral function of the termination scheme selected by the system designer, as discussed in Chapter 5 of the Fairchild ECL Handbook.

Fig. 3. Mode Select and Terminal Count Equation Table

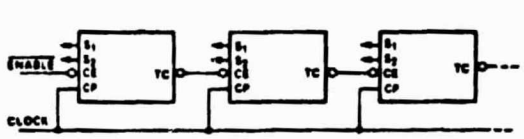
Select		Operating	Terminal Count Output Equation	
S_1	S_2	Mode	F10136 Binary	F10137 BCD
L	L	Preset	$\overline{TC} = LOW$	$\overline{TC} = Q_1 + Q_2$
L	H	Count Up	$\overline{TC} = \overline{CE} + \overline{Q_0} + \overline{Q_1} + \overline{Q_2} + \overline{Q_3}$	$\overline{TC} = \overline{CE} + \overline{Q_0} + Q_1 + Q_2 + \overline{Q_3}$
H	L	Count Down	$\overline{TC} = \overline{CE} + Q_0 + Q_1 + Q_2 + Q_3$	$\overline{TC} = \overline{CE} + Q_0 + Q_1 + Q_2 + Q_3$
H	H	Hold	$\overline{TC} = HIGH$	$\overline{TC} = HIGH$

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

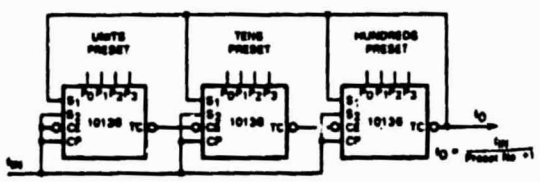
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH				µA	25°C	$V_{IN} = V_{IHA}$
	P_n			220			
	S_2			295			
	CP			290			
	S_1, $\overline{CE}$			245			
I_{EE}	Power Supply Current	−135	−105		mA	25°C	Outputs Open, Pin 12 tied to V_{IH}

AC CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	TEST CONDITIONS
		B	TYP	A		
f_{count}	Count Frequency	125	250		MHz	
t_{PLH} / t_{PHL}	Propagation Delay, Clock to Q_n	1.0	2.2	4.5	ns	
t_{PHL} / t_{PLH}	Propagation Delay, Clock to $\overline{TC}$		4.5		ns	
t_{PHL} / t_{PLH}	Propagation Delay, $\overline{CE}$ to $\overline{TC}$	1.6	3.5	6.9	ns	
t_{TLH} / t_{THL}	Output Transition Time LOW-to-HIGH, HIGH-to-LOW (20% to 80%), (80% to 20%)	1.1	2.0	3.3	ns	
t_s	Set-Up Time Prior to Clock				ns	
	Data		2.0			
	Select		4.0			
	$\overline{CE}$ (to Enable Count)		2.7			
	$\overline{CE}$ (to Inhibit Count)		1.2			
t_h	Hold Time After Clock				ns	
	Data		−2.0			
	Select		−4.0			
	$\overline{CE}$ (to Enable Count)		−1.0			
	$\overline{CE}$ (to Inhibit Count)		−2.5			

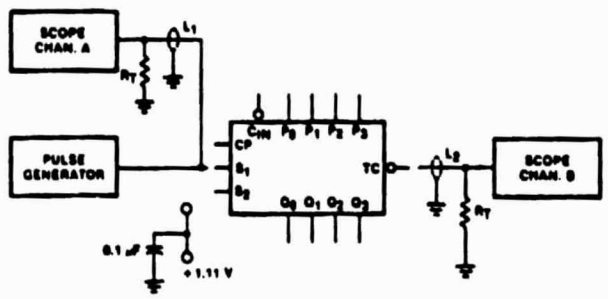


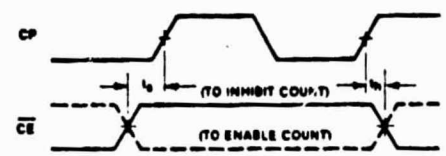
Multi-Stage Counter Using Ripple Carry

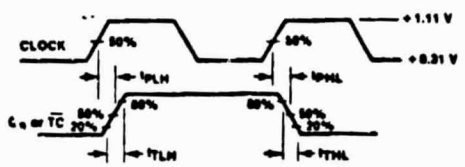


Programmable Down Counter

SWITCHING CIRCUIT AND WAVEFORMS







L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 3.0 pF

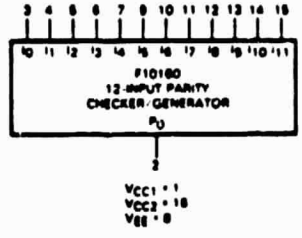
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} - V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

F10160

12-BIT PARITY CHECKER/GENERATOR

DESCRIPTION — The F10160 is a 12-Input Parity Generator. The output will be HIGH when an odd number of inputs are HIGH; typical delay is 4 ns. For applications requiring fewer than 12 inputs, unused inputs may be left open, since internal input resistors hold unconnected inputs LOW.

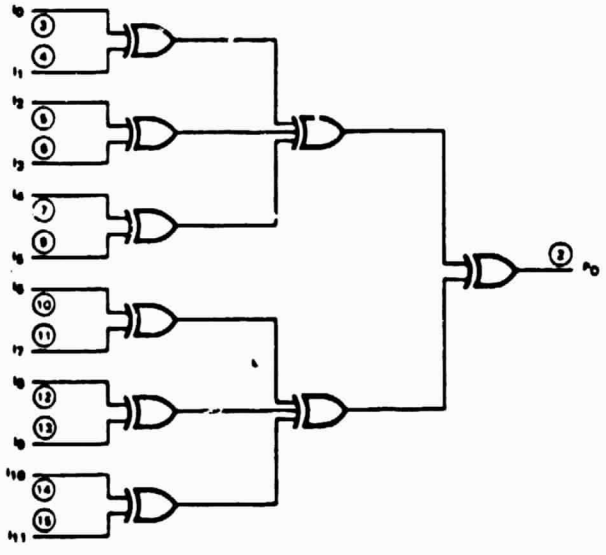
LOGIC SYMBOL



LEAD NAMES

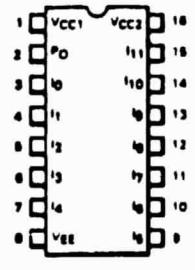
I_n	Inputs
P_O	Parity Odd

LOGIC DIAGRAM



○ = LEAD NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Logic Function	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH (All Inputs)			220	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-59	-46		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH		4.0		ns	
t_{PHL}	Propagation Delay, HIGH to LOW		4.0		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

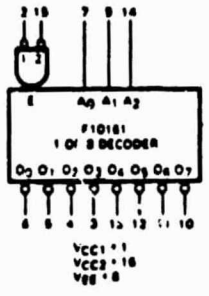
F10161
1-OF-8 DECODER
ACTIVE LOW OUTPUTS

DESCRIPTION — The F10161 accepts a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be LOW while all other outputs are HIGH. Two enable inputs force all outputs HIGH when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

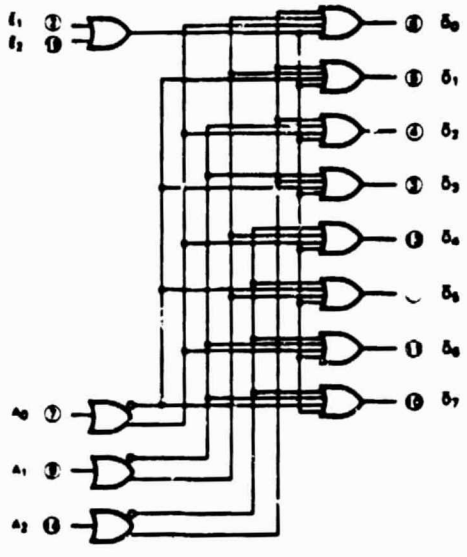
LEAD NAMES

$\overline{E}_n$	Enable (Active LOW)
A_n	Address Inputs
$\overline{O}_n$	Output (Active LOW)

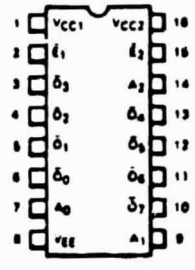
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\bar{E}_2$	$\bar{E}_1$	A_2	A_1	A_0	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

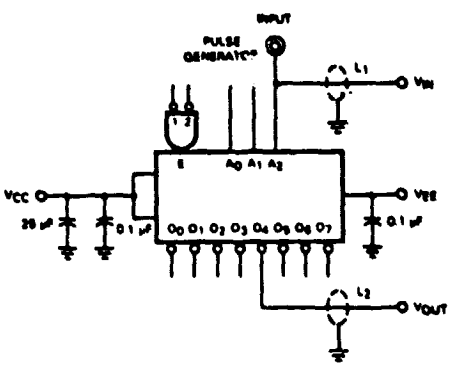
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

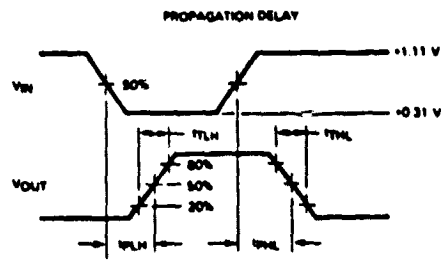
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B	TYP	A				
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-76	-55		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	
t_{PHL}	Propagation Delay	1.5	4.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
V_{EE} = -3.2 V

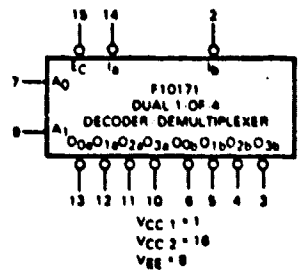
F10171
DUAL 1-OF-4 DECODER/DEMULTIPLEXER
SELECTED OUTPUTS LOW

DESCRIPTION — The F10171 contains a pair of 1-of-4 Decoder/Multiplexers with Common Enable ($\overline{E}_C$) and Address (A_0 and A_1) inputs. In each decoder the unselected (or disabled) outputs are HIGH and the selected (or enabled) output repeats the information present on its data input ($\overline{I}_a$ or $\overline{I}_b$). If the $\overline{E}_C$ input is HIGH all outputs of both decoders are HIGH, as indicated in the truth table. The F10171 can be used as a 1-of-8 decoder/demultiplexer by connecting the True and Complement of the third address bit to $\overline{I}_a$ and $\overline{I}_b$, respectively, and using $\overline{E}_C$ as either a data input or as an enable.

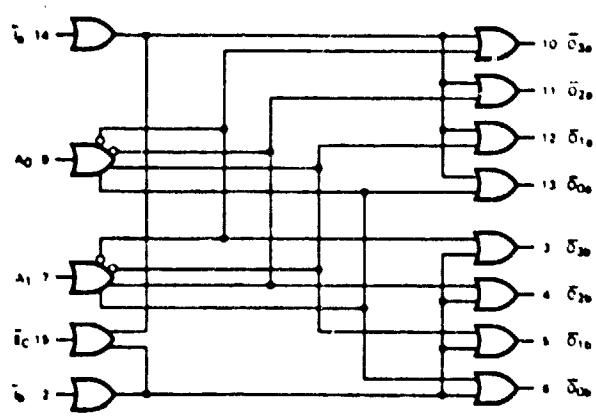
LEAD NAMES

$\overline{E}_C$	Common Enable (Active LOW)
A_n	Address Inputs
$\overline{I}_n$	Data Inputs
$\overline{O}_n$	Outputs

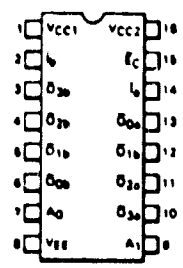
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

E_C	$\bar{I}_a$ / I_b	A_1	A_0	$\bar{O}_{0a}$ / $\bar{O}_{0b}$	$\bar{O}_{1a}$ / $\bar{O}_{1b}$	$\bar{O}_{2a}$ / $\bar{O}_{2b}$	$\bar{O}_{3a}$ / $\bar{O}_{3b}$
L	L	L	L	L	H	H	H
L	H	L	L	H	H	H	H
L	L	L	H	H	L	H	H
L	H	L	H	H	H	H	H
L	L	H	L	H	H	L	H
L	H	H	L	H	H	H	H
L	L	H	H	H	H	H	L
L	H	H	H	H	H	H	H
H	X	X	X	H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75 °C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			220	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-77	-62		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	
t_{PHL}	Propagation Delay, HIGH to LOW	1.5	4.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.1	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.1	2.0	3.3	ns	

F10173

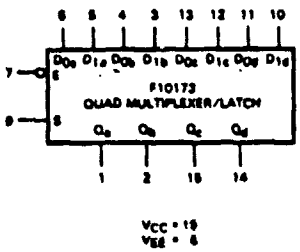
QUAD MULTIPLEXER/LATCH

DESCRIPTION — The F10173 is a Quad 2-Channel Multiplexer with latches. It incorporates a common Enable and a common Data Select input. The Select input determines which Data input is enabled. A HIGH input enables Data inputs D_{0a}, D_{0b}, D_{0c}, and D_{0d} and a LOW enables Data inputs D_{1a}, D_{1b}, D_{1c}, D_{1d}. Any change on the Data input appears at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the enable. While the Enable input is in the HIGH state, a change in the information present at the Data inputs does not affect the output information.

LEAD NAMES

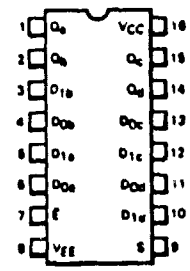
S	Data Select
D_n	Data Inputs
$\overline{E}$	Enable (Active LOW)
Q_n	Outputs

LOGIC SYMBOL

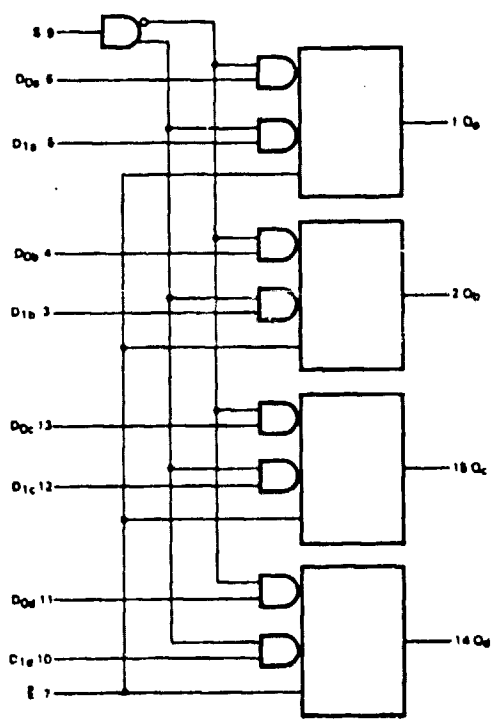


V_{CC} = 16
V_{EE} = 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

TRUTH TABLE

S	$\overline{E}$	Q_{n+1}
H	L	D_{0a}
L	L	D_{1a}
X	H	Q_n

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Enable and Select Data			 245 290	µA	25°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-66			mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output		4.5		ns	
t_{PHL}	Propagation Delay Data to Output		2.5		ns	
t_{PLH}	Propagation Delay Select to Output		3.5		ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		2.0		ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		2.0		ns	
t_s	Set-Up Time Data Select		 1.5 2.5		ns	
t_h	Hold Time Data Select		 0.0 -0.5		ns	

F10174

DUAL MULTIPLEXER

DESCRIPTION — The F10174 is a high speed Dual Channel Multiplexer with output enable capability. The Select inputs determine one of four active Data inputs for each multiplexer. When the Enable input is HIGH, both outputs are forced LOW. The Enable is also useful when OR-wiring several multiplexers to achieve additional channel capability.

LEAD NAMES

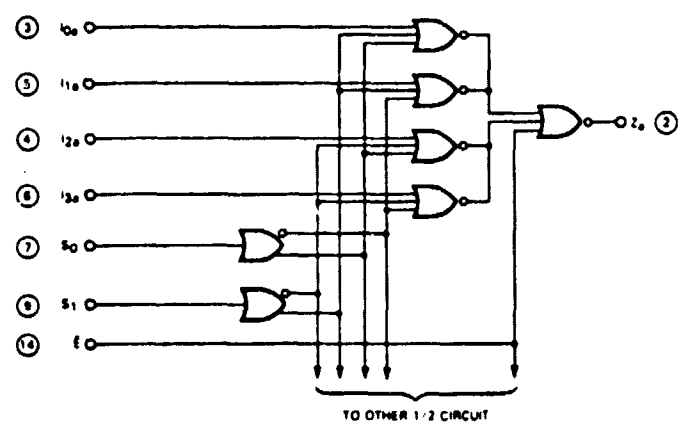
I_n	Address Inputs
$\overline{E}$	Enable (Active LOW)
Z_a	Outputs
S_n	Select Inputs

TRUTH TABLE

$\overline{E}$	S_1	S_0	Z_a	Z_b
H	X	X	L	L
L	L	L	I_{0a}	I_{0b}
L	L	H	I_{1a}	I_{1b}
L	H	L	I_{2a}	I_{2b}
L	H	H	I_{3a}	I_{3b}

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

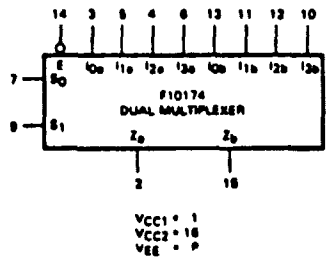
LOGIC DIAGRAM



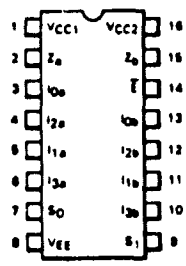
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

○ = LEAD NUMBERS

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH Data Enable			 220 330	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-50	-40		mA	25°C	Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL}	Propagation Delay Data to Output	1.5	3.0	4.5	ns	
t_{PLH}	Propagation Delay Select to Output	2.0	4.0	6.0	ns	
t_{PHL}	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

ECL ISOPLANAR MEMORY F10415 / F10415A

1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10415 and F10415A are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for high speed scratch pad, control and buffer storage applications. Both include full address decoding on the chip, have separate Data In and non-inverted Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

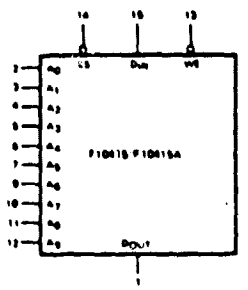
The F10415 and F10415A are packaged in a hermetic ceramic 16-pin dual in-line package and are specified for operation over the temperature range 0°C to 75°C.

- COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC
- TYPICAL READ ACCESS TIME
  - F10415 – 25 ns
  - F10415A – 12 ns
- TYPICAL CHIP SELECT ACCESS TIME
  - F10415 – 7 ns
  - F10415A – 5 ns
- ORGANIZED 1024 WORDS X 1 BIT
- OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION
- POWER DISSIPATION 0.5 mW/BIT
- POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE

PIN NAMES

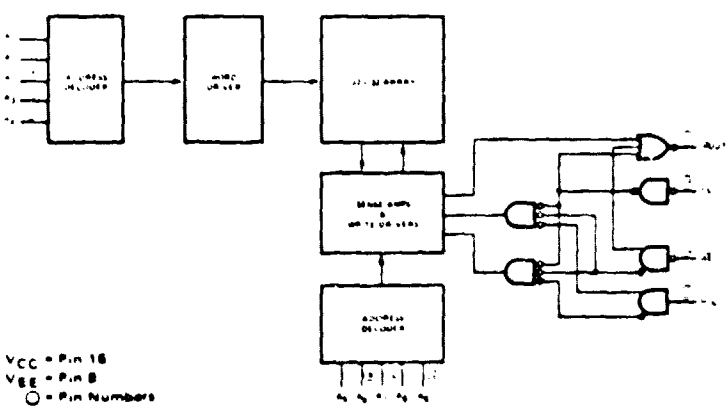
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC SYMBOL



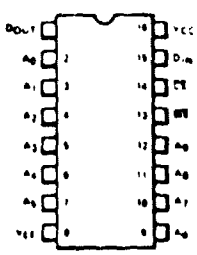
V_{CC} = Pin 16
V_{EE} = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F10415 and F10415A are fully decoded 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F10415 and F10415A to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10415s or F10415As can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is c[illegible]

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	See Note 4
F10415DC, F10415ADC	−5.46 V	−5.2 V	−4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
		−960		−810		+25°C		
		−900		−720		+75°C		
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C		
		−1850		−1650		+25°C		
		−1830		−1625		+75°C		
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA}	
		−980				+25°C		
		−920				+75°C		
V_{OLC}	Output Voltage LOW			−1645	mV	0°C		
				−1630		+25°C		
				−1605		+75°C		
V_{IH}	Input Voltage HIGH	−1145		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		−1105		−810		+25°C		
		−1045		−720		+75°C		
V_{IL}	Input Voltage LOW	−1870		−1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		−1850		−1475		+25°C		
		−1830		−1450		+75°C		
I_{IH}	Input Current HIGH			220	μA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	μA	+25°C	V_{IN} = V_{ILB}	
	All others	−50						
I_{EE}	Power Supply Current		−90		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)	−150	−105			0°C		

NOTES

1 Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

2 The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

3 Typical values are at V_{EE} = −5.2 V, T_A = 25°C and maximum loading.

4 Guaranteed with transverse air flow exceeding 400 linear F P M and 2 minute warm up period. Typical resistance values of the package are
θ_{JA} (Junction to Ambient) = 90 C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F P M air flow)
θ_{JC} (Junction to Case) = 25°C/Watt

5 The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

6 DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET

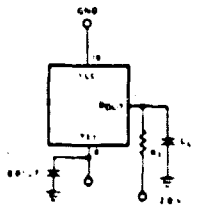
The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an alphabetic scale. The extremities of the scale are "A" the value closest to positive infinity, "B" the value closest to negative infinity.

AC CHARACTERISTICS: V_{EE} = −5.2 V ± 5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C

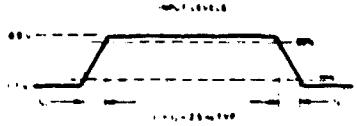
SYMBOL	PARAMETER	F10415ADC* MIN	F10415ADC* TYP (Note 3)	F10415ADC* MAX	F10415DC MIN	F10415DC TYP (Note 3)	F10415DC MAX	UNITS	CONDITIONS
READ MODE									Fig 1a & b measured at
t_{ACS}	Chip Select Access Time		5			7	10	ns	50 % of input swing to
t_{RCS}	Chip Select Recovery Time		5			7	10	ns	output (V_{ILA} for V_{OL}
t_{AA}	Address Access Time		12	20		25	35	ns	or V_{IHB} for V_{OH})
WRITE MODE									
t_W	Write Pulse Width (to Guarantee writing)	12	9		25	20		ns	F10415A t_{WSA} = 8 ns; F10415 t_{WSA} = 20 ns
t_{WSD}	Data Set-up Time Prior to Write		0		5	0		ns	
t_{WHD}	Data Hold Time After Write		0		5	0			
t_{WSA}	Address Set-up Time Prior to Write		5		8	5		ns	F10415A t_W = 12 ns; F10415 t_W = 25 ns
t_{WHA}	Address Hold Time After Write		0		4	1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		0		5	0		ns	Fig. 2 measured at 50 % of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHCS}	Chip Select Hold Time After Write		0		5	0		ns	
t_{WS}	Write Disable Time		5			7	10	ns	
t_{WR}	Write Recovery Time		7			7	10	ns	
RISE TIME AND FALL TIME									
t_r	Output Rise Time		5			5		ns	Measured between 20 % and 80 % points (Fig. 1a)
t_f	Output Fall Time		5			5		ns	
CAPACITANCE									
C_{IN}	Input Pin Capacitance		4	5		4	5	pF	Measure with a Pulse
C_{OUT}	Output Pin Capacitance		7	8		7	8	pF	Technique

*Note: The F10415A AC limits are preliminary

LOADING CONDITIONS



INPUT LEVELS

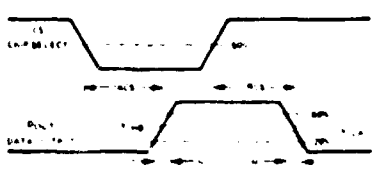


All Timing Measurements Referenced to 50% of Input Levels

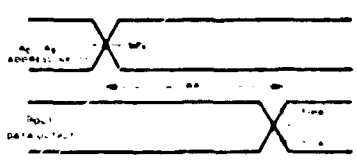
C_L = 30 pF including Jig and Stray Capacitance

R_T = 50 Ω Termination of Scope

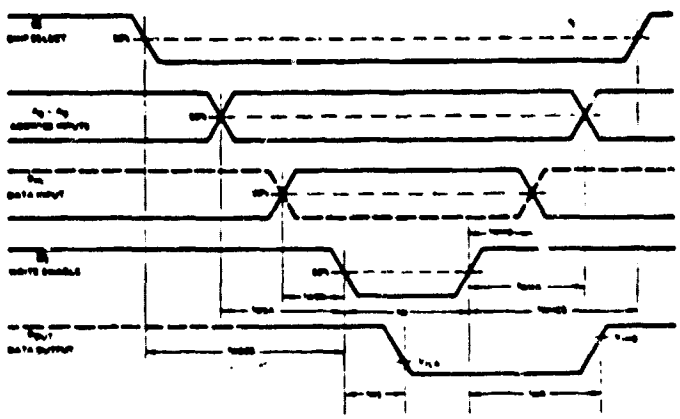
READ MODE PROPAGATION DELAY FROM CHIP SELECT



READ MODE PROPAGATION DELAY FROM ADDRESS

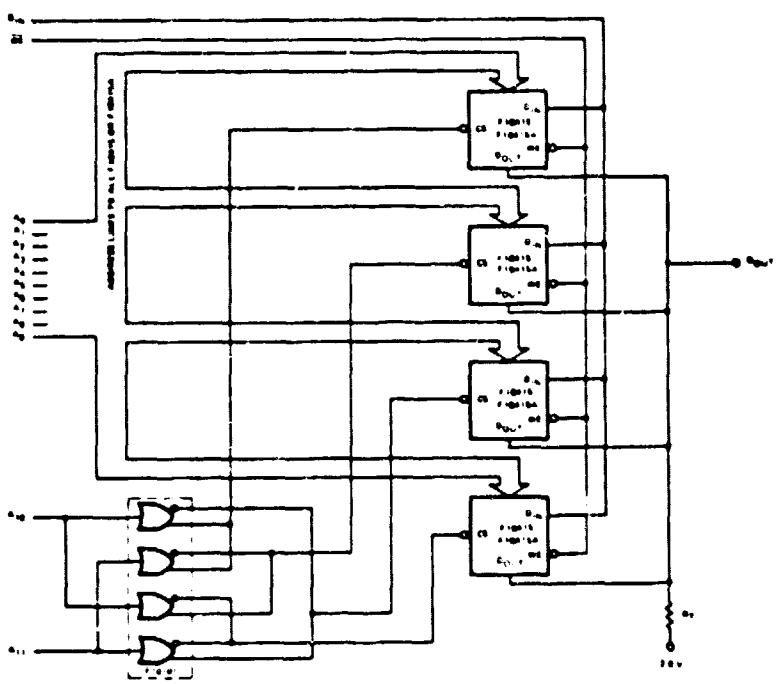


WRITE MODE



NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

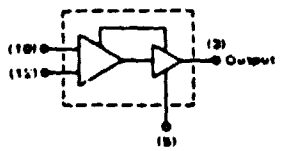
APPLICATIONS



4096-WORD X 1-BIT SYSTEM

VOLTAGE-CONTROLLED OSCILLATOR

MC1648



Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 90 Ω typ
Power Dissipation = 150 mW typ/pkg (−5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

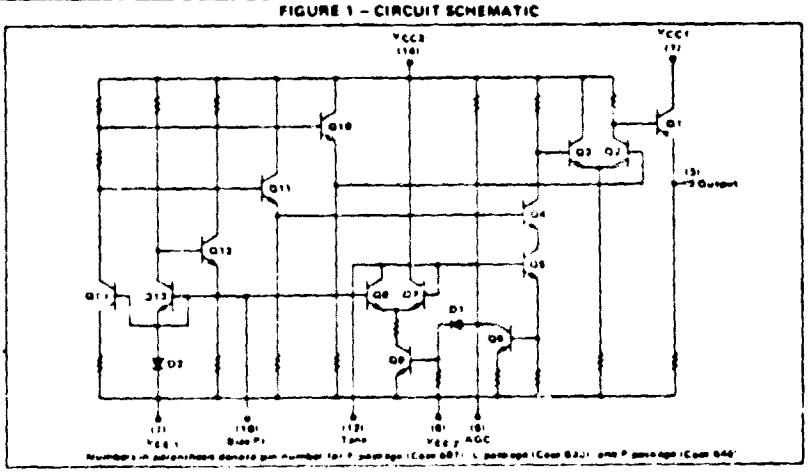
The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity (See Figure 2).

The MC1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

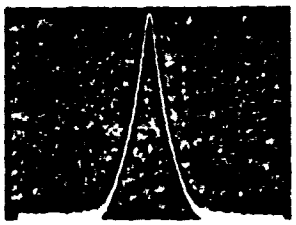
SUPPLY VOLTAGE	GND PIN	SUPPLY PIN
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC



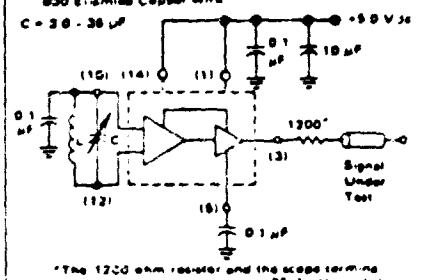
Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



RW = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div

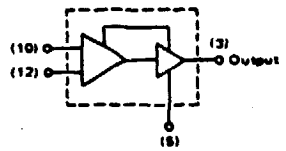
L: Micro Metals toroid #T20-2; 5 turns
#30 Enamelled Copper wire
C = 3.0 – 36 pF



*The 1200 ohm resistor and the scope termination impedance constitute a 26:1 attenuator probe. Loss shall be CT-0730 or equivalent.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts

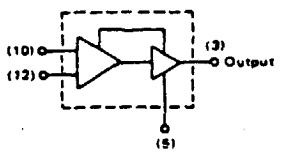


Characteristic	Symbol	Pin Under Test	MC1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage/Current Applied to Pins Listed Below: V_{in} max	V_{IL} min	V_{CC}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	60	—	—	mAdc	—	—	5.0	—	7,8
Logic "1" Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	5.0	3	7,8
Logic "0" Output Voltage	V_{OL}	3	3.10	3.40	3.39	3.63	3.72	3.96	Vdc	12	—	5.0	3	7,8
Bias Voltage	V_{Bias}*	10	1.51	1.85	1.48	1.70	1.20	1.56	Vdc	—	—	5.0	—	7,8
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak-to-Peak Sine Wave Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	5.0	3	7,8
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	5.0	3	7,8
Operation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	5.0	3	7,8

*This measurement guarantees the dc potential at the bias point for purpose of incorporating a varactor tuning diode at this point

ELECTRICAL CHARACTERISTICS

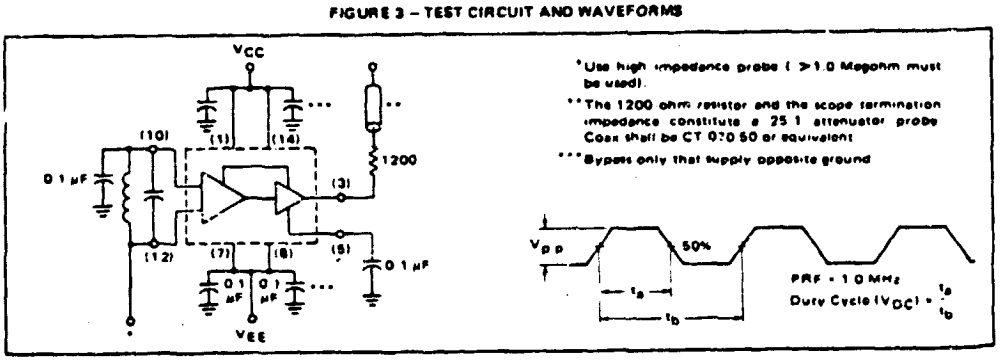
Supply Voltage = -5.2 volts



Characteristic	Symbol	Pin Under Test	MC1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage/Current Applied to Pins Listed Below: V_{in} max	V_{IL} min	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	41	—	—	mAdc	—	—	-5.2	—	1,14
Logic "1" Output Voltage	V_{OH}	3	-1.049	-0.815	-0.950	-0.750	-0.890	-0.650	Vdc	—	12	-5.2	3	1,14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	-5.2	3	1,14
Bias Voltage	V_{Bias}*	10	-3.090	-3.240	-3.080	-3.280	-3.030	-3.430	Vdc	—	—	-5.2	—	1,14
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak-to-Peak Sine Wave Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	-5.2	3	1,14
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	-5.2	3	1,14
Operation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	-5.2	3	1,14

*This measurement guarantees the dc potential at the bias point for purpose of incorporating a varactor tuning diode at this point

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



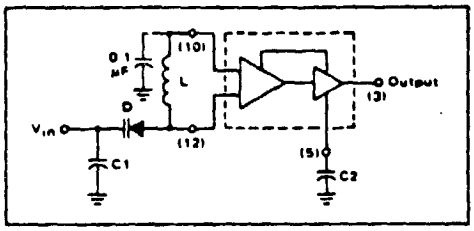
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

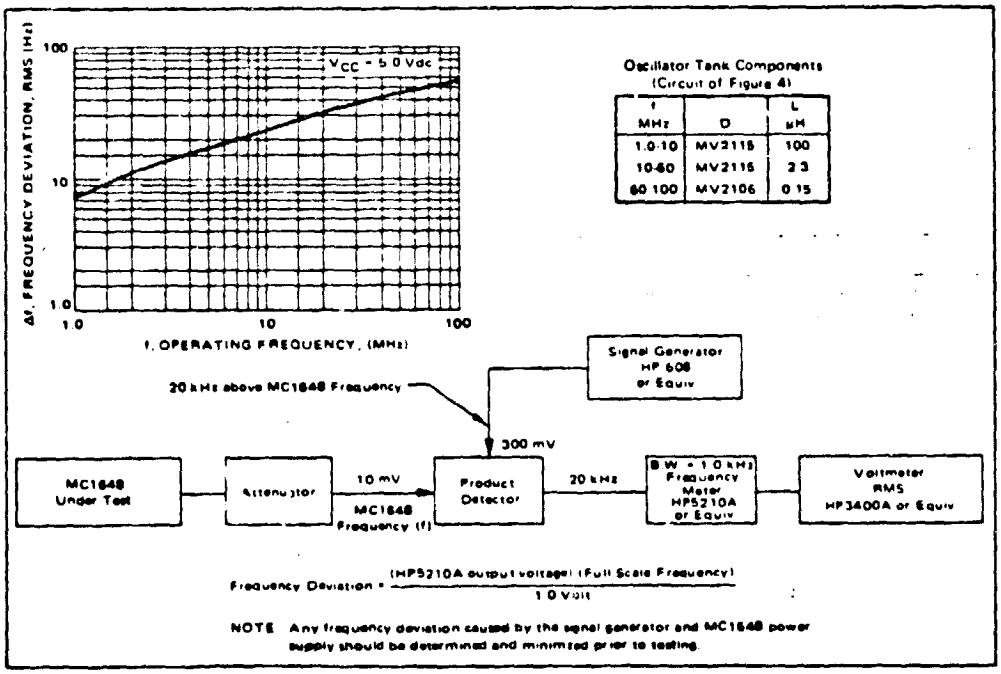
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} (≈ 1.4 V for positive supply operation).

FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



NOTE Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimized prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. T_A = 25°C

FIGURE 6

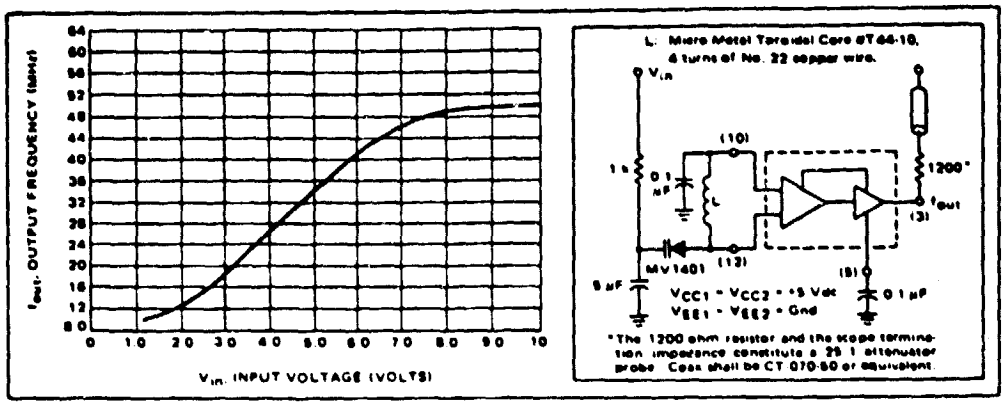


FIGURE 7

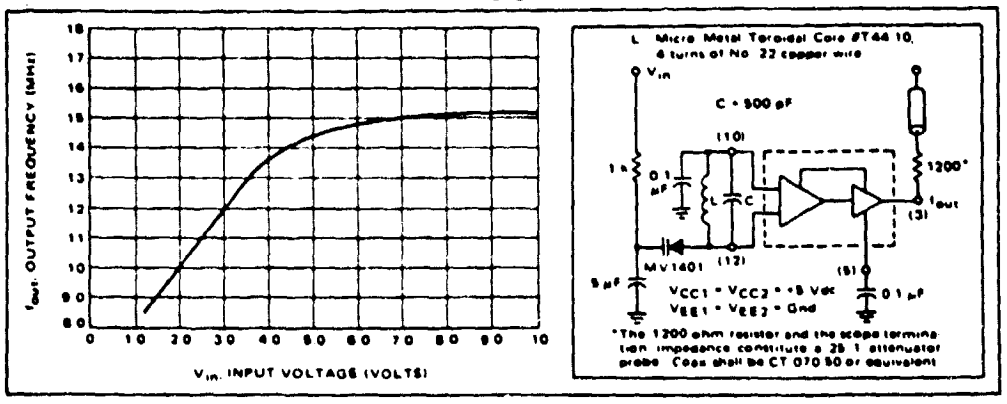
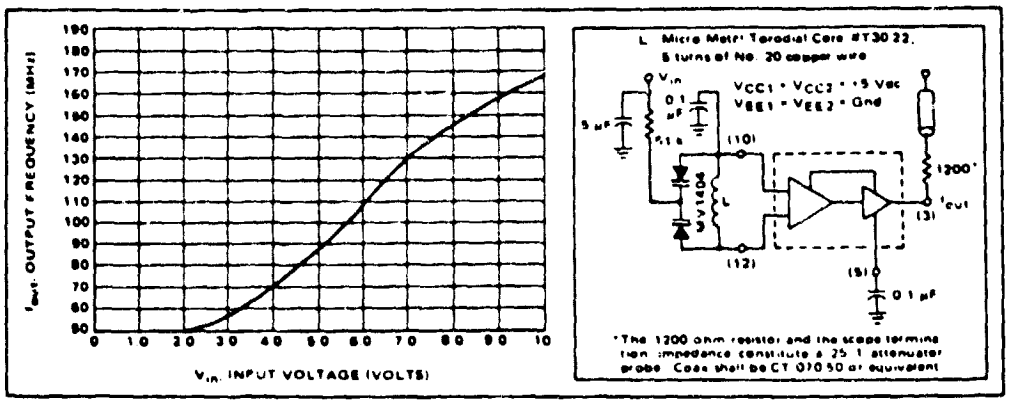


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi \sqrt{L\ (C_D\ (max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter, $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN 535, AN-553, AN 564, AN 594, or Phase Locked Loop Systems Data Book.

PHASE-FREQUENCY DETECTOR

MECL Phase-Locked Loop Components

MOTOROLA

MC12040 • MC12540

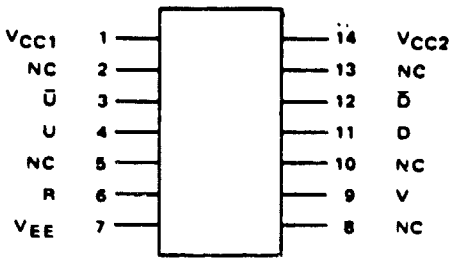
ISSUE C

The MC12040/MC12540 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is very similar to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

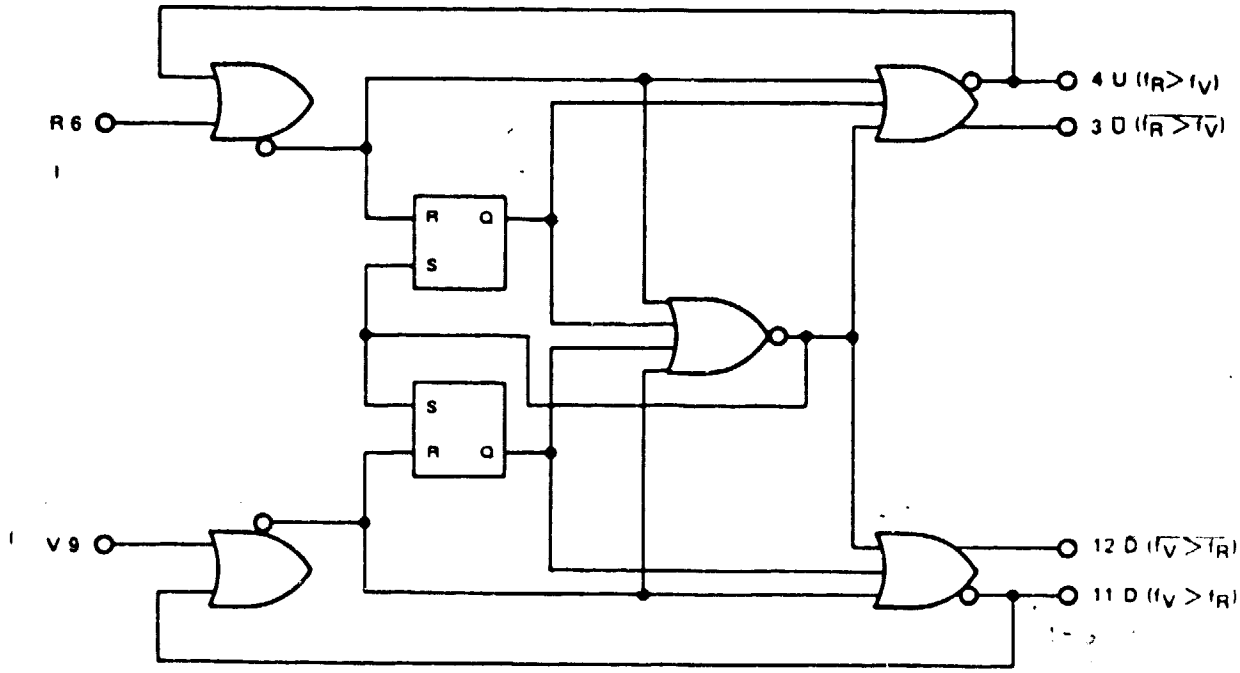
- Operating Frequency = 70 MHz Min. -55° to +125°C

MC12040 – MC12540
CERAMIC PACKAGE
CASE 632-02

MC12040
P SUFFIX
PLASTIC PACKAGE
CASE 648



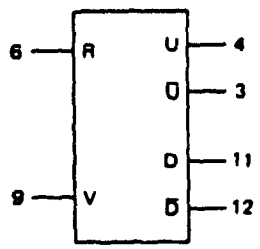
NC – No Connection



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{CC3} = Pin 7

ELECTRICAL CHARACTERISTICS – MC12040

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



INPUT		OUTPUT			
R	V	U	D	D	D
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = Don't Care

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Supply Voltage = -5.2V

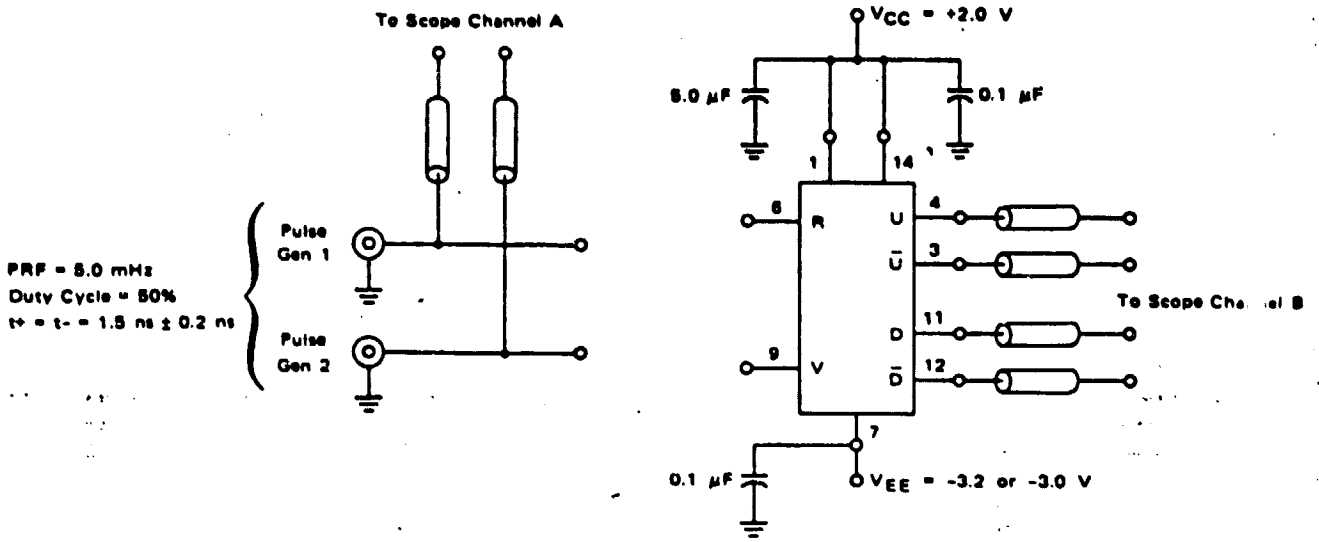
Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	-	-	-120	-60	-	-	mAdc	-	-	-	-	7	1,14
Input Current	I_{INH}	6 9	-	-	-	350 350	-	-	μAdc μAdc	6 9	-	-	-	7 7	1,14 1,14
Logic "1" Output Voltage	V_{OH} ①	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	-	-	-	-	7	1,14
Logic "0" Output Voltage	V_{OL} ①	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	-	-	-	-	7	1,14
Logic "1" Threshold Voltage	V_{OHA} ②	3 4 11 12	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	6.9	-	7	1,14
Logic "0" Threshold Voltage	V_{OLA} ②	3 4 11 12	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	9 6 9 6	6 9 6 9	7	1,14

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

Supply Voltage = +5.0V

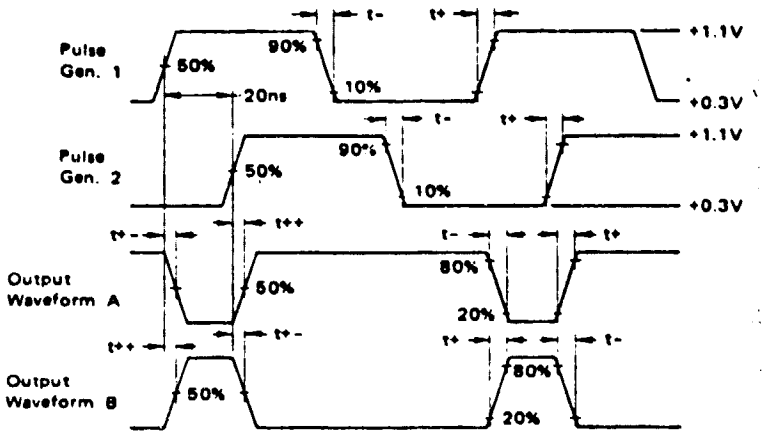
Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7			-115	-60	-		mAdc		-			1,14	7
Input Current	I_{INH}	6 9				350 350	-		μAdc μAdc	6 9				1,14 1,14	7 7
	I_{INL}	6 9			0.5 0.5	-	-		μAdc μAdc		6 9		-	1,14 1,14	7 7
Logic "1" Output Voltage	V_{OH} ①	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc	-	-	-	-	1,14	7
Logic "0" Output Voltage	V_{OL} ①	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc	-	-	-	-	1,14	7
Logic "1" Threshold Voltage	V_{OHA} ②	3 4 11 12	3.980	-	4.020	-	4.080	-	Vdc	-	-	6.9	-	1,14	7
Logic "0" Threshold Voltage	V_{OLA} ②	3 4 11 12	-	3.450	-	3.460	-	3.490	Vdc	-	-	9 6 9 6	6 9 6 9	1,14	7

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω (MC12040) and 100 Ω (MC12540) resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040 0°C Max	MC12040 +25°C Max	MC12040 +75°C Max	MC12540 -55°C Max	MC12540 +25°C Max	MC12540 +125°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	VEE -3.0 or -3.2 V	VCC +2.0 V
Propagation Delay	t_{6+4+}	6 4	B	4.6	4.6	5.6	4.6	4.6	5.0	ns	6	9	7	1,14
	t_{6+12+}	6 12	A	6.0	6.0	7.2	6.0	6.0	6.6		9	6		
	t_{6+3-}	6 3	A	4.5	4.5	5.5	4.5	4.5	4.9		6	9		
	t_{6+11-}	6 11	B	6.4	6.4	7.7	6.4	6.4	7.0		9	6		
	t_{9+11+}	9 11	B	4.6	4.6	5.6	4.6	4.6	5.0		9	6		
	t_{9+3+}	9 3	A	6.0	6.0	7.2	6.0	6.0	6.6		6	9		
	t_{9+12-}	9 12	A	4.5	4.5	5.5	4.5	4.5	4.9		9	6		
	t_{9+4-}	9 4	B	6.4	6.4	7.7	6.4	6.4	7.0		6	9		
Output Rise Time	t_{3+}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4+}	4	B								6	9		
	t_{11+}	11	B								9	6		
	t_{12+}	12	A								9	6		
Output Fall Time	t_{3-}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4-}	4	B								6	9		
	t_{11-}	11	B								9	6		
	t_{12-}	12	A								9	6		

APPLICATIONS INFORMATION

The MC12040/MC12540 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of ± 2π radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle – that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is acomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\bar{U}$ and $\bar{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\bar{U}$ and $\bar{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040/MC12540 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4344/MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 1 – TIMING DIAGRAM

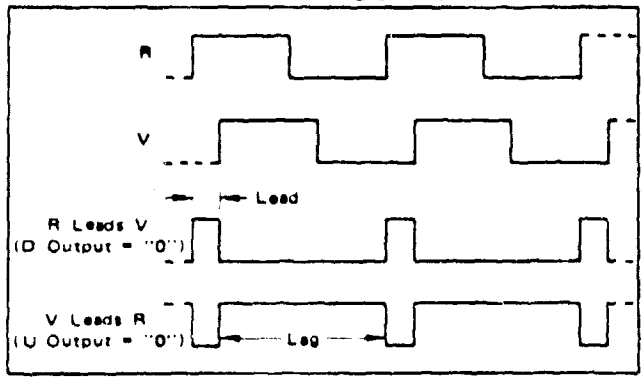
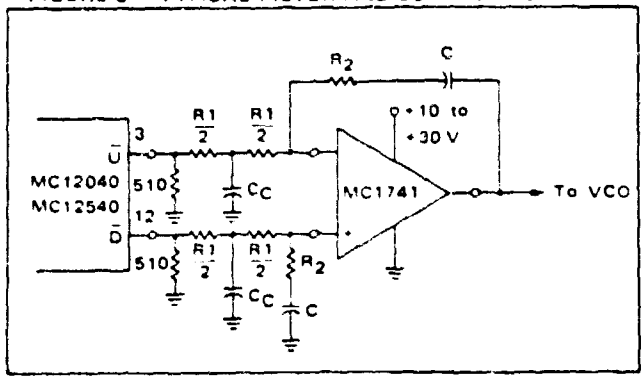


FIGURE 2 – TYPICAL FILTER AND SUMMING NETWORK



Am687·Am687A

Dual Voltage Comparators

Distinctive Characteristics

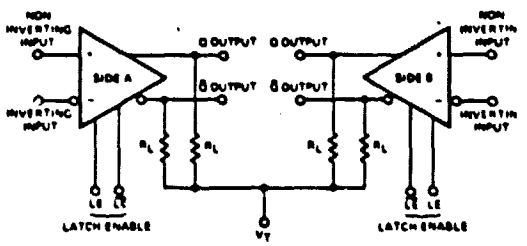
- 8.0ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assembly of hybrid products.
- Available in the hermetic dual-in-line package.

FUNCTIONAL DESCRIPTION

The Am687 and Am687A are fast dual voltage comparators constructed on a single silicon chip with an advanced high-frequency process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

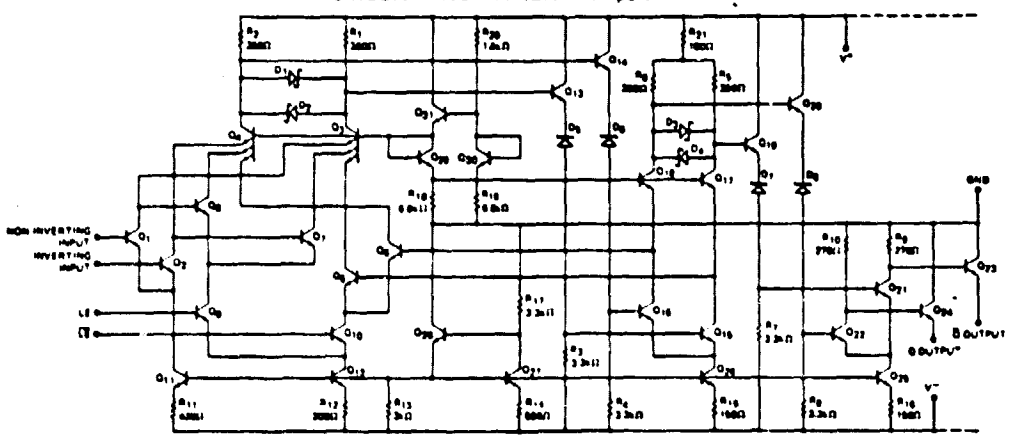
The comparators are similar to the Am685 high-speed comparator but have been designed to operate from a 5V positive supply (instead of 8V), dissipating less power than two Am685's. Separate latch functions are provided to allow each comparator to be independently used in a sample-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and $\overline{LE}$ is LOW, the comparator functions normally. When LE is driven LOW and $\overline{LE}$ is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

FUNCTIONAL DIAGRAM



The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50-200Ω connected to −2.0V, or 200-2000Ω connected to −5.2V.

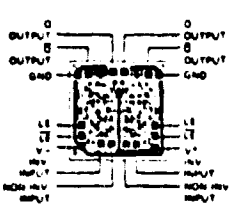
CIRCUIT DIAGRAM (Each Comparator)



ORDERING INFORMATION

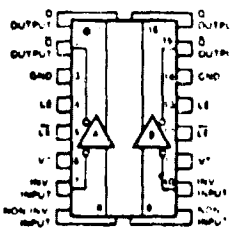
Part Number	Package Type	Temperature Range	Order Number
Am687A	DIP	−30°C to +85°C	AM687ADL
Am687A	DIP	−55°C to +125°C	AM687ADM
Am687	DIP	−30°C to +85°C	AM687DL
Am687	DIP	−55°C to +125°C	AM687DM
Am687	Dice	−30°C to +85°C	AM687XL
Am687	Dice	−55°C to +125°C	AM687XM

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" × 0.066"

CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orient.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Output Voltage	±4 V
Differential Input Voltage	±6 V
Input Current	30 mA
Power Dissipation (Note 2)	600 mW

Operating Temperature Range	
Am687-L, Am687A-L	−30°C to +85°C
Am687-M, Am687A-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am687A-L Am687-L Min.	Am687A-L Am687-L Max.	Am687A-M Am687-M Min.	Am687A-M Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \le 100\,\Omega$, $T_A = 25°C$	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \le 100\,\Omega$	−3.5	+3.5	−3.0	+3.0	mV
ΔV_{OS}	Average Temperature Coefficient of Input Offset Voltage	$R_S \le 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$25°C \le T_A \le T_{A(max.)}$	−1.0	+1.0	−1.0	+1.0	µA
		$T_A = T_{A(min.)}$	−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$25°C \le T_A \le T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \le 100\,\Omega$, $-3.3 \le V_{CM} \le +2.7$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \le 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

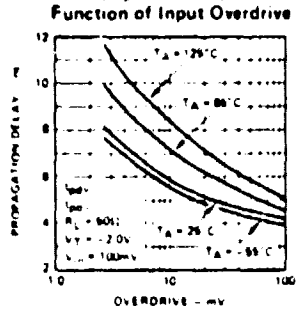
Switching Characteristics (V_{in} = 100 mV, V_{OD} = 5 mV)

Symbol	Parameter	Conditions					
t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \le T_A \le 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \le T_A \le 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	$T_A = 25°C$		4.0		4.0	ns

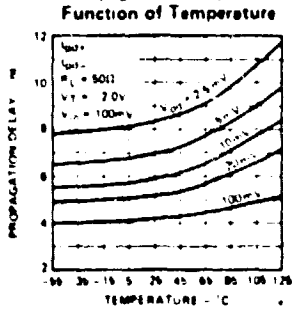
Notes:
2. Derate at 9mW °C for operation at ambient temperatures above +116°C
3. Unless otherwise specified $V^+ = +5.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$, all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

PERFORMANCE CURVES

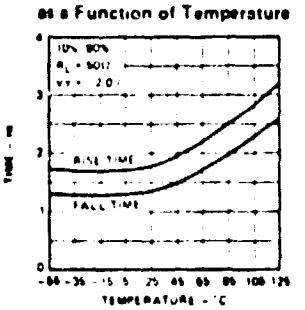
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



2. TTL COMPONENT DATA

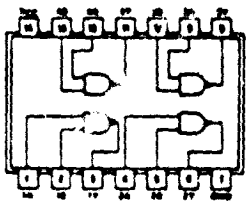
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
$Y = \overline{AB}$

See page 6-4



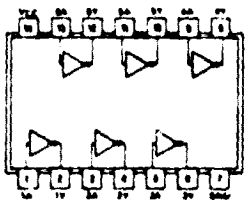
SN5403 (J)
SN54L03 (J)
SN54LS03 (J, W)
SN54S03 (J, W)
SN7403 (J, N)
SN74L03 (J, N)
SN74LS03 (J, N)
SN74S03 (J, N)

HEX INVERTERS

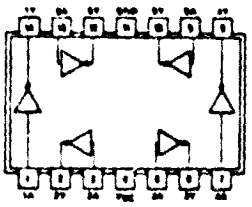
04

positive logic:
$Y = \overline{A}$

See page 6-2



SN5404 (J)
SN54H04 (J)
SN54L04 (J)
SN54LS04 (J, W)
SN54S04 (J, W)
SN7404 (J, N)
SN74H04 (J, N)
SN74L04 (J, N)
SN74LS04 (J, N)
SN74S04 (J, N)



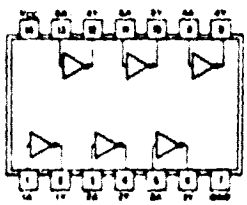
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

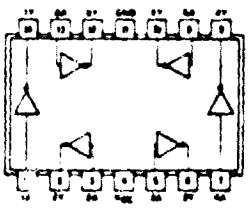
05

positive logic:
$Y = \overline{A}$

See page 6-4



SN5405 (J)
SN54H05 (J)
SN54LS05 (J, W)
SN54S05 (J, W)
SN7405 (J, N)
SN74H05 (J, N)
SN74LS05 (J, N)
SN74S05 (J, N)



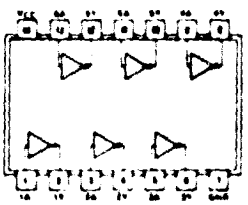
SN5405 (W)
SN54H05 (W)

HEX INVERTER BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

06

positive logic:
$Y = \overline{A}$

See page 6-24



SN5406 (J, W)
SN7406 (J, N)

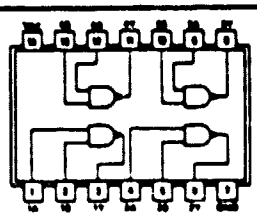
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

00

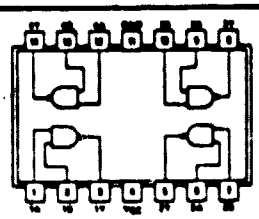
positive logic:
$Y = \overline{AB}$

See page 6-2



SN5400 (J)
SN54H00 (J)
SN54L00 (J)
SN54LS00 (J, W)
SN54S00 (J, W)

SN7400 (J, N)
SN74H00 (J, N)
SN74L00 (J, N)
SN74LS00 (J, N)
SN74S00 (J, N)



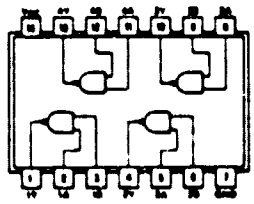
SN5400 (W)
SN54H00 (W)
SN54L00 (T)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

01

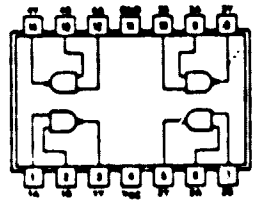
positive logic:
$Y = \overline{AB}$

See page 6-4

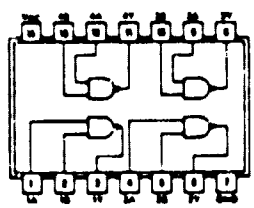


SN5401 (J)
SN54LS01 (J, W)

SN7401 (J, N)
SN74LS01 (J, N)



SN5401 (W)
SN54H01 (W)
SN54L01 (T)



SN54H01 (J)

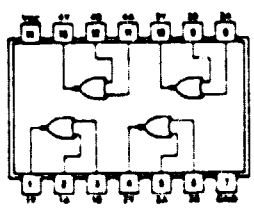
SN74H01 (J, N)

QUADRUPLE 2 INPUT POSITIVE-NOR GATES

02

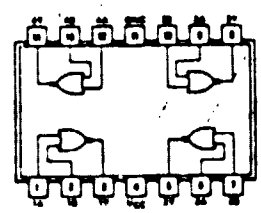
positive logic:
$Y = \overline{A+B}$

See page 6-6



SN5402 (J)
SN54L02 (J)
SN54LS02 (J, W)
SN54S02 (J, W)

SN7402 (J, N)
SN74L02 (J, N)
SN74LS02 (J, N)
SN74S02 (J, N)



SN5402 (W)
SN54L02 (T)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

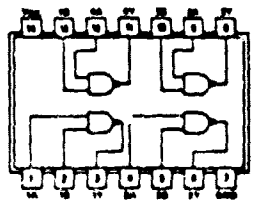
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

26

positive logic:
$Y = \overline{A \cdot B}$

See pages 6-24 and 6-26



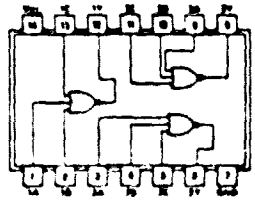
SN5426 (J)
SN54LS26 (J, W)
SN7426 (J, N)
SN74LS26 (J, N)

TRIPLE 3-INPUT
POSITIVE-NOR GATES

27

positive logic:
$Y = \overline{A+B+C}$

See page 6-8



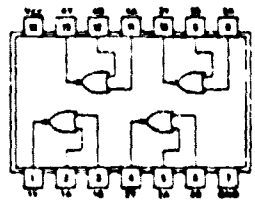
SN5427 (J, W)
SN54LS27 (J, W)
SN7427 (J, N)
SN74LS27 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

28

positive logic:
$Y = \overline{A+B}$

See page 6-20



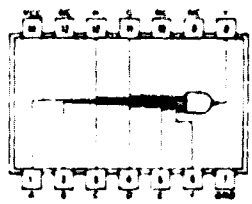
SN5428 (J, W)
SN54LS28 (J, W)
SN7428 (J, N)
SN74LS28 (J, N)

8-INPUT
POSITIVE NAND GATES

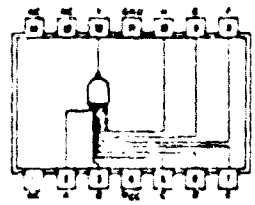
30

positive logic:
$Y = \overline{ABCDEFGH}$

See page 6-2



SN5430 (J)
SN54H30 (J)
SN54L30 (J)
SN54LS30 (J, W)
SN54S30 (J, W)
SN7430 (J, N)
SN74H30 (J, N)
SN74L30 (J, N)
SN74LS30 (J, N)
SN74S30 (J, N)



SN5430 (W)
SN54H30 (W)
SN54L30 (T)

NC – No internal connection

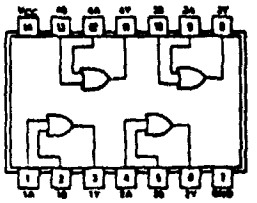
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-OR GATES

32

positive logic:
$Y = A+B$

See page 6-28



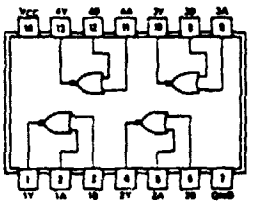
SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

33

positive logic:
$Y = \overline{A+B}$

See pages 6-24 and 6-26



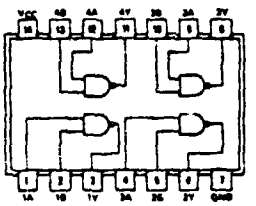
SN5433 (J, W) SN7433 (J, N)
SN54LS33 (J, W) SN74LS33 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

37

positive logic:
$Y = \overline{AB}$

See page 6-20



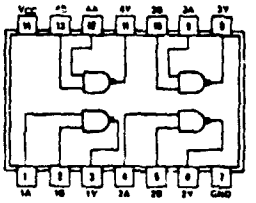
SN5437 (J, W) SN7437 (J, N)
SN54LS37 (J, W) SN74LS37 (J, N)
SN54S37 (J, W) SN74S37 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

38

positive logic:
$Y = \overline{AB}$

See pages 6-24 and 6-26



SN5438 (J, W) SN7438 (J, N)
SN54LS38 (J, W) SN74LS38 (J, N)
SN54S38 (J, W) SN74S38 (J, N)

1976

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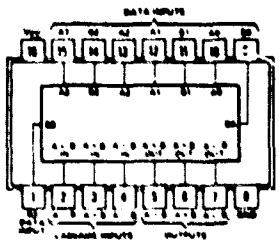
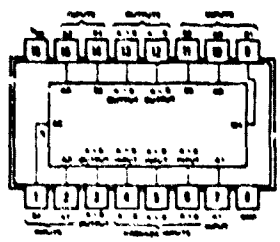
PIN ASSIGNMENTS (TOP VIEWS)

4 BIT MAGNITUDE COMPARATORS

85



SN5485 (J, W) SN7485 (J, N)
SN54LS85 (J, W) SN74LS85 (J, N)
SN54S85 (J, W) SN74S85 (J, N)

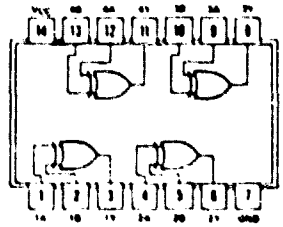


SN54L85 (J) SN74L85 (J, N)

See page 7-57

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = A\bar{B} + \bar{A}B$

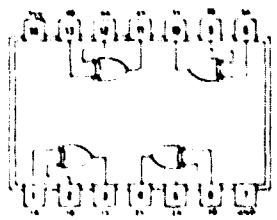


SN5486 (J, W) SN7486 (J, N)
SN54LS86 (J, W) SN74LS86 (J, N)
SN54S86 (J, W) SN74S86 (J, N)

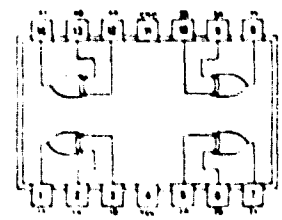
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



SN54L86 (J) SN74L86 (J, N)



SN54L86 (T)

See page 7-65

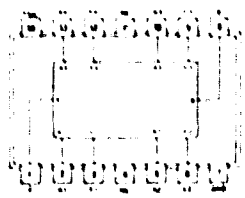
4 BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENTS

87

FUNCTION TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	A1	A2	A3	A4
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level, L = low level
A1, A2, A3, A4 = the level of the respective A input



SN54H87 (J, W) SN74H87 (J, N)
NC – No internal connection

See page 7-70

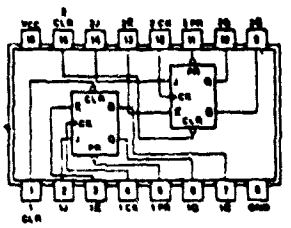
PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

109

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$



SN54109 (J, W) SN74109 (J, N)
SN54LS109A (J, W) SN74LS109A (J, N)

See pages 6-46 and 6-56

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

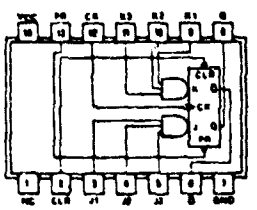
110

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

positive logic: J = J1·J2·J3
K = K1·K2·K3

See page 6-46



SN54110 (J, W) SN74110 (J, N)

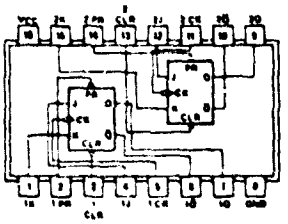
NC—No internal connection

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

111

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	



SN54111 (J, W) SN74111 (J, N)

See page 6-46

See explanation of function tables on page 3-8.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

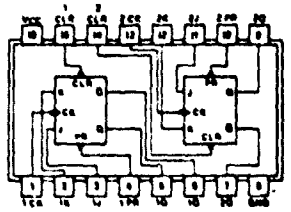
PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS112 (J, W) SN74LS112 (J, N)
SN54S112 (J, W) SN74S112 (J, N)

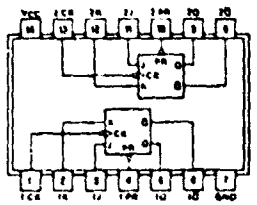
See pages 6-56 and 6-58

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

113

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS113 (J, W) SN74LS113 (J, N)
SN54S113 (J, W) SN74S113 (J, N)

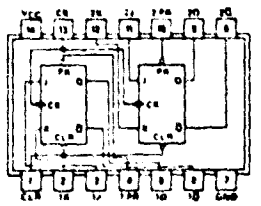
See pages 6-56 and 6-58

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

114

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS114 (J, W) SN74LS114 (J, N)
SN54S114 (J, W) SN74S114 (J, N)

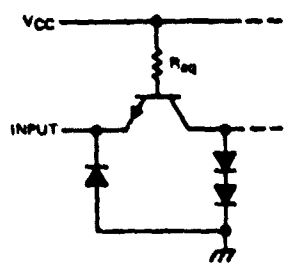
See pages 6-56 and 6-58

See explanation of function tables on page 3-8.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

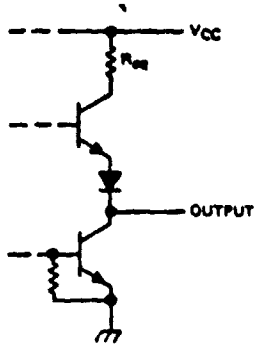
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



INPUT	Req NOM	
	'121	'L121
A1	4 kΩ	8 kΩ
A2	4 kΩ	8 kΩ
B	2 kΩ	4 kΩ

TYPICAL OF BOTH OUTPUTS



'121: R_{eq} = 130 Ω NOM
'L121: R_{eq} = 260 Ω NOM

recommended operating conditions

		54 FAMILY / 74 FAMILY	SN54121 / SN74121			SN54L121 / SN74L121			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−200	μA
Low-level output current, I_{OL}					16			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B		1			1			V/s
	Logic inputs, A1, A2		1			1			V/μs
Input pulse width, $t_{w(in)}$			50			100			ns
External timing resistance, R_{ext}		54 Family	1.4		30	1.4		30	kΩ
		74 Family	1.4		40	1.4		40	
External timing capacitance, C_{ext}			0		1000	0		1000	μF
Duty cycle	R_T = 2 kΩ				67			67	%
	R_T = MAX R_{ext}				70			90	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

TYPES SN54121, SN54L121, SN74121, SN74L121
MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

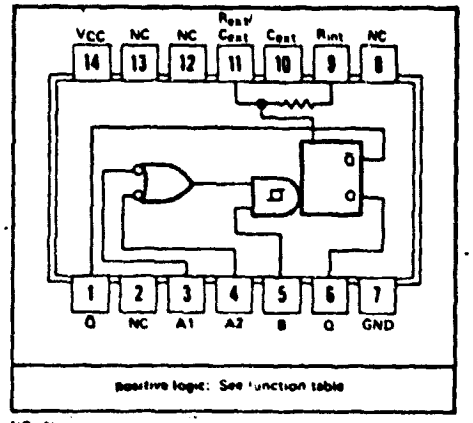
- **Programmable Output Pulse Width**
  With R_{int} . . . 35 ns Typ
  With R_{ext}/C_{ext} . . . 40 ns to 28 Seconds
- **Internal Compensation for Virtual Temperature Independence**
- **Jitter-Free Operation up to 90% Duty Cycle**
- **Inhibit Capability**

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

For explanation of function table symbols, see page 3-8.

SN54121 . . . J OR W PACKAGE
SN54L121 . . . J OR T PACKAGE
SN74121, SN74L121 . . . J OR N PACKAGE



NC—No internal connection

NOTES 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54121/SN54L121 and 2 kΩ to 40 kΩ for the SN74121/SN74L121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_T \ln 2 \approx 0.7\, C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse width jitter is allowed.

TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS*			SN74LS*			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.8		2.7	3.8		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 13	'LS122		6	11		6	11	mA
				'LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 12. To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 3 V to B and clear, and pulse A from 2 V to 0 V.
13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 14

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	$\overline{Q}$				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		$\overline{Q}$				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{wQ} = width of pulse at output Q
NOTE 14: Load circuit and voltage waveforms are shown on page 3-11.

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 7.

When $C_{ext} > 1000$ pF, the output pulse width is defined as:

$$t_w = 0.45 \cdot R_T \cdot C_{ext}$$

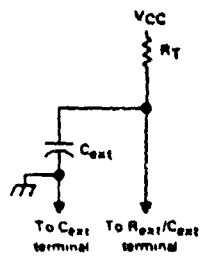
where

R_T is in kΩ (internal or external timing resistance.)

C_{ext} is in pF

t_w is in nanoseconds

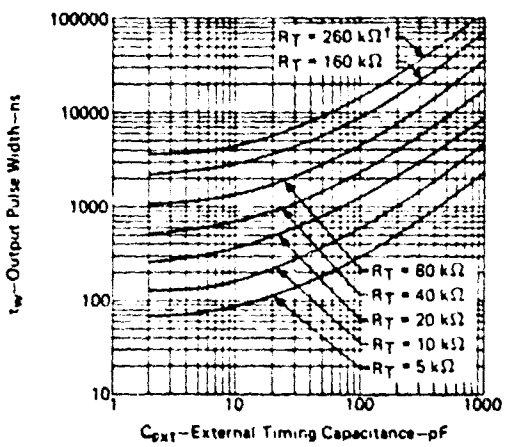
For best results, system ground should be applied to the C_{ext} terminal. The switching diode is not needed for electrolytic capacitance applications.



TIMING COMPONENT CONNECTIONS

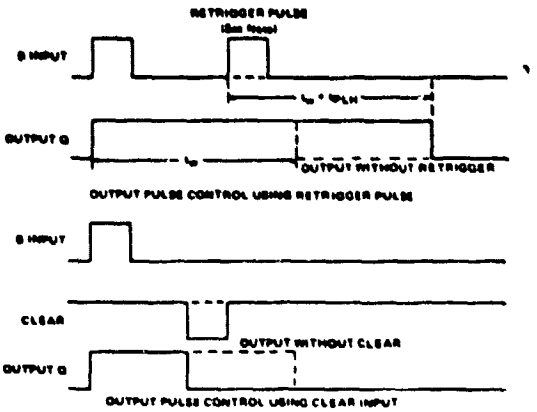
4-63

'LS122, 'LS123
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

description (continued)

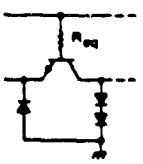
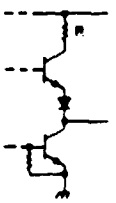


NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

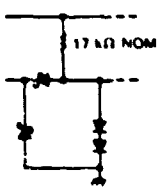
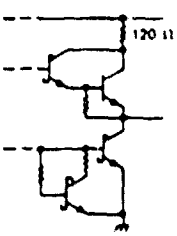
FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs

'122, '123, 'L122, 'L123 CIRCUITS

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS
	
Clear inputs of '122, '123: R_{eq} = 2 kΩ NOM Other inputs of '122, '123: R_{eq} = 4 kΩ NOM Clear inputs of 'L122, 'L123: R_{eq} = 4 kΩ NOM Other inputs of 'L122, 'L123: R_{eq} = 8 kΩ NOM	'122, '123: R = 100 Ω NOM 'L122, 'L123: R = 200 Ω NOM

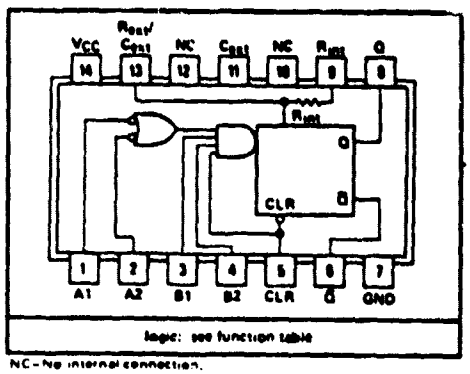
'LS122, 'LS123 CIRCUITS

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS
	

TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123, SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- '122, 'L122, 'LS122 Have Internal Timing Resistors

SN54122, SN54LS122 . . . J OR W
SN54L122 . . . J OR T
SN74122, SN74L122, SN74LS122 . . . J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

NC – No internal connection.

'122, 'L122, 'LS122
FUNCTION TABLE

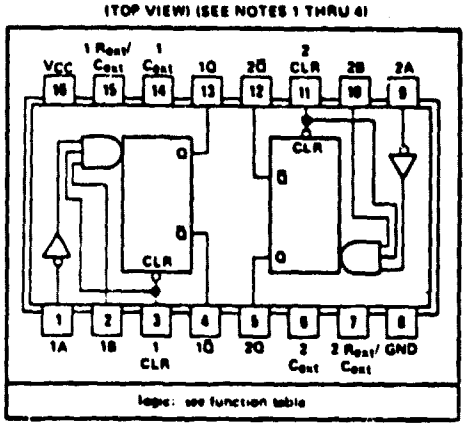
INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

'123, 'L123, 'LS123
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

See explanation of function tables on page 3-8.

SN54123, SN54LS123 . . . J OR W
SN54L123 . . . J
SN74123, SN74L123, SN74LS123 . . . J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, 'L122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122, 'L122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

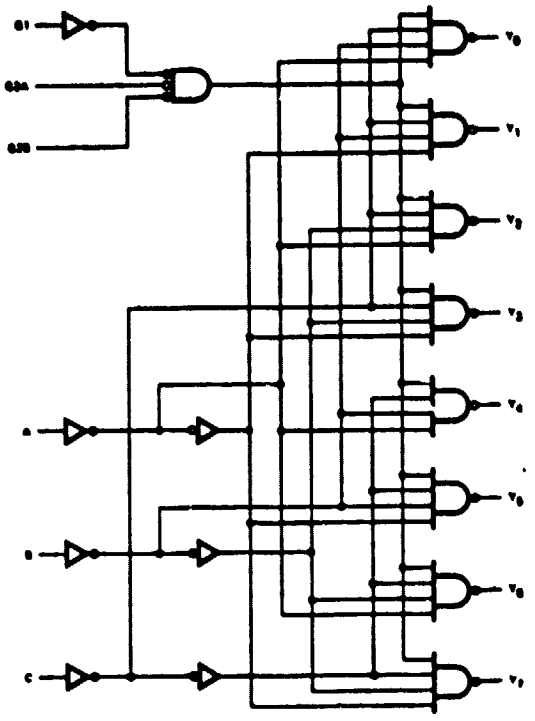
Am25LS138 • Am54LS/74LS138

3-Line To 8-Line Decoder/Demultiplexer

DISTINCTIVE CHARACTERISTICS

- Inverting and non-inverting enable inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440µA source current
- 100% product assurance screening to MIL-STD-883 requirements

LOGIC DIAGRAM



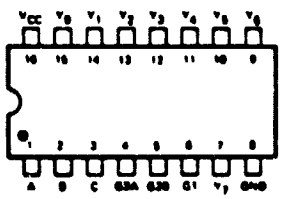
FUNCTIONAL DESCRIPTION

The Am25LS138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

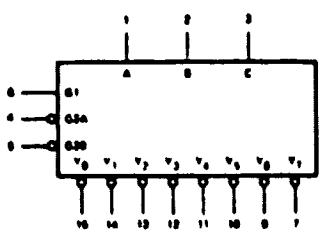
The Am54LS/74LS138 is a standard performance version of the Am25LS138. See appropriate electrical characteristic tables for detailed Am25LS improvements.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ELECTRICAL CHARACTERISTICS Am25LS138

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400µA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4mA V_{IN} = V_{IH} or V_{IL} I_{OL} = 8mA				0.4 0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 4)			6.3	10	mA

ELECTRICAL CHARACTERISTICS Am54LS/74LS138

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400µA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. All, I_{OL} = 4mA V_{IN} = V_{IH} or V_{IL} 74LS only, I_{OL} = 8mA				0.4 0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN. I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 4)			6.3	10	mA

Notes 1 For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2 Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3 Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4 Outputs enabled and open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +VCC max
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25LS153 • Am54LS/74LS153
Am25LS253 • Am54LS/74LS253

Dual 4-Line To 1-Line Data Selectors/Multiplexers

DISTINCTIVE CHARACTERISTICS

- Performs serial to parallel conversion
- Standard, 'LS153, and three-state, 'LS253, output versions
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440µA source current
- 100% product assurance screening to MIL-STD-883 requirements

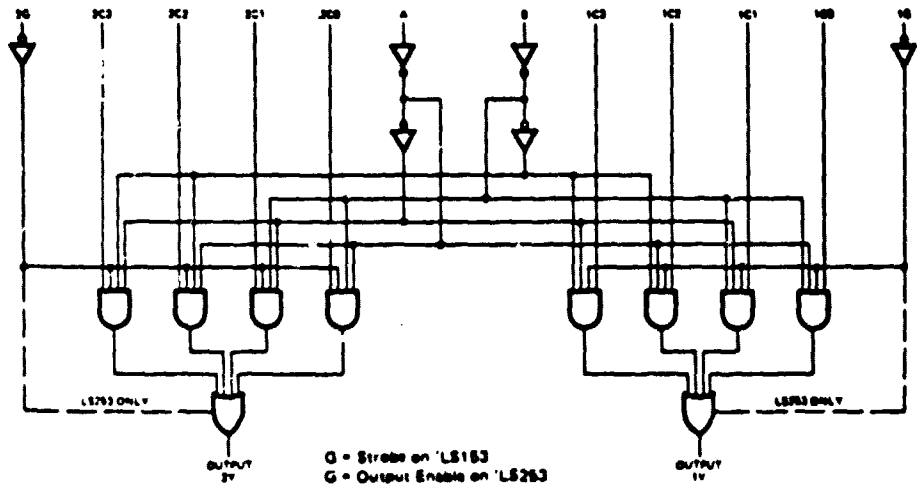
FUNCTIONAL DESCRIPTION

These dual four-input multiplexers provide the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am25LS153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

The Am25LS253 features a three-state output to interface with bus-organized systems. Each section of the Am25LS253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

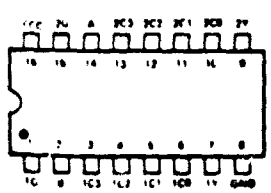
The Am54LS/74LS153 and 253 are standard performance versions of the Am25LS153 and 253. See appropriate electrical characteristic tables for detailed Am25LS improvements.

LOGIC DIAGRAM



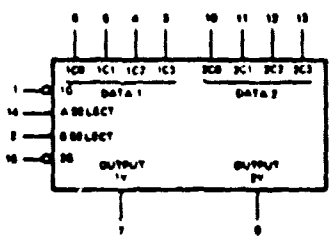
G = Strobe on 'LS153
G = Output Enable on 'LS253

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

Am54LS/74LS153 • Am54LS/74LS253

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	54LS153	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −400µA	2.5	3.4		Volts
		74LS153			2.7	3.4		
		54LS253		I_{OH} = −1mA	2.4	3.4		
		74LS253		I_{OH} = −2.6mA	2.4	3.2		
V_{OL}	Output LOW Voltage			All, I_{OL} = 4mA			0.4	Volts
				74LS only, I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs	54LS			0.7	Volts
				74LS			0.8	
V_I	Input Clamp Voltage		V_{CC} = MAX., V_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current		V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{OZ}	Off-State (HIGH Impedance) Output Current Am54LS/74LS253 Only		V_{CC} = MAX.	V_O = 2.4V			20	µA
				V_O = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX.		−15		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX. (Note 4)	LS153		6.2	10	mA
				LS253		7	12	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all outputs open and all inputs grounded.

3

Am25LS153/54LS153
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Data to Output		10	15		10	15	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			10	16		17	26		
t_{PLH}	Select to Output		19	29		19	29	ns	
t_{PHL}			15	23		25	38		
t_{PLH}	Strobe to Output		16	24		16	24	ns	
t_{PHL}			12	18		21	32		

Am25LS153 ONLY
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Data to Output		24		27	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			25		29		
t_{PLH}	Select to Output		42		48	ns	
t_{PHL}			34		39		
t_{PLH}	Strobe to Output		36		41	ns	
t_{PHL}			28		32		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS157 • Am54LS/74LS157
Am25LS158 • Am54LS/74LS158

Quadruple 2-Line To 1-Line Data Selectors/Multiplexers

DISTINCTIVE CHARACTERISTICS

- Selects four of eight data inputs with single select line and overriding strobe
- Inverting 'LS158 and Non-inverting 'LS157 configurations
- Standard TTL outputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

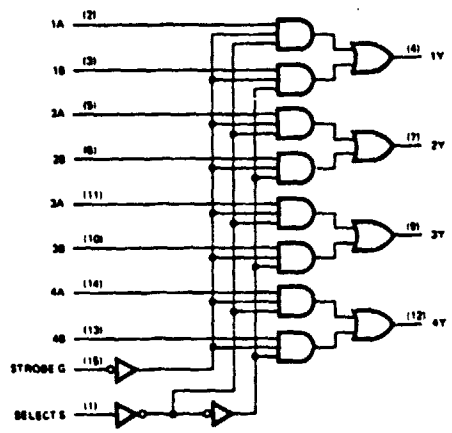
These data selectors/multiplexers are used to select a 4-bit word from one of two sources. The four outputs at the Am25LS157 present true data with respect to the input data. The four outputs of the Am25LS158 present inverted data with respect to the inputs and also minimize propagation delay. A common active-HIGH strobe (active-LOW enable) is provided on all devices.

A single select line, S, is used to select one of the two multiplexer input words. When the select is LOW, the A input word is present at the output. When the select is HIGH, the B input word is present at the output.

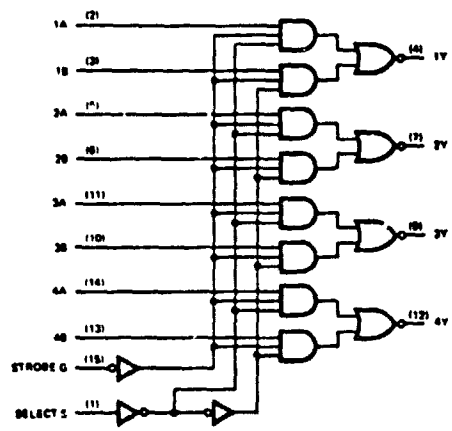
The Am54LS/74LS157 and 158 are standard performance versions of the Am25LS157 and 158. See appropriate electrical characteristic tables for detailed Am25LS improvements.

LOGIC DIAGRAMS

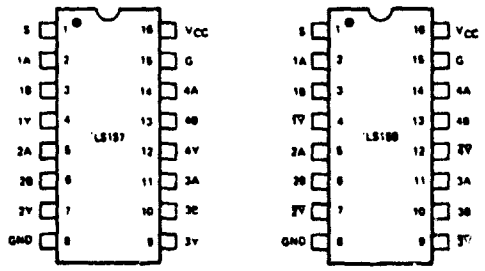
Am25LS157
Am54LS/74LS157



Am25LS158
Am54LS/74LS158

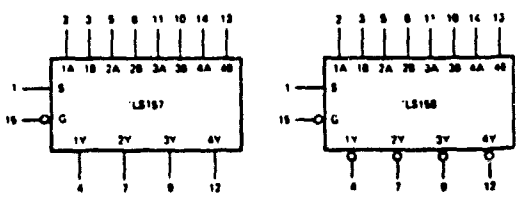


CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am25LS157 • Am25LS158

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440µA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	S or G			−0.36	mA
			A or B			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	S or G			20	µA
			A or B			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	S or G			0.1	mA
			A or B			0.1	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	LS157		9.7	16	mA
			LS158		4.8	8	

Notes 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all outputs open and 4.5V applied to all inputs.

3

Am54LS/74LS157 • Am54LS/74LS158

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400µA, V_{IN} = V_{IH} or V_{IL}	Am54LS	2.5	3.4		Volts
			Am74LS	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	All, I_{OL} = 4mA			0.4	Volts
			74LS only, I_{OH} = 8mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	Am54LS			0.7	Volts
			Am74LS			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	S or G			40	µA
			A or B			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	S or G			0.2	mA
			A or B			0.1	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (Note 4)	LS157		9.7	16	mA
			LS158		4.8	8	

Notes 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all outputs open and 4.5V applied to all inputs.

Am25LS160A/161A/162A/163A
Am54LS/74LS160A/161A/162A/163A

Synchronous Four-Bit Counters

DISTINCTIVE CHARACTERISTICS

- Synchrunous presettable counters
- Decade ('LS160A and 'LS162A) and binary ('LS161A and 'LS163A) counters
- Asynchronous ('LS160A and 'LS161A) and synchronous ('LS162A and 'LS163A) clear inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440µA source current
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS160A, Am25LS161A, Am25LS162A and Am25LS163A synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am25LS160A and Am25LS162A are decade counters and the Am25LS161A and Am25LS163A are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. The load need meet only the set-up and hold time requirements with respect to the clock.

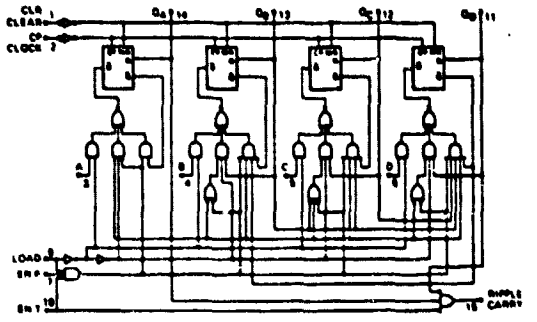
The Am25LS160A and the Am25LS161A feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am25LS 162A and Am25LS163A have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. The enable P or T inputs need meet only the set-up and hold time requirements with respect to the clock.

The Am54LS/74LS160A series are standard performance versions of the Am25LS160A series counters. See appropriate electrical characteristic tables for detailed Am25LS improvements.

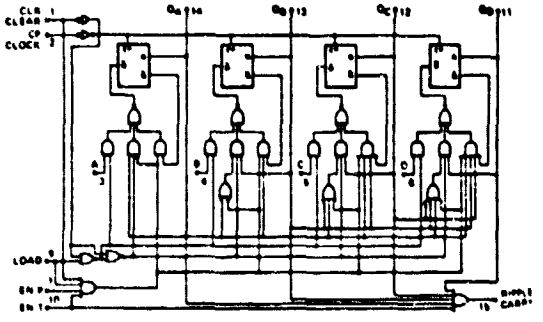
LOGIC DIAGRAMS

Am25LS160A Synchronous Decade Counter



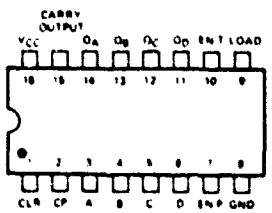
Am25LS162A synchronous decade counters are similar; however, the clear is synchronous as shown for the Am25LS163A binary counters.

Am25LS163A Synchronous Binary Counter



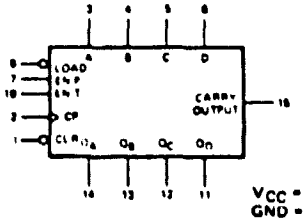
Am25LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the Am25LS160A decade counters.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orient[illegible]

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am25LS160A, 161A, 162A and 163A
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440µA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA		0.25	0.4	Volts
			I_{OL} = 8.0mA		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A, B, C, D, EN P, CP			−0.4	mA
			Load, EN T			−0.8	
			Clear '160A, '161A			−0.4	
			Clear '162A, '163A			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	A, B, C, D, EN P, CP			20	µA
			Load, EN T			40	
			Clear '160A, '161A			20	
			Clear '162A, '163A			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	A, B, C, D, EN P, CP			0.1	mA
			Load, EN T			0.2	
			Clear '160A, '161A			0.1	
			Clear '162A, '163A			0.1	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CCH}	Power Supply Current All Outputs HIGH	V_{CC} = MAX. (Note 4)			18	31	mA
I_{CCL}	Power Supply Current All Outputs LOW	V_{CC} = MAX. (Note 5)			19	32	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CCH} is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.
5. I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25LS164 • Am54LS/74LS164

8-Bit Serial-In, Parallel-Out Shift Register

DISTINCTIVE CHARACTERISTICS

- Gated serial inputs
- Asynchronous clear
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

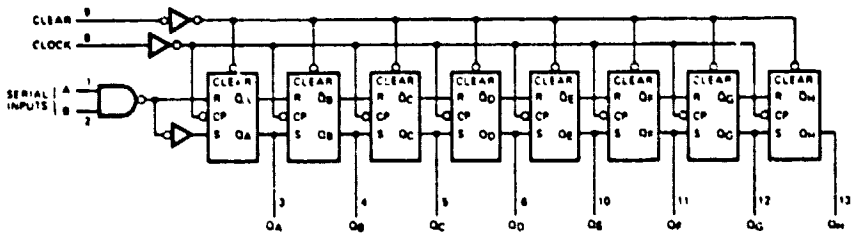
FUNCTIONAL DESCRIPTION

The Am25LS164 and Am54LS/74LS164 are eight-bit, serial in/parallel out shift registers built using advanced Low-Power Schottky processing. A gated input provides enable/disable control over incoming data such that the data can be entered or logic zeros can be entered into the register.

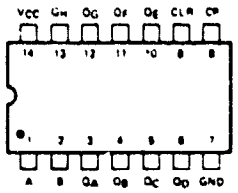
An asynchronous clear input can be used to simultaneously clear the eight flip-flops in the device. When the clear input is LOW, all internal flip-flops are forced LOW independent of the clock input. An incoming data bit is entered into the Q_A flip-flop and the data in all internal flip-flops is shifted right on the LOW-to-HIGH transition of the clock input.

The Am54LS/74LS164 is a standard performance version of the Am25LS164. See appropriate electrical characteristic tables for detailed Am25LS improvements.

LOGIC DIAGRAM

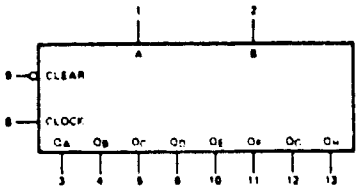


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

3

Am25LS164

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440µA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA		0.25	0.4	Volts
			I_{OL} = 8.0mA		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	Clock, Clear			−0.36	mA
			A, B			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			16	27	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V applied to the clear input.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

DEFINITION OF FUNCTIONAL TERMS

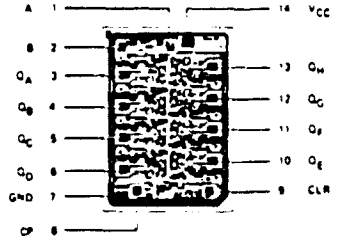
A, B The serial inputs to the device. If either the A input is LOW or the B input is LOW, the Q_A flip flop will be set LOW on the LOW-to-HIGH transition of the clock.

Clear An asynchronous master reset for the eight flip flops in the device. When the clear input is LOW, all internal flip flops are set LOW independent of the clock.

Q_A-Q_H The eight true outputs of the eight-bit register.

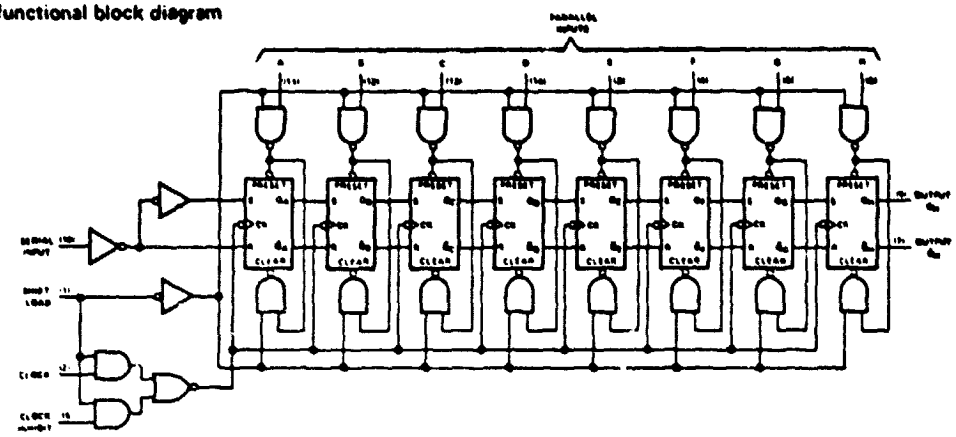
Clock The clock input to the register. Data is entered into the register on the LOW to HIGH transition of the clock input.

Metallization and Pad Layout

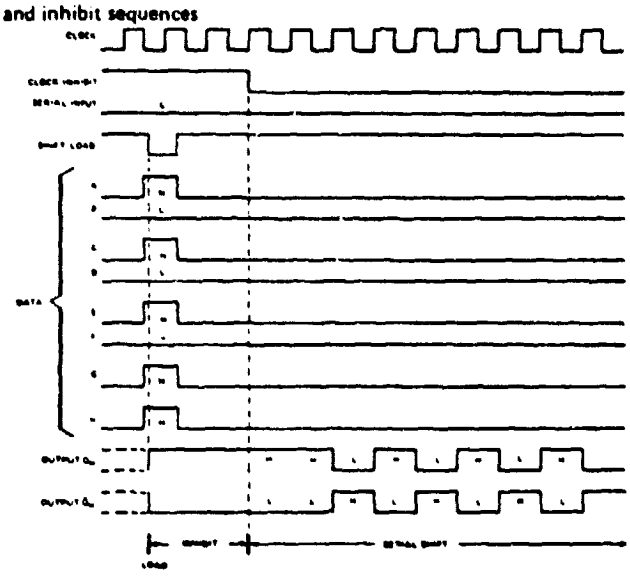


DIE SIZE 0.066" X 0.090"

functional block diagram



typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SN54165, SN74165	5.5 V
SN54LS165, SN74LS165	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5416[illegible]SN54LS165	−55°C to 125°C
SN74165, SN74LS165	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the shift/load input in conjunction with the clock-inhibit inputs.

TTL
MSI

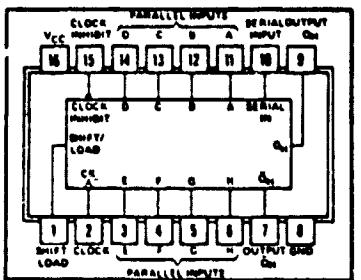
TYPES SN54165, SN54LS165, SN74165, SN74LS165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7611375, OCTOBER 1976

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165	35 MHz	105 mW

SN54165, SN54LS165 . . . J OR W PACKAGE
SN74165, SN74LS165 . . . J OR N PACKAGE
(TOP VIEW)



description

The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

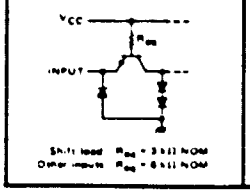
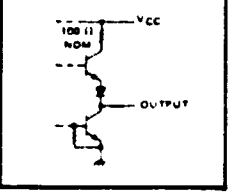
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

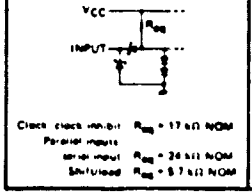
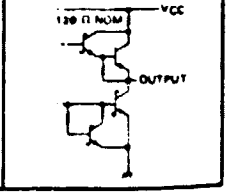
See explanation of function tables on page 3-8.

schematic of inputs and output

'165

EQUIVALENT OF EACH INPUT	TYPICAL OF BOTH OUTPUTS
	

'LS165

EQUIVALENT OF EACH INPUT	TYPICAL OF BOTH OUTPUTS
	

TTL
MSI

TYPES SN54LS280, SN54S280, SN74LS280, SN74S280
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7611829, DECEMBER 1972—REVISED OCTOBER 1976

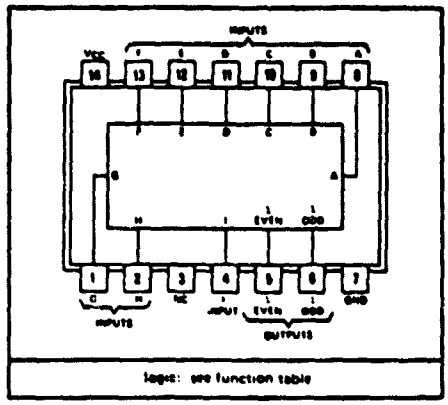
- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:
  'LS280 . . . 80 mW
  'S280 . . . 335 mW

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

SN54LS280, SN54S280 . . . J OR W PACKAGE
SN74LS280, SN74S280 . . . J OR N PACKAGE
(TOP VIEW)



NC—No internal connection

description

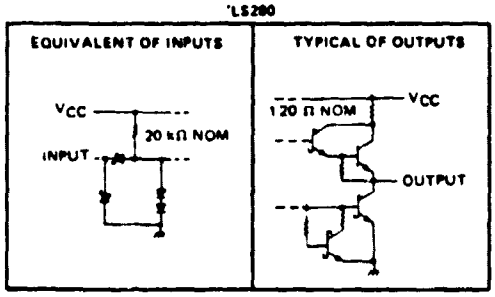
These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade-off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

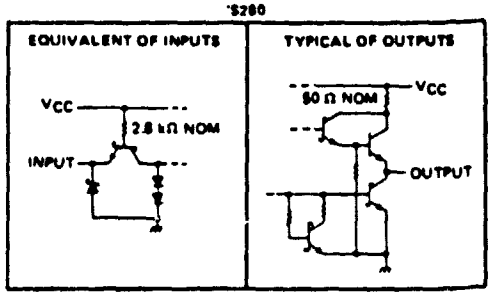
These devices are fully compatible with most other TTL and DTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

schematics of inputs and outputs

'LS280



'S280



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS280 . . . . . −55°C to 125°C
SN74LS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54LS280			SN74LS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−0.4			4	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS280			SN74LS280			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		0.25	0.4		0.25	0.4	V
							0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		16	27		16	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 2 kΩ, See Note 3		33	50	ns
t_{PHL}					29	45	
t_{PLH}	Data	Σ Odd			23	35	ns
t_{PHL}					31	50	

¶t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11

SCHOTTKY† PROM'S

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

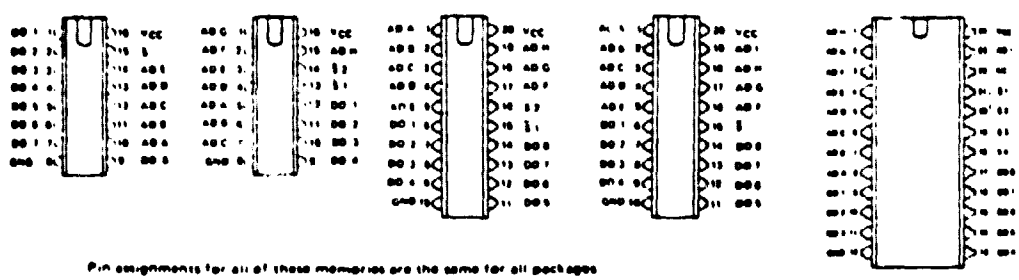
256 BITS (32 WORDS BY 8 BITS) 'S188, 'S288

1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387

2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471

4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473

4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475



Pin assignments for all of these memories are the same for all packages

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20 pin PROM's can be used to significantly improve system density for fixed memories as all are offered in a dual-in-line package having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

†Integrated Schottky-barrier diode-clamped transistor is patented by Texas Instruments, U. S. Patent Number 3,463,975.

description (continued)

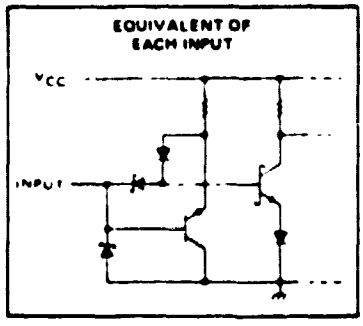
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

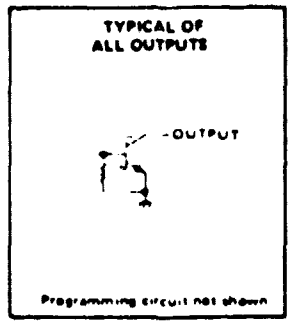
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

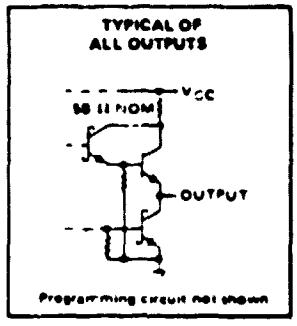
'S188, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S475



'S188, 'S387, 'S470, 'S473, 'S475



'S287, 'S288, 'S471, 'S472, 'S474



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range	SN54S' Circuits	−55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

recommended conditions for programming

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		0.9	1	10	ms
Programming duty cycle			25	35	%
Free-air temperature		0		85	°C

†Absolute maximum ratings

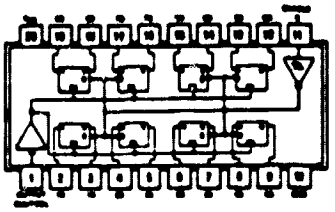
NOTES 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 0.9 ms long.

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE LATCHES

363 TRANSPARENT LATCH
3-STATE OUTPUT
COMMON OUTPUT CONTROL
COMMON ENABLE

See page 7-467

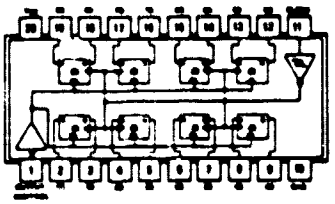


SN54LS363 (J) SN74LS363 (J, N)

OCTAL D-TYPE FLIP-FLOPS

364 COMMON CLOCK
COMMON OUTPUT CONTROL
3-STATE OUTPUTS

See page 7-467

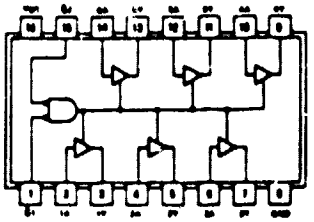


SN54LS364 (J) SN74LS364 (J, N)

HEX BUS DRIVERS

365 3-STATE OUTPUTS
NONINVERTED DATA OUTPUTS
GATED ENABLE INPUTS

See page 6-36

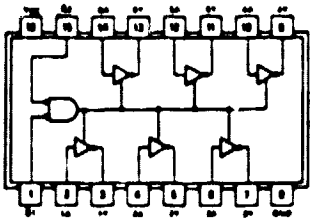


SN54365A (J, W) SN74365A (J, N)
SN54LS365 (J, W) SN74LS365 (J, N)

HEX BUS DRIVERS

366 INVERTED DATA OUTPUT
GATED ENABLE INPUTS
3-STATE OUTPUTS

See page 6-36



SN54366A (J, W) SN74366A (J, N)
SN54LS366 (J, W) SN74LS366 (J, N)

Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

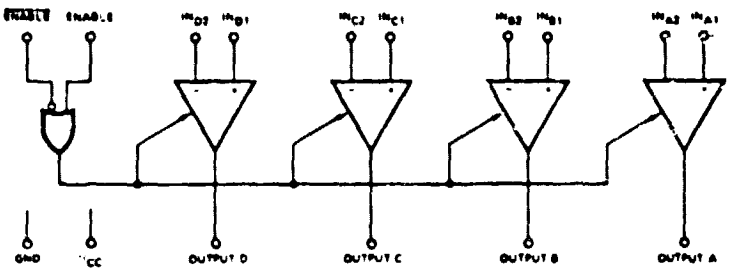
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature three-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

LOGIC DIAGRAM

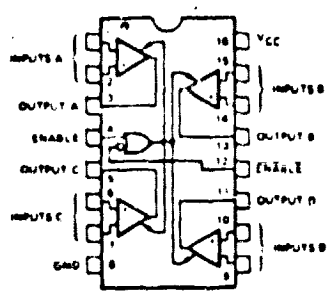


ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32 Order Number	Am26LS33 Order Number
Hermetic DIP	−55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	−55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	−55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65°C to +165°C

ELECTRICAL CHARACTERISTICS Over the operating temperature range

The following conditions apply unless otherwise specified:

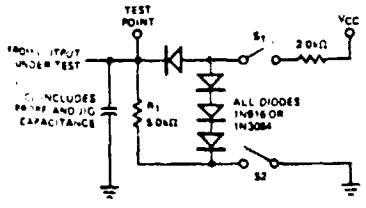
Am26LS32, Am26LS33XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

Am26LS32, Am26LS33XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

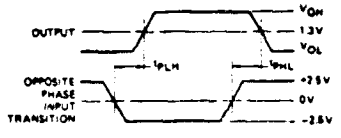
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, $-7V \leq V_{CM} \leq +7V$	0.2	0.06	0.2	Volts
			Am26LS33, $-15V \leq V_{CM} \leq +15V$	0.5	0.12	0.5	
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0k	8.5k		Ω
I_{IH}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IL}	Input Current (Under Test)	$V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $\Delta V_{IN} = +1.0V$, $\overline{ENABLE} = 0.8V$, $I_{OH} = -440\mu A$	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0V$, $\overline{ENABLE} = 0.8V$	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18mA$				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	$V_O = 2.4V$			20	mA
			$V_O = 0.4V$			−20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7V$				20	µA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max., $\Delta V_{IN} = +1.0V$		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
I_I	Input High Current	$V_{IN} = 5.5V$				100	µA
V_{HYS}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV
t_{PLH}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{PHL}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns

Note 1: All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

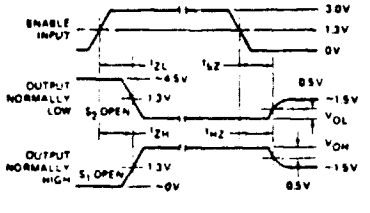
LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY (Notes 1 and 3)



ENABLE AND DISABLE TIMES (Notes 2 and 3)



Notes:

1. Diagram shown for $\overline{Enable}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses. Rate ≤ 1.0MHz, $Z_o = 50\Omega$, $t_r \leq 15ns$; $t_f \leq 6.0ns$

Am26LS31

Quad High Speed Differential Line Driver

DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0ns typical
- Input to output delay – 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when V_{CC} = 0
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 50Ω transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

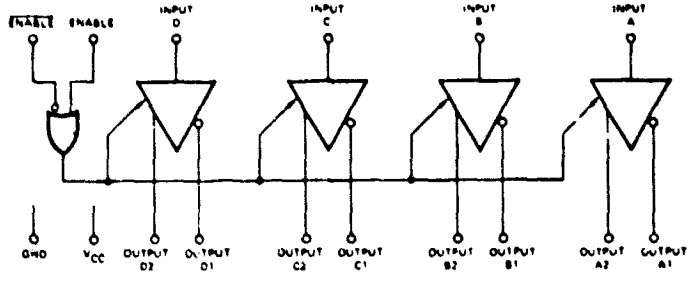
FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logically AND-ed complementary outputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

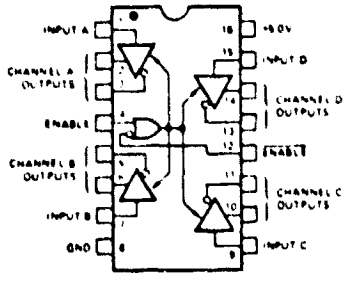
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	-55°C to +125°C	AM26LS31DM
Flat Pak	-55°C to +125°C	AM26LS31FM
Dice	-55°C to +125°C	AM26LS31XM
Hermetic DIP	0°C to +70°C	AM26LS31DC
Molded DIP	0°C to +70°C	AM26LS31PC
Dice	0°C to +70°C	AM26LS31XC

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS31 (M) T_A = −55°C to +125°C V_{CC} = 5V ± 10%

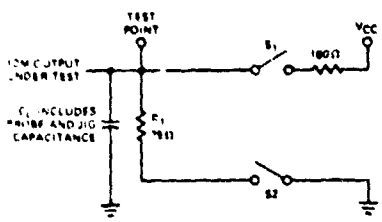
Am26LS31 (C) T_A = 0°C to +70°C V_{CC} = 5V ± 5%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −20mA		2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20mA				0.5	Volts
V_{IH}	Input HIGH Voltage	V_{CC} = Min.		2.0			Volts
V_{IL}	Input LOW Voltage	V_{CC} = Max.				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V				20	µA
I_R	Input Reverse Current	V_{CC} = Max., V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.5V			20	µA
			V_O = 0.5V			−20	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA				−1.5	Volts
I_{SC}	Output Short Circuit Current	V_{CC} = Max.		−30		−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., all outputs disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{SKEW}	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			30	40	ns

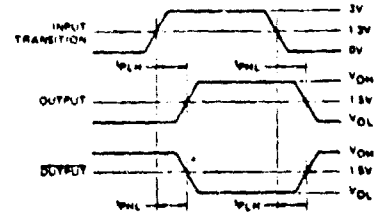
Note 1: Typical values are V_{CC} = 5.0V, T_A = 25°C

Note 2: 50pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V. See Below.

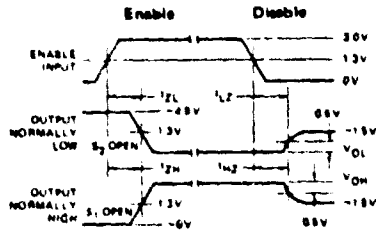
AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY
(Notes 1 and 3)



ENABLE AND DISABLE TIMES
(Notes 2 and 3)



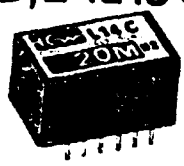
Notes: 1. Diagram shown for Enable LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

Phone: (312) 231-5270
CONNOR-WINFIELD
CORPORATION
West Chicago, Illinois 60185, U.S.A.

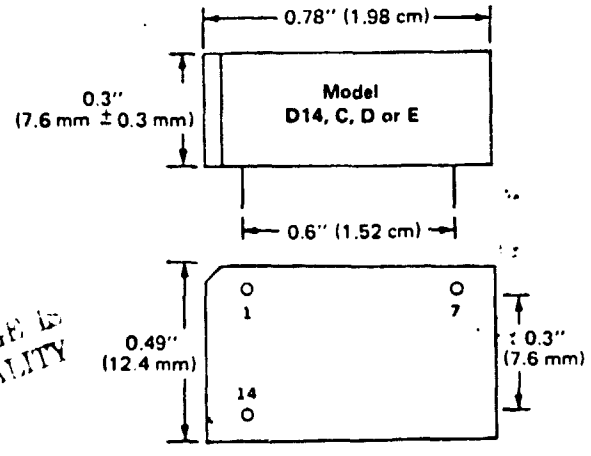
DIP CRYSTAL OSCILLATORS

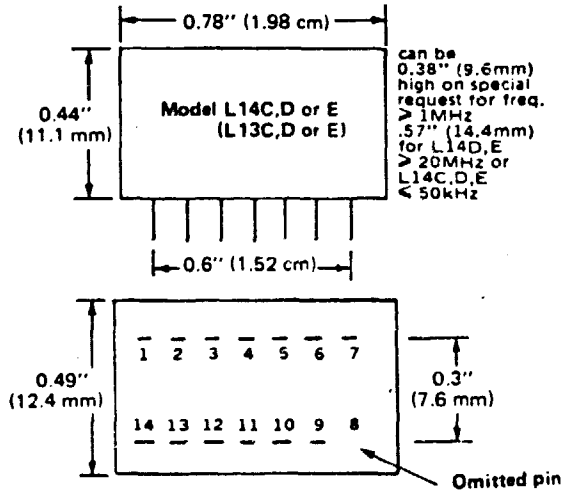
BULLETIN 76AAB4

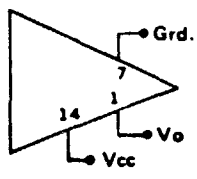
MODELS D14C, D, E L14C, D, E (L13C, D, E)

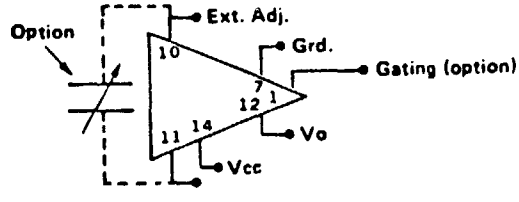


SPECIFICATIONS	MODEL D14C, D or E	MODEL L14 C, D or E (L13C, D or E)*
Fixed Frequencies Available	1MHz to 20 MHz	Model L14C (L13C): 0.1 Hz to 25 MHz L14D,E (L13D,E): 0.1 Hz to 60 MHz
Frequency Tolerance	Model D14C: ± .005%, 0° to + 50°C D14D: ± .0075%, 0°C to + 65°C D14E: ± .01%, – 25°C to + 75°C	L14C (L13C): ± .001%, 0°C to + 50°C L14D (L13D): ± .0025%, 0°C to + 65°C L14E (L13E): ± .005%, – 25°C to + 75°C External Frequency Adjust Option of ± 30 ppm Tolerances to ± .0005%, 0°C to + 50°C are available
Output Waveform Amplitude and Load	Squarewave, Logic 0 < 0.4V, Logic 1 > 2.4V into a 200 Ω to 2K Ω Load	
	Duty Cycle < 10 MHz, 49/51-51/49 Duty Cycle > 10 MHz, 30/70-70/30	Duty Cycle < 10 MHz, 59/51-51/49 Duty Cycle > 10 MHz, 30/70-70/30
Supply Voltage	5 Vdc ± 5%	
Supply Current	10 ma to 30 ma depending on frequency	10 ma to 125 ma depending on frequency
Termination	3 pin DIP to plug into single IC socket, with gold plated pins, .017" (0.43mm) diameter	*14 pin DIP to plug into single IC socket with gold plated pins L14C, D or E: Flat Pins, .016" (0.4 mm) x .023" (0.6 mm) L13C, D or E: Square Pins, .017" (0.4 mm) x .017" (0.4 mm)
Availability	2 to 6 weeks ARO, faster delivery possible with premium charge in some cases	
Price Range Special prices available for larger quantities.	Less than $50 depending on specs & quantity	Unit Price Range: $61 to $222 depending on specifications & quantity









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See other side

Please phone or write for additional information.

3. ANALOG AND DATA CONVERSION COMPONENT DATA

TRW

MONOLITHIC VIDEO A/D CONVERTER

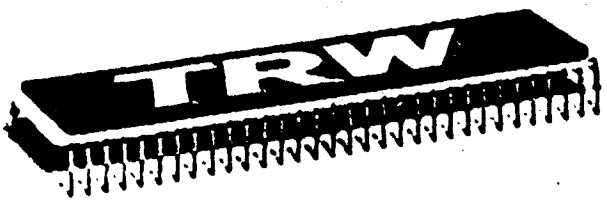
PRELIMINARY INFORMATION

MODEL : TDC1007J

The TRW TDC1007J is an 8 bit fully-parallel (flash) A/D converter capable of digitizing an analog signal at rates from dc to 30 megasamples per second (MSPS). It will accurately sample, without an external sample-and-hold circuit, input signals with frequency components up to 7 MHz (comparator 3 dB bandwidth of 40 MHz).

A single convert signal controls the unit operation, which consists of 255 strobed comparators, combining logic, and an output buffer register. Recovery from a full scale step input occurs within 20 nsec. Controls are provided for straight binary or offset 2s complement output coding, in true or inverted sense.

The TDC1007J is patented (No. 3283170), with other patents pending.

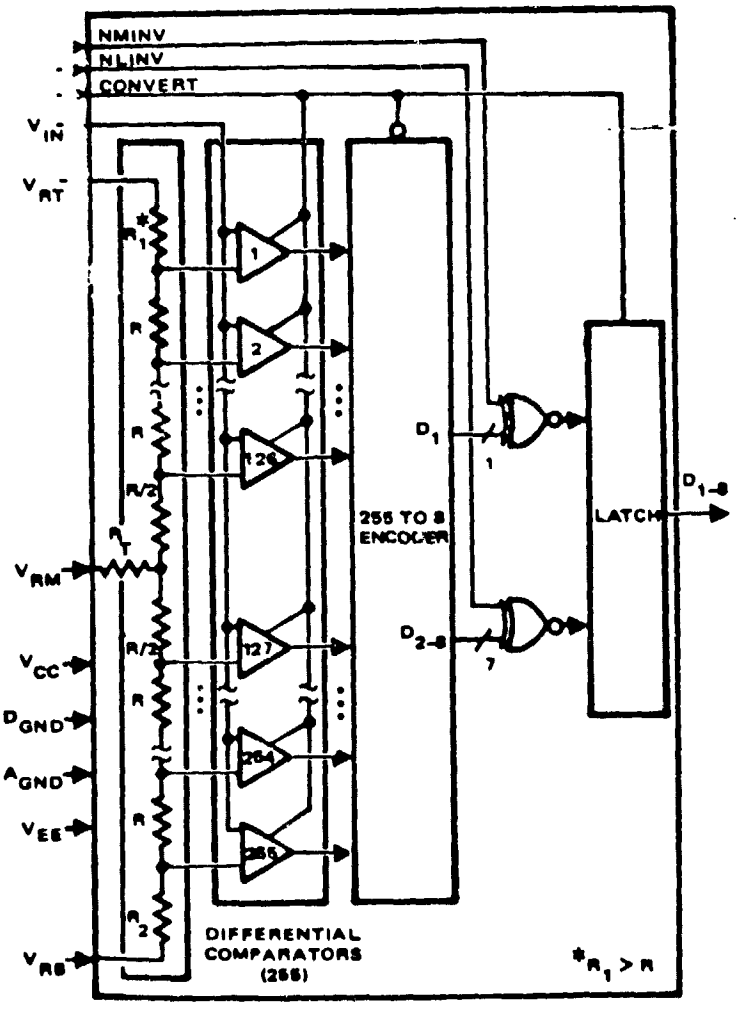


FEATURES

- 8 bit resolution
- 30 MSPS
- No sample-and-hold circuit required
- Aperture jitter 30 pS
- Differential phase 0.5°
- Differential gain 1.5%
- Binary or 2s complement output
- Monolithic, bipolar, TTL
- 64-pin ceramic DIP
- 2.0 W power dissipation

APPLICATIONS

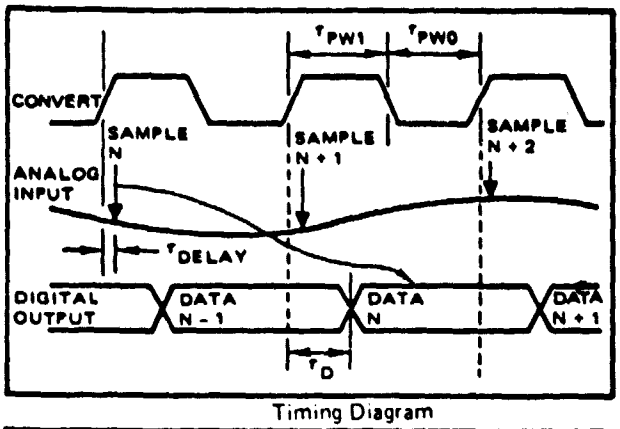
- Video data conversion
  - 3X or 4X NTSC color
  - 3X or 4X PAL color
- Radar data conversion
- High speed multiplexed data acquisition



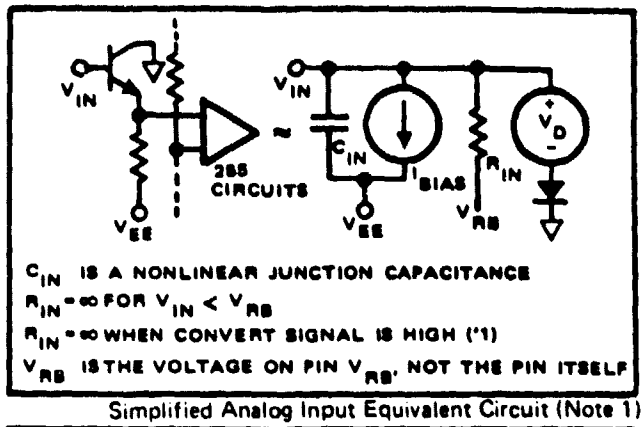
TRW LSI PRODUCTS

P.O. BOX 1125, REDONDO BEACH, CALIFORNIA 90278

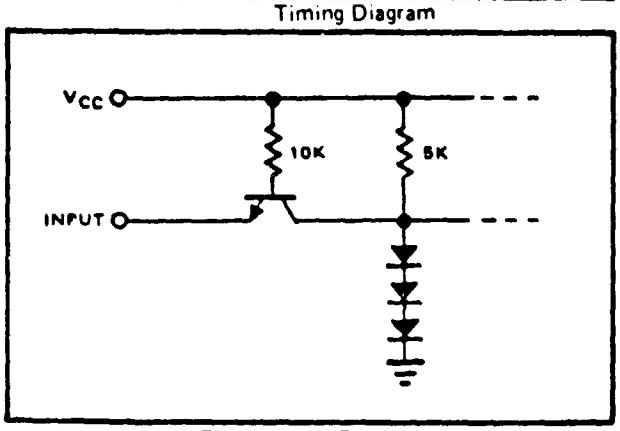
(213) 535-1831



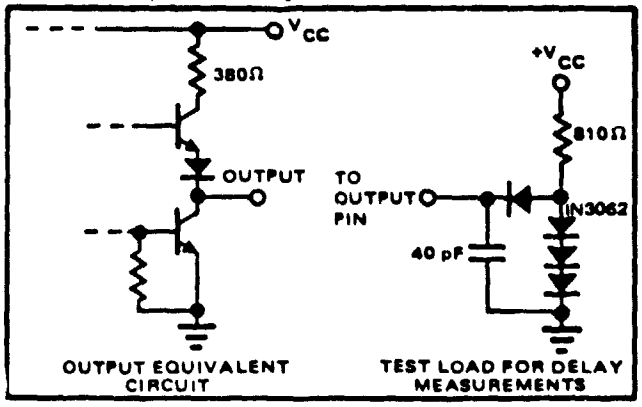
Timing Diagram



Simplified Analog Input Equivalent Circuit (Note 1)



Digital Input Equivalent Circuit



Output Circuits

performance characteristics, typical over recommended operating temperature range

PARAMETER	TEST CONDITIONS		UNIT
Resolution		8 0.39	Bits %
Dynamic Range		2.0	V
Linearity Error	0 to 20 Msp conversion rate	0.2	%
Offset Error, Top	V_{RT} = 0 V V_{RB} = -2.0 V (Note 2)	+30	mV
Bottom	V_{RT} = 0 V V_{RB} = -2.0 V (Note 2)	-24	mV
Aperture Jitter		30	pS
Differential Phase	NTSC or PAL ramp modulated with a 40 IRE color subcarrier (Note 3)	0.5	Deg
Differential Gain		1.5	%
Bandwidth, Small Signal			
3.0 dB		40	MHz
0.1 dB		7	MHz
Transient Response	Recovery from full step input	20	nsec
Signal-to-Noise Ratio	10 MHz bandwidth 25 Msps conversion rate (Note 4)		
Peak Signal/RMS Noise	1.248 MHz input 2.438 MHz input	55 54	dB dB
RMS Signal/RMS Noise	1.248 MHz input 2.438 MHz input	46 45	dB dB
Noise Power Ratio	DC to 8 MHz white noise bandwidth 40 loading 1.248 MHz slot 20 Msps conversion rate (Note 5)	36.5	dB

SPECIFICATIONS

absolute maximum ratings

Supply voltage, V_{CC} . . . . . 0.0 to +7.0 V
V_{EE} . . . . . 0.0 to -7.0 V

Input voltage, digital . . . . . -0.5 to +5.5 V
analog; signal . . . . . +0.5 V to V_{EE}
reference . . . . . +0.5 V to V_{EE}

Output voltage . . . . . -0.5 to +7.0 V

Temperature, operating, ambient . . . . . 0 to +70°C
junction . . . . . +175°C
lead, soldering (10 seconds) . . . . . +300°C
storage . . . . . -65 to +150°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}	+4.5	+5.0	+5.5	V
V_{EE}	-5.75	-6.0	-6.25	V
Reference Input, V_{RT}	-1.1	0	+0.1	V
V_{RB}	-0.9	-2.0	-2.1	V
Convert pulse width, T_{PW1}	15			nsec
T_{PW0}	25			nsec
Operating Ambient Temperature Range	0	+25	+70	°C

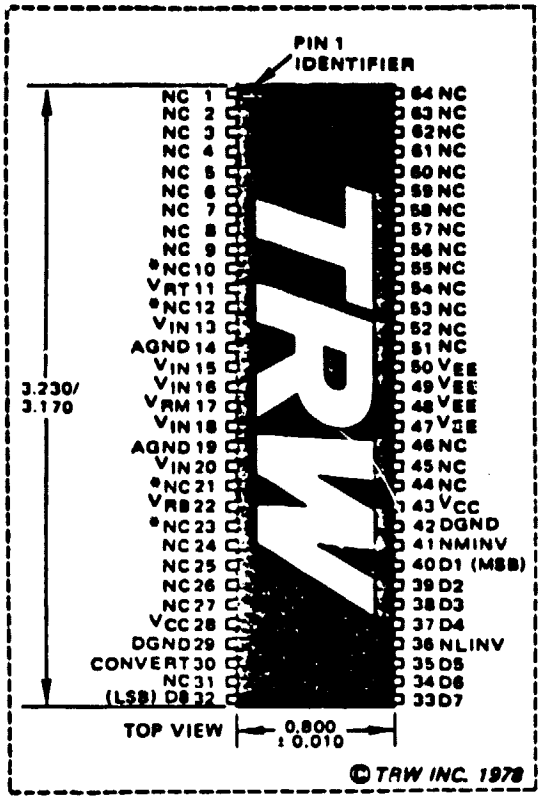
interface specifications over recommended operating temperature range

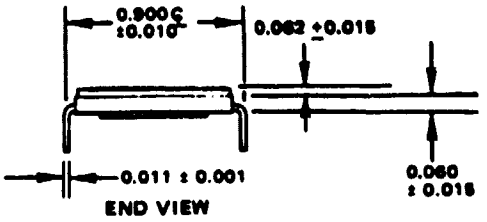
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply						
I_{CC}	Supply Current	V_{CC} = MAX			35	mA
I_{EE}	Supply Current	V_{EE} = MAX			-400	mA
Analog						
Signal Input:						
V_{IN}	Input Voltage Range		0		-2.0	V
R_{IN}	Equivalent Input Impedance	V_{EE} = MAX	5		∞	K
C_{IN}	Input Capacitance				300	pF
I_{BIAS}	Constant Input Bias	V_{EE} = MAX			500	μA
I_B	Clock Synchronous Bias	V_{EE} = MAX			200	μA
Reference Input						
I_{RT}	Reference Current, Top	V_{EE} = MAX V_{RT} = 0.0 V V_{RB} = -2.0 V			+30	mA
I_{RB}	Reference Current, Bottom	V_{EE} = MAX V_{RT} = 0.0 V V_{RB} = -2.0 V			-30	mA
R	Reference Resistor		0.26	0.31		Ω
R_T	Trim Resistor			15		KΩ
Digital						
Inputs:						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current				7.5	μA
I_{IL}	Low Level Input Current				-1.0	mA
Outputs						
V_{OH}	High Level Output Voltage	V_{CC} = NOM I_{OH} = -0.4 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = NOM I_{OL} = 4.0 mA			0.4	V

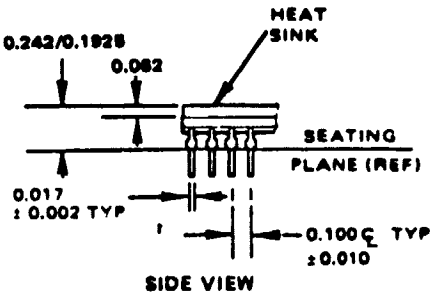
switching characteristics over recommended operating temperature range, V_{CC} = 5.0, V_{EE} = -6.0 V

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_s	Maximum Conversion Rate		20	30		MHz
T_{DELAY}	Aperture Delay			10		nsec
T_D	Digital Output Delay		15	30	45	nsec

PACKAGE INFORMATION







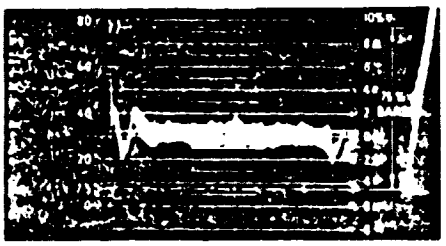
NOTES:

- DIMENSIONS IN INCHES
- ALL POWER AND GROUND PINS MUST BE CONNECTED
- DGND IS +5V GROUND AND REFERENCES TTL I/O BUFFERS ONLY
- ALL V_{IN} PINS MUST BE EXTERNALLY CONNECTED

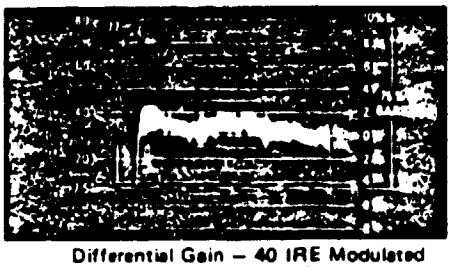
*RECOMMENDED CONNECTION TO ANALOG GROUND FOR INTERELECTRODE SHIELDING

MATING CONNECTORS INCLUDE:

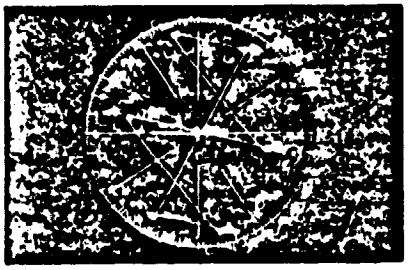
Cambion	703-4064-01-04-12	Low-Profile, Solder Tail, Tin Plate, Jam Socket
Robinson-Nugent	ICN-649-55-G	Low-Profile, Solder Tail, Gold Plate, Jam Socket
Textool	232-2601-00-0605 (2 required)	Solder Tail, Nickel Plate, Zero Insertion Force Socket



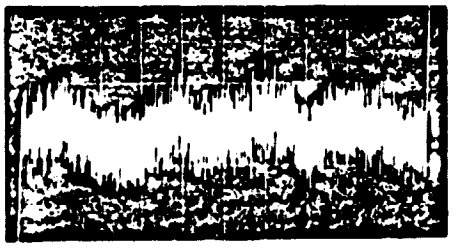
Differential Phase – 40 IRE Modulated NTSC Ramp – 14.3 MSPS Unlocked (Note 3)



Differential Gain – 40 IRE Modulated NTSC Ramp – 14.3 MSPS Unlocked (Note 3)



Vector Diagram – NTSC Color Bars 14.3 MSPS Unlocked (Note 3)



Linearity – 20 MSPS (Note 6)

OUTPUT CODING

	Range		Binary		Offset 2s Complement	
			True	Inverted	True	Inverted
	-2.0000V FS	-2.0480V FS	NMINV = 1	0	0	1
STEP	7.8431 mV STEP	8.000 mV STEP	NLINV = 1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	0.9961V	-1.0160V	01111111	10000000	11111111	00000000
128	-1.0039V	-1.0240V	10000000	01111111	00000000	11111111
129	-1.0118V	-1.0320V	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
255	-2.0000V	-2.0400V	11111111	00000000	01111111	10000000

NMINV and NLINV are to be considered D.C. controls. They may be tied to +5V for a logical '1' and tied to ground for a logical '0'.

NOTES

1. Analog Input. The analog input circuit of Figure 2 is a simplification that is adequate for most interface circuit designs. As shown, the input consists of 255 parallel emitter-follower stages driving voltage comparators. C_{IN} represents the nonlinear emitter-follower junction capacitance, and I_{BIAS} is the constant input bias current. R_{IN} is a linear resistive model of the change in input current due to comparator switching as the input moves through the range. This component does not vary after the input range is exceeded, as no additional comparators can be switched, but do note that the comparator current is zero ($R = \infty$) while the convert signal is high ('1'). The diode voltage in the model represents the base-collector junctions of the emitter-follower transistors, which can conduct if the input exceeds +0.7 V.

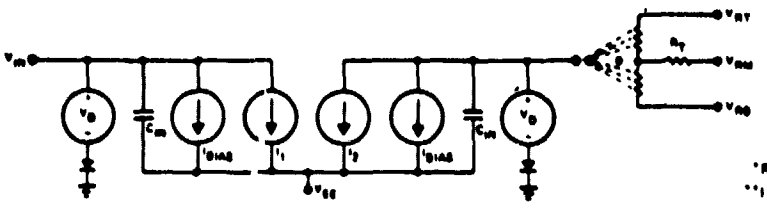
   The 300 pF maximum input capacitance presents a drive requirement similar to that of a 75 ohm coaxial cable, though its nonlinear nature and dc bias characteristics make it unsuited to being driven directly by a 75 ohm line: a source impedance of less than 10 ohms is indicated for optimal performance. One method of providing this drive is demonstrated on the TDC1007PCB (page 9). This is not necessarily the best or most cost effective technique, but it performs well. The LH0033, or equivalent, buffer amplifier also works, and common analog line driver circuits can be adapted to the task. Through the use of NMINV and NLINV, either inverting or noninverting buffers may be accommodated.

2. Reference Inputs. The resistive divider that provides a reference voltage to each of the 255 comparator circuits has both ends and a midpoint tap available to the user, allowing considerable flexibility in the circuit operation. The nominal operating range is 0 to -2 V, requiring approximately 0 V on V_{RT} and -2 V on V_{RB}. This is not to preclude operation over a smaller range, as the circuit will function with a total range of less than 1 volt; but some performance characteristics will change. For example, a quantizer circuit has two major sources of dc linearity error: resistor ladder variations and comparator offset voltages. The former is scaled by a range reduction while the latter is not. The circuit should be operated with V_{RT} and V_{RB} within the recommended +0.1 to -2.1 V range, and V_{RB} at least 800 mV more negative than V_{RT}.

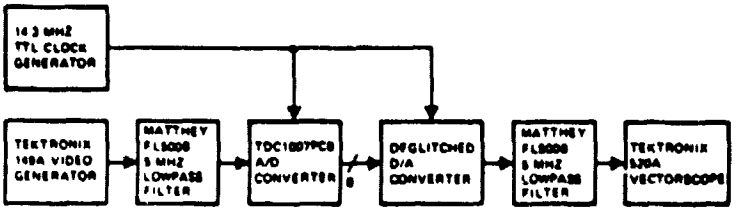
   When one of the 255 comparators turns off due to a drop in analog input voltage, its bias current shifts from the analog input to the reference ladder. When the convert signal is high, comparator bias current is zero. This generates clock and signal related current noise on the reference inputs with a maximum amplitude of I_B, which can be relieved by ensuring adequate bypassing of V_{RT} and V_{RB} to analog ground. If the reference inputs are exercised dynamically, as in an AGC circuit, a bypass capacitor would be inappropriate and a low impedance reference source should be employed. The input-reference circuit is modeled on page 6.

   Calibration is accomplished by adjusting V_{RT} and V_{RB} to set the first and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring that calibration can be achieved with a positive voltage on V_{RT}. Assuming a 0 to -2 V desired range, continuously strobe the converter with -0.0039 V on the analog input, and adjust V_{RT} for output toggling between codes 000 and 001. Then apply -1.9961 V and adjust V_{RB} for toggling between codes 254 and 255. Rather than adjusting V_{RT}, it may be convenient to connect it to analog ground and calibrate the 0 V end of the range with a buffer offset control. V_{RB} is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed on the TDC1007PCB (page 7).

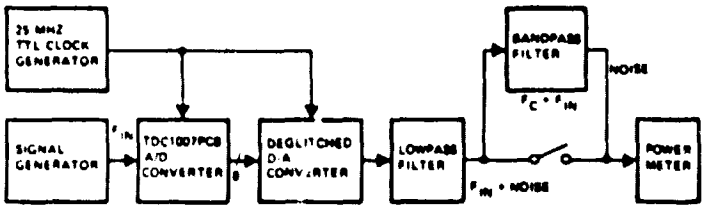
   A midpoint tap, V_{RM}, allows the user to parallel the upper or lower half of the ladder with a trim resistor, R_T. This produces approximately 1/2 LSB adjustment of the linearity midpoint and is included for linearity compensation of an extended temperature version of this part. It is not necessary that adjustment be performed over the commercial temperature range (0 to 70°C). This pin can also be useful as a virtual ground reference for the input buffer amplifier if bipolar conversions are performed. Be aware of the inherent R_T impedance of this node; any load applied to V_{RM} will affect linearity.



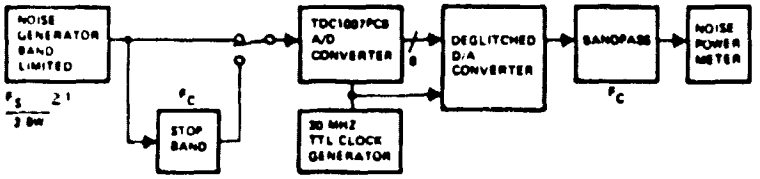
3. NTSC Video Testing. Measurement of video test signals is performed using the setup illustrated. The A/D and D/A converters are strobed at 14.3 MHz, unlocked from the color subcarrier, and the full composite signal encoded. No sin(x)/x correction is performed. Differential phase and gain, in excess of that inherent in 8 bit quantization, are determined by measuring the deviation of the centerline of the trace on a vectorscope monitoring a reconstructed 40 IRE modulated ramp, sampled asynchronously with the color subcarrier. The small "glitches" in the differential gain photograph are due to color bar feedthrough within the test signal generator.



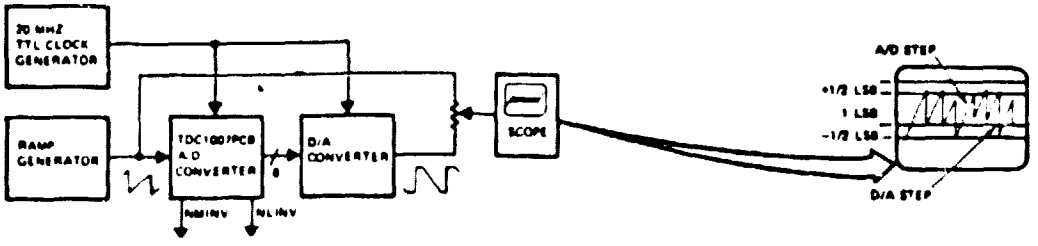
4. Signal-to-Noise Ratio (SNR) Test. A block diagram of the SNR test setup is shown below. The analog input to the A/D converter is a single tone with a p-p amplitude equal to the full scale range of the A/D. Power in the reconstructed waveform is measured over a selected bandwidth ($\leq f_s/2$) and remeasured when the fundamental tone frequency is filtered out at the D/A output. The ratio of the two power readings is the SNR. An ideal A/D converter has a SNR equal to 6n+1.8 dB, where n = number of bits, n>4. This is the RMS signal-to-RMS noise value. Peak signal-to-RMS noise theory is approximately 9 dB higher.



5. Noise Power Ratio Test. A block diagram of the NPR test setup is given below. Bandlimited gaussian noise is the analog input to the A/D converter. Power in the reconstructed waveform is measured in a selected frequency slot and then remeasured with the same frequency slot notched out of the input signal spectrum. The ratio of the two power readings reflects the noise performance, dynamic nonlinearity of the A/D, and aperture effects. The theoretical NPR for the test performed is 40.5 dB.



6. Linearity Testing. Device linearity is readily determined with the test setup below. The A/D output is inverted using the NMINV and NLINV controls. The input is slightly overdriven with a slow ramp, the output and input are summed, and the results displayed on an oscilloscope.



Operational Amplifiers

LH0032/LH0032C ultra fast FET operational amplifier

general description

The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

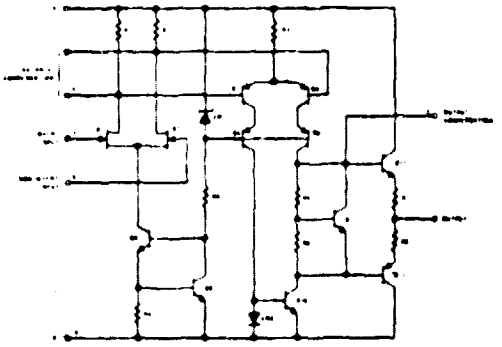
features

- High slew rate — 500 V/μs
- High bandwidth — 70 MHz
- High input impedance — $10^{12}\Omega$
- Low input bias current — 20 pA max
- Offset null with single pot
- Low input offset voltage — 2 mV max
- No compensation for gains above 50

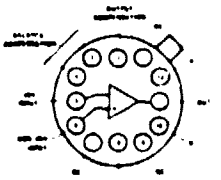
The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range −55°C to +125°C and the LH0032C is guaranteed from −25°C to +85°C.

For information on other National operational amplifiers, see listing on last page.

schematic and connection diagrams



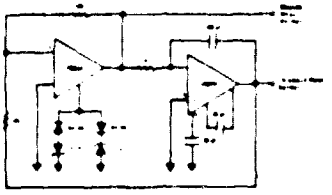
Metal Can Package



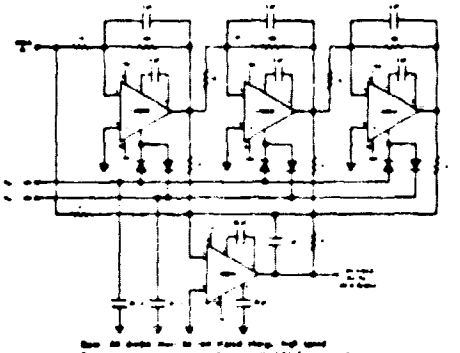
Order Number LH0032G or LH0032CG
See Package 6

typical applications

1 MHz Function Generator



DC to Video Log Amplifier



absolute maximum ratings

Supply Voltage		±18V
Input Voltage		$\pm V_S$
Differential Input Voltage		±30V
Power Dissipation		See curve
Operating Temperature Range	LH0032	-55°C to +125°C
	LH0032C	-25°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LH0032			LH0032C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_S = ±15V $R_S \leq 100k$ T_A = 25°C		2	5		5	15	mV
	V_S = ±15V $R_S \leq 100k$			10			20	mV
Average Offset Voltage Drift	$R_S \leq 100k$		25			25		µV/°C
Input Bias Current	T_A = 25°C		10	100		25	200	pA
				50			150	nA
Input Offset Current	T_A = 25°C		5	25		10	50	nA
				25			5	nA
Large Signal Voltage Gain	V_S = ±15V V_{OUT} = ±10V f = 1 kHz R_L = 1 kΩ T_A = 25°C	60	70		60	70		dB
	V_S = ±15V V_{OUT} = ±10V f = 1 kHz R_L = 1 kΩ	57			57			dB
Input Voltage Range	V_S = ±15V	±10	±12		±10	±12		V
Output Voltage Swing	V_S = ±15V R_L = 1 kΩ	±10	±13.5		±10	±13		V
Power Supply Rejection Ratio	V_S = ±15V ΔV_S = ±10V	80	80		80	80		dB
Common Mode Rejection Ratio	V_S = ±15V ΔV_{IN} = 10V	80	80		80	80		dB
Supply Current	V_S = ±15V T_A = 25°C		18	20		20	22	mA

ac electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	A_V = +1, ΔV_{IN} = 20V	350	500		V/µs
Settling Time to 1% of Final Value	A_V = -1, ΔV_{IN} = 20V		100		ns
Settling Time to 0.1% of Final Value	A_V = -1, ΔV_{IN} = 20V		300		ns
Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V		8	20	ns
Small Signal Delay Time	A_V = +1, ΔV_{IN} = 1V		10	25	ns

Note 1 These specifications apply for ±5V ≤ V_S ≤ ±18V and -55°C to +125°C for the LH0032 and -25°C to +85°C for the LH0032C

Note 2 These specifications apply for V_S = ±15V, R_L = 1 kΩ and T_A = 25°C

REF-01

+10V PRECISION VOLTAGE REFERENCE

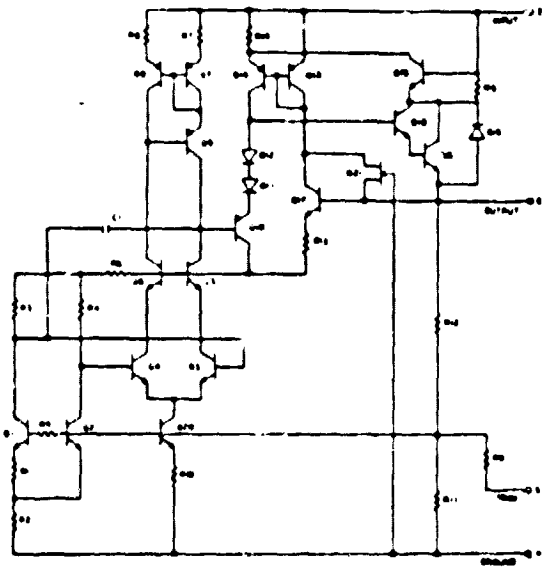
GENERAL DESCRIPTION

The REF-01 Precision Voltage Reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 12 to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-01 an excellent choice whenever a stable voltage reference is required, such as in D/A and A/D converters, in portable instruments, and in digital voltmeters. Full military temperature range devices with screening to MIL-STD 883A are available.

FEATURES

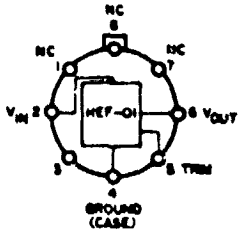
- Adjustable 10 Volt Output . . . . . ±3%
- Excellent Temperature Stability . . . . . 3 ppm/°C
- Low Noise 20μVp-p
- Low Power 15mW
- Wide Input Voltage Range . . . . . 12 to 40V
- High Load Driving Capability . . . . . ±20mA
- No External Components
- Short Circuit Proof
- MIL-STD-883A Screening Available

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J Suffix)

ORDER REF-01AJ
REF-01J
REF-01EJ
REF-01HJ
REF-01CJ
REF-01DJ

Military Temperature Range Devices
with MIL-STD-883A Class B Processing

ORDER REF01-883 AJ
REF01-883 J

ABSOLUTE MAXIMUM RATINGS

Input Voltage REF-01, A, E, H	40 V	Operating Temperature Range	
REF-01C, D	30 V	REF-01A, REF-01	-55°C to +125°C
Power Dissipation (see note)	500mW	REF-01E, REF-01H, REF-01D REF-01C,	0°C to +70°C
Output Short Circuit Duration (to ground or V_{IN})	Indefinite		
Storage Temperature Range	-65°C to +150°C	Note: Derate at 7.1mW/°C above 80°C ambient temperature.	
Lead Temperature (Soldering, 60 sec)	300°C		

ELECTRICAL CHARACTERISTICS

			REF-01A			REF-01			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	–	±3.0	±3.3	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	–	20	30	–	20	30	μVp-p
Input Voltage Range	V_{IN}		12	–	40	12	–	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	–	0.005	0.008	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	μsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		-0.3	-0.5	–	-0.3	-0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
The following specifications apply for V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise noted									
Output Voltage Change with Temperature (Notes 1 and 2)	ΔV_{OT}	0° ≤ T_A ≤ +70°C	–	0.02	0.06	–	0.07	0.17	%
		-55° ≤ T_A ≤ +125°C	–	0.06	0.15	–	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/°C/%
Line Regulation (V_{IN} = 13 to 33V) (Note 4)		0° ≤ T_A ≤ +70°C	–	0.007	0.012	–	0.007	0.012	%/V
		-55° ≤ T_A ≤ +125°C	–	0.009	0.015	–	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0° ≤ T_A ≤ +70°C	–	0.006	0.010	–	0.007	0.012	%/mA
		-55° ≤ T_A ≤ +125°C	–	0.007	0.012	–	0.009	0.015	%/mA

NOTE 1 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2 ΔV_{OT} specification applies trimmed to 10.000V or untrimmed

NOTE 3 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O(0°\text{to}+70°C) = \frac{\Delta V_{OT}\ 0°\text{to}+70°C}{70°C}$

and $TCV_O(-55°\text{to}+125°C) = \frac{\Delta V_{OT}\ -55\text{to}+125°C}{180°C}$

NOTE 4 Line and Load Regulation specifications include the effects of self heating

NOTE 5 Parameters not 100% tested; 90% of units meet this specification

Am124/224/324
Am124A/224A/324A

Quad Op Amps

Distinctive Characteristics

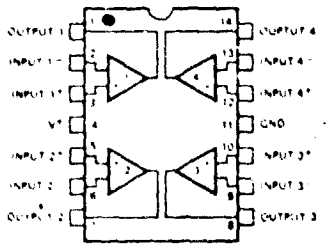
- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated
- Internally frequency compensated for unity gain
- Large dc voltage gain – 100dB
- Wide bandwidth (unity gain) – 1MHz (temperature compensated)
- Wide power supply range:
  Single supply – 3V to 30V
  Dual supplies – ±1.5V to ±15V
- Very low supply current drain (800μA) – essentially independent of supply voltage (1mW/op amp at +5V)
- Low input biasing current – 45nA (temperature compensated)
- Low input offset voltage – 2mV and offset current – 5nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing – 0V to V+ –1.5V

FUNCTIONAL DESCRIPTION

The Am124 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed primarily to operate from a single power supply over a wide range of voltages. These devices can also operate from split power supplies and the low power supply current drain is independent of the magnitude of the power supply voltage.

Functional applications consist of all the conventional op amp circuits which can now be more easily implemented in single power supply systems along with transducer amplifiers and dc gain blocks.

CONNECTION DIAGRAM
Top View

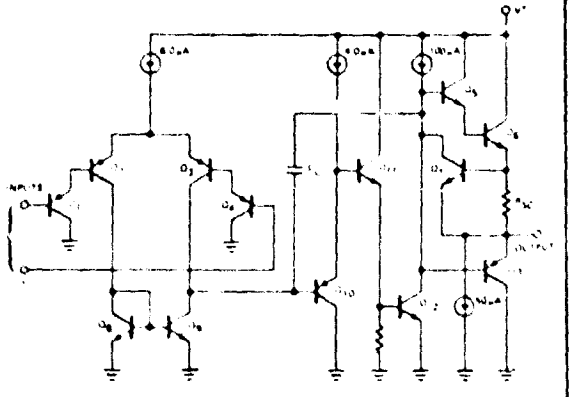


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
	Hermetic DIP	0°C to +70°C	LM224D
Am324	Molded DIP	0°C to +70°C	LM324N
	Dice	0°C to +70°C	LD324
Am224	Hermetic DIP	25°C to +85°C	LM224D
	Hermetic DIP	55°C to +125°C	LM124D
Am124	Flat Pack	55°C to +125°C	LM124F
	Dice	55°C to +125°C	LM124
	Hermetic DIP	0°C to +70°C	LM324AD
Am324A	Molded DIP	0°C to +70°C	LM324AN
	Dice	0°C to +70°C	LM324A
Am224A	Hermetic DIP	25°C to +85°C	LM224AD
	Hermetic DIP	55°C to +125°C	LM124AD
Am124A	Flat Pack	55°C to +125°C	LM124AF
	Dice	55°C to +125°C	LD124A

SCHEMATIC DIAGRAM (Each Amplifier)



ELECTRICAL CHARACTERISTICS ($V^+ = +5.0 V_{DC}$, Note 4)

Parameter	Conditions	Am124A			Am224A			Am324A			Am124/Am224			Am324			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$T_A = 25°C$ (Note 8)		1.0	2.0		1.0	3.0		2.0	3.0		±2.0	±5.0		±2.0	±7.0	mV$_{DC}$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	200	nA$_{DC}$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2.0	10		2.0	15		5.0	30		±3.0	±30		±5.0	±50	nA$_{DC}$
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30 V_{DC}$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V$_{DC}$
Supply Current	$R_L = \infty$, $V_{CC} = 30V$		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0	mA$_{DC}$
	$R_L = \infty$		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15 V_{DC}$ (For large V_O swing), $R_L \geq 2.0k\Omega$, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100		V/mV
Output Voltage Swing	$R_L = 2.0k\Omega$, $T_A = 25°C$										0		$V^+-1.5$	0		$V^+-1.5$	V$_{DC}$
Common Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		dB
Amplifier to Amplifier Coupling (Note 8)	f = 1.0kHz to 20kHz, $T_A = 25°C$ (Input referred)		-120			-120			-120			-120			-120		dB
Output Current	Source: $V_{IN}^+ = 1.0 V_{DC}$, $V_{IN}^- = 0 V_{DC}$, $V^+ = 15 V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA$_{DC}$
	Sink: $V_{IN}^- = 1.0 V_{DC}$, $V_{IN}^+ = 0 V_{DC}$, $V^+ = 15 V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		
	Sink: $V_{IN}^- = 1.0 V_{DC}$, $V_{IN}^+ = 0 V_{DC}$, $T_A = 25°C$, $V_O = 200 mV_{DC}$	12	50		12	50		12	50		12	50		12	50		μA$_{DC}$
Short Circuit to Ground	$T_A = 25°C$ (Note 2)		40	60		40	60		40	60		40	60		40	60	mA$_{DC}$
Input Offset Voltage	Note 5			4.0			4.0			5.0			±7.0			±9.0	mV$_{DC}$
Input Offset Voltage Drift	$R_S = 0\Omega$		7.0	20		7.0	20		7.0	30		7.0			7.0		μV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150	nA$_{DC}$
Input Offset Current Drift			10	200		10	200		10	300		10			10		pA$_{DC}$/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500	nA$_{DC}$
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30 V_{DC}$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V$_{DC}$
Large Signal Voltage Gain	$V^+ = +15 V_{DC}$ (For large V_O swing), $R_L \geq 2.0k\Omega$	25			25			15			25			15			V/mV
Output Voltage Swing	$V^+ = +30 V_{DC}$, $R_L = 2.0k\Omega$	26			26			26			26			26			V$_{DC}$
	V_{OH}: $R_L = 10k\Omega$	27	28		27	28		27	28		27	28		27	28		
	V_{OL}: $V^+ = 5.0 V_{DC}$, $R_L = 10k\Omega$		5.0	20		5.0	20		5.0	20		5.0	20		5.0	20	mV$_{DC}$
Output Current	Source: $V_{IN}^+ = 1.0 V_{DC}$, $V_{IN}^- = 0 V_{DC}$, $V^+ = 15 V_{DC}$	10	20		10	20		10	20		10	20		10	20		mA
	Sink: $V_{IN}^- = 1.0 V_{DC}$, $V_{IN}^+ = 0 V_{DC}$, $V^+ = 15 V_{DC}$	10	15		50	80		50	80		50	80		50	80		
Positive Supply Voltage	Note 7			V^+			V^+			V^+			V^+			V^+	V$_{DC}$

Notes:

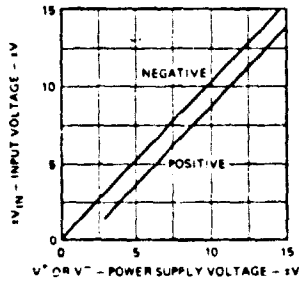
1. For operating at high temperatures, the Am324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The Am224 and Am124 can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers — use external resistors, where possible to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.
4. These specifications apply for $V^+ = +8V_{DC}$ and $-85°C \leq T_A \leq +125°C$, unless otherwise stated. With the Am224, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the Am324 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
5. $V_O = 1.4V$, $R_S = 0\Omega$, with V^+ from 5V to 30V, and over the full input common mode range (0V to $V^+ - 1.5V$).
6. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
7. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32V without damage.
8. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

MAXIMUM RATINGS (Above which the useful life may be impaired)

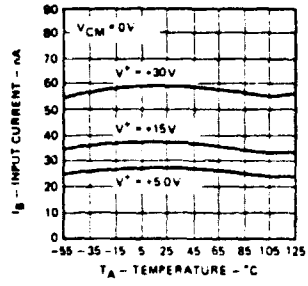
Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (Note 1)	
Molded DIP	570mW
Cavity DIP	900mW
Flat Pak (Am124F)	800mW
Output Short Circuit to GND (Note 2)	
(One Amplifier) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous
Input Current ($V_{IN} < -0.3V_{OL}$) (Note 3)	50mA
Operating Temperature Range	
Am324/Am324A	0°C to +70°C
Am224/Am224A	−25°C to +85°C
Am124/Am124A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL PERFORMANCE CURVES

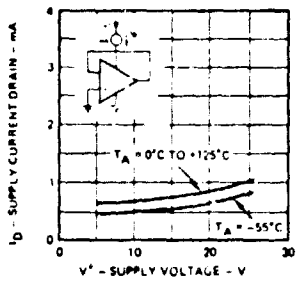
Input Voltage Range



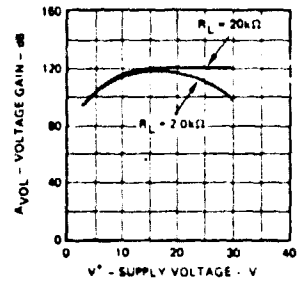
Input Current



Supply Current

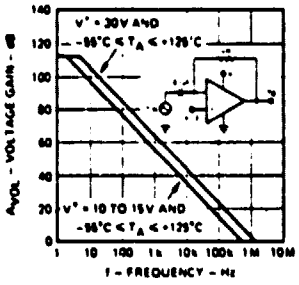


Voltage Gain

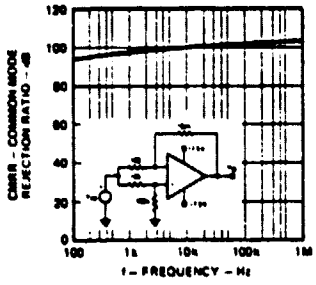


TYPICAL PERFORMANCE CURVES (Cont.)

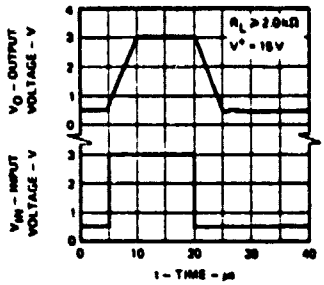
Open Loop Frequency Response



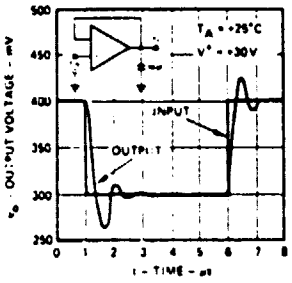
Common-Mode Rejection Ratio



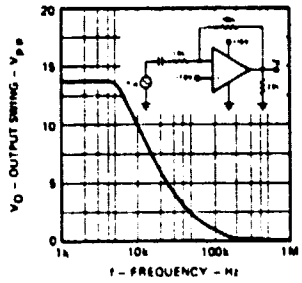
Voltage Follower Pulse Response



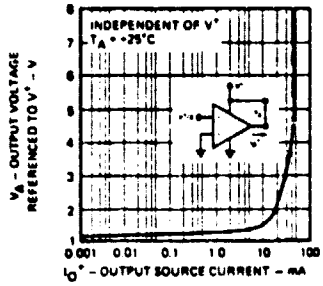
Voltage Follower Pulse Response (Small Signal)



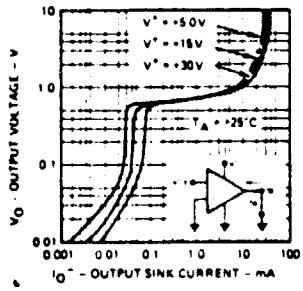
Large Signal Frequency Response



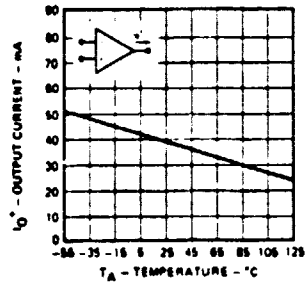
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



absolute maximum ratings

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	900 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current (V_{IN} < −0.3 V_{DC}), (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM339A	0°C to +70°C	−40°C to +85°C
LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

electrical characteristics (V^+ = 5 V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C, (Note 5)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±30	mV$_{DC}$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	100		25	250		25	100		70	250		25	250		25	500	nA$_{DC}$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±3.0	±25		±5.0	±100		±3.0	±25		±5.0	±100		±5	±100		±3	±100	nA$_{DC}$
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V$_{DC}$
Supply Current	R_L = ∞ on all Comparators, T_A = 25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2	mA$_{DC}$
	R_L = ∞ V^+ = 30V, T_A = 25°C														1	2.5				mA$_{DC}$
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC} (To Support Large V_O Swing), T_A = 25°C	50	200		50	200			200			200		25	100		2	20		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		300			300			300			300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, V_O ≤ 1.5 V_{DC}, T_A = 25°C	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA$_{DC}$
Saturation Voltage	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400		250	400		250	400		250	400			600		250	500	mV$_{DC}$
Output Leakage Current	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, V_O = 5 V_{DC}, T_A = 25°C		0.1			0.1			0.1			0.1			0.1			0.1		nA$_{DC}$

electrical characteristics (con't)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4.0			4.0			9.0			9.0		0	15			40	mV$_{DC}$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150			±150			±150			±150		50	200			300	nA$_{DC}$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		300	500			1000	nA$_{DC}$
Input Common-Mode Voltage Range		0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V$_{DC}$
Saturation Voltage	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA			700			700			700			700		400	700			700	mV$_{DC}$
Output Leakage Current	$V_{IN(+)}$ ≥ 1 V_{DC}, $V_{IN(-)}$ = 0, V_O = 30 V_{DC}			1.0			1.0			1.0			1.0			1.0			1.0	µA$_{DC}$
Differential Input Voltage	Keep all V_{IN} ≥ 0 V_{DC} (or V^-, if used), (Note 8)			V^+			V^+			36			36	0		V^+			V_{CC}	V$_{DC}$

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristics of the outputs keeps the chip dissipation very small (P_D ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is a lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a voltage greater than −0.3 V_{DC}.

Note 4: These specifications apply for V^+ = 5 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM339/LM339A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2901, LM3302 temperature range is −40°C ≤ T_A ≤ +85°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to +30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).

Note 9: At output switch point, V_O ≅ 1.4 V_{DC}, R_S = 0Ω with V^+ from 5 V_{DC} and over the full input common-mode range (0 V_{DC} to V^+ − 1.5 V_{DC}).

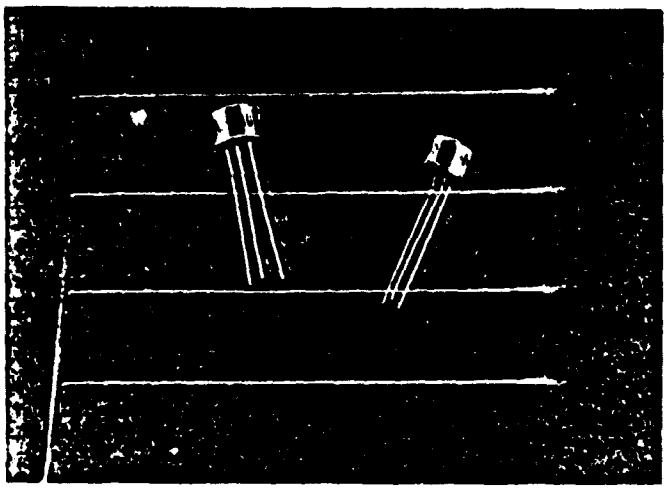
Note 10: For input signals that exceed V_{CC}, only the comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the power supply.

ANALOG DEVICES

Integrated Circuit Low Drift Voltage Reference

AD580

FEATURES
3-Terminal Device:
Voltage In/Voltage Out
V_{out} = 2.5V ±1%: 4.5V < V_{in} < 30V
Excellent Temperature Stability:
10ppm/°C (AD580M)
10ppm/°C (AD580U)
Excellent Long Term Stability: 250μV (25μV/month)
Low Quiescent Current: 1.0mA max
Small IC Package: TO-52 Can
10mA Current Output Capability
Low Cost: $2.00 (100's, AD580J)



PRODUCT DESCRIPTION

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output voltage for inputs between 4.5V and 30V. A unique combination of advanced circuit design and sophisticated thin film resistor processing capability provides the AD580 with a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.0mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8, 10, and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580, allowing operation with 5 volt logic supplies, makes the AD580 a good choice for all digital panel meter applications.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of -55 to +125°C.

PRODUCT HIGHLIGHTS

1. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
2. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for panel meter applications.
3. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities below 10ppm/°C and long term stability better than 250μV.
4. The low quiescent current drain and fast turn-on time of the AD580 make it ideal for CMOS and other low power system applications.
5. Every AD580 is baked for 48 hours at +200°C, temperature cycled 10 times from −65 to +150°C, and receives a high impact shock test.

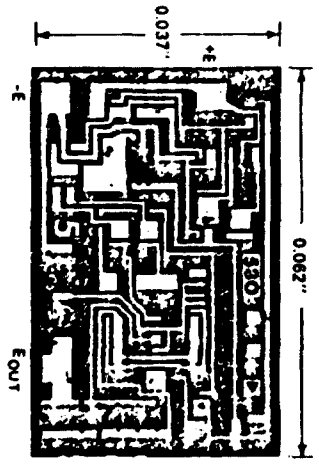
Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1733 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS (typical @ E_{in} = +15V and 25°C unless otherwise specified)

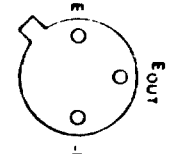
MODEL	AD580J	AD580K	AD580L	AD580M	AD580S	AD580T	AD580U
ABSOLUTE MAX RATINGS							
Input Voltage	40V E_{in}	•	•	•	•	•	•
Power Dissipation @ +25°C							
Ambient Temperature	350mW	•	•	•	•	•	•
Derate Above +25°C	2.8mW/°C	•	•	•	•	•	•
Operating Junction Temp Range	-55 to +150°C	•	•	•	•	•	•
Storage Temperature Range	-65 to +175°C	•	•	•	•	•	•
Lead Temperature (soldering, 10 sec)	+300°C	•	•	•	•	•	•
Thermal Resistance							
Junction to Case	100°C/W	•	•	•	•	•	•
Junction to Ambient	360°C/W	•	•	•	•	•	•
Operating Temperature Range	0 to +70°C	•	•	•	-55 to +125°C	-55 to +125°C	-55 to +125°C
OUTPUT VOLTAGE	2.425V min (2.575V max)	2.450V min (2.550V max)	••	2.475 min (2.525 max)	2.425V min (2.575V max)	••	2.475 min (2.525 max)
OUTPUT TURN-ON SETTLING TIME[1]	6.0μsec to 0.04%	•	•	•	•	•	•
OUTPUT VOLTAGE CHANGE							
T_{min} to T_{max}	15mV max (85ppm/°C)	7mV max (40ppm/°C)	4.3mV max (25ppm/°C)	1.75mV max (10ppm/°C)	25mV max (55ppm/°C)	11mV max (25ppm/°C)	4.5mV max (10ppm/°C)
LINE REGULATION							
$7V \leq V_{in} \leq 30V$	6mV max (0.6mV typ)	4mV max (0.6mV typ)	2mV max	2mV max	6mV max (0.6mV typ)	2mV max	2mV max
$4.5V \leq V_{in} \leq 7V$	3mV max (0.3mV typ)	2mV max (0.3mV typ)	1mV max	1mV max	3mV max (0.3mV typ)	1mV max	1mV max
LOAD REGULATION							
ΔI = 10mA	10mV max	•	•	•	•	•	•
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	•	•	•	•	•	•
NOISE (0.1 to 10Hz)	60μV(p-p)	•	•	•	•	•	•
STABILITY							
Long Term	250μV	•	•	•	•	•	•
Per Month	25μV	•	•	•	•	•	•
PRICE							
(1-24)	$3.00	$6.00	$8.25	$12.50	$11.25	$18.00	$37.50
(25-99)	$2.40	$4.80	$6.90	$10.00	$9.00	$14.50	$30.00
(100-999)	$2.00	$4.00	$5.75	$8.25	$7.50	$12.00	$25.00

NOTE 1: Self heating time constant will depend on heat sinking, raw supply voltage and load conditions.

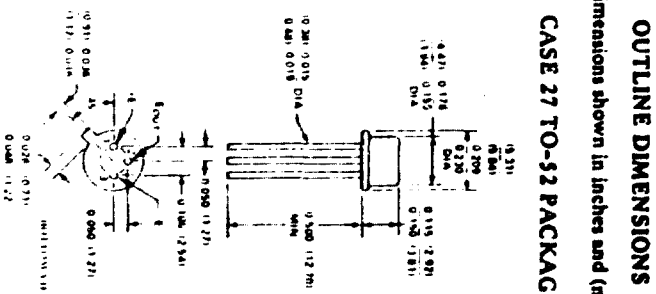
*Specification same as AD580J.
**Specification same as AD580K.
Specifications and prices subject to change without notice.



BONDING DIAGRAM



BOTTOM VIEW



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

CASE 27 TO-52 PACKAGE

National Semiconductor

Voltage Comparators

LM139/LM239/LM339, LM139A/LM239A/LM339A, LM2901, LM3302 low power low offset voltage quad comparators

general description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters, pulse, squarewave and time delay generators, wide range VCO, MOS clock timers, multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic– where the low power drain of the LM339 is a distinct advantage over standard comparators.

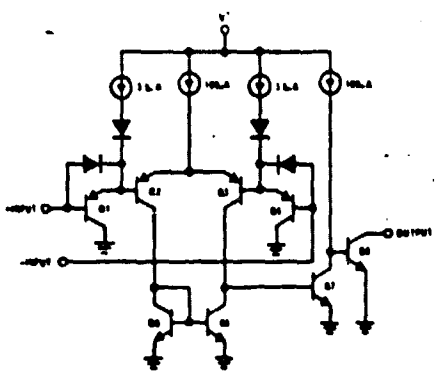
advantages

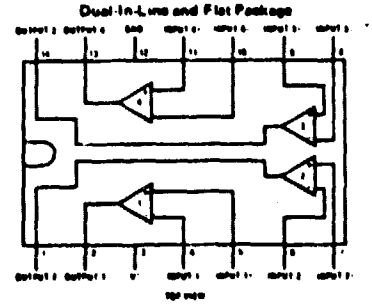
- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

features

- Wide single supply voltage range or dual supplies
  LM139 series, 2 V_{DC} to 36 V_{DC} or
  LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  LM3302 2 V_{DC} to 28 V_{DC} or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) – independent of supply voltage (2 mW/comparator at +5 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and offset voltage ±3 mV
- Input common-mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

schematic and connection diagrams





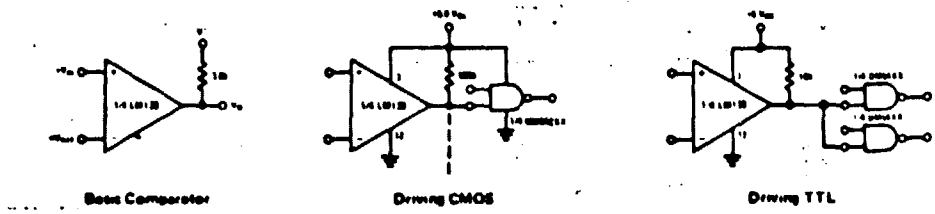
Order Number LM139D, LM139AD, LM239D or LM239AD
See NS Package D14E

Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package J14A

Order Number LM139F, LM139AF, LM239F or LM239AF
See NS Package F14A

Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package N14A

typical applications (V^+ = 5.0 V_{DC})



Basic Comparator | Driving CMOS | Driving TTL

LX1600 Series – See Package PX6
LX1700 Series – See Package PX7
LX1700D Series – See Package PX7D

LX1600A, 1601A, 1602A, 1603A, 1610A, 1620A, LX1700A, 1701A, 1702A, 1703A, 1710A, 1720A, 1730A absolute pressure transducers 10–20 psia to 0–300 psia

LX1601D, 1602D, 1603D, 1604D, 1610D, 1611D, 1612D, 1620D, LX1701D, 1702D, 1703D, 1704D, 1710D, 1711D, 1712D, 1720D differential pressure transducers ±5 psid to 0–100 psid

LX1601G, 1602G, 1603G, 1604G, 1610G, 1611G, 1612G, 1620G, LX1701G, 1702G, 1703G, 1704G, 1710G, 1711G, 1712G, 1720G, 1730G gage pressure transducers ±5 psig to 0–300 psig

general description

These rugged devices are highly accurate, completely field interchangeable temperature compensated linear pressure transducers

A fully signal conditioned transducer with a 10 Vdc output is provided in a small ceramic hybrid circuit configuration ready for PC board mounting (LX1600 series) or surrounded by a tough zinc diecast housing with a molded connector. A nylon molded housing is available where metal enclosures are forbidden. All devices include a voltage regulated input and an operational amplifier output. A conformal coating protects all portions of the circuit from most corrosive or conductive fluids

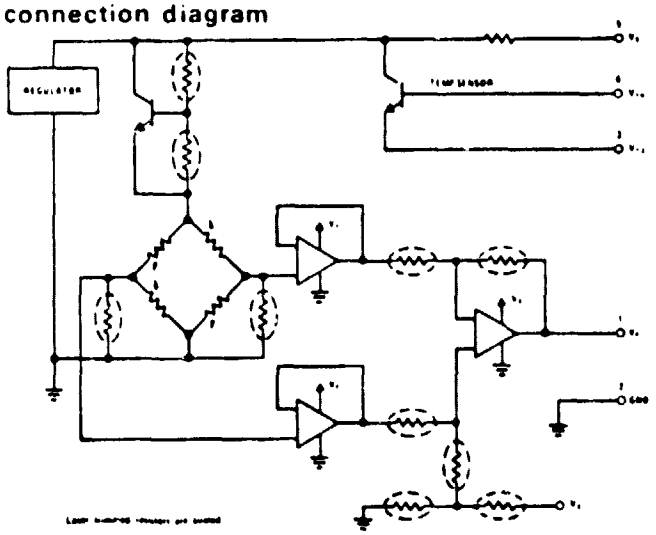
features

- Field interchangeability within ±1.5% of span
- ±3% of span overall accuracy
- Temperature coefficients better than ±0.03% of span/°C (±0.01% of span/°F)
- Repeatability better than ±0.5% of span
- Temperature measurement capability at point of pressure sensing
- Available from local National distributors

applications

- Food and beverage processing
- Medical electronics
- Computer pneumatics
- Hot bulb thermometry
- Fluid systems proportional control
- Hydraulic and pneumatic controls
- Heating, ventilation, refrigeration and air conditioning controls
- Automotive diagnostic, safety, and control systems

circuit and connection diagram



product selection guide

Nominal characteristics (V_E = 15V, T_A = 21°C) (Notes 1 and 2)

PRESSURE RANGE	DEVICE TYPE	CALIBRATED OUTPUT VOLTAGE		PROOF PRESSURE	MAX PRESSURES
ABSOLUTE		LOW END	HIGH END		PKG BURST
0 to 15 psia	LX1600A, LX1700A	2.5 ±0.15V	7.5 ±0.15V	40 psia	300 psia
10 to 20 psia	LX1601A, LX1701A	2.5 ±0.2V	12.5 ±0.2V	40 psia	300 psia
0 to 15 psia	LX1602A, LX1702A	2.5 ±0.15V	12.5 ±0.15V	40 psia	300 psia
0 to 30 psia	LX1603A, LX1703A	2.5 ±0.15V	12.5 ±0.15V	60 psia	300 psia
0 to 60 psia	LX1610A, LX1710A	2.5 ±0.15V	12.5 ±0.15V	90 psia	300 psia
0 to 100 psia	LX1620A, LX1720A	2.5 ±0.15V	12.5 ±0.15V	150 psia	300 psia
0 to 300 psia	LX1730A	2.5 ±0.15V	12.5 ±0.15V	450 psia	500 psia (Note 3)
DIFFERENTIAL	(Note 4)				COMMON MODE
−5.0 to +5.0 psid	LX1601D, LX1701D	2.5 ±0.2V	12.5 ±0.2V	40 psid	300 psia
−5.0 to +5.0 psid	LX1611D, LX1711D	2.5 ±0.2V	12.5 ±0.2V	100 psid	300 psia
−10.0 to +10.0 psid	LX1612D, LX1712D	2.5 ±0.15V	12.5 ±0.15V	125 psid	300 psia
0 to 15 psid	LX1602D, LX1702D	2.5 ±0.15V	12.5 ±0.15V	40 psid	300 psia
0 to 30 psid	LX1603D, LX1703D	2.5 ±0.15V	12.5 ±0.15V	60 psid	300 psia
−15 to +15 psid	LX1604D, LX1704D	2.5 ±0.15V	12.5 ±0.15V	40 psid	300 psia
0 to 60 psid	LX1610D, LX1710D	2.5 ±0.15V	12.5 ±0.15V	90 psid	300 psia
0 to 100 psid	LX1620D, LX1720D	2.5 ±0.15V	12.5 ±0.15V	150 psid	300 psia
GAGE					SEAL
−5.0 to +5.0 psig	LX1601G, LX1701G	2.5 ±0.2V	12.5 ±0.2V	40 psig	50 psig
−5.0 to +5.0 psig	LX1611G, LX1711G	2.5 ±0.2V	12.5 ±0.2V	100 psig	115 psig
−10.0 to +10.0 psig	LX1612G, LX1712G	2.5 ±0.15V	12.5 ±0.15V	125 psig	145 psig
0 to 15 psig	LX1602G, LX1702G	2.5 ±0.15V	12.5 ±0.15V	40 psig	50 psig
0 to 30 psig	LX1603G, LX1703G	2.5 ±0.15V	12.5 ±0.15V	60 psig	70 psig
−15 to +15 psig	LX1604G, LX1704G	2.5 ±0.15V	12.5 ±0.15V	40 psig	50 psig
0 to 60 psig	LX1610G, LX1710G	2.5 ±0.15V	12.5 ±0.15V	90 psig	100 psig
0 to 100 psig	LX1620G, LX1720G	2.5 ±0.15V	12.5 ±0.15V	150 psig	175 psig
0 to 300 psig	LX1730G	2.5 ±0.15V	12.5 ±0.15V	450 psig	500 psig

absolute maximum ratings (Note 5)

Excitation Voltage	30 V_{DC}	(Note 2)
Output Current, I_o	20 mA	
Operating Temperature Range	−40°C to +125°C	
Lead Temperature (Soldering, 10 seconds)	300°C	

electrical specifications

PARAMETER	CONDITIONS	LX16 & 1700 01, 02A LX16 & 1701, 02, 11D LX16 & 1701 02, 11G		LX16 & 1703 10A LX16 & 1703 04, 10, 12D LX16 & 1703, 04, 10, 12G		LX16 & 1720, 1730A LX16 & 1720D LX16 & 1720, 1730G		UNITS
		TYP	MAX	TYP	MAX	TYP	MAX	
Temperature Coefficient	25°C to +75°C							
Centigrade	V_E = 15V (Note 2)	±0.04	±0.09	±0.03	±0.06	±0.02	±0.03	% span/°C
Fahrenheit		±0.033	±0.050	±0.017	±0.025	±0.011	±0.017	% span/°F
Temperature Coefficient	−40°C to −25°C and							
Centigrade	+75°C to +125°C	±0.04	±0.18	±0.03	±0.12	±0.02	±0.06	% span/°C
Fahrenheit	V_E = 15V (Note 2)	±0.033	±0.099	±0.017	±0.067	±0.011	±0.033	% span/°F
Linearity and Hysteresis	Best Straight Line	±0.2	±0.5	±0.2	±0.5	±0.2	±0.5	% span
Repeatability	(Note 7)	±1.0	±2.0	±0.75	±1.50	±0.50	±0.75	% span
Output Voltage Sensitivity ($\Delta V_o / \Delta V_E$)	14.5V < V_E < 25	±0.3	0.5	±0.3	±0.5	±0.3	±0.5	%
Transducer Bias Current	(Note 2)	15	20	15	20	15	20	mA

Note 1 70°F = 21°C, 170°F = 78°C, 240°F = 116°C, 572°F = 300°C, 1 mV/°F = 1.8 mV/°C, 1 psi = 51.71 TORR (mmHg) = 2.036 in Hg = 27.61 in H_2O = 2.307 ft H_2O = 68.95 mbs

Note 2 All devices in the LX16 and 1700 Series except the LX16 and 1700A are regulated and scaled for excitation 14.5 V < V_E < 25V. The LX16 and 1700A are regulated and scaled for excitation 7V < V_E < 25V so as to be ideal for battery operation. Upon special request, the endpoint scaling and regulation of any LX16 and 1700 Series device can be set for battery operation.

Note 3 Package burst pressures are shown for the LX1600 Series except for the LX1630A which cannot be purchased as a standard product without the Zinc or Nylon outer package.

Note 4 The LX17000 Series outer package is available in Nylon only.

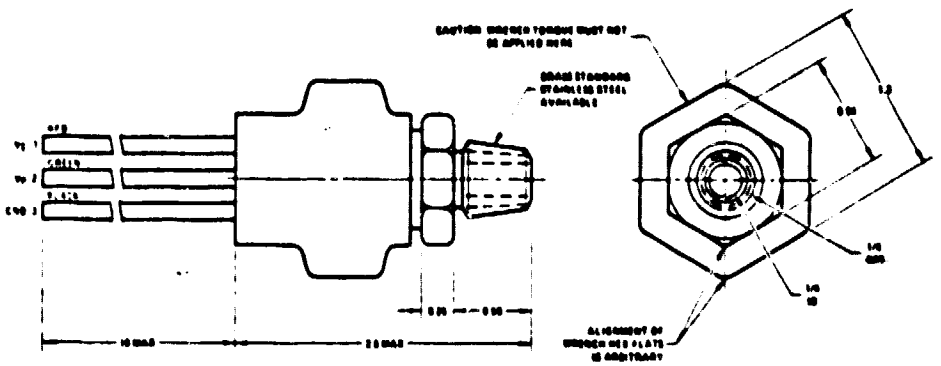
Note 5 The transducers are coated to protect against most corrosive or conductive fluids. Additional isolation is recommended for in vivo medical applications.

Note 6 Upon special request the end points can be set anywhere between a minimum of one volt and a maximum of V_E − 2.0 volts. Similarly the sensitivity can be set up to a max of 5V/psi.

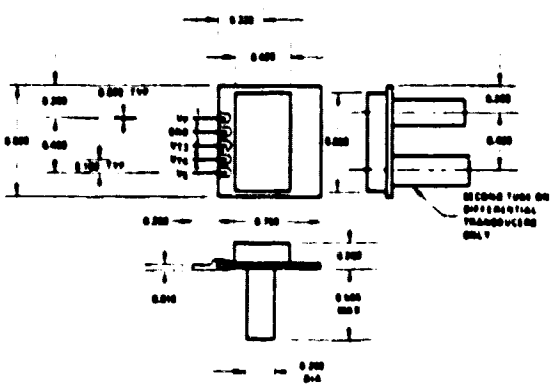
Note 7 This is defined as the output voltage reproducibility over the pressure range from −25°C to +75°C.

Note 8 Caution – Improper constraint of transducer package will be exhibited as parasitic errors in the output voltage.

Package Outlines



PX4
1/4" NPT Pressure Transducer Package



PX6
0.2" Port, Hybrid Pressure Transducer Package

LX5600/LX5600A, LX5700/LX5700A temperature transducers

general description

The LX5600 LX5700 series temperature transducers are highly accurate temperature measurement or control systems for use over a −55°C to +125°C temperature range. Fabricated on a single monolithic chip they include a temperature sensor, stable voltage reference and operational amplifier.

The output of the LX5600/LX5700 is directly proportional to temperature in degrees Kelvin at 10 mV/°K. Using the internal op amp with external resistors any temperature scale factor is easily obtained. By connecting the op amp as a comparator the output will switch as the temperature transverses the set point making the device useful as an on-off temperature controller.

An active shunt regulator is connected across the power leads to the LX5600/LX5700 to provide a stable voltage reference. In addition to providing a reference, it regulates the operating voltage to 6.8V. This allows the use of any power supply voltage with suitable external resistors.

The op amp can amplify the 10 mV/°K from the sensor to almost any desired output. The input bias current is low and relatively constant with temperature ensuring high accuracy when high source impedance is used. Further, the output collector can be returned to a voltage higher than 6.8V allowing the LX5600/LX5700 to drive lamps and relays from a 28V supply.

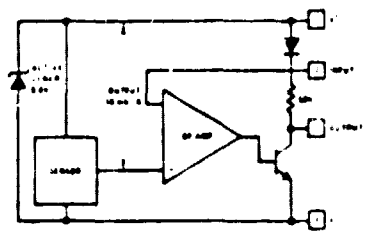
The LX5600 uses the difference in emitter base voltage of transistors operating at different current densities as the basic temperature sensitive element. Since this output depends only on transistor matching the same reliability and stability as present op amps can be expected.

The LX5600 and LX5600A operate over a −55°C to +125°C range and are available in 4 lead TO-5 package. The LX5700 and LX5700A also operate over the −55°C to +125°C range and are available in the 4 lead TO-46 package.

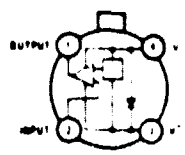
features

- Calibration accuracy of ±4°C over −55°C to +125°C
- Internal op amp with frequency compensation
- Linear output of 10 mV/°K (10 mV/°C)
- Directly calibrated in degrees Kelvin
- Output can drive loads up to 35V
- Internal stable voltage reference
- Four lead device—minimizing wiring

block and connection diagrams



TO-5 Metal Can Package

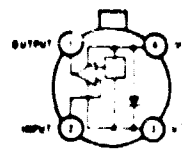


TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE

Order Number LX5600AH or LX5600H

TO-46 Metal Can Package



TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE

Order Number LX5700AH or LX5700H

absolute maximum ratings

Supply Voltage	Internally Regulated	Output Short Circuit Duration	Indefinite
Supply Current (Externally Set)	10 mA	Operating Temperature Range	−55°C to +125°C
Output Collector Voltage	36V	Storage Temperature Range	−65°C to +150°C
Input Voltage Range	0V to +7.0V	Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LX5600A/LX5700A			LX5600/LX5700			UNITS
		TYP VOLTS	ERROR ±mV	ERROR ± % OF SPAN	TYP VOLTS	ERROR ±mV	ERROR ± % OF SPAN	
Output Voltage (Note 2)	T_A = +25°C	2.98	40	2.22	2.98	80	4.44	
Output Voltage (Note 2)	T_A = −55°C	2.18	40	2.22	2.18	80	4.44	
Output Voltage (Note 2)	T_A = 125°C	3.98	40	2.22	3.98	80	4.44	
Linearity	ΔT ≤ +180°C	0.018			0.018			
Long Term Stability	T_A = 125°C	±0.002			±0.002			
Repeatability	T_A = 125°C	±0.002			±0.002			
VOLTAGE REFERENCE		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Breakdown Voltage	1 mA ≤ I_z ≤ 5 mA	6.68	6.85	7.12	6.55	6.85	7.25	V
Reverse Breakdown Voltage Change With Current	1 mA ≤ I_z ≤ 5 mA		10	25		10	35	mV
Temperature Stability			20	60		20	85	mV
Dynamic Impedance	I_z = 1 mA		3.0			3.0		Ω
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz		30			30		μV
Long Term Stability	T_A = +125°C		6.0			6.0		mV
OP AMP								
Input Bias Current	T_A = +25°C		35	75		3[illegible]	150	nA
Input Bias Current			45	150		[illegible]	250	nA
Voltage Gain	R_L = 36k, V** = 36V	2000	15000		1500	15000		V/V
Output Leakage Current	T_A = 25°C (Note 3)		0.2	1.0	2.0	0.2		μA
Output Leakage Current	(Note 3)		1.0	5.0	8.0	1.0		μA
Output Source Current	V_{OUT} ≤ 4.05	10			10			μA
Output Sink Current	1V ≤ V_{OUT} ≤ 36V	2.0			2.0			mA

Note 1: These specifications apply for −55°C ≤ T_A ≤ +125°C and 0.9 mA ≤ I_{SUPPLY} ≤ 1.1 mA unless otherwise specified.

Note 2: The output voltage applies to the basic thermometer configuration with the output and feedback terminals shorted and a load resistance of [illegible] 1.0 MΩ. This is the feedback sense voltage and includes errors in both the sensor and op amp. This voltage is specified for the sensor in a rapidly stirred oil bath.

Note 3: The output leakage current is specified with ≥ 100 mV overdrive. Since this voltage changes with temperature, the voltage drive for turn-off changes and is defined as V_{OUT} (with output and input shorted) −100 mV. This specification applies for V_{OUT} = 36V.

application hints

Although the LX5600/LX5700 were designed to be as trouble-free as possible, certain precautions should be taken to insure the best possible performance.

Like any temperature sensor, internal power dissipation will raise the sensor temperature above ambient. Nominal operating current for the shunt regulator is 1.0 mA and causes 7.0 mW of power dissipation. In free, still, air this raises the package temperature by about 1.2°K. Although the regulator will operate at higher reverse currents and the output will drive loads up to 5.0 mA, these higher currents can raise the sensor temperature over 19°K above ambient—degrading accuracy. Therefore, the sensor should be operated at the lowest possible power level.

With moving air, liquid or surface temperature sensing, self heating is not as great a problem since the measured media will conduct the heat from the sensor. Also, there are many small heat sinks designed for transistors which will improve heat transfer to the sensor from the surrounding medium. A small finned clip-on heat sink is quite effective in free air. It should be mentioned that the LX5600 die is on the base of the package and therefore cooling to the base is preferrable.

The internal reference [illegible] provides a temperature stable voltage for offsetting the temperature output or setting a comparison point in temperature controllers. However, since this reference is at the same temperature as the sensor temperature changes will also cause reference drift. For application where maximum accuracy is needed an external reference should be used. Of course, for fixed temperature controllers the internal reference is adequate.

12 BIT MN5210 SERIES ADJUSTMENT–FREE A/D CONVERTERS

DESCRIPTION

The MN5210 Series Devices are extremely fast 12 Bit Successive Approximation A/D Converters providing both parallel and serial output. These devices have a maximum conversion time of 13 μSec which allows full accuracy with a 1 MHz clock.

These hybrid converters are housed in miniature 24 pin glass/ceramic dual-in-line packages. Miniature size, low power consumption and adjustment free operation contribute to the reasons why these converters provide the user with the best possible selection for compact and efficient systems.

All converters are completely laser trimmed and totally adjustment free. They require only one external component, a non-critical 2.2μf capacitor. Additionally, due to highly stable thin film resistor networks, these converters provide long term maintenance free operation.

These converters are available in three input voltage ranges: 0 to −10 volts (MN5210/13), ±5 volts (MN5211/14), and ±10 volts (MN5212/15). For each of these input ranges, the user has the option of specifying a model complete with an internal reference or for improved absolute accuracy, a model which uses an external reference.

In all cases ±1/2 LSB linearity is guaranteed over the entire operating temperature range. Additionally all units are tested 100% for linearity and accuracy at their temperature extremes as well as at room temperature.

All models of the MN5210 Series may be procured for operation over the entire −55°C to +125°C military temperature range ("H" models) with the same end temperature operating characteristics as the commercial 0°C to 70°C range. In addition, full military temperature operation devices are available processed to the Class B requirements of MIL-STD-883 (inquire about Micro Networks' "Option B").

FEATURES

- **Very High Speed**
  1.0 μSec/Bit max.
- **Totally adjustment-free**
  No full scale or zero adjustment necessary
- **Low Power**
  700mW
- **Small**
  24 Pin DIP
- **±1/2 LSB linearity worst case**
- **Hermetically sealed package**
- **Parallel and serial outputs**
- **Full Mil operation**
  -55°C to +125°C ("H" models) Available fully screened & processed to the Class B requirements of MIL-STD-883

APPLICATIONS

- Remote Equipment
- Medical Instrumentation
- Aerospace
- Computer I/O Equipment

Micro Networks Corporation
324 Clark Street • Worcester, Massachusetts 01606
Tel: (617) 852-5400 • TWX 710-340-0067

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0 to 70°C (-55°C to +125°C "H" Models)
Storage Temperature	−65°C to +150°C
Positive Supply	+18 Volts
Negative Supply	−18 Volts
Logic Supply	+7 Volts
Analog Input	±25 Volts
Digital Outputs	Logic Supply
Digital Inputs	+5.5 Volts
Reference Supply (Models MN5213, 14, 15 and 16)	−15 Volts

SPECIFICATIONS (T_A=25°C, Voltages ±15, +5 unless otherwise stated)

PERFORMANCE:

INPUT RANGE	INPUT IMPEDANCE
0 to −10V	6.7k
+5V to −5V	6.7k
+10V to −10V	13k
0 to +10V	6.7k

	HIGH PERFORMANCE MN5210 MN5211 MN5212 MN5216		HIGH ACCURACY (Ext.Ref= -10.000V) MN5213 MN5214 MN5215		
	TYP.	MAX.	TYP.	MAX.	UNITS
Resolution		12		12	Bits
Linearity (0° to 70°C) (Note 1)		±½		±½	LSB
Zero Error		1		1	LSB
Zero Error (0° to 70°C) (Note 1)		2		2	LSB
Absolute Accuracy 25°C (Note 2)		2		2	LSB
Absolute Accuracy (0° to 70°C) (Notes 1 & 2)		±.4		±.1	%
Conversion Time (Note 5)		13		13	µSec
Power Supply Requirements					
Current Drain +15 Volt Supply	23	28	23	28	mA
Current Drain −15 Volt Supply	15	19	5	6.3	mA
Current Drain + 5 Volt Supply	25	42	25	42	mA
Current Drain −10 Volt Reference			1.5	2.0	mA
Power Supply Rejection					
+15 Volts (Note 3)	±.02		±.02		%F.S.R./%Supply
−15 Volts (Note 3)	±.05		±.02		%F.S.R./%Supply
Power Consumption	695	915	567	744	mW

LOGIC RATINGS

	MIN.	TYP.	MAX.	UNITS
Input Logic Commands				
Logic "0"			.8	Volts
Logic "1"	2.0			Volts
Loading		.5		TTL Load
Clock Input Pulse Width	100			nSec
Output Logic				
Logic "0"			.4	Volts
Logic "1"	2.4	3.6		Volts
Serial Output				NRZ
Parallel Output (See Timing Diagram)				
Fanout-High	8			TTL Load
Fanout-Low	2			TTL Load

LOGIC CODING

MN5210/5213	MN5211/5214	MN5212/5215	MN5216	MSB LSB
OV	+5.0000	+10.000	+9.9976	0 0 0 0 0 0 0 0 0 0 0 0
−5.000V	0	0	+4.9976	1 0 0 0 0 0 0 0 0 0 0 0
−9.9976V	−4.9976	−9.995	0	1 1 1 1 1 1 1 1 1 1 1 1

NOTE 1. For "H" models, the specification applies for operation over the temperature range of -55°C to +125°C.

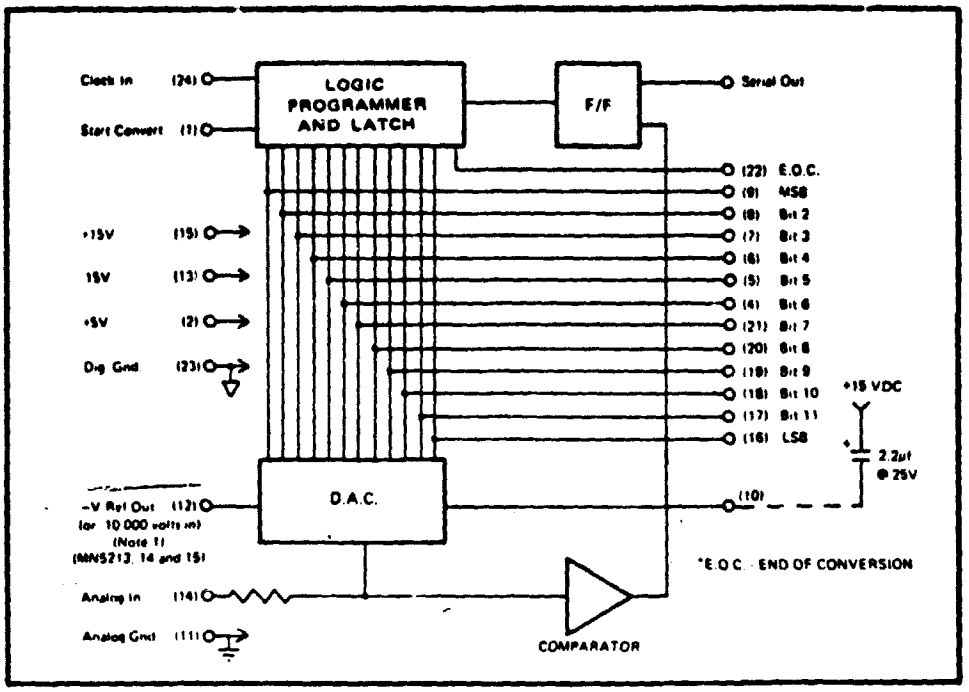
NOTE 2. Absolute accuracy includes all errors, gain, zero, and linearity. All converters are tested 100% at the temperature extremes for linearity and absolute accuracy.

NOTE 3. For proper operation ±15 Volt power supplies tolerance should not be greater than ±3%.

NOTE 4. FSR is the abbreviation for "Full Scale Range" and is equal to the peak to peak output voltage, i.e. 10 volts for ±5V range.

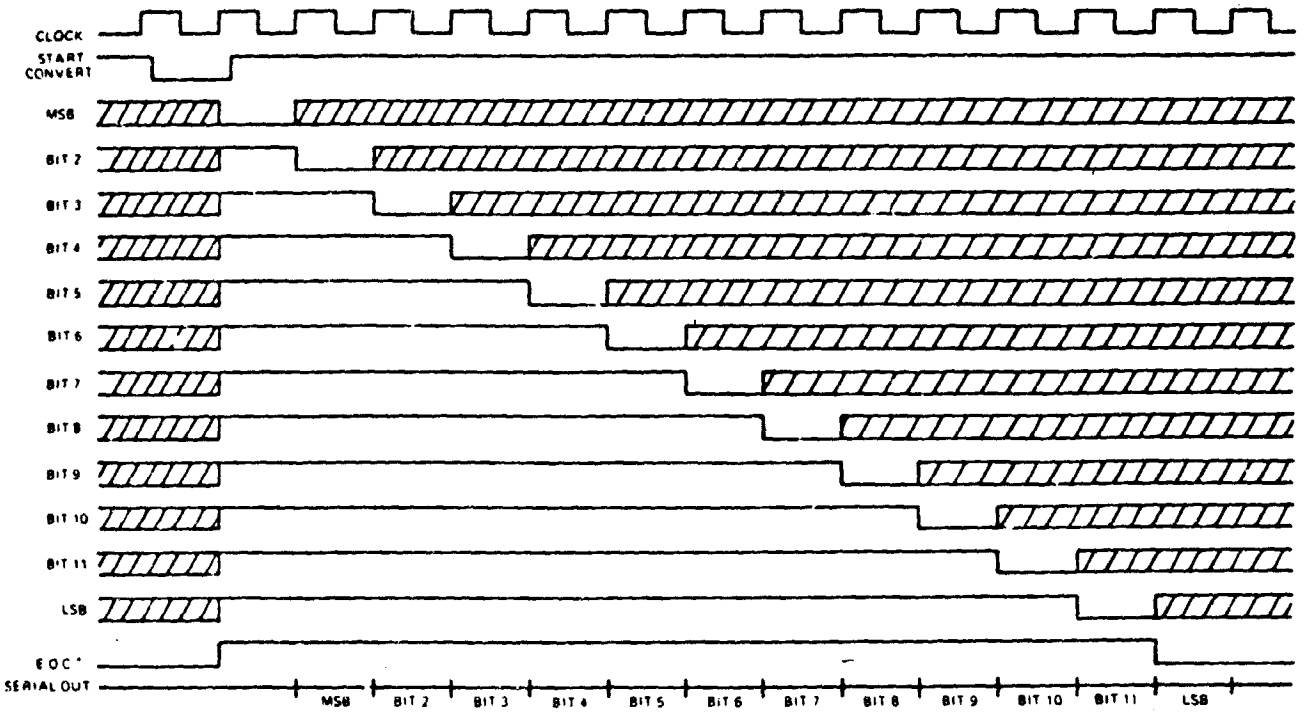
NOTE 5. Conversion time is specified with external 2.2µf capacitor (see block diagram). Without this capacitor conversion time is typically 20µ Sec.

BLOCK DIAGRAM



NOTE 1. The maximum current which should be drawn from the -V Ref output (Available only on internal reference models) is 100 µA.

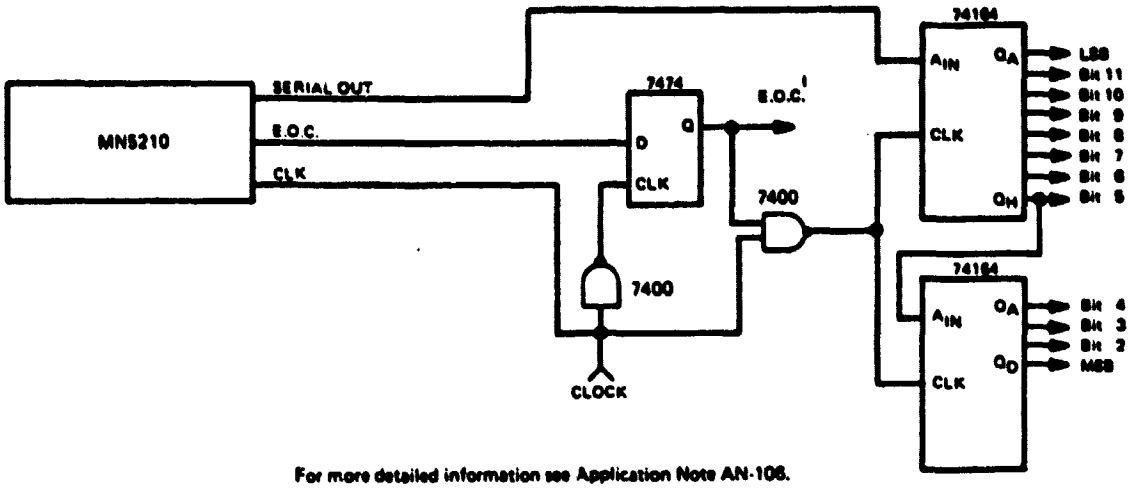
TIMING DIAGRAM



NOTES:

1. Shaded areas shown for parallel data outputs denotes states determined by data input immediate prior to shaded area.
2. For continuous operation connect start convert (Pin 1) to end of conversion (Pin 22).
3. Reset the converter by holding the start 'low' during a low to high transition of the clock. The start must be low for a minimum of 25 nSec prior to the clock transition. After the start is again set high the conversion will begin on the next low to high transition of the clock. The start may be set low at any time during a conversion to reset and begin again.
4. At the end of conversion the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
5. The serial output is non-return to zero.
6. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.
7. Micro Networks reserves the right to make design, specification, and process changes and improvements.

APPLICATION
SERIAL TO PARALLEL CONVERSION



For more detailed information see Application Note AN-108.

PIN DESIGNATIONS

Pin 1	Start	Pin 13	−15V
Pin 2	+5V	Pin 14	Analog in
Pin 3	Serial Out	Pin 15	+15V
Pin 4	Bit 6	Pin 16	LSB
Pin 5	Bit 5	Pin 17	Bit 11
Pin 6	Bit 4	Pin 18	Bit 10
Pin 7	Bit 3	Pin 19	Bit 9
Pin 8	Bit 2	Pin 20	Bit 8
Pin 9	MSB	Pin 21	Bit 7
Pin 10	Ext. Capacitor	Pin 22	E.O.C. (end of conversion)
Pin 11	Analog Ground	Pin 23	DIG Grd
Pin 12	-V ref out (int. ref. models) -V ref in (ext. ref. models)	Pin 24	Clock Input

MODEL NUMBER **MN521X H/B**

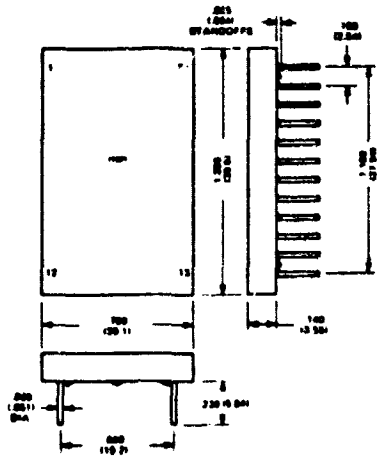
Model selection
Add "H" for -55 to +125°C operation
Add "/B" for 100% screened (883 Class B)*

Example

0 to 70°C(±5V, Int. Ref.)	MN5211
-55 to +125°C Operation	MN5211H
-55 to +125°C and 100% screened *883	MN5211H/B

*Micro Networks Option "B"

ORDERING INFORMATION



Outline dimensions in inches (and millimeters).

Micro Networks Corporation
324 Clark Street • Worcester, Massachusetts 01606
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FINAL PERFORMANCE DATA

MODULAR POWER SUPPLIES

DATE 10-4-7X

PART NO. ASN-M5.5/9V-C5/5V-CA SERIAL NO. A4190

OUTPUT VOLTAGE VS INPUT VOLTAGE AT 74.5 WATTS

INPUT VOLTAGE	E_o # 1 5.5 VDC	E_o # 2 5 VDC	E_o # 3 VDC	E_o # 4 VDC	E_o # 5 VDC	E_o # 6 VDC
24	5.506	5.021				
30	5.509	5.022				
E_o adj	4.90-5.89	4.5V-5.47				
OUTPUT VOLTAGE & RIPPLE VS OUTPUT POWER						
OUTPUT POWER	E_{IN} = 27 VDC					
100%	5.507	5.022				
50%	5.511	5.021				
RIPPLE (VRMS)						
100%	18 mV	5.1mV				
50%	18mV	4.5mV				

INPUT CURRENT

INPUT VOLTAGE	FULL LOAD	HALF LOAD	NO LOAD
24	5.0	2.5	0.25A
30	4.5	2.4	0.25A

TEST CONDITIONS

1. AMBIENT TEMPERATURE 25° C
2. HEAT SINK: ALUMINUM
   19" X 7" X 1/8" THICK

RM

ARNOLD MAGNETICS CORP.
11520 W. JEFFERSON BLVD.
CULVER CITY, CA. 90230
(213) 870-7014

AMC 9

FINAL PERFORMANCE DATA
DC INPUT

DATE 10/16/78

MODEL NO. SHU-2/4V

SERIAL NO. A4189

OUTPUT VOLTAGE vs INPUT VOLTAGE AT 8 WATTS			
INPUT VOLTAGE (VDC)	OUTPUT NUMBER 1 2 VDC + RED TO- BLACK	OUTPUT NUMBER 2 _____ VDC + _____ TO- _____	OUTPUT NUMBER 2 _____ VDC + _____ TO- _____
26	2.000 VDC		
30	1.999 VDC		
OUTPUT VOLTAGE & RIPPLE vs OUTPUT POWER (AT 28 VDC INPUT)			
OUTPUT POWER (% OF) (RATED)			
100%	2.000 VDC		
50	2.006 VDC		
RIPPLE (mVRMS)			
100%	4.4 mv		
50	3.3 mv		
INPUT CURRENT vs OUTPUT POWER (AT 28 VDC INPUT)			
100%	.75 Amp.		
50			
U/L	.15 Amp.		

TEST CONDITIONS

1. AMBIENT TEMPERATURE 25°C
2. HEAT SINK: ALUMINUM 19" x 7" x 1/8" THICK

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CULVER CITY, CALIFORNIA 90230