MODIFIED REFERENCE SPS WITH SOLID STATE TRANSMITTING ANTENNA

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1.0 INTRODUCTION

The motivations for considering solid state microwave power amplifiers for the solar power satellite transmitting antenna have been the possibilities of greatly increased system reliability due to elimination of electron tube cathodes, a lower mass per unit power and transmitting array area due to the high power densities obtainable in semiconductors (the active region of a power GaAs FET has a power density exceeding 10^{15}W m^{-3}!), and, probably, cost savings due to development of small hardware items that can be handled by individuals instead of organizations.

In order to provide a fair assessment of where we stand today with regard to solid state SPS technology, the design described here is close to that of the NASA/DOE reference and is implemented using today's solid state technology with only a small "push." The small push is raising the efficiency of DC-RF conversion from the .68 obtained by RCA in 1975 to somewhat over .8 of the solid state SPS. This is generally considered feasible by semiconductor industry representatives.

Other solid state SPS configurations can yield somewhat better performance. However, these generally do not provide as fair a vehicle for comparison with the reference and usually also incorporate somewhat more advanced technologies.

2.0 SOLID STATE MICROWAVE POWER AMPLIFIER TECHNOLOGY

Currently a wide variety of solid state devices suitable for use as microwave amplifiers exist. These include bipolar and field effect transistors, many types of two-terminal devices (tunnel, Gunn, IMPATT, BARITT and TRAPATT diodes) and electron bombarded semiconductors (EBS). (EBS have been included as being solid state since the electron beam only supplies a small control current, with the bulk of the supply current staying in the semiconductor.) For those active devices with over two terminals, there are several classes of circuit configurations that the active devices may be used in. Finally, there is a growing number of commonly used solid state materials out of which components may be fabricated, using several types of process at each step of the fabrication.

State of the art power-added efficiency, gain and single device power as a function of frequency for various types of CW microwave output solid state devices are shown on Figures 1 through 3. As technology evolves the curves will move towards the upper right-hand corners of the graphs.

Given the results of Figure 1, it would appear that there is no hope of achieving efficient solid state DC-microwave conversion in the near future. All the two terminal devices have efficiencies less than .36, which is so low as to make their use for SPS impractical. Most of the three terminal devices are not much better. However, in the case of three-terminal devices, the classes of amplifiers presently used (Classes A and B for GaAs FETs and Class C for bipolar transistor amplifiers) inherently limit their efficiency. Other classes of amplifiers, summarized on Figure 4, can have efficiencies approaching unity.

In fact, to achieve the desired efficiencies of .8 or greater requires that the devices be used in "switched mode" types of amplifiers, which attain high efficiency by minimizing the I-V product time integral over the operating cycle. This generally require device switching times about a factor of ten less than the RF period. Experimental amplifiers with efficiencies of over 90% have been built at frequencies above 100 MHz. NASA-sponsored microwave amplifier studies have recently been initiated to determine the feasibility of high efficiency at microwave frequencies.

Because of the many high frequency components in the waveforms characteristics of fast switches, efficient switching amplification devices must have large bandwidths. This leads to different device noise properties than those at the narrowband SPS reference system klystron tubes. While the switching amplifiers do have frequency selective output circuits that transform the switched waveform into a sine wave, these will not be nearly as selective as a 5-cavity klystron. However, the solid state design will benefit due to its small module size giving a larger ground footprint than that of the larger klystron module.

Achieved device gains vs frequency are shown on Figure 2. There is a striking difference between small-signal and power gain for FETs. At the SPS frequency of 2.5 GHz bipolars have about 8 db gain while GaAs FETs yield around 10 db. In general, GaAs FETs have several db more gain than bipolars throughout the spectrum. As for the other devices, IMPATTs can have gains of over 20 db and electron beam semiconductors are projected to yield about 20 db. The low gain of Static Induction Transistors (SITs) at 1 GHz eliminates them from consideration at present, although they appear to have great potential for further development due to their high power bandwidth product.

The power per device is an important SPS parameter since the number of devices which can be efficiently combined in a module is limited by circuit losses and the power per module determines the RF power density per unit transmitting array area. The single device power chart (Figure 3) shows that silicon bipolar transistors, GaAs FETs and multi-mesa IMPATTs can all handle powers above 10 watts, which is an adequate power level for SPS application. Of the devices considered here, only E-beam semiconductor devices are capable of generating a power level of 100 watts per device which would be adequate for one device per radiating element. For the other devices, power combining will be necessary.

The fundamental failure modes in semiconductor devices are wearout failure modes that tend to be concentrated at surfaces, both internal and exposed, and are generally electrochemical in origin. In the case of the internal surfaces, transport of species to and away from interfaces eventually degrades contacts. In the case of external surfaces, impurities can come in from outside to form compounds and high electric fields can cause breakdown.

EBS cathodes presently have an expected lifetime of 2×10^5 hours, over an order of magnitude less than that required for a 30-year satellite, so they appear unsuitable. The two remaining solid state amplifier candidates are GaAs FETs and Si bipolar transistors. Si bipolar lifetimes are limited by electromigration of emitter finger metallizations due to localized high current densities. This gives relatively sudden and complete hard (open or short circuit) failures, whereas GaAs FETs seem to suffer from contact degradation which decreases performance gradually.

Of the three terminal devices, GaAs Field Effect Transistors (FET's) and Si-bipolar transistors provide approximately equal power capability at 2.45 GHz and appear potentially feasible for SPS use. GaAs FET's were selected as the preferred DC-RF conversion devices because they have higher gain than silicon bipolars, higher power added efficiencies, roughly equal power capabilities at 2.5 GHz and lower device metallization current densities leading to better expected reliabilities. GaAS FET's for SPS application could be fabricated separately and mounted in hybrid fashion or combined with other components on larger GaAS chips in integrated circuits. The latter alternative is preferred because of its significantly lower costs in mass production, although it does entail somewhat more development. For conservatism and in consideration of the fact that efficient "switched mode" amplifiers require gain at frequencies higher than the fundamental, the maximum single device powers in the solid state baseline design satellite were chosen to be 7.5 watts. For devices like this, a reasonable operating voltage is 15 volts.

A current small signal GaAS FET lifetime versus temperature curve is shown on Figure 5. There is currently no lifetime data on power GaAS FET's in the literature. When it appears, it is likely to be somewhat worse than Figure 5, but Figure 5 probably represents lifetimes achievable with development of the relatively new GaAs FET technology. It should be noted that solid state devices fail with log-normal statistics. Since the SPS failure criterion is loss of 2% the transmitting array with no maintenance, the mean time to failure required for the device is about a factor of ten more than the SPS life. Thus the average junction temperature for SPS GaAS FET's should be no higher than 140°C.

Figure 6 shows current and projected GaAS FET costs with an estimated 70% production rate improvement curve (i.e., units produced at the rate of 2n per year cost 70% as much as units produced at the rate of n per year). For the anticipated projected rates, the cost per unit power for GaAS FET's are nearly the same as the projected cost per unit power for klystrons. In practice, integrated circuits with several stages of driver amplifiers and other circuitry will be incorporated with the power amplifier. Since production costs are roughly equivalent to chip size and the output FET is anticipated to use approximately 70% of the total semiconductor area, the above cost estimates are adequate to first order.

3.0 SOLID STATE ANTENNA MODULE INTEGRATION

Cost effective integration of the low power, low voltage solid-state devices into mass producible antenna array elements represents the prime challenge in solid-state microwave power transmitter design. The "natural" array element size of about a wavelength squared and radiative cooling considerations for the peak microwave density areas at the transmitting array center yield 11 devices per λ^2 at an anticipated 5.5 kw m^{-2} radiated microwave power per unit area. For central array modules of the modified reference solid-state SPS both a small module size and combining of several devices were used to get the 4-FET .6λ x .6λ microstrip cavity combining module shown in Figure 7.

To avoid the power combining losses associated with circuit hybrids, the power from 4 solid-state amplifiers is combined by direct coupling of each amplifier's output to the radiating antenna structure. The resulting savings in transmitter efficiency range from 4% to 10%, depending upon the configurations being compared. The selected power-combining antenna consists of a printed (metallized) microstrip circuit on a ceramic type dielectric substrate which is backed by a shallow lightweight aluminum cavity which sums the power of four microwave sources. The antenna behaves like two half wavelength slot-line antennas coupled together via a common cavity structure. Feedback is taken from sampling probes in the module

cavity and used to correct for amplifier phase errors. This insures that the insertion phase of each module is identical even though the power amplifiers are fabricated to relatively loose (low cost) insertion phase requirements.

The modules are fabricated by starting with metallized (microstrip) 25 mil thick alumina dielectric cards which are attached to a 7.5 mil thick aluminum sheet metal carrier. A 7.5 mil thick stamped aluminum back plate is then attached, covering the substrate and all circuit components. This back cover defines the antenna cavity as well as shielding the otherwise exposed electronic components on the substrate. The high thermal conductivity of the aluminum components and of the alumina substrate allows the module's waste heat to spread to all surfaces as evenly as possible.

For the lower power density areas of the array an alternate dipole radiator module configuration is proposed. (See Figure 8.) This module design is approximately a third the mass per unit area of the 4-FET cavity radiator module because it has nearly no ceramic and significantly less metallization.

4.0 ANTENNA INTEGRATION

Variations of the basic cavity radiator and dipole radiator modules have been used to define a 1.42 km diameter transmitting antenna with a 9.54 db 10-step Gaussian taper similar to that of the reference SPS. Since its peak transmitted power per unit area is ¼ that of the reference satellite, its grid output power is half that of the reference, or 2.5 Gw.

Antenna quantization scheme specifications are summarized on Figure 9. There are seven basic module types of varying mass. As the 4-FET cavity radiator and 2-FET dipole module powers are reduced the module masses may also be reduced by removing superflous metal not required for lateral thermal conduction. The 2-FET cavity radiator can also take advantage of reduced dielectric mass. No claim is made that these designs are optimized; they represent hopefully conservative estimates for likely module configurations.

To reduce I^2R power bussing losses the 15 volt modules must be connected in a series-parallel arrangement. The connection hierarchy selected for the (.6λ by .6λ) cavity radiator modules has four modules in parallel to form units called rows. Twelve rows are connected in series to form strings. Three strings in parallel make up a panel, which is the least replaceable unit. One hundred forty-four panels in a 12 x 12 series-parallel matrix form subarrays of the same size (10m x 10 m) as in the current baseline, with a subarray voltage drop of 2.16 kv. Two subarrays are connected in series to give a 4.32 kv distribution voltage.

In the case of subarrays using the slightly larger (.6λ x .8λ) dipole moduler the hierachy is the same except that the rows only have three modules in parallel.

A reliability assessment of the described cavity radiator module subarray hierarchy as a function of probability of amplifier failure, Q, is summarized in Figure 10. In case only one amplifier failure per row is permitted, string failures will cause 2% rf power reduction (with 50% probability) in 22 years for an amplifier MTBF of 3.5×10^6 hours. The random failures at this time cause an additional 0.8% of amplifiers to have failed so that the total rf power reduction at this time is 2.8%. If two amplifier failures per row are allowed, the power loss due to string failures of 2% and random amplifier failures of 3.2% together

result in a subarray power loss of 5.2% after 63 years. These results indicate that, for the SPS requirement of less than 2% rf converter failures in a 30 year period, the objectives of maintenance-free operation are achievable. This provides encouragement for further effort to address the issues of series-paralleling such large strings.

An additional reliability feature beyond those considered in the assessment of all the module designs for string protection is the use of an external high temperature resistor which is shunted in to dissipate the nominal module power when the power amplifier in a module becomes open-circuited. By making the resistors small filaments a visual indication of failure is provided.

Although the failure reliability aspects of the above series-parallel configuration appear workable, other valid questions remain. The modules each have separate inputs that must be kept from coupling to neighboring outputs over the power supply lines. This is believed feasible but has not yet been experimentally demonstrated. Also, in a real system startup and shutdown transients are experienced. There must be kept from "rattling around" in the series-parallel matrix and selectively blowing out modules. Protection against these transients is believed assured if all the modules present similar impedances to the power line and have some over-voltage protection.

5.0 SATELLITE CONFIGURATION

A trade study done to decide on the preferred power distribution system to the 4.32 kv subarray pairs from the solar array compared directly bussed DC, high voltage AC and high voltage DC with DC-DC convertors. The results are shown on Figure 11 in the form of conductor and power loss make-up array mass as a function of conductor temperature. Direct DC won out despite a low power bussing efficiency of .73. However, it should be noted that should power convertor technology improvements result in 25% power convertor mass reductions, high voltage DC with DC-DC convertors would be the preferred option.

Satellite efficiency and sizing, done in a fashion similar to the NASA/DOE reference SPS design, clearly shows the impact of the buss losses on Figure 12.

The completed 2.5 GW modified reference SPS configuration is shown on Figure 13. The technology of the non-microwave subsystems is the same as the reference except for elimination of the antenna yoke by using linear actuators between the antenna edge and the rotary platform and the use of a pentahedral main satellite bay structure. Both changes reduce satellite mass somewhat.

Figure 14 gives a mass and cost summary. Total mass per unit transmitted power is up 30% from the reference because of DC bussing and DC-microwave conversion inefficiencies, with costs tracking. A second pass through the design, concentrating on increasing power bussing efficiency to achieve mass reductions, might reduce this difference but it is unlikely to erase it.

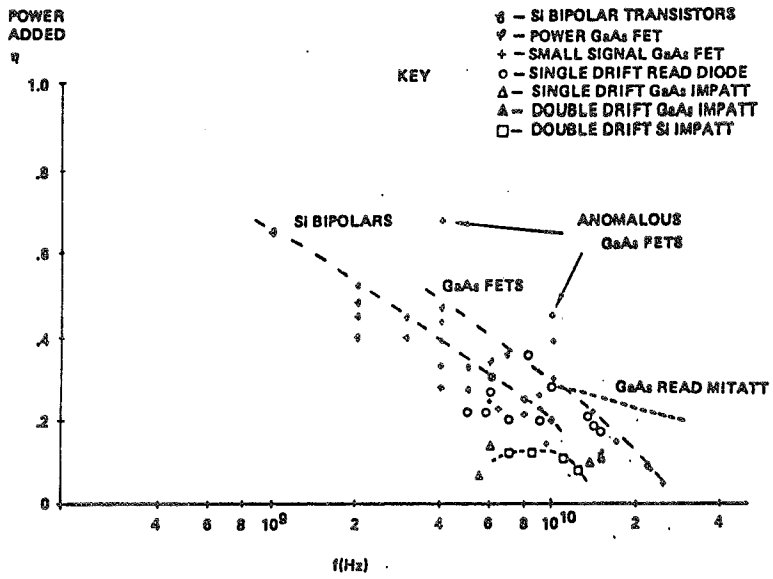

Figure 1. CW Solid State Device Efficiency vs Frequency—1978

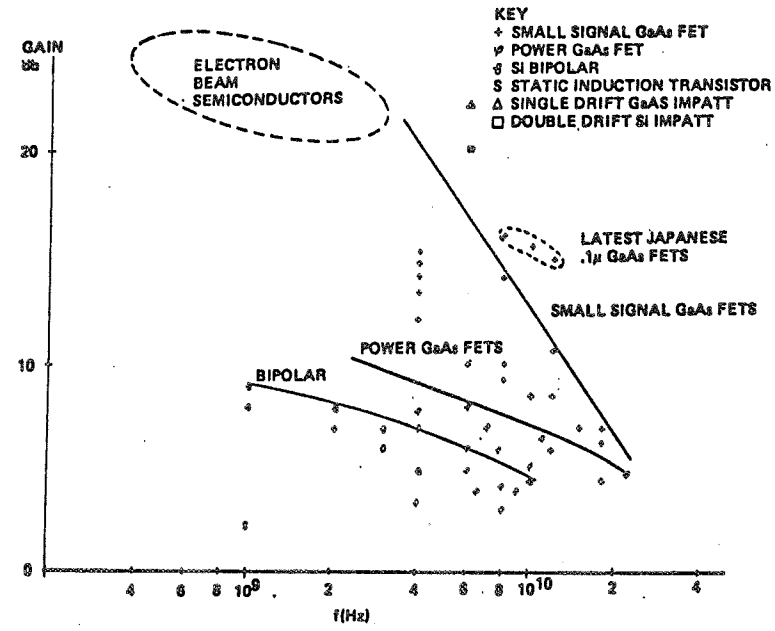

Figure 2. Solid State Device Gain vs Frequency—1978

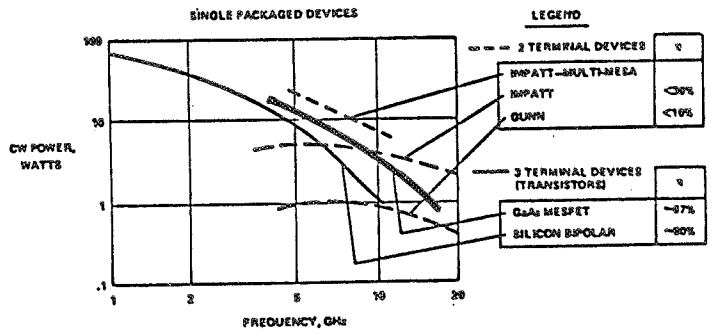

Figure 3. Solid State CW Power vs Frequency—1978

Figure 4. Characteristics of Various Amplifier Classes

Amplifier Class		Maximum Power-added Efficiency for Sine Wave Output	Typical Efficiency Values Achieved	@ Frequency	Duty Cycle at Maximum Efficiency	Active Device Saturated ?	Active Device Cut Off ?
	A	.5	.3	@ 4 GHz	1.0	No	No
	B	.785	.5	@ 4 GHz	.5	No	Yes
	C (Unsaturated)	.896	.6	@ 2.5 GHz	.3	No	Yes
Switched Mode Amplifiers	D	1.0	.9	@ 10 MHz	.5	Yes	Yes
	E	1.0	.9	@100 MHz	.5	Yes	Yes
	F	1.0	.9	@ 10 MHz	.5	Yes	Yes
	S	1.0	.8	@ 100 KHz	Variable >>1	Yes	Yes
	Multivoltage	1.0	.8	@ 10 MHz	Variable	Yes	Yes
	G	.818	.7	@ 100 KHz	Variable	Yes	Yes

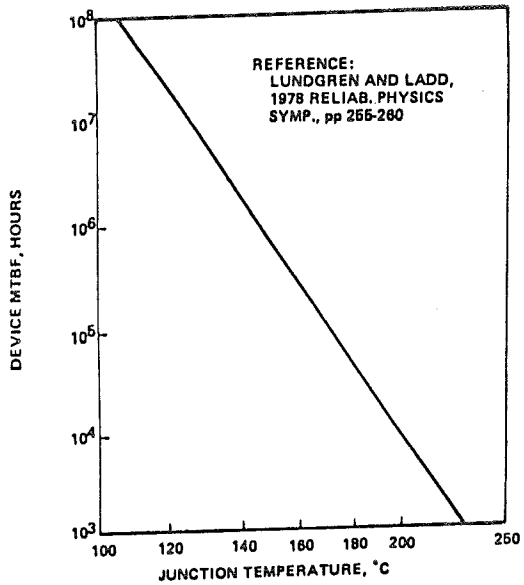

Figure 5. Small Signal GaAs FET Lifetime vs Junction Temperature

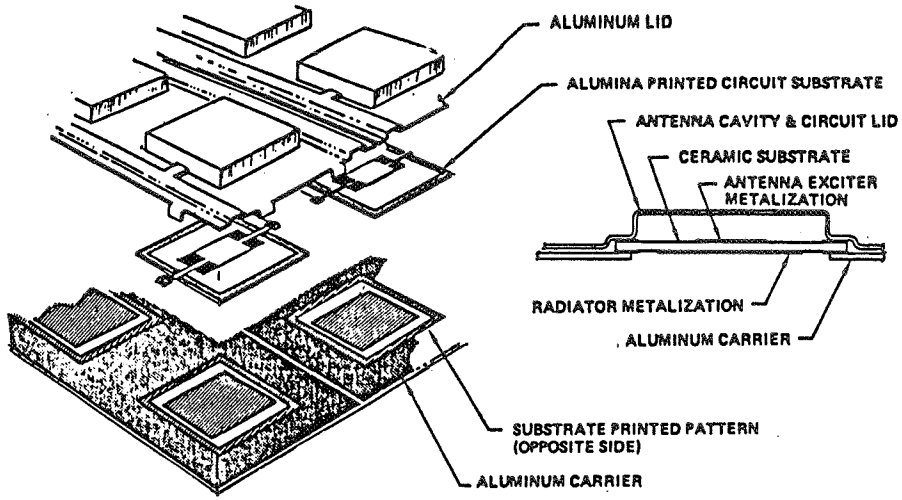

Figure 7. Solid State Combiner-Radiator Module

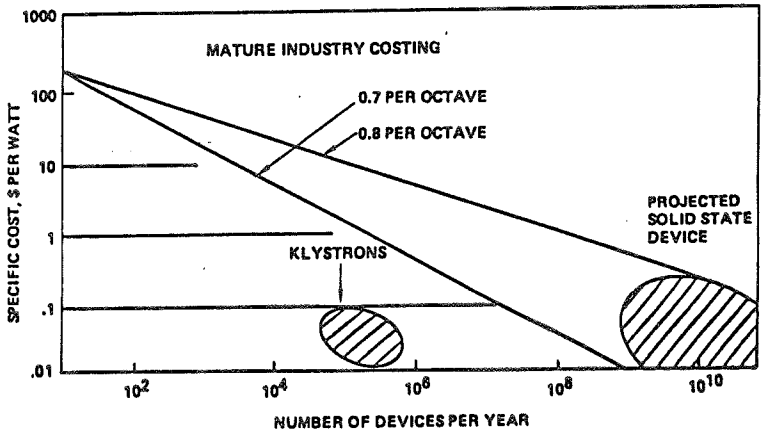

Figure 6. Projected GaAs FET Costs

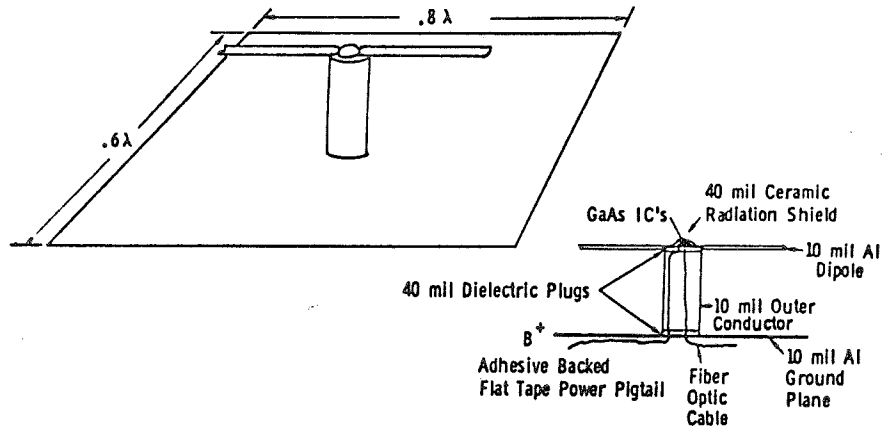

Figure 8. Solid State Dipole Radiator Module

STEP	OUTSIDE RADIUS (m)	STEP AREA (m^2)	NUMBER OF SUBARRAYS	MODULE TYPE	MODULE POWER (W)	$(P/A)_{RF}$ (Kwm^{-2}	$(M/P)_{RF}$ ($kg\ km^{-1}$)	STEP MODULE MASS (T)	NO. FETS (M)
1	124.8	48,970	456	High Power 4-FET, Cavity Radiator (4.06 kgm^{-2})	28.7	5.50	.742	200	37.82
2	249.6	146,830	1,360	"	24.0	4.45	.917	600	112.80
3	322.4	130,820	1,208	Reduced Power 4-FET Cavity Radiator (3.58 kgm^{-2})	19.2	3.56	1.006	468	100.20
4	384.8	138,640	1,280	"	16.0	2.97	1.207	496	108.17
5	457.6	192,680	1,784	2-FET Cavity Radiator (3.06 kgm^{-2})	12.8	2.37	1.289	590	73.99
6	520.0	191,680	1,776	2 FET Dipole (1.47 kgm^{-2})	12.8	1.78	.826	582	55.24
7	561.6	141,390	1,312	"	9.6	1.33	1.101	208	40.81
8	582.4	74,795	696	"	8.5	1.18	1.244	110	21.65
9	644.8	238,950	2,208	1 FET Dipole (1.47 kg m^{-2})	6.4	.89	1.652	351	34.34
10	707.2	264,880	2,448	"	4.3	.59	2.476	389	38.07
	TOTALS		14,528					3,694	621.09

Figure 9. Solid State Transmitting Antenna Quantization

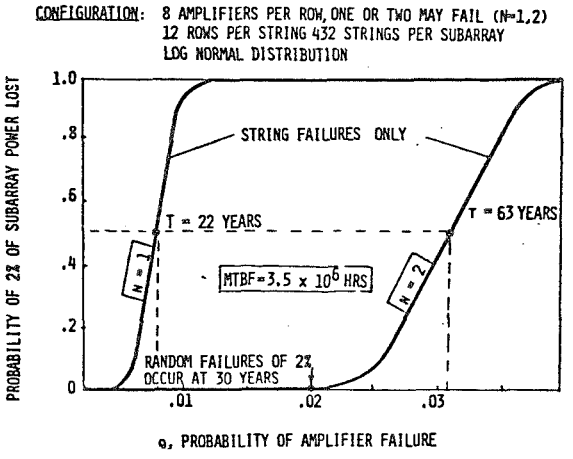

Figure 10. Solid State SPS Array Center Subarray Reliability

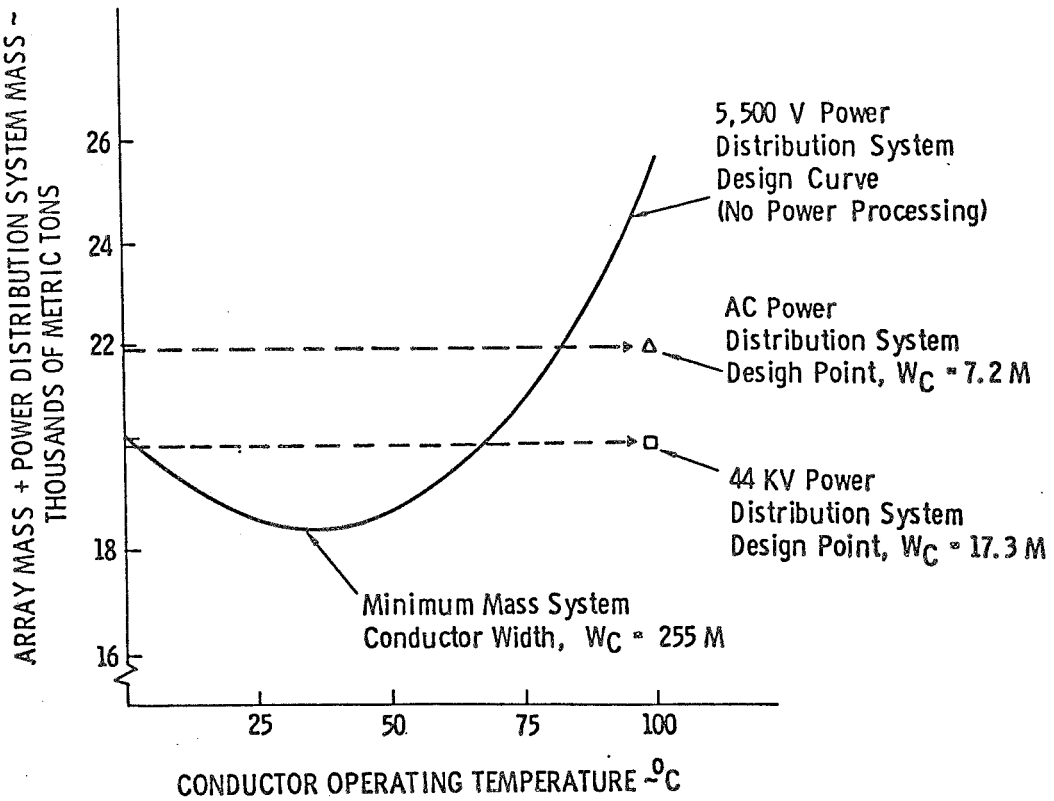

Figure 11. Power Distribution System Analysis

ITEM	EFFICIENCY	MEGAWATTS	
Array Mismatch			
Array Mismatch	.965	6050	Ideal Array Output
Main Bus I^2R	.729	5838	
Antenna Distr	.97	4256	Total Antenna Input
DC-RF Conversion	.8	4128	
Waveguide I^2R	N/A	3303	Total RF Radiated Power
Ideal Beam	.965	3303	
Inter-Subarray Losses	.976	3187	
Intra-Subarray Losses	N/A	3110	
Atmosphere Loss	.98	3110	
Intercept	.95	3048	
Rectenna RF-DC	.89	2896	Incident on Rectenna
Grid Interface	.97	2577	
	.413	2500 Net to Grid	

TOTAL ARRAY OUTPUT 6050 MW
TOTAL SOLAR ARRAY AREA = 33.8 km^2

Figure 12. Solid State SPS Efficiency and Sizing

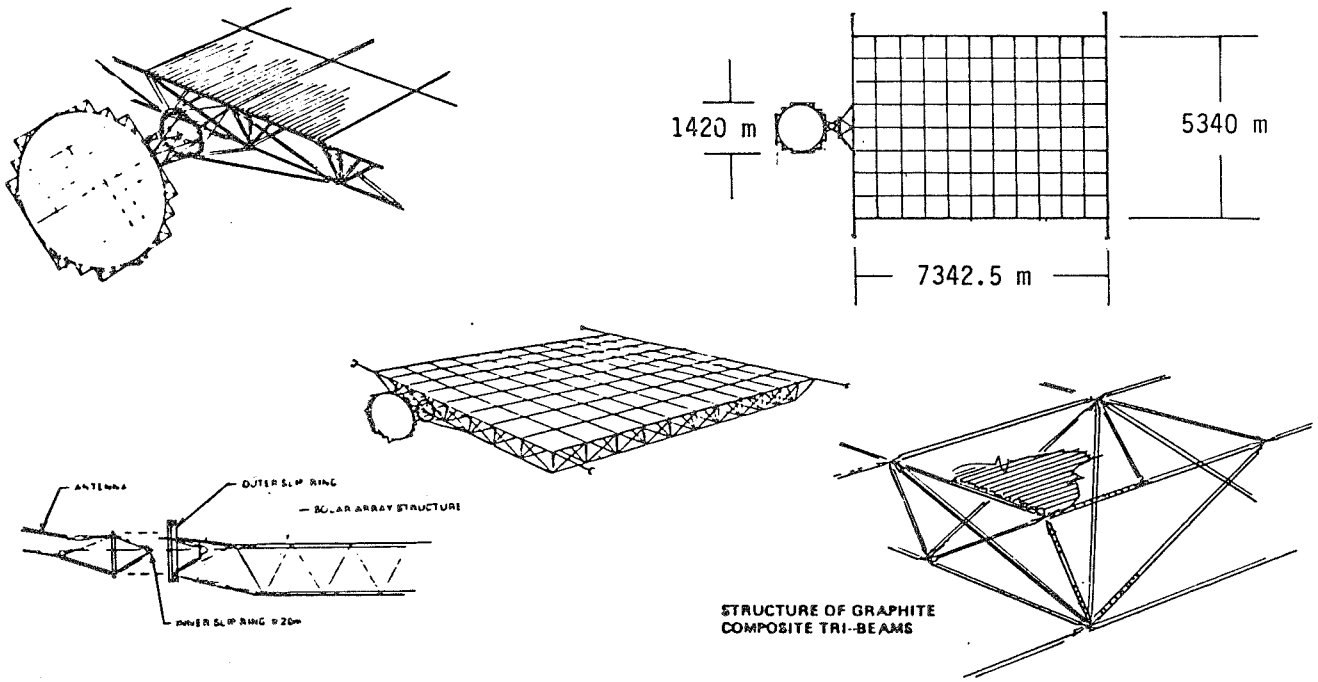

Figure 13. 2.5 Gw Solid State SPS Configuration

		MASS (MT)	ESTIMATING BASIS	(COST ($M)
1.1	SPS	35,204		4,541
1.1.1	ENERGY CONVERSION	22,087		2,350
1.1.1.1	STRUCTURE	2,851	Detailed Estimate	275
1.1.1.2	CONCENTRATORS	(0)	Not Required	(0)
1.1.1.3	SOLAR BLANKETS	14,409	Scaled from Reference	1,355
1.1.1.4	POWER DISTRIB.	4,400	Detailed Estimate	530
1.1.1.5	THERMAL CONTROL	(0)	Allocated to Subsystems	(0)
1.1.1.6	MAINTENANCE	427	Scaled from Reference	190
1.1.2	POWER TRANSMISSION	6,365		1,134.5
1.1.2.1	STRUCTURE	460	Scaled from Reference	38
1.1.2.2	TRANSMITTER SUBARRAYS	4,480	Detailed Estimate	888.5
1.1.2.3	POWER DISTR. & COND.	1,262	Scaled from 1.1.1.4	124
1.1.2.4	PHASE DISTR.	25	Scaled from Reference	51
1.1.2.5	MAINTENANCE	20	Docking Ports Only	20
1.1.2.6	ANTENNA MECH. POINTING	118	Scaled by Mass x Area	13
1.1.3	INFO MGMT & CONTROL	145	Scaled from Ref.	73
1.1.4	ATT. CONT. & STA. KP.	146	Scaled From Ref	110
1.1.5	COMMUNICATIONS	0.2	Same as Ref.	8
1.1.6	INTERFACE	113	Est. Based on Simplification	46.3
1.1.7	GROWTH & CONTINGY.	6,348	Same % as Reference	819

Figure 14. Solid State SPS Mass and Cost Summary